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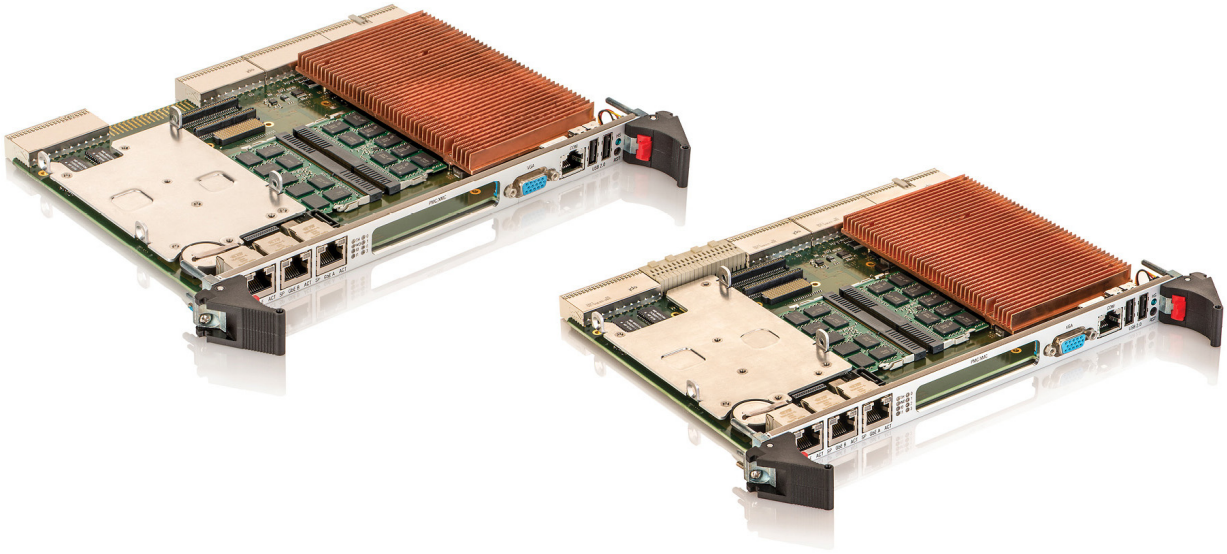
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» User Guide «



CP6005(X)-SA

Doc. ID: 1055-2501, Rev. 1.0

Date: December 20, 2013

Revision History

Revision	Brief Description of Changes	Date of Issue
1.0	Initial issue	20-Dec-2013

Imprint

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1 Introduction

1.1 Board Overview

The CP6005(X)-SA is a highly integrated 6U CompactPCI® processor board based on the 4th generation Intel® Core™ i7/i5 processor in combination with the Intel® QM87 Chipset. The CP6005-SA is a fully-compliant PICMG 2.16 processor board whereas the CP6005X-SA offers additional dual 10 Gigabit Ethernet and PCI Express to the backplane.

With the powerful, 4th generation quad-core Intel® Core™ i7 and dual-core Intel® Core™ i5 processors, the CP6005(X)-SA offers extraordinary performance-per-watt values and is an ideal backbone for powerful network-intensive applications providing virtualization (VT-X, VT-D) and highest graphics performance. The new-generation graphics controller has up to 40 execution units providing OpenCL 1.2/OpenGL 4.0 and triple independent display support. Five Gigabit Ethernet channels on the CP6005-SA provide well-weighted data throughput for external and internal PICMG® 2.16-compliant Ethernet traffic. The CP6005X-SA supports two additional 10 Gigabit Ethernet ports combined with x4 PCI Express® 2.0 via a rear I/O ZDplus connector, all based on PICMG® 2.20 for high bandwidth requirements.

The Intel® Advanced Vector Extensions AVX 2.0 enhancements provide a huge performance improvement in floating-point-intensive computations, which are a key part of digital signal and image processing applications such as medical imaging and radar or sonar.

Both PICMG 2.16-compliant CP6005-SA and CP6005X-SA processor boards offer up to 16 GB dual-channel 1600 MHz DDR3L ECC memory via two SODIMM sockets providing up to 25 GB/sec data throughput. Thanks to hot swap support and IPMI (PICMG 2.9-compliant Intelligent Platform Management Interface), the CPU board meets the highest demands for the management of high-availability applications. Many of these are data and telecommunications applications also including highly sensitive security-related solutions as well as image processing systems.

The Intel® QM87 Chipset provides advanced I/O technology including USB and Serial ATA channels for an onboard 2.5-inch SATA hard disk or SSD and an industrial-grade NAND Flash SSD device—all usable in a 4HP single slot. The highly integrated CP6005(X)-SA features also an XMC site according to XMC.3 supporting x8 PCI Express® (alternatively a 32-bit/66 MHz PCI PMC site) for various market available extensions. Based on the Kontron rear I/O concept, existing rear transition modules are fully functional on the CP6005-SA, where the CP6005X-SA provides additional 10 GbE and PCI Express on the backplane for communication between CompactPCI® slots. Appropriate backplanes and systems are available.

Delivering a stable product based on Intel®'s embedded product line, the CP6005(X)-SA ensures long term availability. This eliminates the risk of unplanned design changes and unexpected expensive application modification. While minimizing deployment risks, the CP6005(X)-SA provides a broad range of software support to ease the process of product integration and maximize the competitive advantage of meeting the time-to-market window.

The board is offered with various board support packages including Windows, VxWorks and Linux operating systems. For further information concerning the operating systems available for the CP6005(X)-SA, please contact Kontron.

1.2 System Expansion Capabilities

1.2.1 PMC Module

The CP6005(X)-SA has a 3.3 V, PMC mezzanine interface configurable for 32-bit / 66 MHz PCI operation. This interface supports a wide range of PMC modules with PCI interface including all of Kontron's PMC modules and provides an easy and flexible way to configure the CP6005(X)-SA for various application requirements. For information on the PMC interface, refer to Chapter 2.7.7, "PMC Interface".

1.2.2 XMC Module

The CP6005(X)-SA has one XMC mezzanine interface for support of x1, x4 and x8 PCI Express 2.0 XMC modules providing an easy and flexible way to configure the CP6005(X)-SA for various application requirements. For information on the XMC interface, refer to Chapter 2.7.8, "XMC Interface".

1.2.3 CP6005(X)-SA-MK2.5SATA Assembly Kit

The CP6005(X)-SA comes with an optional CP6005(X)-SA-MK2.5SATA assembly kit comprised of one MMADP-SATA01 module and the necessary components needed for mounting the module on the CP6005(X)-SA. The MMADP-SATA01 module is required for connecting an onboard 2.5" SATA HDD or SSD to the CP6005(X)-SA via an onboard SATA extension connector. For further information concerning the MMADP-SATA01 module, refer to Chapter 6.

1.2.4 SATA Flash Module

The CP6005(X)-SA provides support for up to 64 GB NAND flash memory in combination with an optional SATA Flash module, which is connected to the CP6005(X)-SA via an onboard SATA extension connector. For further information concerning the SATA Flash module, refer to Chapter 7.

1.2.5 Rear I/O Module

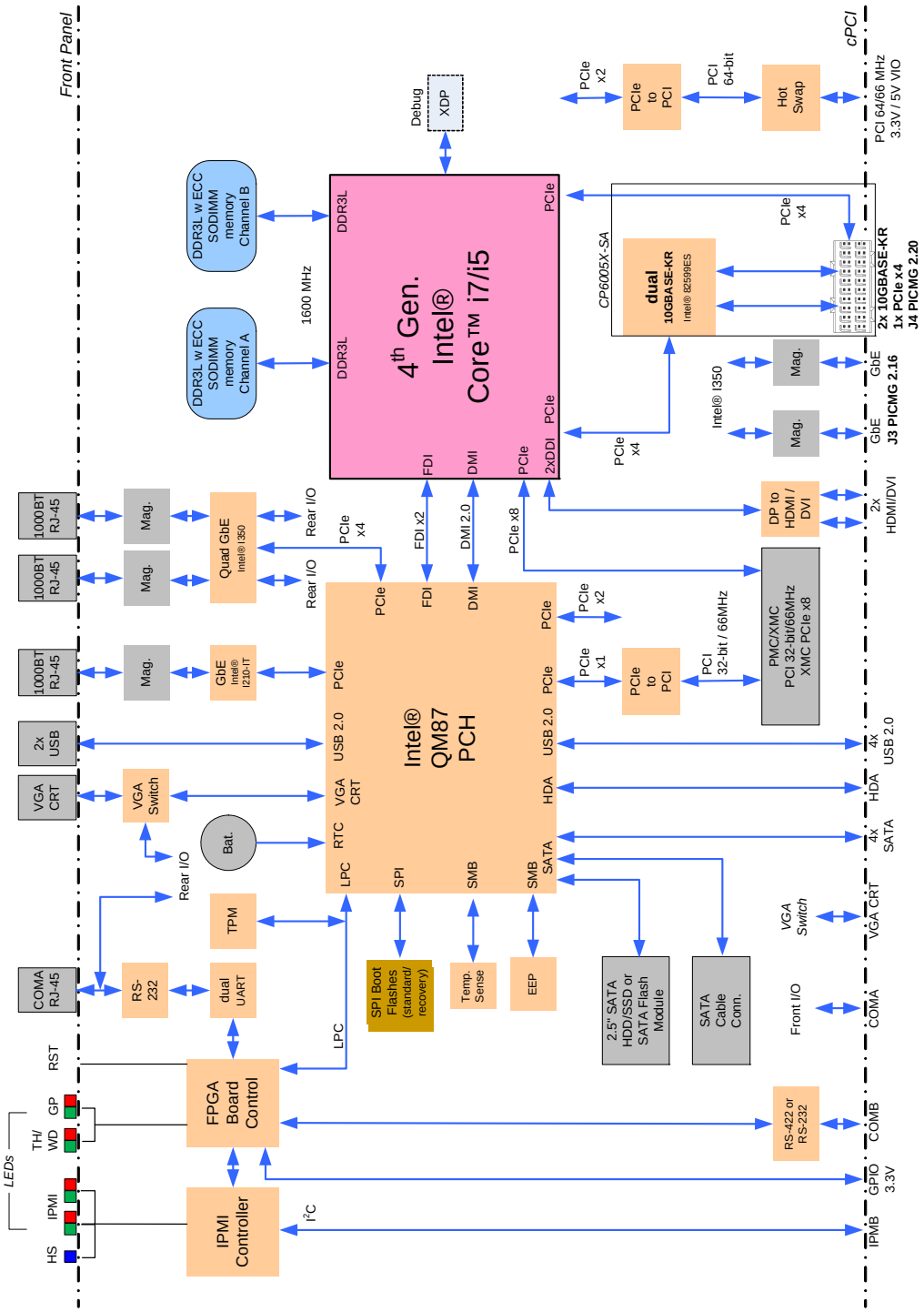
The CP6005(X)-SA provides support for one rear I/O module via the CompactPCI rear I/O connectors. For further information about the compatibility of rear I/O modules with the CP6005(X)-SA, refer to the CP6005(X)-SA datasheet.

1.3 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

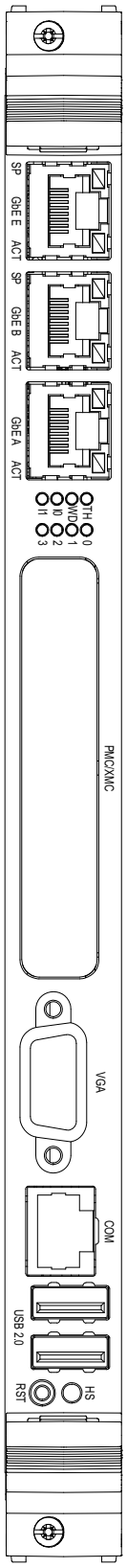
1.3.1 Functional Block Diagram

Figure 1: CP6005(X)-SA Functional Block Diagram



1.3.2 Front Panel

Figure 2: 4 HP CP6005(X)-SA Front Panel



IPMI LEDs

I0/I1 (red/green): Indicate the software status of the IPMI controller

System Status LEDs

HS (blue): Hot Swap Status
TH (red/green): Temperature Status
WD (green): Watchdog Status

General Purpose LEDs

LED3–0 (red/green/amber): General Purpose / POST Code

Note: If the General Purpose LEDs 3–0 are lit red during boot-up, a failure is indicated before the uEFI BIOS has started.

Integral Ethernet LEDs

ACT (green): Ethernet Link/Activity
SPEED (orange): 1000BASE-T Ethernet Speed
SPEED (green): 100BASE-TX Ethernet Speed
SPEED (off) + ACT (on): 10BASE-T Ethernet Speed

1.3.3 Board Layout

Figure 3: 4 HP CP6005-SA Board Layout (Top View)

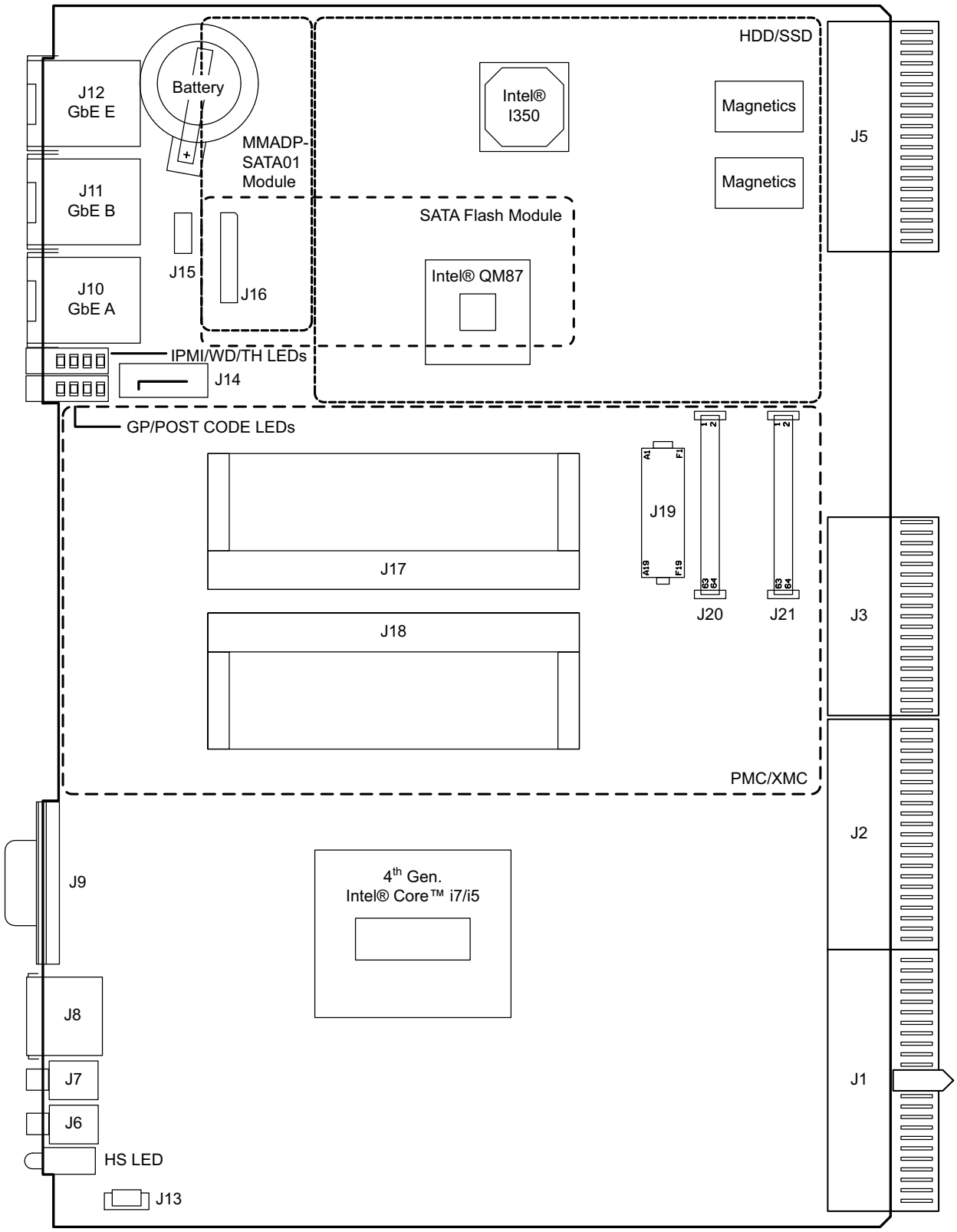


Figure 4: 4 HP CP6005X-SA Board Layout (Top View)

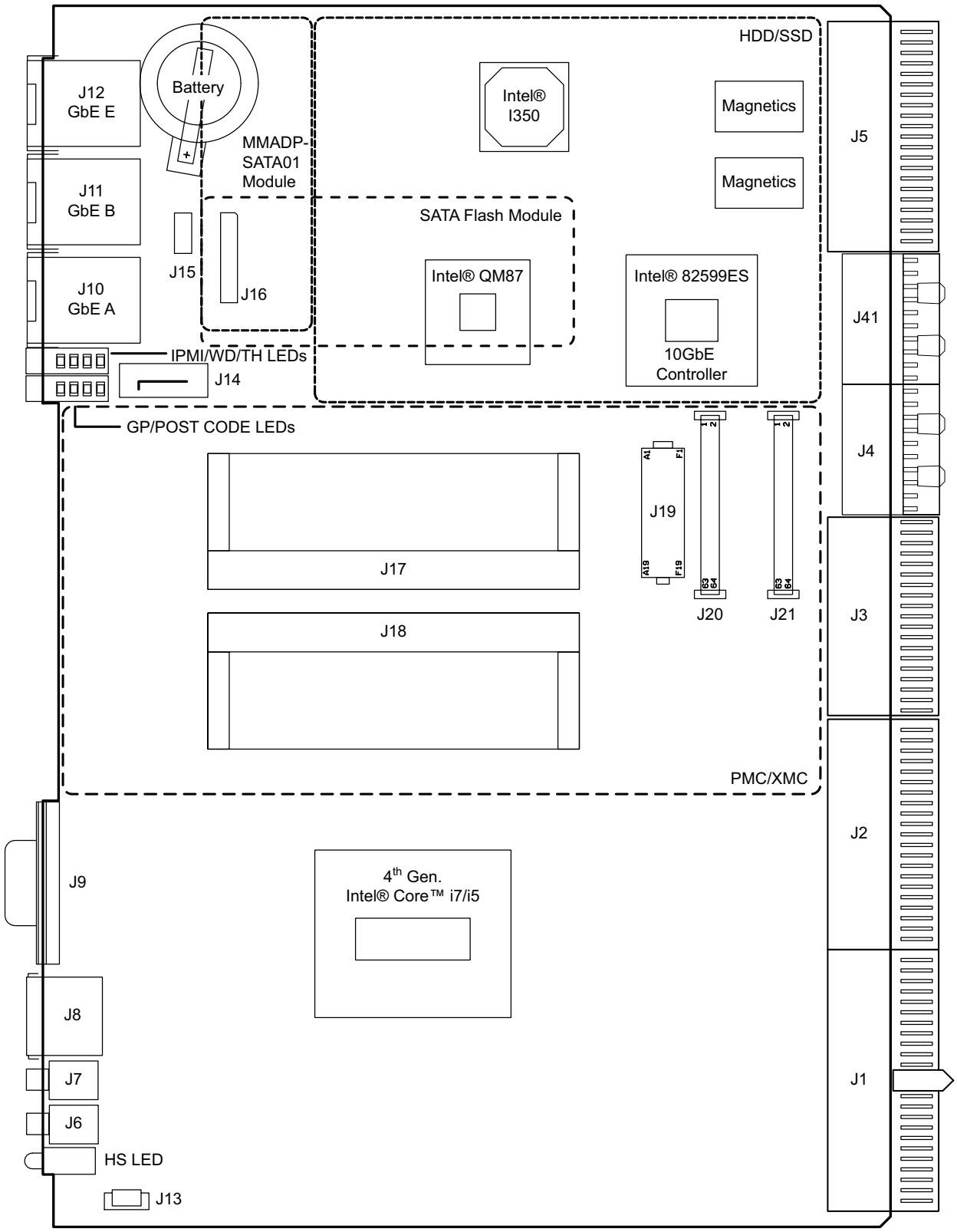
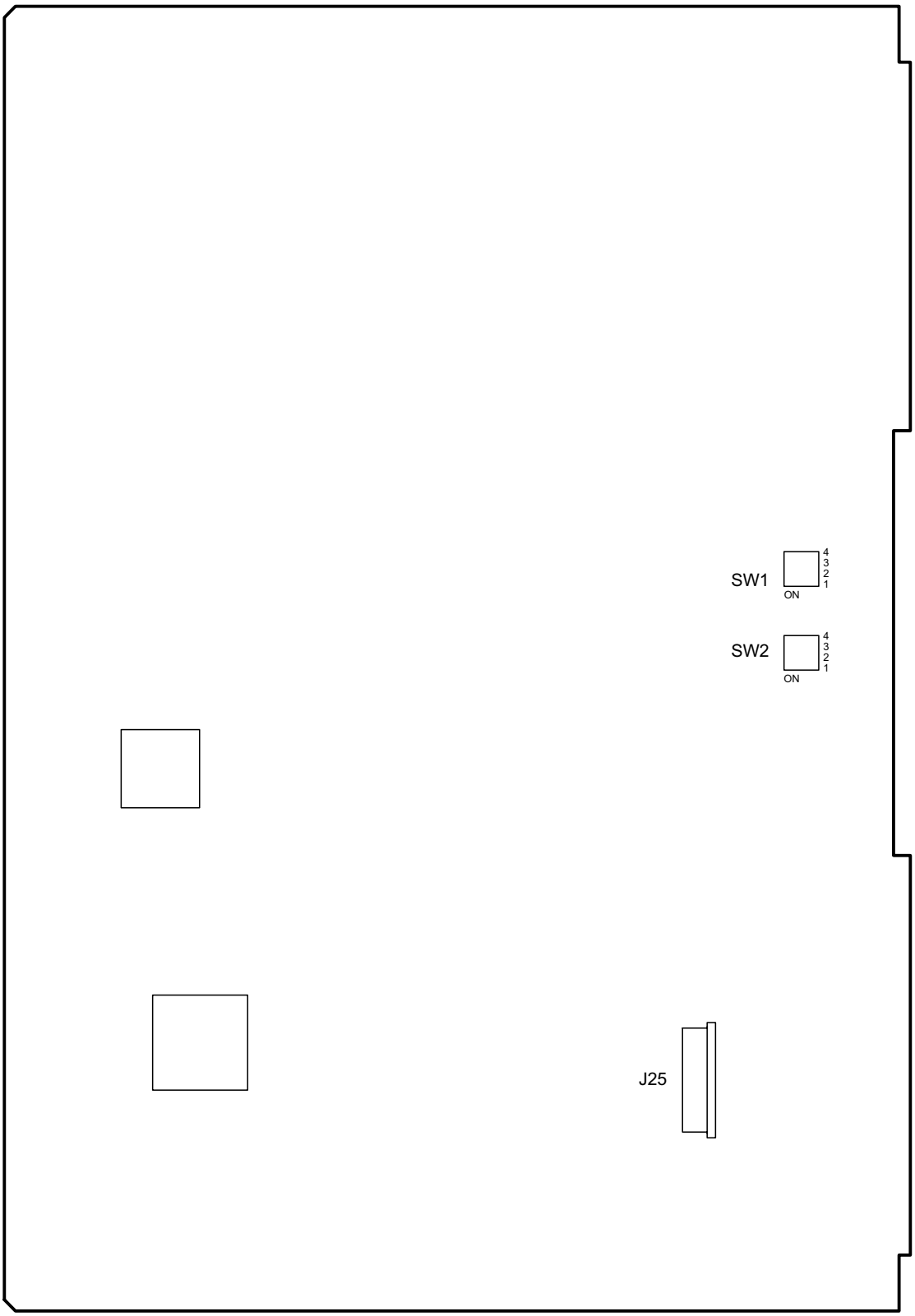


Figure 5: 4 HP CP6005(X)-SA Board Layout (Bottom View)



1.4 Technical Specification

Table 1: CP6005(X)-SA Main Specifications

FEATURES		SPECIFICATIONS
Processor & Chipset	CPU & Graphics Controller	The CP6005(X)-SA supports the following 4th generation processors: » Quad-core Intel® Core™ i7-4860EQ (SV), 1.8 GHz, 6 MB L3 cache, GT3e, Intel® Iris™ Pro Graphics 5200 » Quad-core Intel® Core™ i7-4700EQ (SV), 2.4 GHz, 6 MB L3 cache, GT2, Intel® HD Graphics 4600 » Dual-core Intel® Core™ i5-4400E (SV), 2.7 GHz, 3 MB L3 cache, GT2, Intel® HD Graphics 4600
	PCH	Intel® QM87 Chipset
Memory	Main Memory	Up to 16 GB, dual-channel DDR3 SDRAM memory with ECC running at 1600 MHz on two SODIMM sockets
	Flash Memory	Two 16 MB SPI boot flash chips for two separate uEFI BIOS images Up to 64 GB SLC NAND flash via an onboard SATA Flash module (SSD)
	EEPROM	EEPROM with 64 kbit
Interfaces	CompactPCI	CompactPCI interface: » Compliant with CompactPCI Specification PICMG 2.0 R 3.0: » System controller operation » 64-bit / 66 MHz PCI or PCI-X master interface with dedicated PCIe-to-PCI-X bridge » 3.3V or 5V signaling levels (universal signaling support) » Compliant with the Packet Switching Specification PICMG 2.16. The CP6005(X)-SA supports System Master hot swap functionality and application-dependent hot swap functionality when used in a peripheral slot. When used as a System Master, the CP6005(X)-SA supports individual clocks for each slot and the ENUM signal handling is in compliance with the PICMG 2.1 Hot Swap Specification. When installed in a peripheral slot, the CP6005(X)-SA is isolated from the CompactPCI bus. It receives power from the backplane and supports rear I/O and, if the system supports it, packet switching (in this case up to two channels of Gigabit Ethernet).
	Standard Rear I/O	The following interfaces are routed to the rear I/O connectors J3 and J5. COMA (RS-232 signaling) and COMB (RS-232 signaling); no buffer on the rear I/O module is necessary » 4 x USB 2.0 » 1 x CRT VGA, 2 x HDMI/DVI » 1 x HDA » 2 x Gigabit Ethernet (compliant with PICMG 2.16, R 1.0) » 4 x SATA 3 Gb/s » 4 x GPIs and 4 GPOs (LVTTL signaling) » System write protection

Table 1: CP6005(X)-SA Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Interfaces	High-Speed Serial Rear I/O Interconnection (CP6005X-SA)	The following interfaces are provided on the rear I/O via two ZDplus high-speed connectors, J4 and J41 (PICMG 2.20): » Two 10GBASE-KR interfaces » One x4 PCI Express 2.0 operating at 5 GT/s as a root complex controller only The port mapping of the high-speed serial rear I/O interconnection on the CP6005(X)-SA is capable of supporting two 10GBASE-KR/40GBASE-KR4 interfaces, one x8 PCI Express 3.0 operating at 8 GT/s, and two SATA 6 Gb/s ports. However, the current implementation provides support for only two 10GBASE-KR and one x4 PCI Express 2.0 operating at 5 GT/s.
	10 Gigabit Ethernet (CP6005X-SA)	Two 10GBASE-KR interfaces for high-speed serial rear I/O interconnection based on the Intel® 82599ES dual-port 10 Gigabit Ethernet controller
	Gigabit Ethernet	Five 10 Base-T/100 Base-TX/1000 Base-T Gigabit Ethernet interfaces based on one Intel® I210-IT Gigabit Ethernet controller and one Intel® I350 quad-port Gigabit Ethernet controller: » Three RJ-45 connectors on the front panel » Two ports on the rear I/O (PICMG 2.16)
	USB	Six USB ports supporting UHCI (USB 1.1) and EHCI (USB 2.0): » Two type A USB 2.0 connectors on the front panel » Four USB 2.0 ports on the rear I/O interface
	Serial	Two 16C550-compatible UARTs: » One RS-232 port on the front panel and routed to rear I/O, COMA » One RS-232 port on the rear I/O, COMB
	XMC	XMC interface: » One onboard XMC connector for connecting a standard XMC module » Up to x8 PCI Express 2.0 ports operating at 5 GT/s (up to x8 PCI Express 3.0 operating at 8 GT/s on request)
	SATA	» Two SATA 6 Gb/s interfaces for: » Up to 64 GB flash memory via an onboard SATA Flash module, or » Onboard 2.5" HDD / SSD is supported in combination with the MMADP-SATA01 module » One standard SATA 6 Gb/s interface for the standard SATA connector » Four SATA 3 Gb/s ports accessible via rear I/O » High-performance RAID 0/1/5/10 functionality on all SATA ports
Sockets	Front Panel Connectors	» VGA: one 15-pin, D-Sub connector, J9 » USB: two 4-pin, type A connectors, J6 and J7 » Ethernet: three 8-pin, RJ-45 connectors, J10, J11 and J12 » Serial port: one 8-pin, RJ-45 connector, J8 (COMA) » XMC front panel bezel cutout

Table 1: CP6005(X)-SA Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Sockets	Onboard Connectors	» One XMC connector, J19 (P15) » Two SATA connectors » One 7-pin, standard SATA connector, J14 » One 34-pin, SATA extension connector, J16 » One JTAG connector, J15 » One XDP-SFF (debug) connector, J25 » Four CompactPCI connectors J1, J2, J3 and J5 » Two ZDplus high-speed serial rear I/O connectors, J4 and J41 (PICMG 2.20) (CP6005X-SA) » Two 204-pin DDR3L SODIMM sockets, J17 and J18
LEDs	Front Panel LEDs	IPMI LEDs: » IO/I1 (red/green): Software status of the IPMI controller System Status LEDs: » WD (green): Watchdog status » TH (red/green): Temperature status » HS (blue): Hot swap status General Purpose LEDs: » LED3–0 (red/green/amber): General purpose / POST code Ethernet LEDs: » ACT (green): Network link / activity » SPEED (green/orange): Network speed
Switches	DIP Switches	Two onboard DIP switches, SW1 and SW2 for board configuration on the rear side of the board
	Reset Switch	One hardware reset switch on the front panel
	Hot Swap Switch	One switch for hot swap purposes integrated in the front panel in accordance with PICMG 2.1 Rev. 2.0
Timer	Real-Time Clock	Real-time clock with 256 Byte CMOS RAM; battery-backup available
	Watchdog Timer	Software-configurable, two-stage Watchdog with programmable timeout ranging from 125 ms to 4096 s in 16 steps Serves for generating IRQ or hardware reset
	System Timer	The Intel® QM87 Chipset contains three 8254-style counters with fixed uses. In addition to the three 8254-style counters, the Intel® QM87 Chipset includes eight individual high-precision event timers that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register.
IPMI	IPMI Controller	NXP® ARM7 microcontroller with 512 kB firmware flash and automatic rollback strategy The IPMI controller carries out IPMI commands such as monitoring several onboard temperature conditions, board voltages and the power supply status, and managing hot swap operations. The IPMI controller is accessible via two IPMBs, one host Keyboard Controller Style (KCS) Interface and up to four Gigabit Ethernet Interfaces (IOL).

Table 1: CP6005(X)-SA Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Thermal	Thermal Management	CPU and board overtemperature protection is provided by: » Temperature sensors integrated in the 4th gen. Intel® Core™ i7/i5 processor: » One temperature sensor for monitoring each processor core » One temperature sensor for monitoring the graphics core » One temperature sensor for monitoring the package die temperature » One temperature sensor integrated in the Intel® QM87 Chipset for monitoring the chipset » One onboard temperature sensor for monitoring the board temperature » Specially designed heat sink
Security	TPM	Trusted Platform Module (TPM) 1.2 for enhanced hardware- and software-based data and system security
Software	uEFI BIOS	Phoenix SecureCore Tiano™ (SCT) BIOS firmware based on the uEFI Specification and the Intel Platform Innovation Framework for EFI: » LAN boot capability for diskless systems (standard PXE) » Automatic fail-safe recovery in case of a damaged image » Non-volatile storage of setting in the SPI boot flash (battery only required for the RTC) » Compatibility Support Module (CSM) providing legacy BIOS compatibility based on Phoenix SCT3 » Command shell for diagnostics and configuration » uEFI Shell commands executable from mass storage device in a pre-OS environment (open interface)
	IPMI Firmware	IPMI firmware providing the following features: » Keyboard Controller Style (KCS) interface » Dual-port IPMB interface for out-of-band management and sensor monitoring » IPMI over LAN (IOL) and Serial over LAN (SOL) support » Sensor Device functionality with configurable thresholds for monitoring board voltages, CPU state, board reset, etc. » FRU Inventory functionality » System Event Log (SEL), Event Receiver functionalities » Sensor Data Record Repository (SDRR) functionality » IPMI Watchdog functionality (power-cycle, reset) » Board monitoring and control extensions: » Graceful shutdown support » uEFI BIOS fail-over control: selection of the SPI boot flash (standard/recovery) » Field-upgradeable IPMI firmware: » via the KCS, IPMB or IOL interfaces » Download of firmware does not break the currently running firmware or payload activities » Two flash banks with rollback capability: manual rollback or automatic in case of upgrade failure
	Operating Systems	There are various operating systems available for the CP6005(X)-SA. For further information, please contact Kontron.

Table 1: CP6005(X)-SA Main Specifications (Continued)

FEATURES		SPECIFICATIONS
General	Power Consumption	See Chapter 4 for details.
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +70°C Extended Storage: -40°C to +85°C Without hard disk and without battery
	Battery	3.0 V lithium battery for RTC with battery socket Battery type: UL-approved CR2025 Temperature ranges: Operational (load): -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage (no load): -40°C to +70°C typical
	Climatic Humidity	93% RH at 40 °C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	233.35 mm x 160 mm 6U, 4 HP, CompactPCI Serial-compliant form factor
	Board Weight	CP6005-SA with heat sink: 778 grams CP6005X-SA with heat sink: 796 grams The above-mentioned board weight refers to the CP6005(X)-SA without extension modules such as the SATA Flash module or the MMADP-SATA01 module.

1.5 Standards

This product complies with the requirements of the following standards.

Table 2: Standards

TYPE	ASPECT	STANDARD
CE	Emission	EN55022, EN61000-6-3
	Immission	EN55024, EN61000-6-2
	Electrical Safety	EN60950-1
Mechanical	Mechanical Dimensions	IEEE 1101.10
Environmental	Climatic Humidity	IEC60068-2-78 (see note below)
	WEEE	Directive 2002/96/EC Waste electrical and electronic equipment
	RoHS 2	Directive 2011/65/EU Restriction of the use of certain hazardous substances in electrical and electronic equipment

In addition, boards ordered with the ruggedized service comply with the following standards as well.

Table 3: Additional Standards for Boards Ordered with Ruggedized Service

TYPE	ASPECT	STANDARD	REMARKS
Environmental	Vibration (Sinusoidal)	IEC60068-2-6	Ruggedized version test parameters: 10-300 (Hz) frequency range 2 (g) acceleration 1 (oct/min) sweep rate 10 cycles/axis 3 axes
	Single Shock	IEC60068-2-27	Ruggedized version test parameters: 30 (g) acceleration 9 (ms) shock duration half sine 3 number of shocks per direction (total: 18) 6 directions 5 (s) recovery time
	Permanent Shock	IEC60068-2-29	Ruggedized version test parameters: 15 (g) acceleration 11 (ms) shock duration half sine 500 number of shocks per direction 6 directions 5 (s) recovery time

Note: Customers desiring to perform further environmental testing of the CP6005(X)-SA must contact Kontron for assistance prior to performing any such testing.

Boards **without conformal coating** must not be exposed to a change of temperature which can lead to condensation. Condensation may cause irreversible damage, especially when the board is powered up again.

Kontron does not accept any responsibility for damage to products resulting from destructive environmental testing.

1.6 Related Publications

The following publications contain information relating to this product.

Table 4: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems	PICMG 2.0, Rev. 3.0 CompactPCI Specification PICMG 2.16, Rev. 1.0 CompactPCI Packet Switching Backplane Specification PICMG 2.20, Rev. 1.0 CompactPCI Packet Serial Mesh Backplane Specification PICMG 2.9, Rev. 1.0 CompactPCI System Management Specification PICMG 2.1, Rev. 2.0 CompactPCI Hot Swap Specification
	IPMI - Intelligent Platform Management Interface Specification v2.0
	Kontron CompactPCI Backplane Manual, ID 24229
XMC Module	ANSI/VITA 42.0-200x XMC Switched Mezzanine Card Auxiliary Standard ANSI/VITA 42.3-2006 XMC PCI Express Protocol Layer Standard IEEE 1386-2001, IEEE Standard for a Common Mezzanine Card (CMC) Family
Platform Firmware	Unified Extensible Firmware Interface (uEFI) Specification, Version 2.1
All Kontron products	Product Safety and Implementation Guide, ID 1021-9142

2 Functional Description

2.1 Processor and Chipset

The CP6005(X)-SA supports the Intel® Core™ i7-4860EQ, the Intel® Core™ i7-4700EQ (SV), and the Intel® Core™ i5-4400E processors in combination with the mobile Intel® QM87 Express Chipset.

Table 5: Features of the Processors Supported on the CP6005(X)-SA

FEATURE	Intel® Core™ i7-4860EQ (SV), 1.8 GHz	Intel® Core™ i7-4700EQ (SV), 2.4 GHz	Intel® Core™ i5-4400E (SV), 2.7 GHz
Processor Cores	four	four	two
Processor Base Frequency (HFM)	1.8 GHz	2.4 GHz / 1.7 GHz	2.7 GHz
Maximum Turbo Frequency	3.2 GHz	3.2 GHz	3.3 GHz
LFM	800 MHz	800 MHz	800 MHz
Hyper-Threading	supported	supported	supported
SpeedStep®	supported	supported	supported
L1 cache per core	64 kB	64 kB	64 kB
L2 cache per core	256 kB	256 kB	256 kB
L3 cache	6 MB	6 MB	3 MB
On-package cache	up to 128 MB	--	--
DDR3L Memory	up to 16 GB / 1600 MHz	up to 16 GB / 1600 MHz	up to 16 GB / 1600 MHz
Graphics	Intel® Iris™ Pro Graphics 5200	Intel® HD Graphics 4600	Intel® HD Graphics 4600
Graphics Base Frequency	750 MHz	400 MHz	400 MHz
Graphics Max. Dynamic Frequency	1.0 GHz	1.0 GHz	900 MHz
Graphics Execution Units	40	20	20
Configurable Thermal Design Power	--	cTDP	--
Power Limit Reduction	Power Limit Reduction	--	Power Limit Reduction
Thermal Design Power	47 W	47 W / 37 W	37 W

Note: The Intel® Core™ i7-4700EQ processor supports the cTDP-Down mode to 37 W. The maximum power consumption of the Intel® Core™ i7-4860EQ and Intel® Core™ i5-4400E processors can be reduced to approx. 10 W using the Power Limit Reduction feature. This feature can be configured via the **kBoardConfig** uEFI Shell command. For information on this command, refer to the Chapter 9, uEFI BIOS.

For further information about the processors used on the CP6005(X)-SA, please visit the Intel website. For further information concerning the suitability of other Intel processors for use with the CP6005(X)-SA, please contact Kontron.

2.1.1 Integrated Processor Graphics Controller

The 4th gen. Intel® Core™ i7/i5 processor includes a highly integrated processor graphics controller with up to 40 execution units delivering high-performance 3D, 2D graphics capabilities. The integrated processor graphics controller has three independent display interfaces allowing for support of multiple display configurations and provides three digital ports capable of driving the following resolutions:

- VGA CRT: up to 1920 x 2000 pixels @ 60 Hz
- HDMI: up to 4096 x 2304 pixels @ 24 Hz / 2560 x 1600 pixels @ 60 Hz
- DVI: up to 1920 x 1200 pixels @ 60 Hz

2.2 Memory

The CP6005(X)-SA supports a dual-channel (72-bit) DDR3L SDRAM memory with Error Checking and Correcting (ECC) running at 1600 MHz. It provides two 204-pin sockets for two DDR3L ECC SODIMM modules that support up to 16 GB system memory. The maximum memory size per channel is 8 GB.

The available memory module configuration can be either 4 GB, 8 GB or 16 GB. However, when the internal processor graphics controller is enabled, the amount of memory available to applications is less than the total physical memory in the system. The chipset's Dynamic Video Memory Technology, for example, dynamically allocates the proper amount of system memory required by the operating system and the application.

Note: Only qualified DDR3L ECC SODIMM modules from Kontron are authorized for use with the CP6005(X)-SA. Replacement of the SODIMM modules by the customer without authorization from Kontron will void the warranty.

2.3 Watchdog Timer

The CP6005(X)-SA provides a Watchdog timer that is programmable for a timeout period ranging from 125 ms to 4096 s in 16 steps.

The Watchdog timer provides the following modes or operation:

- Timer-only mode
- Reset mode
- Interrupt mode
- Dual-stage mode

In dual-stage mode, a combination of both interrupt and reset is generated if the Watchdog is not serviced.

2.4 Battery

The CP6005(X)-SA is provided with an UL-approved CR2025, 3.0 V, "coin cell" lithium battery for the RTC. When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CP6005(X)-SA.

2.5 Flash Memory

The CP6005(X)-SA provides flash interfaces for the uEFI BIOS and the SATA Flash module.

2.5.1 SPI Boot Flash for uEFI BIOS

The CP6005(X)-SA provides two 8 MB SPI boot flashes for two separate uEFI BIOS images, a standard SPI boot flash and a recovery SPI boot flash. The fail-over mechanism for the uEFI BIOS recovery can be controlled via the DIP switch SW1, switch 2. The SPI boot flash includes a hardware write protection option, which can be configured via the uEFI BIOS. If write protection is enabled, the SPI boot flash cannot be written to.

Note: The uEFI BIOS code and settings are stored in the SPI boot flashes. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash. Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

2.5.2 SATA Flash Module

The CP6005(X)-SA supports up to 64 GB flash memory in combination with an optional SATA Flash module. The SATA Flash module cannot be used in conjunction with the MMADP-SATA01 Module.

2.6 Trusted Platform Module 1.2

The CP6005(X)-SA supports the Trusted Platform Module (TPM) 1.2. TPM1.2 is a security chip specifically designed to provide enhanced hardware- and software-based data and system security. TPM1.2 is based on the Atmel AT97SC3204 security controller and stores sensitive data such as encryption and signature keys, certificates and passwords, and is able to withstand software attacks to protect the stored information.

2.7 Board Interfaces

2.7.1 Front Panel LEDs

The CP6005(X)-SA provides three system status LEDs, one Hot Swap Status LED (HS LED), one temperature status LED (TH LED) and one Watchdog status LED (WD LED), as well as two IPMI LEDs (I0 and I1) and four General Purpose/POST code LEDs (LED3–0). Their functionality is described in the following chapters and reflected in the registers mentioned in Chapter 3, Configuration.

2.7.1.1 Watchdog and Temperature Status LEDs

Table 6: Watchdog and Temperature Status LEDs' Functions

LED	COLOR	STATE	FUNCTION
TH LED	red / green	Off	Power failure
		Green	Board in normal operation
		Red	CPU has reached maximum allowable operating temperature and the performance has been reduced
		Red blinks	CPU temperature above 125°C (CPU has been shut off) In this event, all General Purpose LEDs (LED3–0) are blinking red as well.
WD LED	red / green	OFF	Watchdog inactive
		Green	Watchdog active, waiting to be triggered
		Red	Watchdog expired

Note: If the TH LED flashes red at regular intervals, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur and the processor has been shut off. To turn to normal operation, the power must be switched off and then on again.

2.7.1.2 IPMI LEDs and HS LED

The IPMI LEDs I0 and I1 show the software status of the IPMI controller. The Hot Swap LED (HS LED) indicates when the board may be extracted. It can be switched on or off by software and may be used, for example, to indicate that the shutdown process is finished and the board is ready for extraction.

Table 7: IPMI and HS LEDs' Functions

LED	COLOR	STATE	FUNCTION
I0 (right)	red	Off	IPMI controller running
		On	IPMI controller out of service or in reset state
		Blinking	IPMI controller firmware upgrade
	green	Pulsing	Traffic on the IPMB bus
I1 (left)	red	On	Health error detected
	red/amber	Blinking	Health error detected, IPMI controller running showing its heart beat
		Pulsing	Health error detected, KCS interface active
	green	Off	No health error detected
		Pulsing	KCS interface active
		Blinking	IPMI controller running showing its heart beat
HS LED	blue	Off	Board in normal operation Do not extract the board.
		Blinking	Board hot swap in progress Board is not ready for extraction. Do not actuate the hot swap handle. Blinking pattern: a) Long on, short off: the IPMI controller starts the payload b) Long off, short on: the IPMI controller shuts down the payload Wait until the HS LED stops blinking and remains on to extract the board.
		On	a) Board ready for hot swap extraction, or b) Board has just been inserted in a powered system

Note: The status of the IPMI-controlled LEDs (I0, I1, and HS LED) may be temporarily overwritten by the PICMG-defined "Set FRU LED State" command to implement, for example, a lamp test.

2.7.1.3 General Purpose LEDs

The General Purpose LEDs (LED3–0) are designed to indicate the boot-up POST code after which they are available to the application. If the LED3–0 are lit red during boot-up, a failure is indicated. In this event, please contact Kontron for further assistance.

Table 8: General Purpose LEDs' Functions on the CP6005-SA

LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION DURING uEFI BIOS POST (if POST code config. is enabled)	FUNCTION AFTER BOOT-UP
LED3	red	Power failure	--	--
	green	--	uEFI BIOS POST bit 3 and bit 7	--
	amber	--	--	--
LED2	red	CPU catastrophic error	CPU catastrophic error	--
	green	--	uEFI BIOS POST bit 2 and bit 6	SATA channels active
	amber	--	--	--
LED1	red	Hardware reset	--	--
	green	--	uEFI BIOS POST bit 1 and bit 5	--
	amber	--	--	--
LED0	red	uEFI BIOS boot failure	--	--
	green	--	uEFI BIOS POST bit 0 and bit 4	--
	amber	--	--	--

Table 9: General Purpose LEDs' Functions on the CP6005X-SA

LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION DURING uEFI BIOS POST (if POST code config. is enabled)	FUNCTION AFTER BOOT-UP
LED3	red	Power failure	--	--
	green	--	uEFI BIOS POST bit 3 and bit 7	--
	amber	--	--	--
LED2	red	CPU catastrophic error	CPU catastrophic error	--
	green	--	uEFI BIOS POST bit 2 and bit 6	SATA channels active
	amber	--	--	--
LED1	red	Hardware reset	--	--
	green	--	uEFI BIOS POST bit 1 and bit 5	10 Gigabit Ethernet link signal status of the high-speed serial rear I/O port 2 (10GbE2 Intel® 82599ES port 0)
	amber	--	--	--
LED0	red	uEFI BIOS boot failure	--	--
	green	--	uEFI BIOS POST bit 0 and bit 4	10 Gigabit Ethernet link signal status of the high-speed serial rear I/O port 1 (10GbE1 Intel® 82599ES port 1)
	amber	--	--	--

For further information regarding the configuration of the General Purpose LEDs, refer to Chapter 3.3.7, LED Configuration Register, and Chapter 3.3.8, LED Control Register.

Note: The bit allocation for Port 80 is the same as for the POST code.

How to Read the 8-Bit POST Code

Due to the fact that only 4 LEDs are available and 8 bits must be displayed, the POST code output is multiplexed on the General Purpose LEDs.

Table 10: POST Code Sequence

STATE	GENERAL PURPOSE LEDs
0	All LEDs are OFF; start of POST sequence
1	High nibble
2	Low nibble; state 2 is followed by state 0

The following is an example of the General Purpose LEDs' operation if the POST configuration is enabled (see also Tables 8 and 9).

Table 11: POST Code Example

	LED3	LED2	LED1	LED0	RESULT
HIGH NIBBLE	off (0)	on (1)	off (0)	off (0)	0x4
LOW NIBBLE	off (0)	off (0)	off (0)	on (1)	0x1
POST CODE	0x41				

Note: Under normal operating conditions, the General Purpose LEDs should not remain lit during boot-up. They are intended to be used only for debugging purposes. In the event that a General Purpose LED lights up during boot-up and the CP6005(X)-SA does not boot, please contact Kontron for further assistance.

2.7.2 USB Interfaces

The CP6005(X)-SA provides six USB 2.0 ports:

- Two on front I/O
- Four on the CompactPCI rear I/O interface

On the front panel, the CP6005(X)-SA has two standard, type A, USB 2.0 connectors, J6 and J7.

2.7.3 VGA Interface

The CP6005(X)-SA provides one standard VGA interface for connection to a monitor. The VGA interface is implemented as a standard VGA connector, J9, on the front panel.

2.7.4 Serial Ports

The CP6005(X)-SA provides two serial ports:

- COMA (RS-232) available either on the front panel or on the CompactPCI rear I/O interface
- COMB (RS-232) on the CompactPCI rear I/O interface

COMA and COMB are fully compatible with the 16550 controller. The rear I/O COMA port includes a complete set of handshaking and modem control signals. The COMB port includes RXD, TXD, CTS, and RTS signals.

The COMA and COMB ports provide maskable interrupt generation. The data transfer on the COM ports is up to 115.2 kbit/s. If RS-422 is required on the COMB port, please contact Kontron for further assistance.

The serial port COMA is implemented as an 8-pin RJ-45 connector, J8. The following figure and table provide pinout information for the serial connector J8 (COMA).

Figure 6: Serial Port Connector J8

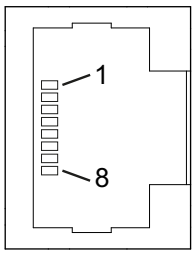


Table 12: Serial Port Connector J8 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	RTS	Request to send	O
2	DTR	Data terminal ready	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	DSR	Data send request	I
8	CTS	Clear to send	I

2.7.5 Gigabit Ethernet

The CP6005(X)-SA board provides five 10Base-T/100Base-TX/1000Base-T Ethernet interfaces. They are based on one Intel® I350 quad-port Gigabit Ethernet controller and one Intel® I210-IT Gigabit Ethernet controller.

The Intel® I350 quad-port Gigabit Ethernet controller provides four Gigabit Ethernet interfaces, two on the front panel, GbE A and GbE B, and two on the rear I/O, PICMG 2.16 LPa and PICMG 2.16 LPb. All four Ethernet channels support IPMI over LAN (IOL) and Serial over LAN (SOL).

Table 13: Gigabit Ethernet Controller Port Mapping

ETHERNET CONTROLLER	PORT MAPPING	IOL/SOL Channel (IPMI)
Intel® I350, port 0	Rear I/O port PICMG 2.16 LPb	2
Intel® I350, port 1	Rear I/O port PICMG 2.16 LPa	3
Intel® I350, port 2	Front I/O connector J11 (GbE B)	4
Intel® I350, port 3	Front I/O connector J10 (GbE A)	5
Intel® Intel® I210-IT	Front I/O connector J12 (GbE E)	--

The Intel® Intel® I210-IT Gigabit Ethernet controller provides one Gigabit Ethernet interface on the front panel, GbE E.

The Gigabit Ethernet interfaces are implemented as three standard RJ-45 Ethernet connectors, J10, J11 and J12 on the front panel.

2.7.5.1 10 Gigabit Ethernet Interfaces (CP6005X-SA)

The CP6005X-SA supports two 10GBASE-KR Ethernet interfaces on the rear I/O using the Intel® 82599ES dual-port 10 Gigabit Ethernet controller.

The following table indicates the 10 Gigabit Ethernet port mapping of the CP6005X-SA.

Table 14: 10 Gigabit Ethernet Controller Port Mapping

ETHERNET CONTROLLER	PORT MAPPING
Intel® 82599ES, port 0	High-speed serial rear I/O interconnection port 2 (10GBE2)
Intel® 82599ES, port 1	High-speed serial rear I/O interconnection port 1 (10GBE1)

2.7.6 SATA Interfaces

The CP6005(X)-SA provides six SATA ports:

- One SATA 6 Gb/s port on the J16 connector for mounting either a SATA Flash module or an onboard 2.5" HDD/SSD via the MMADP01-SATA01 module
- One SATA 6 Gb/s port on the standard SATA connector, J14, for connection to SATA devices via cable
- Four SATA 3 Gb/s ports on the CompactPCI rear I/O interface

All six SATA interfaces provide high-performance RAID 0/1/5/10 functionality.

2.7.7 PMC Interface

The CP6005(X)-SA provides one 3.3 V standard PMC interface with a dedicated 32-bit/66 MHz PCI Express-to-PCI bridge. The PMC interface is compliant with the IEEE 1386.1-2001 specification, which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor.

A PMC module can be connected to the CP6005(X)-SA via the standard PMC connectors J20 (Jn1) and J21 (Jn2).

Table 15: PMC PCI Frequency Configuration

FREQUENCY	M66EN Signal J21 (Jn2)	DIP SWITCH SW2 SWITCH 3
33 MHz	Low	OFF
33 MHz	--	ON
66 MHz	High	OFF

2.7.8 XMC Interface

For easy and flexible configuration a standard XMC connector, J19, is available. The board uses one x8 PCI Express 2.0 interface operating at 5.0 GT/s and compliant with the ANSI/VITA 42.0 and ANSI/VITA 42.3 specifications. x8 PCI Express 3.0 operating at 8 GT/s is available on request.

2.7.9 CompactPCI Interface

The CP6005(X)-SA supports a flexibly configurable, hot swap CompactPCI interface. In the system slot the PCI/ PCI-X interface is in the transparent mode, and in the peripheral slot the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus. This mode is known as "passive mode".

2.7.9.1 Board Functionality when Installed in System Slot

The CP6005(X)-SA supports a flexibly configurable, hot swap CompactPCI interface. In the system slot the PCI/ PCI-X interface is in the transparent mode, and in the peripheral slot the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus. This mode is known as "passive mode".

2.7.9.2 Board Functionality when Installed in System Slot

In the system slot, the CompactPCI interface can be either a 64-bit/66 MHz PCI or PCI-X interface via a dedicated PCI Express-to-PCI-X bridge from Pericom (PI7C9X130).

The CP6005(X)-SA supports up to seven peripheral slots with 33 MHz and up to 4 peripheral slots with 66 MHz through a backplane.

The PCI Express-to-PCI-X bridge detects the PCI mode (PCI or PCI-X) and the bus speed (33 MHz or 66 MHz) via two PCI control signals on J1: PCIXCAP (pin B16) and M66EN (pin D21). The following configurations are supported by the CompactPCI interface.

Table 16: CompactPCI PCI/ PCI-X Configuration

FREQUENCY	MODE	M66EN J1, PIN D21	PCIXCAP J1, PIN B16	DIP SWITCH SW2 SWITCH 2	DIP SWITCH SW2 SWITCH 1
33 MHz	PCI	Low	Low	OFF	OFF
33 MHz	PCI	--	Low	OFF	ON
66 MHz	PCI	High	Low	OFF	OFF
66 MHz	PCI	High	--	ON	OFF
66 MHz	PCI-X	--	Pull-down resistor	OFF	OFF

Note: To support 66 MHz PCI/ PCI-X frequency, the CompactPCI signaling voltage (VI/O) must be 3.3 V.
The CP6005(X)-SA provides automatic voltage detection for the VI/O to switch the PCI frequency to 33 MHz in an 5V environment.

2.7.9.3 Board Functionality when Installed in Peripheral Slot (Passive Mode)

In a peripheral slot, the board receives power but does not communicate on the CompactPCI bus; all CompactPCI signals are isolated. In this configuration, the communication is achieved via the two Gigabit Ethernet ports as defined in the PICMG 2.16 specification.

2.7.9.4 Packet Switching Backplane (PICMG 2.16)

The CP6005(X)-SA supports two Gigabit Ethernet ports on the J3 connector in accordance with the CompactPCI Packet Switching Backplane Specification PICMG 2.16. The two ports are connected in the chassis via the CompactPCI Packet Switching Backplane to the Fabric slots "A" and "B". The PICMG 2.16 feature can be used in the system slot and in the peripheral slot as well.

2.7.9.5 Hot Swap Support

To ensure that a board may be removed and replaced in a working bus without disturbing the system, the following additional features are required:

- Power ramping
- Precharge
- Hot swap control and status register bits
- Automatic interrupt generation whenever a board is about to be removed or replaced
- A Hot Swap LED to indicate that the board may be safely removed

2.7.9.6 Power Ramping

On the CP6005(X)-SA a special hot swap controller is used to ramp up the onboard supply voltage. This is done to avoid transients on the +3.3V, +5V, +12V and -12V power supplies from the hot swap system. When the power supply is stable, the hot swap controller generates an onboard reset to put the board into a definite state.

2.7.9.7 Precharge

Precharge is provided on the CP6005(X)-SA by a resistor on each signal line (PCI bus) connected to a +1V reference voltage.

2.7.9.8 Handle Switch

A microswitch is situated in the extractor handle. The status of the handle is included in the onboard logic. The microswitch is connected to the onboard connector J13.

2.7.9.9 ENUM# Interrupt

If the board is operated in the system slot, the ENUM signal is an input.

2.7.9.10 Hot Swap LED

The blue HS LED can be switched on or off by software. It may be used, for example, to indicate that the shutdown process is finished and the board is ready for extraction.

2.7.10 CompactPCI Connectors

The complete CompactPCI connector configuration comprises up to four standard connectors (2mm Hard Metric) designated as J1, J2, J3 and two high-speed serial ZDplus connectors, J4 and J41.

Their functions are as follows:

- J1 and J2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J3 and J5 with standard rear I/O interface functionality
- J4 and J41 for high-speed serial rear I/O interconnection

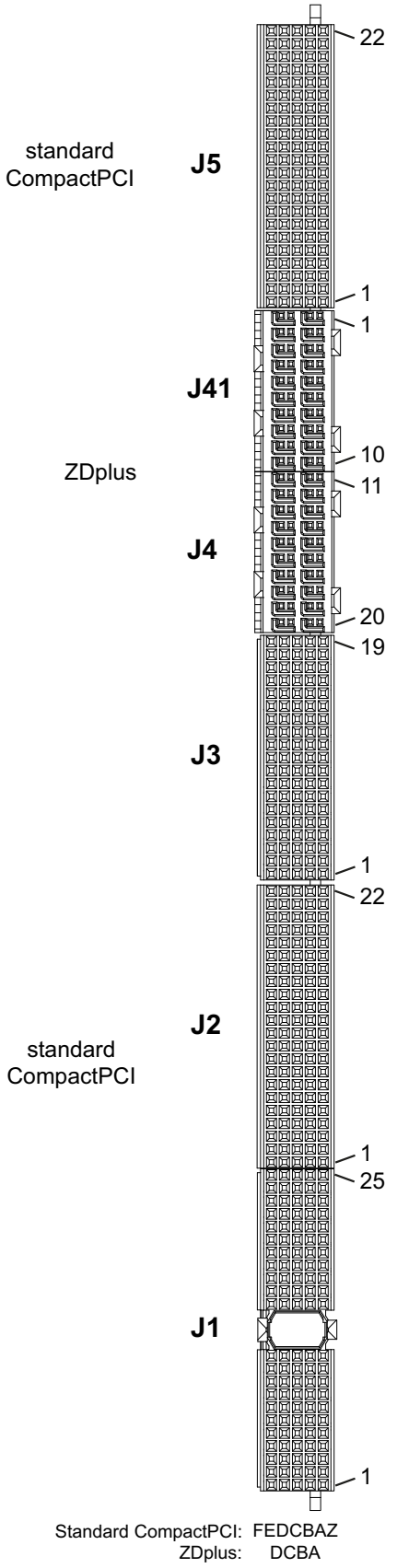
The CP6005(X)-SA is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

2.7.10.1 Connector Keying

The CompactPCI connector J1 supports guide lugs to ensure a correct polarized mating.

The CP6005(X)-SA supports universal PCI VI/O signaling voltages with one common termination resistor configuration and includes a PCI VI/O voltage detection circuit. If the PCI VI/O voltage is 5 V, the maximum supported PCI frequency is 33 MHz.

Figure 7: CompactPCI Connectors



2.7.10.2 CompactPCI Connectors J1 and J2 Pinout

The CP6005(X)-SA is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 17: CompactPCI Bus Connector J1 System Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	REQ64#	ENUM#	3.3V	5V	GND
24	NC	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	NC	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	NC	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	NC	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	NC	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	NC	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	NC	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	NC	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	NC	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
15	NC	3.3V	FRAME#	IRDY#	BDSEL#	TRDY#	GND
14-12	Key Area						
11	NC	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	NC	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	NC	C/BE[3]#	NC	AD[23]	GND	AD[22]	GND
8	NC	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	NC	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	NC	REQ0#	CPCI_Present#	3.3V	CLK0	AD[31]	GND
5	NC	RSV	RSV	RST#	GND	GNT0#	GND
4	NC	IPMB PWR	Health#	V(I/O)	RSV	RSV	GND
3	NC	INTA#	INTB#	INTC#	5V	INTD#	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	-12V	TRST#	+12V	5V	GND

Table 18: CompactPCI Bus Connector J1 Peripheral Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	*	*	3.3V	5V	GND
24	NC	*	5V	V(I/O)	*	*	GND
23	NC	3.3V	*	*	5V	*	GND
22	NC	*	GND	3.3V	*	*	GND
21	NC	3.3V	*	*	*	*	GND
20	NC	*	GND	V(I/O)	*	*	GND
19	NC	3.3V	*	*	GND	*	GND
18	NC	*	GND	3.3V	*	*	GND
17	NC	3.3V	IPMB SCL	IPMB SDA	GND	*	GND
16	NC	*	*	V(I/O)	*	*	GND
15	NC	3.3V	*	*	BDSEL#	*	GND
14-12	Key Area						
11	NC	*	*	*	GND	*	GND
10	NC	*	GND	3.3V	*	*	GND
9	NC	*	NC	*	GND	*	GND
8	NC	*	GND	V(I/O)	*	*	GND
7	NC	*	*	*	GND	*	GND
6	NC	*	CPCI_Present#	3.3V	*	*	GND
5	NC	RSV	RSV	RST#**	GND	*	GND
4	NC	IPMB PWR	Healthy#	V(I/O)	RSV	RSV	GND
3	NC	*	*	*	5V	*	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	-12V	TRST#	+12V	5V	GND

Note: A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP6005(X)-SA is inserted in a peripheral slot.
** When the CP6005(X)-SA is inserted in a peripheral slot, the function of the RST# signal can be enabled or disabled.

Table 19: 64-bit CompactPCI Bus Connector J2 System Slot Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	CLK6	GND	RSV	RSV	RSV	GND
20	NC	CLK5	GND	RSV	GND	RSV	GND
19	NC	GND	GND	IPMB2_SDA	IPMB2_SCL	IPMB2_Alert	GND
18	NC	RSV	RSV	RSV	GND	RSV	GND
17	NC	RSV	GND	PRST#	REQ6#	GNT6#	GND
16	NC	RSV	RSV	DEG#	GND	RSV	GND
15	NC	RSV	GND	FAL#	REQ5#	GNT5#	GND
14	NC	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	NC	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	NC	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	NC	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	NC	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	NC	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	NC	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	NC	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	NC	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	NC	C/BE[5]#	NC	V(I/O)	C/BE[4]#	PAR64	GND
4	NC	V(I/O)	RSV	C/BE[7]#	GND	C/BE[6]#	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Table 20: 64-bit CompactPCI Bus Connector J2 Peripheral Slot Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	*	GND	RSV	RSV	RSV	GND
20	NC	*	GND	RSV	GND	RSV	GND
19	NC	GND	GND	IPMB2_SDA	IPMB2_SCL	IPMB2_Alert	GND
18	NC	RSV	RSV	RSV	GND	RSV	GND
17	NC	RSV	GND	*	*	*	GND
16	NC	RSV	RSV	DEG#	GND	RSV	GND
15	NC	RSV	GND	FAL#	*	*	GND
14	NC	*	*	*	GND	*	GND
13	NC	*	GND	V(I/O)	*	*	GND
12	NC	*	*	*	GND	*	GND
11	NC	*	GND	V(I/O)	*	*	GND
10	NC	*	*	*	GND	*	GND
9	NC	*	GND	V(I/O)	*	*	GND
8	NC	*	*	*	GND	*	GND
7	NC	*	GND	V(I/O)	*	*	GND
6	NC	*	*	*	GND	*	GND
5	NC	*	NC	V(I/O)	*	*	GND
4	NC	V(I/O)	RSV	*	GND	*	GND
3	NC	*	GND	*	*	*	GND
2	NC	*	*	SYSEN#	*	*	GND
1	NC	*	GND	*	*	*	GND

Note: A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP6005(X)-SA is inserted in a peripheral slot.

2.7.10.3 CompactPCI Rear I/O Connectors J3 and J5 Pinout

The CP6005(X)-SA board provides rear I/O connectivity for peripherals. Standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connectors J3 and J5.

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus, the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system rear I/O feature a special backplane is necessary. The CP6005(X)-SA with rear I/O is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support.

The CP6005(X)-SA conducts all standard rear I/O signals through the J3 and J5 connectors.

Table 21: CompactPCI Rear I/O Connector J3 Pinout

PIN	Z	A	B	C	D	E	F
19	NC	RIO_VCC	RIO_VCC	RIO_3.3V	RIO_+12V	RIO_-12V	GND
18	NC	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	NC	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	NC	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	NC	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	NC	LPa:LINK	LPb:LINK	LPab:CT1	RSV	FAN:SENSE2	GND
13	NC	LPa:ACT	LPb:ACT	RSV	RSV	FAN:SENSE1	GND
12	NC	RSV	RSV	GND	RSV	RSV	GND
11	NC	RSV	RSV	GND	RSV	RSV	GND
10	NC	USB1:VCC	USB0:VCC	GND	USB3:VCC	USB2:VCC	GND
9	NC	USB1:D-	USB1:D+	GND	USB3:D-	USB3:D+	GND
8	NC	USB0:D-	USB0:D+	GND	USB2:D-	USB2:D+	GND
7	NC	RIO_3.3V	GPI0	GPI1	GPI2	SPEAKER	GND
6	NC	VGA:RED	VGA:GREEN	VGA:SDA	DEBUG:CLK	DEBUG:DAT	GND
5	NC	VGA:BLUE	VGA:HSYNC	VGA:VSYNC	VGA:SCL	RSV	GND
4	NC	RSV	RSV	SPB:CTS	SPB:TXD	RSV	GND
3	NC	SPB:RTS	SPB:RXD	RSV	RSV	RSV	GND
2	NC	SPA:RI	SPA:DTR	SPA:CTS	SPA:TXD	RSV	GND
1	NC	SPA:RTS	SPA:RXD	SPA:DSR	SPA:DCD	RIO_ID1	GND

Note: The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.
Failure to comply with the above will result in damage to your board.

Table 22: CompactPCI Rear I/O Connector J3 Signals

SIGNAL	DESCRIPTION
SPA	COMA signaling (RS-232)
SPB	COMB signaling (RS-232)
VGA	Graphic signaling
USB0 to USB3	USB port signaling
SPEAKER	Standard PC speaker
FAN	Fan speed sensoring
DEBUG	Debug output
LPa	Rear I/O LAN Port A
LPb	Rear I/O LAN Port B
GPIO	General purpose digital input/output; 3.3 V only

Note: The VGA interface can be used both on the front panel and on the rear I/O. However, the VGA signals are switched to front I/O or rear I/O, depending on the uEFI BIOS setting.
COMA can be used either on the front panel or on the rear I/O. It is not possible to use COMA on the front panel and on the rear I/O simultaneously.

Table 23: CompactPCI Rear I/O Connector J5 Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GPI3	PWM1:OUT	GND	PWM2:OUT	BATT (3.0V)	GND
21	NC	HDA:SYNC	HDA:RST	GND	HDA:SDOUT	SYS_WP#	GND
20	NC	GPO0	HDA:SDIN1	GND	GPO1	HDA:SDIN2	GND
19	NC	GND	GND	GND	HDA:SDIN0	HDA:BITCLK	GND
18	NC	HDMI2:D0+	HDMI2:D0-	GND	GND	GND	GND
17	NC	HDMI2:D2+	HDMI2:D2-	GND	HDMI2:D1+	HDMI2:D1-	GND
16	NC	RSV	HDMI2:HPDET	GND	GPO2	GPO3	GND
15	NC	HDMI2:CLK+	HDMI2:CLK-	GND	HDMI2:SDA	HDMI2:SDC	GND
14	NC	GND	GND	GND	GND	GND	GND
13	NC	HDMI1:D0+	HDMI1:D0-	GND	HDMI1:D1+	HDMI1:D1-	GND
12	NC	HDMI1:D2+	HDMI1:D2-	GND	RSV	RSV	GND
11	NC	RSV	HDMI1:HPDET	GND	HDMI1:SDA	HDMI1:SDC	GND
10	NC	HDMI1:CLK+	HDMI1:CLK-	GND	RSV	RSV	GND
9	NC	GND	GND	GND	GND	GND	GND
8	NC	SATA3:TX+	SATA3:TX-	GND	SATA3:RX+	SATA3:RX-	GND
7	NC	GND	GND	GND	GND	GND	GND
6	NC	SATA2:TX+	SATA2:TX-	GND	SATA2:RX+	SATA2:RX-	GND
5	NC	GND	GND	GND	GND	GND	GND
4	NC	SATA1:TX+	SATA1:TX-	GND	SATA1:RX+	SATA1:RX-	GND
3	NC	GND	GND	GND	GND	GND	GND
2	NC	SATA0:TX+	SATA0:TX-	GND	SATA0:RX+	SATA0:RX-	GND
1	NC	GND	GND	GND	GND	GND	GND

Table 24: CompactPCI Rear I/O Connector J5 Signals

SIGNAL	DESCRIPTION
SATA0..3	SATA Port 0..3 Signaling
HDMI1	HDMI signaling
HDMI2	HDMI signaling
HDA	High-definition audio signaling
PWM	Pulse width modulation output for fan
GPIO	General purpose digital input/output; 3.3 V only
SYS_WP#	System write protection for non-volatile memory devices; 3.3 V only
BATT (3.0V)	Back-up power input for RTC and CMOS RAM; 3.0 V only

2.7.10.4 High-Speed Serial Rear I/O Connectors J41 and J4 Pinout (CP6005X-SA)

The CP6005X-SA provides rear I/O connectivity via two ZDplus high-speed serial rear I/O connectors, J4 and J41, and supports the following high-speed serial rear I/O interfaces:

- Two 10GBASE-KR interfaces
- One x4 PCI Express 2.0 operating at 5 GT/s as a root complex controller only

For the system rear I/O feature a special backplane is necessary. The CP6005X-SA is compatible with all Kontron 6U CompactPCI passive backplanes that are compliant with the PICMG 2.20 specification.

Table 25: High-Speed Serial Rear I/O Connector J41 Pinout

POS	A		B		C		D	
	SIGNAL	DRIVEN BY	SIGNAL	DRIVEN BY	SIGNAL	DRIVEN BY	SIGNAL	DRIVEN BY
1	PE1_RST#	Board/ Tristate*	PE2_RST#	Board/ Tristate*	PE_END_ROOT#	BCKPL	PE_1x8_2x4#	-- (BCKPL)
2	40GBE1_TX0+	Board	40GBE1_TX0-	Board	40GBE1_RX0-	BCKPL	40GBE1_RX0+	BCKPL
3	NC (40GBE1_TX1+)	--	NC (40GBE1_TX1-)	--	NC (40GBE1_RX1-)	--	NC (40GBE1_RX1+)	--
4	NC (40GBE1_TX2+)	--	NC (40GBE1_TX2-)	--	NC (40GBE1_RX2-)	--	NC (40GBE1_RX2+)	--
5	NC (40GBE1_TX3+)	--	NC (40GBE1_TX3-)	--	NC (40GBE1_RX3-)	--	NC (40GBE1_RX3+)	--
6	40GBE2_TX0+	Board	40GBE2_TX0-	Board	40GBE2_RX0-	BCKPL	40GBE2_RX0+	BCKPL
7	NC (40GBE2_TX1+)	--	NC (40GBE2_TX1-)	--	NC (40GBE2_RX1-)	--	NC (40GBE2_RX1+)	--
8	NC (40GBE2_TX2+)	--	NC (40GBE2_TX2-)	--	NC (40GBE2_RX2-)	--	NC (40GBE2_RX2+)	--
9	NC (40GBE2_TX3+)	--	NC (40GBE2_TX3-)	--	NC (40GBE2_RX3-)	--	NC (40GBE2_RX3+)	--
10	NC (SATA1_TX+)	--	NC (SATA1_TX-)	--	NC (SATA1_RX-)	--	NC (SATA1_RX+)	--

Table 26: High-Speed Serial Rear I/O Connector J4 Pinout

POS	A		B		C		D	
	SIGNAL	DRIVEN BY	SIGNAL	DRIVEN BY	SIGNAL	DRIVEN BY	SIGNAL	DRIVEN BY
11	NC (SATA2_TX+)	--	NC (SATA2_TX-9	--	NC (SATA2_RX-)	--	NC (SATA2_RX+)	--
12	NC (PE1_TX7+)	--	NC 8PE1_TX7-9	--	NC (PE1_RX7+)	--	NC (PE1_RX7-)	--
13	NC (PE1_TX6+)	--	NC (PE1_TX6-)	--	NC (PE1_RX6+)	--	NC (PE1_RX6-)	--
14	NC (PE1_TX5+)	--	NC (PE1_TX5-)	--	NC (PE1_RX5+)	--	NC (PE1_RX5-)	--
15	NC (PE1_TX4+)	--	NC (PE1_TX4-)	--	NC (PE1_RX4+)	--	NC (PE1_RX4-)	--
16	PE1_TX3+	Board	PE1_TX3-	Board	PE1_RX3+	BCKPL	PE1_RX3-	BCKPL
17	PE1_TX2+	Board	PE1_TX2-	Board	PE1_RX2+	BCKPL	PE1_RX2-	BCKPL
18	PE1_TX1+	Board	PE1_TX1-	Board	PE1_RX1+	BCKPL	PE1_RX1-	BCKPL
19	PE1_TX0+	Board	PE1_TX0-	Board	PE1_RX0+	BCKPL	PE1_RX0-	BCKPL
20	PE1_CLK+	Board/ Tristate*	PE1_CLK-	Board/ Tristate*	NC (PE2_CLK+)	--	NC (PE2_CLK-)	--

* If the board is plugged in a backplane slot with PCI Express root-complex configuration, the signals are driven by the board. If the board is plugged in a backplane slot with PCI Express endpoint configuration, the signals are in Tristate mode.

Table 27: High-Speed Serial Rear I/O Connectors J41 and J4 Signal Description

SIGNAL	DESCRIPTION
40GBE1_TX/RX	10GBASE-KR/40GBASE-KR4 port 1 transmit/receive signals (10GBASE-KR only)
40GBE2_TX/RX	10GBASE-KR/40GBASE-KR4 port 2 transmit/receive signals (10GBASE-KR only)
SATA1_TX/RX	SATA port 1 transmit/receive signals (not used)
SATA2_TX/RX	SATA port 1 transmit/receive signals (not used)
PE1_CLK	PCI Express reference clock for 1 x8 or 1 x4 configuration
PE2_CLK	PCI Express reference clock for 2 x4 configuration (not supported on the CP6005(X)-SA)
PE1_RST#	PCI Express system reset for 1 x8 or 1 x4 configuration
PE2_RST#	PCI Express system reset for 2 x4 configuration (not supported on the CP6005(X)-SA)
PE_END_ROOT#	PCI Express endpoint high or root-complex backplane configuration 1 = endpoint configuration 0 = root-complex configuration
PE_1x8_2x4#	PCI Express for 1 x8 or 2 x4 backplane configuration (not supported on the CP6005(X)-SA)

2.7.11 High-Speed Serial Rear I/O Interconnection

The high-speed serial rear I/O interconnection has been designed to meet the PICMG 2.20 R1.0 standard. In addition, Kontron has made minor improvements to ensure maximum signal integrity, such as:

- » upgraded high-speed ZDplus connector mechanically compliant with the PICMG 2.20 providing better shielding to support up to 15 GHz signal frequency
- » high-speed interconnection supporting 10GBASE-KR/40GBASE-KR4, one x8 PCI Express 3.0 port operating at 8 GT/s and two SATA 6 Gb/s ports

Note: The PICMG 2.20 configuration allows coexistence with PICMG 2.16 fabrics.

Table 28: High-Speed Serial Rear I/O Interconnection Port Mapping

CON	POS	PICMG 2.20	PORT DEFINITION	CP6005X-SA
J41	1	AUX	PCIe Control	PCIe Control
	2	PORT 1	10GBASE-KR/ 40GBASE-KR4 Port 1	10GBE1
	3	PORT 2		--
	4	PORT 3		--
	5	PORT 4		--
	6	PORT 5	10GBASE-KR/ 40GBASE-KR4 Port 2	10GBE2
	7	PORT 6		--
	8	PORT 7		--
	9	PORT 8		--
	10	PORT 9	SATA 6 Gb/s Port 1	--
J4	11	PORT 10	SATA 6 Gb/s Port 2	--
	12	PORT 11	1 x8 PCIe Gen 3	--
	13	PORT 12		--
	14	PORT 13		--
	15	PORT 14		--
	16	PORT 15		1 x4 PCIe Gen 2
	17	PORT 16		
	18	PORT 17		
	19	PORT 18		
	20	CLOCK	PCIe Reference Clock	PCIe Reference Clock

3 Configuration

3.1 DIP Switch Configuration

3.1.1 DIP Switch SW1

The DIP switch SW1 serves for general board configuration.

Table 29: DIP Switch SW1 Functionality

SWITCH	SETTING	FUNCTIONALITY
1	***OFF***	***Boot-up with POST code indication on LED3–0***
	ON	Boot-up with no POST code indication on LED3–0
2	***OFF***	***Boot from the standard SPI boot flash***
	ON	Boot from the recovery SPI boot flash
3	***OFF***	***Non-volatile memory write protection disabled*** (if no other write protection sources are enabled)
	ON	Non-volatile memory write protection enabled
4	***OFF***	***Boot using the currently saved uEFI BIOS settings***
	ON	Clear the uEFI BIOS settings and use the default values

The default setting is indicated by using italic bold.

To clear the uEFI BIOS settings and the passwords, proceed as follows:

1. Set DIP switch SW1, switch 4, to the ON position.
2. Apply power to the system.
3. Wait 30 seconds and then remove power from the system. During this time period no messages are displayed.
4. Set DIP switch SW1, switch 4, to the OFF position.

3.1.2 DIP Switch SW2

The DIP switch SW2 serves for CompactPCI and PMC PCI interface configuration.

Table 30: DIP Switch SW2 Functionality

SWITCH	SETTING	FUNCTIONALITY
1	***OFF***	***CompactPCI frequency 33/66 MHz, auto detection via the backplane***
	ON	CompactPCI frequency configured to 33 MHz
2	***OFF***	***CompactPCI mode (PCI/PCI-X) auto detection via the backplane***
	ON	CompactPCI interface configured to PCI mode
3	***OFF***	***PMC PCI frequency 33/66 MHz, auto detection via the PMC interface***
	ON	PMC PCI frequency configured to 33 MHz
4	***OFF***	Reserved
	ON	

3.2 System Write Protection

The CP6005(X)-SA provides write protection for non-volatile memories via the DIP switch SW1, the uEFI Shell and a backplane pin. If one of these sources is enabled, the system is write protected. Please contact Kontron for further information before using these functions.

3.3 CP6005(X)-SA-Specific Registers

Table 31: CP6005(X)-SA-Specific Registers

ADDRESS	DEVICE
0x284	Write Protection Register (WPROT)
0x285	Reset Status Register (RSTAT)
0x288	Board ID High Byte Register (BIDH)
0x28A	Geographic Addressing Register (GEOAD)
0x28C	Watchdog Timer Control Register (WTIM)
0x28D	Board ID Low Byte Register (BIDL)
0x290	LED Configuration Register (LCFG)
0x291	LED Control Register (LCTRL)
0x292	General Purpose Output Register (GPOUT)
0x293	General Purpose Input Register (GPIN)

3.3.1 Write Protection Register (WPROT)

The Write Protection Register holds the write protect signals for non-volatile devices.

Table 32: Write Protection Register (WPROT)

ADDRESS		0x284						
BIT	7	6	5	4	3	2	1	0
NAME	SWP	Reserved			SFWP	DSWP	BSWP	SSWP
ACCESS	R	R			R/W	R	R	R/W
RESET	0	000			0	0	0	0
BITFIELD		DESCRIPTION						
7	SWP	System write protection status: 0 = Onboard non-volatile memory devices not write protected 1 = Onboard non-volatile memory devices write protected						
3	SFWP	Reserved						
2	DSWP	This bit reflects the state of the system write protection via DIP switch SW1, switch 3: 0 = System not write protected via DIP switch 1 = System write protected						
1	BSWP	This bit reflects the state of the system write protection via backplane (SYS_WP#): 0 = System not write protected via backplane 1 = System write protected						
0	SSWP	This bit reflects the state of the system write protection via software: 0 = System devices not write protected via software 1 = System write protected If this bit is programmed once, it cannot be reprogrammed.						

3.3.2 Reset Status Register (RSTAT)

The Reset Status Register is used to determine the host's reset source.

Table 33: Reset Status Register (RSTAT)

ADDRESS		0x285						
BIT	7	6	5	4	3	2	1	0
NAME	PORS	Reserved	SRST	Reserved	IPRS	FPRS	CPRS	WTRS
ACCESS	R/W	R	R/W	R	R/W	R/W	R/W	R/W
RESET	N/A	0	0	0	0	0	0	0

BITFIELD		DESCRIPTION
7	PORS	Power-on reset status: 0 = System reset generated by warm reset 1 = System reset generated by power-on (cold) reset Writing a '1' to this bit clears the bit.
5	SRST	Software reset status: 0 = Reset is logged by the IPMI controller 1 = Reset is not logged by IPMI controller The uEFI BIOS / software sets this bit to inform the IPMI controller that the next reset should not be logged.
3	IPRS	IPMI controller reset status: 0 = System reset not generated by IPMI 1 = System reset generated by IPMI Writing a '1' to this bit clears the bit.
2	FPRS	Front panel push button reset status: 0 = System reset not generated by front panel reset 1 = System reset generated by front panel reset Writing a '1' to this bit clears the bit.
1	CPRS	CompactPCI reset status (PRST signal): 0 = System reset not generated by CompactPCI reset input 1 = System reset generated by CompactPCI reset input Writing a '1' to this bit clears the bit.
0	WTRS	Watchdog timer reset status: 0 = System reset generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears the bit.

Note: The Reset Status Register is set to default values by power-on (cold) reset, not by a warm reset.

3.3.3 Board ID High Byte Register (BIDH)

Table 34: Board ID High Byte Register (BIDH)

ADDRESS	0x288							
BIT	7	6	5	4	3	2	1	0
NAME	BIDH							
ACCESS	R							
RESET	0xB4							
BITFIELD		DESCRIPTION						
7	BIDH	Board identification: CP6005-SA: 0xB400 CP6005X-SA: 0xB401						

3.3.4 Geographic Addressing Register (GEOAD)

The Geographic Addressing Register holds the CompactPCI geographic address (site number) used to assign the Intelligent Platform Management Bus (IPMB) address to the CP6005(X)-SA.

Table 35: Geographic Addressing Register (GEOAD)

ADDRESS	0x28A							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved			GA				
ACCESS	R			R				
RESET	000			N/A				
BITFIELD		DESCRIPTION						
7..5	Res.	Reserved						
4..0	GA	Geographic address						

Note: The Geographic Addressing Register is set to default values by power-on (cold) reset, not by a warm reset.

3.3.5 Watchdog Timer Control Register (WTIM)

Table 36: Watchdog Timer Control Register (WTIM)

ADDRESS	0x28C							
BIT	7	6	5	4	3	2	1	0
NAME	WTE	WMD		WEN/WTR	WTM			
ACCESS	R/W	R/W		R/W	R/W			
RESET	0	00		0	0000			

BITFIELD		DESCRIPTION
7	WTE	Watchdog timer expired status bit: 0 = Watchdog timer has not expired 1 = Watchdog timer has expired. Writing a '1' to this bit resets it to 0.
6..5	WMD	Watchdog mode: 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)
4	WEN/WTR	Watchdog enable / Watchdog trigger control bit: 0 = Watchdog timer not enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog timer is enabled, it will indicate a '1'. 1 = Watchdog timer enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3..0].
3..0	WTM	Watchdog timeout settings: 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = 512 s 1101 = 1024 s 1110 = 2048 s 1111 = 4096 s

3.3.6 Board ID Low Byte Register (BIDL)

Table 37: Board ID Low Byte Register (BIDL)

ADDRESS	0x28D							
BIT	7	6	5	4	3	2	1	0
NAME	BIDL							
ACCESS	R							
RESET	0x00 (CP6005-SA) / 0x01 (CP6005X-SA)							

BITFIELD		DESCRIPTION
7	BIDL	Board identification: CP6005-SA: 0xB400 CP6005X-SA: 0xB401

3.3.7 LED Configuration Register (LCFG)

The LED Configuration Register holds a series of bits defining the onboard configuration for the front panel General Purpose LEDs.

Table 38: LED Configuration Register (LCFG)

ADDRESS	0x290							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved				LCON			
ACCESS	R				R/W			
RESET	0000				0000			

BITFIELD		DESCRIPTION
3..0	LCON	LED3–0 configuration: 0000 = POST Mode (LEDs build a binary vector to display Port 80 signals) 0001 = General Purpose Mode (LEDs are controlled via the LCTRL register) 0010 - 1111 = Reserved

Beside the configurable functions described above, LED3–0 fulfill also a basic debug function during the power-up phase as long as the first access to Port 80 is processed. For further information on reading the 8-bit uEFI BIOS POST Code, refer to Chapter 2.7.1.3, “General Purpose LEDs”.

3.3.8 LED Control Register (LCTRL)

The LED Control Register enables the user to switch on and off the front panel General Purpose LEDs.

Table 39: LED Control Register (LCTRL)

ADDRESS	0x291							
BIT	7	6	5	4	3	2	1	0
NAME	LCMD				LCOL			
ACCESS	R/W				R/W			
RESET	0000				0000			

BITFIELD		DESCRIPTION
7..4	LCMD	LED command: 0000 = Get LED0 1000 = Set LED0 0001 = Get LED1 1001 = Set LED1 0010 = Get LED2 1010 = Set LED2 0011 = Get LED3 1011 = Set LED3 0100 - 0111 = Reserved 1100 - 1111 = Reserved
3..0	LCOL	LED color: 0000 = Off 0001 = Green 0010 = Red 0011 = Red+Green 0100 - 1111 = Reserved

Note: The LED Control Register can only be used if the General Purpose LEDs indicated in the “LED Configuration Register” (see Table 38) are configured in General Purpose Mode.

3.3.9 General Purpose Output Register (GPOUT)

The General Purpose Output Register holds the general purpose output signals of the rear I/O Compact-PCI connectors.

Table 40: General Purpose Output Register (GPOUT)

ADDRESS	0x292							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved				GPO3	GPO2	GPO1	GPO0
ACCESS	R				R/W	R/W	R/W	R/W
RESET	0000				0	0	0	0

BITFIELD		DESCRIPTION
3..0	GPO3..0	General purpose output signals: 0 = Output low 1 = Output high

3.3.10 General Purpose Input Register (GPIN)

The General Purpose Input Register holds the general purpose input signals of the rear I/O CompactPCI connectors.

Table 41: General Purpose Input Register (GPIN)

ADDRESS	0x293							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved				GPI3	GPI2	GPI1	GPI0
ACCESS	R				R	R	R	R
RESET	0000				1	1	1	1

BITFIELD		DESCRIPTION
3..0	GPI3.. 0	General purpose input signals: 0 = Input low 1 = Input high

4 Power Considerations

4.1 CP6005(X)-SA Voltage Ranges

The CP6005(X)-SA has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The system power supply must comply with the CompactPCI® specification.

The following table specifies the ranges for the input power voltage within which the board is functional.

Table 42: DC Operational Input Voltage Range

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE
+3.3 V	3.2 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.
+12 V	11.4 V min. to 12.6 V max.
-12 V	-11.4 V min. to -12.6 V max.

Note: Failure to comply with the instructions above may result in damage to the board or improper operation.

4.1.1 Start-Up Requirement

Power supplies must comply with the following guidelines, in order to be used with the CP6005(X)-SA:

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

4.1.2 Power-Up Sequence

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation.

Both voltages must reach their minimum in-regulation level not later than 20 ms after the output power ramp start.

4.1.3 Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Note: All of the input voltages must be functionally coupled to each other so that if one input voltage fails, all other input voltages must be regulated proportionately to the failed voltage. For example, if the +5V begins to decrease, all other input voltages must decrease accordingly. This is required in order to preclude cross currents within the CP6005(X)-SA. Failure to comply with above may result in damage to the board or improper system operation.

Note: If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until the capacitors are discharged. If the voltage rises again before it has gone below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 10 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

4.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CP6005(X)-SA baseboard and for additional configurations. The processor and the memory dissipate the majority of the thermal power.

The power consumption measurements were carried out using the following testing parameters:

- CP6005(X)-SA installed in the system slot
- Ethernet ports not connected
- 4 GB DDR3L SDRAM in dual-channel mode
- +3.3 V, 5 V, and 12 V main supply voltage
- 2.5 m/s airflow

The operating systems used were uEFI Shell and Windows® 7, 64-bit. All measurements were conducted at an ambient temperature of 25 °C. The power consumption values indicated in the tables below can vary depending on the ambient temperature. This can result in deviations of the power consumption values of up to 15%.

The power consumption was measured using the following the 4th generation processors:

- Quad-core Intel® Core™ i7-4860EQ (SV), 1.8 GHz, 6 MB L3 cache, GT3e
- Quad-core Intel® Core™ i7-4700EQ (SV), 2.4 GHz, 6 MB L3 cache, GT2
- Quad-core Intel® Core™ i7-4700EQ (SV), 1.7 GHz, 6 MB L3 cache, GT2 (cTDP enabled)
- Dual-core Intel® Core™ i5-4400E (SV), 2.7 GHz, 3 MB L3 cache, GT2

The power consumption was measured using the following configurations:

» Work load: uEFI Shell

For this measurement the processor cores were active, the graphics controller was in idle state (no application running) and Intel® Turbo Boost Technology was enabled.

» Work load: Idle

For this measurement all processor cores and the graphics controller were in idle state (no application running) and Intel® Turbo Boost Technology was enabled.

» Work load: Typical

For this measurement all processor cores were operating at maximum work load and the graphics controller was performing basic operation (e.g. dual-screen output configuration with no 3D graphics application running) while Intel® Turbo Boost Technology was disabled. These values represent the power dissipation reached under realistic, OS-controlled applications with the processor operating at maximum performance.

» Work load: Maximum

These values represent the maximum power dissipation achieved through the use of specific tools to heat up the processor cores and graphics controller. For this measurement Intel® Turbo Boost Technology was enabled. These values are unlikely to be reached in real applications.

Note: To support the extended temperature range (+70°C), the maximum power consumption of the processors must be reduced. The Intel® Core™ i7-4700EQ processor supports the cTDP-Down mode to 37 W. The maximum power consumption of the Intel® Core™ i7-4860EQ and Intel® Core™ i5-4400E processors can be reduced to approx. 10 W using the Power Limit Reduction feature. This feature can be configured via the **kBoardConfig** uEFI Shell command. For information on this command, refer to the Chapter 9, uEFI BIOS.

Table 43: Workload: uEFI Shell

NOMINAL VOLTAGE	Core™ i7-4860EQ (SV) 1.8 GHz, GT3e	Core™ i7-4700EQ (SV) 2.4 GHz, GT2	Core™ i7-4700EQ (SV) 1.7 GHz, GT2	Core™ i5-4400E (SV) 2.7 GHz, GT2
+12 V	0.1 W	0.1 W	0.1 W	0.1 W
5 V	15.0 W	15.0 W	15.0 W	15.0 W
3.3 V	7.0 W	7.0 W	7.0 W	7.0 W
Total	22.1 W	22.1 W	22.1 W	22.1 W

Table 44: Workload: Idle

NOMINAL VOLTAGE	Core™ i7-4860EQ (SV) 1.8 GHz, GT3e	Core™ i7-4700EQ (SV) 2.4 GHz, GT2	Core™ i7-4700EQ (SV) 1.7 GHz, GT2	Core™ i5-4400E (SV) 2.7 GHz, GT2
+12 V	0.1 W	0.1 W	0.1 W	0.1 W
5 V	6.0 W	6.0 W	6.0 W	6.0 W
3.3 V	7.0 W	7.0 W	7.0 W	7.0 W
Total	13.1 W	13.1 W	13.1 W	13.1 W

Table 45: Workload: Typical

NOMINAL VOLTAGE	Core™ i7-4860EQ (SV) 1.8 GHz, GT3e	Core™ i7-4700EQ (SV) 2.4 GHz, GT2	Core™ i7-4700EQ (SV) 1.7 GHz, GT2	Core™ i5-4400E (SV) 2.7 GHz, GT2
+12 V	--	0.1 W	0.1 W	0.1 W
5 V	--	28.0 W	25.0 W	24.0 W
3.3 V	--	8.0 W	8.0 W	8.0 W
Total	--	36.1W	33.1W	32.1 W

Table 46: Workload: Maximum

NOMINAL VOLTAGE	Core™ i7-4860EQ (SV) 1.8 GHz, GT3e	Core™ i7-4700EQ (SV) 2.4 GHz, GT2	Core™ i7-4700EQ (SV) 1.7 GHz, GT2	Core™ i5-4400E (SV) 2.7 GHz, GT2
+12 V	0.1 W	0.1 W	0.1 W	0.1 W
5 V	51.0 W	51.0 W	40.0 W	40.0 W
3.3 V	12.0 W	12.0 W	12.0 W	12.0 W
Total	63.0 W	63.0 W	52.1 W	52.1 W

4.2.1 Power Consumption of the CP6005(X)-SA Accessories

The following table indicates the power consumption of the CP6005(X)-SA accessories.

Table 47: Power Consumption of CP6005(X)-SA Accessories

POWER CONSUMPTION	POWER 5 V	POWER 3.3 V
DDR3L SDRAM update from 4 GB to 8 GB	—	approx. 1.0 W
DDR3L SDRAM update from 4 GB to 16 GB	—	approx. 1.0 W
SATA Flash module	—	approx. 1.0 W

4.2.2 Power Consumption per Gigabit Ethernet Port

The following table indicates the power consumption per Gigabit Ethernet port.

Table 48: Power Consumption per Gigabit Ethernet Port

POWER CONSUMPTION	POWER 5 V	POWER 3.3 V
One 1000 Mb/s Ethernet port connected	—	approx. 0.5 W

4.2.3 Power Consumption per 10 Gigabit Ethernet Port (CP6005X-SA)

The following table indicates the power consumption per 10 Gigabit Ethernet port.

Table 49: Power Consumption per 10 Gigabit Ethernet Port

POWER CONSUMPTION	POWER 5 V	POWER 3.3 V
One 10GBASE-KR Ethernet port connected and active	—	approx. 1.3 W

4.2.4 Power Consumption of PMC Module

A maximum power of 7.5 W is available on the PMC slot. This is in accordance with the draft standard P1386/Draft 2.4a. The maximum power of 7.5 W can be arbitrarily divided on the 3.3 V and 5 V voltage lines.

The following table indicates the current of a PMC module.

Table 50: PMC Module Current

VOLTAGE	CONTINUOUS CURRENT	PEAK CURRENT
3.3 V	2.27 A	3.0 A
5 V	1.5 A	2.0 A
+12 V	0.6 A	0.8 A
-12 V	0.4 A	0.4 A

4.2.5 Power Consumption of XMC Modules

A maximum power of 20 W is available on the XMC slot and it can be arbitrarily divided on the 3.3 V and 5 V (VPWR) voltage lines. XMC modules are based on 3.3 V power along with variable power (VPWR) defined as either 5 V or 12 V in the ANSI/VITA 42.0-200x XMC Switched Mezzanine Card Auxiliary Standard specification. On the CP6005(X)-SA, the VPWR is configured to 5 V.

The following table indicates the current of an XMC module.

Table 51: XMC Module Current

VOLTAGE	CONTINUOUS CURRENT	PEAK CURRENT
3.3 V	1.0 A	1.25 A
5 V (VPWR)	3.0 A	3.5 A
+12 V	0.6 A	0.8 A
-12 V	0.4 A	0.4 A

Note: XMC integrators should carefully review the power ratings, cooling capacity and airflow requirements in the application prior to installation of an XMC module on the CP6005(X)-SA.

5 Thermal Considerations

The thermal characteristic graphs shown in the following sections are intended to serve as guidance for reconciling the required computing power with the necessary system volumetric airflow over the ambient temperature. The graphs contain two curves representing upper level working points based on different levels of average CPU utilization. When operating below the corresponding curve, the CPU runs without any intervention of thermal supervision (the CPU is below 100°C). When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop (the CPU is at 125°C) in order to protect the CPU and the chipset from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

An airflow of 2.0 m/s to 3.0 m/s is a typical value for a standard Kontron ASM rack. For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be determined for such environments.

How to read the diagram

Select a specific CPU and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must be more than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth. The volumetric flow rate is specified in m^3/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m^3/h; 1 m^3/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s (meter-per-second) or in fps (feet-per-second) respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps

The following figures illustrate the thermal operational limits of the CP6005(X)-SA taking into consideration power consumption vs. ambient air temperature vs. airflow rate.

Note: The CP6005(X)-SA must be operated within the thermal operational limits indicated below.

5.1 Operational Limits for the CP6005(X)-SA

Figure 8: CP6005(X)-SA with Core™ i7-4860EQ (SV), 1.8 GHz

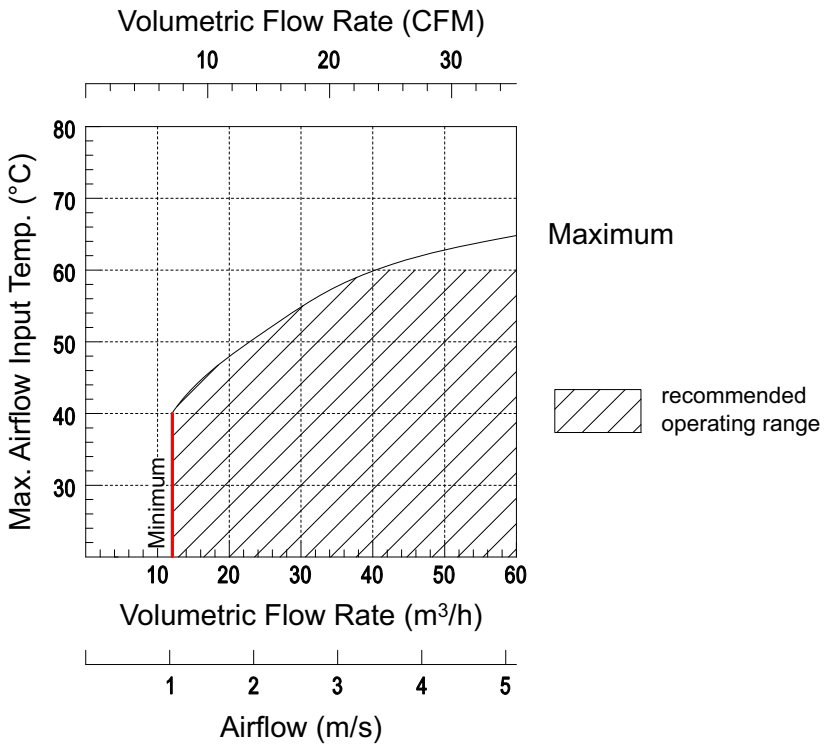


Figure 9: CP6005(X)-SA with Core™ i7-4700EQ (SV), 2.4 GHz

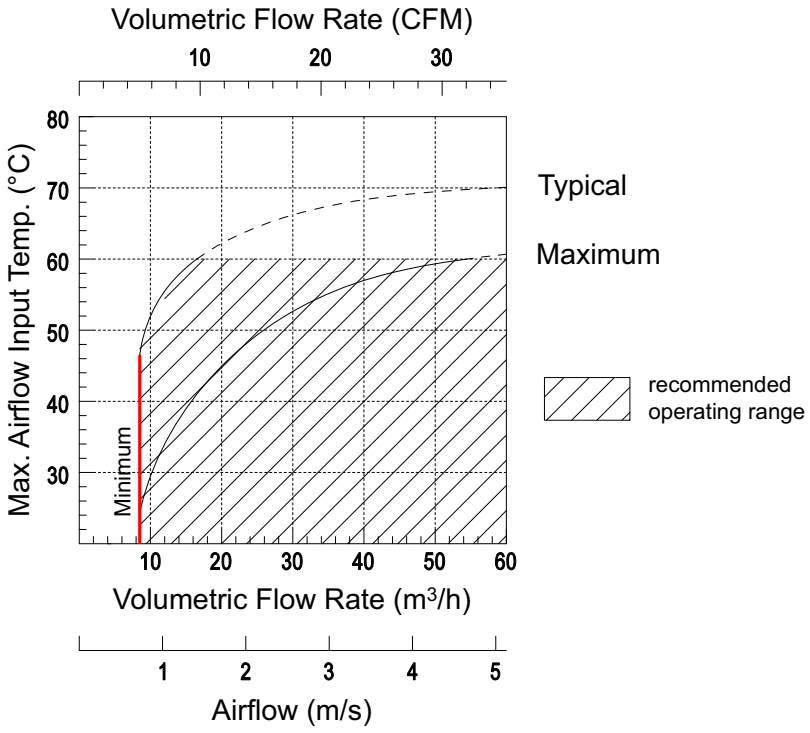


Figure 10: CP6005(X)-SA with Core™ i7-4700EQ (SV), 1.7 GHz

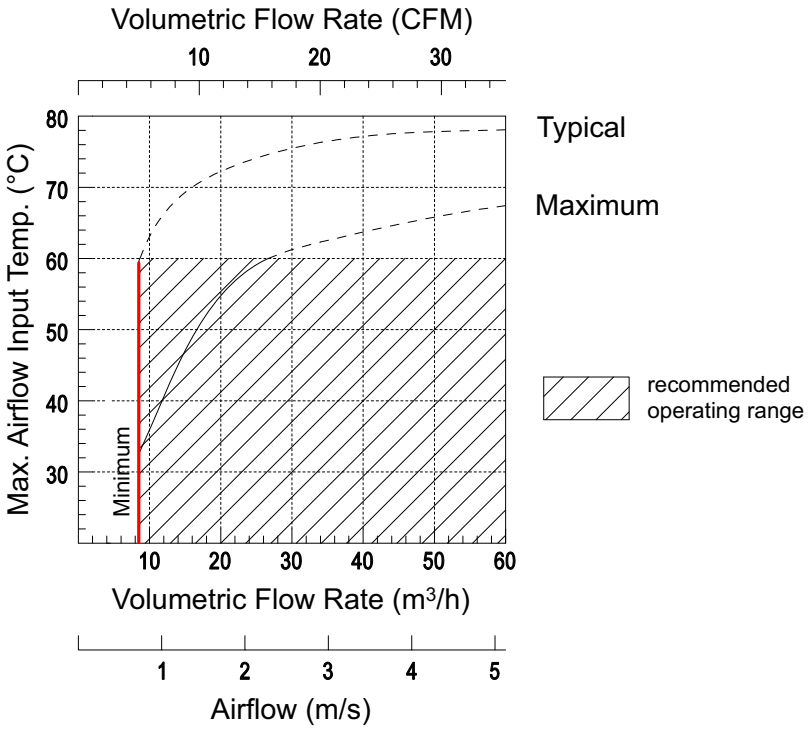
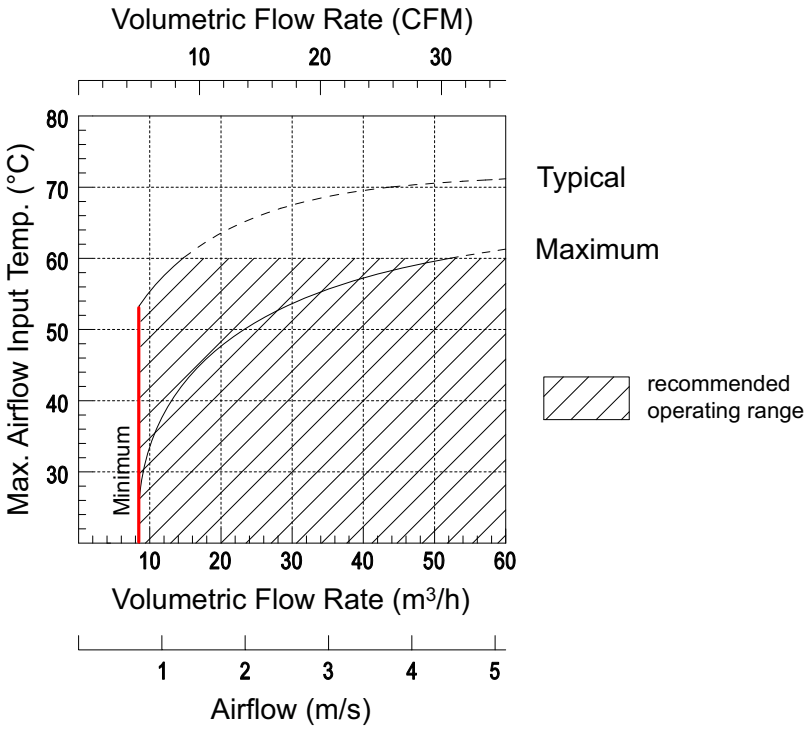


Figure 11: CP6005(X)-SA with Core™ i5-4400E (SV), 2.7 GHz



5.1.1 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the CP6005(X)-SA must also be considered. Devices such as HDDs, SSDs, PMC modules, XMC modules, and SATA Flash modules which are directly attached to the CP6005(X)-SA must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions. In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

Note: As Kontron assumes no responsibility for any damage to the CP6005(X)-SA or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP6005(X)-SA complies with the thermal considerations set forth in this document.

6 CP6005(X)-SA-MK2.5-SATA Assembly Kit

The optional CP6005(X)-SA-MK2.5-SATA assembly kit includes the MMADP-SATA01 module and the necessary components required for mounting the 2.5" SATA HDD/SSD on the CP6005(X)-SA.

6.1 MMADP-SATA01 Module Overview

The MMADP-SATA01 module has been designed for use with the Kontron CP6005(X)-SA board and enables the user to connect an onboard 2.5" SATA HDD/SSD to the CP6005(X)-SA.

Note: If the MMADP-SATA01 module is mounted on the CP6005(X)-SA, the SATA Flash module cannot be used with the CP6005(X)-SA.

6.2 Technical Specifications

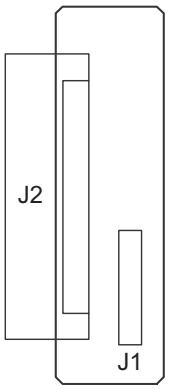
Table 52: MMADP-SATA01 Main Specifications

MMADP-SATA01		SPECIFICATIONS
Interface	Board-to-Board Connectors	One 34-pin, male, board-to-board connector, J1, for connection to the CP6005(X)-SA
	SATA Connector	One 22-pin SATA connector, J2
General	Power Supply for SATA devices	3.3 V and 5 V (12 V not available)
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +70°C Extended Storage: -40°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Board Weight	ca. 5 grams (without HDD/SSD)

6.3 MMADP-SATA01 Module Layout

The MMADP-SATA01 module includes one board-to-board connector, J1, for connection to the CP6005(X)-SA board and one standard SATA connector, J2, for connection to an onboard 2.5" SATA HDD/SSD device.

Figure 12: MMADP-SATA01 Module Layout



7 SATA Flash Module

The CP6005(X)-SA provides an optional SATA Flash module with up to 64 GB NAND flash memory. The SATA Flash module is connected to the CP6005(X)-SA via the board-to-board connectors J17 located on the CP6005(X)-SA and J2 located on the SATA Flash module. The SATA Flash module has been optimized for embedded systems providing high performance, reliability and security.

Note: If the SATA Flash module is mounted on the CP6005(X)-SA, the MMADP-SATA01 module cannot be used with the CP6005(X)-SA.

7.1 Technical Specifications

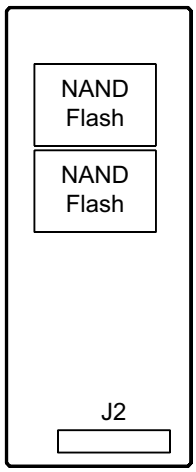
Table 53: SATA Flash Module Main Specifications

MMADP-SATA01		SPECIFICATIONS
Interface	Board-to-Board Connector	One 34-pin, male, board-to-board connector, J2, for connection to the CP6005(X)-SA
Memory	Memory	Up to 64 GB SLC-based NAND flash memory » Built-in full hard disk emulation » Up to 100 MB/s read rate » Up to 90 MB/s write rate
General	Power Consumption	typ. 1.0 W; 3.3 V supply
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +70°C Extended (on request) Storage: -40°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	70 mm x 28 mm
	Board Weight	ca. 14 grams

Note: Write protection is available for this module. Contact Kontron for further assistance if write protection is required.

7.2 SATA Flash Module Layout

Figure 13: SATA Flash Module Layout (Bottom View)



8 Installation

This chapter is oriented towards an application environment. Some aspects may, however, be applicable to a development environment.

8.1 Safety

To ensure personnel safety and correct operation of this product, the following safety precautions must be observed:

- All operations involving the CP6005(X)-SA require that personnel be familiar with system equipment, safety requirements and the CP6005(X)-SA.
- This product contains electrostatically sensitive components which can be seriously damaged by electrical static discharge (ESD). Therefore, proper handling must be ensured at all times.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.
- Do not touch components, connector-pins or traces.

Kontron assumes no liability for any damage resulting from failure to comply with these requirements.

8.2 General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

8.3 Board Installation

The CP6005(X)-SA is designed for use either as a system board or as an autonomous CPU board in a peripheral slot.

When installed in the system slot, the CP6005(X)-SA provides all required functions for supporting the hot swapping of peripheral boards which are capable of being hot swapped.

When installed in a peripheral slot, the CP6005(X)-SA operates autonomously, meaning that it only draws power from the backplane.

8.3.1 Hot Swap Insertion

Prior to following the steps below, ensure that the safety requirements are met.

To insert the CP6005(X)-SA in a running system proceed as follows:

1. Ensure that the board ejection handles are open.
2. Insert the board into the slot designated until it makes contact with the backplane connectors.
3. Using the ejector handles, engage the board with the backplane. When the ejector handles are closed, the board is engaged.
4. The blue HS LED turns on and then off indicating that the CP6005(X)-SA is operating.
5. Fasten the front panel retaining screws.
6. Connect all external interfacing cables to the board as required.

8.3.2 Hot Swap Removal

Prior to following the steps below, ensure that the safety requirements are met. When removing a board from the system, particular attention must be paid to the components that may be hot, such as heat sink, etc.

To remove the CP6005(X)-SA from a running system proceed as follows:

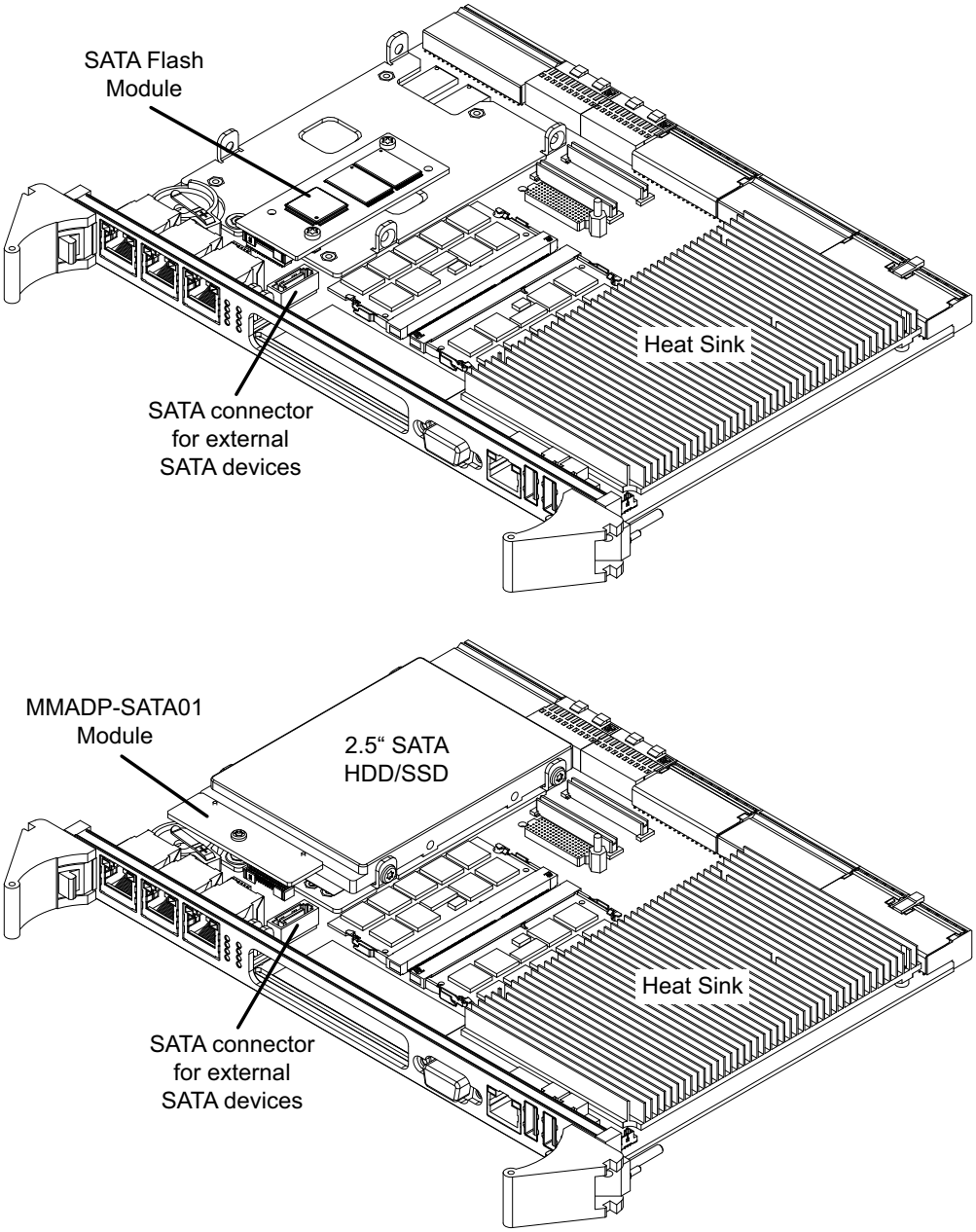
1. Unlock the board ejection handles by pressing their release buttons.
   The blue HS LED starts blinking indicating that the shutdown process has begun.
2. After approximately 1 to 15 seconds, the HS LED turns on steady indicating that the CP6005(X)-SA may be removed from the system.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Using the ejector handles, disengage the board from the backplane and remove it from the system.

8.4 Installation of Peripheral Devices

The CP6005(X)-SA is designed to accommodate various peripheral devices, such as SATA, PMC, XMC, and rear I/O devices. The following figure shows the placement of the SATA Flash module and the MMADP-SATA01 module, which is required for connecting an onboard HDD/SSD to the CP6005X-SA.

Prior to installation of a peripheral device, ensure that the safety requirements are met. Special attention must be paid to avoid touching any components that may be hot, such as heat sink, etc.

Figure 14: Connecting a Peripheral Device to the CP6005X-SA



8.4.1 SATA Flash Module Installation

A SATA Flash module may be connected to the CP6005(X)-SA via the onboard connector, J16. This optionally available module must be physically installed on the CP6005(X)-SA prior to installation of the CP6005(X)-SA in a system. During installation it is necessary to ensure that the SATA Flash module is properly seated in the onboard connector J16, i.e. the pins are aligned correctly and not bent.

8.4.2 Installation of External SATA Devices

The following information pertains to external SATA devices which may be connected to the CP6005(X)-SA via normal cabling.

Some symptoms of incorrectly installed SATA devices are:

- Device on a SATA channel does not spin up: check power cables and cabling. May also result from a bad power supply or SATA device.
  The SATA connector on the CP6005(X)-SA provides only a data connection. The power for this device must be supplied by a separate connector. For further information, refer to the respective documentation of the device.
- SATA device fail message at boot-up: may be a bad cable or lack of power going to the drive.

8.4.3 Onboard 2.5” HDD/SSD Installation

One 2.5” SATA HDD/SSD may be directly connected to the board via the adapter module MMADP-SATA01 and the J16 connector. This module is required to provide SATA interfacing to the HDD/SSD. For further information regarding the MMADP-SATA01 module, refer to Chapter 6.

8.4.4 PMC Module Installation

The CP6005(X)-SA supports the installation of a PMC module via the J20 to J21 connectors. For information on the installation of the PMC module, refer to the documentation provided with the module.

8.4.5 XMC Module Installation

The CP6005(X)-SA supports the installation of an XMC module via the J19 connector. For information on the installation of the XMC module, refer to the documentation provided with the module.

8.4.6 Rear Transition Module Installation

For physical installation of rear transition modules, refer to the documentation provided with the module itself.

8.5 Battery Replacement

The CP6005(X)-SA RTC may be backed up using a single UL-approved CR2025, 3.0 V “coin cell” lithium battery from one of three possible points of installation:

- onboard
- on the rear transition module

Only one battery may be installed at a time. Refer to Table 1 for battery requirements.

9 uEFI BIOS

9.1 Starting the uEFI BIOS

The CP6005(X)-SA is provided with a Kontron-customized, pre-installed and configured version of SecureCore Tiano™ (referred to as uEFI BIOS in this manual), Phoenix BIOS firmware based on the Unified Extensible Firmware Interface (uEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the CP6005(X)-SA.

The uEFI BIOS comes with a Setup program which provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The Setup program allows the accessing of various menus which provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS Setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <F2> key.
4. If the uEFI BIOS is password-protected, a request for password will appear.

   Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A Setup menu will appear.

The CP6005(X)-SA uEFI BIOS Setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the Setup screens. The following table provides information concerning the usage of these hot keys.

Table 54: Navigation

HOT KEY	DESCRIPTION
<F1>	The <F1> key is used to invoke the General Help window.
<F5> or <->	The <F5> key or the <Minus> key is used to select the next lower value within a field.
<F6> or <+>	The <F6> key or the <Plus> key is used to select the next higher value within a field.
<F9>	The <F9> key is used to load the standard default values.
<F10>	The <F10> key is used to save the current settings and exit the uEFI BIOS Setup.
<→> <←>	The <Left/Right> arrows are used to select major Setup menus on the menu bar. For example: Main screen, Advanced screen, Security screen, etc.
<↑> <↓>	The <Up/Down> arrows are used to select fields in current menu, for example a Setup function or a sub-screen.
<ESC>	The <ESC> key is used to exit a major Setup menu and enter the Exit Setup menu. Pressing the <ESC> key in a sub-menu causes the next higher menu level to be displayed.
<RETURN>	The <RETURN> key is used to execute a command or select a submenu.

9.2 Setup Menus

The Setup utility features four menus listed in the selection bar at the top of the screen:

- Main
- Advanced
- Security
- Boot
- Exit

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white.

Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an Item Specific Help window providing an explanation of the respective function.

9.2.1 Main Setup Menu

Upon entering the uEFI BIOS Setup program, the Main Setup menu is displayed. This screen lists the Main Setup menu sub-screens and provides basic system information as well as functions for setting the system time and date.

Table 55: Main Setup Menu Sub-Screens and Functions

SUB-SCREEN	FUNCTION	DESCRIPTION
System Information	BIOS Version, Build Time, etc.	Read-only field. Displays information about the system BIOS, processor, memory, etc.
Boot Features	CSM Support	Enables/Disables Compatibility Support Module
	Quick Boot	Enables/Disables time-optimized POST, causing certain preconfigured OEM optimizations to be made when the system boots.
	USB Legacy	Enables/Disables support for USB devices including mouse, keyboard, mass storage, and so on.
	Console Redirection	Enables/Disables console redirection over serial port.
	Terminal Type	Selects the terminal type to be emulated.
	Baudrate	Selects the baud rate of the serial port.
	Flow Control	Specifies the type of flow control to be used for the serial port.
	Continue C.R. after POST	Enables/Disables console redirection after the operating system has loaded.

9.2.2 Advanced Setup Menu

The Advanced Setup menu provides sub-screens and functions for advanced configuration.

Note: Setting items on this screen to incorrect values may cause the system to malfunction.

Table 56: Advanced Setup Menu Sub-Screens and Functions

SUB-SCREEN	FUNCTION	DESCRIPTION
Processor Configuration	CPU Flex Ratio Override	Enables/Disables CPU Flex Ratio Programming.
	CPU Flex Ratio Settings	CPU Flex Ratio Settings: This value must be between Max. Efficiency Ratio (LFM) and Maximum non-turbo ratio set by Hardware (HFM). See Table 5, Features of the Processors Supported on the CP6005(X)-SA, for possible LFM/HFM values. The active nominal CPU frequency is Ratio*100MHz.
ME Configuration	ME FW Downgrade	Enables/Disables ME FW Downgrade function.

9.2.3 Security Setup Menu

The Security Setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The CP6005(X)-SA provides no factory-set passwords.

Table 57: Security Setup Menu Functions

FUNCTION	DESCRIPTION
Supervisor Password is:	Read-only field.
User Password is:	Read-only field.
Set Supervisor Password	Sets or clears the Supervisor Password.
Supervisor Hint String	Press “Enter” to specify a hint string for the Supervisor Password.
Set User Password	Sets or clears the User Password.
User Hint String	Press “Enter” to specify a hint string for the User Password.
Min. password length	Specifies the minimum password length.
Authenticate User on Boot	Enables the user authentication prompt on the boot.
HDD Password Select	Specifies whether to enable User-only support for HDD or User and Master support.
HDD00 Password State	Read-only field.
Set HDD00 User Password	Specifies and confirms the HDD User Password.
Set HDD00 Master Password	Specifies and confirms the HDD Master Password.
TPM Support	Enables/Disables TPM support.

Note: If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.

Table 58: TPM Configuration Sub-Screen

FUNCTION	DESCRIPTION
Current TPM State	Read-only field.
TPM Action	Enacts TPM Action. Note: Most TPM actions require TPM to be Enabled to take effect.
Omit Boot Measurements	Enabling this option causes the system to omit recording boot device attempts in PCR[4].

9.2.3.1 Remember the Password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords may lead to being completely locked out of the system.

If the system cannot be booted because neither the User Password nor the Supervisor Password are known, refer to the Chapter 3.1, for information about clearing the uEFI BIOS settings, or contact Kontron for further assistance.

Note: The HDD security passwords cannot be cleared using the above method.

9.2.4 Boot Setup Menu

The Boot Setup menu lists the for boot device priority order, which is dynamically generated.

Table 59: Boot Priority Order

FUNCTION		DESCRIPTION
Boot Priority Order	1. Internal Shell	Keys used to view or configure devices: <↑> and <↓> arrows select a device. <+> and <-> move the device up or down. <Shift + 1> enables or disables a device. <Del> deletes an unprotected device.
	2. USB FDD:	
	3. USB CD:	
	4. ATAPI CD:	
	5. USB HDD:	
	6. ATA HDD0:	
	7. ATA HDD1:	
	8. ATA HDD2:	
	9. ATA HDD3:	
	10. ATA HDD4:	
	11. ATA HDD5:	
	12. Other HDD:	
	13. PCI LAN:	

9.2.5 Exit Setup Menu

The Exit Setup menu provides functions for handling changes made to the uEFI BIOS settings and the exiting of the Setup program.

Table 60: Exit Setup Menu Functions

FUNCTION	DESCRIPTION
Exit Saving Changes	Equal to F10, save all changes of all menus, then exit the uEFI BIOS Setup. Finally, resets the system automatically.
Exit Discarding Changes	Never save changes, then exit the uEFI BIOS Setup.
Load Setup Defaults	Equal to F9. Load standard default values.
Discard Changes	Load the original value of this boot time, not the default Setup value.
Save Changes	Save all changes of all menus, but do not reset system.

9.3 The uEFI Shell

The Kontron uEFI BIOS features a built-in and enhanced version of the uEFI Shell. For a detailed description of the available standard shell scripting refer to the EFI Shell User's Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage (http://sourceforge.net/projects/efi-shell/files/documents/).

Please note that not all shell commands described in the EFI Shell Command Manual are provided by the Kontron uEFI BIOS.

9.3.1 Introduction, Basic Operation

The uEFI Shell forms an entry into the uEFI boot order and is the first boot option by default.

9.3.1.1 Entering the uEFI Shell

To enter the uEFI Shell, follow the steps below:

1. Power on the board.
2. Ignore the message: "Press the <F2> key".
3. Press the ESC key within 5 seconds after a message such as the one below appears:

```
EFI Shell version 2.31 [4660.22136]
Current running mode 1.1.2
Device mapping table
blk0     :Removable HardDisk - Alias hd33b0b0b fs0
          Acpi(PNP0A03,0)/Pci(1D|7)/Usb(1, 0)/Usb(1, 0)/HD(Part1,Sig17731773)
...
Press the ESC key within 5 seconds to skip startup.nsh, and any other key to
continue.
```

The output produced by the device mapping table can vary depending on the board's configuration.

If the ESC key is pressed before the 5-second timeout has elapsed, the shell prompt is shown:

```
Shell>
```

9.3.1.2 Exiting the uEFI Shell

To exit the uEFI Shell, follow one of the steps below:

1. Invoke the **exit** uEFI Shell command to select the boot device in the boot menu for the OS to boot from.
2. Reset the board using the **reset** uEFI Shell command.

9.3.2 Kontron-Specific uEFI Shell Commands

The Kontron uEFI implementation provides the following additional commands related to the specific HW features of the Kontron system.

Table 61: Kontron-Specific uEFI Shell Commands

COMMAND	DESCRIPTION
kBoardConfig	Configures non-volatile board settings, such as: » Pxe » PrimaryDisplay » VGA » SataMode » SataSpeed » Sata2Hotplug » Sata3Hotplug » Sata4Hotplug » Sata5Hotplug » IntelVT » IntelHT » SpeedStep » CpuTurbo » cTDP » C3State » C6State » C7State » WrProtSystem » ComBMode » AutoUpdate If AutoUpdate is enabled, an automatic update procedure from the connected mass storage device is initiated after a reset. The update status is indicated in the log file located in the directory where the firmware images are stored. **Note:** The parameters of the kBoardConfig command are not case-sensitive.
kBoardInfo	Shows a summary of board-specific data and displays/checks various parameters such as the current uEFI BIOS revision, etc.
kBootScript	Manages the flash-stored startup script If the shell is launched by the boot process, it executes a shell script stored in the flash. If the shell script terminates, the shell will continue the boot process. However, the shell script can also contain any other boot command.
kFlash	Programs and verifies the SPI boot flashes holding the uEFI BIOS code uEFI BIOS binary files must be available from connected mass storage devices, such as USB flash drive or harddisk.
kIpmi	Executes a comprehensive set of IPMI functions from the uEFI Shell using the KCS interface and upgrades the IPMI firmware.
kNvram	Manages the NVRAM to restore the system's default settings Since all uEFI settings are stored inside the NVRAM, the default settings are loaded after invoking this command.

Table 61: Kontron-Specific uEFI Shell Commands

COMMAND	DESCRIPTION
kPassword	Controls uEFI Setup and Shell passwords This command is used to determine the status of both passwords (set or not set) and to set or clear the uEFI Shell and Setup passwords. Both user and superuser (Supervisor) passwords can be controlled with this command. Call without options to get current password status. Entering an empty password clears the password.
kRamdisk	Creates and manages RAMdisks This command is used to perform file operations when no real filesystem is connected to the system.
kReset	Controls the board's reset behavior This command controls if the board shall react on a CompactPCI backplane reset if it is used in a peripheral slot. It has no effect if the board is installed in the CompactPCI system slot. The parameter of this command is volatile and set to off at the next start.
kUpdate	Controls the Kontron common update tool When using the **kUpdate** command, the structure of the ZIP archive must not be altered. **kUpdate** automatically starts the update procedure via **kUpdate -u.** If a certain image is intended to be used, enter **kUpdate -s** to select the respective image.
kWatchdog	Configures the Kontron onboard Watchdog This command is used to enable the Kontron onboard Watchdog with reset target before OS boot. This can be used to detect if the OS fails to boot and react by reset.

The uEFI Shell commands are not case-sensitive. Each uEFI Shell command is provided with a detailed online help that can be invoked by entering "<cmd> <space> <-?>" in the command line. To display the uEFI Shell command list, enter <help> or <?> in the command line.

9.4 uEFI Shell Scripting

9.4.1 Startup Scripting

If the ESC key is not pressed and the timeout is run out, the uEFI Shell tries to execute some startup scripts automatically. It searches for scripts and executes them in the following order:

1. Kontron flash-stored startup script
2. If there is no Kontron flash-stored startup script present, the uEFI-specified **`startup.nsh`** script is used. This script must be located on the root of any of the attached FAT formatted disk drive.
3. If none of the startup scripts is present or the startup script terminates, the default boot order is continued.

9.4.2 Create a Startup Script

Startup scripts can be created using the uEFI Shell built-in editor **edit** or under any OS with a plain text editor of your choice. To create a startup shell script, simply save the script on the root of any FAT-for-

matted drive attached to the system. To copy the startup script to the flash use the **kBootScript** uEFI Shell command.

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the **kRamdisk** uEFI Shell command.

9.4.3 Examples of Startup Scripts

9.4.3.1 Execute Shell Script on Other Harddrive

This example (`startup.nsh`) executes the shell script named `bootme.nsh` located in the root of the first detected disc drive (`fs0`).

```
fs0:
bootme.nsh
```

9.4.3.2 Enable Watchdog

The uEFI Shell provides an environment variable used to control the execution flow. The following sample start-up script shows the uEFI Shell environment variable `wdt_enable` used to control the Watchdog.

```
echo -off
echo “Executing sample startup.nsh...”
if %wdt_enable% == “on” then
   kwatchdog -t 15
   echo “Watchdog enabled”
endif
```

To create a uEFI Shell environment variable, use the **set** uEFI Shell command as shown below:

```
Shell> set wdt_enable on
Shell> set
   wdt_enable : on
Shell> reset
```

9.4.3.3 Handling the Startup Script in the SPI Boot Flash

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the following instructions:

1. Press <ESC> during power-up to log into the uEFI Shell.

2. Create a RAM disk and set the proper working directory as shown below:

```
Shell> kramdisk -s 3 -c -m myramdisk
Shell> myramdisk:
```

3. Enter the sample start-up script mentioned above in this section using the **edit** uEFI Shell command.

```
myramdisk:\> edit boot.nsh
```

4. Save the start-up script to the SPI boot flash using the **kBootScript** uEFI Shell command.

```
myramdisk:\> kbootscript -p boot.nsh
```

5. Reset the board to execute the newly installed script using the **reset** uEFI Shell command.

```
myramdisk:\> reset
```

6. If a script is already installed, it can be edited using the following **kBootScript** uEFI Shell commands.

```
myramdisk:\> kbootscript -g boot.nsh
myramdisk:\> edit boot.nsh
```

9.5 Firmware Update

Firmware updates are typically delivered as a ZIP archive containing only the firmware images. The content of the archive with the directory structure must be copied on a data storage device with FAT partition. If the command **kBoardConfig AutoUpdate** has been enabled, the images are automatically detected during boot-up and an update of the uEFI BIOS or the IPMI firmware is carried out.

9.5.1 Updating the uEFI BIOS

9.5.1.1 uEFI BIOS Fail-Over Mechanism

The CP6005(X)-SA has two SPI boot flashes programmed with the uEFI BIOS, a standard SPI boot flash and a recovery SPI boot flash. The basic idea behind that is to always have at least one working uEFI BIOS flash available regardless if there have been any flashing errors or not.

9.5.1.2 Updating Procedure

The standard SPI boot flash can be updated with the latest uEFI BIOS from the ZIP archive using the **kUpdate -u** or the **kFlash -p** uEFI Shell command. When using the **kUpdate** command, the directory structure of ZIP archive must not be altered. The update status is indicated in the log file located in the directory where the firmware images are stored.

9.5.1.3 uEFI BIOS Recovery

In case of the standard SPI boot flash being corrupted and therefore the board not starting up, the board can be booted from the recovery SPI boot flash if the DIP switch SW1, switch 2 is set to ON. For further information, refer to the Chapter 3.1, DIP Switch Configuration.

Note: The uEFI BIOS code and settings are stored in the SPI boot flashes. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash. Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

9.5.1.4 Determining the Active Flash

Sometimes it may be necessary to check which flash is active. On the uEFI BIOS, this information is available via the **kBoardInfo** uEFI Shell command.

9.5.2 Updating the IPMI Firmware

9.5.2.1 IPMI Rollback Mechanism

The CP6005(X)-SA's IPMI controller has an internal flash, where the boot block or the active IPMI firmware is running from, as well as an external flash, where two IPMI firmware images are stored, namely:

- a copy of the currently active image, and
- the previously good image or the newly downloaded image.

During firmware upgrade, the previously good image in the external flash is replaced by the newly downloaded image. Then the boot block activates the new image by copying it to the internal flash. If the newly downloaded image was successfully activated, its copy in the external flash is now the active image. The copy of the old active image becomes the previously good image.

Manual rollback is also possible via the **kIpmi hpm rollback** uEFI Shell command.

9.5.2.2 Determining the Active IPMI Firmware Image

To determine the active IPMI firmware image, use the **kIpmi info** command.

9.5.2.3 Updating Procedure

The active IPMI firmware image can be updated with the latest HPM.1 file from the ZIP archive using the **kUpdate -u** or the **kIpmi hpm upgrade** uEFI Shell command. When using the **kUpdate** command, the structure of ZIP archive must not be altered.

10 IPMI Firmware

10.1 Overview

The CP6005(X)-SA provides an IPMI controller (NXP® ARM7) with 512 kB of internal firmware flash as well as external firmware flash for firmware upgrade and rollback. The IPMI controller carries out IPMI commands such as monitoring several onboard temperature conditions, board voltages and the power supply status, and managing hot swap operations. The IPMI controller is accessible via two IPMBs, one host Keyboard Controller Style (KCS) interface and up to four Gigabit Ethernet interfaces (IOL).

The CP6005(X)-SA is fully compliant with the IPMI - Intelligent Platform Management Interface v2.0 and the PICMG 2.9 R1.0 specifications.

The following are key features of the CP6005(X)-SA's IPMI firmware:

- Keyboard Controller Style (KCS) interface
- Dual-port IPMB interface for out-of-band management and sensor monitoring
- IPMI over LAN (IOL) and Serial over LAN (SOL) support
- Sensor Device functionality with configurable thresholds for monitoring board voltages, CPU state, board reset, etc.
- FRU Inventory functionality
- System Event Log (SEL), Event Receiver functionalities
- Sensor Data Record Repository (SDRR) functionality
- IPMI Watchdog functionality (power-cycle, reset)
- Board monitoring and control extensions:
  - Graceful shutdown support
  - uEFI BIOS fail-over control: selection of the SPI boot flash (standard/recovery)
- Field-upgradeable IPMI firmware:
  - via the KCS, IPMB or IOL interfaces
  - Download of firmware does not break the currently running firmware or payload activities
- Two flash banks with rollback capability: manual rollback or automatic in case of upgrade failure

For general information on the Kontron IPMI Firmware, refer to the IPMI Firmware User Guide.

10.2 IPMI Firmware and KCS Interface Configuration

Initially the default configuration of the IPMI firmware (KCS interface) is:

- IRQ = 11
- MODE = SMC
- IPMB = single-ported.

If this is the required configuration, no further action is required. If the configuration must be modified, the **kIpmi** uEFI Shell command is used to modify the configuration as required, e.g. “kIpmi irq [0|11]”, “kIpmi mode [smc|bmc]”, and “kIpmi ipmb [single-ported|dual-ported]”. For information on the **kIpmi** uEFI Shell command, refer to the uEFI BIOS Chapter.

The KCS interface serves for the communication between the CP6005(X)-SA’s payload and the IPMI controller. The IPMI OS kernel s require the KCS interface configuration during their loading time. The KCS interface configuration is available in the “IPMI Device Information Record” included in the SMBIOS table.

10.3 Supported IPMI and ATCA Commands

10.3.1 Standard IPMI Commands

The following table shows an excerpt from the command list specified in the IPMI specification 2.0. The shaded table cells indicate commands not supported by the CP6005(X)-SA IPMI firmware.

M = mandatory, O = optional

Table 62: Standard IPMI Commands

COMMAND	IPMI 2.0 SPEC. SECTION	NETFN	CMD	KONTRON SUPPORT ON IPMI CONTROLLER
IPM DEVICE “GLOBAL” COMMANDS				M
Get Device ID	20.1	App	01h	M / Yes
Cold Reset	20.2	App	02h	O / Yes
Warm Reset	20.3	App	03h	O / No
Get Self Test Results	20.4	App	04h	O / Yes
Manufacturing Test On	20.5	App	05h	O / No
Set ACPI Power State	20.6	App	06h	O / Yes
Get ACPI Power State	20.7	App	07h	O / Yes
Get Device GUID	20.8	App	08h	O / No
Broadcast “Get Device ID”	20.9	App	01h	M / Yes
BMC WATCHDOG TIMER COMMANDS				O
Reset Watchdog Timer	27.5	App	22h	O / Yes
Set Watchdog Timer	27.6	App	24h	O / Yes
Get Watchdog Timer	27.7	App	25h	O / Yes
BMC DEVICE AND MESSAGING COMMANDS				O
Set BMC Global Enables	22.1	App	2Eh	O / Yes

Table 62: Standard IPMI Commands (Continued)

COMMAND	IPMI 2.0 SPEC. SECTION	NETFN	CMD	KONTRON SUPPORT ON IPMI CONTROLLER
Get BMC Global Enables	22.2	App	2Fh	O / Yes
Clear Message Flags	22.3	App	30h	O / Yes
Get Message Flags	22.4	App	31h	O / Yes
Enable Message Channel Receive	22.5	App	32h	O / Yes
Get Message	22.6	App	33h	O / Yes
Send Message	22.7	App	34h	O / Yes
Read Event Message Buffer	22.8	App	35h	O / Yes
Get BT Interface Capabilities	22.9	App	36h	O / No
Get System GUID	22.14	App	37h	O / No
Get Channel Authentication Capabilities	22.13	App	38h	O / Yes
Session Control	22.15 to 22.20	App	39h to 3Dh	O / Yes
Get AuthCode	22.21	App	3Fh	O / No
Channel Commands	22.22 to 22.30	App	40h to 47h	O / Yes
User Commands	24.1 to 24.9	App	48h to 4Fh	O / Yes
Get Channel OEM Payload Info	24.10	App	50h	O / No
Master Write-Read	22.11	App	52h	O / Yes
Get Channel Cipher Suits	22.15	App	54h	O / No
Suspend/Resume Payload Encryption	24.3	App	55h	O / Yes
Set Channel Security Keys	22.25	App	56h	O / No
Get System Interface Capabilities	22.9	App	57h	O / No
CHASSIS DEVICE COMMANDS				O
Get Chassis Capabilities	28.1	Chassis	00h	O / Yes
Get Chassis Status	28.2	Chassis	01h	O / Yes
Chassis Control	28.3	Chassis	02h	O / Yes
Extended Chassis Control Commands	28.4 to 28.8	Chassis	03h, 04h, 0Ah, 05h, 06h	O / No
Set Power Cycle Interval	28.9	Chassis	0Bh	O / Yes
Extended Chassis Control Commands	28.11 to 28.13	Chassis	07h to 09h	O / No
Get POH Counter	28.14	Chassis	0Fh	O / Yes
EVENT COMMANDS				M
Set Event Receiver	29.1	S/E	00h	M / Yes
Get Event Receiver	29.2	S/E	01h	M / Yes
Platform Event (a.k.a. “Event Message”)	29.3	S/E	02h	M / Yes
PEF AND ALERTING COMMANDS	30.1 to 30.8	S/E	10h to 17h	O / No
SENSOR DEVICE COMMANDS				M
Get Device SDR Info	35.2	S/E	20h	M / Yes
Get Device SDR	35.3	S/E	21h	M / Yes
Reserve Device SDR Repository	35.4	S/E	22h	M / Yes
Get Sensor Reading Factors	35.5	S/E	23h	O / No
Set Sensor Hysteresis	35.6	S/E	24h	O / Yes

Table 62: Standard IPMI Commands (Continued)

COMMAND	IPMI 2.0 SPEC. SECTION	NETFN	CMD	KONTRON SUPPORT ON IPMI CONTROLLER
Get Sensor Hysteresis	35.7	S/E	25h	O / Yes
Set Sensor Threshold	35.8	S/E	26h	O / Yes
Get Sensor Threshold	35.9	S/E	27h	O / Yes
Set Sensor Event Enable	35.10	S/E	28h	O / Yes
Get Sensor Event Enable	35.11	S/E	29h	O / Yes
Re-arm Sensor Events	35.12	S/E	2Ah	O / No
Get Sensor Event Status	35.13	S/E	2Bh	O / No
Get Sensor Reading	35.14	S/E	2Dh	M / Yes
Set Sensor Type	35.15	S/E	2Eh	O / No
Get Sensor Type	35.16	S/E	2Fh	O / No
FRU DEVICE COMMANDS				M
Get FRU Inventory Area Info	34.1	Storage	10h	M / Yes
Read FRU Data	34.2	Storage	11h	M / Yes
Write FRU Data	34.3	Storage	12h	M / Yes
SDR DEVICE COMMANDS				O
Get SDR Repository Info	33.9	Storage	20h	O / Yes
Get SDR Repository Allocation Info	33.10	Storage	21h	O / Yes
Reserve SDR Repository	33.11	Storage	22h	O / Yes
Get SDR	33.12	Storage	23h	O / Yes
Add SDR	33.13	Storage	24h	O / Yes
Partial Add SDR	33.14	Storage	25h	O / Yes
Delete SDR	33.15	Storage	26h	O / Yes
Clear SDR Repository	33.16	Storage	27h	O / Yes
Get SDR Repository Time	33.17	Storage	28h	O / No
Set SDR Repository Time	33.18	Storage	29h	O / No
Enter SDR Repository Update Mode	33.19	Storage	2Ah	O / No
Exit SDR Repository Update Mode	33.20	Storage	2Bh	O / No
Run Initialization Agent	33.21	Storage	2Ch	O / Yes
SEL DEVICE COMMANDS				O
Get SEL Info	40.2	Storage	40h	O / Yes
Get SEL Allocation Info	40.3	Storage	41h	O / Yes
Reserve SEL	40.4	Storage	42h	O / Yes
Get SEL Entry	40.5	Storage	43h	O / Yes
Add SEL Entry	40.6	Storage	44h	O / Yes
Partial Add SEL Entry	40.7	Storage	45h	O / No
Delete SEL Entry	40.8	Storage	46h	O / Yes
Clear SEL	40.9	Storage	47h	O / Yes
Get SEL Time	40.10	Storage	48h	O / Yes
Set SEL Time	40.11	Storage	49h	O / Yes
Get Auxiliary Log Status	40.12	Storage	5Ah	O / No

Table 62: Standard IPMI Commands (Continued)

COMMAND	IPMI 2.0 SPEC. SECTION	NETFN	CMD	KONTRON SUPPORT ON IPMI CONTROLLER
Set Auxiliary Log Status	40.13	Storage	5Bh	O / No
LAN DEVICE COMMANDS				O
Set LAN Configuration Parameters	23.1	Transport	01h	O / Yes
Get LAN Configuration Parameters	23.2	Transport	02h	O / Yes
Suspend BMC ARPs	23.3	Transport	03h	O / No
Get IP/UDP/RMCP Statistics	23.4	Transport	04h	O / Yes
SERIAL/MODEM DEVICE COMMANDS	25.1 to 25.12	Transport	10h to 1Bh	O / No
SOL COMMANDS				O
SOL Activating	26.1	Transport	20h	O / Yes
Set SOL Configuration Parameters	26.2	Transport	21h	O / Yes
Get SOL Configuration Parameters	26.3	Transport	22h	O / Yes

Note: Some of the above-mentioned commands, such as SDR device commands, work only if the IPMI controller is configured as BMC. For further information, refer to the IPMI specification 2.0.

10.3.2 AdvancedTCA and AMC Commands

The following table shows an excerpt from the command list specified in the PICMG 3.0 R 2.0 AdvancedTCA Base Specification and the PICMG AMC.0 Advanced Mezzanine Card Specification, R 1.0. The shaded table cells indicate commands not supported by the IPMI firmware.

M = mandatory

Table 63: Standard IPMI Commands

COMMAND	IPMI 2.0 SPEC. SECTION	NETFN	CMD	KONTRON SUPPORT ON IPMI CONTROLLER
AdvancedTCA				M
Get PICMG Properties	3-9	PICMG	00h	M / Yes
FRU Control	3-22	PICMG	04h	N/A
Get FRU LED Properties	3-29	PICMG	05h	M / Yes
Get LED Color Capabilities	3-25	PICMG	06h	M / Yes
Set FRU LED State	3-26	PICMG	07h	M / Yes
Get FRU LED State	3-27	PICMG	08h	M / Yes
Get Device Locator Record ID	3-29	PICMG	0Dh	M / Yes

10.4 Firmware Identification

10.4.1 Get Device ID Command

Table 64: Get Device ID Command

COMMAND		LUN	NetFn	CMD
Get Device ID		00h	App = 06h	01h
REQUEST DATA				
Byte	**Data Field**			
--	--			
RESPONSE DATA				
Byte	**Data Field**			
1	Completion code			
2	10h	Device ID		
3	80h	Device Revision		
4	02h	Firmware Revision 1: Major Firmware Revision (varies depending on firmware revision)		
5	00h	Firmware Revision 2: Minor Firmware Revision, BCD encoded (varies depending on firmware revision)		
6	51h	IPMI Version, holds IPMI command specification version, BCD encoded		
7	BDh or BFh	Additional Device Support (SMC or BMC mode)		
8..10	98h 3Ah 00h	Manufacturer ID, LSB first 03A98h = 15000 = Kontron		
11..12	00h B4h	Product ID, LSB first B400h = Identifies the board/family firmware		
13*	Release number of the IPMI firmware (varies depending on firmware revision): 10h for R10 11h for R11			
14*	Board Geographical Address/slot number: 1 ... = Board in chassis slot 1...			
15..16*	Reserved			

* Bytes 13 through 16 are optional and defined by Kontron.

Invoking the IPMI command **`Get Device ID`** returns among other information the following data:

- » Manufacturer ID = 3A98h (Kontron IANA ID)
- » Product ID = B3C0h, identifies the board family of the IPMI firmware
- » Firmware revision (byte 4:5) reflects the version of the running firmware, which will change after firmware update.
- » Release number of the IPMI firmware (byte 13) will be incremented with each firmware update

10.4.2 Device Locator Record

The device ID string which can be found by reading the Device Locator Record (SDR Type 12h) contains the string “BMC:x ... x”. For example, invoking the “ipmitool” command **`ipmitool sdr list mcloc`** will return the device ID strings of all available boards. If the IPMI controller is in BMC mode, this string will be displayed without change. If the IPMI controller is in SMC mode, then the string will be changed into “Sxx: x ... x” where xx is the slot number where the board is residing, e.g. “S09: x ... x”.

10.5 Board Control Extensions

10.5.1 SPI Boot Flash Selection—uEFI BIOS Failover Control

The uEFI BIOS code is stored in two different SPI boot flash devices designated as the standard SPI boot flash and the recovery SPI boot flash.

By default, the uEFI BIOS code stored in the standard SPI boot flash is executed first. If this fails, the uEFI BIOS code in the recovery SPI boot flash is then executed.

During boot-up, the uEFI BIOS reports its operational status to the IPMI controller within a given time. If the status is "failed" or not reported within the given time, the IPMI controller selects the recovery SPI boot flash, resets the board's processor, and waits for the status report from the uEFI BIOS again.

In the event the recovery boot operation fails, the IPMI controller reports it, but takes no further action of its own.

When a boot operation fails, a "Boot Error - Invalid boot sector" event is asserted for the related sensor:

- "FWH0 Boot Err" sensor indicates the standard SPI boot flash has failed
- "FWH1 Boot Err" sensor indicates the recovery SPI boot flash has failed

10.5.2 uEFI BIOS Boot Order Selection

Normally the uEFI BIOS will apply the boot order which was selected in the uEFI BIOS menu “uEFI Boot/ Boot Option Priorities”. But there is another alternative boot order which is stored in the IPMI controller's non-volatile memory. This boot order can be set and read by IPMI OEM commands. At payload start the IPMI controller writes this boot order into a register where the uEFI BIOS can read it. If this IPMI controller's boot order has a non-zero value, the uEFI BIOS will use it instead of its own boot order.

10.5.3 Set Control State (SPI Boot Flash Selection, Boot Order Selection)

Table 65: Set Control State

COMMAND	LUN	NetFn	CMD
Set Control State (SPI Boot Flash, Boot Order)	00h	OEM = 3Eh	20h
REQUEST DATA			
Byte	**Data Field**		
1	Control ID: 00h = SPI boot flash selection 9Dh = uEFI BIOS boot order configuration		
2	**Control state for SPI boot flash selection (00h):** 00h = Standard SPI boot flash is selected (default) 01h = Recovery SPI boot flash is selected **Note:** The DIP switch SW1, switch 2, may overwrite the above selection. **Control state for uEFI BIOS boot order configuration (9Dh):** 00h = Boot order is according to uEFI BIOS setup (default) 01h = Next boot device is: Floppy 02h = Next boot device is: HDD 03h = Next boot device is: CD 04h = Next boot device is: Network 05h = Next boot device is: USB Floppy 06h = Next boot device is: USB HDD 07h = Next boot device is: USB CD-ROM		
RESPONSE DATA			
Byte	**Data Field**		
1	Completion code		

Note: The settings mentioned above are stored in EEPROM and applied (to logic) each time the IPMI controller detects power-on.

10.5.4 Get Control State (SPI Boot Flash Selection, Boot Order Selection)

This command is used to read out the SPI boot flash and boot order settings.

Table 66: Get Control State

COMMAND	LUN	NetFn	CMD
Get Control State (SPI Boot Flash, Boot Order)	00h	OEM = 3Eh	21h
REQUEST DATA			
Byte	**Data Field**		
1	Control ID: 00h = SPI boot flash selection 9Dh = uEFI BIOS boot order configuration		
RESPONSE DATA			
Byte	**Data Field**		
1	Completion code		
4	Current control state (see section “Set Control State”) 00h .. 01h for control ID = SPI boot flash selection 00h .. FFh for control ID = uEFI BIOS boot order configuration		

10.6 Sensors Implemented on the Board

The IPMI controller includes several sensors for voltage or temperature monitoring and various others for pass/fail type signal monitoring. Every sensor is associated with a Sensor Data Record (SDR). Sensor Data Records contain information about the sensor's identification such as sensor type, sensor name, and sensor unit. SDRs also contain the configuration of a specific sensor such as threshold, hysteresis or event generation capabilities that specify the sensor's behavior. Some fields of the sensor SDR are configurable using IPMI commands, others are always set to built-in default values.

The IPMI controller supports sensor device commands and uses the static sensor population feature of IPMI. All Sensor Data Records can be queried using Device SDR commands.

The sensor name (ID string) has a name prefix which is 'NNN:' in the lists below. When reading the sensor name after board insertion, this prefix becomes automatically adapted to the role (BMC or SMC) and the physical position (slot number) of the board in a rack. If the IPMI controller is set up as a BMC, the prefix will be 'BMC:' independent of the slot where it resides. If the IPMI controller is set up as an SMC, the prefix will be 'Sxx:' where xx is the slot number (e.g. 09).

The sensor number is the number which identifies the sensor e.g. when using the IPMI command **`Get Sensor Reading.`** Please note that "ipmitool" accepts sensor numbers in decimal (e.g. "10") or hexadecimal (e.g. "0xa") notation.

The IPMI tool "ipmitool" displays for the command "ipmitool sdr list" the contents of the sensor data record repository (SDRR) of the whole rack if the SDRR has been generated. The generation of the SDRR must always be redone after adding or removing a board from the rack. For further information, refer to the IPMI Firmware User Guide, section "IPMI Setup for the Rack".

10.6.1 Sensor List

The following table indicates all sensors available on the CP6005(X)-SA. For further information on Kontron's OEM-specific sensor types and sensor event type codes presented in the following table, refer to section "OEM Event/Reading Types".

Table 67: Sensor List

SENSOR NUMBER / ID STRING	SENSOR TYPE (CODE) / EVENT/READING TYPE (CODE)	Assertion Mask / Deassertion Mask/ Reading Mask	DESCRIPTION	LED I1 Active/ Reading Mask
00h / NNN:Hot Swap	Hot Swap (F0h) / Sensor-specific (6Fh)	00FFh / 0000h / 00FFh	Hot swap sensor	N
01h / NNN:Temp CPU	Temperature (01h) / Threshold (01h)	1A81h / 7A81h / 3939h	CPU die temperature	Y/ 0F3Ch
02h / NNN:Temp PCH	Temperature (01h) / Threshold (01h)	0A80h / 7A80h / 3838h	Chipset temperature	Y/ 0F3Ch
03h / NNN:Temp Board	Temperature (01h) / Threshold (01h)	7A95h / 7A95h / 3F3Fh	Board temperature	Y/ 0F3Ch
04h / NNN:Pwr Good	Power supply (08h) / OEM (73h)	0000h / 0000h / 009Fh	Status of all power lines	N

Table 67: Sensor List (Continued)

SENSOR NUMBER / ID STRING	SENSOR TYPE (CODE) / EVENT/READING TYPE (CODE)	Assertion Mask / Deassertion Mask/ Reading Mask	DESCRIPTION	LED I1 Active/ Reading Mask
05h / NNN:Pwr Good Evt	Power supply (08h) / OEM (73h)	009Fh / 009Fh / 009Fh	Power fail events for all power lines	Y / 009Fh
06h / NNN:Board 3.3V	Voltage (02h) / Threshold (01h)	2204h / 2204h / 1212h	Board 3.3V supply	Y / 0F3Ch
07h / NNN:Board 5VIPMI	Voltage (02h) / Threshold (01h)	2204h / 2204h / 1212h	Management Power (MP) 5V	Y / 0F3Ch
08h / NNN:Board 5.0V	Voltage (02h) / Threshold (01h)	2204h / 2204h / 1212h	Board 5V supply	Y / 0F3Ch
09h / NNN:Board 12V	Voltage (02h) / Threshold (01h)	2204h / 2204h / 1212h	Board 12V supply	Y / 0F3Ch
0Ah / NNN:IPMB 5V	Voltage (02h) / Threshold (01h)	2204h / 2204h / 1212h	IPMB 5V supply	N
0Bh / NNN:Fan1 Speed	Fan (04h) / Threshold (01h)	0000h / 0000h / 1B1Bh	Speed [rpm] Fan 1	N
0Ch / NNN:Fan2 Speed	Fan (04h) / Threshold (01h)	0000h / 0000h / 1B1Bh	Speed [rpm] Fan 2	N
0Dh / NNN:Last Reset	OEM (CFh) / “digital” Discrete (03h)	0002h / 0000h / 0003h	Board reset event	Y / 0002h
0Eh / NNN:Slot System	Entity presence (25h) / Sensor-specific (6Fh)	0000h / 0000h / 0003h	Board is in system slot (SYSEN)	N
0Fh / NNN:PCI Present	Entity presence (25h) / Sensor-specific (6Fh)	0000h / 0000h / 0003h	Board is selected (BDSEL) and in system slot (SYSEN)	N
11h / NNN:IPMI WD	Watchdog2 (23h) / Sensor-specific (6Fh)	010Fh / 0000h / 010Fh	IPMI watchdog	Y / 010Fh
12h / NNN:IPMB State	IPMB status change (F1h) / Sensor-specific (6Fh)	000Fh / 0000h / 000Fh	IPMB-0 state (refer to PICMG 3.0 Rev 2.0, 3.8.4.1)	N
13h / NNN:ACPI State	System ACPI Power State (22h) / Sensor-specific (6Fh)	7FFFh / 0000h / 7FFFh	System ACPI power state	N
14h / NNN:Health Error	Platform Alert (24h) / “digital” Discrete (03h)	0000h / 0000h / 0003h	Aggregates states (power, temperatures etc.). Visualization by the Health LED (LED I1, red).	N
15h / NNN:CPU 0 Status	Processor (07h) / Sensor-specific (6Fh)	0463h / 0400h / 04E3h	CPU status: “Processor Throttled, THERMTRIP or CAT error”	Y / 0403h
16h / NNN:POST Value	POST value OEM (C6h) / Sensor-specific (6Fh)	4000h / 0000h / 40FFh	POST code value (port 80h)	N
17h / NNN:FWH0 BootErr	Boot error (1Eh) / Sensor-specific (6Fh)	0008h / 0008h / 0008h	Boot error on standard SPI boot flash	Y / 0008h
18h / NNN:FWH1 BootErr	Boot error (1Eh) / Sensor-specific (6Fh)	0008h / 0008h / 0008h	Boot error on recovery SPI boot flash	Y / 0008h
19h / NNN:XMC present	Entity Presence (25h) / Sensor-specific (6Fh)	0000h / 0000h / 0003h	Presence of XMC board	N

Table 67: Sensor List (Continued)

SENSOR NUMBER / ID STRING	SENSOR TYPE (CODE) / EVENT/READING TYPE (CODE)	Assertion Mask / Deassertion Mask/ Reading Mask	DESCRIPTION	LED I1 Active/ Reading Mask
1Ah / NNN:FRU Agent	OEM FRU Agent (C5h) / Discrete (0Ah)	0140h / 0000h / 0147h	FRU initialization agent state	Y/ 0140h
1Bh / NNN:IPMC Storage	Management Subsystem Health (28h) / Sensor-specific (6Fh)	0002h / 0000h / 0003h	IPMI controller storage access error	Y/ 0002h
1Ch / NNN:IPMC Reboot	Platform Alert (24h) / "digital" Discrete (03h)	0002h / 0000h / 0003h	2 = (Re-) Boot of IPMI controller	N
1Dh / NNN:IPMC FwUp	OEM FW Update (C7h) / Sensor-specific (6Fh)	010Fh / 0000h / 10Fh	IPMI FW update / manual rollback / automatic rollback	N
1Eh / NNN:Ver change	Firmware version changed (2Bh) / Sensor-specific (6Fh)	0002h / 0000h / 0002h	IPMI FW version, uEFI BIOS version, and logic version changed; update sensor data record repository	N
1Fh / NNN:SEL State	Event Logging Disabled (10h) / Sensor-specific (6Fh)	003Ch / 0000h / 003Ch	State of event logging	N
20h / NNN:IPMI Info-1	OEM Firmware Info 1 (C0h) / OEM (70h)	0003h / 0000h / 7FFFh	For internal use only	N
21h / NNN:IPMI Info-2	OEM Firmware Info 2 (C0h) / OEM (71h)	0003h / 0000h / 7FFFh	For internal use only	N
22h / NNN:IniAgent Err	Initialization Agent (C2h) / "digital" Discrete (03h)	0002h / 0000h / 0003h	Initialization agent error status. Used on BMC only. 1 = error free	Y/ 0002h
23h / NNN:Board Rev	OEM Board Revision (CEh)/ Sensor-specific (6Fh)	0000h / 0000h / 7FFFh	Board revision information	N
24h / BMC:Link-GbE-A	LAN (27h) / Sensor-specific (6Fh)	0000h / 0000h / 0003h	LAN link status of the front GbE A	N
25h / BMC:Link-GbE-B	LAN (27h) / Sensor-specific (6Fh)	0000h / 0000h / 0003h	LAN link status of the front GbE B	N
28h / BMC:Link-LPa	LAN (27h) / Sensor-specific (6Fh)	0000h / 0000h / 0003h	LAN link status of the rear I/O port PICMG 2.16 LPa	N
29h / BMC:Link-LPb	LAN (27h) / Sensor-specific (6Fh)	0000h / 0000h / 0003h	LAN link status of the rear I/O port PICMG 2.16 LPb	N
*2Ch / BMC:1Link-10GBE1	LAN (27h)/ Sensor-specific (6Fh)	0000h / 0000h / 0003h	Link status of the 10 GbE interface on rear I/O port 1 (10GBE1, Intel® 82599 port 1)	N
*2Dh / BMC:1Link-10GBE2	LAN (27h)/ Sensor-specific (6Fh)	0000h / 0000h / 0003h	Link status of the 10 GbE interface on rear I/O port 2 (10GBE2, Intel® 82599 port 0)	N

* The "1Link-10GBE1" and "1Link-10GBE2" sensors are only present on the CP6005X-SA.

10.7 Sensor Thresholds

Table 68: Thresholds - Standard and Extended Temperature Range

Sensor Number / ID String	01h / NNN:Temp CPU	02h / NNN:Temp PCH	03h / NNN:Temp Board (0°C to +60°C)	03h / NNN:Temp Board (-40°C to +70°C)
Upper non-recoverable	110 °C	118 °C	85 °C	95 °C
Upper critical	100 °C	108 °C	80 °C	90 °C
Upper non-critical	90 °C	98 °C	70 °C	80 °C
Normal max.	85 °C	93 °C	65 °C	75 °C
Nominal	75 °C	83 °C	55 °C	65 °C
Normal min.	3 °C	3 °C	0 °C	0 °C
Lower non-critical	1 °C	n.a.	- 1 °C	- 40 °C
Lower critical	n.a.	n.a.	- 2 °C	- 42 °C
Lower non-recoverable	n.a.	n.a.	- 5 °C	- 45 °C

Table 69: Voltage Sensor Thresholds

Sensor Number / ID String	06h / NNN:Board 3.3V	07h / NNN:Board 5VIPMI	08h / NNN:Board 5.0V	09h / NNN:Board 12V	0Ah / NNN:IPMB 5V
Upper non-recoverable	n.a.	n.a.	n.a.	n.a.	n.a.
Upper critical	3.50 V	5.29 V	5.29 V	12.9 V	5.29 V
Upper non-critical	n.a.	n.a.	n.a.	n.a.	n.a.
Normal max.	3.47 V	5.25 V	5.25 V	12.7 V	5.25 V
Nominal	3.30 V	5.00 V	5.00 V	12.0 V	5.0 V
Normal min.	3.14 V	4.51 V	4.75 V	11.5 V	4.75 V
Lower non-critical	n.a.	n.a.	n.a.	n.a.	n.a.
Lower critical	3.11 V	4.47 V	4.71 V	11.3 V	4.71 V
Lower non-recoverable	n.a.	n.a.	n.a.	n.a.	n.a.

10.8 OEM Event/Reading Types

OEM (Kontron) specific sensor types and codes are presented in the following table.

Table 70: OEM Event/Reading Types

OEM SENSOR TYPE (CODE)	OEM EVENT/ READING TYPE (CODE)	DESCRIPTION
Firmware Info 1 (C0h)	70h	Internal Diagnostic Data
Firmware Info 2 (C0h)	71h	Internal Diagnostic Data
Initialization Agent (C2h)	03h (“digital” Discrete)	Offsets / events: 0: Initialization O.K. 1: Initialization Error
FRU Agent (C5h)	0Ah (Discrete)	FRU initialization agent, using a standard reading type.
Post Value (C6h)	6Fh (sensor type specific)	Error is detected if the POST code is != 0 and doesn't change for a defined amount of time. In case of no error: Bits [7:0] = POST code (payload Port 80h) In case of error: Bits [15:0] = 4000h Data2 = POST code, low nibble Data3 = POST code, high nibble
Firmware Upgrade Manager (C7h)	6Fh (sensor type specific)	Offsets / events: 0: First Boot after upgrade 1: First Boot after rollback (error) 2: First Boot after errors (watchdog) 3: First Boot after manual rollback 4..7: Reserved 8: Firmware Watchdog Bite, reset occurred
Board Reset (CFh)	03h (“digital” Discrete)	Data 2 contains the reset type: ...WARM = 0 ...COLD = 1 ...FORCED_COLD = 2 ...SOFT_RESET = 3 ...MAX = 4 Data 3 contains the reset source: ...IPMI_WATCHDOG = 0 ...IPMI_COMMAND = 1 ...PROC_INT_CHECKSTOP = 2 ...PROC_INT_RST = 3 ...RESET_BUTTON = 4 ...POWER_UP = 5 ...LEG_INITIAL_WATCHDOG = 6 ...LEG_PROG_WATCHDOG = 7 ...SOFTWARE_INITIATED = 8 ...SETUP_RESET = 9 ...UNKNOWN = 0xFF

Table 70: OEM Event/Reading Types (Continued)

OEM SENSOR TYPE (CODE)	OEM EVENT/ READING TYPE (CODE)	DESCRIPTION	
e.g. for Power Good / Power Good Event	73h	Sensor-specific Offset	Event
		0h	HS fault#
		1h	HS early fault#
		2h	DEG#
		3h	FAL#
		4h	BDSELState
		5h..6h	n.a.
		7h	vccMainGood
		8h..Eh	n.a.
Board revision (CEh)	6Fh (sensor type specific)	Bits [7:0] = Board Revision number	

10.9 IPMI Firmware Code

10.9.1 Firmware Upgrade

The IPMI's operational code can be upgraded via the open-source tool “ipmitool” or via uEFI BIOS commands. The upgrade tool/commands allow download and activation of new operational code and also rollback to the “last known good” operational code. For further information on the IPMI firmware upgrade, refer to the uEFI BIOS Chapter in this manual and the IPMI Firmware User Guide.

10.9.2 IPMI Firmware and FRU Data Write Protection

If the board is plugged in a write-protected CompactPCI slot, neither the IPMI firmware or the FRU data can be updated or reprogrammed. The IPMI firmware stores the write protect state in it’s local NV-RAM.

Note: The write protection mode is still active when the payload is off even if the IPMI firmware reboots. To disable the write protection mode, plug the board in a non-write-protected CompactPCI slot and switch on the payload.

10.10 LAN Functions

Four Gigabit Ethernet channels on the board support IPMI over LAN (IOL) and Serial over LAN (SOL). While IOL serves to transport IPMI commands and their responses via Gigabit Ethernet, SOL serves to transport any serial data via Gigabit Ethernet.

Please note that IOL and SOL need the Ethernet device to be powered. Therefore, the board (payload) must be fully powered.

For information on the assignment of the IOL/SOL channels, refer to the “Gigabit Ethernet” section in the “Functional Description” chapter.

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