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cPCI-MXS64

6U CompactPCI® 64-bit System Processor

Technical Reference Manual
Version 1.4, February 2003

Note: The latest releases of the Technical Reference Manuals are available at:
ftp://ftp.kontron.ca/Support/Product_Manuals/

kontron
www.kontron.com

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European Statement

Warning

This is a class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

Safety Standard

UL Recognized Component, File # E186339 vol. 1 section 2

Care and handling precautions for Lithium batteries

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

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cPCI-MXS64 – Technical Reference Manual

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READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board**. If you do not have any jumper cap, we suggest you to use the Watchdog Timer jumper cap.

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel.

Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Hay un peligro de explosion si la pila no ha si bien remplazada. Remplace la pila con el mismo tipo o con aquellas recomendadas por el fabricante. Para desacerce de las pilas usadas, siga las instructiones del fabricante.

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IMPORTANT

J1 and J2 are de-facto industry standard as defined by PICMG

J3, J4 and J5 are user-defined connectors and will vary from various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

POWERING-UP THE SYSTEM

If you should encounter a problem, verify the following items:

Make sure that all connectors are properly connected.

Verify your boot diskette.

If the system still does not start up properly, you should try booting your system with only the power cord and video monitor connected to the board this is the minimum required to see if the board is working).

If you still are not able to start up your system, please refer to the emergency Procedure in the Appendix Section.

If you still are not able to get your board up and running, contact our technical Support department for assistance.

PREVENTING VIRUSES

Kontron Inc. takes every precaution against computer viruses. To safeguard against computer viruses in general, do not freely lend your diskettes and regularly perform virus scans on all your computer systems.

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

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UNPACKING AND SAFETY PRECAUTIONS

Static Electricity

Since static electricity can damage the board, the following precautions should be taken:

1. Keep the board in its antistatic package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its antistatic wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage, or items are missing, notify Kontron immediately.

When unpacking you will find:

1. 6U CompactPCI® 64-bit System Processor board
2. One Quick Reference sheet
3. One CDROM containing drivers.

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3. HOT SWAP CAPABILITY
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5. COMPATIBILITY WITH KONTRON PRODUCTS
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1.1. PRODUCT OVERVIEW

Kontron's 6U CompactPCI® system processor is ideal for data/telecommunication, CTI, and industrial control/monitoring markets.

The cPCI-MXS64 6U CompactPCI system processor brings scalable multiprocessing capability to the telecom and industrial automation markets. It is designed to operate as a "system" processor and must be installed in CompactPCI system slot.

Fully hot swappable, the cPCI-MXS64 communicates with other processor boards using the CompactPCI backplane as the physical layer of a 1 Gb/s Ethernet.

To provide the necessary interconnect, support local versions of the following OS: Microsoft Windows NT, Microsoft Windows 2000, Linux, VxWorks and pSOS.

Multi-level PCI-to-PCI bridging is fully supported. Based on Intel's 21154 PCI-to–PCI - transparent bridge, the feature set of the cPCI-MXS64 includes a rich selection of standard peripherals.

The cPCI-MXS64 offers a natural growth path to high performance, high availability as well as hot swap and scalable multiprocessing technology.

The cPCI-MXS64 can be ordered in either front I/O interfacing (video, serial port, 2xEthernet, all available on the face plate) or rear I/O interfacing through cPCI I/O connectors J3, J4 and J5 (no interconnection capability on the face plate).

CompactPCI Connectors

Rear I/O cPCI connectors are PICMG 2.0 Rev 3.0 compliant. CompactPCI connectors are located at the rear edge of the processor board. The complete cPCI connector configuration of the cPCI-MXS64 is composed of four connectors referred to as J1, J2, J3, J4, and J5.

Their function is described below:

J1	32 bit PCI signaling, power
J2	64 bit extension, arbitration, clocks, reset and. power
J3, J4, J5	Handle I/O signals.

CompactPCI™ connectors are also known as 2mm Hard Metric connectors.

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1.2. PRODUCT SPECIFICATIONS

The cPCI-MXS64 industrial system processor features:

- Intel's enhanced performance Pentium® processor.
  cPCI-MXS64: low power Mobile Pentium®III 500 & 700MHz, 256KB on-die L2 pipelined burst cache.
- 440BX AGP set.
- Supporting up to 768 MB SDRAM with parity or ECC.
- PCI Ultra DMA/33 IDE, SCSI-2.
- 64-bit AGP SVGA CRT controller.
- CompactFlash™ Disk interfacing on primary EIDE channel, user upgradable, master/slave.
- Ports available
  - Two Universal Serial Bus (USB).
  - Two 10/100Mbps Ethernet.
  - Four serial ports (three RS-232 only: Serial Port 1, 2 and 4; one RS-232/422/485: Serial Port 3).
  - One Parallel port, bi-directional with all IEEE 1284 protocols supported with BIOS selectable IRQs and addressing.
  - Mouse and keyboard available through front plate or Rear Transition Module.
  - SCSI, supports 16-bit Ultra Wide LVD SCSI up to 80Mbps (Symbios SYM53C895).
- Floppy interface (360KB to 1.44MB).
- Optional hard disk/floppy mezzanine module for high level of integration.
- High availability controller capable to detect the insertion or removal of HA cPCI peripheral boards.
- J3/J4/J5 connectors to handle I/O signals such as serial, parallel, and USB ports, Ethernet and video, SCSI, and IDE interfaces, keyboard, speaker, mouse, and reset signals, SMBus.

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Software:

- Enable/disable of Ethernet and SCSI ports by software.
- Enable/disable of video by hardware.
- Serial/parallel port mapping/disable by software
- Remote operation/monitoring (VT-100 serial port console redirection),
- Programmable two-stage watchdog timer by software
- Fully compatible with existing application software using platforms PC and MS-DOS®, Windows® 3.1, Windows® 95, Windows® NT, Windows® 2000, OS/2® Warp, QNX™, NOVELL™, and UnixWare™.
- Supports: Advanced Configuration and Power Interface (ACPI 1.0), Advanced Power Management (APM 1.2), advanced thermal management (resume, overheat alarm and auto slow down) and Green support.
- Hardware monitor (voltages, temperature, and fan speed),

- Power failure circuit
- Two year warranty.

The cPCI-MXS64 can be purchased either for front plate I/O interfacing (video serial port, Ethernet) or RTM (Rear Transition Module) I/O interfacing (no interconnection capability available on the front plate) through cPCI I/O connectors and backplane.

CompactPCI Connectors

Rear panel cPCI connectors are PICMG 2.0 Rev2.1 CompactPCI™ specification compliant. CompactPCI connectors are located at the rear edge of the board. The complete cPCI connector configuration is composed of five connectors referred to as J1, J2, J3, J4, and J5.

Their function is described below:

J1/J2	carry out arbitration and PCI bus signals, and power.
J3/J4/J5	handle I/O signals.

CompactPCI™ connector is also known as 2mm Hard Metric connector.

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1.3. HOT SWAP CAPABILITY

The cPCI-MXS64 supports Hot Swap capability which means that hot swappable boards can be removed from or installed in the system while online (without powering-down the system).

Hot Swap consists of board hardware with the Hot Swap additions to the Hardware Connection Layer, and the Hot-Plug Service. Upon insertion of the board (any hot swappable board but the system host, cPCI-MXS64, the hardware connection layer will initialize the board and the Hot-Plug Service provides the means for reconfiguring the system.

High Availability is an attribute of a system designed to keep running (maintain availability) in the event of a system component failure. To provide a high degree of availability, a system requires a higher degree of control.

High Availability (HA) uses a higher degree of control than just indicating insertion and extraction. HA systems are able to control the Hardware Connection Process. To do this, the capabilities of the system are extended to allow software control of a board's hardware connection state. A hardware connection sequence is made possible through the use of different pin lengths and the process ends with the mating of the shortest pin (BD_SEL#).

The platform adds hardware to provide more control of each board's Hardware Connection Layer. The signals: BD_SEL#, HEALTHY#, and PCI_RST# are used to individually control each slot of the system.

BD_SEL# is one of the shortest pins. This pin is the last to mate and the first to break contact. This ensures that the sensing of its connection takes place at a time when all other pins are reliably connected. It is driven low to enable power on. For systems not implementing hardware connection control, it is grounded on the backplane.

HEALTHY# is used to acknowledge the health of the board. It signals that a board is suitable to be released from reset and allowed onto the PCI bus. In a HA system, the software can detect a faulty board when it fails to assert HEALTHY# after BD_SEL# has been asserted. A running board can also become not healthy at any time.

PCI_RST# as defined by the CompactPCI® Specification, is a signal on the backplane, driven by the system host. Platforms may implement this signal as a radial signal from the Hot Swap Controller to further control the electrical connection process. Platforms that do this must OR the system host's reset signal with the slot specific signal to maintain the bussed signal's function.

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The Software Connection Control resources on the board provide a signal (ENUM#) for system host notification and a switch and LED to interface with the operator.

Full Hot Swap boards drive the ENUM# signal to the system host to indicate a service request. This signal is provided to notify the system host that either a board has been freshly inserted or is about to be extracted. This signal informs the system host that the configuration of the system has changed. The system host then performs any necessary maintenance such as installing a device driver upon board insertion, or unloading drivers for hot swap boards that are about to be extracted. The application that is using the board is also notified that the resource will no longer be available.

The Hot Swap Switch allows the operator to indicate desire to extract the board. A blue LED, located on the front of the board, is illuminated when it is safe to extract the board. This LED indicates that system software has been placed in a state for orderly extraction of the board. The hardware connection layer provides protection only for the hardware during insertions and extractions. This method allows the operator to insert or extract boards without the extra step of reconfiguring the system at the console.

All actions are initiated by the operator, and must be performed in the correct sequence for proper system operation.

Full Hot Swap boards present the following resources to software executing on the system host (nominally implementing the Hot-Plug Service and Hot-Plug System Driver)

- An ENUM# signal, which is an open collector (open drain) bussed signal, to signal a change in status for the board.
- A switch actuated with the lower ejector handle, indicating the beginning of the extraction process or end of the insertion process.
- A LED to indicate the status of the software connection process.
- A set of four control and status bits on each board allows the system host's software to determine the source of the ENUM# signal and control the LED.

  Full Hot Swap boards allow the full range of system capabilities.

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1.4. INTERFACING WITH THE ENVIRONMENT

1.4.1 cPCI

The cPCI-MXS64 system processor is provided for rack-mounted systems to offer the highest modularity. Through the J1/J2 segment, the board can drive up to seven external CompactPCI slots, supporting individual REQ/GNT arbitration pair signals and clock.

> **NOTE**
>
> All I/O signals are available in front I/O and rear I/O configuration.
>
> A. In front I/O configuration, the following I/Os signals are available on the faceplate: SVGA, Serial Port 1, Ethernet 1 and 2, keyboard and mouse. All other I/Os are connected to J3-J5.
>
> B. In Rear I/O configuration, all I/O signals are connected to J3-J5
>
> A backplane dedicated to the cPCI-MXS64 is provided by Kontron and is referred to as cBP08R, cPCI Passive Backplane.

1.4.2 Mezzanine

The mezzanine is a hardware interface concept introduced by Kontron to increase the I/O connectivity of the cPCI-MXS64, but respecting the dual slot 6U form factor restrictions.

The onboard mezzanine connector features PCI bus, IDE, floppy, keyboard and mouse signals, for potential mezzanine applications: Kontron provides an optional storage mezzanine composed with a hard drive, a floppy disk drive.

> **NOTE**
>
> A bridge can be added on the mezzanine to support seven extra slots. These slots support HA cPCI I/O boards

A complete *CompactPCI* development system CxP-0816 is also available from Kontron.

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1.5. COMPATIBILITY WITH OTHER KONTRON PRODUCTS

The cPCI-MXS64 System Processor is a member of the Kontron's CompactPCI product family.

The boards are fully compliant with the PICMG 2.0 Rev.2.1 and PICMG 2.1 CompactPCI specifications.

When building a basic environment around the cPCI-MXS64, the platform may be composed of any of the following devices:

- cPCI-MXS64 6U System Processor
- cMC Mezzanine card with hard disk and floppy disk drive
- cMCB Mezzanine card with bridge, hard disk and floppy disk
- cSM-DVDHD Storage module with DVD and Hard Disk
- cSM-DVD Storage module with DVD only
- CxP0816 including
  - 8U 19-inch enclosure
  - Front loaded hot swappable 2U fan tray
  - Power supply (300W ATX or 350W AC or DC in single or redundant configuration)
  - One of the following backplanes:

    cBP-08R : 8 slots CompactPCI (PICMG 2.1)

    cBP-16R, 16 slots CompactPCI (PICMG 2.1)

    cTBP-08R, Telephony 8 slots HA CompactPCI (PICMG 2.5)

    cTBP-16R 16 slots Telephony HA CompactPCI (PICMG 2.5)

- cTM80-STD2S 6Ux8HPx80mm Rear Transition Module, standard pinout.

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1.6. MEZZANINE CARD CONCEPT

The capability of the cPCI-MXS64 to connect with other devices is enforced by PCI Mezzanine Cards (PMC). A fully equipped cPCI-MXS64 board may appear as follows:



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1.6.1 Kontron's Mezzanine Concept

This is Kontron's concept to expand the I/O capability of the board. It is built around two connectors:

- Mezzanine connector handling IDE and floppy disk drive signals.
- Mezzanine connector handling a complete PCI signal set (primary bus) including the REQ/GNT arbitration signal pair.

These two connectors represent an open door for future development of expansion and I/O mezzanine cards.

A Mezzanine Card referred to as cMC and cMCB are available from Kontron.

1.6.2 PMC Concept

PCI Mezzanine Card (PMC) is a standard specification that allows PCI I/O devices to be connected to the PCI bus. It conforms to the ANSI/IEEE P1386.1 specification that defines Standard Physical and Environmental Layers for PMC devices.

The cPCI-MXS64 features the PMC concept onboard to provide an extra method to support the 32-bit I/O devices available on the market.

PMC devices connect directly to standard PMC connectors. A mechanical cutout (with its EMI proof cap) is provided to allow integrated connectors and indicators to be available directly on the front plate through PMC card.

1.6.3 CompactFlash Feature

The cPCI-MXS64 board also supports standard CompactFlash disk through a CompactFlash module.

CompactFlash disk is a method of storing and transferring data. It is supported on the board as a standard IDE drive and connects to the primary EIDE interface.

The CompactFlash drive can be set as a Master or Slave device and combined with any standard hard disk drive by setting the jumper W3 (see Section 3.1, setting jumpers).

CompactFlash is installed on J18 connector. For more information on CompactFlash installation and setups, please refer to Section 2.1 – *CompactFlash Interface*.

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PART 2

2. ONBOARD FEATURES

1. COMPACTFLASH INTERFACE
2. ENHANCED IDE INTERFACES
3. ETHERNET INTERFACES
4. FLOPPY DISK INTERFACE
5. PS/2 KEYBOARD AND MOUSE INTERFACE
6. PARALLEL PORT
7. POWER MANAGEMENT
8. SCSI INTERFACE
9. SERIAL PORTS
10. THERMAL MANAGEMENT
11. USB INTERFACES
12. VIDEO INTERFACES

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2.1. COMPACTFLASH INTERFACE

The board supports an IDE compatible flash disk by using a CompactFlash module. CompactFlash (C-Flash) disks are the resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power. The cPCI-MXS64 supports all CompactFlash size presently available and future sizes when available.

The C-Flash disk connects on the cPCI-MXS64 via the onboard Flash Disk connector.

Related Jumpers

cPCI-MXS64: W3 to set the CompactFlash disk as master or slave.

BIOS Settings

Section 4.1.2 Main Menu: Hard Disk autodetect to set the type of hard disk.

2.1.1 Setups

The CompactFlash disk connects directly on the primary EIDE interface. It must be declared the same way as a standard hard disk using the BIOS setup program (Autodetect function).

To setup the CompactFlash disk for Master or Slave configuration, use the CompactFlash jumper located on the system processor.

To locate and install this jumper, please refer to Section 3.1, *Setting Jumpers*.

NOTE

Since device use ATA/IDE interface, no specific flash disk driver is required for various operating systems.

CAUTION

When using a CompactFlash module, the maximum operational temperature should not exceed 50°C.

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2.2. ENHANCED IDE INTERFACES

The board features two channel Bus Master PCI EIDE dedicated to Primary and Secondary IDE logical interfaces. Each channel supports up to two IDE devices (including CD-ROMs, hard disks, plus CompactFlash on the primary IDE interface) with independent timings, in Master/Slave combination.

Signal Paths

The primary IDE interface is available through both the cPCI I/O connector and the Mezzanine connector.

The secondary IDE interface is only available through the cPCI I/O connector.

Related Jumpers

None

BIOS Settings

Section 4.1.11 Integrated Peripherals.

The IDE interfaces supports PIO mode 4 transfers up to 16.6MB/sec and Bus Master IDE transfer up to 33MB/sec (Ultra-DMA 33). It does not consume any ISA DMA resources and integrates 16x32-bit buffers for optimal transfers.

> ➢ **CAUTION**
>
> When connecting IDE devices to the Primary IDE interface, Master and Slave devices must be shared in respect of the device allocation on both the cPCI I/O connector and the mezzanine
>
> Two Master devices (or two Slave devices) must not be installed on the same interface at the same time.

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2.3. ETHERNET INTERFACES

Both Ethernet controllers reside on the Primary PCI bus.

Each interface supports 10Base-T and 100Base-TX specifications: 10Mbps and 100Mbps network speeds are automatically detected and switched.

Signal Path

See note on page 1.5.

Related Jumpers

None.

BIOS Settings

Section 4.1.11 Integrated Peripherals: Enable/Disable Ethernet Controller.

2.3.1 Front Plate Configuration

Ethernet 1 and 2 signals are available on front plate connectors only when the board is ordered for front access.

Activity and link indicators are built in the connector.

2.3.2 cPCI I/O Configuration

Ethernet 1 and 2 signals are available on CPCI I/O connectors only when the board is ordered for rear access.

> ➢ **CAUTION**
>
> The combination of both front and rear panel configurations is not supported.

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The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program. Please refer to Section 4.1 BIOS Setup Program.

A diskette entitled **"Network Drivers** for Intel 82559 is included with the cPCI-MXS64. It contains network drivers for most common operating systems.

2.4. FLOPPY DISK INTERFACE

The onboard floppy disk controller is IBM PC XT/AT compatible. It handles 3.5" and 5.25", low and high density disks. Up to two drives can be supported in any combination.

Signal Paths

The Floppy Disk Controller interface is available through the cPCI I/O connector and through the Mezzanine connector (see Section 1.4.1)

Related Jumpers

None.

BIOS Settings

Section 4.1.4 Standard CMOS: Select type of floppy.
Section 4.1.11 Integrated Peripherals: Enable/Disable onboard FDC Controller.

2.5. PS/2 KEYBOARD / PS/2 MOUSE INTERFACE

The onboard keyboard controller is 8042 software compatible. PS/2 Keyboard and mouse signals are available through an output that supports direct connection to the interface. Since signals of both devices are combined on the same connector, a Y-cable is required to split the signals and feed a standard AT keyboard and a PS/2 mouse.

Signal Path

PS/2 keyboard and PS/2 mouse signals are available through J5 cPCI I/O connector and J14 Mezzanine connector.

Related Jumpers

None.

BIOS Settings

11.3.7 Integrated Peripherals : USB Keyboard Support; PS/2 Mouse Function Control

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2.6. PARALLEL PORT

The cPCI-MXS64 features one multi-mode parallel port. It is compatible with Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).

Signal Path

The Parallel Port interface is only available through J5 cPCI I/O connector.

Related Jumpers

None

BIOS Settings

Section 4.1.11 Integrated Peripherals: Onboard Parallel Port; Parallel Port Mode

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector. Differences are described as follows:

Pin Number (J5)	Standard Mode	EPP Mode	ECP Mode
A15	SLCT	-	SLCT
B15	PE	-	PERROR[1], ACKREVERS[2]
C15	BUSY	WAIT	BUSY[1], PERIPHACK[2]
D15	ACK#	INTR#	ACK#
E16	SLCTIN#	ADDRSTRB#	SLCTIN#
B17	INIT#	-	INIT[1]#, REVERSERQST[2]#
D17	ERR#	-	FAULT[1]#,PERIPHRQST[2]#
A18	ALF	DATASTB	ALF[1], HOSTACK[2]
E17	D0	D0	D0
C17	D1	D1	D1
A17	D2	D2	D2
D16	D3	D3	D3
C16	D4	D4	D4
B16	D5	D5	D5
A16	D6	D6	D6
E15	D7	D7	D7

[1] Compatible mode

[2] High Speed Mode

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> **NOTE**
>
> To operate in EPP or ECP mode, ensure the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

2.6.1 Standard Mode

The Standard mode is unidirectional. It is supported to maintain the compatibility with the IBM PC standard.

2.6.2 EPP Mode

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high performance block I/O transfers. The EPP mode always uses the most optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.

EPP mode assumes that the parallel port can be used to connect more than one peripheral device using multiplexor or daisy chain configurations.

A multiplexor is an external device that permits up to eight parallel port devices to share a single parallel port.

A daisy chain device has two ports: input and output. The input port is connected either to the host parallel port or the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

2.6.3 ECP Mode

ECP (Extended Capabilities Port) works the same as EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from the peripheral.

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> NOTE
>
> For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department.

2.7. POWER MANAGEMENT

Power Management features are supported at the BIOS level. All Power Management options are described in Section 4.1.8 – *Power Management Setup*.

2.8. SCSI INTERFACE

The boards feature SYM53C895 PCI to Ultra2 SCSI I/O Processor. Supports Ultra2 SCSI synchronous transfer rates up to 80 Mbytes/s on a 16-bit, LVD SCSI bus.. Signals are available through J3-J4 cPCI I/O connector.

Signal Path

SCSI interface signals are only available through the J3-J4 cPCI I/O connector or through RTM (Rear Transition Module).

Related Jumpers

W6 – To determine the SCSI termination (hardware, software or disabled)

BIOS Settings

11.3.7 Integrated Peripherals: Enable/Disable the Onboard PCI SCSI Chip.

To operate with SCSI devices the onboard SCSI controller must enabled through the AWARD BIOS setup program.

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2.9. SERIAL PORTS

Four full function serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbps.

Each serial port is specified as follows:

Designation	Communication Mode	Output Path
Serial Port 1	RS-232	Front Plate DB-9, cPCI J5
Serial Port 2	RS-232	cPCI J5
Serial Port 3	RS-232, RS-422, RS-485	cPCI J3
Serial Port 4	RS-232	cPCI J3
Serial Port 3	Infrared	cPCI-J3

UART registers are individually addressable and fully programmable.

2.9.1 SERIAL PORT 1

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as Serial Port 1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

Signal Path

Serial Port 1 signal path depends on the output configuration you have ordered for the board

Related Jumpers

W5 – Remote reset on Serial Port 1 or Serial Port 2 or disabled

BIOS Settings

Section 4.1.11 Integrated Peripherals : Enable/Disable Onboard FDC Controller;
Select Com Port Address of Serial Port 1

2.9.1.1. Remote Reset

A remote hardware reset of the cPCI-MXS64 is possible by sending a break on the Serial Port 1 or Serial Port 2 (see Section 3.1 for Remote Reset jumper setting). A break is simple an abnormally long start bit (100ms or more) on the incoming data line. A break signal is embedded in the data, so no special wire is required.

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Related Jumpers

W5– Remote reset on Serial Port 1 or Serial Port 2 or disabled to select whether the serial port 1 or 2 is used to control the remote reset

Bios Settings

None

The remote reset will work in RS-232 and RS-422 modes. It will also work with a modem, since the modem will repeat the break signal over the telephone network. All major telecommunication software have the capability of sending a break signal, usually by pressing the CTRL-B keys or the ALT-B keys on the keyboard. Only a standard telephone line and a modem in auto-answer mode are needed. The only limitation is that the communication speed must be 1200bps or more. If the communication speed is to slow, a false reset can occur.

The break signal is entirely detected by hardware. For truly remote operation, use the VT-100 mode, which allows remote BIOS setup and console redirection.

2.9.1.2. Front Plate Configuration

The Serial Port 1 signals are available through a DB-9 connector located on the front plate. cPCI I/O Configuration

The complete signal set is tied to the J5 cPCI I/O connector to be used through the Rear Transition Module (RTM).

2.9.2 Serial Port 2

Serial Port 2 is buffered directly for RS-232 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

The Serial Port 2 port is 100% compatible with the IBM-AT serial port.

Signal Path

Serial Port 2 signals are only available through the J5 cPCI I/O connector.
COM2 signals (COM2_IRRX and COM2_IRTX) are available at J3 connector.

Related Jumpers

None

BIOS Settings

Section 4.1.11 Integrated Peripherals: Onboard Serial Port 2

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2.9.3 Serial Port 3

The Serial Port 3 supports Infrared, RS-232, RS-422, and RS-485 operation modes. When assigned as Serial Port 3, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

RS-422 and RS-485 modes allow communication using differential signals through one pair of wires (RS-485) or two (RS-422) to increase the noise immunity during data transfers.

RS-422 and RS-485 protocols offer advantages such as increased speed over longer distances or improved reliability over similar RS-232 setups.

Signal Path

In RS-232, RS-422, and RS-485 operation modes Serial Port 3 signals are only available through the J5 cPCI I/O connector.

Related Jumpers

W8 & W9 to connect/disconnect
RS-422/RS-485 termination resistors (see Section 3.1, Setting Jumpers)

BIOS Settings

11.3.7 Integrated Peripherals: Onboard Serial Port 3; Serial Port 3 Mode.

Upon a power-up or reset, the Serial Port 3 interface circuits are automatically configured for the operation mode setup in the BIOS. The Serial Port 3 signal assignation on the J5 cPCI I/O connector depends on the operation mode (RS-232, RS-422, or RS-485) it has been set.

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2.9.3.1. Infrared Mode

Infrared (IR) interface signals are provided to drive IR module for remote operations through Serial Port 3. When set in IR mode, the IR interface supports multi-protocol infrared operations. The IR interface is IrDA 1.1 compliant, and supports TEMIC/HP modules, SHARP ASK IR, and consumer IR.

2.9.3.2. RS-232 Protocol

When configured for RS-232 operation mode, the Serial Port 3 is 100% compatible with the IBM-AT serial port signals.

2.9.3.3. RS-422 Protocol

The RS-422 protocol (Full Duplex) uses both RX and TX lines during a communication session.

> ➢ **CAUTION**
>
> In RS-422 mode, W8 and W9 jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 *Jumper Settings*)

2.9.3.4. RS-485 Protocol

The RS-485 protocol (Half Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires, and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.

In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal is used to control the direction of the RS-485 buffer.

When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

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> ➢ CAUTION
>
> When installing the cPCI-MXS64 at one end of the network, W8 and W9 jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 – *Setting Jumpers*).

2.9.4 Serial Port 4

The Serial Port 4 is buffered directly for RS-232 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

When assigned as Serial Port 4 logical port, the port is 100% compatible with the IBM-AT serial port.

Signal Path
Serial Port 4 signals are only available through the J3 cPCI I/O connector.

Related Jumpers
None

BIOS Settings
11.3.7 Integrated Peripherals: Onboard Serial Port 4; IRQ Line for Serial Port 4.

2.10. THERMAL MANAGEMENT

Two temperature sensors are provided to supervise the thermal environment. One is used to monitor the CPU die temperature, while the second one, located on the CPU casing, allows the monitoring of the ambient temperature around the CPU.

The temperature is controlled according to two temperature levels, the Low temperature limit, which indicates normal operating conditions, and the High temperature limit, which indicates an overheating condition.

The temperature management consists in reducing the CPU clock speed throttling when the temperature goes over the high limit (overheating condition) and suspending the throttling operation as soon as the temperature returns under the low temperature limit (normal condition).

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The clock speed may be throttled by a CPU overheating due to the fan failure. In such a case, the temperature control is triggered as soon as the temperature reaches the high temperature limit of the die.

The ambient temperature of the CPU generally raises up due to an augmentation of the temperature in the casing. In that case, the clock speed will be slowed down as soon as the ambient temperature reaches the high ambient temperature value.

Thermal management operations are controlled by the BX chipset, and settings are provided through the BIOS setup program interface, *Thermal Management Setup* option (See Section 4.1.10 *CPU Board Feature Setup, Thermal management Options).*

2.11. USB INTERFACES

Signals for two USB ports are available through the cPCI I/O connector J5.

The USB strengths are as follows: capability to daisy chain as many as 127 devices per interface, fast bi-directional, isochronous/asynchronous interface, 12Mbps transfer rate, and standardization of peripheral interfaces into a single format.

Signal Paths
Both USB 0 and USB 1 interface signals are available through the cPCI I/O connector (J5).

Related Jumpers
None

BIOS Settings
4.1.9 PnP/PCI Configuration: Assign IRQ For USB

USB supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

The cPCI-MXS64 board fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible.

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2.12. VIDEO INTERFACE

The high-performance video capability of the board is based on Accelerated Graphics Port (AGP) technology. The video controller, Intel 69000, with its integrated 2Meg of high performance SDRAM is capable of CRT resolutions up to 1024 x 768 x 64K colors or 1280 x 1024 x 256 colors.

The video interface features 64-bit 2D graphics engine, 64-bit GUI accelerator engine with multiple window video acceleration.

Signal Path

The VGA video signal path depends on the output configuration you have ordered for the board.

Related Jumpers

W7 to enable or disable onboard VGA feature.
See Section 3.1 – *Jumper Settings*

BIOS Settings

4.1.9 PnP/PCI Configuration: Init Display First; Assign IRQ for VGA

- **Front Plate Configuration**
  VGA interface signals are available on J12, standard VGA connector, located on the front plate of the board, only when the board is ordered for front access operations. This configuration allows direct connection of CRT display onto the board.

- **cPCI I/O Configuration**
  VGA interface signals are available on J4 cPCI I/O connector only when the board is ordered for rear panel output operations.

2.12.1 Supported Resolutions

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of colors specification are listed below:

Resolution	Number of Colors
640x480, 800x600, 1024x768, 1280x1024	256 (8 bits)
640x480, 800x600, 1024x768	65,536 (16 bits)
640x480, 800x600	16.8 million (24 bits)
640x480, 800x600	16.8 million (32 bits)

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2.12.2 Major Features Description

- **VGA Compatibility**

  The video controller includes all registers and data paths required for VGA controller and supports extensions to VGA, including resolutions up to 800x600x16.8 million colors non-interlaced. The 16-bit images are displayed at up to 1024x768 resolution.

- **2D Graphics Engine**

  The 2D graphics engine is an advanced 32-bit three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

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PART 3

3. INSTALLING THE BOARD

1. SETTING JUMPERS
2. REGISTER'S DESCRIPTION
3. ONBOARD INTERCONNECTIVITY
4. CUSTOMIZING THE BOARD
5. BUILDING A cPCI SYSTEM
6. cPCI I/O SIGNALS

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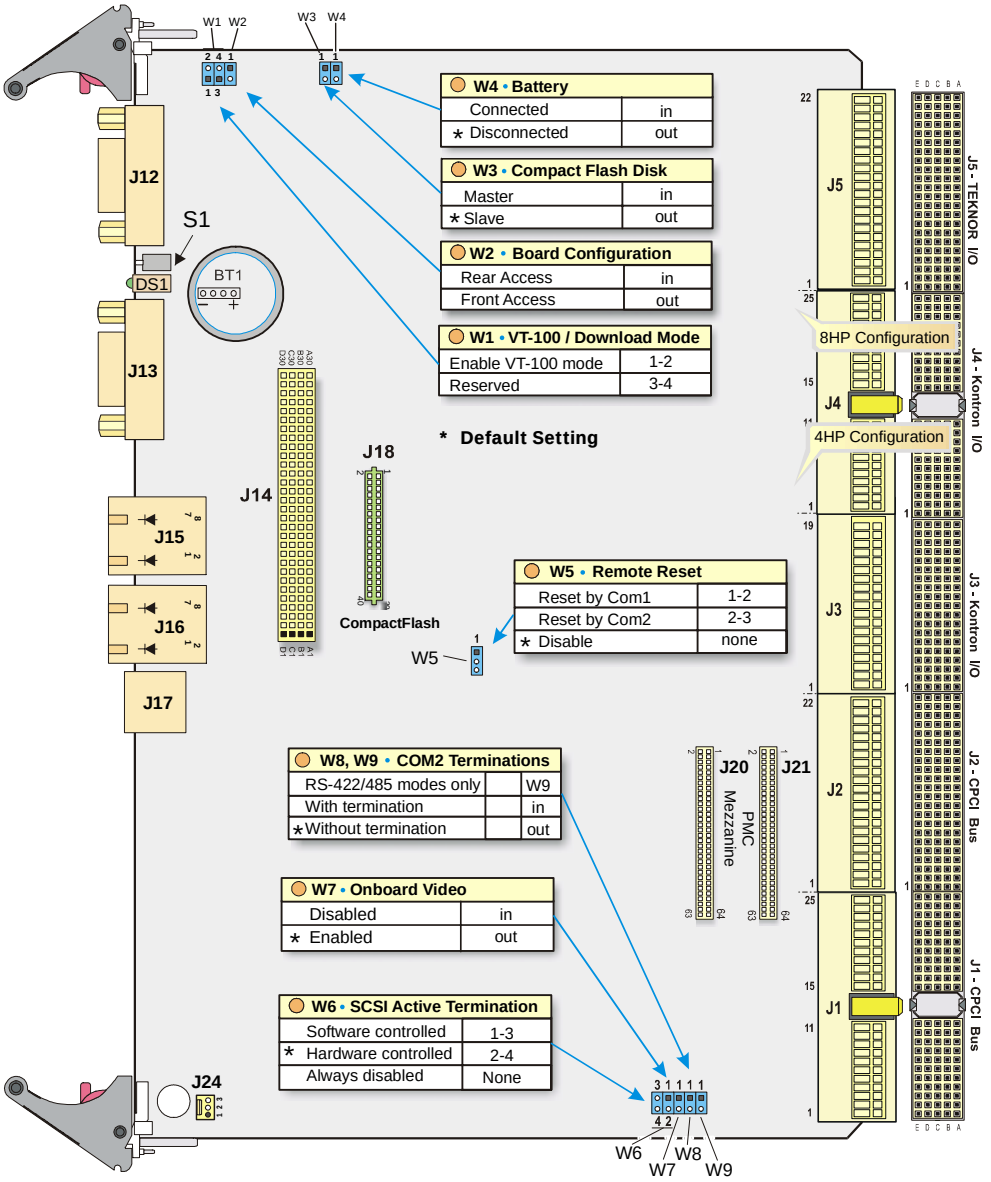
3.1. SETTING JUMPERS

3.1.1 Jumper Description for the cPCI-MXS64

Description		
VT-100 Mode (1-2) **Download Mode (3-4)**	When enabled, allows VT100 or ANSI terminal connection When enabled, allows data serial download from a remote computer.	**W1**
Board Configuration	Defines if used with Front Access or Rear Access	**W2**
CompactFlash Setting	Use this connector to setup the CompactFlash device in Master or Slave configuration.	**W3**
Onboard Battery	Connects or Disconnects the battery to/from the board circuitry.	**W4**
Remote Reset	To select Serial Port 1 or Serial Port 2 as a source for the remote hardware reset.	**W5**
SCSI Termination	Use this jumper to disable SCSI termination or select the termination control method from Software Controlled and Hardware Controlled options.	**W6**
Onboard Video	Use this jumper to enable or disable the onboard video feature.	**W7**
Serial Port 2 Termination	Use these jumpers to connect or disconnect the termination resistors on/from Serial Port 3 when set for RS-422/RS-485 operation mode 0.	**W8, W9**

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3.1.2 cPCI-MXS64 – Jumper Settings



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3.1.3 Register's Description RS232/RS485

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n90h*	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	n90h*	NU	NU	NU	RS485	RS232	ST1	NU	NU
Power-up Default					0	1	0		

ST1 : Enable RTS2 to be used as 485TX ENABLE when in 485 mode
RS232 : Enable UART2 RS232 operation
RS485 : Enable UART2 RS422 and 485 operation

The serial port 2 mode can be controlled by setting three bits. Here are the possibilities.

Mode	Bit RS485	Bit RS232	Bit ST1
RS232	0	1	X
RS422	1	0	0
RS485	1	0	1

X : Don't care

3.1.4 History and Monitor Status

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n91h*	PBRST	NU	WDO	NU	NU	NU	NU	PFO
WRITE	n91h*	NU	NU	NU	NU	NU	NU	NU	NU
Power-up Default									

PFO : Read the external power fail flag
PBRST : When high, indicate that the last system reset was caused by push button reset switch
WDO : When high, indicate that the last system reset was caused by watchdog time out

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3.1.5 Multimedia, History Status

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n92h*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHIS
WRITE	n92h*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHIS
Power-up Default							1		1

CLRHIS : When low, clear all history bits. Put this bit to 1 to enable history logging.
WD_LOCK : When high, lock the state of the enable bit for the digital watchdog

3.1.6 Monitoring Status and I/O Access

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n93h*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
WRITE	n93*h	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
Power-up Default						0		0	0

I2C_DATA : I2C data
I2C_CLK : I2C Clock
IDCHIP : One-wire clock/data for silicon ID chip

3.1.7 Uart 3 PnP Configuration

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n94*h	CND3	CIS3_1	CIS3_0	CBAS3_1	CBAS3_0	Reserved	Reserved	Reserved
WRITE	n94*h	CND3	CIS3_1	CIS3_0	CBAS3_1	CBAS3_0	Reserved	Reserved	Reserved
Power-up Default		0	0	0	0	1	0	0	1

CND3 : When low, decode the base address.
CIS3_[1..0] : COM port interrupt select.
CBAS3_[1..0] : COM base address select.

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The serial port 3 & 4 interrupt can be controlled in the following way.

CIS	Bit 1	Bit 0
IRQ 3	0	0
IRQ 4	0	1
IRQ 5	1	0
IRQ 7	1	1

The serial port 3 & 4 base address can be controlled in the following way.

CBAS	Bit 1	Bit 0
3F8	0	0
2F8	0	1
3E8	1	0
2E8	1	1

3.1.8 Uart 4 PnP Configuration

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n95*	CND4	CIS4_1	CIS4_0	CBAS4_1	CBAS4_0			
WRITE	n95*	CND4	CIS4_1	CIS4_0	CBAS4_1	CBAS4_0			NU
Power-up Default		0	0	0	1	1			

CND4 : When low, decode the base address
CIS4_ : [1..0] COM port interrupt select.
CBAS4_ : [1..0] COM base address select.

3.1.9 Digital Watchdog

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n96*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
WRITE	n96*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
Power-up Default		0	0	0	1				

WDEN : Enable/disable digital watchdog.
WDD[2..0] : Duration of digital watchdog.

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The digital watchdog duration can be controlled in the following way.

WDD[2..0]	NMI(T)	RESET(T)
000	16T	NMI(T)+8T
001	64T	NMI(T)+8T
010	256T	NMI(T)+8T
011	1024T	NMI(T)+8T
100	4096T	NMI(T)+8T
101	16384T	NMI(T)+8T
110	65536T	NMI(T)+8T
111	262144T	NMI(T)+8T

Time-out selection with T = 1.08ms (TBC)

3.1.10 NMI Control

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n97*	BATFEN	BATFLT	NU	NU	NU	NU	WDNMIEN	WDNMI
WRITE	n97*	BATFEN	NU	NU	NU	NU	NU	WDNMIEN	NU
Power-up Default		0						0	

WDNMI : When high, signal NMI from watchdog time-out.
WDNMIEN : Enable NMI generation from digital watchdog
BATFLT : When high, signal NMI from local RTC battery monitor
BATFEN : Enable NMI generation for bat fault.

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3.1.11 0Register BITs Description (Summary)

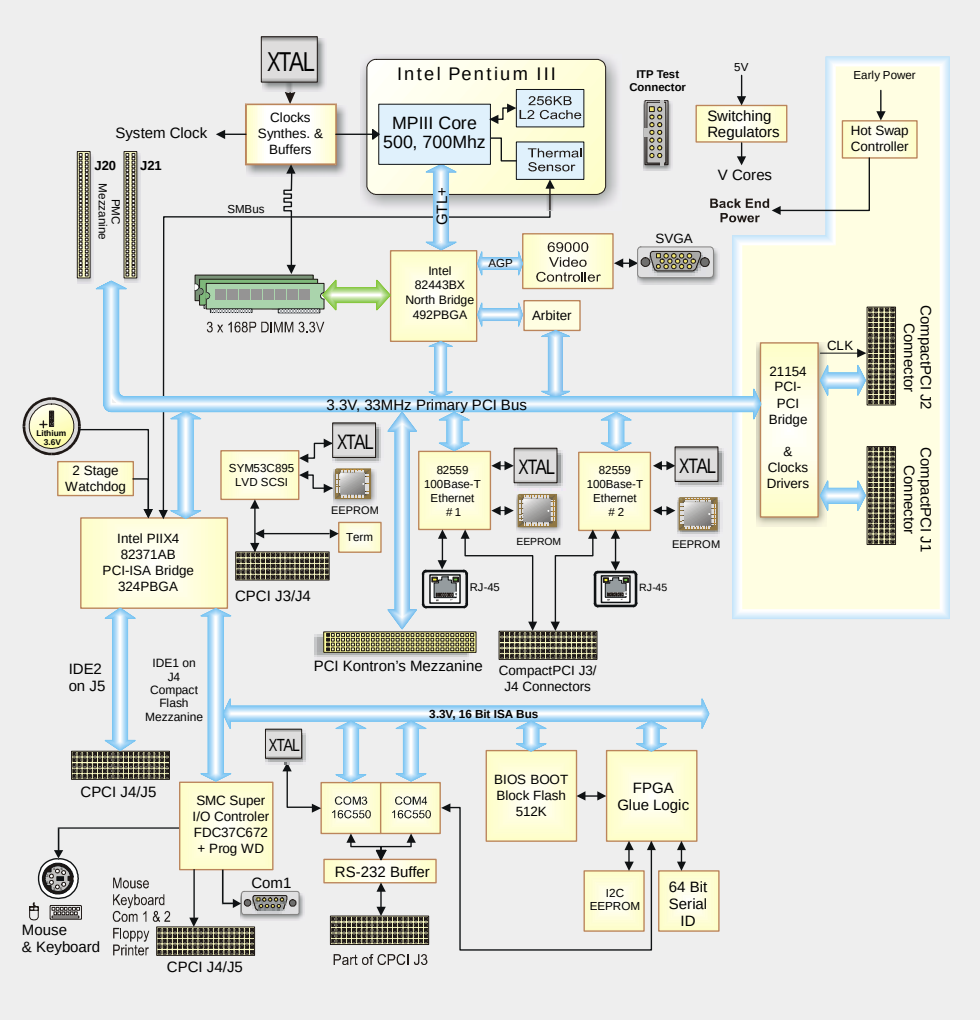
Address	CPLD	D7	D6	D5	D4	D3	D2	D1	D0
n90*	READ	NU			RS485	RS232	ST1	NU	
	WRITE								
n91*	READ	PBRST	NU	WDO	NU				PFO
	WRITE	NU		NU					NU
n92*	READ	NU					WD_LOCK	NU	_CLRHIS
	WRITE								
n93*	READ	NU				IDCHIP	NU	I2C_CLK	I2C_DATA
	WRITE								
n94*	READ	_CND3	CIS3_1	CIS3_0	CBAS3_1	CBAS3_0	RESERVED		
	WRITE								
n95*	READ	_CND4	CIS4_1	CIS4_0	CBAS4_1	CBAS4_0	NU		RESERV.
	WRITE								NU
n96*	READ	WDEN	WDD2	WDD1	WDD0	NU			
	WRITE								
n97*	READ	BATFEN	BATFLT	NU				WDNMIEN	WDNMI
	WRITE		NU						NU
n98*	READ	RESERVED							
	WRITE								
n99*	READ	RESERVED							
	WRITE								
n9A*	READ	NU	RESERVED						
	WRITE		NU						
n9B*	READ	NU			RESERVED				
	WRITE				NU				

The base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer can be set to 190h, 290h, and 390h (see *Chipset Features Setup*).

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3.2. ONBOARD INTERCONNECTIVITY

3.2.1 cPCI-MXS64 Block Diagram



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The cPCI-MXS64 is not only a matter of computation power. The boards also provide a high capability to interface with peripherals through three integrated chips:

- Host-to-PCI bridge for. 443BX from Intel: interface with the processor (host), system memory, video controller, and Primary PCI bus (3.3V / 33MHz).
- PCI-to-PCI bridge - 21154 from Intel: manage the PCI bus signals on J1 and J2 cPCI connectors. When used with a CompactPCI backplane drives seven cPCI slots.
- PCI-to-ISA bridge - 82371AB PIIX4 from Intel: interface the ISA bus to the Primary PCI bus.

3.2.2 Mobile Pentium® II / III Processor

The cPCI-MXS64 system board supports the Intel's Low Power 500 & 700MHz Pentium III processor (Higher clock speeds will be available when Intel will release the corresponding parts).

It consists of a Pentium® III processor core with an integrated second level cache of 256KB (on-die, full CPU speed, ECC capable) and a 64-bit high performance 100MHz front side bus

The processor interfaces to the 440BX AGPset through the 64-bit low power GTL + data bus interface.

3.2.3 North Bridge Chipset

This chipset consist of 443BX AGPset, 64/72-bit SDRAM data interface with ECC support, Low Power GTL Bus, five PCI arbitration channels, PCI bus rev. 2.1, Accelerated Graphics Port Interface (AGP). The bus is optimized for 100MHz operation.

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3.2.4 21154 PCI-to-PCI Bridge

The 21154 is configure as a 32/64-bit 33MHz PCI-to-PCI bridge that allows the board to support up to seven cPCI slot on its secondary PCI bus through a passive backplane. The bridge is fully compliant with the PCI Local Bus Specification, Rev. 2.1. It provides full support for delayed transactions, which enables the buffering of memory read, I/O and configuration transactions. The 21154 have separate posted write, read data and delayed transaction queues with a high buffering capability.

In addition, it supports buffering of simultaneous multiple posted writes and delayed transactions in both directions.

The PCI-to-PCI bridge allows the Primary and Secondary PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications where system resources are highly used.

3.2.5 82371AB PCI-to-ISA Bridge / IDE Xcelerator (PIIX4)

The PCI-to-ISA bridge is configured to support signals to directly drive IDE interfaces, USB ports, extra communication ports (Serial Ports 3 and 4), and standard Serial Ports (1 and 2), floppy disk drives, mouse and keyboard through a super I/O controller (FDC37C672).

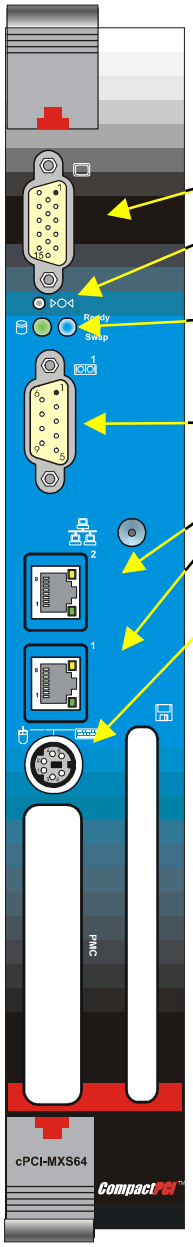
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3.2.6 Onboard Connectors and Headers

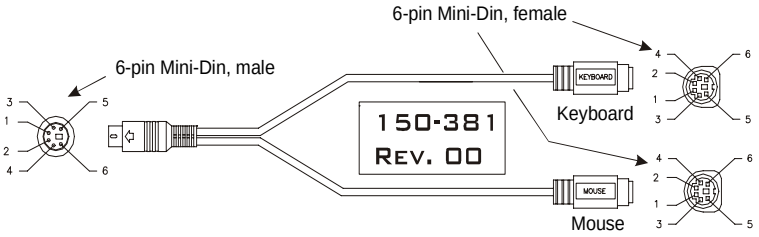
Description	Connector	Comments
CompactPCI Bus	J1/J2	J1- cPCI bus signals and power. J2 – Additional system slot signals.
CompactPCI I/O	J3	Serial Ports 3 and 4, Ethernet 1, power.
CompactPCI I/O	J4/J5	Supports PS/2 mouse, serial ports 1 and 2, first IDE channel, parallel port, keyboard, speaker, floppy disk, reset, USB, SMBus, and power signals.
DIMM Sockets	J6, J7, J8	Supports 168-pin 64/72-bit DIMMs, up to 768MB of RAM.
Processor Socket	J9	MXS64 : Mobile Pentium II / III connector
VGA	J12	Supports standard 15-pin DSUB female connector.
Serial Port 1	J13	Supports standard 9-pin DSUB male connector.
Kontron's Mezzanine	J14, J19	This connector handles PCI bus signals to the mezzanine.
Ethernet 1, 2	J16/J15	RJ-45 connectors with built-in activity and link indicators.
Keyboard/Mouse	J17	Mouse and keyboard signals are combined on a standard 6-pin DSUB female connector.
CompactFlash	J18	This connector is dedicated to the Kontron's CompactFlash module to support CompactFlash disk.
Storage Mezzanine	J19	This connector is implemented to support floppy drive and hard disk signals.
PMC	J20, J21	The PCI Mezzanine Card (PMC) connectors support one standard PMC device.
Battery	BT1	CMOS backup battery connector.

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3.2.7 Front Plate Connectors and Indicators



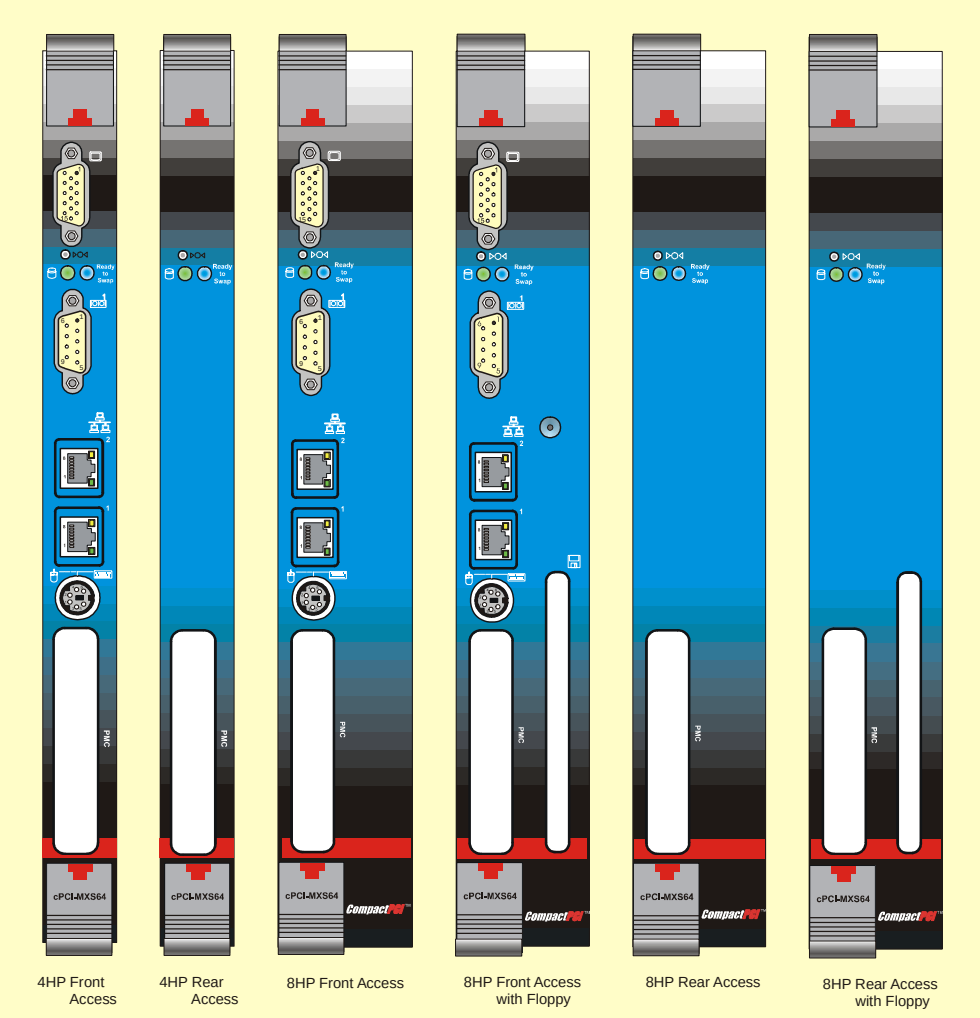
Name	Description	Comments
J12	Video Connector	Standard 15-pin DSUB female connector
S1	Reset Button	Use a small tool to press the button and proceed to a hardware reset of the board
DS1 DS2	IDE/SCSI LEDs HOT SWAP	Indicates an activity on IDE/SCSI devices Indicate a board failure/ready to swap
J13	Com Port 1	Standard 9-pin DSUB male connector
J16, J15	Ethernet 1 and 2	RJ-45 connectors with built-in activity and link indicators
J17	Keyboard and Mouse	To connect a keyboard and/or a mouse through this connector, you need a Y shaped splitter cable (Kontron part number 150-381)



The front plate supports a PMC cutout and a cap that also act as an EMI shield when there are no PMC device installed.

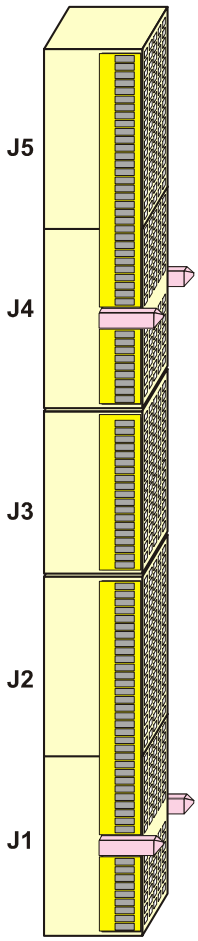
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3.2.8 Faceplate Options



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3.2.9 CompactPCI Connectors



- **cPCI J5 Connector**

  Supports PS/2 mouse, serial ports 1 and 2, primary IDE channel, parallel port, keyboard, speaker, floppy disk, reset, USB, SMBus and power signals.

- **cPCI J4 Connector**

  Supports Ethernet1, secondary IDE channel, SCSI, VGA, and power signals.

- **cPCI J3 Connector**

  Supports serial ports 3 and 4, V-Port, Ethernet1, and power signals.

- **cPCI J2 Connector (P2 on the cPCI-MXS64)**

  Supports additional system slot signals, PCI 64-Bit extension, and power.

- **cPCI J1 Connector (P1 on the cPCI-MXS64)**

  Supports cPCI bus signals, and power.

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3.3. CUSTOMIZING THE BOARD

3.3.1 Processor and Fan

cPCI-MXS64

Your board will be installed with the Mobile Pentium III processor, Low Power 500 & 700MHz and its adequate cooling system.

Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. Improper installation may damage the board and/or the CPU.

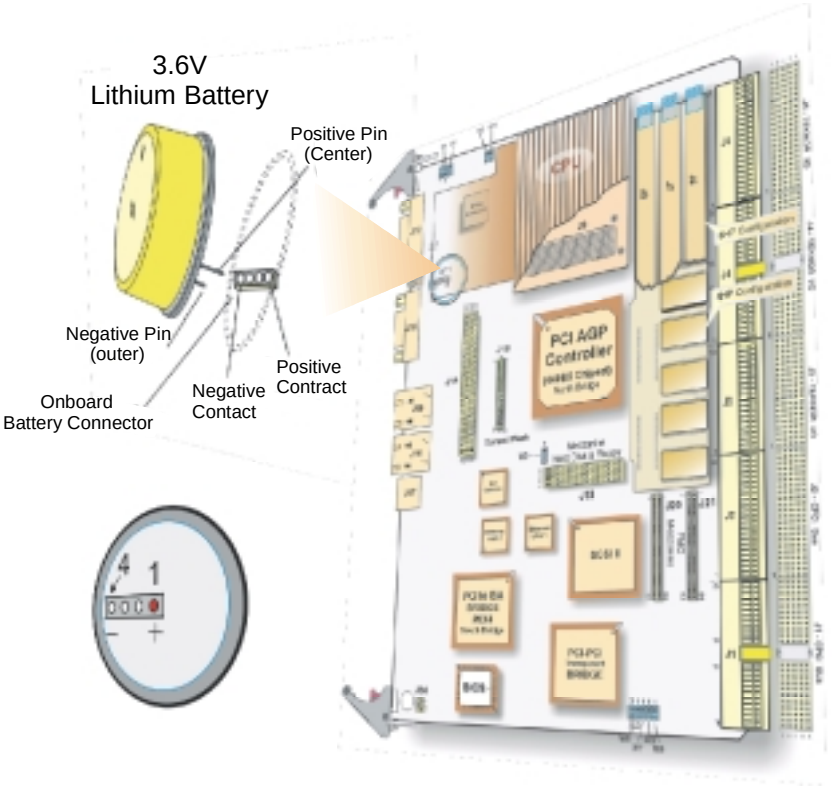
> ➢ CAUTION
>
> Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. Improper installation may damage the board and/or the CPU
>
> Before installing a processor on your board, **you must contact our technical support** for the installation procedure

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3.3.2 Backup Battery

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time lock (RTC).

When replacing, the battery must be connected as follows:



WARNING

Danger of explosion if battery is incorrectly replaced

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions. When you receive a board, remove the **onboard battery jumper** to enable the battery (See Section 3 for jumper settings)

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3.3.3 Memory

3.3.3.1. SDRAM System Memory

The cPCI-MXS64 supports three 168-pin DIMM (Dual In-Line Memory Module) sockets for memory configuration from 128MB to 768MB of Synchronous DRAM in 4HP configuration and from 64MB to 768MB in 8HP configuration.

The memory characteristics must conform to the following:

- 1.15 inch height, 168-pin DIMM.
- Standard 3.3V only.
- 64-bit and 72-bit modules, single-sided or double-sided.
- Unbuffered 100MHz (SDRAM).
- Serial Presence Detect (SPD) EEPROM.
- Errors Checking and Correction (ECC) capabilities or parity bit with 72-bit modules.
- Compliant with Intel's PC SDRAM Unbuffered DIMM Specification (100MHz) Rev. 1.0.

Modules can be installed in any socket and order. The total system memory is equal to the sum of the memory module size installed in the three DIMM sockets.



NOTE

When populating with more than one memory module, each socket must be installed with the same memory type (64/72-bit), however the capacity of each module may be different from the other.

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For the latest list of tested DIMMs devices please consult our FTP site at :

ftp://ftp.kontron.ca/Support/Product_Memory_AVL_Approved%20Vendor%20List/

3.3.3.2. DIMM Installation

> **NOTE**
>
> If a Mezzanine card is installed, it must be removed before installation of DIMMs.

To install the DIMMs in the sockets, proceed as follows:

1. With the board flat on the table, turn it so that the front plate is facing you.
2. Hold the module vertically so that the bottom connector key is at right. Install the DIMM straight down into the DIMM socket. The socket's keys will ensure a correct mating.
3. Press firmly on the top edge of the memory module to engage it into the socket. The module is fully inserted when the retaining clips snap into notches located at each end of the module.

If necessary, work your way by inserting the other modules, one by one.

To remove the DIMMs from the sockets, pull simultaneously on the retaining clips located on each side of the socket. Once the module has snapped out, pull gently on it.

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3.3.4 Supervision Features

The cPCI-MXS64 provides a set of programmable I/O registers to setup the Intel PIIX4 (I/O addresses 4030h to 4037h) and the XILINX FPGA (I/O addresses programmable at 190h-193h, 290h-293h or 390h-393h using the AWARD Chipset Features Setup).

Only register bits needed to program the power fail detection and watchdog functions are described below.

3.3.4.1. Power Fail Monitoring

The power failure detector status can be readout from one bit of the system register located at the address 4031h (See table below). The detection conforms to the following conditions (* = active low signal):

It always monitors the +5V power supply. When it drops below 4.65V (typical), the system is reset.

It can monitor the onboard battery. When the battery is in a low condition (below 2.9V typical), the PFO* (power fail output) signal goes low. The status of the PFO* signal can be read at I/O address 4031h, bit 1 (0 = failed, 1 = good). An interrupt handler can then service the interrupt. If you choose not to generate an NMI, you can use an algorithm to detect a low battery condition and respond accordingly.

Register	Bit #	Function	Software Programming
4030h	0-7	Reserved	Reserved
4031h	0, 2-7	Reserved	Reserved
	1	Power Fail Output (Internal/External Battery or External Power Source)	Read: 0 = Failed, 1 = Good
4032h	0, 2-7	Reserved	Reserved
	1	Watchdog Stage 1 Status	Read: 0 = Timed out, 1 = Normal
4034h	0-7	Reserved	Reserved
4035h	0-1, 4-7	Reserved	Reserved
	2	Watchdog enable	Write: 1 = Disable, 0 = Enable
	3	Watchdog reset	Write: 1-0-1 (toggle) to activate the watchdog (when enabled)
4036h	0-7	Reserved	Reserved
4037h	0-7	Reserved	Reserved

For more information, contact the Technical Support department

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3.3.4.2. Watchdog

The function of a watchdog is to reset the CPU board if the processor is not able to generate a trigger for longer than the watchdog time-out period. This feature is useful in embedded systems where human supervision is not required or impossible.

The cPCI-MXS64 provides a two-stage digital watchdog with software programmable time-out period.

Following a reset of any source, the watchdog is disabled. The watchdog can be enabled by software.

Dual Stage Watchdog

Enabling the Programmable Watchdog

To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register 0x92h (bit 2), then set th4e bit WDEN (bit 7) in register n92h and relock it by setting the lock bit in register 0x92 (bit 2). The following is an example in C language:

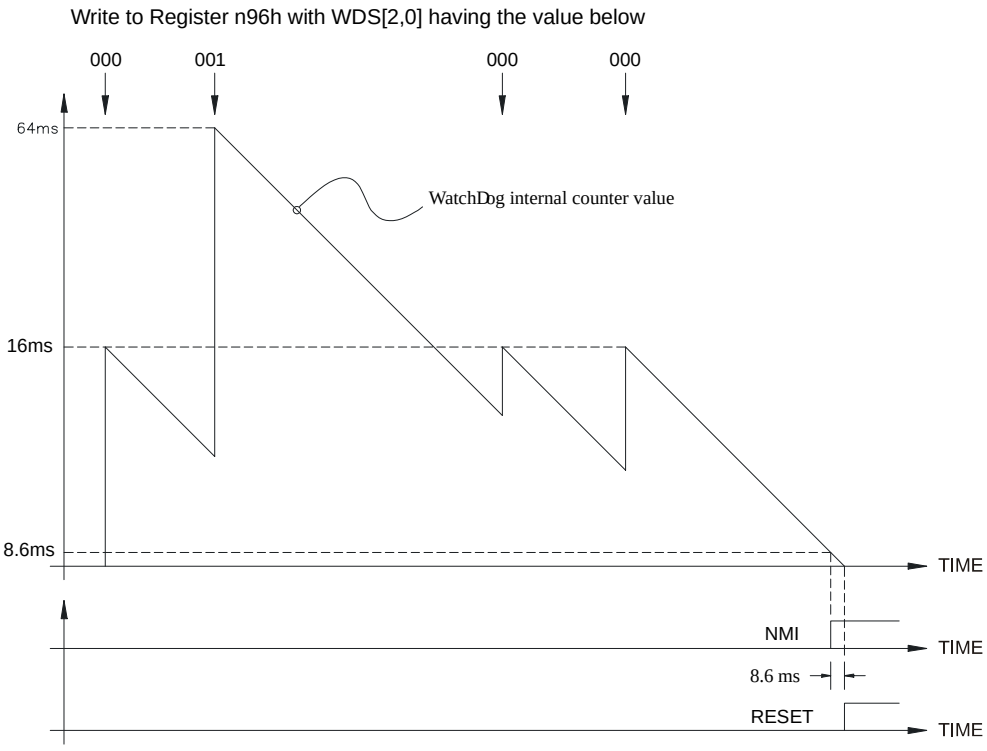
```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390
void ArmWatchdog(void)
{
    outp{TekReg+2,  inp(TekReg+2) & 0xFB);      // unlock watchdog enable bit
    outp{TekReg+6,  inp(TekReg+6) | 0xF0);      // enable and trigger at max time-out
    outp{TekReg+2,  inp(TekReg+2) | 0x04);      // lock watchdog enable bit
}
```

Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register n92h (n=1, 2 or 3). The action of writing to the register is the trigger and the value written to the register tells the watchdog the current time-out to use (see register n92h description). For a fixed time-out, the software simply writes a constant in register x92h.

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A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register n92h. The processor must initialize the counter to prevent it from reaching count 0 (timeout).

The following C language procedure can be used to trigger the programmable watchdog.

```
#define TekReg 0x190            // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout)      // select timeout at runtime: 0x80 = 0.016s,
                                // 0x90 = 0.065s, 0xA0 = 0.261s, ...
{
   outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```


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TIME-OUT

The programmable watchdog has two stages: the first stage has a variable time-out while the second stage has a fixed one.

The first stage time-out is chosen at runtime from eight preset values (see table below). The first stage time-out generates an NMI interrupt (if enabled in register n92h). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler; see register n92h description for a suggestion on how to do this.

The second stage times-out 8.6ms ±10% (depending on the temperature) after the first one and generates a master reset.

WDS[2,0]	NMI Timeout	RESET Timeout
000	0.016s	0.016s + 1ms
001	0.065s	0.065s + 1ms
010	0.261s	0.261s + 1ms
011	1.044s	1.044s + 1ms
100	4.174s	4.174s + 1ms
101	16.69s	16.69s + 1ms
110	66.79s	66.79s + 1ms
111	267.1s	267.1s + 1ms

A reset from the programmable watchdog is latched for reset source identification; see reset history description in Section 4.3.

3.3.4.3. Thermal Management

The thermal management is built around two digital temperature sensors and a thermal watchdog. Both devices can be programmed to set their outputs when the temperature of the processor or the ambient temperature exceeds a programmable high limit, and reset its output when the temperature is under a programmable low limit. A special routine is implemented to throttle the CPU clock until the temperature falls below the programmed low limit.

Please refer to Section 4.1.10 *CPU/Board Features Setup– Thermal Management Options* for a complete information on thermal management setups.

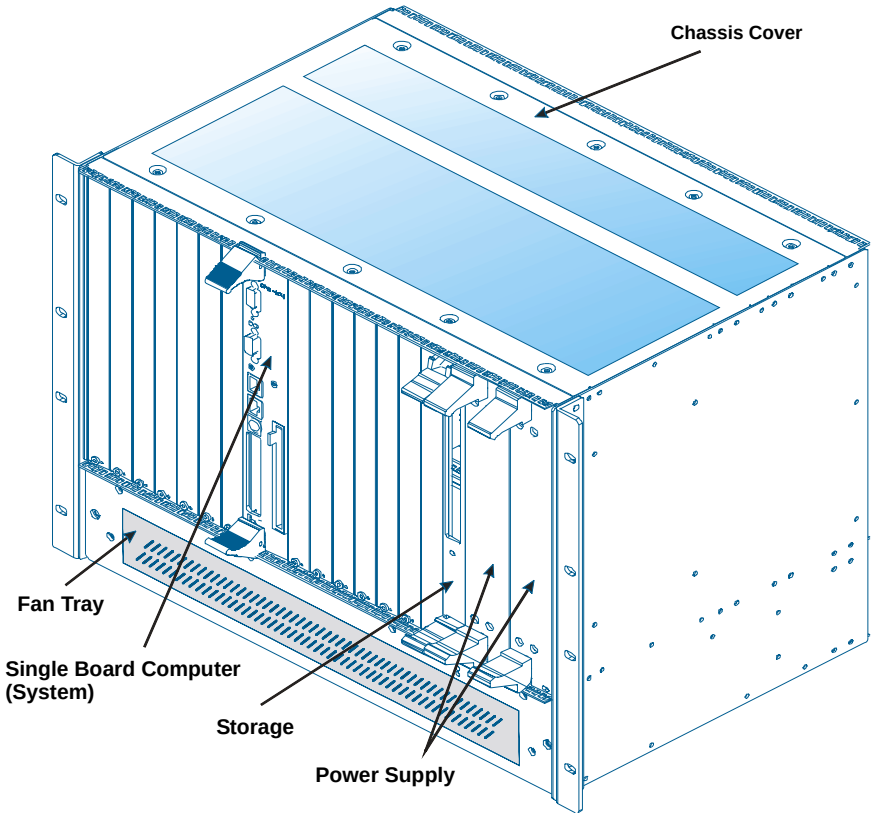
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3.4. BUILDING A cPCI SYSTEM

When building a CompactPCI system, a minimum requirement consists in: a chassis, a CompactPCI backplane, a storage module, a power supply unit, and a ventilation system.

The main AC power is drawn to the chassis components through an IEC power plug with a 2-stage filter, fuse holder and power switch. All power features are provided at the rear of the chassis.

The chassis may be used either as a desktop system or a rack-mount bay.



CxP0816

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3.4.1 Backplane

An entry-level backplane is provided by Kontron. It is referred to as cBP-08R. It features eight cPCI slots (one PCI I/O segment), and includes J3-J5 I/O connectors on all slots.

A 16-cPCI-slot backplane (cBP-16R) is also available from Kontron. It supports two PCI I/O segment: one is driven directly by the system processor while the other is managed through a PCI-to-PCI bridge implemented on the cMCB-2RC mezzanine card (Storage/PCI-to-PCI mezzanine).

All Kontron's CompactPCI backplanes feature pass-through connectors (J3-J5) to support Rear Panel I/O connections.



IMPORTANT

J1 and J2 are de-facto industry standard as defined by PICMG.

J3, J4 and J5 are user-defined connectors and will vary from various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

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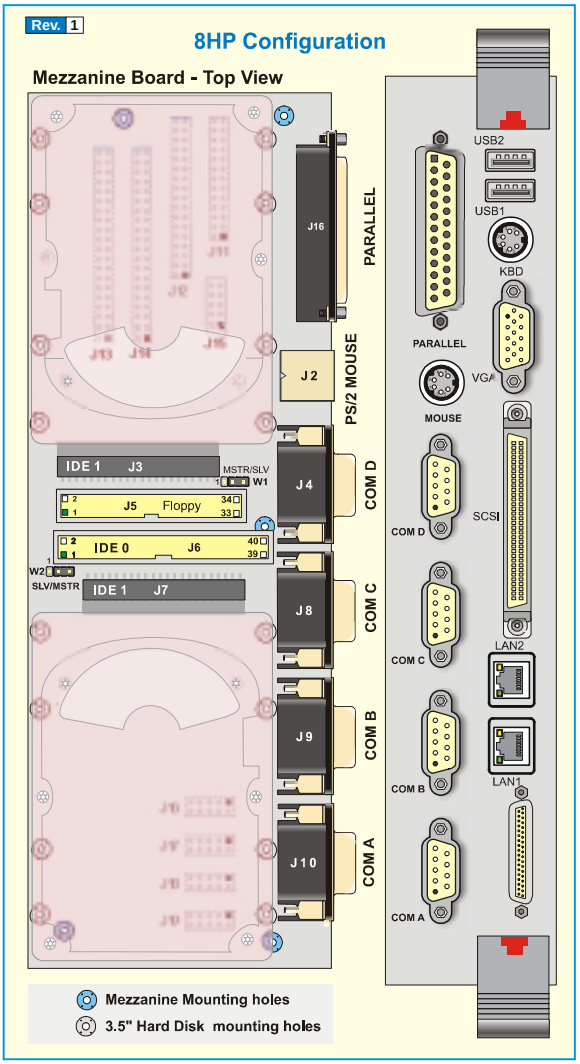
3.4.2 Rear-Panel I/O

This feature is intended to issue the I/O capabilities of the system processor to the rear of the enclosure using a Rear I/O Transition module (cTM80-STD2S).

The Rear I/O Transition module gathers all the I/O signals of the CPU board and makes them easily accessible through standard headers and connectors located at the rear of enclosure. The cTM80-STD Transition Module is illustrated below.

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The cTM80-STD Transition Module (8HP configuration)



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3.4.3 Storage Devices

A mezzanine card (cMC or cMCB-2RC) attaches directly to the system processor. 6U form factor storage modules are supported when using the cBP-08R backplane.

There are two ways of supplying data storage with Kontron's product line.

1. cMC : Mezzanine Card that is installed directly onto the processor board.
2. cSM-DVD : 6U-form factor storage module that is front-loaded into the CxP0816 chassis.

3.4.4 Power Supply

6U power supply modules featuring load sharing redundant mode and hot-swap capabilities allow on-site replacements of defective module while the system remains powered.

A standard ATX power supply unit is also supported.

3.4.5 Fan Tray

The ventilation unit of the enclosure conforms to the global requirement of the system in fully loaded configuration.

3.4.6 Installing the Board into a Bay

The cPCI-MXS64 is mechanical Eurocard form factor boards. It takes advantages of the IEEE1101.10 specifications that ensure a mechanical interchange capability between different plug-in elements in sub-racks.

Due to the high-density pinout of the Hard Metric connector, some precautions must be taken when connecting or disconnecting a board to/from a backplane:

1. Rail guides must be installed on the enclosure to slide the board to the backplane.
2. Do not use force if there is any mechanical resistance while inserting the board.
3. Screw the front plate to the enclosure to firmly attach the board to its enclosure.
4. Use the extractor handles to disconnect and extract the board from its enclosure.

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3.4.7 Connector Keying

CompactPCI connector support guide lugs to ensure a correct polarized mating. A proper mating is enhanced by the use of color-coded keys for 3.3V and 5V operation.

Color-coded keys prevent inadvertent installation of a 5V peripheral board in a 3.3V slot. The cPCI-MXS64 is universal. It does not support coding key. The PCI bus does not require to be keyed. Backplane connectors must always be keyed according to the signaling (VIO) level.

Coding Key Colors are defined as follows:

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	none
-48V	Red

3.4.8 Bus Mastering

The cPCI-MXS64 provides seven pairs of REQ/GNT (0-6) arbitration signals through the Secondary PCI bus. This means the board is capable of driving up to seven cPCI slots with PCI Bus Master capabilities.

3.4.9 Connection

To install the cPCI-MXS64 board into a bay, proceed as follows:

1. Locate the 6U system slot
2. Remove the front plate of the slot where you intend to insert the cPCI-MXS64.
3. Ensure the module is properly aligned with the guide-rails and slide it gently until it touches the backplane connector

WARNING

1. Some mechanical parts of the guide-rail are fragile (shield contacts and clips). Do not use force to insert and connect a CompactPCI module.
2. If there is any mechanical resistance while you insert a module, first ensure there is no mechanical obstacle and check for the alignment of all parts.

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5. To engage the board's connectors into the backplane connector, press simultaneously on the front plate.
6. Fasten the module using the fellow-plate fixing screw to secure the module to the system chassis.

To remove the module from the chassis, proceed as follows:

1. Remove the front plate fixing screws.
2. Press the handle to act as a lever to disengage the CompactPCI connector from the backplane.
3. Pull on the handle and gently remove the board.

3.5. cPCI I/O SIGNALS

This section describes integrated feature signals available on rear panel cPCI I/O connectors (J3, J4, and J5)

3.5.1 J3 Signal Specification

3.5.1.1. Ethernet LEDs

Signal	Pin Assignation	Description
LAN0, 1: SPLED	A6, E6	Speed LED signal
LAN0, 1: LINKLED	B6, D6	Link integrity LED signal
LAN0, 1:ACTLED	C6, A7	Transmit / receive activity LED signal

3.5.1.2. Ethernet 1

Signal	Pin Assignation	Description
LAN1:ETX+	A9	Ethernet High Transmit Data line
LAN1:ETX-	B9	Ethernet Low Transmit Data line
LAN1:ERX+	C9	Ethernet High Receive Data line
LAN1:ERX-	D9	Ethernet Low Receive Data line

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3.5.1.3. Serial Port 3

Signal	Pin Assignation	Description
COM3:DCD	A13	Data Carrier Detect
COM3:RXD	C13	Receive Data
COM3:DSR	D13	Data Set Ready
COM3:TXD	E13	Transmit Data
COM3:RTS	A14	Ready To Send
COM3:CTS	B14	Clear To Send
COM3:RI	C14	Ring Indicator
COM3:DTR	E14	Data Terminal Ready

3.5.1.4. Serial Port 4

Signal	Pin Assignation	Description
COM4:DCD	A11	Data Carrier Detect
COM4:RXD	C11	Receive Data
COM4:DSR	D11	Data Set Ready
COM4:TXD	E11	Transmit Data
COM4:RTS	A12	Ready To Send
COM4:CTS	B12	Clear To Send
COM4:RI	C12	Ring Indicator
COM4:DTR	E12	Data Terminal Ready

3.5.1.5. IDE LED Signals.

Signal	Pin Assignation	Description
IDE1:ACT#	B18	Secondary IDE activity
DE0:ACT#	C18	Primary IDE activity

3.5.1.6. IR Serial Port 2

Signal	Pin Assignation	Description
COM2 : IRRX	D18	IR receive data line (Serial Port 2)
COM2 : IRTX	E18	IR transmit data line (Serial Port 2)

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3.5.1.7. Hot Swap HA (High Availability) Signals

Signal	Pin Assignation	Description
BDSEL S2-S5	A15, B15, E15, D19	Board Select, one of the shortest pins (the last to mate and the first to break contact).
HEALTHY S2-S4	A16, B16, D17	Used to acknowledge the health of the board
PCIRST S2-S4	A17, C15, E17	Used to indicate the CompactPCI Bus reset signal

3.5.1.8. Miscellaneous Signals

Signal	Pin Assignation	Description
PWRBT#	A19	ACPI Reserved
EXT-SMI	B19	System Management Interrupt Input
PX4-NMI	C19	Non Maskable Interrupt Input
PWROK-33	E19	High when 3.3V supply is valid on the board

3.5.2 J4 Signal Specification

3.5.2.1. Power Management

Signal	Pin Assignation	Description
I2C:CLK	A1	I2C clock signal
I2C:DATA	B1	I2C data signal
LID	C1	Reserved
EXTFANFAIL0#	D1	Enclosure fan 0 fail
EXTFAN1FAIL1#	E1	Enclosure fan 1 fail
SM-BYPASS#	A2	Reserved

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3.5.2.2. SCSI Interface

Signal	Pin Assignation	Description
SD 0-15	E7, D7, C7, B7, A7, E6, D6, C6, E2, D2, C2, B2, E8, D8, C8, B8	SCSI Data – The SCSI data lines drive the ID during arbitration and selection, and command and data information as well as status and messages.
/IO	A3	In/Out – Indicates the In direction when asserted and the Out direction when not asserted.
/SREQ	B3	Request – A target will assert REQ to indicate a byte is ready or is needed by the Target.
/CD	C3	Command/Data – Indicates Command or message phase when asserted, and Data phase when not asserted.
/SSEL	D3	SCSI Select – The line is driven after a successful arbitration to select as an initiator or reselect as a target and otherwise it is received.
/SMSG	E3	SCSI Message - Indicates a Message phase when asserted, and Command or Data phase when not asserted.
/RST	A4	Reset – Signal is interpreted as a hard reset and will clear all commands pending on the SCSI bus.
/ACK	B4	Acknowledge – Indicate a byte is ready for or was received from the Target.
/BSY	C4	Busy – Handshake signal used during arbitration.
/SATN	E4	Attention – This line is activated when a special condition occurs.
/WIDEPS	B5	Wide Present – When Low, indicates that a wide (16-bit) cable is present.
TERMPWR	C5, D5	Termination Power.
/SDPH, /SDPL	A8, B6	SCSI High/Low Parity – Provide odd parity for data lines.

3.5.2.3. Video Interface

Signal	Pin Assignation	Description
SDATA	D9	Video serial data line (video I2C)
SCLK	A10	Video serial clock line (video I2C)
HSYNC	B10	Horizontal sync line
VSYNC	C10	Vertical sync line
RED	D10	Analog Red video signal
GREEN	E10	Analog Green video signal
BLUE	A11	Analog Blue video signal

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3.5.2.4. Ethernet 1 Interface

Signal	Pin Assignation	Description
LAN0:ETX+	A16	Ethernet 1 High Transmit Data line
LAN0:ETX-	B16	Ethernet 1 Low Transmit Data line
LAN0:ERX+	C16	Ethernet 1 High Receive Data line
LAN0:ERX-	D16	Ethernet 1 Low Receive Data line

3.5.2.5. Hot Swap HA (High Availability) Signals

Signal	Pin Assignation	Description
BDSEL S6-S8	C11, E20, B25	Board Select, one of the shortest pins (the last to mate and the first to break contact).
HEALTHY S5-S8	C9, D15, C22, C25	Used to acknowledge the health of the board
PCIRST S5-S8	E9, E15, A25, D25	Used to indicate the CompactPCI Bus reset signal

3.5.2.6. IDE 1 Interface

Signal	Pin Assignation	Description
IDE1:RST#	A17	
IDE1:0-15	B20, E19, C19, A19, D18, B18, E17, C17, D17, A18, C18, E18, B19, D19, A20, C20	Sec. Disk Data – These signals are used to transfer data to or from the IDE device.
IDE1:REQ	A21	Sec. Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
IDE1:IOW#	C21	Sec. Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from SDD lines.
IDE1:IOR#	E21	Sec. Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
IDE1:IORDY	B22	Sec. I/O Channel Ready – In normal mode, this input signal is driven directly by the corresponding IDE device IORDY signal.
IDE1:DACK#	D22	Sec. DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IRQ15	E22	
IDE1:IO16	A23	
IDE1: A 0-2	D23, B23, E23	Sec. Disk Address – These signals indicates which byte in either the ATA command block or control block is being addressed.
IDE1:CS1#, IDE1 :CS3#	A24, B24	Secondary Chip Select - For ATA control register.
SEC-PD1	C24	
/FAL1	E24	

IDE 1 (IDE 1) is assigned to the Secondary IDE logical interface. It supports directly two IDE devices configured as master and slave devices.

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3.5.3 J5 Signal Specification

3.5.3.1. IDE 0 Interface

Signal	Pin Assignation	Description
IDE0:RST	A1, B1	
IDE0: 0-15	B4, E3, C3, A3, D2, B2, E1, C1, D1, A2, C2, E2, B3, D3, A4, D4	Prim. Disk Data – These signals are used to transfer data to or from the IDE device.
IDE0:REQ	A5	Prim. Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
IDE0:IOW#	C5	Prim. Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from SDD lines.
IDE0:IOR#	E5	Prim. Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
PIORDY	B5	Prim. I/O Channel Ready – In normal mode, this input signal is driven directly by the corresponding IDE device IORDY signal.
IDE0:DACK#	D5	Prim. DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IRQ14	E4	IRQ14 line
IDE0:O16#	A6	IOCS16 line
IDE0:A 0-2	D6, C7, E6	Prim. Disk Address – These signals indicates which byte in either the ATA command block or control block is being addressed.
IDE0:CS1#, IDE0 :CS3#	A7, B7	
PRI-PD1	D7	
IDE0:DIAG#	C6	

3.5.3.2. USB 0 and 1 Interfaces

Signal	Pin Assignation	Description
USB0, 1: DATA (+/-)	B18, C18, D19, E19	USB Data – Differential data path for USB 0 and 1 ports
USB0, 1: GND	B19, D18	USB Ground – Differential ground reference for USB 0 and 1 ports
USB0, 1: VCC	C19, E18	USB Voltage – Differential power level for USB 0 and 1 ports

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3.5.3.3. Floppy Disk Interface

Signal	Pin Assignation	Description
FD:DRVEN 0-1#	E7, A8	Drive 0-1 density select
FD:INDEX#	B8	Index
FD:MTR 0-1#	C8, A9	Motor 0-1 enable
FD:DS 0-1#	E8, D8	Drive 0-1 select
FD:DIR#	B9	Direction
FD:STEP#	C9	Step pulse
FD:WDATA#	D9	Write disk data
FD:WGATE#	E9	Write gate
FD:TRK0#	A10	Track 0
FD:WRTPRT#	B10	Write protected
FD:RDATA#	C10	Read disk data
FD:HDSEL#	D10	Head select
FD-DSKCHG#	E10	Disk change

3.5.3.4. Serial Port 2

Signal	Pin Assignation	Description
COM2:DCD	A11	Data Carrier Detect
COM2:RXD	C11	Receive Data
COM2:DSR	D11	Data Set Ready
COM2:TXD	E11	Transmit Data
COM2:RTS	A12	Ready To Send
COM2:CTS	B12	Clear To Send
COM2:RI	C12	Ring Indicator
COM2:DTR	E12	Data Terminal Ready

3.5.3.5. Serial Port 1

Signal	Pin Assignation	Description
COM1:DCD	A13	Data Carrier Detect
COM1:RXD	C13	Receive Data
COM1:DSR	D13	Data Set Ready
COM1:TXD	E13	Transmit Data
COM1:RTS	A14	Ready To Send
COM1:CTS	B14	Clear To Send
COM1:RI	C14	Ring Indicator
COM1:DTR	E14	Data Terminal Ready

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3.5.3.6. Parallel Port

Signal	Pin Assignation	Description
SLCT	A15	Printer select
PE	B15	Paper end
BUSY	C15	Busy signal
ACK#	D15	Acknowledge handshake
D 0-7	E17, C17, A17, D16, C16, B16, A16, E15	Parallel port data bus
SLCTIN#	E16	Printer select
ALF	A18	Auto line feed
INIT#	B17	Initiate output
ERR#	D17	Error at printer
STB#	A19	Strobe signal

3.5.3.7. Miscellaneous Signals

Signal	Pin Assignation	Description
SMBDATA#	B20	Onboard SMbus data
SMBALERT#	C20	Onboard SMbus Alert (CPU overheating)
SMBCLK	E20	Onboard SMbus Clock
PBRST#	A22	Reset
DIAG-OC#	C22	Reserved
SPEAKER	E22	Speaker signal

3.5.3.8. Keyboard Interface

Signal	Pin Assignation	Description
KB:DATA	A21	Keyboard data
KB:CLK	B21	Keyboard clock
KB:VCC	C21	Keyboard power

3.5.3.9. Mouse Interface

Signal	Pin Assignation	Description
MOUSE:DATA	D21	Mouse data
MOUSE:CLK	E21	Mouse clock

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PART 4

4. SOFTWARE SETUPS

1. **BIOS SETUP PROGRAM**

2. **VT100 MODE**

NOTE **UPDATING OR RESTORING THE BIOS IN FLASH**

(see the Kontron FTP site and select the "support" section)

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4.1. BIOS SETUP PROGRAM

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery holds this information when the board is powered off, and the BIOS Setup program is required to make changes to the setup.

> NOTES
>
> Make sure you setup the BIOS Setup software prior to installing your operating system and your drivers.
>
> For systems that need the BIOS to first attempt to boot from LAN, follow these steps:
>
> 1. Set the *Boot From LAN First* option to "Enabled" in the BIOS Setup's *BIOS Features Setup*
> 2. Follow the complete procedure in the Boot From LAN utility (this utility is located on the driver's CDROM).

4.1.1 Accessing the BIOS Setup Program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the cPCI-MXS64 system processor. The cPCI-MXS64 and uses the AWARD Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

> ➢ **CAUTION**
>
> Before modifying CMOS setup parameters, ensure that the W4 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section 3.1).

To run the AWARD Setup program incorporated in the ROM BIOS:

Turn on or reboot the system.

Hit the DELETE key when the message - "Press DEL To Enter SETUP" appears near the bottom of the screen.

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The main menu of the AWARD BIOS CMOS Setup Utility appears on the screen.

```
                    KONTRON T6002 BIOS VERSION 2.0
                         CMOS SETUP UTILITY
                    AWARD SOFTWARE, INC. (2A69TU00)

STANDARD CMOS SETUP                  LOAD BIOS DEFAULTS
BIOS FEATURES SETUP                  LOAD SETUP DEFAULTS
CHIPSET FEATURES SETUP               SUPERVISOR PASSWORD
POWER MANAGEMENT SETUP               USER PASSWORD
THERMAL MANAGEMENT SETUP             IDE HDD AUTO DETECTION
PNP/PCI CONFIGURATION                SAVE & EXIT SETUP
INTEGRATED PERIPHERALS               EXIT WITHOUT SAVING

Esc     :    Quit                    ↑ ↓ → ←     :    Select Item
F10     :    Save & Exit Setup       (Shift)F2   :    Change Color

                    Time, Date, Hard Disk Type . . .
```

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS Default settings consist of the **safest** set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP Default values provide **optimum performance** settings for all devices and system features.

> ➢ **CAUTION**
>
> These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

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4.1.2 Main Menu

The Main Menu includes the following categories:

Category	Description
Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS (date, time, hard disk type, floppy disk type, video adapter type, memory…).
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
PnP/PCI Configuration	This Setup page sets Plug and Play and PCI configuration options.
CPU/Board Features Setup	This Setup page sets processor speed, thermal management and board monitoring options.
Integrated Peripherals	I/O subsystems that depend on the integrated peripherals controller in your system.
Load Bios Defaults	The BIOS defaults are **fail safe** settings that consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.
Load Setup Defaults	The Setup defaults are the **optimal** settings that provide the optimum performance for all devices and system features. **If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.**
Supervisor/User Password Setting	Change, set or disable the password. It allows you to limit the access to the system and the Setup, or only to the Setup.
IDE HDD Auto Detection	Forces the detection of the IDE hard disk drives parameters and puts them in the Standard CMOS Setup page.
Save & Exit	After having modified the BIOS Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.
Exit Without Saving	This option is used to exit AWARD Setup without saving the configuration to CMOS RAM or Flash BIOS.

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4.1.3 Setups

The arrow keys (↑ ↓ → ←) are used to highlight items on the menu and the PAGEUP and PAGEDOWN keys are used to change the entry values for the highlighted item. To enter in a submenu, press the ENTER key. Also, you can press the F1 key to obtain help information or the ESC key to close a menu or to quit the program.

Key	Function
↑	Moves to previous item.
↓	Moves to next item.
←	Moves to the item a the left.
→	Moves to the item at the right.
ESC	When in the Main Menu: Quits program (Answer 'Y' to save changes into CMOS). When in other screens: Exits and returns to the Main Menu.
PAGEUP or +	Increases the numeric value or changes value.
PAGEDOWN or -	Decreases the numeric value or changes value.
F5	When in the Main Menu: Restores the previous setup values for all the BIOS parameters (except Standard CMOS Setup) which were displayed when you entered the program. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Restores the previous setup values for that setup screen only.
F6	When in the Main Menu: Loads the BIOS Defaults of all the BIOS parameters (except Standard CMOS Setup). The BIOS Defaults are fail safe settings, which consists of the safest set of parameters. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the BIOS Defaults for all the BIOS parameters for that setup screen only.
F7	When in the Main Menu: Loads the Setup Defaults for all the BIOS parameters (except Standard CMOS Setup). When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the Setup Defaults for the BIOS parameters for that setup screen only. If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.
F10	When in the Main Menu: Saves all the CMOS changes and exit.

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4.1.4 Standard CMOS Setups

Function	Description
Date/Time	The current values for each category are displayed. Enter new values through the keyboard.
Hard Disks	Two IDE controllers are defined on the cPCI-MXS64 board. The Primary and Secondary controllers can both have two disks: Master Disk or Slave Disk. Only three settings are available for the hard disk type: Auto, User and None. Types 1 to 46 are not predefined in the system: Use auto-detect or enter the parameters for the type in the user-defined.
Drive A / Drive B	Select the type of floppy disk installed for drive A and drive B.
Video	This option specifies the basic type of display adapter card installed in the system.
Halt on	This option specifies the type of errors that will stop the system during the BIOS booting procedure. A message asks that you press F1 to continue or press the DELETE key to enter Setup. The settings are: All errors, No errors, All but keyboard, All but diskette, and All but disk/key (default setting).
Memory	This display-only option indicates the amount of Base, Extended and other types of memory installed in the system.

4.1.5 Saving & Exiting Operations

Use one of the following options available from the Main Menu:

Function	Description
Save & Exit	After having modified the BIOS Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.
Exit Without Saving	This option is used to exit AWARD Setup without saving the configuration to CMOS RAM or Flash BIOS.

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4.1.6 BIOS Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Virus Warning	Dis.	Dis.	En. / Dis.	When Enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. **Note: Many disk diagnostic programs and OS setups (e.g., Win95 setup), that access the boot sector table, can trigger the virus-warning message. If you plan to run such a program, we recommend that you first disable the virus warning.**
Quiet POST	Dis.	Dis.	En./Dis.	At the power on self-test (POST), only the AWARD logo and the "Press DEL to enter SETUP" message appears.
Quick Power On Self Test	Dis.	En.	En./Dis.	Select Enabled to reduce the amount of time required running the POST. A quick POST skips certain steps. We recommend that you enable quick POST to save time, since most major OS do their own tests
Full Screen Logo Show	Dis.	Dis.	En./Dis.	When enabled, a full screen bitmap (.BMP) picture will appear during the POST or you can have your logo being displayed (contact the Technical Support, see appendix G).
Boot from LAN First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the LAN. The complete procedure for this function is available on the "Boot from LAN" utility diskette.
Raid Card Boot First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the RAID disk card.
Boot Sequence	A,C, SCSI	C,A, SCSI	A,C,SCSI; C,A,SCSI; C,CDROM,A; CDROM,C,A; D,A,SCSI; E,A,SCSI; F,A,SCSI; SCSI,A,C; SCSI,C,A; C only; LS/ZIP,C.	This option defines the searching order in the BIOS for the boot device(s). **Note: The Boot from LAN First and Raid Card Boot First options take precedence over this option.**
Swap Floppy Drive	Dis.	Dis.	En./Dis.	Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.
Boot Up Floppy Seek	En.	Dis.	En./Dis.	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modern PCs have 40 track floppy drives, we recommend that you set this field to "Disabled" to save time.
Drive A Boot Permit	En.	En.	En./Dis.	When Disabled, this option will not permit booting from Drive A.
Floppy Disk Access Control	R/W	R/W	R/W, Read Only	When Read Only, this option will not permit writing to the floppy disk.

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BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Report No FDD For Win 95	No	No	Yes, No	Select Yes to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the Integrated Peripherals screen, select NO on the Onboard FDC Controller option.
Hard Disk Write Protect	Dis.	Dis.	En./Dis.	When Enabled, this option will not permit writing to the hard disk.
HDD S.M.A.R.T. Capability	Dis.	En.	En./Dis.	When Enabled, the Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.) features of the HDD are supported. S.M.A.R.T is used for prediction of device degradation and/or faults.
Delay For HDD (Secs)	0	0	0-15	This number of seconds inserted prior to HDD initialization. 0 is disabled.
OS Select For DRAM > 64MB	Non-OS/2	Non-OS/2	Non-OS/2, OS/2	Select OS2 only if you are running OS/2 with greater than 64MB of RAM.
Gate A20 Option	Norm.	Fast	Normal, Fast	When Fast, enables fast switching of Gate A20 via the 440BX chipset, instead of the keyboard controller.
Security Option	Setup	Setup	Setup, Normal	If you have set a password, select whether the password is required every time the system boots (“System” option), or only when you enter Setup (“Setup” option).
Diskette Access For	All	All	All, Supervisor	When this option is set to Supervisor and the Security option to System, all floppy disk accesses (read/write) are limited to the Supervisor (supervisor password required).
Boot Up NumLock Status	On	On	On, Off	Control the state of the NumLock key when the system boots. When set to “On”, the numeric keypad generates numbers instead of controlling cursor operations.
Typematic Rate Setting	Dis.	En.	En./Dis.	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.
Typematic Rate (Chars/s)	30	30	6-30 char/sec.	When the typematic rate setting is Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key).
Typematic Delay (msec)	250	250	250-1000 ms	When the typematic rate setting is Enabled, you can select a typematic delay (the delay before keystrokes begin to repeat when you hold down a key).
VT100 Settings				
Comport	1	1	1,2,3,4	Use this option to select which COM port will be used for VT100
Speed	Auto	Auto	Auto, 2400, 9600, 19200, 38400, 57600, 115200	Select the baud rate of COM port. being used in VT100 mode.
Parity	None	None	None, Odd, Mark, Even, Space	Use this option to select the parity .
Data	8	8	7, 8	Use this option to specify the number of data bits being used.
Stop	1	1	1, 2	Use this option to specify the number of stop bits being used.

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4.1.7 Chipset Features Setup

This part of the setup allows you to define chipset-specific options and features.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
CPU Internal Cache	Dis.	En.	En./Dis.	Enables or Disables the CPU Internal Cache (L1 cache).
External Cache	Dis.	En.	En./Dis.	Enables or Disables the External Cache (L2 cache).
CPU L2 Cache ECC Checking	Dis.	En.	En./Dis.	Enables or Disables ECC Checking for L2 cache. **Note: processors provided by Kontron support ECC. However, not all Pentium® II / III processors support ECC. Check Intel's website to know if your processor supports ECC:** http://developer.intel.com/support/processors/pentiumII/identify.htm.
SDRAM RAS-to-CAS Delay	3	3	2, 3	**Note: Upon boot-up, the BIOS will detect and display the optimal value for the SDRAM options (first four options in this menu), if it is different from the Setup value. You must enter the AWARD Setup, and set the options at the suggested value if you want the best performance.** This option inserts a timing delay between the CAS and RAS strobe signals, used when SDRAM is written to, read from, or refreshed. The number selected is the number of clocks to be inserted between a row activate command and either a read or write command.
SDRAM RAS Precharge Time	3	3	2, 3	Selects the number of CPU clocks for the RAS precharge. If an insufficient number of cycles is allowed for the RAS to accumulate its charge before SDRAM refresh, the refresh may be incomplete and the DRAM may fail to retain data.
SDRAM CAS Latency Time	3	3	2, 3	This option controls the number of clocks between when a read command is sampled by the SDRAMs and when the chipset samples read data from the SDRAMs. Select 3 for 3 DCLKs and 2 for 2 DCLKs. If a given row is populated with a registered SDRAM DIMM, an extra clock is inserted between the read command and when the chipset samples read data.
SDRAM Precharge Control	Dis.	Dis.	En./Dis.	When Enabled, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.
DRAM Data Integrity Mode	Non-ECC	ECC	ECC, Non-ECC	When set to ECC, allows auto-correction of the data read from memory. The ECC error flags' status register and the error pointer are updated if error correction occurs in this mode. When set to Non-Ecc, no error checking or error reporting is done. This option will work in ECC mode only if all installed memory banks supports ECC (Error Checking and Correction)
Memory Hole At 15M-16M	Dis.	Dis.	En./Dis.	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Video BIOS Cacheable	Dis.	En.	En./Dis.	Selecting Enabled allows caching of the video BIOS ROM at C0000h plus the VGA BIOS size, resulting in better video performance. However, in any program writes to this memory area, a system error may occur.
Video RAM Cacheable	Dis.	En.	En./Dis.	When Enabled, video memory region is cacheable. Some off-board video card drivers may behave strangely; in such a case, disable this option.
8 Bit I/O Recovery Time	3	1	1-8, NA	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 8-bit and 16-bit I/O.
16 Bit I/O Recovery Time	2	1	1-4, NA	

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Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PCI/VGA Palette Snoop	Dis.	Dis.	En./Dis.	Palette snooping allows multiple VGA devices operating on different buses to handle data from the CPU on each set of palette registers. When set to Enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both to be identical. When set to Disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers.
Passive Release	En.	En.	En./Dis.	When Enabled, CPU to PCI bus accesses are allowed during passive release otherwise the arbiter only accepts another PCI master access to local SDRAM.
Delayed Transaction	Dis.	Dis.	En./Dis.	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specifications version 2.1.
Supervisor I/O Base Address	190h	190h	190h, 290h, 390h	This option determines the base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer.
Power-Supply Type	AT	AT	AT, ATX	This option selects the type of power supply.
AGP Aperture Size (MB)	64	64	4 to 256	This option selects the size in megabytes of the AGP Aperture.
Video BIOS Shadow	En.	En.	En./Dis.	Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. Award permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals. Shadowing copies from ROM into system RAM, where the CPU can read it through the 64-bit DRAM bus. Firmware not shadowed must be read by the system through the 8 or 16-bit ISA bus. Shadowing improves the performance of the system BIOS and similar firmware for expansion peripherals. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Note that on a PCI VGA card (on board or off-board), the VGA BIOS is always shadowed. Video BIOS shadows into memory area C0000 plus the VGA BIOS size. The remaining areas between C0000 and DFFFF shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.
C8000-CBFFF	En.	En.	En./Dis.	
CC000-CFFFF	En.	En.	En./Dis.	
D0000-D3FFF	En.	En.	En./Dis.	
D4000-D7FFF	En.	En.	En./Dis.	
D8000-DBFFF	En.	En.	En./Dis.	
DC000-DFFFF	En.	En.	En./Dis.	

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4.1.8 Power Management Setup

This part of the setup configures power conservation options.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
ACPI Function	Dis.	En.	En./Dis.	The Advanced Configuration and Power Interface (ACPI) allows Operating System Direct Power Management (OSPM) and make advanced configuration architectures possible. When Enabled, the OS supports ACPI or OSPM (e.g., Win98, and Windows 2000 **Note: When Enabled, and the OS is ACPI compliant, the OS setting take precedence over all settings in this menu.**
Power Management	User Def.	User Def.	User Define, Min Saving, Max Saving	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. Max Saving: Maximum power savings. Inactivity period is 1 minute in each mode. Min Saving: Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). User Define: Set each mode individually. Select time-out periods in the PM Timers section (see below).
PM Control by APM	Yes	Yes	Yes, No	If Yes, the OS can control the PM by APM calls. If No, the BIOS will control the PM (Power Management)
Video Off Method	V/H SYNC + Blank	V/H SYNC + Blank	Blank Screen V/H SYNC+Blank, DPMS,	Determines the manner in which the monitor is blanked. V/H SYNC + Blank: System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS Support: Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values. Blank Screen: System only writes blanks to the video buffer.
Video Off After	Standby	Standby	NA, Suspend, Standby, Doze,	As the system moves from lesser to greater power-saving modes, select the mode **in which you want the monitor to blank.**
Doze Mode	Dis.	Dis	Disable 1min to 1h	After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at lower speed while all other devices still operate at full speed.
Standby Mode	Dis.	Dis.	Disable 1min to 1h	After entering Doze mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, the video shuts off while all other devices still operate at full speed.
Suspend Mode	Dis.	Dis.	Disable 1min to 1h	After entering Standby mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, all devices including the CPU shut off and the system waits for an event to wake them up again.
HDD Power Down	Dis.	Dis.	Disable 1-15min	After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active. The HDD power down mode is only available if the hard drive has this capability.
HDD Down When Suspend	En.	En.	En./Dis.	When Enabled and the system goes in Suspend Mode, the hard disk is shut down.
Throttle Duty Cycle	75.0%	75.0%	12.5%-75.0%	When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of time that the clock **does not run.** When 12.5% is selected, the CPU is running at nearly Full Speed and if 75% is selected, the CPU will be idle 75% of time.
PCI / VGA Act-Monitor	Dis.	Dis.	En./Dis.	When Enabled, continuous video activity restarts the global timer for Standby mode.
Soft-OFF by PWR-BTTN	Instant-off	Instant-off	Instant-off, Delay 4 sec.	This option only works with an ATX power supply. It allows two configurations for the power button: Instant-off for power supply on/off switch, or Delay 4 sec. for entering Suspend Mode after pressing the button at least 4 seconds.

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Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Resume by Ring	Dis.	En.	En./Dis.	When Enabled and a modem is connected to a serial port, allows a modem ring to re-activate the CPU when in Suspend mode.
IRQ 8 Break Suspend	Dis.	En.	En./Dis.	When Enabled, the RTC alarm interrupt is monitored to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Resume by Alarm	Dis.	Dis.	En./Dis.	When Enabled, allows setup of a time to re-activate the CPU when in Suspend mode with the options Date (of Month) Alarm and Time (hh:mm:ss) Alarm. **Note: The IRQ 8 Break Suspend option in this setup screen must be Enabled to use the RTC alarm.**
Reload Global Timer Events:				
IRQ[3-7,9-15], NMI	Dis.	En.	En./Dis.	When any of the options below is Enabled, monitoring of the interrupt will occur to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Primary IDE 0	Dis.	En.	En./Dis.	
Primary IDE 1	Dis.	En.	En./Dis.	
Secondary IDE 0	Dis.	En.	En./Dis.	
Secondary IDE 1	Dis.	En.	En./Dis.	
Floppy Disk	Dis.	En.	En./Dis.	
Serial Port	En.	En.	En./Dis.	
Parallel Port	Dis.	En.	En./Dis.	

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4.1.9 PnP/PCI Configuration

This part of the setup configures PnP/PCI options.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PNP OS Installed	Yes	No	Yes, No	If the operating system (OS) is Plug and Play (for example Windows 95), select "**Yes**" if you want the OS to allocate resources according to Plug and Play standards, or "**No**" if you want the same resource allocations at every system boot-up. Select "**No**" when the OS is **not** Plug and Play (for example, DOS). **Note: When set to "Yes", only the boot devices will get Resources.**
Resources Controlled By	Auto	Man.	Auto, Man.	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear as well as Used Mem Base Address and Length as the BIOS automatically assigns them.
Reset Configuration Data	Dis.	Dis.	En./Dis.	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.
IRQ *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for an IRQ line, this resource will not be available for PCI/ISA PnP.
DMA *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for a DMA channel, this resource will not be available for PCI/ISA PnP.
Init Display First	Onboard	Onboard	PCI Slot, Onboard, AGP	Initializes the specified video display. The chosen display becomes the primary display. Other display devices are ignored by the BIOS and configured by the OS.
Assign IRQ For VGA	Dis.	Dis.	En./Dis.	When Enabled, the video card is assigned an IRQ.
Assign IRQ For USB	En.	En.	En./Dis.	When Enabled, the USB is assigned an IRQ. When Disabled, the IRQ is freed up for another purpose.
PCI Latency Timer	32	32	0-255 (integers)	This option specifies the value of the Latency Timer for the PCI bus master, in units of PCI bus clocks.
Used MEM Base Address	N/A	N/A	N/A, C800, CC00, D000, D400, D800, DC00	Select a base address for the memory area used by any peripheral that requires high memory.
Used MEM length	16K	16K	16K, 32K, 48K, 64K	Select a base address for the memory area used by any peripheral that requires high memory. When this option is not set to N/A, the menu for used memory lengths available is displayed.

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4.1.10 CPU/Board Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Current Processor(s) Speed	nnn	nnn	nnn	This option displays the current processor speed.
Front Side Bus Speed	nnn	nnn	nnn	This option displays the current Front Side Bus speed. This speed is selected by the CPU auto-detection logic.
Thermal Management Options:				
. Thermal Management	Dis.	Dis.	En./Dis.	When this option is enabled, the CPU temperature is monitored. Whenever the CPU overheats, the CPU slows down to lower the temperature.
. Thermal Audio Alarm	Dis.	Dis.	En./Dis.	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. Such an alarm may not be supported by the Operating System.
. CPU 1 Die Temperature	-	-	Varies	Displays the current die (internal) CPU temperature, when Thermal Management is enabled.
. Resume Alarm (°C)	50	50	10-70	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
. Overheat Alarm (°C)	70	70	30-90	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm
. CPU1 Local Temperature	-	-	Varies	Displays the current case (external) CPU temperature, when Thermal Management is enabled.
. Resume Alarm (°C)	42	42	10-70	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
. Overheat Alarm (°C)	50	50	30-90	
Save CMOS in Flash	Dis.	Dis.	En./Dis.	Saving CMOS memory content into Flash Memory will prevent to loose CMOS options when battery fails.
Watchdog Timer	Dis	Dis	En./Dis.	This option enables the Watchdog option when the POST is running.
Watchdog After POST	Ds	Dis	En./Dis.	This option enables Watchdog circuit after the POST sequence
Watchdog Duration (ms)	262144	262144	64 to 262144	Use this option to setup duration time (in ms) of the Watchdog timing circuitry.
Current CPU Fan 1 and 2 speed	-	-	Varies	Speed sensing device sets this value according to the fan speed. If no fan is installed or if a fan has no tachymetric capability, this value will be 0.
Current Vcpp1 and 2	-	-	Varies	This value is set according to the actual value of Vcpp1 & Vcpp2
Vin values : +12V, +5V, +3.3V, +2.5V	-	-	Varies	The values of these voltages are each displayed according to the current value.

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4.1.11 Integrated Peripherals

Option	BIOS Default	Setup Default	Possible Settings	Description
On-Chip Primary/Secondary	En.	En.	En./Dis.	Select Enabled to activate the Primary/Secondary IDE channel. The four options below appear only if the On-Chip Primary option is enabled.
On-Chip Primary IDE				
Master PIO Slave PIO Master UDMA Slave UDMA	Auto	Auto	Auto, Modes 0-4	Use this option to set a PIO mode (0-4) for each of the onboard IDE devices. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.
On-Chip Secondary IDE				
Master PIO Slave PIO Master UDMA Slave UDMA	Dis.	Auto	Auto, Disabled.	Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.
IDE HDD Block Mode	Dis.	En.	En./Dis.	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
Onboard PCI SCSI Chip	En.	En.	En./Dis.	Enables/disables the onboard SCSI controller.
Ethernet Controller 1 and 2	En.	En.	En./Dis.	Enables/disables the onboard Ethernet controller.
USB Keyboard Support	OS	OS	OS/BIOS	This option is for DOS and BIOS support only (Win 95 has it is own drivers). **It does not enable or disable the USB controller.**
PS/2 Mouse Function Control	Auto	Auto	Auto/Dis.	When set to Auto, the PS/2 mouse is automatically enabled, if it is present.
Onboard FDC Controller	En.	En.	En./Dis.	Select Disabled to disable the onboard floppy disk controller (FDC).
Onboard Serial Port 1	3F8/ IRQ4	3F8/ IRQ4	Dis, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3	Select a COM port address and IRQ# for Serial Port 1
Onboard Serial Port 2	Dis	2F8	3F8,2F8, 3E8, 2E8 Disabled	Select a COM port address for Serial Port 2.
IRQ Line	3	3	3,4,5,7	Sets IRQ line for serial port 2
Onboard Serial Port 3	3E8/ IRQ4	3E8/ IRQ4	Dis, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3	Select a COM port address and IRQ# for Serial Port 3
Serial Port 3 Mode	RS-232	RS-232	RS-232 RS-422 RS-485	Select the operation mode for Serial Port 3.
Onboard Serial Port 4	Dis	2E8	3F8,2F8, 3E8, 2E8 Disabled	Select a COM port address for serial port 4.
IRQ Line	3	3	3,4,5,7	Sets the IRQ line for serial port 4.
Onboard Parallel Port	378/ IRQ7	378/ IRQ7		Select a LPT address and IRQ# for the physical parallel (printer) port. Possible settings are: Disabled, 3BC/IRQ7, 378/IRQ7, 278/IRQ5,
Parallel Port Mode	ECP + EPP1.9	ECP + EPP1.9		Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support ECP or EPP mode. Possible settings are SPP, EPP1.9+SPP, ECP, ECP+EPP1.9, Normal, EPP1.7+SPP, ECP+EPP1.7
ECP Mode Use DMA	3	3	1, 3	Select a DMA channel for the parallel port.

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4.2. BIOS UPDATE & EMERGENCY PROCEDURE

BIOS UPDATE PROCEDURE

The BIOS update procedure can be found with the Emergency Recovery procedure on our ftp site: ftp://ftp.kontron.ca/Support in the FAQ section:

Download the FAQ# KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

EMERGENCY PROCEDURE

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and falled back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

Please go on our FTP site in order to get the latest Emergency Recovery BIOS for that specific product.

BIOS maybe found at: Ftp://Ftp.Kontron.ca/Support/BIOS_Emergency/

Emergency Recovery Procedure is included within the Zip file of the Emergency BIOS to download. Latest Emergency Recovery procedure can be found on the FAQ section of the FTP site under FAQ # KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

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4.3. VT100 MODE

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.3.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix® or Procom® can also be used.

4.3.2 Setup & Configuration

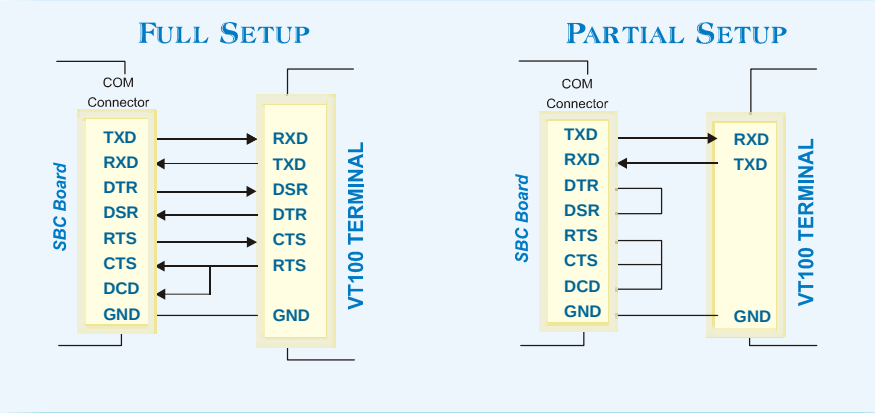
Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the “BIOS Feature Setup”
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

> NOTE
>
> If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.
8. Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.

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4.3.3 Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bauds.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video.

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PART 5

APPENDICES

A. BOARD SPECIFICATIONS

B. MEMORY & I/O MAPS

C. INTERRUPT LINES

D. BOARD DIAGRAMS

E. CONNECTOR PINOUTS

F. BIOS SETUP ERROR CODES

G. EMERGENCY PROCEDURE

H. GETTING HELP & RMA

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A. BOARD SPECIFICATIONS

FEATURES	DESCRIPTION
Overview	CompactPCI System Processor board
Supported Microprocessors	Pentium III Processor – Low Power 500MHz
CHIPSET	Intel 440BX AGPset. 22-signal High-Availability controller: #Select, #Healthy, #Reset for 7 CPCI I/O slots #Enum, (43 with mezzanine)
Bus Interface	100MHz Front side bus CompactPCI bus,64 bits (33MHz) through J1 and J2 PCI-PCI bridge: DEC 21154; supports up to 7 REQ/GNT for fully loaded CompactPCI® system PCI Mezzanine (PMC) Proprietary Mezzanine with PCI bus, FD and EIDE support SMBus (for power management of CPU temperature monitoring, DRAM control, clock buffers and power control)
Cache Memory	cPCI-MXS64 : Level 1: 16/16KB instruction/Data CPU-internal Level 1 Level 2: 256KB internal, 64-bit wide, pipelined burst
System Memory	Three 168-pin Latching DIMM sockets, 64/72-bit Up to 768Mb of SDRAM with parity or ECC (for single bit error correction and double bit error detection)
Data Path	64-bit on CPU, 32-bit on video memory; 32-bit on local PCI and 64-bits on CompactPCI connectors
Interrupts	11 edge sensitive and configurable 4 PCI level sensitive, configurable to any interrupt vector for PnP compatibility.
Flash Memory	512KB for BIOS field upgrade; Silicon Serial ID TAG for unique board identification accessible via software.
Video	32-bit AGP video controller (Intel 69000) with 2MB video memory CRT resolutions up to 1024 x 768 x 64K colors or 1280 x 1024 x 256 colors
Clock/Calendar	Real-time clock with (replaceable) battery backup, CMOS RAM

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Board Specifications (continued)

<table>
<tr><td>Connectors in “Front” configuration</td><td>Front Plate
CRT — 15-pin D-Sub
COM1 — 9-pin D-Sub
Ethernet 1 and 2 — 2 x RJ-45 with built-in LEDs
PS/2 mouse + Keyboard — 6-pin mini-DIN</td></tr>
<tr><td>Interfaces on J3/J4/J5</td><td>Rear CPCI I/O Connectors (J3/J4/J5)
(Rear-panel transition module, cTM80-STD2S available separately)
CRT
Parallel Port
Speaker I/F
Ethernet (2)
SCSI
Fan fail monitoring
Serial Ports (4)
SMBus
Reset Switch
PS/2 mouse
EIDE (2)
USB (2)
I^2C
Infrared
Keyboard
Floppy disk I/F
Onboard Expansions
PCI Mezzanine Card PMC.
Proprietary mezzanine.
CompactFlash.</td></tr>
<tr><td>I/O</td><td>I/O — SMC FDC37C672
USB Ports — Two
Serial Ports — Four (three RS-232, COM1, 2, 4; Com3 configurable as RS-422/485)
Parallel Port — One bi-directional with all IEEE 1284 protocols supported with BIOS selectable IRQs and addressing
Floppy Disk — Support for two drives (360KB to 1.44MB)
EIDE — Two channel Bus Master PCI EIDE; support for four IDE Type 4 drives (master/slave configuration); LBA, PIO Mode 0-4 and Ultra DMA/33.
CompactFlash™ — Optional bootable CompactFlash™ disk interfaces to primary EIDE channel, user upgradable, master/slave.
SCSI — LSI Logic Symbios ® SYM53C895 PCI to Ultra2 SCSI I/O Processor with LVD Link™ Universal Transceivers. Transfert rate up to 80MB/s
Ethernet — Two 10/100Mb/s Ethernet, PCI 10/100Base-TX ports (Intel 82559 controller)
HD/FD Mezzanine Card — Optionally onboard using Kontron’s cMC series mezzanine cards</td></tr>
</table>

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Board Specifications (continued)

Supervisory	Two-stage software programmable Watchdog timer drives NMI on 1st stage and system reset on 2nd stage. Programmable CPU temperature monitor/alarm Power failure/low battery detector Front Panel LED : IDE activity and SCSI activity, Hot Swap, Ethernet and link activity
OS Compatibility	MS-DOS™, Windows® 95/98, Windows®NT, VxWorks™, pSOS™, QNX™, Linux, Novell, and Solaris Mechanical.
BIOS Features	Award Elite BIOS 4.51 in Boot Block Flash with recovery code; save CMOS in Flash option, and boot from LAN capability. Auto configuration, extended setup. CC000-E0000 address blocking; PnP tables. Setup console redirection to serial port *(VT100 mode) with CMOS setup access. Software enable/disable of onboard Ethernet & SCSI; hardware enable/disable of onboard video Diskless, keyboardless and videoless operation extensions. System, video, SCSI, LAN and extension BIOS shadowing. Programmable bus and I/O speeds, and memory wait states Advanced security feature for floppy and HDD; DMI & HDD S.M.A.R.T. support. Advanced Configuration and Power Interface (ACPI 1.0), Advanced Power Management (APM 1.2), advanced thermal management (resume, overheat alarm and auto slow-down), and Green support.
Mechanical	Compliant to IEEE 1101.10, compliant to PICMG2.0 Rev 2.1) 233x160x41 mm / 9.2 x 6.3 x 1.6 in, 6U x 8HP (dual slot) Mechanically 233x160x20.5 mm / 9.2 x 6.3 x 0.8 in;6U x 4HP (single slot) Mechanically
Power Requirements	Supply Voltages : +3.3, +5%-3%, +5V +5%-3%, +12V ±5% Supply Current:* +3.3V, 4.5 Amps maximum +5V, 3.5 Amps maximum +12V, 0.1 Amps maximum Power Dissipation cPCI-MXS64 : 34W maximum * Mobile Pentium III, 500MHz with 768MB SDRAM

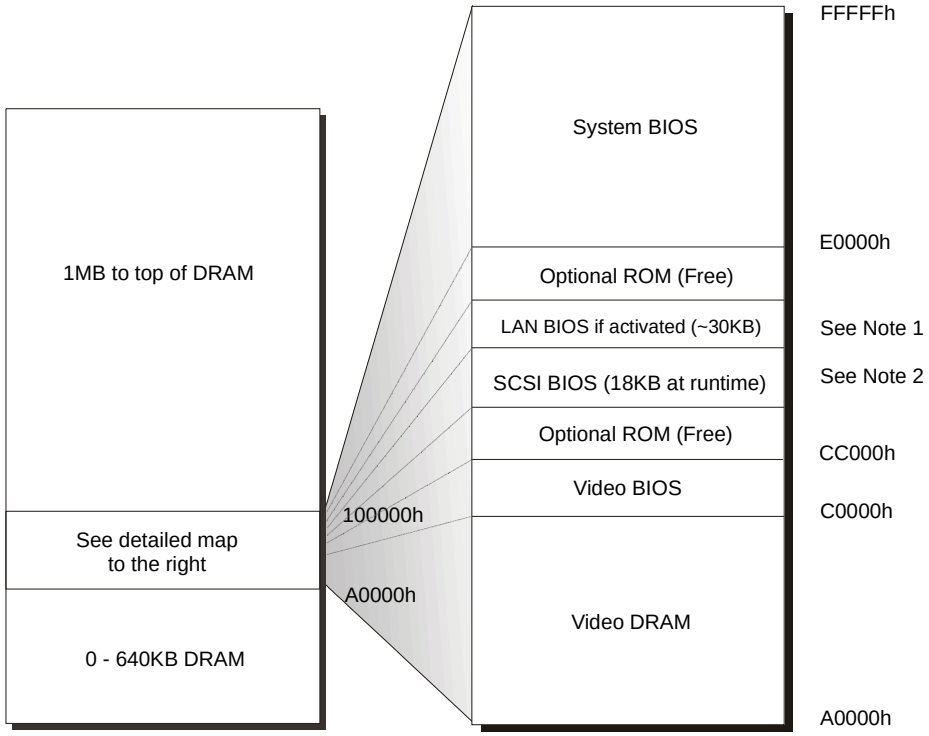
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Board Specifications (continued)

Environmental		Operating	Storage and Transit
	Temperature	0-60°C / 32-140°F	-40 to +70°C / -40 to 158°F
	Humidity	5% to 95% @ 40°C/104°F non-condensing	5% to95% @ 40°C/104°F non-condensing
	Altitude	4,572m / 15,000 ft	15,240m / 50,000ft
	Shock	Designed to meet IEC 68-2-27	
	Vibration	Designed to meet IEC 68-2-6	
	Reliability	MTBF: cPCI-MXS64 : 54810 hours @ 20°C (MIL-HDBK-217F) Board serial number in EEPROM USB, keyboard and mouse protected by self-resetting fuse 2 year limited warranty Designed to meet or exceed : Safety: UL1950, CSA C22.2 No 950, EN 60950, IEC950 EMI/EMC FCC 47 CFR Part 15/CISPR22, Class B, CE Mark to EN55022/EN50082	

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B. MEMORY & I/O MAPS Memory Mapping



Note 1 : LAN BIOS address may vary

Note 2 : SCSI BIOS address may vary.
Size is only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-FFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
E0000-FFFFF	System BIOS
100000-Top of DRAM	1 MB - Top of DRAM

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B.1 I/O MAPPING

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
190-197	290-297	390-397		Kontron Control Port
1F0-1F7, 3F6				Primary IDE
170-177, 376				Secondary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	278-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

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C. INTERRUPT LINES

C.1 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard (Output Buffer Full)	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Parallel Port 2 or Available [1]	IRQ 13	Coprocessor Error
IRQ *6	Floppy Controller	IRQ 14	Primary IDE * or available [1]
IRQ 7*	Parallel Port 1 or Available [1]	IRQ 15	Secondary IDE * or available [1]

* :All functions marked with an asterisk (*) can be disabled or reconfigured.
1 Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

C.2 DMA CHANNELS

The cPCI-MXS64 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

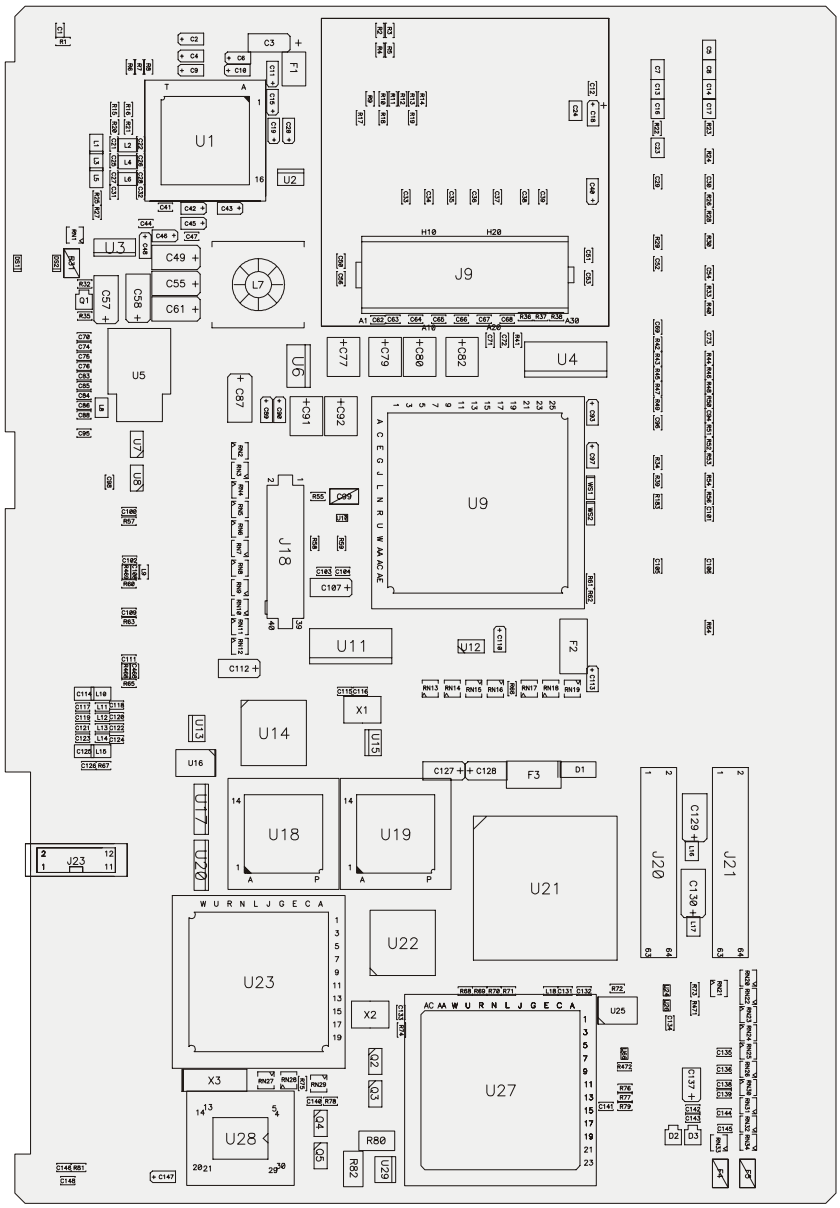
According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

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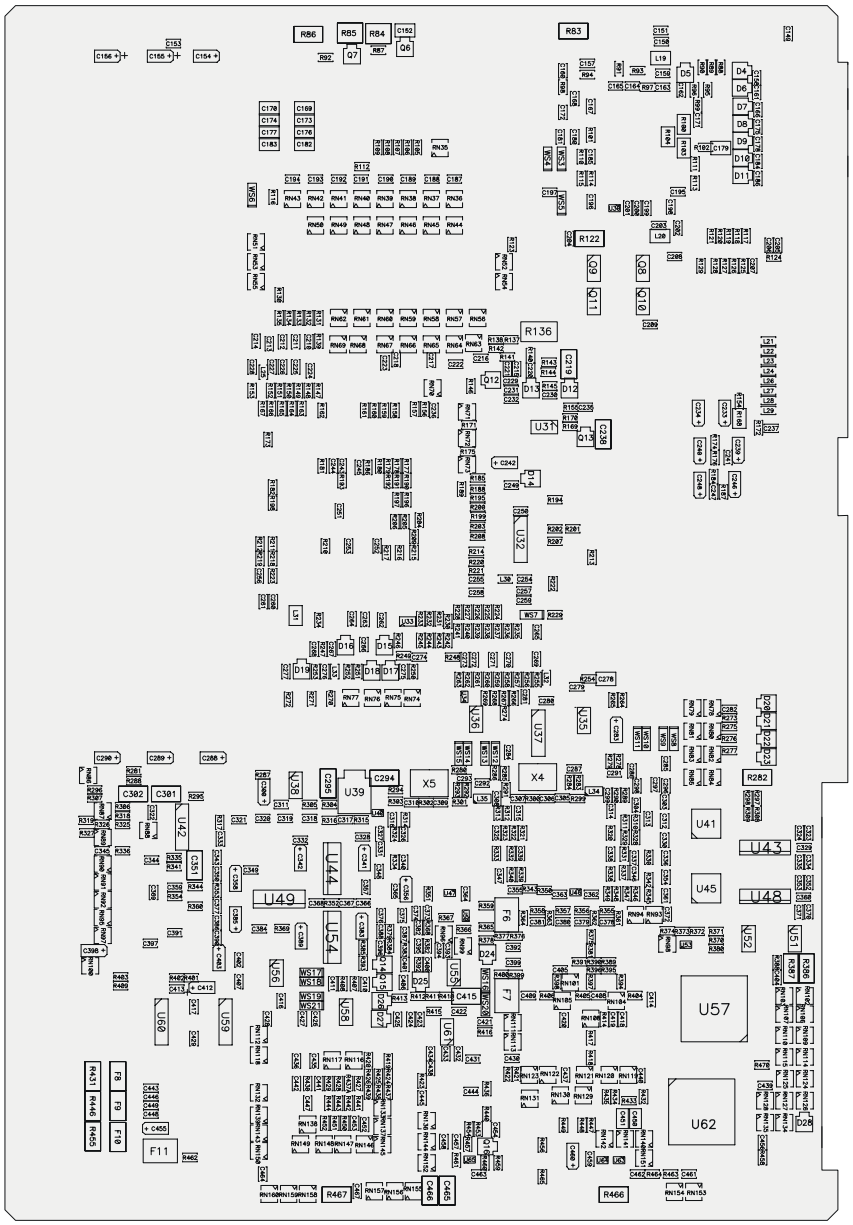
D. BOARD DIAGRAMS

D.1 TOP DEVICES SURFACE MOUNT



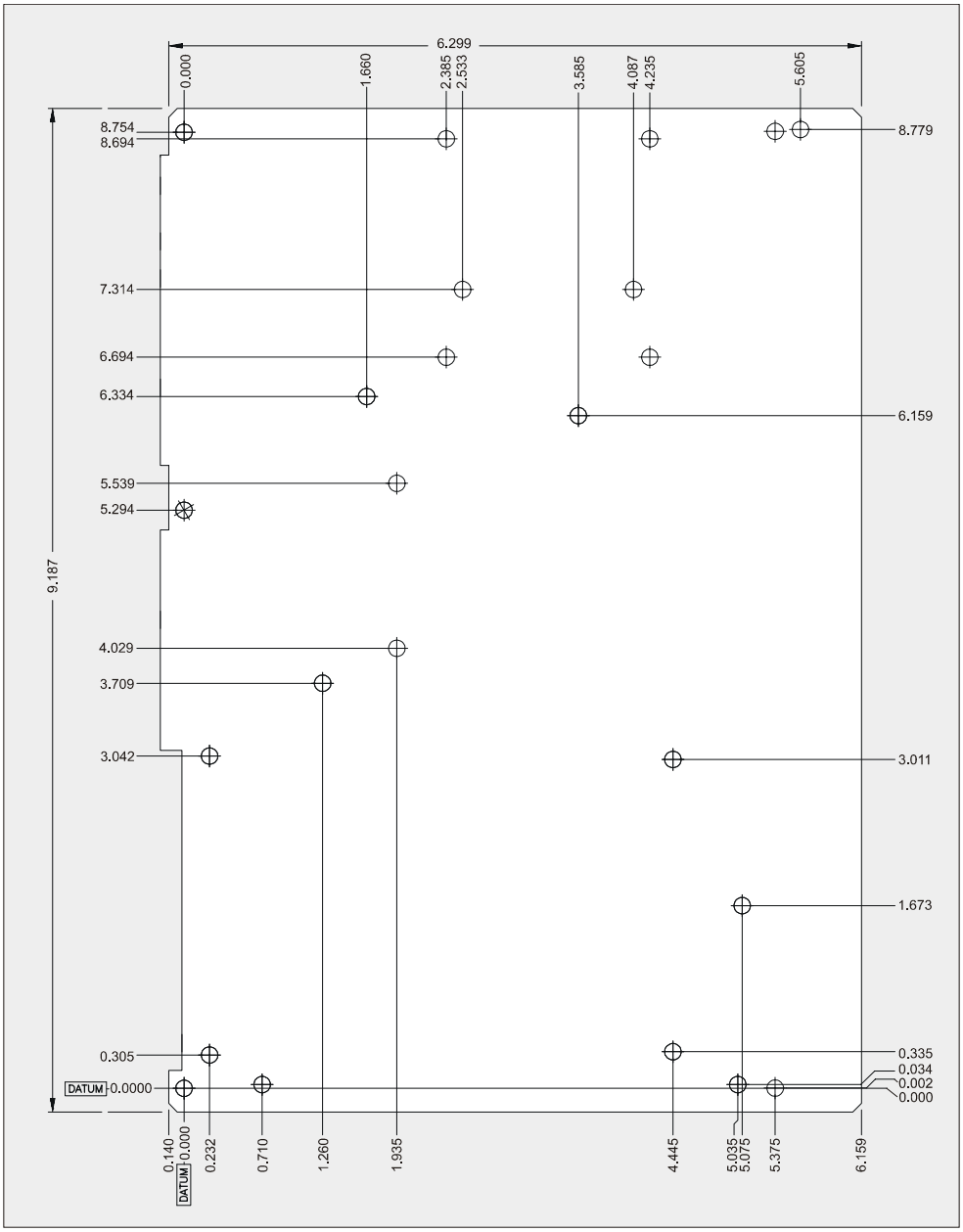
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D.2 ASSEMBLY BOTTOM DIAGRAM



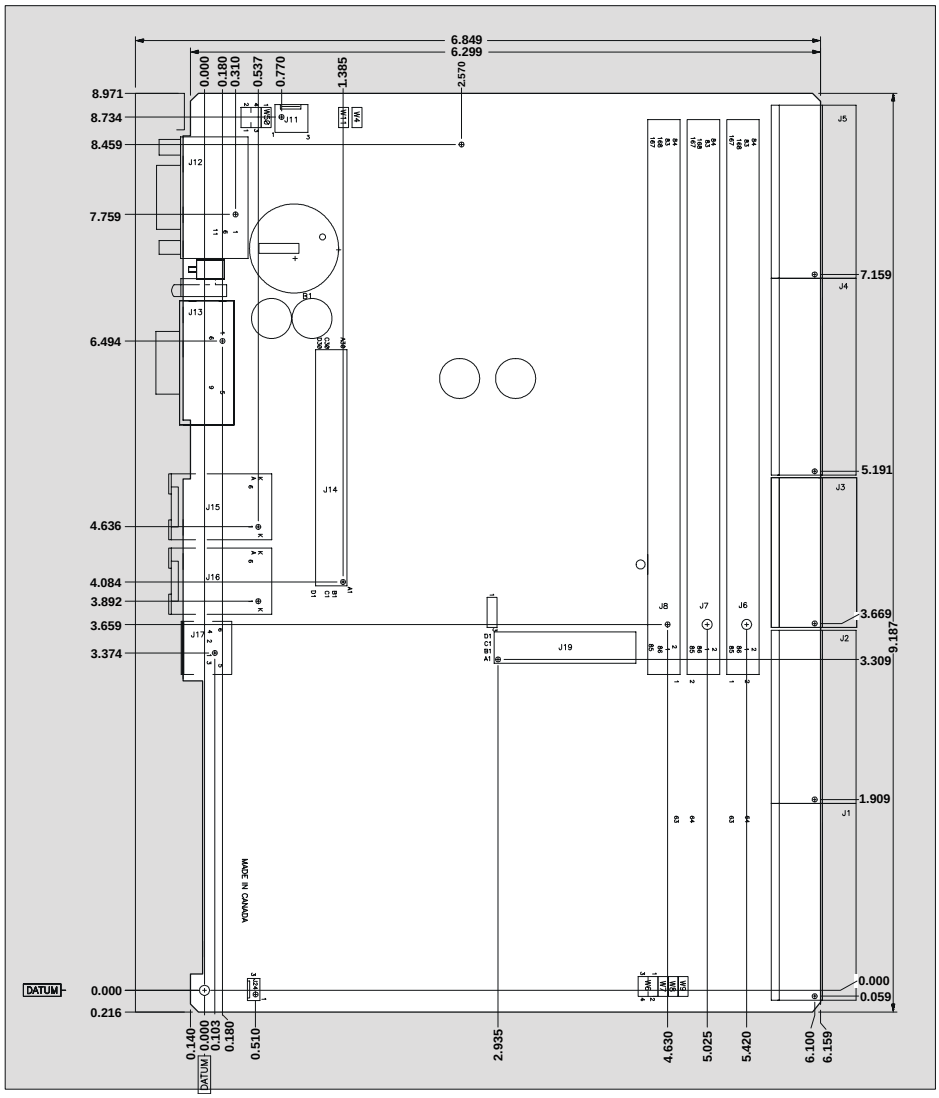
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D.3 MOUNTING HOLES



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D.4 CONNECTOR HOLES



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E. CONNECTOR PINOUTS

E.1 cPCI-MXS64 CONNECTORS AND HEADERS

MXS64	Connector J14
J1	CPCI Bus Connector
J2	CPCI Bus Connector
J3	CPCI I/O Connector
J4	CPCI I/O Connector
J5	CPCI I/O Connector
J12	CRT VGA Connector (Front panel configuration only)
J13	Serial Port 1 – RS-232 (Front panel configuration only)
J14	Mezzanine PCI Connector
J15	Ethernet 1 Connector (Front panel configuration only)
J16	Ethernet 2 Connector (Front panel configuration only)
J17	Keyboard/Mouse Connector
J18	CompactFLASH Disk Connector
J19	Mezzanine Storage Connector
J20, J21	PCI Mezzanine Card (PMC)
J24	Hot Swap Switch
S1	Reset Switch
BT1	CMOS Battery Backup connector

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E.2 J1 cPCI Bus

	ROW A	ROW B	ROW C	ROW D	ROW E
1	VCC5E	-12VE	RSV	+12VE	VCCE
2	RSV	VCCE	RSV	RSV	RSV
3	INTA#	INTB#	INTC#	VCCE	INTD#
4	Reserved	HEALTHY#	VI/O	INTP	INTS
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0#
6	REQ0#	GND	VCC3E	CLK0	AD31
7	AD30	AD29	AD28	GND	AD27
8	AD26	GND	V I/O	AD25	AD24
9	CBE3#	RSB	AD23	GND	AD22
10	AD21	GND	VCC3E	AD20	AD19
11	AD18	AD17	AD16	GND	CBE2#
12 13 14	**KEY AREA**				
15	VCC3E	FRAME#	IRDY#	BD_SEL#	TRDY#
16	DEVSEL#	GND	V I/O	STOP#	LOCK#
17	VCC3E	I2C_SCL	I2C_SDA	GND	PERR#
18	SERR#	GND	VCC3E	PAR	CBE1#
19	VCC3E	AD15	AD14	GND	AD13
20	AD12	GND	V I/O	AD11	AD10
21	VCC3E	AD9	AD8	M66EN	CBE0#
22	AD7	GND	VCC3E	AD6	AD5
23	VCC3E	AD4	AD3	VCCE	AD2
24	AD1	VCCE	V I/O	AD0	ACK64#
25	VCCE	REQ64#	ENUM#	VCC3E	VCCE

Long pins : 3D, 4C,5D, 6C, 7D, 9D, 10D, 17D, 19D, 22C, 23D, 24C

Short pins : 9B, 15D

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E.3 J2 cPCI Bus

		ROW A	ROW B	ROW C	ROW D	ROW E
1		S_CLK1	GND	REQ1#	GNT1#	REQ2#
2		S_CLK2	S_CLK3	SYSEN#	GNT2#	REQ3#
3		S_CLK4	GND	GNT3#	REQ4#	GNT4#
4		V I/O	BRSV	CBE7	GND	CBE6#
5		CBE5#	RSV	V I/O	CBE4#	PAR64
6		AD63	AD62	AD61	GND	AD60
7		AD59	GND	V I/O	AD58	AD57
8		AD56	AD55	AD54	GND	AD53
9		AD52	GND	V I/O	AD51	AD50
10		AD49	AD48	AD47	GND	AD46
11		AD45	GND	V I/O	AD44	AD43
12		AD42	AD41	AD40	GND	AD39
13		AD38	GND	V I/O AD37	AD36	
14		AD35	AD34	AD33	GND	AD32
15		BRSV	GND	FAL#	REQ5	GNT5#
16		BRSV	BRSV	DEG#	GND	BRSV
17		BRSV	GND	PRST#	REQ6#	GNT6
18		BRSV	BRSV	BRSV	GND	BRSV
19		GND	GND	Reserved	Reserved	Reserved
20		CLK5	GND	RSV	GND	RSV
21		CLK6	GND	RSV	RSV	RSV
22		GA4	GA3	GA2	GA1	GA0

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E.4 J3 cPCI Bus

	ROW A	ROW B	ROW C	ROW D	ROW E
1	RSV	SCSI:D11+	SCSI:I/O+	RSV	GND
2	GND	RSV	GND	RSV	GND
3	RSV	VCC	SCSI:D9+	SCSI:DIFFSENS	RSV
4	RSV	SCSI:D10+	RSV	SCSI:CD+	Rsv
5	RSV	GND	RSV	GND	SCSI:SEL+
6	LAN0:SPLED	LAN0:LINKLED	LAN0:ACTLED	LAN1:LINKLED	LAN1:SPLED
7	LAN1:ACTLED	SD7	SD6	SD5	SD4
8	GND	VCC	VCC	SD3	SD2
9	LAN1 :ETX+	LAN1 :ETX-	LAN1 :ERX+	LAN1 :ERX-	GND
10	GND	WR_80#	SD1	+12V	+12V
11	COM4:DCD	GND	COM4:RXD	COM4:DSR	COM4:TXD
12	COM4:RTS	COM4:CTS	COM4:RI	VCC	COM4:DTR
13	COM3:DCD	VCC	COM3:RXD	COM3:DSR	COM3:TXD
14	COM3:RTS	COM3:CTS	COM3:RI	SCSI:D8+	JDTR3#
15	S2BDSEL#	S3BDSEL#	S3PCIRST#	SD0	S4BDSEL#
16	S2HEALTHY#	S3HEALTHY#	RSV	RSV	SCSI:REQ+
17	S2CIRST#	RSV	RSV	S4HEALTHY#	S4PCIRST#
18	RSV	IDE1:DASP#	IDE0:DASP#	COM2:IRRX	COM2:IRTX
19	RSV	RSV	RSV	S5BDSEL#	RSV

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E.5 J4 cPCI Bus

	ROW A	ROW B	ROW C	ROW D	ROW E
1	I2C:CLK	I2C-DATA	LID	EXTFANFAIL0#	EXTFANFAIL1#
2	SM-BYPASS#	SCSI:D11-	SCSI:D10-	SCSI:D9-	SCSI:D8-
3	SCSI:IO-	SCSI:REQ-	SCSI:CD-	SCSI:SEL-	SCSI:MSG-
4	SCSI:RST-	SCSI:ACK-	SCSI:BSY-	SCSI:BSY+	SCSI:ATN-
5	SCSI:ACK+	N.C.	SCSI:TERMPWR	SCSI:TEMPWR	SCSI:DPL+
6	SCSI:ATN+	SCSI:DPL-	SCSI:D7-	SCSI:D6-	SCSI:D5-
7	SCSI:D4-	SCSI:D3-	SCSI:D2-	SCSI:D1-	SCSI:D0-
8	SCSI:DPH-	SCSI:D15-	SCSI:D14-	SCSI:D13-	SCSI:D12-
9	SCSI:RST+	SCSI:MSG+	S5HEALTHY#	VGA:SDATA	S5PCIRST#
10	VGA:SCLK	VGA:HSYNC	VGA:VSYNC	VGA:RED	VGA:GREEN
11	VGA:BLUE	SCSI:D3+	S6BDSEL#	SCSI:D5+	SCSI:D6+
12 13 14	**KEY AREA**				
15	SCSI:D0+	VCC	VCC	S6HEALTHY#	S6PCIRST#
16	LAN0 :ETX+	LAN0 :ETX-	LAN0 :ERX+	LAN0 :ERX-	SCSI:D7+
17	IDE1:RESET#	SCSI:D15+	IDE1:D7	IDE1:D8	IDE1:D6
18	IDE1:D9	IDE1:D5	IDE1:D10	IDE1:D4	IDE1:D11
19	IDE1:D3	IDE1:D12	IDE1:D2	IDE1:D13	IDE1:D1
20	IDE1:D14	IDE1:D0	IDE1:D15	SCSI:D4+	S7BDSEL#
21	IDE1:REQ	SCSI:D13+	IDE1:IOW#	SCSI:DPH+	IDE1:IOR#
22	SCSI:D12+	IDE1 :IORDY	S7HEALTHY#	IDE1:DACK#	IDE1:IRQ15
23	IDE1:IO16	IDE1: A1	SCSI:D2+	IDE1:A0	IDE1:A2
24	IDE1:CSI#	IDE1:CS3#	SCSI:D14+	SCSI:D1+	SM_BTI#
25	S7PCIRST#	S8BDSEL#	S8HEALTHY#	S8PCIRST#	VCC

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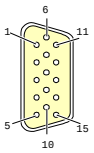
E.6 J5 cPCI Bus

		ROW A	ROW B	ROW C	ROW D	ROW E
1		IDE0:RESET#	IDE0:RESET#	IDE0:D7	IDE0:D8	IDE0:D6
2		IDE0:D9	IDE0:D5	IDE0:D10	IDE0:D4	IDE0:D11
3		IDE0:D3	IDE0:D12	IDE0:D2	IDE0:D13	IDE0:D1
4		IDE0:D14	IDE0:D0	USB1:GND	IDE0:D15	IDE0:IRQ14
5		IDE0:REQ	IDE0:IORDY	IDE0:IOW#	IDE0:DACK#	IDE0:IOR#
6		IDE0:IOCS16	GND	IDE0:PDIAG#	IDE0:A0	IDE0:A2
7		IDE0:CS1#	IDE0 :CS3#	IDE0 :A1	PRI_PD1	FD_WGATE#
8		FD:DRVEN1#	FD:INDEX#	FD:MTR0#	FD:DS1#	FDE0_A2#
9		FD:MTR1#	FD:DIR#	FD:STEP#	FD:WDATA#	FD:DRVEN0#
10		FD:TRK0#	FD:WRTP RT#	FD:RDATA#	FD:HDSEL#	FD:DSKCHG#
11		COM2:DCD	GND	COM2:RXD	COM2:DSR#	COM2:TXD
12		COM2:RTS	COM2:CTS	COM2:R#	VCC	COM2:DTR
13		COM1:DCD	VCC	COM1:RXD	COM1:DSR#	COM1:TXD
14		COM1:RTS	COM1:CTS	COM1:R#	GND	COM1:DTR
15		LPT:SLCT	LPT:PE	LPT:BUSY	LPT:ACK#	LPT:D7
16		LPT:D6	LPT:D5	LPT:D4	LPT:D3	LPT:SLCTIN#
17		LPT:D2	LPT:INIT#	LPT:D1	LPT:ERR#	LPT:D0
18		LPT:ALF#	USB1:DATA+	USB1:DATA-	USB0:GND	USB0:VCC
19		LPT:STB#	USB1:GND	USB1:VCC	USB0:DATA+	USB0:DATA-
20		VCC	SMBDATA	SMBALERT#	GND	SMBCLK
21		KB:DATA	KB:CLK	KB:VCC	MOUSE:DATA	MOUSE:CLK
22		PBRST#	GND	DIAG_OC#	VCC	SPEAKER

E.7 J12, Video (VGA)

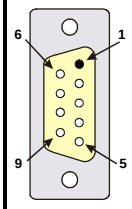
Signal		Signal		Signal	
RED	1	Analog GND	6	N.C.	11
GREEN	2	Analog GND	7	SDATA	12
BLUE	3	Analog GND	8	HSYNC	13
N.C.	4	N.C.	9	VSYNC	14
GND	5	GND	10	SCLK	15

Top View

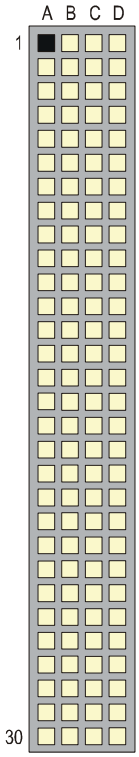


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E.8 J13, SERIAL PORT 1 - RS-232

Pin Number		Top View	Pin Number	
Signal				Signal
DSR	6		1	DCD
RTS	7		2	RXD
CTS	8		3	TXD
RI	9		4	DTR
			5	GND

E.9 J14, MEZZANINE PCI

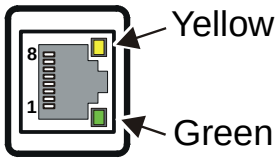
	A	B	Top View	C	D	
1	MS2_BD_SEL#	PBRST#		MS4_BD_SEL#	AD0	1
2	MS2_HEALTHY#	AD2		AD1	VCC	2
3	AD5	GND		AD4	AD3	3
4	C/BE0#	AD7		GND	AD6	4
5	GND	AD9		AD8	GND	5
6	AD11	VCC		AD10	MS8_HEALTHY#	6
7	AD14	AD13		GND	AD12	7
8	VCC3	C/BE1#		AD15	VCC3	8
9	SERR#	GND		MS4_HEALTHY#	PAR	9
10	GND	PERR#		VCC3	MEZ_SDONE	10
11	STOP#	VCC3		LOCK#	GND	11
12	VCC3	TRDY#		GND	DEVSEL#	12
13	FRAME#	GND		IRDY#	VCC3	13
14	GND	AD16		VCC3	C/BE2#	14
15	AD18	VCC3		AD17	GND	15
16	AD21	AD20		GND	AD19	16
17	VCC3	AD23		AD22	VCC3	17
18	RSV	GND		MS4_PCI_RST#	MS8_BD_SEL#	18
19	AD24	C/BE3#		MS5_BD_SEL#	MS7_PCI_RST#	19
20	GND	AD26		AD25	GND	20
21	AD29	VCC		AD28	AD27	21
22	MS2_PCI_RST#	AD30		GND	AD31	22
23	REQ_MEZ#	GND		MS5_HEALTHY#	VCC	23
24	GND	MS8_PCI_RST#		MS5_PCI_RST#	GNT_MEZ#	24
25	MS3_BD_SEL#	VCC		MS6_BD_SEL#	GND	25
26	MS3_HEALTHY#	PCLK_MEZ		MS6_HEALTHY#	MS7_HEALTHY#	26
27	MS3_PCI_RST#	VCC		MS6_PCI_RST#	GND	27
28	GND	INTA#		MS7_BD_SEL#	PCIRST#	28
29	+12V	INTB#		INTC#	INTD#	29
30	-12V	ENUM#		SMBCLK	SMBDATA	30

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J15/J16, ETHERNET 1 AND 2

Signal	
TX+	1
TX-	2
RX+	3
N.C.	4
N.C.	5
RX-	6
N.C.	7
N.C.	8

Top View

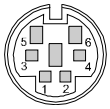


Note
These two LEDs might be reversed.

E.10 J17, PS/2 KEYBOARD/MOUSE

Signal	
KB:DATA	1
MOUSE:DATA	2
GND	3
VCC	4
KB:CLK	5
MOUSE:CLK	6

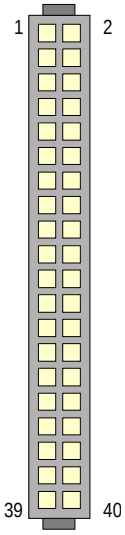
Front View



E.11 J18, COMPACTFLASH DISK

Pin Number	Signal
1	D11
3	D12
5	D13
7	D14
9	D15
11	CS1#
13	DMACK#
15	DMARQ
17	PDIAG#
19	IRQ15
21	VCC
23	GND
25	RESET#
27	CSEL
29	A1
31	A0
33	D0
35	D1
37	D2
39	IOCS16#

Top View

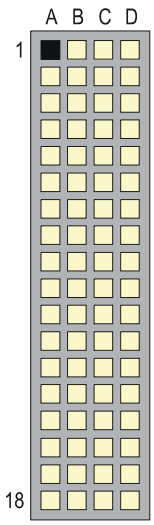


Pin Number	Signal
2	GND
4	D3
6	D4
8	D5
10	D6
12	D7
14	CS0#
16	IOR#
18	IOW#
20	VCC
22	VCC
24	GND
26	GND
28	A2
30	DASP#
32	IORDY#
34	D8
36	D9
38	D10
40	GND

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E.12 J19, STORAGE MEZZANINE

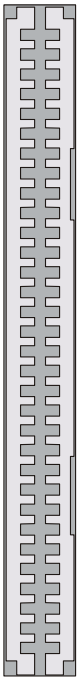
	A	B	Top View	C	D	
1	VCC	VCC		VCC	VCC	1
2	VCC	VCC		VCC	D0	2
3	MOUSE:CLK	MOUSE:DATA		D1	D2	3
4	KB:DATA	KB:CLK		D3	D4	4
5	KB:VCC	GND		D5	D6	5
6	GND	GND		D7	D8	6
7	GND	GND		D9	D10	7
8	GND	GND		D11	D12	8
9	GND	GND		D13	D14	9
10	FD:DS1#	FD:DRVEN0#		D15	BRSTDRV#	10
11	FD:DRVEN1#	FD:MTR1#		IOW#	REQ	11
12	FD:INDEX#	FD:DS0#		IORDY0	IOR#	12
13	FD:DSKCHG#	FD:ET		IRQ14	DACK#	13
14	FD:MTR0#	FD:DIR#		A0	A1	14
15	FD:STEP#	FD:WDATA#		A2	GND	15
16	FD:GATE#	FD:TRK0#		IDE:ACT#	CS1#	16
17	FD:WRTPTR#	FD:RDATA#		CS3#	DIAG#	17
18	FD:HSEL#	+12V		IOCS16#	+12V	18



Active Low Signal

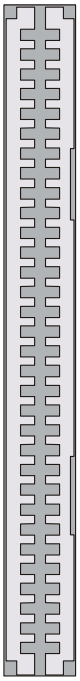
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E.13 J20, PMC

Pin Number		Top View	Pin Number	
Signal				Signal
N.C.	1		2	-12V
GND	3		4	INTA#
INTB#	5		6	INTC#
BUSMODE1#	7		8	VCC
INTD#	9		10	N.C.
GND	11		12	N.C.
PCLK	13		14	GND
GND	15		16	GNT #
REQ –#	17		18	VCC
VCC	19		20	AD31
AD28	21		22	AD27
AD25	23		24	GND
GND	25		26	C/BE3#
AD22	27		28	AD21
AD19	29		30	VCC
VCC	31		32	AD17
FRAME#	33		34	GND
GND	35		36	IRDY#
DEVSEL#	37		38	VCC
GND	39		40	LOCK#
SDONE	41		42	SB0#
PAR	43		44	GND
VCC	45		46	AD15
AD12	47		48	AD11
AD9	49		50	VCC
GND	51		52	C/BE0#
AD6	53		54	AD5
AD4	55		56	GND
VCC	57		58	AD3
AD2	59		60	AD1
AD0	61		62	VCC
GND	63		64	N.C.

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E.14 J21, PMC

Pin Number		Top View	Pin Number	
Signal				Signal
+12V	1		2	N.C.
N.C.	3		4	N.C.
N.C.	5		6	GND
GND	7		8	N.C.
N.C.	9		10	N.C.
BUSMODE2#	11		12	VCC3
PCIRST#	13		14	BUSMODE3#
VCC3	15		16	BUSMODE4#
N.C.	17		18	GND
AD30	19		20	AD29
GND	21		22	AD26
AD24	23		24	VCC3
IDSEL	25		26	AD23
VCC3	27		28	AD20
AD18	29		30	GND
AD16	31		32	C/BE2#
GND	33		34	N.C.
TRDY#	35		36	VCC3
GND	37		38	STOP#
PERR#	39		40	GND
VCC3	41		42	SERR#
C/BE1#	43		44	GND
AD14	45		46	AD13
GND	47		48	AD10
AD8	49		50	VCC3
AD7	51		52	N.C.
VCC3	53		54	N.C.
N.C.	55		56	GND
N.C.	57		58	N.C.
GND	59		60	N.C.
N.C.	61		62	VCC3
GND	63		64	N.C.

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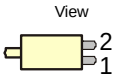
E.15 HOT SWAP SWITCH

Signal	
VCC3E	1
SW_OPEN#	2
GND	3



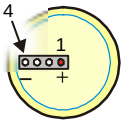
E.16 S1 – RESET SWITCH

Signal	
RESET#	1
GND	2



E.17 BT1, CMOS BATTERY BACKUP CONNECTOR

Signal	
Battery (+)	1
Battery (-)	4



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F. BIOS SETUP ERROR CODES

F.1 POST BEEP

POST beep codes are defined in the BIOS to provide low level tone indication when an error occurs during the BIOS initialization.

Beep codes consist of a combination of long and short beeps. They are described as follows:

Beep Codes

Post code	Beep Code	Description
41	**-*	Enterring the boot block recovery code (i.e. Main BIOS checksum error)
22	*-*-*	Error when getting the boot block flash ID code
33	*-*-*-*	Error when erasing the boot block flash
44	*-*-*-*-*	Error when programming the boot block flash
55	*-*	Success of the boot block recovery code. The board is ready to be manually reset.

Legend * = 1 Short beep code, ** = 1 Long beep code, - = Silence

F.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

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F.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list includes messages for both the ISA and EISA BIOS.

CMOS BATTERY HAS FAILED

1. If it's the first boot, check for the onboard battery jumper (jumper W4 for both the cPCI-MXS64). The board is shipped with W4 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.

2. CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. A weak battery may have caused this error. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-maskable Interrupt condition, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

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F.4 POST CODES

POST #	Designation	Description	
01	BOOT BLOCK	Boot Block in EMERGENCY : Clear Base Memory Area.	
03	Initialize Chips	1. Clear CMOS shutdown byte. 2. Initialize EISA extended registers. (Not for us since we don't have EISA bus.)	
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.	
05	Blank Video, Initialize Keyboard	1. Clear CMOS reset status byte. 2. Early Keyboard initialization.	Boot Block in EMERGENCY: Initialize Keyboard Controller.
06	EPROM Checksum	1. Test F000h segment shadow readable and writeable for POST access correct. If not, show POST FE and beep continuously… 2. Autodetect Flash EPROM.	
07	Test CMOS Interface and Battery Status	1. Install the Kontron segment. 2. Verifies CMOS is working correctly (walking bit test). 3. Restore CMOS from Flash if option is enabled. 4. Check for OVERRIDE KEY (INSERT key).	
08	Program Chipset default	Program Chipset default (show POST BEh).	
09	Early Cache Initialization	1. Check for Intel's and/or Cyrix CPU. 2. Early Cache Initialization when cache is separate from chipset. 3. Turn off Gate A20.	
0A	Setup Interrupt Vector Table	1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 2. Early Power Management Initialization.	
0B	Test CMOS RAM Checksum	1. Verify time and date for valid values. 2. If Override enabled, check for Override key. If Override key pressed, Kill CMOS checksum. 3. Check CMOS Battery (useless if save CMOS in FLASH enabled since it's already done). 4. Verify Checksum, if bad, load defaults. 5. Copy CMOS in the stack. 6. Clear CMOS Alarm date. 7. Clear HD if Hidden. 8. Clear Floppy "B" if only one drive. 9. Detect for a Math Co-processor. 10. Set Fast Gate A20 Flag in CMOS. 11. If "B" drive only is set the 2 Drive are set… 12. Program Chipset for early Power Management. 13. P6 Bios Update (if applicable). *14. Kill Onboard PnP IO.* *15. PnP Early Initialization.* *16. PnP System Resource:* *1. Get ESCD.* *2. Create default SYSTEM_MAP.* *3. Decode/Record ISA ESCD resources.* *4. Record I/O port for PnP operation.* 17. Chipset Early Shadow.	

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POST Codes (continued)

POST #	Designation	Description	
0C	Initialize Keyboard	1. Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary).	Boot Block 1st : Verify BIOS checksum.
		2. Disable (if necessary). Thermal Management. 3. Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0. 4. Set CD-ROM found variable to 0. 5. Initialize zone 40:0h for the keyboard buffer.	Boot Block in EMERGENCY 2nd : Init. vector 00h through 77h.
0D	Initialize Video Interface & Chipset	*1. On M1 set the cache for the memory installed.* *2. On PCI, do a PCI ROM init.* 3. On P6, Init. Apic. 4. Init. Chipset. 5. Turn ON CPU Cache. 6. Set Maximum Speed. 7. Measure CPU Clock Speed. 8. Restore Speed. 9. Turn Off CPU Cache. 10. Early Video Shadow. 11. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. 12. Init. T380 if necessary.	Boot Block in EMERGENCY: Try to init. Video Card…
0E	Test Video Memory	1. If CGA or MONO, test video memory. 2. Beep the speaker. 3. Show the LOGO. 4. Install VT100 driver if necessary. 5. Write sign-on message to screen. 6. Write Copyright message to screen. 7. Write Evaluation message to screen. 8. Show CPU type and speed.	
0F	Test DMA Controller 0	Test DMA Controller 0.	
10	Test DMA Controller 1	Test DMA Controller 1.	
11	Test DMA Page Registers	Test DMA Page Registers.	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented.	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented.	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	

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POST Codes (continued)

POST #	Designation	Description
17	Test Struck 8259's Interrupt Bits	Nothing
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.
1A-1E	Reserved	Reserved
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).
20-2F	Enable Slots 0-15	Initialize slot 0 (System Board) to slot 15.
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
31	Test Base & Extended Memory	1. Test base memory from 256K to 640K and extended memory above 1MB using various patterns. 2. The last test is filling memory with 0's. 3. On a quick memory test or if user press the ESC key while testing memory, only the last test is performed.
32	Test EISA Extended Memory	If EISA Mode flag is set, then test EISA memory found in slots Initialization. NOTE 1: This will be skipped in ISA mode. NOTE 2: This POST also Detect & Report I/O PORTS and also Init. Super IO.
33-3C	Reserved	Reserved
3C	Setup Enable	
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.
3E	Setup Cache Controller	Initialize cache controller.
3F-40	Reserved	Reserved
41	Initialize Floppy Drive & Controller	1. Verify if we should enter setup. If so, enter setup. 2. Initialize floppy disk drive controller and any drive. | Boot Block in EMERGENCY: Scan for Floppy for emergency disk…
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.
44	Reserved	Reserved
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.
46	Reserved	Reserved
47	Set Speed for Boot	Set Speed for Boot.
48-4C	Reserved	Reserved
4D	Init. PC-Speaker to LINE OUT	Enable access to PC-Speaker to LINE OUT and Enable/Disable it. (T934).

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POST Codes (continued)

POST #	Designation	Description
4E	Manufacturing POST Loop or display Messages	1. Reboot if Manufacturing POST Loop pin is set. 2. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST). 3. Enter SETUP if needed.
4F	Security Check	*Ask password security if needed.*
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.
51	Pre-Boot Enable	1. Enable Parity checker. 2. Enable NMI. 3. Enable cache before boot.
52	Initialize Option (ROM scan)	1. Call POST 81 2. Initialize any ROMs present from C8000h to DBFFFh. Disable POST code from segment E0000h. 3. Initialize any ROMs present from DC000h to E0800h. NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.
54-5F	Reserved	Reserved
60		Store boot partition of head & cylinder.
61	Final Init	*For last µs detail before boot.*
62	Num Lock ON	Put Num Lock ON and Daylight Saving.
63	Boot Attempt	1. Call POST 82. 2. Set Low stack. 3. Boot via int 19h.
64-7F	Reserved	Reserved
80	Kontron Segment Move 1	Install the Kontron segment from Flash to DC00:0h.
81	Kontron Segment Move 2	Install the Kontron segment from DC00:0h to 7000:0h.
82	Kontron Segment Move 3	Install the Kontron segment from 7000:0h to EC00:0h.
83	Check & Program CPLD	Check & Program CPLD for valid UserCode & IDCode.
84	Kontron CRC Check	Check if Kontron block have a valid CRC. If not, the Emergency procedure is launched.
85-AF	Reserved	Reserved
B0	Spurious	If interrupt occurs in protected mode.
B1	Unclaimed NMI	If unmasked NMI occurs, display: Press F1 to disable NMI, F2 reboot.
B2-BD	Reserved	Reserved
BE	Early Prog Chipset Def.	Going to early program chipset to default values (called from POST_8s).
BF	Program Chip Set	Called early at POST 0Dh to program chipset from CT-TABLE.

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POST Codes (continued)

POST #	Designation	Description	
C0	Turn ON/OFF Cache	OEM Specific - Cache control.	Boot Block: First POST.
C1	Memory presence	OEM Specific - Test to size on-board memory test.	Boot Block: Search for Boot Block Signature "*BBSS*".
C2	Early Memory Initialization	OEM Specific - Board Initialization.	
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select.	Boot Block: Expand compressed BIOS
C4	Special Display Switch Handling	OEM Specific - Display/Video switch handling so that display switch errors never occur.	
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.	Boot Block: Early Shadow System BIOS.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.	Boot Block: Cache Sizing
C7	Reserved	Reserved	
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.	
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.	
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.	
CB-CF	Reserved	Reserved	
D0	Power Management Full speed	Trying to go back or into full speed mode.	
D1	Power Management -- Doze mode	Trying to go or in Doze mode.	
D2	Power Management --Sleep mode	Trying to go or in Sleep mode.	
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.	
D4-DF	Debug	Available POST codes for use by source code customers during development.	
E0	Reserved	Reserved	
E1-EE	Setup Page	Page 1 to Page 14	
EF	Shadow Error	In POST 6 to signal a Shadow Error.	
F0-FE	Reserved	Reserved	
FF	Boot	The system is now booted or waiting for an OS.	

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G. EMERGENCY PROCEDURE

Follow this procedure only in case of emergency such as a critical error occurred during the Boot Block Flash BIOS update (when using UBIOS utility program or if you meet one of the following symptoms at anytime:

1. No POST code on a power up (when using a POST card).
2. System stops at POST 41(when using a POST card) and associated beep code is generated (Refer to Section E.1).
3. Board does not boot, even after usual hardware and connection verifications.

G.1 HOW TO RUN EMERGENCY PROCEDURE

To run an EMERGENCY PROCEDURE, proceed as follows:

1. Remove battery jumper.
2. Disable the Power Fail Detection function.
3. Connected a 1.44MB floppy drive (drive A) to the board, and insert the EMERGENCY diskette, that you previously created, in it.
4. Power on the board. (Note that no VGA is present during this procedure.)
5. Boot block flash update will be completed when the POST code 55 is displayed (when using a POST card) or the associated beep code sounds (indicated in Section E-5).
6. After the procedure is successfully completed, power down the board, install your battery and Power Fail Detection jumpers.

   The boot block flash BIOS should be correctly programmed and the system should run properly.

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G.2 GENERATE AN EMERGENCY FLOPPY DISKETTE :

Use a system that has a 1.44 Mbytes floppy drive A.

1. Insert the Kontron Emergency Diskette in drive A:
2. Copy the two files WDISK.COM and EMERDISK.TEK to your hard drive (those files are available from the driver's CDROM).
3. Insert a DOS formatted floppy diskette in drive A:.
4. At the DOS prompt of your hard drive (same path of the two files WDISK.COM and EMERDISK.TEK), type WDISK EMERDISK.TEK then press Enter key.
5. The program may display one of the following messages:

   "Emergency Code transferred"

   The emergency diskette has been successfully created. Take the appropriate actions and restart from the step 4) when you see the following messages.

   "Write to disk failure!"

   Verify if your floppy diskette is write-protected.

   "The file to program in flash was not found"

   Be sure that EMERDISK.TEK file is in your current path.

   "Unable to read the binary file" or "Unable to close the opened file"

   Possible floppy diskette corruption or bad data transfer between floppy disk and host system.

   "Unable to allocate a memory block of 256 Kbytes"

   Not enough memory to run the WDISK program.

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H. GETTING HELP

At Kontron, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products or services, you may reach us at the above numbers or by writing to :

Kontron Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

Kontron Inc, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

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Returning Defective Merchandise

If your Kontron product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:

   - The Kontron Invoice number
   - Your purchase order number
   - The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:

   - Make a copy of the request form on the following page.
   - Fill out the form and be as specific as you can about the board's problem.
   - Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.

6) When returning a Kontron board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

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kontron

RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name : _____

Company Name : _____

Street Address : _____

City : _____ Province/State: _____

Country : _____ Postal/Zip Code: _____

Phone Number : _____ Extension : _____

Fax Number : _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Kontron's Technical Support department in CanadaCanada at (450) 437-8053

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