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cPCI-DT64

6U CompactPCI® 64-bit Universal Dual Processor

Technical Reference Manual
Version 1.5, August 2005

Note: The latest releases of the Technical Reference Manuals are available at:
http://www.kontron.com or at ftp://ftp.kontron.ca/Support/

kontron
www.kontron.com

Ref. : M6006_TECH_1

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FCC COMPLIANCE STATEMENT

Warning

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

European Statement

Warning

This is a Class B product. If not installed in a properly shielded enclosure and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his own expense. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this product.

Safety Statement

UL Recognized Component, File # E186339 vol. 1 section 2

This product bears the combined UL Recognized Component Mark for Canada and U.S. It indicates investigations to the UL Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment. It is destinated to be used in end-product equipment where the acceptability of the combination is determined by Underwriters Laboratories Inc.

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READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board.**

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le manufacturier. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel.
Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Peligro de explosion si la pila se substituye incorrectamente.
Substituya solamente por el mismo o el tipo equivalente recomendado por el fabricante. Disponga de las pilas usadas segun las instruccciones.

Care and handling precautions for Lithium batteries

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

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IMPORTANT

J1 and J2 are de-facto industry standard as defined by PICMG

J3, J4 and J5 are user-defined connectors and will vary from various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

POWERING-UP THE SYSTEM

If you encounter a problem, verify the following items:

Make sure that all connectors are properly connected.

Verify your boot devices.

If the system still does not start up properly, you should try booting your system with only the video monitor connected to the board with no other I/O peripherals attached, including Compact PCI or PMC adapters.

Make sure that your system provides the minimum DC voltages required at the board's slot especially if DC power is carried out by cables.

If **you are still not able** to start up your system, please refer to the emergency procedure in the appendix section.

If you are still not able to get your board up and running, contact our technical Support department for assistance.

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

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UNPACKING AND SAFETY PRECAUTIONS

Static Electricity

Since static electricity can damage the board, the following precautions should be taken:

1. Keep the board in its antistatic package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its antistatic wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage, or items are missing, inform immediately Kontron.

When unpacking you will find:

1. 6U CompactPCI® 64-bit Universal Dual-Processor board
2. One Quick Reference sheet
3. One CDROM containing drivers.
4. Cables listed on the order

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TABLE OF CONTENTS

1. PRODUCT DESCRIPTION

1.1. Product Overview 1-1

1.2. Board Specifications 1-3

1.3. Hot Swap capability 1-9

1.4. Interfacing with the Environment 1-11

1.4.1. CPCI 1-11

1.4.2. Mezzanine 1-11

1.5. Compatibility with other KONTRON Products 1-12

1.6. Mezzanine Card Concept 1-13

1.6.1. Kontron's Mezzanine Concept 1-13

1.6.2. CompactFlash Feature 1-14

2. ON-BOARD FEATURES

2.1. IPMI - Intelligent platform Management INterface 2-1

2.1.1. IPMI Glossary 2-1

2.1.2. IPMI Implementation features 2-2

2.1.3. Firmware Update 2-2

2.1.4. IPMI KCS support in different OS 2-3

2.1.5. IPMI in a Compact PCI chassis 2-3

2.1.6. IPMI Chassis Minimum Setup 2-4

2.1.7. IPMI Sensors 2-5

2.1.8. IPMI Supported Commands 2-5

2.2. CompactFlash Interface 2-8

2.2.1. Setups 2-8

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2.3. Enhanced IDE Interfaces 2-9

2.4. Ethernet Interfaces 2-10

2.4.1. Front Plate Configuration 2-10

2.4.2. CPCI I/O Configuration 2-10

2.5. Floppy Disk Interface 2-11

2.6. PS/2 Keyboard / PS/2 Mouse Interface 2-11

2.7. Serial Ports 2-12

2.7.1. SERIAL PORT 1 2-12

2.7.1.1. Front Plate Configuration 2-12

2.7.1.2. CPCI I/O Configuration 2-12

2.7.2. Serial Port 2 2-13

2.7.2.1. RS-232 Protocol: 2-14

2.7.2.2. RS-422 Protocol: 2-14

2.7.2.3. RS-485 Protocol: 2-14

2.8. Thermal Management 2-15

2.9. USB Interfaces 2-16

2.10. Video Interface 2-16

2.10.1. Supported Resolutions 2-17

2.10.2. Major Features Description 2-17

3. INSTALLING THE BOARD

3.1. Setting Jumpers 3-1

3.1.1. Jumper Description for the CPCI-DT64 3-1

3.1.2. CPCI-DT64 – Jumper Settings & location for REV1 3-2

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3.2. Register's Description 3-3
3.2.1. Supervisor Registers 3-3
3.2.2. Register 190h: Serial port 2 configuration. 3-3
3.2.3. Register 191h: Reset History & CPU Fault 3-4
3.2.4. Register 192h: Clearing Reset History & Lock for Watchdog 3-4
3.2.5. Supervision Features 3-5
3.2.5.1. Watchdog 3-5
3.2.5.2. Dual-stage Watchdog 3-5
3.2.5.3. Power Failure Detection 3-7
3.2.6. Reset History 3-8
3.2.7. Register BITs description (summary) 3-9
3.3. On-board Interconnectivity 3-10
3.3.1. cPCI-DT64 Block Diagram 3-10
3.3.2. Pentium® III processor 3-11
3.3.3. On-board Connectors and Headers 3-11
3.3.4. Front Plate Connectors and Indicators 3-12
3.3.5. CompactPCI Connectors 3-13
3.4. Customizing the Board 3-14
3.4.1. Processor and Fan 3-14
3.4.1.1. Recommended operating and preventive maintenance: 3-14
3.4.2. Backup Battery 3-15
3.4.3. Memory 3-16
3.5. Building a CPCI System 3-17
3.5.1. Backplane 3-18
3.5.2. Rear-Panel I/O 3-19
3.5.3. Storage Devices 3-20
3.5.4. Power Supply 3-20
3.5.5. Fan Tray 3-20
3.5.6. Installing the Board into a Bay 3-20

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3.5.7. Connector Keying 3-21
3.5.8. Bus Mastering 3-21
3.5.9. Connection 3-21
3.6. CPCI I/O Signals 3-22
3.6.1. J3 Signal Specification 3-22
3.6.1.1. Ethernet 3-22
3.6.1.2. Serial Port 1 (COM 1) 3-23
3.6.1.3. Serial Port 2 (COM 2) 3-23
3.6.1.4. USB0, USB1 3-24
3.6.1.5. Keyboard 3-24
3.6.1.6. Mouse 3-24
3.6.1.7. Speaker 3-24
3.6.1.8. POST 3-24
3.6.1.9. Video 3-25
3.6.1.10. ID 3-25
3.6.1.11. Power 3-25
3.6.1.12. ID 3-25
3.6.2. J4 Signal Specification 3-26
3.6.2.1. SCSI Interface 3-26
3.6.2.2. PIM Interface 3-27
3.6.2.3. JN4 (mezzanine connector) 3-28
3.6.3. J5 Signal Specification 3-29
3.6.3.1. IDE Interface 3-29
3.6.3.2. Floppy Disk Interface 3-30
3.6.3.3. Ground and Reserved pins 3-30

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4. SOFTWARE SETUP

4.1. PHOENIX BIOS Setup Program 4-0

4.1.1. Accessing the BIOS setup program 4-0

4.1.2. The Menu Bar 4-2

4.1.2.1. The Legend Bar 4-2

4.1.2.2. The Field Help Window 4-4

4.1.2.3. The General Help Windows 4-4

4.1.2.4. Main Menu Selection 4-5

4.1.2.5. Advanced Menu Selection 4-8

4.1.2.6. Monitoring Menu Selection 4-16

4.1.2.7. Boot Menu Selection 4-23

4.1.2.8. Exit Menu Selection 4-23

4.1.2.9. Boot Utilities 4-24

4.1.2.10. POST and IPMI Leds 4-24

4.1.2.11. Phoenix Quiet Boot 4-27

4.1.2.12. Press <ESC> 4-27

4.1.2.13. Press <Del> 4-27

4.1.2.14. POST Error 4-27

4.1.2.15. Keyboard Input Request 4-31

4.1.2.16. Phoenix Multiboot 4-31

4.2. Installing Drivers 4-32

4.2.1. Video Drivers 4-32

4.2.2. Ethernet Drivers 4-32

4.2.3. Other Drivers 4-32

4.3. Console Redirection (VT100 Mode) 4-33

4.3.1. Requirements 4-33

4.3.2. Setup & Configuration 4-33

4.1.1 Running Without a Terminal 4-35

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PART FIVE – Installation and Settings

A. MEMORY & I/O MAPS A-1

A.1 Memory Mapping A-1

A.2 I/O Mapping A-2

B. INTERRUPT LINES B-1

B.1 IRQ Lines B-1

B.2 DMA Channels B-1

C. BOARD DIAGRAMS C-1

C.1 Top Devices Surface Mount C-1

C.2 Bottom Device Surface Mount C-3

C.3 Mounting Holes C-5

C.4 Top Mounting Components C-7

D. CONNECTOR PINOUTS D-1

D.1 cPCI- DT64 Connectors and Headers D-1

D.2 J1 CPCI Bus D-2

D.3 J2 CPCI Bus D-3

D.4 J3 CPCI Bus D-4

D.5 J4 CPCI Bus (PIM) D-5

D.6 J4 CPCI Bus (SCSI) D-6

D.7 J5 CPCI Bus D-7

D.8 J10, Video (VGA) D-8

D.9 J11, Serial Port 1 - RS-232 ..... D-8

D.10 J12, J13, Ethernet LAN 2 and LAN 1 ..... D-8

D.11 J14, PS/2 Mouse & Keyboard D-9

D.12 J15, Hot Swap Switch D-9

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D.13 J16, CompactFlash Disk D-9
D.14 J17 – IDE MEZZANINE D-10
D.15 SW1 – Reset Switch D-11
D.16 BT1, CMOS Battery Backup Connector D-11
D.17 JN1 – PIM (PCM64, J1) D-12
D.18 JN2 – PIM (PCM64, J2) D-13
D.19 JN3 – PIM (PCM64, J3) D-14
D.20 JN4 – PIM (PCM64, J4) D-15

E. BIOS SETUP ERROR CODES E-1

E.1 POST Beep E-1
E.2 POST Messages E-2
E.3 Error Messages E-2

F. BIOS UPDATE & EMERGENCY PROCEDURE F-1

G. GETTING HELP G-1

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PART 1

1. PRODUCT DESCRIPTION

1. PRODUCT OVERVIEW
2. BOARD SPECIFICATIONS
3. HOT SWAP CAPABILITY
4. INTERFACING WITH THE ENVIRONMENT
5. COMPATIBILITY WITH OTHER KONTRON PRODUCTS
6. MEZZANINE CARD CONCEPTS

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1.1. PRODUCT OVERVIEW

The Kontron's cPCI-DT64 is designed to accommodate the endless demands for increased bandwidth among mission-critical voice messaging, CTI and Internet/Intranet server applications.

This board is a state-of-the-art Dual CPU High Performance Serverworks-based CompactPCI 6U processor available in 4 or 8HP as a system or peripheral board. The board complements Kontron's current family of 6U CompactPCI™ processor boards offering by addressing the very high performance needs of the data / telecommunication and Computer Telephony Integration (CTI) server.

This system processor is the introductory engine for Kontron's new CPCI pinout. It also introduces a new mezzanine board for SCSI (compatible with the PMC standard) and a proprietary mezzanine for hard disk in single or dual slot. Moreover, it includes dual Gigabit Ethernet interfaces (RJ-45) as a standard feature.

The cPCI-DT64 packs new power onto a single SBC by incorporating two Intel PIII-based processors at a speed of 800MHz, 933MHz and 1.26GHz, a front side bus of 133MHz, and up to 4GB of system memory in 8HP and 2GB in 4HP. Its performance is further enhanced by a 64-bit/66MHz PCI bus design, which effectively quadruples previous PCI bandwidths.

Fully hot swappable, the cPCI-DT64 can communicates at 1Gb/s with other processor boards using CompactPCI 2.16 backplane (XL-PSB/VHDS Platform) at the physical layer.

The cPCI-DT64 offers a natural growth path to high performance, high availability as well as hot swap and scalable multiprocessing technology. It can be ordered in either front I/O (interfacing video, serial port COM1, Ethernet ports LAN0 and LAN1, PS2/Mouse, Keyboard and mezzanine slot available on the face plate) or rear I/O interfacing through CPCI I/O connectors J3, J4 and J5 (no interconnection capability on the face plate).

Options

The cPCI-DT64 can be purchased either for front plate I/O interfacing (video, serial port, Ethernet and PS2/Keyboard) or rear I/O interfacing via the CTM80-2 RTM (Rear Transition Module) through CPCI I/O connectors and backplane; in the latter, no interconnection capability is available on the front plate.

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CompactPCI Connectors

Rear I/O CPCI connectors are PICMG 2.0 Rev 3.0 compliant. CompactPCI connectors are located at the rear edge of the processor board. The complete CPCI connector configuration of the cPCI-DT64 is composed of five connectors referred to as J1, J2, J3, J4, and J5.

Their function is described below:

J1	32 bit PCI signaling, power
J2	64 bit extension, arbitration, clocks, reset and power
J3, J4, J5	Handle I/O signals.

Note : CompactPCI™ connectors are also known as 2mm Hard Metric connectors.

IMPORTANT

J1 and J2 are de-facto industry standard as defined by PICMG

J3, J4 and J5 are user-defined connectors and will vary from various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

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1.2. BOARD SPECIFICATIONS

FEATURES	DESCRIPTION
Overview	6U CompactPCI 66MHz/64-bit System or Peripheral Processor board Note: 66MHz supported through 5 slots backplane (1 System + 4 I/O)
Supported Microprocessors	4HP: Intel's 370-pins FC-PGA Single or Dual PentiumIII Low Voltage 800MHz. Single or Dual PentiumIII Low Voltage 933MHz Single PentiumIII Mobile 1.2GHz 8HP: Intel's 370-pins FC-PGA Single or Dual PentiumIII 1.26GHz.
CHIPSET	ServerWorks ServerSet III LE chipset (CNB30LE North Bridge & CSB5 South Bridge)
Bus Interface	• Front side bus at 133 MHz • Local PCI Bus at 64-bit/66 MHz (for PCI-PCI bridges and PMC slot) • CompactPCI bus up to 64-bit/66 MHz • Universal PCI-to-PCI bridge: supports up to 14 REQ/GNT for fully loaded CompactPCI system • Kontron embedded mezzanine for second PCI bus, SCSI and EIDE • Video AGP 2X SMBus (for system management of CPU temperature monitoring, DRAM control and power monitoring)
Cache Memory	• 16K/16K Instruction / Data CPU-internal Level 1 • 256KB 64-bit wide on-die Level 2 Advanced Transfer Cache
System Memory	• Four 184-pin latching DIMM sockets, PC-133 • 8HP: Up to 4GB of RSDRAM with parity or ECC (for single bit error correction and double bit error detection) • 4HP :Up to 2GB of RSDRAM with parity or ECC (for single bit error correction and double bit error detection)
Data Path	• 64-bit on CPU, • 32-bit on video memory; • 64-bit on local PCI (Ethernet, PCI Bridge and Mezzanine) • 64-bit on CompactPCI
Bridge	• 64-bit/66MHz universal PCI-PCI Bridge (PLX HB6) for CompactPCI bus driving 7 I/O slots(33MHz) or 4 I/O slots(66MHz).
Interrupts	• 8 CompactPCI interrupts, configurable to any interrupt vector for PnP compatibility

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Board Specifications (continued)

Flash Memory	• 1MB Firmware Hub for BIOS field upgrade • Silicon Serial ID TAG for unique board identification accessible via software • 4KB user serial EEPROM
Video	• 32-bit PCI video controller (Intel 69000) with 2MB video memory • CRT resolutions up to 1280 x 1024, 256 colors, 60Hz
Clock/Calendar	Real-time clock with (replaceable) battery backup, CMOS RAM
Connectors in "Front" configuration	**Front Plate** CRT — 15-pin D-Sub COM1 — 9-pin D-Sub Ethernet 1 and 2 — 2 x RJ-45 with built-in LEDs PS/2 mouse + Keyboard — 6-pin mini-DIN *Optional SCSI PMC adapter — 68-pin VHDCI
Interfaces on J3/J4/J5 **(see note below)**	**Rear CPCI I/O Connectors (J3/J4/J5)** **(Rear-panel transition module,** cTM80-2 **available separately)** CRT, Speaker I/F, SCSI, Floppy disk I/F, Serial Ports (2), Reset Switch, PS/2 Mouse & Keyboard, USB (2), Ethernet (2), EIDE **On-board Expansions** PCI Mezzanine Card PMC. Proprietary mezzanine. CompactFlash.

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Board Specifications (continued)

I/O	**Super I/O**	LSI - PC87417 super I/O
	USB Ports	Two (USB 1.1 compliant), available through Rear I/O only
	Serial Ports	Two Serial Ports: COM1: RS-232 COM2 configurable as RS-232/422/485
	Floppy Disk	Support for two drives (360KB to 1.44MB) supported only through the Rear Transition Module
	EIDE	PCI EIDE Ultra DMA/100, support for four IDE drives in a master/slave configuration, PIO Mode4, Bus Master IDE or synchronous DMA mode transfers up to 100MB/s
	CompactFlash™	Optional bootable CompactFlash™ disk interfaces to primary EIDE channel, user upgradable, master/slave.
	Ethernet	Two 10Base-T/100Base-Tx/1000Base-T Ethernet interfaces ports (Intel 82544 controller).
	HD Mezzanine Card	Optionally on-board using Kontron's cMC series mezzanine cards
	SCSI	Optional PCI-ULTRA160/320 (Ultra3) LVDS SCSI supports up to 640 MB/s dual channel or 320 MB/s single channel (Symbios/LSI)
Supervisory	• Two-stage software programmable Watchdog timer drives NMI on first stage and system reset on second stage. Time out from 16msec to 4.5min • Hardware system monitor • IPMI • Power failure detector • Low battery voltage detector • CPU temperature sensor / thermal management • Board temperature sensor • 12V, 5V, 3.3V, VBAT and Vcore voltage supervisor	

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Board Specifications (continued)

OS Compatibility	▸ **Dual CPU configuration** • Microsoft Windows 2000 family • Microsoft Windows XP • Windows NT4 family • Linux Red Hat 8.0 • FreeBSD 5 • UnixWare 7.1.1 • QNX RTP 6.2.1 ▸ **Single CPU configuration** • All above mentioned OSs, and the following: MS-DOS 6.22
Hardware Compatibility	• Upgrade path for many previous Kontron's boards (DXS64, DMXP64GX, DMXS64GX) • CPCI J3, J4 and J5 pin-outs have been changed from previous boards. **Do not use** older RTM with this board. Use only the CTM80-2 Rear transition Module.
BIOS Features	• Phoenix BIOS in Boot Block Flash with recovery code. • Save CMOS in Flash option and Boot from LAN capability. • 0-E0000 address blocking; PnP tables • Setup console redirection to serial port (VT100 mode) with CMOS setup access • Software enable/disable of on-board Ethernet; hardware enable/disable of on-board video • Diskless, keyboardless, and videoless operation extensions • Programmable I/O wait states • DMI & HDD S.M.A.R.T. support • Intelligent System Monitoring (chassis intrusion and advanced thermal management such as resume, overheat alarm and auto slow down) • Green support
Mechanical	Compliant to IEEE 1101.10, compliant to PICMG2.0 Rev 3.0 266.7 x 160 x 41 mm / 10.5 x 6.3 x 1.6 in, 6U x 8HP (dual slot) 266.7 x 160 x 20.5 mm / 10.5 x 6.3 x 0.8 in; 6U x 4HP (single slot)

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Board Specifications (continued)

Power Requirements	Single 800MHz 2Gig Mem	Dual 800MHz 2 Gig Mem	Single 933MHz 2Gig Mem	Dual; 933MHz 2Gig Mem	Single 1.2GHz 2Gig Mem	Single 1.26GHz 4Gig Mem	Dual 1.26GHz 4Gig Mem
5Volts Typical	1.2A	2.0A	1.2A	2.2A	2.4A	3.3A	5.9A
5Volts Maximum CPU intensive	1.8A	3.4A	1.8A	3.6A	3.6A	5.0A	10.0A
3.3 volts Typical	4.8A	5.0A	4.6A	4.8A	4.8A	6.1A	6.3A
3.3 volts Maximum CPU intensive	7.7A	8.0A	7.3A	6.7A	7.4A	8.7A	9.3A
+12 Volts	<100mA	<100mA	<100mA	<100mA	<100mA	<100mA	<100mA
-12 Volts	<10mA	<10mA	<10mA	<10mA	<10mA	<10mA	<10mA
- 5 volts	Not used	Not used	Not used	Not used	Not used	Not used	Not used
Typical: Measurements taken within BIOS setup.							

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Environmental		
	Operating	**Storage and Transit**
Temperature	4HP: 0-50°C / 32-104°F / with 8.08cfm 8HP: 0-50°C / 32-104°F / with 10.8cfm	-40 to +70°C / -40 to 158°F -40 to +70°C / -40 to 158°F
Humidity	5% to 95% @ 40°C/104°F non-condensing	5% to 95% @ 40°C/104°F non-condensing
Altitude	4,000m / 13,123ft Note: may require additional cooling above 1800m/5905ft	15,000m / 49,212ft
Shock	Designed to meet IEC 68-2-27	
Vibration	5 to 500Hz, 1G, each axis	5 to 50Hz, 2G; 50 to 500Hz, 3G, each axis
Reliability	MTBF: > 140 000 @ 30°C/86°F (Telcordia SR-332, Issue 1)	
	Board Silicon Serial ID	
	USB, keyboard and mouse protected by self-resetting fuse	
	Meets or exceeds : Safety: UL1950, CSA C22.2 No 950, EN 60950, IEC950 EMI/EMC USA FCC 47 CFR Part 15/CISPR22, Class B Canada ICES-003 Class B Europe CE Mark to EN55022 Class B / EN55024	
	2 year limited warranty	

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1.3. HOT SWAP CAPABILITY

The cPCI-DT64 supports Hot Swap capability which means that hot swappable boards can be removed from or installed in the system while online (without powering-down the system).

Hot Swap consists of board hardware with the Hot Swap additions to the Hardware Connection Layer, and the Hot-Plug Service. Upon insertion of the board (any hot swappable board but the system host, cPCI-DT64) the hardware connection layer will initialize the board and the Hot-Plug Service provides the means for reconfiguring the system.

High Availability is an attribute of a system designed to keep running (maintain availability) in the event of a system component failure. To provide a high degree of availability, a system requires a higher degree of control.

High Availability (HA) uses a higher degree of control than just indicating insertion and extraction. HA systems are able to control the Hardware Connection Process. To do this, the capabilities of the system are extended to allow software control of a board's hardware connection state. A hardware connection sequence is made possible through the use of different pin lengths and the process ends with the mating of the shortest pin (BD_SEL#).

The platform adds hardware to provide more control of each board's Hardware Connection Layer. The signals: BD_SEL#, HEALTHY#, and PCI_RST# are used to individually control each slot of the system.

BD_SEL# is one of the shortest pins. This pin is the last to mate and the first to break contact. This ensures that the sensing of its connection takes place at a time when all other pins are reliably connected. It is driven low to enable power on. For systems not implementing hardware connection control, it is grounded on the backplane.

HEALTHY# is used to acknowledge the health of the board. It signals that a board is suitable to be released from reset and allowed onto the PCI bus. In an HA system, the software can detect a faulty board when it fails to assert HEALTHY# after BD_SEL# has been asserted. A running board can also become not healthy at any time.

PCI_RST# as defined by the CompactPCI® Specification, is a signal on the backplane, driven by the system host. Platforms may implement this signal as a radical signal from the Hot Swap Controller to further control the electrical connection process. Platforms that do this must OR the system host's reset signal with the slot specific signal to maintain the bussed signal's function.

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The Software Connection Control resources on the board provide a signal (ENUM#) for system host notification and a switch and LED to interface with the operator.

Full Hot Swap boards drive the ENUM# signal to the system host to indicate a service request. This signal is provided to notify the system host that either a board has been freshly inserted or is about to be extracted. This signal informs the system host that the configuration of the system has changed. The system host then performs any necessary maintenance such as installing a device driver upon board insertion, or unloading drivers for hot swap boards that are about to be extracted*. The application that is using the board is also notified that the resource will no longer be available.

The Hot Swap Switch allows the operator to indicate desire to extract the board. A blue LED, located on the front of the board, is illuminated when it is safe to extract the board. This LED indicates that system software has been placed in a state for orderly extraction of the board. The hardware connection layer provides protection only for the hardware during insertions and extractions. This method allows the operator to insert or extract boards without the extra step of reconfiguring the system at the console.

WARNING

All actions are initiated by the operator, and must be performed in the correct sequence for proper system operation.

Full Hot Swap boards present the following resources to software executing on the system host (nominally implementing the Hot-Plug Service and Hot-Plug System Driver)

- An ENUM# signal, which is an open collector (open drain) bussed signal, to signal a change in status for the board.
- A switch actuated with the lower ejector handle, indicating the beginning of the extraction process or end of the insertion process.
- A LED to indicate the status of the software connection process.
- A set of four control and status bits on each board allows the system host's software to determine the source of the ENUM# signal and control the LED.

Full Hot Swap boards allow the full range of system capabilities.

* To do this operation, you need a third party hot swap driver.

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1.4. INTERFACING WITH THE ENVIRONMENT

1.4.1. CPCI

The cPCI-DT64 system processor is provided for rack-mounted systems to offer the highest modularity. Through the J1/J2 segment, the board can drive up to **seven** external CompactPCI slots, supporting individual REQ/GNT arbitration pair signals and clock.

NOTE

A. **In front I/O configuration**, the following I/Os signals are available on the faceplate: SVGA, Serial Port 1, Ethernet 1 and 2, keyboard and mouse. All other I/Os are connected to J3, J4, and J5.

B. **In Rear I/O configuration**, all I/O signals are connected to J3, J4 and J5

1.4.2. Mezzanine

The mezzanine is a hardware interface to increase the I/O connectivity of the cPCI-DT64, but respecting the dual slot 6U form factor restrictions.

The on-board mezzanine connector features IDE signals for mezzanine applications: Kontron provides a storage mezzanine with an optional hard drive.

A complete *CompactPCI platform* (XL-PSB/VHDS) is available from Kontron.

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1.5. COMPATIBILITY WITH OTHER KONTRON PRODUCTS

The cPCI-DT64 System Processor is a member of the Kontron's CompactPCI product family.

The boards are fully compliant with the PICMG 2.0 Rev.2.1 and PICMG 2.1 CompactPCI specifications.

When building a basic environment around the cPCI-DT64, the platform may be composed of any of the following devices:

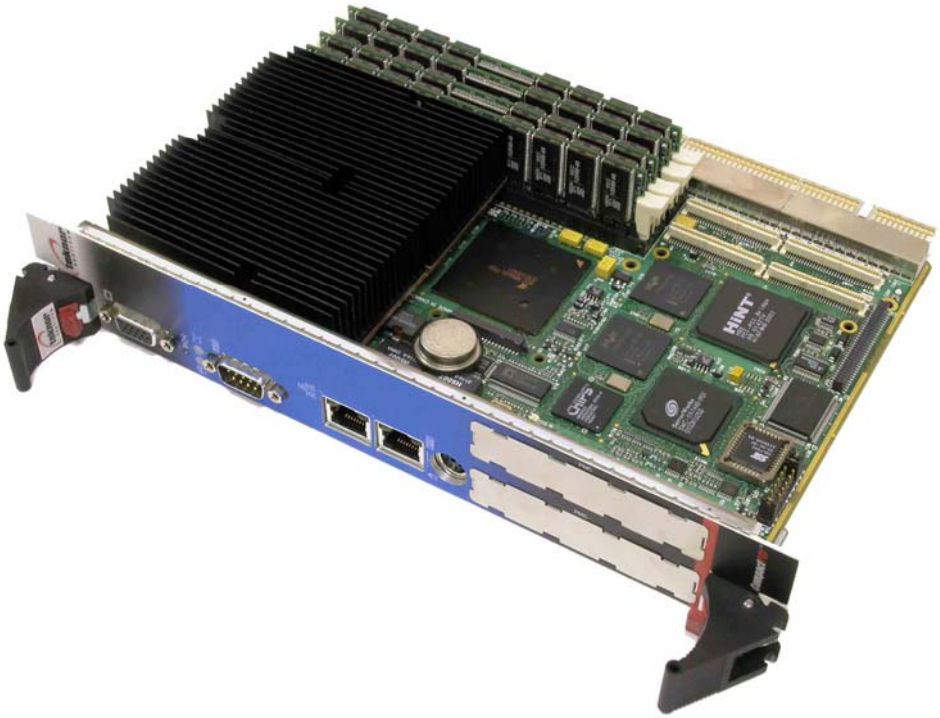
- cPCI-DT64 6U System Processor
- cSM-DVDHD Storage module with DVD and Hard Disk
- cSM-DVD Storage module with DVD only
- XL-PSB including
    - 8U 19-inch enclosure
    - Front loaded hot swappable 2U fan tray
    - Power supply (350W AC or DC in single or redundant configuration)
    - One of the following backplanes:

        XL-PSB : 16 slots CompactPCI (PICMG 2.1)
- cTM80-2 6Ux8HPx80mm Rear Transition Module, standard pinout.
- XL-CXP
- XL-VHDS
- XL-LP42

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1.6. MEZZANINE CARD CONCEPT

The capability of the cPCI-DT64 to connect with other devices is enforced by PCI Mezzanine Cards (PMC). A fully equipped cPCI-DT64 board may appear as follows:



This is Kontron's concept to expand the I/O capability of the board. It is built around two connectors:

- Mezzanine connector handling IDE signals.
- Mezzanine connector handling a complete PCI signal set (primary bus) including the REQ/GNT arbitration signal pair.

These two connectors represent an open door for future development of expansion and I/O mezzanine cards.

The current limits for the PMC card are as follows:
max 3A @ 5V
max 3A @ 3.3V
max 0.75A @ 12V
max 0.75A @ -12V

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1.6.2. CompactFlash Feature

The cPCI-DT64 board also supports standard CompactFlash disk through a CompactFlash module.

CompactFlash disk is a method of storing and transferring data. It is supported on the board as a standard IDE drive and connects to the primary EIDE interface.

The CompactFlash drive can be set as a Master or Slave device and combined with any standard hard disk drive by setting the jumper W6 (see Section 3.1, setting jumpers).

CompactFlash is installed on J16 connector. For more information on CompactFlash installation and setups, please refer to Section 2.2 – *CompactFlash Interface*.

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PART 2

2. ON-BOARD FEATURES

1. IPMI - INTELLIGENT PLATFORM MANAGEMENT INTERFACE
2. COMPACTFLASH INTERFACE
3. ENHANCED IDE INTERFACES
4. ETHERNET INTERFACES
5. FLOPPY DISK INTERFACE
6. PS/2 KEYBOARD AND MOUSE INTERFACE
7. SERIAL PORTS
8. THERMAL MANAGEMENT
9. USB INTERFACES
10. VIDEO INTERFACES

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2.1. IPMI - INTELLIGENT PLATFORM MANAGEMENT INTERFACE

The board is equipped with a stand-alone micro-controller running IPMI-compliant firmware. IPMI is a standard that defines how users can monitor system hardware and sensors, control system components and log important system events. It is an open-standard hardware manageability interface specification. IPMI is also the basic building block that allows building a broad range of Service Availability functions. More information can be found on Intel Web site at

http://www.intel.com/design/servers/ipmi/ or
http://www.intel.com/platforms/applied/eiacomm/papers/25133701.pdf

IPMI specification can be found on Intel Web Site at

http://www.intel.com/design/servers/ipmi/spec.htm

2.1.1. IPMI Glossary

IPMI:	Intelligent Platform Management Interface
BMC :	Baseboard Management Controller
SEL:	System Event Log
SDR:	Sensor Data Record
SDRR:	Sensor Data Record Repository
IPMB:	Intelligent Platform Management Bus
KCS:	Keyboard Controller Style
FRU:	Field Replaceable Units
SMS:	System Management Software

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2.1.2. IPMI Implementation features

- Compliant to IPMI specification 1.5
- Can be configured as BMC or Satellite by software (BIOS Setup Menu)
- Firmware designed for and tailored to CompactPCI implementation
- Compliant to PICMG 2.9 specification
- KCS SMS interface with interrupt support
- Dual Port IPMB configurable as 2 independent channels or in redundant mode (BIOS Setup Menu)
- Out of band management and monitoring using IPMB interface allows access to sensors regardless of SBC state.
- Sensor threshold fully configurable
- Complete IPMI Watchdog functionality
- Complete SEL, SDR repository and FRU functionality
- Master Read/Write I2C support for external I2C devices communications (FRU, EEPROM, FAN, etc..)
- Firmware fully upgradeable
- Firmware can be fully customized to customers requirements.
- Interoperable with other vendors IPMI solutions (validated with Intel's IPMI implementation)

2.1.3. Firmware Update

A DOS IPMI tool package is available from Kontron and includes a utility name "ipmifwu" (IPMI firmware update). This utility allows the reprogramming of a binary in the firmware. See the 'ipmifwu' usage display for complete utility options (by running 'ipmifwu –h'. Refer to Kontron Web site for package and firmware availability or contact Kontron Technical Support. **Note that some firmware releases might not be compatible with some BIOS versions. Always upgrade both BIOS and firmware as recommended**.

Here is the standard procedure and command to upgrade the IPMI firmware

i. Boot DOS

ii. Place both firmware binary and utility 'ipmifwu.exe' on a floppy

iii. Insert the floppy and run the following:

'ipmifwu –f firmware.bin –p –r'

This action will program the firmware(-p) with file firmware.bin (-f)

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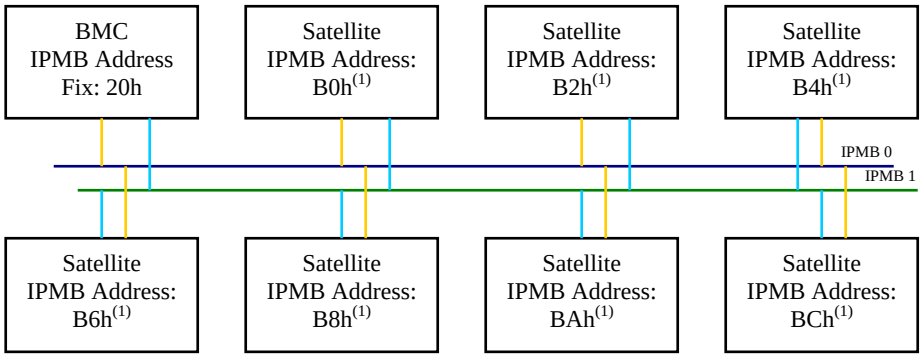
2.1.4. IPMI KCS support in different OS

LINUX: An open source KCS driver is available for Linux at http://openipmi.sourceforge.net. This driver includes all the necessary functionality (and more) to communicate with the firmware.

Intel provides some Linux KCS reference drivers available at the following address: http://www.intel.com/design/servers/ipmi/ipmi_driver.htm

WINDOWS: Intel provide some Windows KCS reference drivers available at the following address: http://www.intel.com/design/servers/ipmi/ipmi_driver.htm

2.1.5. IPMI in a Compact PCI chassis



(1) IPMB address for satellite is determined via the location of the slot in the chassis

BMC

In a CompactPCI system, there can only be 1 BMC present at a time. The BMC includes the SEL and the SDRR for the complete system. The BMC is connected to the other blades in the system via the dual port IPMB interface. The board's firmware can be set to BMC by selecting the option in the BIOS Setup Menu.

Satellite

In a Compact PCI system, there can be many satellites. Each satellite is connected to the other blades via the dual port IPMB interface. The board firmware can be set to Satellite mode by selecting the option in the BIOS menu.

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SEL

The SEL repository is only present in the BMC. If an event occurs on any blade or other IPMI-enabled device, the sensor event is sent through the IPMB bus (if SEL is not local) and stored in the BMC SEL repository.

SDRR

The SDRR is only present in the BMC. Normally, the SDRR contains all the sensor record for the complete system. A utility is provided in the IPMI DOS tool package named 'fillsf.exe' to make a full system discovery and configure the SDRR with the found sensors records. Factory configured boards will contain all the local sensors in the SDRR.

FRU

A FRU is available in BMC or Satellite mode. The FRU contains product informations such as Part Number and Serial Number. Refer to the PICMG specification 2.9 for more details on the FRU byte structure. Fillsf.exe can be used to update the FRU.

2.1.6. IPMI Chassis Minimum Setup

A minimal chassis configuration on a system may be the following:

- Elect a BMC by setting the firmware mode to BMC in the BIOS Setup Menu. By default, all the blades are shipped in satellite mode.
- Configure the SDRR with all the present sensors in the system. This step may be done using the fillsf.exe utility. The SDRR must be rebuilt everytime there is a configuration change in the system.
- Probe the BMC SEL for event or any other available information using the SMS of your choice or by sending commands directly using the available tools.

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2.1.7. IPMI Sensors

The IPMI firmware include the following category of sensors:

- Temperatures (CPU, board)
- Currents (5V, 12V, 3.3V, etc..)
- Voltages (5V, 12V, 3.3V, etc..)
- Board Ejector
- IPMB Line Stuck (PICMG 2.9 required sensor)
- IPMB1 Alert (PICMG 2.9 required sensor)
- LANs Link
- Reset Source
- PCI Error Source (P64SERR, P32SERR, etc..)
- Power Source
- Chipset Source
- Board Select
- SMI, NMI
- Init Agent Error Source

2.1.8. IPMI Supported Commands

The IPMI firmware supports the following commands from the KCS and IPMB interfaces. Please refer to the IPMI specification for further details about each command.

Global Commands

Get Device ID
Cold Reset
Get Self Test Results
Broadcast “Get Device ID”

SEL Device Commands

Get SEL Info
Get SEL Allocation Info

Event Commands

Set Event Receiver
Get Event Receiver
Platform Event

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SEL Device Commands

- Get SEL Info
- Get SEL Allocation Info
- Reserve SEL
- Get SEL Entry
- Add SEL Entry
- Delete SEL Entry
- Clear SEL
- Get SEL Time
- Set SEL Time

Sensor Device

- Get Device SDR Info
- Get Device SDR
- Reserve Device SDR Repository
- Set Sensor Hysteresis
- Get Sensor Hysteresis
- Set Sensor Threshold
- Get Sensor Threshold
- Set Sensor Event Enable
- Get Sensor Event Enable
- Get Sensor Reading

BMC-System Interface

- Set BMC Global Enables
- Get BMC Global Enables
- Clear Message Flags
- Get Message Flags
- Enable Message Channel Receive
- Get Message
- Send Message
- Read Event Message Buffer
- Get BT Interface Capabilities
- Master Write-Read I2C

SDR Repository Device

- Get SDR Repository Info
- Get SDR Repository Allocation Info
- Reserve SDR Repository
- Get SDR
- Add SDR
- Partial Add SDR
- Delete SDR
- Clear SDR Repository
- Run Initialization Agent

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BMC Watchdog Timer

Reset Watchdog Timer
Set Watchdog Timer
Get Watchdog Timer

OEM Command

Get Init Agent Last Error

FRU Inventory Device

Get FRU Inventory Area Info
Read FRU Inventory Data
Write FRU Inventory Data

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2.2. COMPACTFLASH INTERFACE

The board supports an IDE compatible flash disk by using a CompactFlash module. CompactFlash (C-Flash) disks are the resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power.

The CompactFlash disk connects on the cPCI-DT64 via the on-board Flash Disk connector.

Related Jumpers

W6 to set the CompactFlash disk as master or slave.

BIOS Settings

Section 4.1.2.4 Main Menu Selection: Hard Disk autodetection to set the type of hard disk.

2.2.1. Setups

The CompactFlash disk connects directly on the primary EIDE interface. It must be declared the same way as a standard hard disk using the BIOS setup program (Autodetect function).

To setup the CompactFlash disk for Master or Slave configuration, use the CompactFlash jumper located on the system processor.

To locate and install this jumper, please refer to Section 3.1, *Setting Jumpers*.

NOTE

Since device use ATA/IDE interface, no specific flash disk driver is required for various operating systems.

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2.3. ENHANCED IDE INTERFACES

The board features two channel Bus Master PCI EIDE dedicated to Primary and Secondary IDE logical interfaces. Each channel supports up to two IDE devices (including CD-ROMs, hard disks, plus CompactFlash on the primary IDE interface) with independent timings, in Master/Slave combination.

Signal Paths

The primary IDE interface is only available through the mezzanine connector and the CompactFlash connector.

The secondary IDE interface is only available through the CPCI I/O connector.

Related Jumpers

None

BIOS Settings

Section 4.1.2.5 , Advanced Menu Selection

The IDE interfaces supports PIO mode 4 transfers up to 16.6MB/sec and Bus Master IDE transfer up to 66MB/sec (Ultra-DMA/100).



CAUTION

Two Master devices (or two Slave devices) must not be installed on the same interface at the same time.

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2.4. ETHERNET INTERFACES

Both Ethernet controllers reside on the Primary PCI bus.

Each interface supports 10Base-T/100Base-TX/1000Base-T Ethernet specifications: 10Mbps, 100Mbps and 1000Mbps network speeds are automatically detected and switched.

Related Jumpers
None.

BIOS Settings
Section 4 Advanced Menu, On-board Ethernet Controller.

2.4.1. Front Plate Configuration

Ethernet 1 and 2 signals are available on front plate connectors (J13 and J12) only when the board is ordered for front access.

Activity and link indicators are built in the connector.

2.4.2. CPCI I/O Configuration

CAUTION

The combination of both front and rear panel configurations is not supported.

The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program. Please refer to Section 4.1 PHOENIX BIOS Setup Program.

The Network Drivers for the Intel 82544 Ethernet controller are available from Kontron WEB site and FTP site at ftp://ftp.kontron.ca/Support , (see Support section).

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2.5. FLOPPY DISK INTERFACE

The on-board floppy disk controller is IBM PC XT/AT compatible. It handles 3.5", low and high density disks. Up to two drives can be supported in any combination.

Signal Paths

The Floppy Disk Controller interface is available through the CPCI I/O connector.

Related Jumpers

None.

BIOS Settings

Section 4.1.1, Main Menu, Legacy Diskette A and Legacy Diskette B.

Section 4.1.2.5, Advanced Menu Selection, I/O Device Configuration, Floppy Disk Controller and Base I/O address.

2.6. PS/2 KEYBOARD / PS/2 MOUSE INTERFACE

The on-board keyboard controller is 8042 software compatible. PS/2 Keyboard and mouse signals are available through an output that supports direct connection to the interface. Since signals of both devices are combined on the same connector, a Y-cable is required to split the signals and feed a standard AT keyboard and a PS/2 mouse.

Signal Path

PS/2 keyboard and PS/2 mouse signals are available through J5 CPCI I/O connector. and J14 faceplate connector.

Related Jumpers

None.

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2.7. SERIAL PORTS

Two full function serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbps.

Each serial port is specified as follows:

Designation	Communication Mode	Output Path
Serial Port 1 (COM 1)	RS-232	Front Plate DB-9 (J11), CPCI J3
Serial Port 2 (COM2)	RS-232/RS422/RS485	CPCI J3

UART registers are individually addressable and fully programmable.

2.7.1. SERIAL PORT 1

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as Serial Port 1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

Signal Path

Serial Port 1 signal path depends on the output configuration you have ordered for the board

Related Jumpers

None

BIOS Settings

Section 4.1.2.5, Advanced Menu Selection, On-board Device Configuration, Serial Port 1.

2.7.1.1. Front Plate Configuration

The Serial Port 1 signals are available through a DB-9 connector located on the front plate (J11)

2.7.1.2. CPCI I/O Configuration

The complete signal set is tied to the J3 CPCI I/O connector to be used through the Rear Transition Module (RTM).

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2.7.2. Serial Port 2

Serial Port 2 is buffered directly for RS-232 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

The Serial Port 2 is 100% compatible with the IBM-AT serial port.

Signal Path
Serial Port 2 signals are only available through the J3 CPCI I/O connector

Related Jumpers
W7 & W8

BIOS Settings

Section 4.1.2.5, Advanced Menu Selection, On-board Device Configuration, Serial Port 2.

Upon a power-up or reset, the Serial Port 2 interface circuits are automatically configured for the operation mode setup in the BIOS. The Serial Port 2 signal assignation on the J3 CPCI I/O connector depends on the operation mode (RS-232, RS-422, or RS-485) it has been set:

J3 Connector		RS-232	RS-422	RS-485
Pin#	Name			
D3	SP1:DCD	DCD	DCD	DCD
B3	SP1:RX#	RXD	RX(-)	RX/TX(-)
C3	SP1:DSR	DSR	DSR	DSR
D4	SP1:DX#	TXD	TX(-)	-
A3	SP1:RTS	RTS	RX(+)	RX/TX(+)
C4	SP1:CTS	CTS	TX(+)	-
A4	SP1:RI	RI	RI	RI
B4	SP1:DTR	DTR	DTR	DTR

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2.7.2.1. RS-232 Protocol:

When configured for RS-232 operation mode, the Serial Port 2 is 100% compatible with the IBM-AT serial port signals.

2.7.2.2. RS-422 Protocol:

The RS-422 protocol (Full Duplex) uses both RX and TX lines during a communication session.

> **CAUTION**
>
> In RS-422 mode, W7 and W8 jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 *Jumper Settings*)

2.7.2.3. RS-485 Protocol:

The RS-485 protocol (Half Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires, and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.

In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal is used to control the direction of the RS-485 buffer.

When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

> **CAUTION**
>
> When installing the cPCI-DT64 at one end of the network, W7 and W8 jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 – *Setting Jumpers*).

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2.8. THERMAL MANAGEMENT

The processor module includes a user-defined temperature sensor / alarm function, which provides thermal monitoring of the processor.

Two temperature sensors are provided to supervise the thermal environment. One is used to monitor the CPU die temperature, while the second one, located on the CPU casing, allows the monitoring of the ambient temperature around the CPU.

The temperature is controlled according to two temperature levels, the Low Temperature Limit, which indicates normal operating conditions, and the High Temperature Limit, which indicates an overheating condition.

The temperature management consists in reducing the CPU clock speed throttling when the temperature goes over the high limit (overheating condition) and suspending the throttling operation as soon as the temperature returns under the low temperature limit (normal condition).

The clock speed may be throttled by a CPU overheating due to a fan failure. In such a case, the temperature control is triggered as soon as the temperature reaches the high temperature limit of the die.

The ambient temperature of the CPU generally raises up due to an augmentation of the temperature in the casing. In that case, the clock speed will be slowed down as soon as the ambient temperature reaches the high ambient temperature value.

Thermal management operations are controlled by the chipset, and settings are provided through the BIOS setup program interface (see section 4.1.2.6 PHOENIX BIOS *Setup Program, Monitoring Menu Selection, and Hardware Monitor Controls).*

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2.9. USB INTERFACES

The USB strengths are as follows: capability to daisy chain as many as 127 devices per interface, fast bi-directional, isochronous/asynchronous interface, 12Mbps transfer rate, and standardization of peripheral interfaces into a single format.

Signal Paths
Both USB 0 and USB 1 interface signals are available through the CPCI I/O connector (J3).

Related Jumpers
None

BIOS Settings
Advanced : Legacy USB Support (keyboard and mouse)

USB supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

The cPCI-DT64 board fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible.

2.10. VIDEO INTERFACE

The high-performance video capability of the board is based on Accelerated Graphics Port (AGP) technology. The video controller, Intel 69000, with its integrated 2Meg of high performance SDRAM is capable of CRT resolutions up to 1280 x 1024 x 256 colors (1MB RAM).

The video interface features 64-bit 2D graphics engine, 64-bit GUI accelerator engine with multiple window video acceleration.

Signal Path
In front I/O configuration : J10 on the faceplate
In Rear I/O configuration : J3 CPCI connector

Related Jumpers
W4 to enable or disable on-board VGA feature.
See section 3.1 – *Jumper Settings*

BIOS Settings
Advanced PCI, Default Primary Video Adapter.; Advanced Chipset Control: Graphic Aperture.

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- **Front Plate Configuration**
  VGA interface signals are available on J10, standard VGA connector, located on the faceplate, only when the board is ordered for front access operations. This configuration allows direct connection of CRT display onto the board.

- **CPCI I/O Configuration**
  VGA interface signals are available on J3 CPCI I/O connector only when the board is ordered for rear panel output operations.

2.10.1. Supported Resolutions

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of colors specification are listed below:

Resolution	Number of Colors
1280x1024	256 (8 bits)
640x480, 800x600, 1024x768, 1280x1024	256 (8 bits)
640x480, 800x600, 1024x768	65,536 (16 bits)
640x480, 800x600	16.8 million (24 bits)
640x480, 800x600	16.8 million (32 bits)

2.10.2. Major Features Description

- **VGA Compatibility**

  The video controller includes all registers and data paths required for VGA controller and supports extensions to VGA, including resolutions up to 800x600x16.8 million colors non-interlaced. The 16-bit images are displayed at up to 1024x768 resolution.

- **2D Graphics Engine**

  The 2D graphics engine is an advanced 32-bit three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

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PART 3

3. INSTALLING THE BOARD

1. SETTING JUMPERS
2. REGISTER'S DESCRIPTION
3. ON-BOARD INTERCONNECTIVITY
4. CUSTOMIZING THE BOARD
5. BUILDING A CPCI SYSTEM
6. CPCI I/O SIGNALS

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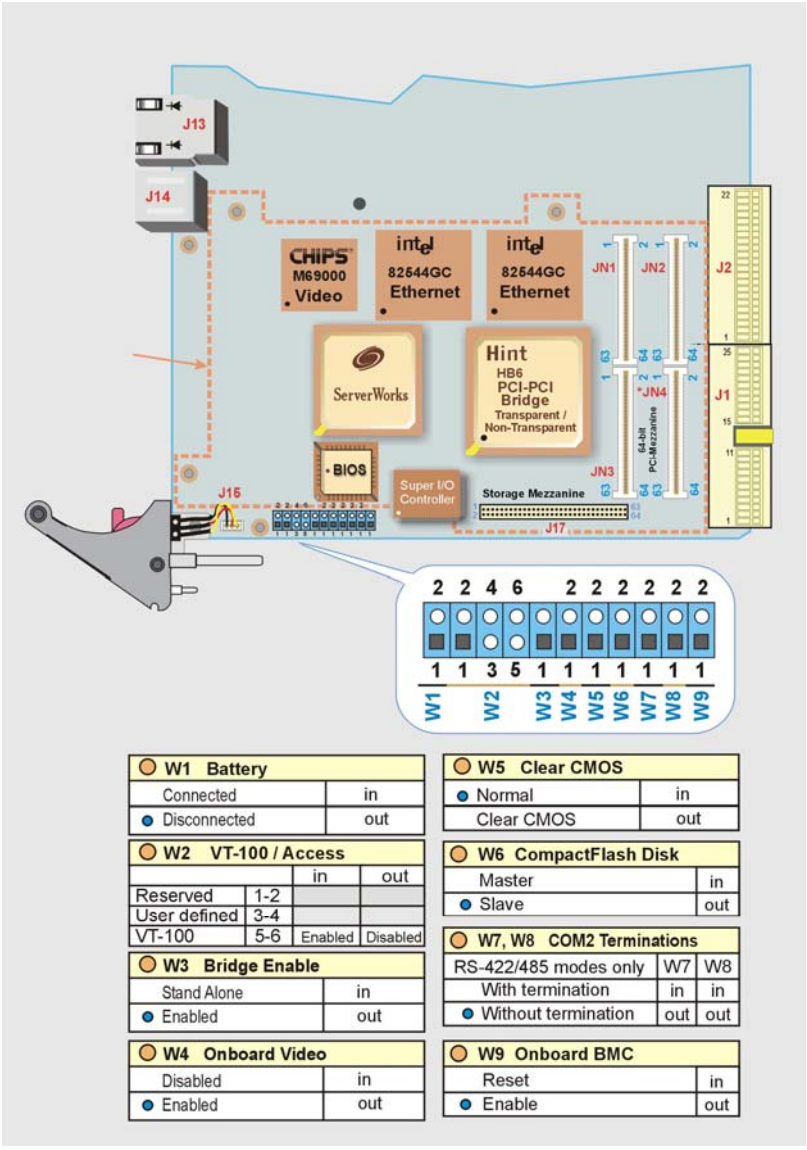
3.1. SETTING JUMPERS

3.1.1. Jumper Description for the cPCI-DT64

Description			
On-board Battery	Connects or Disconnects the battery to/from the board circuitry.		**W1**
Reserved	This jumper is reserved	**1-2**	**W2**
User defined	This jumper is defined by the user	**3-4**	
VT-100 Access	When enabled, allows VT100 or ANSI terminal connection (data serial download from a remote computer).	**5-6**	
Bridge	Enables or disables the bridge		**W3**
On-board Video	Use this jumper to disable the on-board video feature.		**W4**
Clear CMOS	When the jumper is out, all CMOS information is cleared		**W5**
CompactFlash Setting	Use this connector to setup the CompactFlash device in Master or Slave configuration.		**W6**
Serial Port 2 Termination	Use these jumpers to connect or disconnect the termination resistors on/from Serial Port 2 when set for RS-422/RS-485 operation mode 0.		**W7** **W8**
On-board BMC	Enables or disables the BMC Controller		**W9**

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3.1.2. cPCI-DT64 – Jumper Settings & location for REV1



W1 Battery	
Connected	in
● Disconnected	out

W2 VT-100 / Access			
		in	out
Reserved	1-2		
User defined	3-4		
VT-100	5-6	Enabled	Disabled

W3 Bridge Enable	
Stand Alone	in
● Enabled	out

W4 Onboard Video	
Disabled	in
● Enabled	out

W5 Clear CMOS	
● Normal	in
Clear CMOS	out

W6 CompactFlash Disk	
Master	in
● Slave	out

W7, W8 COM2 Terminations		
RS-422/485 modes only	W7	W8
With termination	in	in
● Without termination	out	out

W9 Onboard BMC	
Reset	in
● Enable	out

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3.2. REGISTER'S DESCRIPTION

3.2.1. Supervisor Registers

The Supervisor Registers consist of eight I/O registers that are used to configure and control the special features of the board, the Programmable Watchdog and the Power Fail Detection.

These registers are 8-bit wide and can be located at three different I/O base addresses: x90h.

This section includes a description of each I/O register and bit available for programming and configuring the CPCI-DT64.

3.2.2. Register x90h: Serial port 2 configuration.

Bit	7	6	5	4	3	2	1	0
Reset				0	0	0		
Read				RS485	RS232	ST1		
Write				RS485	RS232	ST1		

Used by the BIOS, only during the POST.

Serial port 2 configuration/use

ST1 — Enable RTS2 to be used as 485TX enable when in 485 mode (1: enable, 0: disable).

RS232 — Enable RS-232 mode for serial port 2 (1: enable, 0: disable).

RS485 — Enable RS-422/RS-485 mode for serial port 2 (1: enable, 0: disable).

NOTE

The RS232 and RS485 bits are initialized by the BIOS during POST (Power-On Self Test). If a modification of these bits is required, be aware that there is a hardware protection so that RS232 and RS485 buffers cannot be activated at the same time. This protection is provided at the register level. If you write to x90h register with bits 3 and 4 set, you will actually write 0 in both of these bits. This condition can be read back.

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3.2.3. Register x91h: Reset History & CPU Fault

Bit	7	6	5	4	3	2	1	0
Reset								
Read	PBRES		WDO					
Write								

Used by the BIOS at runtime; do not write to this register.

Reset history

PBRES — This bit is set when the reset button is pressed. It is cleared at power-up and when the bit CLRHIS* is "0" (see register x92h description).

WDO — This bit is set when the watchdog produces a reset. It is cleared at power-up and when the bit CLRHIS* is "0" (see register x92h description).

* = Active low signal

3.2.4. Register x92h: Clearing Reset History & Lock for Watchdog

Bit	7	6	5	4	3	2	1	0
Reset						1		1
Read						LOCK		CLRHIS*
Write						LOCK		CLRHIS*

Not used by the BIOS.

Reset history

CLRHIS* — A 0-1 pulse will clear all reset history bits (refer to the x91h register described previously). In normal operation, always keep the CLRHIS* bit to "1" otherwise the reset source will not be captured (the history latch are disabled when CLRHIS* is "0").

Programmable watchdog

LOCK — When set, the state of the enable bit for the programmable watchdog (WDEN) cannot be changed.

* = Active low signal

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3.2.5. Supervision Features

3.2.5.1. Watchdog

The function of the watchdog feature is to reset the CPU board when the NMI handler is unable to generate a trigger for longer than the watchdog timeout period. This feature is useful in embedded systems where human supervision is not required or impossible.

The CPCI-DT64 provides a two-stage digital watchdog with a software programmable timeout period.

The watchdog can be enabled by software.

3.2.5.2. Dual-stage Watchdog

3.2.5.2.1. Enabling the Programmable Watchdog

To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register x92h, then set the bit WDEN in register x96h and re-lock it by setting the lock bit in register x92h. The following is an example in C language.

```
#define TekReg 0x190            // define base address (0x190, 0x290 or 0x390)

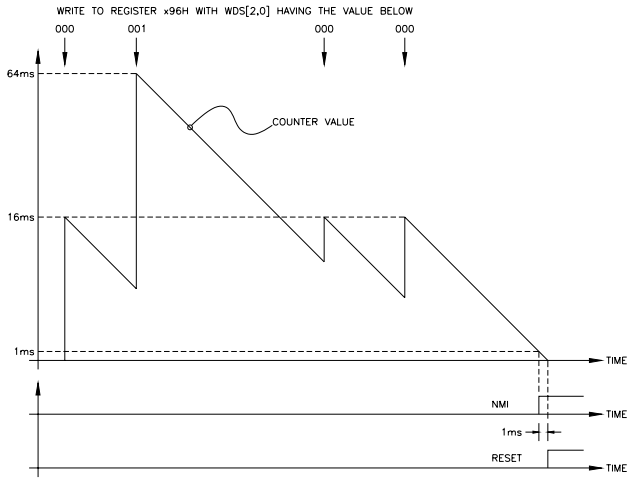
void ArmWatchdog(void)
{
   outp(TekReg+2,inp(TekReg+2) & 0xFB);  // unlock watchdog enable bit
   outp(TekReg+6,inp(TekReg+6) | 0xF0);  // enable & trigger at max timeout
   outp(TekReg+2,inp(TekReg+2) | 0x04);  // lock watchdog enable bit
}
```

3.2.5.2.2. Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register x96h. The result of writing to the register is the trigger and the value written to the register telling the watchdog the current timeout to use (see register x96h description). For a fixed timeout, the processor simply writes a constant in register x96h.

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A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register x96h. The processor must initialize the counter to prevent it from reaching count 0 (timeout).

The following C language function can be used to trigger the programmable watchdog.

```
#define TekReg 0x190              // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout)        // select timeout at runtime: 0x80, 0x90, 0xA0, ... 0xF0
{
   outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

3.2.5.2.3. Timeout

The programmable watchdog has two stages: the first stage has a variable timeout while the second stage has a fixed one.

The first stage timeout is chosen at runtime from eight preset values (see table below). The first stage timeout generates an NMI interrupt (if enabled in register x97h). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler (see register x97h description for a suggestion on how to do this).

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The second stage times-out 1ms after the first one and generates a master reset.

WDS[2,0]	NMI Timeout	RESET Timeout
000	15ms	0.015s + 8.06ms
001	62.5ms	0.0625s + 8.06ms
010	250ms	0.250s + 8.06ms
011	1s	1s+ 8.06ms
100	4s	4s + 8.06ms
101	16s	16s + 8.06ms
110	64s	64s + 8.06ms
111	256s	256 + 8.06ms

When the NMI is enabled, if the processor is still running and memory content is not corrupted, the processor can answer the NMI and trigger the watchdog again to gain time for a graceful shutdown.

A reset from the programmable watchdog is latched for reset source identification; refer to the x92h register description in Section 3.2.4.

3.2.5.3. Power Failure Detection

The board has many power failure detection features (* = active low signal):

It always monitors the +12V, +5V, +3.3V, +2.5V and V_{CORE} power supply voltages. When one of these voltages drops below a typical threshold value, the system is reset.

It can monitor the on-board battery. Jumper W1 must be shorted to connect the on-board battery. When the battery is in a low condition (below 2.9V typical), the BatFlt bit at I/O address x97h, will read 1 (x97h, bit 6: 1 = failed, 0 = good). To generate an NMI (non-maskable interrupt) when the battery fails, the BatFltEn bit must contain a 1 (x97h, bit 7: 1 = enable NMI, 0 = disable NMI). The interrupt can then be serviced by an interrupt handler. If you choose not to generate an NMI, you can still use an algorithm to detect a low battery condition at x97h, bit 6, and respond accordingly.

It can monitor an offboard 3.6V battery. Jumper W1 must be shorted to connect the offboard battery.

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3.2.6. Reset History

Following a reset, the application software can read the register x91h and examine the bits PBRES and WDO. Based on the values of those bits, the following conclusions can be drawn about the reset source.

PBRES	WDO	RESET Source
0	0	Power-up, Ctrl-Alt-Del or software runaway
1	0	Reset switch or remote reset
0	1	Programmable watchdog
1	1	Watchdog and a reset switch.

For proper operation, the bit CLRHIS* of register x92h should be pulsed (0-1) immediately after reading the history bits.

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3.2.7. Register BITs description (summary)

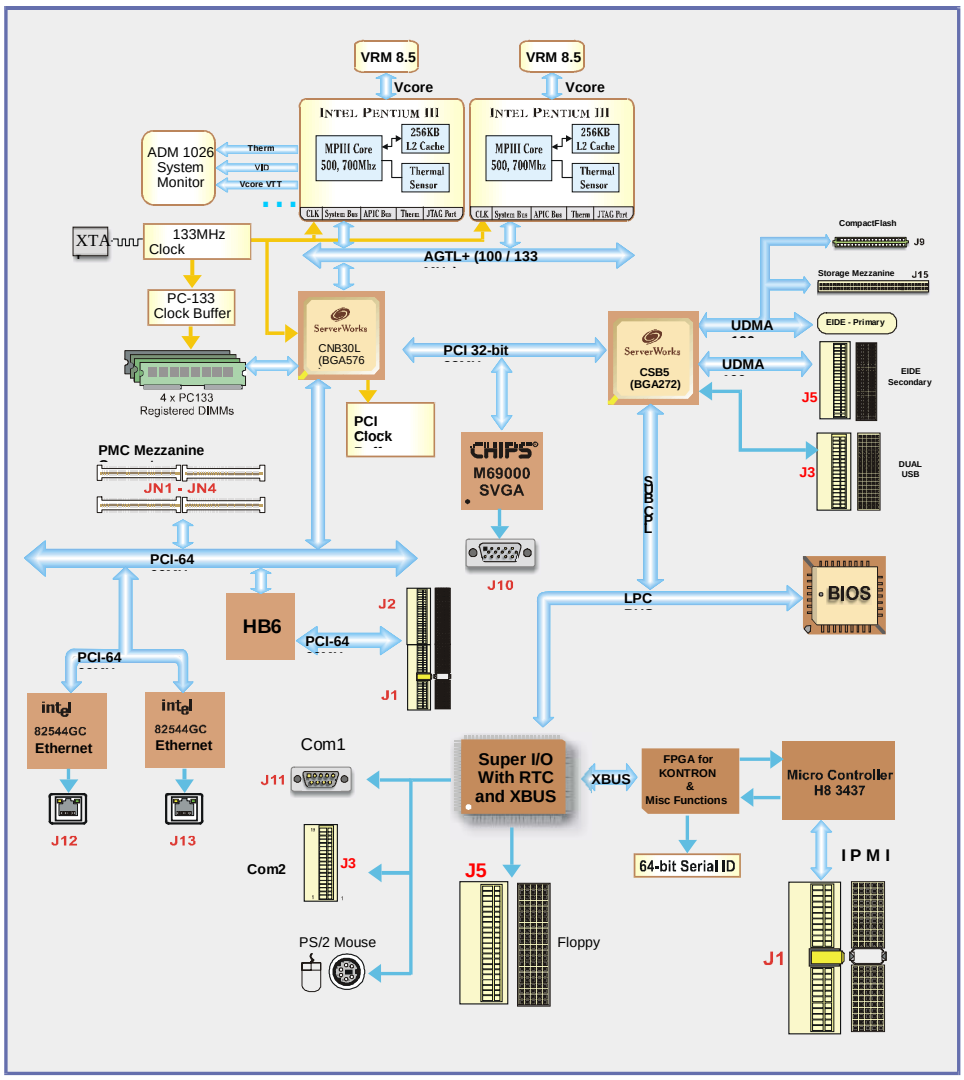
Address	CPLD	D7	D6	D5	D4	D3	D2	D1	D0
190*	READ	NU			RS485	RS232	ST1	NU	
	WRITE								
191*	READ	PBRST	NU	WDO	NU				PFO
	WRITE	NU		NU					NU
192*	READ	NU					WD_LOCK	NU	_CLRHIS
	WRITE								
193*	READ	NU				IDCHIP	NU	I2C_CLK	I2C_DATA
	WRITE								
194*	READ	_CND3	CIS3_1	CIS3_0	CBAS3_1	CBAS3_0	RESERVED		
	WRITE								
195*	READ	_CND4	CIS4_1	CIS4_0	CBAS4_1	CBAS4_0	NU		RESERV.
	WRITE								NU
196*	READ	WDEN	WDD2	WDD1	WDD0	NU			
	WRITE								
197*	READ	BATFEN	BATFLT	NU				WDNMIEN	WDNMI
	WRITE		NU						NU
198*	READ	RESERVED							
	WRITE								
199*	READ	RESERVED							
	WRITE								
19A*	READ	NU	RESERVED						
	WRITE		NU						
19B*	READ	NU			RESERVED				
	WRITE				NU				

The base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer can be set to 190h, 290h, and 390h (see *Chipset Features Setup*).

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3.3. ON-BOARD INTERCONNECTIVITY

3.3.1. cPCI-DT64 Block Diagram



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3.3.2. Pentium® III processor

The cPCI-DT64 system board supports the Intel's 800MHz, 933MHz and 1.26GHz Pentium III processor & Tualatin (Higher clock speeds will be available when Intel will release the corresponding parts).

It consists of a Pentium® III processor core with an integrated second level cache of 256KB (on-die, full CPU speed, ECC capable) and a 64-bit high performance 133MHz front side bus

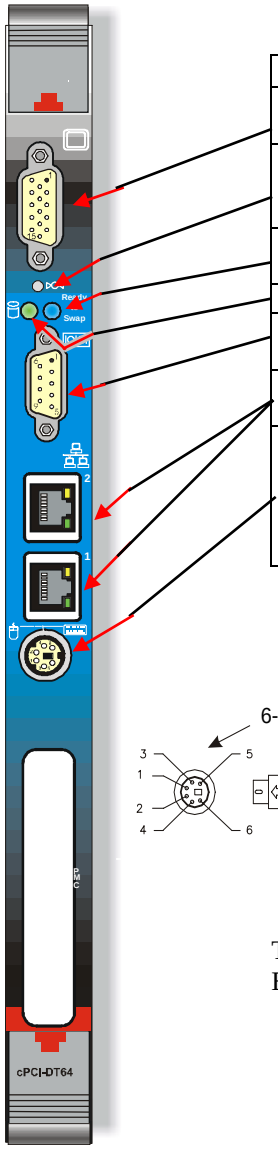
3.3.3. On-board Connectors and Headers

Description	Connector	Comments
CompactPCI Bus	J1/J2	J1- CPCI bus signals and power J2- 64 bit extension, arbitration, clocks, reset and power.
CompactPCI I/O	J3	Serial Ports 1 and 2, LAN 0 and 1, PS/2 Keyboard and Mouse, VGA and USB
CompactPCI I/O	J4 (SCSI)	SCSI (SCSI board version)
CompactPCI I/O	J4 (PIM)	Mezzanine signals (PIM board version)
CompactPCI I/O	J5	Legacy connections (IDE and FLOPPY)
Memory Socket	J6-J8	Memory Sockets
VGA	J10	Supports standard 15-pin DSUB female connector
Serial Port 1	J11	Supports standard 9-pin DSUB male connector.
Ethernet LAN2	J12	RJ-45 connector with built-in activity and link indicators
Ethernet LAN1	J13	RJ-45 connector with built-in activity and link indicators
Keyboard/Mouse	J14	Keyboard and Mouse signals (6-pin DSUB female connector) to be used with a splitter cable (part #150-381)
Hot Swap	J15	Hot Swap Switch
CompactFlash	J16	Supports the Kontron's module dedicated to CompactFlash disks
Storage Mezzanine	J17	This mezzanine supports 1 hard drive EIDE
PCI Mezzanine	JN1-JN4	64-Bit, 66MHz PCI-Mezzanine
Battery	BT1	CMOS backup battery connector

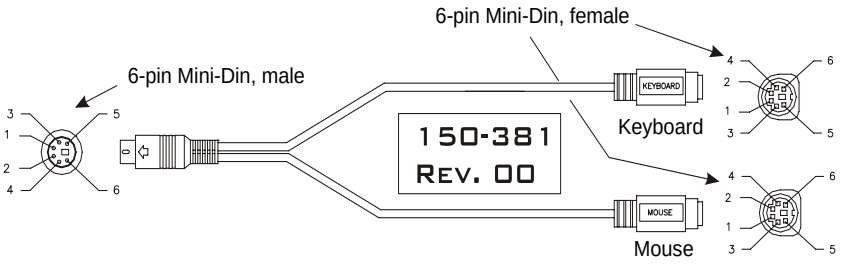
Located on faceplate

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3.3.4. Front Plate Connectors and Indicators



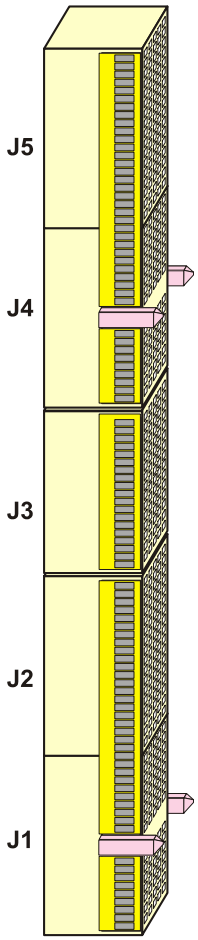
Name	Description	Comments
J10	Video Connector	Standard 15-pin DSUB female connector
SW1	Reset Button	Use a small tool to press the button and proceed to a hardware reset of the board
Blue LED	Ready to Swap	Lights when the board is ready to be swapped.
Green LED	HDD Activity	Indicates an activity on IDE
J11	Com Port 1	Standard 9-pin DSUB male connector
J12, J13	Ethernet 2 and 1	RJ-45 connectors with built-in activity and link indicators
J14	PS/2 Mouse and Keyboard	To connect a keyboard and/or a mouse through this connector, you need a Y shaped splitter cable (Kontron part number 150-381)



The front plate supports a PMC cutout and a cap that also act as an EMI shield when there are no PMC device installed.

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3.3.5. CompactPCI Connectors



- **CPCI J5 Connector**

  Legacy connections (IDE, Floppy)

- **CPCI J4 Connector**

  SCSI Ultra-160/320 connections (SCSI board version)
  or
  PIM connections (PIM board version)

- **CPCI J3 Connector**

  LAN0 and LAN1, Serial Ports 1 and 2, PS/2 Keyboard and Mouse, VGA, POST, ID, and USB.

- **CPCI J2 Connector**

  64 bit extension, arbitration, clocks, reset and power.

- **CPCI J1 Connector**

  Supports CPCI bus signals, and power.

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3.4. CUSTOMIZING THE BOARD

3.4.1. Processor and Fan

Your board will be installed with Pentium III processors and their adequate cooling system.

> **CAUTION**
>
> Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. Improper installation may damage the board and/or the CPU

3.4.1.1. Recommended operating and preventive maintenance:

The operational battery voltage must be between 2.9 and 3.6 volts.

When in storage, if it is kept in it's original packaging, the battery must be replaced:

- After 10 years and/or
- The battery voltage is below 2.9 volts.

For preventive operational maintenance, we recommend to verify the battery voltage every 4 years. The normal battery life expectancy is 10 years in storage mode or 3.9 years in operating mode with an estimated consumption constant load of 10µA, when the unit is continuously running.

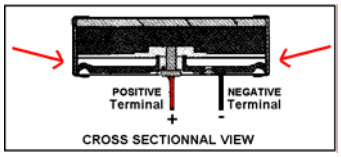
Kontron ordering part number: 100-001
Tadiran ordering part number: 15-51-86-420-007 (TL-5186)

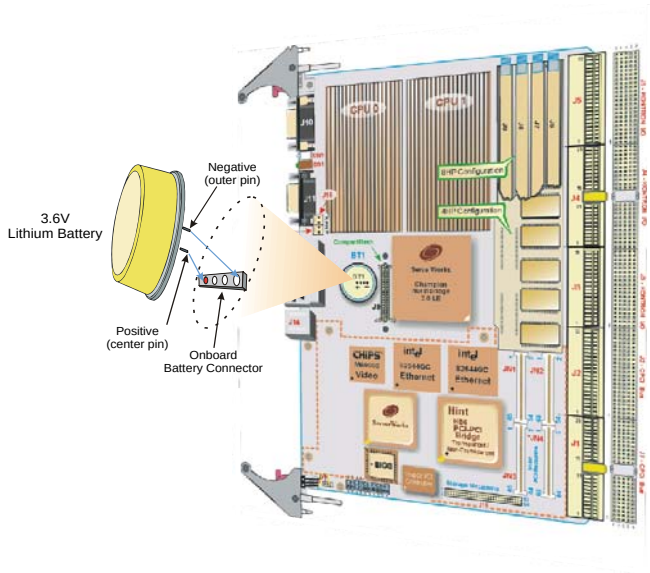
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3.4.2. Backup Battery

An on-board 3.6V lithium battery is provided to backup BIOS setup values and the real time clock (RTC). When replacing, the battery must be connected as follows:

- ❖ First, place your index and thumb at each side of the battery and gently pull out the battery, then you may insert a new one firmly in place with respect to the positive and negative location of the pins. The positive pin is the one pointing to the Ethernet connector and the negative pin is the one pointing to J9.





WARNING

Danger of explosion if battery is incorrectly replaced Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions. When you receive a board, remove the **install the battery jumper** to enable the battery (See section 3 for jumper settings)

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3.4.3. Memory

The board supports from 256MB to 4 GB of 64/72-bit RSDRAM (in 8HP configuration) divided into four DIMM sockets (J6, J7, J8 and J9) or from 512MB to 2 GB of 64/72-bit RSDRAM (in 4HP configuration, using a special module).

Related Jumpers
None

BIOS Setups
See 4.1.2.4 – *Phoenix Setup Program, Advanced, Advanced Chipset Control*

The RSDRAM DIMMs must conform to the following:

- 2.5V only, single-sided or double-sided
- (PC-133) RSDRAM
- Serial Presence Detect (SPD) EEPROM
- 64-bit and 72-bit DIMMs
- Error Checking and Correction (ECC) or parity bit, with 72-bit DIMMs.

Installation

- On an anti-static plane, place the board so that you are facing the DIMM sockets (the edge bracket must be located on the right).
- Insert the DIMM into the socket, aligning the notches on the module with the socket's key inserts.
- Push vertically the DIMM into the socket until the retaining clips snap on. Repeat these steps to populate the other sockets.

To remove a DIMM from a socket, push down the retaining clips on each side of the socket, to release the module. Pull the module upward to remove.

For the latest list of tested DIMMs devices please consult our FTP site at :

ftp://ftp.kontron.ca/Support/Product_Memory_AVL_Approved%20Vendor%20List/

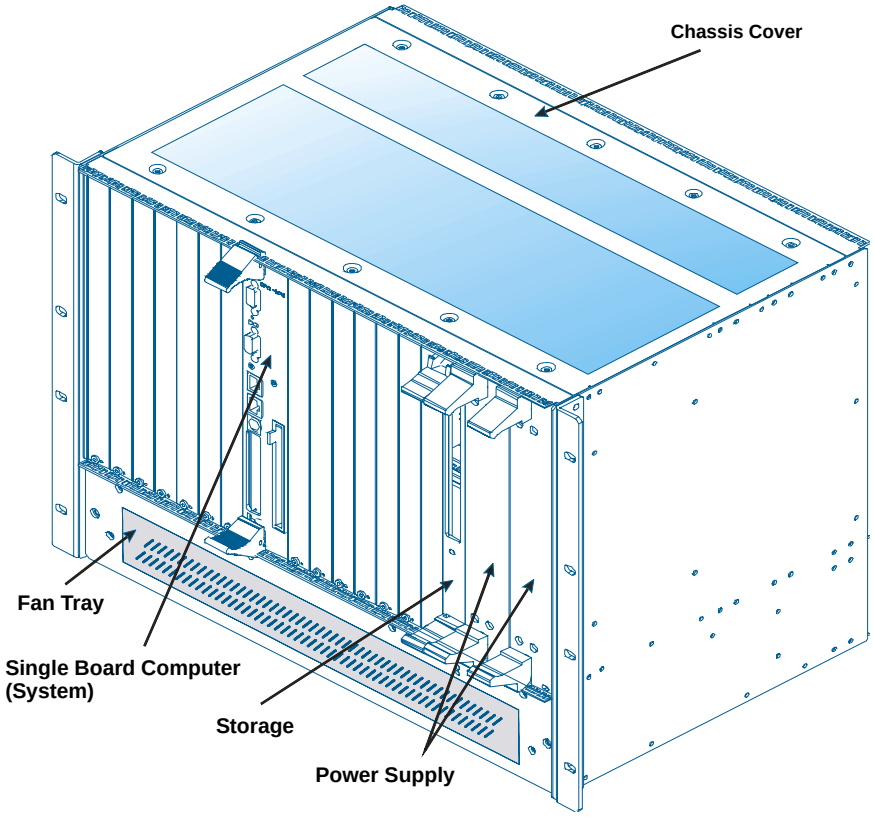
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3.5. BUILDING A CPCI SYSTEM

When building a CompactPCI system, a minimum requirement consists in: a chassis, a CompactPCI backplane, a storage module, a power supply unit, and a ventilation system.

The main AC power is drawn to the chassis components through an IEC power plug with a 2-stage filter, fuse holder and power switch. All power features are provided at the rear of the chassis.

The chassis may be used either as a desktop system or a rack-mount bay.



CXP08 and XL-PSB/VHDS

(CXP16 not supported)

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3.5.1. Backplane

An entry-level backplane is provided by Kontron. It is referred to as cBP-08R. It features 8 CPCI slots (one PCI I/O segment), and includes J3-J4-J5 I/O connectors on all slots.

All Kontron's CompactPCI backplanes feature pass-through connectors (J3-J4-J5) to support Rear Panel I/O connections.



IMPORTANT

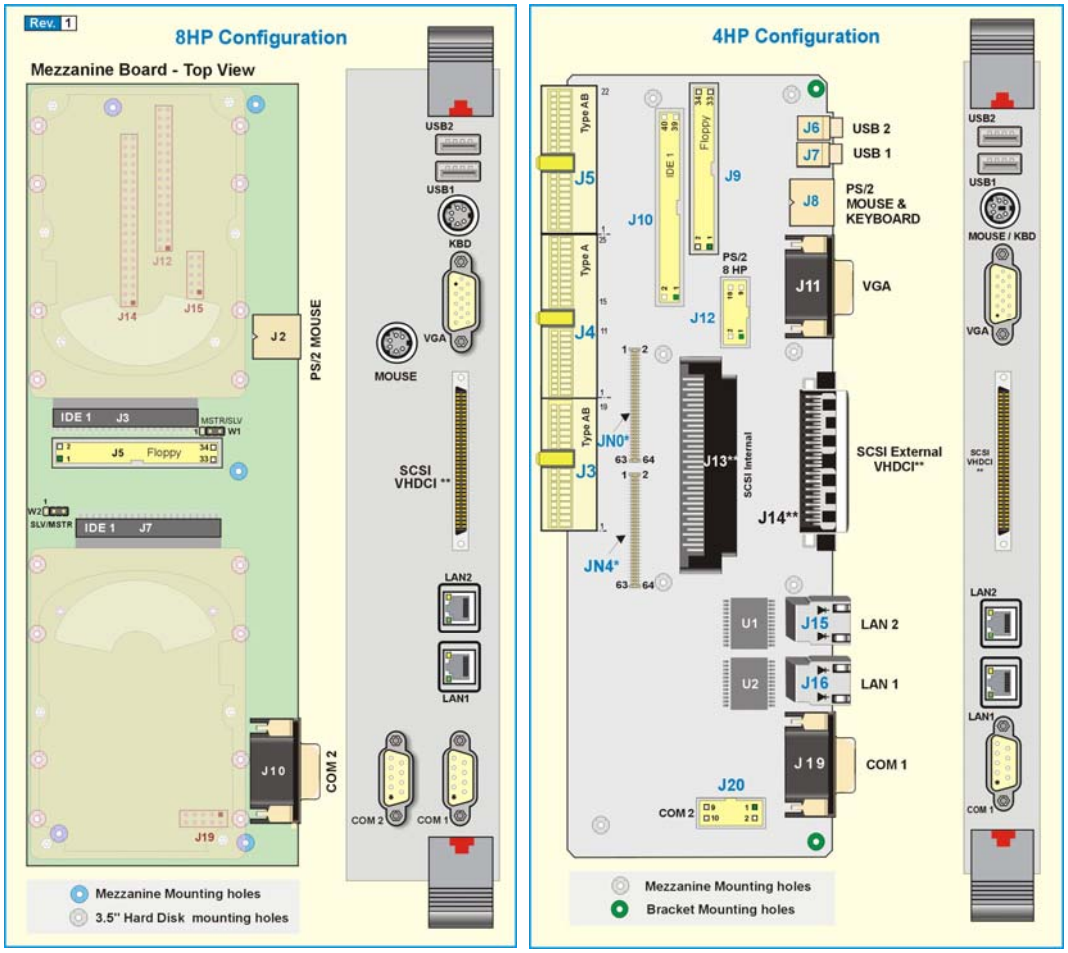
J1 and J2 are de-facto industry standard as defined by PICMG. J3, J4 and J5 are user-defined connectors and will vary from various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

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3.5.2. Rear-Panel I/O

This feature is intended to issue the I/O capabilities of the system processor to the rear of the enclosure using a Rear I/O Transition module (cTM80-2).

The Rear I/O Transition module gathers all the I/O signals of the CPU board and makes them easily accessible through standard headers and connectors located at the rear of enclosure. The cTM80-2. Transition Module is illustrated below.



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3.5.3. Storage Devices

A mezzanine card attaches directly to the system processor. 6U form factor storage modules are supported when using the cBP-08R backplane.

There are two ways of supplying data storage with Kontron's product line.

1. On-board Mezzanine Card that is installed directly onto the processor board.
2. cSM-DVD : 6U form factor storage module that is front loaded into the CxP08 chassis.

3.5.4. Power Supply

6U power supply modules featuring load sharing redundant mode and hot-swap capabilities allow on-site replacements of defective module while the system remains powered.

3.5.5. Fan Tray

The ventilation unit of the enclosure conforms to the global requirement of the system in fully loaded configuration.

3.5.6. Installing the Board into a Bay

The cPCI-DT64 is mechanical Eurocard form factor boards. It takes advantages of the IEEE1101.10 specifications that ensure a mechanical interchange capability between different plug-in elements in sub-racks.

Due to the high-density pinout of the Hard Metric connector, some precautions must be taken when connecting or disconnecting a board to/from a backplane:

1. Rail guides must be installed on the enclosure to slide the board to the backplane.
2. Do not use force if there is any mechanical resistance while inserting the board.
3. Screw the front plate to the enclosure to firmly attach the board to its enclosure.
4. Use the extractor handles to disconnect and extract the board from its enclosure.

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3.5.7. Connector Keying

CompactPCI connector support guide lugs to ensure a correct polarized mating. A proper mating is enhanced by the use of color coded keys for 3.3V and 5V operation.

Color coded keys prevent inadvertent installation of a 5V peripheral/system board in a 3.3V slot. The cPCI-DT64 is universal. It does not requires keying. The PCI bus requires to be keyed. Backplane connectors must always be keyed according to the signaling (VIO) level.
Coding Key Colors are defined as follows:

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	none
-48V	Red

3.5.8. Bus Mastering

The cPCI-DT64 provides seven pairs of REQ/GNT (0-6) arbitration signals through the Secondary PCI bus. This means the board is capable of driving up to seven CPCI slots with PCI Bus Master capabilities.

3.5.9. Connection

To install the cPCI-DT64 board into a bay, proceed as follows:

1. Locate the 6U system slot
2. Remove the front plate of the slot where you intend to insert the cPCI-DT64.
3. Ensure the module is properly aligned with the guide-rails and slide it gently until it touches the backplane connector

WARNING

1. Some mechanical parts of the guide-rail are fragile (shield contacts and clips). Do not use force to insert and connect a CompactPCI module.

2. If there is any mechanical resistance while you insert a module, first ensure there is no mechanical obstacle and check for the alignment of all parts.

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4. To engage the board's connectors into the backplane connector, press simultaneously the handles on the front plate.
5. Fasten the module using the fellow-plate fixing screw to secure the module to the system chassis.

To remove the module from the chassis, proceed as follows:

1. Remove the front plate fixing screws.
2. Press the handle to act as a lever to disengage the CompactPCI connector from the backplane.
3. Pull on the handle and gently remove the board.

3.6. CPCI I/O SIGNALS

This section describes integrated feature signals available on rear panel CPCI I/O connectors (J3, J4, and J5)

3.6.1. J3 Signal Specification

3.6.1.1. Ethernet

Signal	Pin Assignation	Description
LAN0, 1:ACT	A13, B13	Transmit / receive activity LED signal
LAN0, 1:LINK	A14, B14	Link integrity LED signal
LAN:CT	C14	

Signal	Pin		Signal	Pin	
LAN0:DA+	A18		LAN1:DA+	A16	Ethernet differential signals
LAN0:DA-	B18		LAN1:DA-	B16	
LAN0:DB+	A17		LAN1:DB+	A15	
LAN0:DB-	B17		LAN1:DB-	B15	
LAN0:DC+	D18		LAN1:DC+	D16	
LAN0:DC-	E18		LAN1:DC-	E16	
LAN0:DD+	D17		LAN1:DD+	D15	
LAN0:DD-	E17		LAN1:DD-	E15	

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3.6.1.2. Serial Port 1 (COM 1)

Signal	Pin Assignation	Description
COM1:DCD	D1	Data Carrier Detect
COM1:RX	B1	Receive Data
COM1:DSR	C1	Data Set Ready
COM1:TX	D2	Transmit Data
COM1:RTS	A1	Ready To Send
COM1:CTS	C2	Clear To Send
COM1:RI	A2	Ring Indicator
COM1:DTR	B2	Data Terminal Ready

3.6.1.3. Serial Port 2 (COM 2)

Signal	Pin Assignation	Description
COM2:DCD	D3	Data Carrier Detect
COM2:RXD	B3	Receive Data
COM2:DSR	C3	Data Set Ready
COM2:TXD	D4	Transmit Data
COM2:RTS	A3	Ready To Send
COM2:CTS	C4	Clear To Send
COM2:RI	A4	Ring Indicator
COM2:DTR	B4	Data Terminal Ready

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3.6.1.4. USB0, USB1

Signal	Pin Assignation	Description	
USB0:DATA+, DATA-	B8, A8	USB Data	Differential data path for USB 0 port
USB1:DATA+, DATA-	B9, A9	USB Data	Differential data path for USB 1 port
USB0,1:VCC	B10, A10	USB Voltage	Differential power level for USB 0 and 1 port

3.6.1.5. Keyboard

Signal	Pin Assignation	Description
KB:DATA	E4	Keyboard Data
KB:CLK	E5	Keyboard Clock

3.6.1.6. Mouse

Signal	Pin Assignation	Description
MOUSE:DATA	E3	Mouse Data
MOUSE:CLK	E2	Mouse Clock

3.6.1.7. Speaker

Signal	Pin Assignation	Description
SPEAKER	E7	Speaker signal

3.6.1.8. POST

Signal	Pin Assignation	Description
POST:DATA	E6	POST data
POST:CLK	D6	POST clock

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3.6.1.9. Video

Signal	Pin Assignation	Description
VGA:HSYNC	B5	Horizontal synchronization
VGA:VSYNC	C5	Vertical synchronization
VGA:SCL	D5	Video serial clock line
VGA:SDA	C6	Video serial data line
VGA:RED	A6	Analog red video signal
VGA:GREEN	B6	Analog green video signal
VGA:BLUE	A5	Analog blue video signal

3.6.1.10. ID

Signal	Pin Assignation	Description
ID0 – ID4	A7, E1, B7, C7, D7	

3.6.1.11. Power

Signal	Pin Assignation	Description
VCC	A19, B19	+5V Supply voltage
VCC3	C19	+3.3V Supply voltage
+12V	D19	+12V Supply voltage
-12V	E19	-12V Supply voltage
GND	C15 - C18	Ground

3.6.1.12. ID

Signal	Pin Assignation	Description
Reserved	A11, A12, B11, B12, C8-C13, D8-D14, E8-E14	Reserved for Kontron internal use.

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3.6.2. J4 Signal Specification

3.6.2.1. SCSI Interface

Signal	Pin Assignation	Description
D0+ to D15+	D4, A5, D5, A7, D7, A8, D8, A10, A24, D24, D22, D25, A1, D1, A2, D2	SCSI Data The SCSI data lines drive the ID during arbitration, selection, command and data information as well as status and messages.
D0- to D15-	E4, B5, E5, B7, E7, B8, E8, B10, B24, E24, B25, E25, B1, E1, B2, E2	
TERMPWR1 to TERMPWR9	A16,B16, A15, B15, D15, E15, B11, D11, E11	Termination Power.
IO +/-	D22, E22	In/Out – Indicates the In direction when asserted and the Out direction when not asserted.
REQ + / -	A22, B22	Request – A target will assert REQ to indicate a byte is ready or is needed by the Target.
CD + / -	D21, E21	Command/Data – Indicates Command or message phase when asserted, and Data phase when not asserted.
SEL + / -	A21, B21	SCSI Select – The line is driven after a successful arbitration to select as an initiator or reselect as a target and otherwise it is received.
MSG + / -	D19, E19	SCSI Message - Indicates a Message phase when asserted, and Command or Data phase when not asserted.
RST + / -	A19, B19	Reset – Signal is interpreted as a hard reset and will clear all commands pending on the SCSI bus.
ACK +/-	D18, E18	Acknowledge – Indicate a byte is ready for or was received from the Target.
BSY + / -	A18, B18	Busy – Handshake signal used during arbitration.
ATN + / -	D16, E16	Attention – This line is activated when a special condition occurs.

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SCSI Interface (continued)

DPL + / -	D10, E10	SCSI High/Low Parity – Provide odd parity for data lines.
DPH + / -	A4, B4	
DIFFSENS	A11	Differential Sense Detects the voltage level of a SCSI signal to determine whether it is a single-ended or LVD
VCC	B23	+5V
VCC3	E23	+3.3V
GND	A3, A6, A9, A17, A20, B3, B6, B9, B17, B20, C1 to C25, D3,D6,D9, D17, D20, E3, E6,E9, E17, E20	Ground
Reserved	A23, D23	

3.6.2.2. PIM Interface

Signal	Pin Assignation	Description
PIM1 to PIM 10	A25, D25, B25, E25, A24,D24, B24, E24, A22, D22	PIM Interface
PIM11 to PIM20	B22, E22, A21, D21, B21, E21, A19, D19, B19, E19	
PIM21 to PIM30	A18, D18, B18, E18, A16, D16, B16, E16, A15, D15	
PIM31 to PIM40	B15, E15, A11, D11, B11, E11, A10,D10, B10, E10	
PIM41 to PIM50	A8, D8, B8, E8, A7,D7, B7, E7, A5, D5	
PIM51 to PIM60	B5, E5, A4, D4, B4, E4, A2, D2, B2, E2	
PIM61 to PIM64	A1, D1, B1, E1	
VCC	B23	+5V
VCC3	E23	+3.3V
GND	A3, A6, A9, A17, A20, B3, B6, B9, B17, B20, C1 to C25, D3,D6,D9, D17, D20, E3, E6,E9, E17, E20	Ground

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3.6.2.3. JN4 (mezzanine connector)

P1+ to P32+	1, 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46, 49, 50, 53, 54, 57, 58, 61, 62
P1- to P32-	3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28, 31, 32, 35, 36, 39, 40, 43, 44, 47, 48, 51, 52, 55, 56, 59, 60, 63, 64

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3.6.3. J5 Signal Specification

3.6.3.1. IDE Interface

Signal	Pin Assignation	Description
IDE:RESET#	E15	Reset signal
IDE1:D0-D15	A18, D18, A17, D17, A16, D16, A15, D15, B15, E16, B16, E17, B17, E18, B18, E19,	Disk Data – These signals are used to transfer data to or from the IDE device.
IDE1:DMARQ	D19	Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
IDE1:IOW#	B19	Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from data lines.
IDE1:IOR#	A19	Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
IDE1:IORDY	E20	I/O Channel Ready –This input signal is negated to extend the host transfer cycle of any host register read/write access when the drive is not ready to respond to a data transfer request. When not negated, it is in a high impedance state.
IDE1:DMACK#	D20	DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IDE1:ACT#	A22	Activity indicator
IDE1:IRQ	B20	IRQ line
IDE1:IOCS16#	A20	I/O Chip Select - Indicates to the host that the 16 bit data port has been addressed and the drive is prepared to send/receive a 16 bit data word.
IDE1:A0 – A2	B21, D21, A21	Disk Address – These signals indicate which byte in either the ATA command block or control block is being addressed.
IDE1:CS0#, CS1#	D22, B22	Chip Select - For ATA control register
IDE1:PDIAG#	E21	Diagnostic - Will be asserted by Drive 1 to indicate to Drive 0 that it has passed diagnostics. Following a power-on reset or software reset, Drive 1 will negate - PDIAG within 1 msec to indicate to Drive 0 that it is busy.

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3.6.3.2. Floppy Disk Interface

Signal	Pin Assignation	Description
FD:INDEX#	B11	Index
FD:MTR0,1#	A11, B12	Motor 0-1 enable
FD:DSEL 0,1#	D12, E12	Drive 0-1 select
FD:DIR#	A12	Direction
FD:STEP#	E13	Step pulse
FD:WDATA#	D13	Write disk data
FD:WGATE#	B13	Write gate
FD:TRK0#	A13	Track 0
FD:WRPROT#	E14	Write protected
FD:RDATA#	D14	Read disk data
FD:HDSEL#	B14	Head select
FD:DSKCHG#	A14	Disk change
FD:DENSEL#	E11	Density select
FD:MSEN0 FD:MSEN1	A10 B10	
FD:FDEDIN#	D11	

3.6.3.3. Ground and Reserved pins

Signal	Pin Assignation	Description
GND	ROW C (C1-C22)	Ground
RSV	A1-A9, B1-B9, D1-D10, E1-E10, E22	Reserved pins

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PART 4

4. SOFTWARE SETUP

1. **PHOENIX BIOS SETUP PROGRAM**

2. **INSTALLING DRIVERS**

3. **CONSOLE REDIRECTION (VT-100 MODE)**

Note **UPDATING OR RESTORING THE BIOS IN FLASH**

See Kontron FTP site at location
ftp://ftp.kontron.ca/Support

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4.1. PHOENIX BIOS SETUP PROGRAM

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

4.1.1. Accessing the BIOS setup program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the DT64 peripheral processor. The DT64 uses the Phoenix Setup program, a setup utility in flash memory that is accessed by pressing the <DELETE> key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

> **CAUTION**
>
> Before modifying CMOS setup parameters, ensure that the W1 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section 3.2).

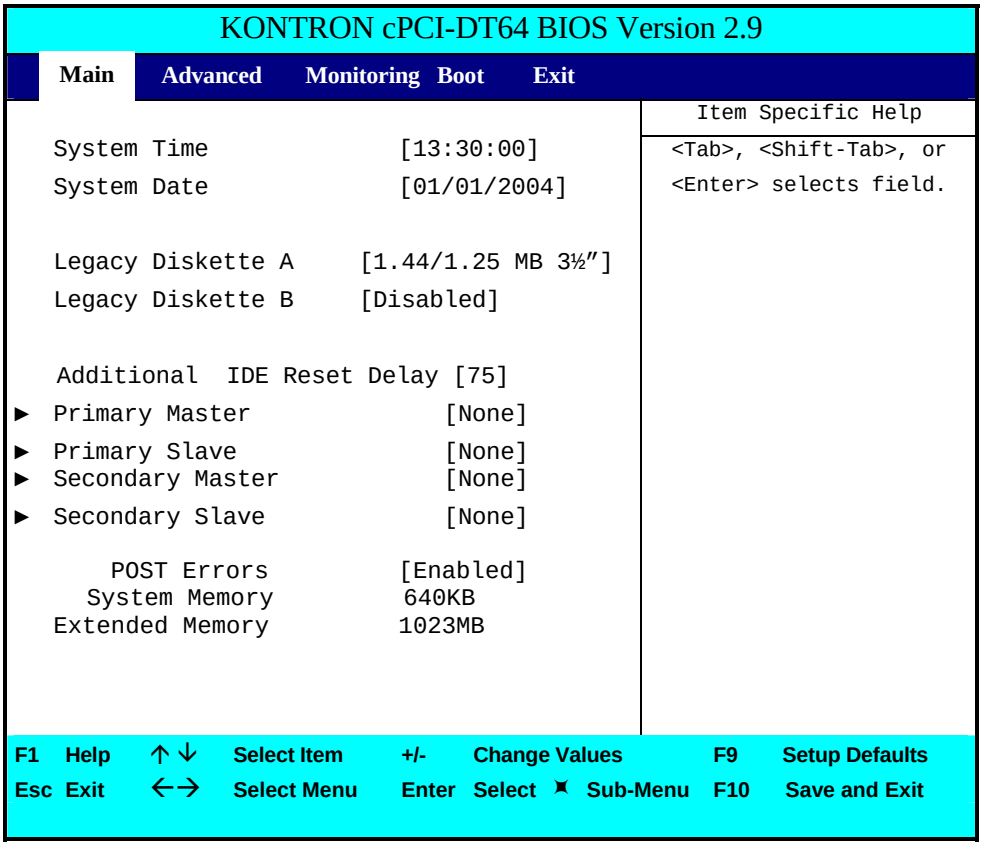
To run the Phoenix Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- When you get the following message, hit <DELETE> key to enter SETUP

```
PhoenixBIOS 4.0 Release 6.0
Copyright 1985-2000 Phoenix Technologies Ltd.
All Rights Reserved
KONTRON  cPCI-DT64 BIOS Version 2.9
```


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The main menu of the Phoenix BIOS CMOS Setup Utility appears on the screen.



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Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the SETUP defaults will affect all parameters and will reset options previously altered.

The Setup Defaults values provide **optimum performance** settings for all devices and system features.

> **CAUTION**
>
> These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

> **NOTES**
>
> The CMOS setup option described in this section is based on **BIOS Version 2.9**. The options and default settings may change in a new BIOS release.

4.1.2. The Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu selection	Description
Main	Use this menu for basic system configuration
Advanced	Use this menu to set the Advanced Features available on your system
Monitoring	Use this menu to configure the system monitoring
Boot	Use this menu to determine the booting device order.
Exit	Use this menu chose Exits option

Use the left and right ← and → arrows keys to make a selection.

4.1.2.1. The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates:

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Key	Function
<F1> or <Alt-H>	General Help windows (see 4.1.2.2)
<Esc>	Exit this menu.
← → arrow keys	Select a different menu
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<F5> or <->	Select the Previous Value for the field.
<F6> or <+> or <Space>	Select the Next Value for the field.
<F9>	Load the Default Configuration values for all menus
<F10>	Save and exit.
<Enter>	Execute Command, display possible value for this field or Select the Sub menu

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To select an item, use the arrow keys to move the cursor to the field your want. Then use the plus-and-minus value keys to select a value for that field. To save values commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub-menu, use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A pointer (►) marks all sub menus.

4.1.2.2. The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

4.1.2.3. The General Help Windows

Pressing <F1> or <Alt-H> on any menu brings up the General Help window that describes the legend keys and their alternates:

```
                    General Help

Setup changes system behavior by modifying the BIOS
configuration. Selecting incorrect values may
cause system boot failure; load Setup Default values to
recover.

<Up/Down>  arrows select fields in current menu.
<PgUp/PgDn> moves to previous/next page on scrollable menus.
<Home/End>  moves to top/bottom item of current menu.

Within a field, <F5> or <-> selects next lower value and
<F6>, <+>,  or  <Space>  selects next higher value.

<Left/Right> arrows select menus on menu bar.
<Enter> displays more options for items marked with ▪ .

<F9> loads factory installed Setup Default values.
<F10> saves current settings and exists Setup.

<Esc> or <Alt-X> exits Setup; in sub-menus, pressing these keys returns to
the previous menu.

<F1> or <Alt-H> displays General Help (this screen).

                          [        ]
```


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4.1.2.4. Main Menu Selection

The scroll bar on the right of any windows indicates that there is more than one page of information in the window. Use <PgUp> and <PgDn> to display all the pages. Pressing <Home> and <End> displays the first and last page. Main Menu Selection
You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.
Legacy Diskette A: Legacy Diskette B:	Disabled 360Kb 5.1/4” 1.2MB, 5.1/4” 720 Kb 3 1/2” 1.44/1. 25 MB 3 1/2” 2.88 MB 3 1/2	Select the type of floppy disk drive installed in your system. **Note :** 1.25MB 3 1/2” references a 1024 byte/sector Japanese media format. The 1.25MB, 3 1/2 diskette requires a 3-Mode floppy-disk drive.
Additional IDE Reset Delay	0 to 255 ms	Additional Delay after IDE soft reset for auto-detect the drives.

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Main Menu Selection (continued)

Feature	Options			Description
Primary Master	Type	None		None : No booting device installed.
		CD-ROM	Multi-Sector Transfers LBA Mode Control 32 BIT I/O Transfer Mode Ultra DMA Mode SMART Monitoring	**Multi-Sector Transfers** Choices : Disabled, 2,4,8, and 16 sectors Any selection except Disabled determines the number of sectors transferred per block. Standard is 16 sectors per block. **LBA Mode Control** Choices : Disabled, Enabled Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, heads, and Sectors. **32 Bit I/O** Choices : Disabled, Enabled Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus. **Transfer Mode** Choices : Standard, Fast PIO 1, Fast PIO 2, Fast PIO 3, Fast PIO 4, FPI0 3 / DMA 1, FPIO 4 / DMA2. Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform. **Ultra DMA Mode** Choices : Disabled, Mode 0, 1, 2, 3, 4. Select the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **SMART Monitoring** Display type of Monitoring. This field is a "Display Only".
		ATAPI Removable		Same choices as CD-ROM

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Main Menu Selection (continued)

Feature	Options			Description
Primary Master (Continued)	Type (continued	IDE Removable		Same choices as CD-ROM
		Other ATAPI		Same choices as CD-ROM
		(USER)	Cylinders	**Cylinders** Set the number of cylinders
			Heads	**Heads** Set the number of heads. Choices are 1 to 16
			Sectors	**Sectors** Set the number of sectors per track
			Maximum Capacity	**Maximum Capacity** Maximum capacity is displayed according to the cylinders, heads and sectors selected.
			Multi-Sector Transfers	**Multi-Sector Transfers** Choices are : Disabled, 2, 4, 8 and 16 sectors. Specify the number of sectors per block for multiple sector transfers. "MAX" refers to the size the disk returns when queried.
			LBA mode Control	**LBA Mode Control** Choices are : Enabled, Disabled Enabling LBA cause Logical Block Addressing to be used in place of Cylinders Heads and Sectors
			32 Bit I/O	**32 Bit I/O** Choices are : Enabled, Disabled. This setting enables or disables 32 bit IDE data transfers.
			Transfer Mode	**Transfer Mode** Choices are : Standard, Fast PIO 1, Fast PIO 2, Fast PIO 3, Fast PIO 4, FPI0 3 / DMA 1, FPIO 4 / DMA2. Select the method for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
			Ultra DMA Mode	**Ultra DMA Mode** Choices are: Disabled, Mode 0 to 4. Select the Ultra DMA mode used for moving data to/from the drive Autotype the drive to select the optimum transfer mode.
			SMART Monitoring	**SMART Monitoring** IDE Failure Prediction
		Auto		BIOS autodetects the hard disk installed
Primary Slave	Same as Primary Master			

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Main Menu Selection (continued)

Feature	Options	Description
Secondary Master	Same as Primary Master	
Secondary Slave	Same as Primary Master	
POST Errors	Enabled Disabled	Pauses and displays SETUP entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot.
System Memory	N/A	Displays amount of conventional memory detected during boot up.
Extended Memory	N/A	Displays the amount of RAM memory detected during boot up minus the base memory (1 Mbyte).

4.1.2.5. Advanced Menu Selection

You can make the following selections on the Advanced Menu. Use the sub menus for other selections.

Feature	Options	Description
Boot Settings Configuration	**This is a Sub-Menu, see section 4.1.2.5.1**	Additional setup menus to configure boot settings
PCI Configuration	**This is a Sub-Menu, see section 4.1.2.5.2**	Additional setup menus to configure PCI devices
Cache Memory	**This is a Sub-Menu, see section 4.1.2.5.3**	Determines how to configure the specified block of memory
On-Board Device Configuration	**This is a Sub-Menu, see section 4.1.2.5.4**	Peripheral Configuration
Advanced Chipset Control	**This is a Sub-Menu, see section 4.1.2.5.5**	
Console Redirection	**This is a Sub-Menu, see section 4.1.2.5.6**	Additional setup menus to configure console.

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4.1.2.5.1. Boot Settings Configuration

You can make the following selections on the Boot Settings Configuration Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
Installed O/S	Other Win95 Win98 WinMe Win2000	Other : General Settings Win95/Win98/WinMe/Win2000: Specific Settings **Note :** An incorrect setting can cause some operating systems to display unexpected behavior.
Enable ACPI	Yes No	Enable/Disable ACPI BIOS (Advance Configuration and Power Interface)
Reset Configuration Data	No Yes	Select "Yes" if you want to clear the Extended System Configuration Data (ESCD) area.
Boot-time Diagnostic Screen	Enabled Disabled	Displays the Diagnostic Screen during Boot. Always Enabled when Console Redirection is activated.
Clearing Extended Memory	Enabled Disabled	Allows the system to skip clearing memory if quick boot is enabled. This will decrease the time needed to boot the system. Some OS require memory to be cleared.
Summary Screen Delay	None 5 seconds	Delay to display the system configuration at boot time.
Save CMOS in FLASH	Disabled Enabled	Saving CMOS memory content into Flash Memory will prevent loosing CMOS options when battery fails.
Retry Boot Sequence	Disable Enabled	Enable this option to retry the boot sequence until a successful boot. (infinite retry)
SMART Device Monitoring	Disable Enabled	IDE Failure Prediction
PS/2 Mouse	Disable Enabled	'Disabled' prevent any installed PS/2 mouse from functioning, but frees up IRQ 12. 'Enabled' forces the PS/2 mouse port to be enabled regardless if a mouse is present.
Use Multiprocessor Specification	1.1 1.4	Configures the multiprocessor specification (MPS) revision level. Some operating systems will require revision 1.1 for compatibility reasons.

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4.1.2.5.2. PCI Configuration

You can make the following selections on the PCI Configuration Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
On-board Ethernet Controller	**This is a Sub-Menu, see section 4.1.2.5.2.1**	Additional setup menus to configure embedded Ethernet Controller
Mezzanine PMC Expansion Slot	**This is a Sub-Menu, see section 4.1.2.5.2.2**	Additional setup menus to configure PMC Expansion Slot.
PCI Performance setting	**This is a Sub-Menu, see section 4.1.2.5.2.3**	Additional setup menus to configure PCI Performance settings
Default Primary Video Adapter	On-board External	Select "External" to have PCI video card (must be installed) to be set as boot Display Device.
Delay before PCI Initialization	0 to 7	Delay in seconds before PCI Initialization. Some external card may require a minimum delay after reset before they can be accessed. Card with on-board CPU that emulate a PCI Controller (ex.: RAID) are more likely to require a delay.
Local Bus IDE adapter	Disabled Both	Enabled the integrated local bus IDE adapter.
USB Host Controller	Enabled Disabled	Enables or Disable the USB hardware (Disabled resources will be freed up for other uses).
USB BIOS Legacy Support	Auto Enabled Disabled	Enables or Disables support for USB Keyboards and Mice. (Enable for use with a non-USB aware Operating System such as DOS or UNIX) Select Auto to Automatic Enable USB Host Controller and USB BIOS Legacy Support if NO PS/2 keyboard
Reset Slave Board from Host	Disabled Enabled	Enabled – The PCI Reset from System Board will Reset Slave Board. Disabled – Reset only the secondary side of the PCI-PCI Slave Bridge.
PCI Reset on Warm Boot	None PCI Slots	Select if RST# signal is to be asserted on Warm Boot.

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4.1.2.5.2.1. On-board Ethernet Controller

You can make the following selections on the On-board Ethernet Controller Sub-Menu.

Feature	Options	Description
On-board Ethernet 1 Controller	Enabled Disabled	Enables/Disables on-board Ethernet 1 controller
Option ROM Scan	Enabled Disabled	Initialize device expansion ROM
On-board Ethernet 2 Controller	Enabled Disabled	Enables/Disables on-board Ethernet 2 controller
Option ROM Scan	Enabled Disabled	Initialize device expansion ROM

4.1.2.5.2.2. Mezzanine PMC Expansion Slot

You can make the following selections on the Mezzanine PMC Expansion Slot Sub-Menu.

Feature	Options	Description
On-board PMC Expansion Slot	N/A	
Option ROM Scan	Enabled Disabled	Initialize device expansion ROM
Mezzanine PMC Expansion Slot	N/A	
Option ROM Scan	Enabled Disabled	Initialize device expansion ROM

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4.1.2.5.2.3. PCI Performance setting

You can make the following selections on the PCI Performance setting Sub-Menu.

Feature	Options	Description
PCI Bridges Cache Line Size	0, 2, 8 or 16	Set the Cache Line Size on DWORDS.
Default Primary Latency Timer	Default, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks for device not in this menu. Default = 20h for PCI bridges. Default = value based on Minimum Grant for all other PCI devices.
Default Secondary Latency Timer	None, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks.
Primary Host Bridge Latency Timer	None, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks.
Secondary Host Bridge Latency Timer	None, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks.

4.1.2.5.3. Cache Memory

You can make the following selections on the Cache Memory Sub-Menu.

Feature	Options	Description
Memory Cache	Enabled Disabled	Sets the state of memory cache.
Cache System BIOS area	Uncached Write Protect	Controls caching of system BIOS area.
Cache Video BIOS area	Uncached Write Protect	Controls caching of video BIOS area.
Cache Base 0-512K	Uncached Write Through Write Protect Write Back	Controls caching of 512K base memory.
Cache Base 512K-640K	Uncached Write Through Write Protect Write Back	Controls caching of 512K-640K base memory.
Cache Extended Memory Area	Uncached Write Through Write Protect Write Back	Controls caching of system memory.

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4.1.2.5.4. On-board Device Configuration

You can make the following selections on the On-board Device Configuration Sub-Menu.

Feature	Options	Description
Serial port A	Enabled Disabled Auto	Configure serial port 1 using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Base I/O address	3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4 or 2E8/IRQ3	Sets the base I/O address for serial port 1.
Serial port B	Enabled Disabled Auto	Configure serial port 2 using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Mode	RS-422 RS-485 RS-232	Set the mode for Serial Port 2.
Base I/O address	3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4 or 2E8/IRQ3	Sets the base I/O address for serial port 2.
Floppy Disk Controller	Enabled Disabled	Enables the Floppy Disk Controller

4.1.2.5.5. Advanced Chipset Control

You can make the following selections on the Advanced Chipset Control Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
CNB30 Setting	**This is a Sub-Menu, see section 4.1.2.5.5.1**	CNB30 advanced chipset setup.
Error Command Settings	**This is a Sub-Menu, see section 4.1.2.5.5.2**	SERR# and PERR# enable or disable

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4.1.2.5.5.1. CNB30 Setting

You can make the following selections on the CNB30 Setting Sub-Menu.

Feature	Options	Description
PCI Back to Back Write	Enabled Disabled	PCI Back-to-Back write enabled or disable for Processor Bus-to-PCI posted writes.
IOQ Threshold Value	Hardwired, 1, 2, 3, 4, 5, 6, or 7	Uses hardware setting if set to Hardwired. Otherwise uses the IOQ value set by the user.
CAS Latency	3 or 2	SDRAM CAS Latency

4.1.2.5.5.2. Error Command Settings

You can make the following selections on the Error Command Settings Sub-Menu.

Feature	Options	Description
ECC Config	Enabled Disabled	Enable/Disable ECC Support
Scrubbing	Enabled Disabled	When enabled, CNB30 writes back the ECC corrected memory data back to the DRAM
Correctable Error	Enabled Disabled	Enable/Disable Correctable Error Settings
Action after Uncorrectable ECC	Continue Halt Reboot	Select what the system will do when an Uncorrectable ECC error has been detected

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4.1.2.5.6. Console Redirection

You can make the following selections on the Console Redirection Sub-Menu.

Feature	Options	Description
Com Port Address	On-board COMA On-Board COMB	If enabled, it will use a port on the motherboard. Install the VT100 jumper to use the Console Redirection.
Baud Rate	300, 1200, 2400, 9600, 19.2K, 38.4K, 57.6K, 115.2K	Enables the specified baud rate.
Parity	None	Fix setting: No Parity
Data Bits	8	Fix setting: 8 Data Bits
Stop Bit(s)	1	Fix setting: 1 Stop Bit
Console Type	VT100 VT100, 8bit PC ANSI, 7bit PC ANSI VT-100+ VT-UTF8	Enables the specified console type.
Flow Control	None XON/XOFF CTS/RTS	Enables Flow Control
Console connection	Direct Via modem	Indicate whether the console is connected directly to the system or a modem is used to connect.
Continue C.R. after POST	Off, On	Enables Console Redirection after OS has loaded.

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4.1.2.6. Monitoring Menu Selection

You can make the following selections on the Monitoring Menu. Use the sub menus for other selections.

Feature	Options	Description
Intelligent System Monitoring	**This is a Sub-Menu, see section 4.1.2.6.1**	
DMI Event Logging	**This is a Sub-Menu, see section 4.1.2.6.2**	View and modify DMI event logs.
IPMI System Management	**This is a Sub-Menu, see section 4.1.2.6.3**	NOTE: the submenu is not available if the BMC reset jumper is installed (W9). The BIOS setup will in that case show: Check the BMC reset jumper and the IPMI Firmware version update.
Watchdog After POST	**Disabled** **Enabled**	Enables the watchdog circuit after the POST sequence. Application software must refresh the watchdog to prevent system reset.
Watchdog Duration	**16 seconds** **1 minute** **4 minutes**	Select the duration time of the watchdog timing circuitry.
Display and Clear Reset History	Enabled Disabled	Enable/disable Display FPGA Reset History in Summary Screen and Clear FPGA History.
FPGA IRQ	Disabled IRQ 5 IRQ 7 IRQ 9	Select FPGA IRQ for SWITCH, WATCHDOG and ENUM# events. If '*' is shown, this IRQ# is already used by KCS-SMS IRQ.

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4.1.2.6.1. Intelligent System Monitoring

You can make the following selections on the Intelligent System Monitoring Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
Intelligent System Monitoring	Disabled Enabled	Enables/Disables the Intelligent System Monitor device. When enabled, the system will monitor some system states such as temperature and power supplies.
Interrupt Generation	Disabled Enabled	Enables/Disables the generation of interrupts when an event occurs. This must be set to DISABLED when programs such as LANDesk® are loaded onto the system.
Beep codes for non-thermal events	Disabled Enabled	Produces beep codes when the Intelligent System Monitoring events occur for either the chassis, the fan or the voltages. Codes are as follows: One long beep plus: 2 short beeps for chassis intrusion 3 short beeps for fan events 4 short beeps for voltage events This alarm may not be supported by the operating system.
Thermal Audio Alarm	Disabled Enabled	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. This alarm may not be supported by the operating system.
Hardware Monitor Temperature	**This is a Sub-Menu, see section 4.1.2.6.1.1**	
Hardware Monitor Voltage Inputs	**This is a Sub-Menu, see section 4.1.2.6.1.2**	
Control Temperature Events	**This is a Sub-Menu, see section 4.1.2.6.1.3**	
Control Voltage Events	**This is a Sub-Menu, see section 4.1.2.6.1.4**	

4.1.2.6.1.1. Hardware Monitor Temperature

Feature	Options	Description
System board Temperature	**Displays a Status and limit set in other menu.**	
CPU 1 Die Temperature		
CPU 2 Die Temperature		

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4.1.2.6.1.2. Hardware Monitor Voltage Inputs.

Feature	Options	Description
Vcore CPU 1	**Displays a Status and limit set in other menu.**	
Vcore CPU 2		
Vcc3 3.3V		
Vcc 5V		
Vin 2.5V		
Vtt		
Vbat		
Vin 12V		
Vin –12		
Vin 1.8V Ethernet		
Vin 1.5V Ethernet		
Vin 2.5V Ethernet		

4.1.2.6.1.3. Control Temperature Events.

Feature	Options	Description
CPU 1 Temperature Interrupt	Enabled Disabled	This option enables Temperature events handling.
CPU 2 Temperature Interrupt	Enabled Disabled	This option enables Temperature events handling.
Resume Alarm (ºC)	10ºC to 70ºC with step of 4ºC	Full speed (Normal mode) will be resumed when the temperature comes down to the selected temperature.
Overheat Alarm (ºC)	30ºC to 90ºC with step of 4ºC	The CPU will be slowed down (Doze mode) When it reaches the selected temperature.
Shutdown Alarm (ºC)	60ºC to 95ºC with step of 5ºC	The CPU will be halted when it reaches the selected temperature. The system will have to be restarted.

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4.1.2.6.1.4. Control Voltage Events.

Feature	Options	Description
Vcore CPU 1 Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vcore CPU 2 Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vcc3 3.3V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vcc 5V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin 2.5V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vtt Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vbat Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin 12V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin -12 Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin 1.8V Ethernet Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin 1.5V Ethernet Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin 2.5V Ethernet Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.

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4.1.2.6.2. DMI Event Logging

You can make the following selections on the DMI Event Logging Sub-Menu.

Feature	Options	Description
Event log capacity	Space Available or Full	Report the space available in the DMI event log. If set to 'Full', the event log has no more available space to store DMI events.
Event log validity	valid or Invalid	Report the validity of the DMI Event log buffer (in ESCD Flash area).
View DMI event log	Enter	View the contents of the DMI event log.
Clear all DMI event logs	Yes NO	Setting this to yes will clear the DMI event log after rebooting.
Event Logging	Enabled Disabled	Select 'Enabled' to allow logging of DMI events.
ECC Event Logging	Enabled Disabled	Select 'Enabled' to allow logging of ECC events.
Mark DMI events as read	Enter	Press Enter to mark all DMI events in the event log as read.

4.1.2.6.3. IPMI System Management

You can make the following selections on the IPMI System Management Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
IPMI Device and Firmware Information	This is a submenu, see section 4.1.2.6.3.1	Intelligent Platform Management Interface (IPMI) information.
FRU Board Information	This is a submenu, see section 4.1.2.6.3.2	Field Replaceable Unit (FRU) information about the board.
KCS-SMM SMI	Disabled Enabled	Allow Baseboard Management Controller (BMC) SMI handler for the initialization or startup of certain functions in the Management Controllers, such as setting the initial timestamp time. WARNING: option forced to Disabled if the TEST jumper (W3) is installed. If this is the case, it will be impossible to enable this SMI Handler (only option available will be Disabled)..

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IPMI System Management (continued)

Feature	Options	Description
Sensors Refresh Rate	5 seconds 30 seconds 1 minute 5 minutes 1 hour	Select the refresh rate at which some sensor values will be sent to the management controller. Sending sensors from BIOS takes CPU time from OS
KCS-SMS IRQ	Disabled IRQ 5 IRQ 7	Select BMC IRQ for the System Management Software (SMS). SMS takes platform management information and links it into other aspects of systems management, such as software management and distribution, alerting, and remote console access. If '*' is shown, this IRQ# is already used by FPGA IRQ.
Dual Port IPMB Redundancy	Enabled Disabled	Intelligent Platform Management Bus (IPMB). Enabled - IPMB1 is hidden behind IPMB0 and used as a Redundancy channel. Disabled - IPMB0 and IPMB1 operate as separate channels.
Management Controller Configuration	BMC Satellite	BMC - the board is the 'central' management controller. Satellite - the Board is a Satellite Management Controller, under the control of an external 'central' Management Controller. The BMC manages the interface between system management and the platform management hardware.
Clear SEL	Yes No	Select 'YES' if you want to clear all contents of the IPMI System Event Log on next boot only.
IPMI Watchdog Timer Use	None BIOS/POST OS Load Both	Indicates the current use assigned to the Watchdog Timer. BIOS/POST – Watchdog Timer used by the BIOS POST. OS Load - OS Load Timeout. This mode requires SMS or OS support.
BIOS Timer Countdown	30 seconds 1 minute 2 minutes 4 minutes	Initial BIOS Timer Countdown Value.
OS Load Timer Countdown	30 seconds 1 minute 2 minutes 4 minutes 8 minutes 16 minutes 32 minutes	Initial OS Load Timer Countdown Value.
OS load Timer Action	None Hard Rst Pwr down Pwr Cycle	

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4.1.2.6.3.1. IPMI Device and Firmware Information

Feature	Static information	Description
Product ID	6006	Kontron board identifier. Provide a numeric value that identifies a particular System (or board) type.
IPMI Version	1.5	IPMI specification version. This field holds the version of the IPMI specification that the controller is compatible with. (Subject to change)
Device ID	1	IPMI implementation ID used with this product ID. Provide a numeric value that identifies a particular controller type.
Device Revision	0	
Firmware Revision	3.00	IPMI firmware revision. (Subject to change)
SDR Revision	10	Sensor Data Records package revision. (Subject to change)
CPCI Slot Number	8	

4.1.2.6.3.2. FRU Board Information

Feature	Static information	Description
Board Product Number	DT64	Inventory information about the board. (Board Serial and Part Numbers are examples only)
Board Serial Number	1000123456	
Board Part Number	T6006#A#A_1000	

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4.1.2.7. Boot Menu Selection

Feature	Options	Description
	Hard Drive Bootable Add-in Cards Primary Master Removable Devices Legacy Floppy Drives Hard Drive Bootable Add-in Cards * ATAPI CD-ROM Drive Network Boot	Keys used to view or configure devices: **<Enter>** expands or collapses devices with a **+** or **–** **<Ctrl+Enter>** expands all **<Shift + 1>** enables or disables a device **<+>** or **<->** moves the device up or down **<n>** May move removable device between Hard Disk or Removable Disk **<d>** Remove a device that is not installed. * Note : The hard drives and SCSI drives detected will be listed in this section and the first drive in the list will be the boot drive.

4.1.2.8. Exit Menu Selection

Feature	Options		Description
	Exit Saving Changes	Yes / No	**Exit Saving Changes** Setup and save your changes to CMOS.
	Exit Discarding Changes	Yes / No	**Exit Discarding Changes** Exit utility without saving Setup data to CMOS.
	Load Setup Defaults	Yes / No	**Load Setup Defaults** Exit utility without saving Setup data to CMOS.
	Discard Changes	Yes / No	**Load Setup Defaults** Load default values for all SETUP items.
	Saves Changes	Yes / No	**Discard Changes** Load previous values from CMOS for all SETUP items.
			Save Changes Save Setup Data to CMOS.

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4.1.2.9. Boot Utilities

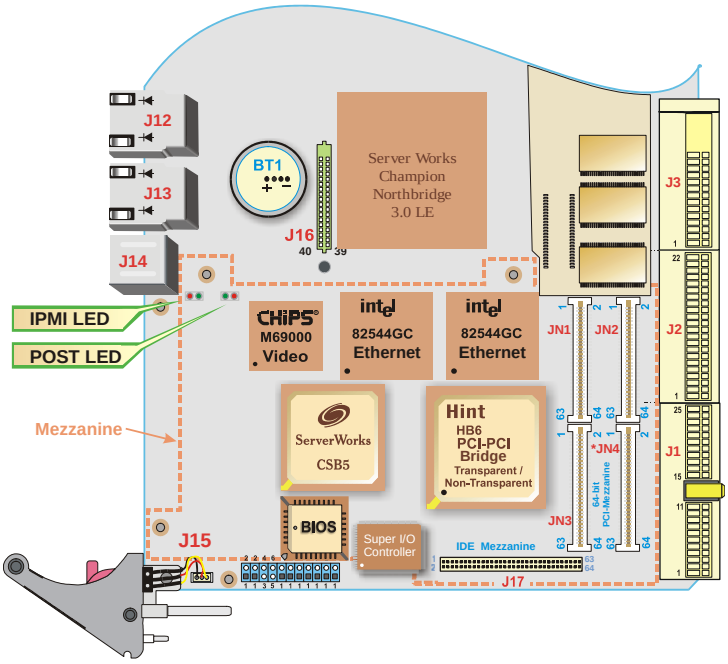
Phoenix Boot Utilities are : Phoenix QuietBoot™
Phoenix MultiBoot™

Phoenix QuietBoot displays a graphic illustration rather than the traditional POST messages while keeping you informed of diagnostic problems.

Phoenix MultiBoot is a boot screen that displays a selection of boot devices from which you can boot your operating system.

4.1.2.10. POST and IPMI Leds

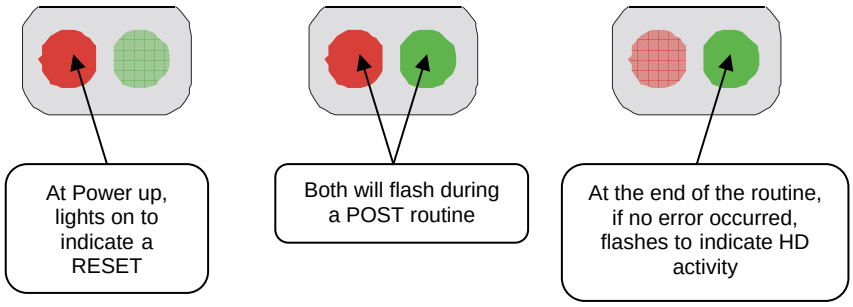
POST and IPMI leds locations



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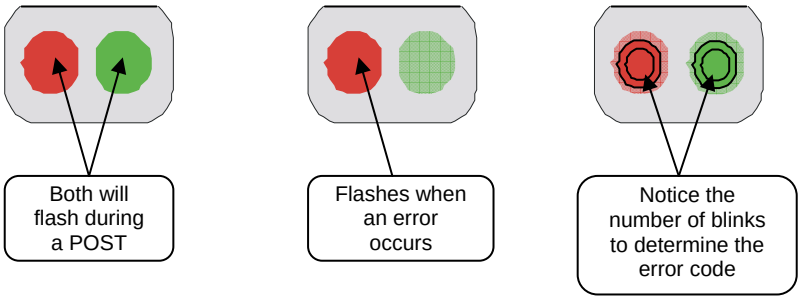
POST LED

The following figure indicates the sequence that the debug LED will perform from the beginning of a power up until it reaches the end of a POST routine.



At the beginning of each POST routine, the debug LED lights YELLOW (both LEDs light on). If the BIOS detects an error condition, it halts POST after issuing an error post debug code and the LED will light RED indicating an error.

Soon afterward, the debug LED will flash RED then GREEN. Notice the number of time it flashes RED and GREEN and use these counts during troubleshooting to establish at what point the system failed and what routine was being performed.



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IPMI LED

This table explain how the IPMI led is working.

Led Color	**RED**		**GREEN**	
Normal status	**OFF**		**SLOW BLINKING**	
Blinking speed	Slow (100 msec ON; 1.4 sec OFF)	Fast 8 x (150 msec ON; 50 msec OFF)	Slow (250 msec ON; 3 sec OFF)	Fast 8 x (150 msec ON; 50 msec OFF)
Signification	The IPMI wants to communicate with the SMS/SMM but doesn't get an answer from it.	A package is transmit or receive on the IPMB bus	The IPMI firmware is running normally; it's a heart beat	A package is transmit or receive from the KCS interface

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4.1.2.11. Phoenix Quiet Boot

Right after you turn on or reset the computer, Phoenix QuietBoot displays the QuietBoot Screen, a graphic illustration created by the computer manufacturer instead of the text-based POST screen, which displays a number of PC diagnostic messages.

To exit the QuietBoot screen and run Setup, display the Multiboot menu, or simply display the PC diagnostic messages, you can simply press one of the hot keys described below.

The QuietBoot Screen stays up until just before the operating system loads unless:

- You press <ESC> to display the POST screen.
- You press <Del> to enter Setup.
- POST issues an error message.
- The BIOS or an option ROM requests keyboard input.

The following explains each of these situations.

4.1.2.12. Press <ESC>

1. Pressing <ESC> switches the POST screen and the boot process continues with the text-based POST screen until the end of POST, and then displays the BootFirst Menu, with these options:
1. Load the operating system from a boot device of your choice.
2. Enter Setup.
3. Exit the Boot First Menu (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.

4.1.2.13. Press <Del>

Pressing < Del > at any time during POST enter Setup.

4.1.2.14. POST Error

Whenever POST detects a non-fatal error, QuietBoot switches to the POST screen and displays the errors. It then displays this message:

Press <F1> to resume, <Del> to Setup

Press <F1> to continue with the boot. Press <Del> if you want to correct the error in Setup.

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4.1.2.14.1. **PhoenixBIOS 4.0 Release 6.0,** POST Tasks and Beep Codes

When you turn on or reset an IBM- compatible PC, the BIOS first performs a number of tasks, called the **Power- On- Self- Test** (**POST**). These tasks test and initialize the hardware and then boot the Operating System from the hard disk. At the beginning of each POST task, the BIOS outputs the **test- point error code** to I/ O port 80h. Programmers and technicians use this code during trouble shooting to establish at what point the system failed and what routine was being performed. Some motherboards are equipped with a seven-segment LED display that displays the current value of port 80h. For production boards which do not contain the LED display, you can purchase an installable "Port 80h" card that performs the same function. If the BIOS detects a terminal error condition, it issues a terminal- error beep code (See following), attempts to display the error code on upper left corner of the screen and on the port 80h LED display, and halts POST. It attempts repeatedly to write the error to the screen. This attempt may "hash" some CGA displays.
If the system hangs before the BIOS can process the error, the value displayed at the port 80h is the last test performed. In this case, the screen does not display the error code.

4.1.2.14.2. Terminal POST Errors

There are several POST routines that require success to finish POST. If they fail, they issue a **POST Terminal Error** and shut down the system. Before shutting down the system, the error handler issues a beep code signifying the test point error, writes the error to port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both mono and color adapters). The routine drives the beep code from the test point error as follows:

1. The 8- bit error code is broken down to four 2- bit groups.
2. Each group is made one- based (1 through 4) by adding 1.
3. Short beeps are generated for the number in each group.

Example: **Testpoint 16h = 00 01 01 10 = 1- 2- 2- 3 beeps**

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4.1.2.14.3. POST Task Routines

The following is a list of the Test Point codes written to port 80h at the start of each routine, the beep codes issued for terminal errors, and a description of the POST routine. Unless otherwise noted, these codes are valid for PhoenixBIOS 4.0 Release 6.0.

NOTE: The following routines are sorted by their test point numbers assigned in the BIOS code. Their actual order as executed during POST can be quite different.

02h Verify Real Mode	03h Disable Non- Maskable Interrupt (NMI)
04h Get CPU type	06h Initialize system hardware
08h Initialize chipset with initial POST values	09h Set IN POST flag
0Ah Initialize CPU registers	0Bh Enable CPU cache
0Ch Initialize caches to initial POST values	0Eh Initialize I/ O component
0Fh Initialize the local bus IDE	10h Initialize Power Management
11h Load alternate registers with initial POST values	12h Restore CPU control word during warm boot
13h Initialize PCI Bus Mastering devices	14h Initialize keyboard controller
16h 1- 2- 2- 3 BIOS ROM checksum	17h Initialize cache before memory autosize
18h 8254 timer initialization	1Ah 8237 DMA controller initialization
1Ch Reset Programmable Interrupt Controller	20h 1- 3- 1- 1 Test DRAM refresh
22h 1- 3- 1- 3 Test 8742 Keyboard Controller	24h Set ES segment register to 4 GB
26h Enable A20 line	28h Autosize DRAM
29h Initialize POST Memory Manager	2Ah Clear 512 KB base RAM
2Ch 1- 3- 4- 1 RAM failure on address line ***xxxx*** *	2Eh 1- 3- 4- 3 RAM failure on data bits ***xxxx*** * of low byte of memory bus
2Fh Enable cache before system BIOS shadow	30h 1- 4- 1- 1 RAM failure on data bits ***xxxx*** * of high byte of memory bus
32h Test CPU bus- clock frequency	33h Initialize Phoenix Dispatch Manager
36h Warm start shut down	38h Shadow system BIOS ROM
3Ah Autosize cache	3Ch Advanced configuration of chipset registers
3Dh Load alternate registers with CMOS values	42h Initialize interrupt vectors
45h POST device initialization	46h 2- 1- 2- 3 Check ROM copyright notice
48h Check video configuration against CMOS	49h Initialize PCI bus and devices
4Ah Initialize all video adapters in system	4Bh QuietBoot start (optional)
4Ch Shadow video BIOS ROM	4Eh Display BIOS copyright notice
50h Display CPU type and speed	51h Initialize EISA board
52h Test keyboard	54h Set key click if enabled
58h 2- 2- 3- 1 Test for unexpected interrupts	59h Initialize POST display service
5Ah Display prompt "Press F2 to enter SETUP"	5Bh Disable CPU cache
5Ch Test RAM between 512 and 640 KB	60h Test extended memory
62h Test extended memory address lines	64h Jump to UserPatch1
66h Configure advanced cache registers	67h Initialize Multi Processor APIC
68h Enable external and CPU caches	69h Setup System Management Mode (SMM) area
6Ah Display external L2 cache size	6Bh Load custom defaults (optional)

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Test Point codes (continued)

6Ch Display shadow- area message	6Eh Display possible high address for UMB recovery
70h Display error messages	72h Check for configuration errors
76h Check for keyboard errors	7Ch Set up hardware interrupt vectors
7Eh Initialize coprocessor if present	80h Disable on-board Super I/ O ports and IRQs
81h Late POST device initialization	82h Detect and install external RS232 ports
83h Configure non- MCD IDE controllers	84h Detect and install external parallel ports
85h Initialize PC- compatible PnP ISA devices	86h Re- initialize on-board I/ O ports.
87h Configure Motheboard Configurable Devices (optional)	88h Initialize BIOS Data Area
89h Enable Non- Maskable Interrupts (NMIs)	8Ah Initialize Extended BIOS Data Area
8Bh Test and initialize PS/ 2 mouse	8Ch Initialize floppy controller
8Fh Determine number of ATA drives (optional)	90h Initialize hard- disk controllers
91h Initialize local- bus hard- disk controllers	92h Jump to UserPatch2
93h Build MPTABLE for multi- processor boards	95h Install CD ROM for boot
96h Clear huge ES segment register	97h Fixup Multi Processor table
98h 1- 2 Search for option ROMs. One long, two short beeps on	checksum failure
99h Check for SMART Drive (optional)	9Ah Shadow option ROMs
9Ch Set up Power Management	9Dh Initialize security engine (optional)
9Eh Enable hardware interrupts	9Fh Determine number of ATA and SCSI drives
A0h Set time of day	A2h Check key lock
A4h Initialize Typematic rate	A8h Erase F2 prompt
AAh Scan for F2 key stroke	ACh Enter SETUP
AEh Clear Boot flag	B0h Check for errors
B2h POST done - prepare to boot operating system	B4h 1 One short beep before boot
B5h Terminate QuietBoot (optional)	B6h Check password (optional)
B9h Prepare Boot	BAh Initialize DMI parameters
BBh Initialize PnP Option ROMs	BCh Clear parity checkers
BDh Display MultiBoot menu	BEh Clear screen (optional)
BFh Check virus and backup reminders	C0h Try to boot with INT 19
C1h Initialize POST Error Manager (PEM)	C2h Initialize error logging
C3h Initialize error display function	C4h Initialize system error handler
C5h PnPnd dual CMOS (optional)	C6h Initialize notebook docking (optional)
C7h Initialize notebook docking late	C8h Force check (optional)
C9h Extended checksum (optional)	D2h Unknown interrupt
E0h Initialize the chipset	E1h Initialize the bridge
E2h Initialize the CPU	E3h Initialize system timer
E4h Initialize system I/ O	E5h Check force recovery boot
E6h Checksum BIOS ROM	E7h Go to BIOS
E8h Set Huge Segment	E9h Initialize Multi Processor
EAh Initialize OEM special code	EBh Initialize PIC and DMA
ECh Initialize Memory type	EDh Initialize Memory size
EEh Shadow Boot Block	EFh System memory test
F0h Initialize interrupt vectors	F1h Initialize Run Time Clock
F2h Initialize video	F3h Initialize System Management Mode
F4h 1 Output one beep before boot	F5h Boot to Mini DOS
F6h Clear Huge Segment	F7h Boot to Full DOS

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* If the BIOS detects error 2C, 2E, or 30 (base 512K RAM error), it displays an additional word- bitmap (***xxxx***) indicating the address line or bits that failed. For example, "2C 0002" means address line 1 (bit one set) has failed. "2E 1020" means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16 rather than 32- bit bus. The BIOS also sends the bitmap to the port- 80 LED display. It first displays the check point code, followed by a delay, the high- order byte, another delay, and then the low- order byte of the error. It repeats this sequence continuously.

4.1.2.15. Keyboard Input Request

If the BIOS or an Option ROM (add-on card) requests keyboard input, QuietBoot switches over to the POST screen and the Option ROM displays prompts for entering the information. POST continues from there with the regular POST screen.

4.1.2.16. Phoenix Multiboot

Phoenix Multiboot expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, or CDROM. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in **The Boot First Menu**.
Multiboot consist of :

The Setup Boot Menu
The Boot First Menu

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4.2. INSTALLING DRIVERS

4.2.1. Video Drivers

Various drivers are provided for different operating systems and software. To install a driver, refer to the Setup program located on the CD-ROM (provided with your board).

4.2.2. Ethernet Drivers

Various drivers are provided for different operating systems and software. To install a driver, use the Setup program and the ReadMe.txt file located on the CD-ROM (provided with your board).

4.2.3. Other Drivers

For other operating system drivers and installation instructions or for more information, contact Kontron's Technical Support department.

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4.3. CONSOLE REDIRECTION (VT100 MODE)

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.3.1. Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix© or Procom© can also be used.

4.3.2. Setup & Configuration

Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the "Advanced" page, "Console Redirection" menu.
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

> ■ **NOTE**
>
> If you do not require a full cable for your terminal, you can set up a partial cable by using only the TxD and RxD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Install the VT100 jumper. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.

Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.

Console Redirection is done by refreshing the Video address @ B8000h at the selected BAUD rate. This means that a low baud rate refreshes the screen slowly, but the CPU time is maximized for the applications. A high BAUD rate refreshes the screen rapidly but the CPU is frequently interrupted by the Serial Port.

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Console Redirection provided by Phoenix based BIOS offers various escape sequences to emulate keyboard function keys. The following table lists the escape sequences available.

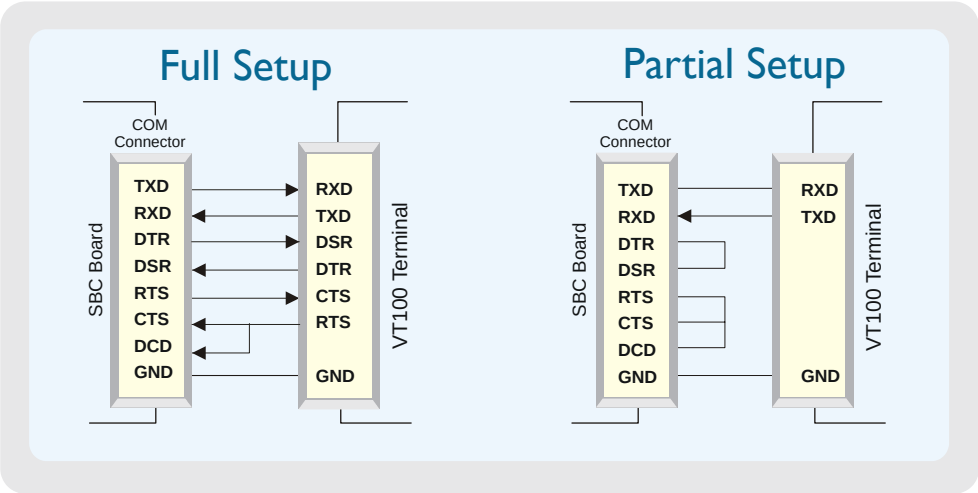
Escape sequence	Function		Escape sequence	Function
Esc Del	Warm Reset		Esc [6 4 ~	(Ctrl-F1)
Esc O P	F1		Esc [6 5 ~	(Ctrl-F2)
Esc O Q	F2		Esc [6 6 ~	(Ctrl-F3)
Esc O R	F3		Esc [6 7 ~	(Ctrl-F4)
Esc O S	F4		Esc [6 8 ~	(Ctrl-F5)
Esc O w	F3		Esc [6 9 ~	(Ctrl-F6)
Esc O x	F4		Esc [7 0 ~	(Ctrl-F7)
Esc O t	F5		Esc [7 1 ~	(Ctrl-F8)
Esc O u	F6		Esc [7 2 ~	(Ctrl-F9)
Esc O q	F7		Esc [7 3 ~	(Ctrl-F10)
Esc O r	F8		Esc [7 4 ~	(Ctrl-F11)
Esc O p	F10		Esc [7 5 ~	(Ctrl-F12)

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4.1.1 Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bauds.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the on-board video.



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PART 5

APPENDICES

A. MEMORY & I/O MAPS

B. INTERRUPT LINES

C. BOARD DIAGRAMS

D. CONNECTOR PINOUTS

E. BIOS SETUP ERROR CODES

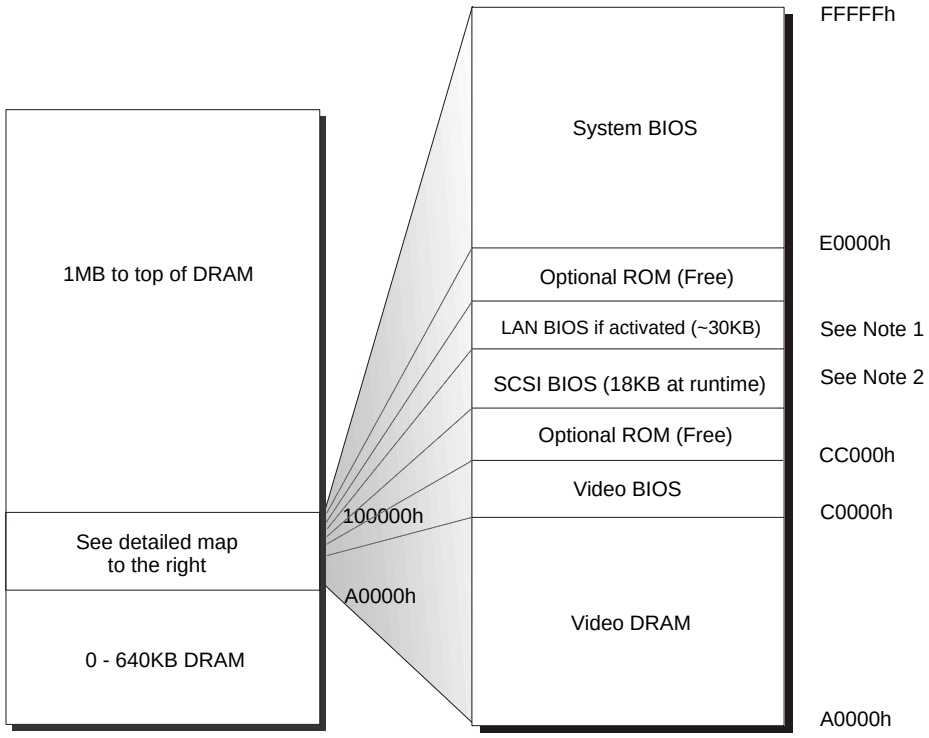
F. BIOS UPDATE & EMERGENCY PROCEDURE

G. GETTING HELP & RMA

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A. MEMORY & I/O MAPS

A.1 MEMORY MAPPING



Note 1 : LAN BIOS address may vary

Note 2 : SCSI BIOS address may vary.
Size is only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-FFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
E0000-FFFFF	System BIOS
100000-Top of DRAM	1 MB - Top of DRAM

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A.2 I/O MAPPING

Address	Optional Address	Function
000-01F		DMA Controller 1
020-03F		Interrupt Controller 1
040-05F		Timer
060-06F		Keyboard
070-07F		Real-time clock
080-09F		DMA Page Register
0A0-0BF		Interrupt Controller 2
0C0-0DF		DMA Controller 2
0F0-0F1, 0F8-0FF		Math Coprocessor
190-197		Kontron Control Port
1F0-1F7, 3F6		Primary IDE
170-177, 376		Secondary IDE
3F0-3F7	370-377	Floppy Disk
3F8-3FF (COM1)	2F8-2FF (COM2)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB		Graphics Controller (I2C Port)

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B. INTERRUPT LINES

B.1 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard (Output Buffer Full)	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Available [1]	IRQ 13	Coprocessor Error
IRQ *6	Floppy Controller	IRQ 14	Primary IDE * or available [1]
IRQ 7*	Available [1]	IRQ 15	Secondary IDE * or available [1]

* :All functions marked with an asterisk (*) can be disabled or reconfigured.
1 Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

B.2 DMA CHANNELS

The cPCI-DT64 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

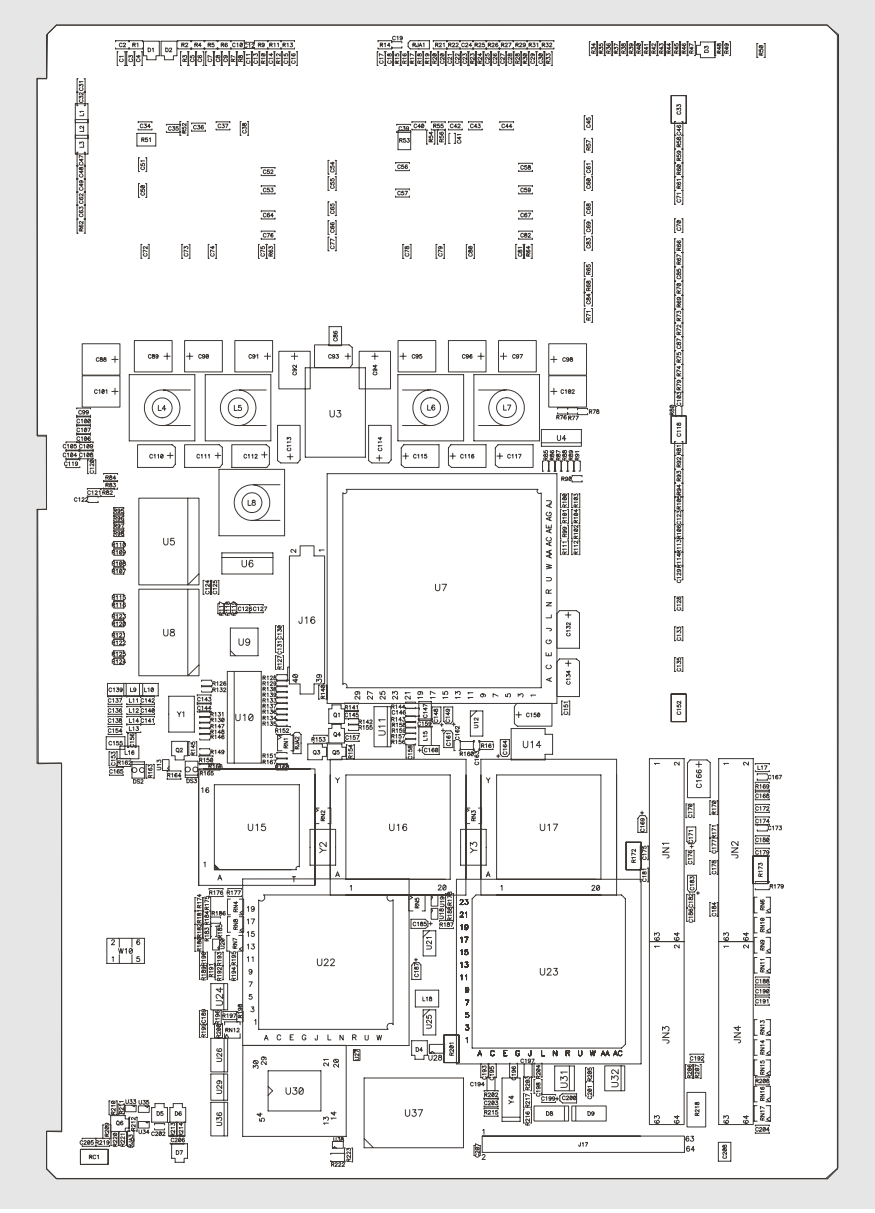
Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

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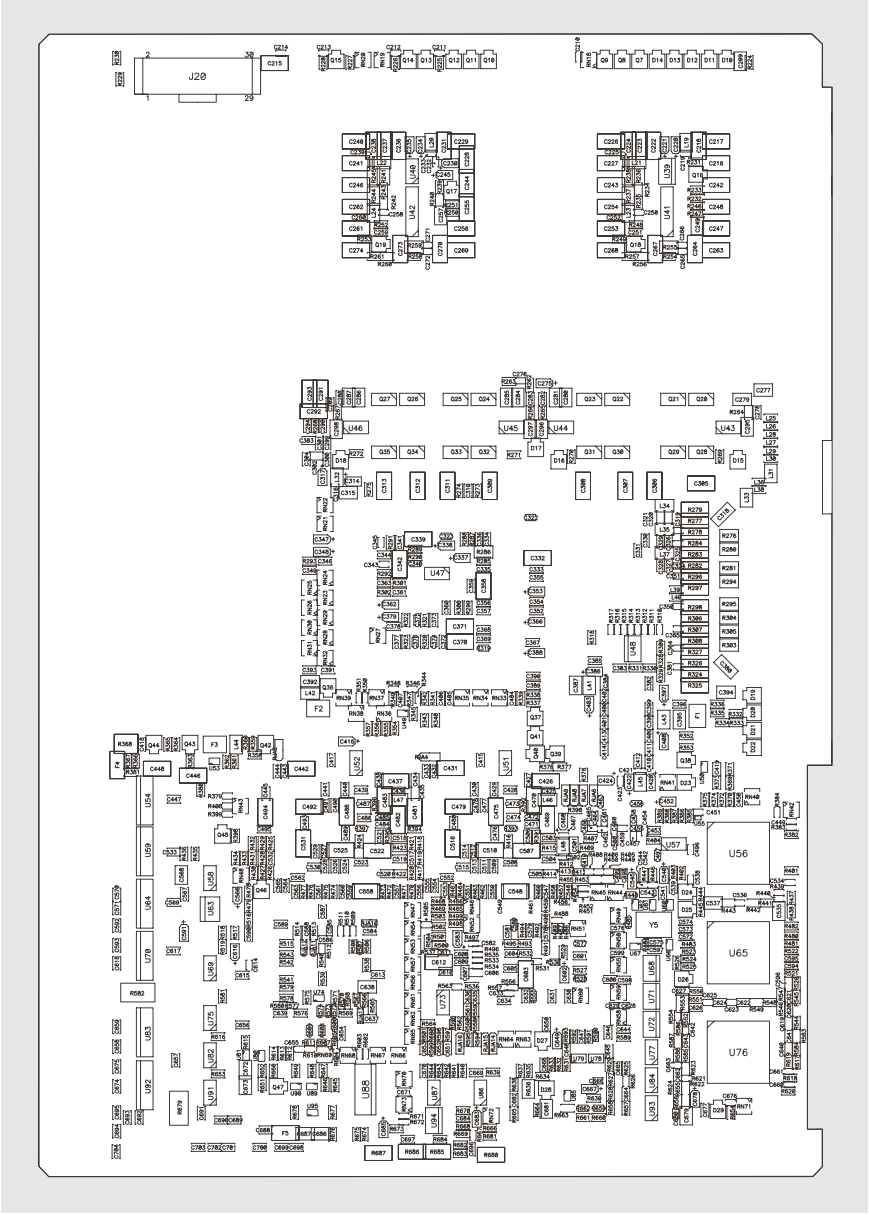
C. BOARD DIAGRAMS

C.1 TOP DEVICES SURFACE MOUNT



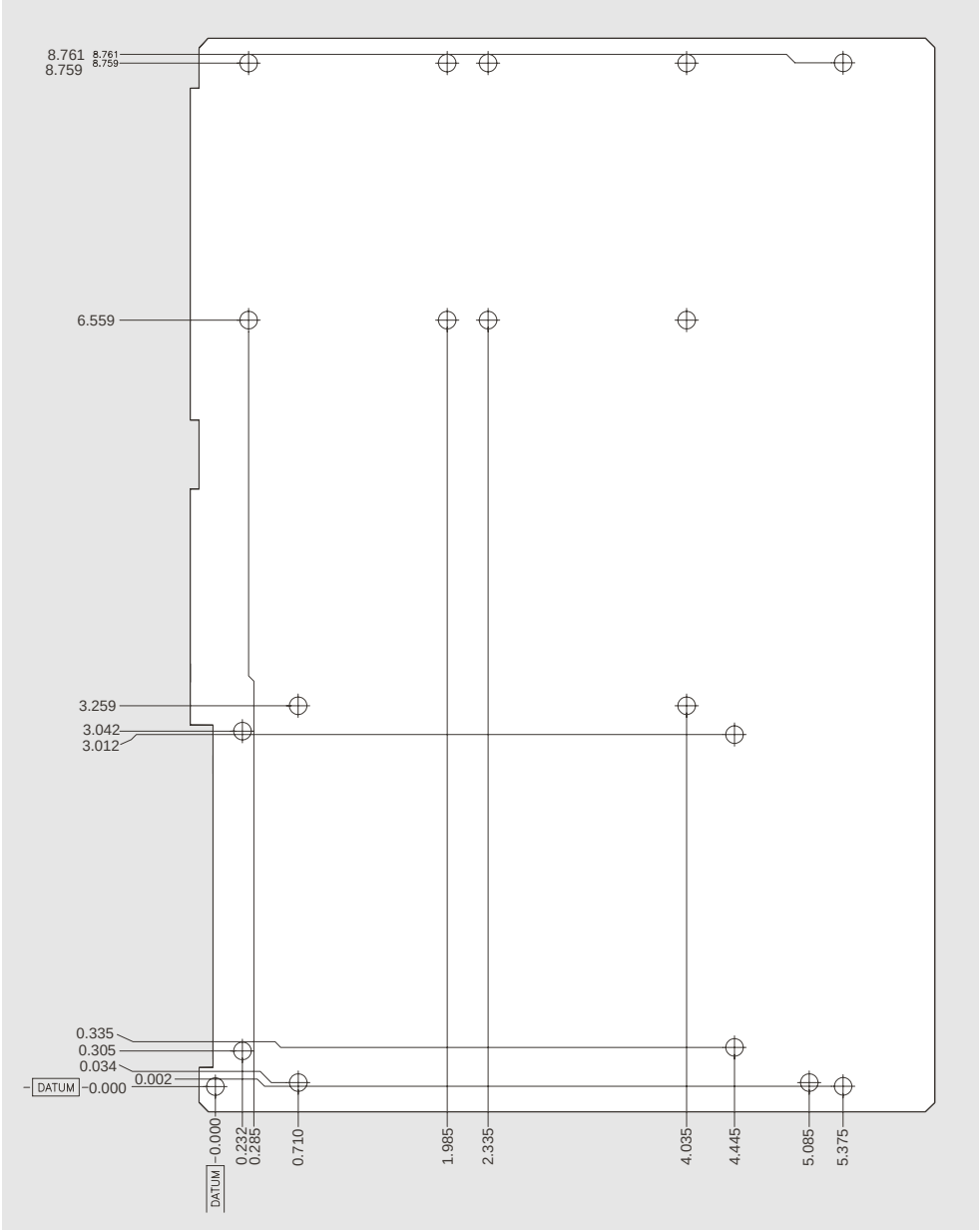
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C.2 BOTTOM DEVICE SURFACE MOUNT



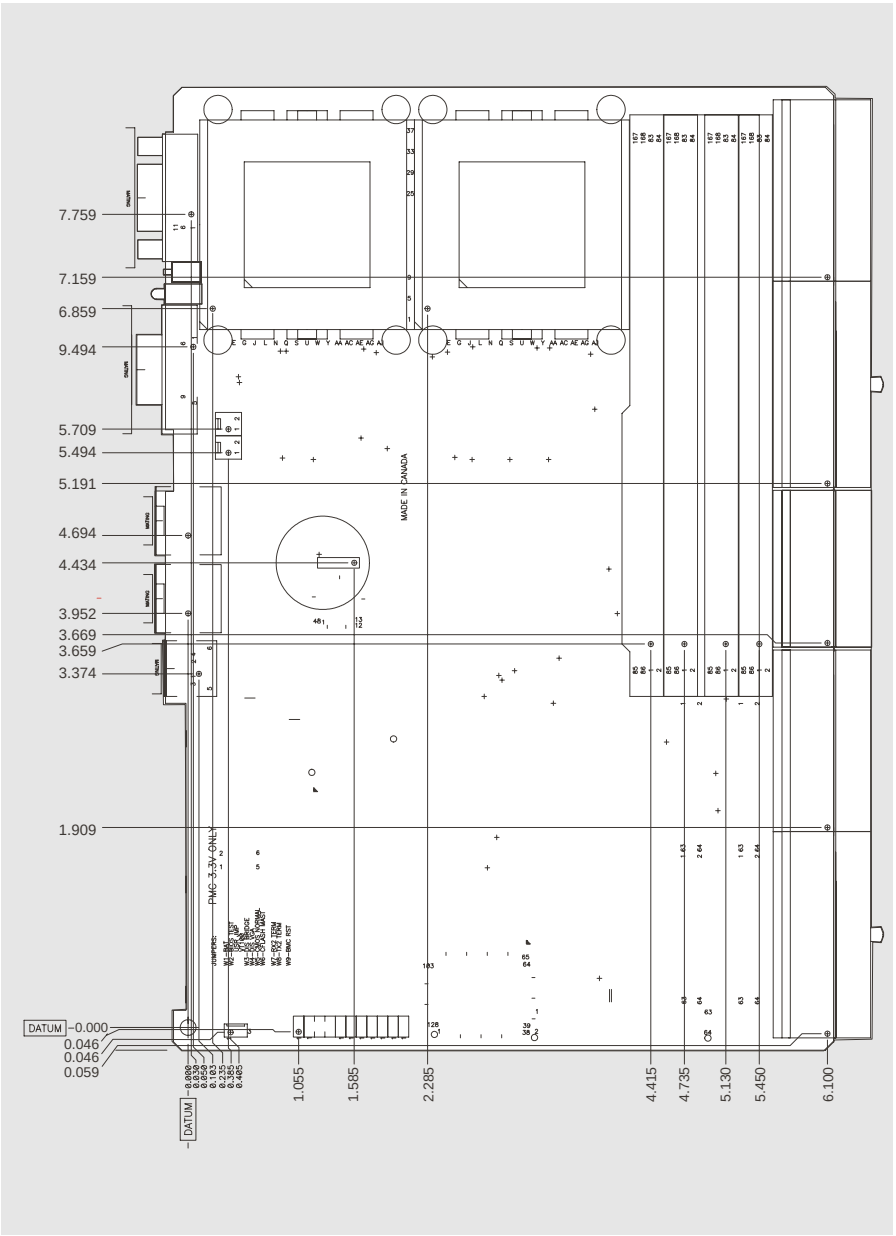
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C.3 MOUNTING HOLES



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C.4 TOP MOUNTING COMPONENTS



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D. CONNECTOR PINOUTS

D.1 cPCI- DT64 CONNECTORS AND HEADERS

Connector #	Description
J1	CPCI Bus connector
J2	CPCI Bus connector
J3	CPCI I/O connector
J4	CPCI I/O connector
J5	CPCI I/O connector
J6-J9	DIMM Sockets
J10	CRT VGA Connector (Front panel configuration only)
J11	Serial Port 1 – RS-232 (Front panel configuration only)
J12, J13	Ethernet LAN2 and LAN1 connectors (Front panel configuration only)
J14	PS/2 Keyboard and Mouse connector
J15	Hot Swap switch
J16	CompactFlash
J17	IDE Mezzanine card
JN1 –JN4	64Bit/66MHz mezzanine
SW1	Reset switch
BT1	CMOS Battery Backup connector

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D.2 J1 cPCI Bus

	ROW A	ROW B	ROW C	ROW D	ROW E
1	VCC5E	-12VE	RSV	+12VE	VCCE
2	RSV	VCCE	RSV	RSV	RSV
3	INTA#	INTB#	INTC#	VCCE	INTD#
4	IPMB0_PWR	HEALTHY#	VI/O	INTP	INTS
5	RSV	RSV	RST#	GND	GNT0#
6	REQ0#	PCI_PRESENT#	VCC3E	CLK0	AD31
7	AD30	AD29	AD28	GND	AD27
8	AD26	GND	VI/O	AD25	AD24
9	CBE3#	IDSEL	AD23	GND	AD22
10	AD21	GND	VCC3E	AD20	AD19
11	AD18	AD17	AD16	GND	CBE2#
12 13 14	**KEY AREA**				
15	VCC3E	FRAME#	IRDY#	BD_SEL#	TRDY#
16	DEVSEL#	PCIXCAP	VI/O	STOP#	LOCK#
17	VCC3E	IPMB0_SCL	IPMB0_SDA	GND	PERR#
18	SERR#	GND	VCC3E	PAR	CBE1#
19	VCC3E	AD15	AD14	GND	AD13
20	AD12	GND	VI/O	AD11	AD10
21	VCC3E	AD9	AD8	M66EN	CBE0#
22	AD7	GND	VCC3E	AD6	AD5
23	VCC3E	AD4	AD3	VCCE	AD2
24	AD1	VCCE	VI/O	AD0	ACK64#
25	VCCE	REQ64#	ENUM#	VCC3E	VCCE

Active Low

Long pins : 3D, 4C,5D, 6C, 7D, 9D, 10D, 17D, 19D, 22C, 23D, 24C

Short pins : 9B, 15D

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D.3 J2 cPCI Bus

	ROW A	ROW B	ROW C	ROW D	ROW E
1	S_CLK1	GND	REQ1#	GNT1#	REQ2#
2	S_CLK2	S_CLK3	SYSEN#	GNT2#	REQ3#
3	S_CLK4	GND	GNT3#	REQ4#	GNT4#
4	V I/O	RSV	CBE7#	GND	CBE6#
5	CBE5#	64_EN#	V I/O	CBE4#	PAR64
6	AD63	AD62	AD61	GND	AD60
7	AD59	GND	V I/O	AD58	AD57
8	AD56	AD55	AD54	GND	AD53
9	AD52	GND	V I/O	AD51	AD50
10	AD49	AD48	AD47	GND	AD46
11	AD45	GND	V I/O	AD44	AD43
12	AD42	AD41	AD40	GND	AD39
13	AD38	GND	V I/O	AD37	AD36
14	AD35	AD34	AD33	GND	AD32
15	RSV	GND	FAL#	REQ5#	GNT5#
16	RSV	RSV	DEG#	GND	RSV
17	RSV	GND	PRST#	REQ6#	GNT6#
18	RSV	RSV	RSV	GND	RSV
19	GND	GND	IMPB1_SDA	IMPB1_SCL	IMPB1_ALERT#
20	S_CLK5	GND	RSV	GND	RSV
21	S_CLK6	GND	RSV	RSV	RSV
22	GA4	GA3	GA2	GA1	GA0

Active Low

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D.4 J3 cPCI Bus

	ROW A	ROW B	ROW C	ROW D	ROW E
1	COM1:RTS	COM1:RX	COM1:DSR	COM1:DCD	ID1
2	COM1:RI	COM1:DTR	COM1:CTS	COM1:TX	MOUSE:CLK
3	COM2:RTS	COM2:RX	COM2:DSR	COM2:DCD	MOUSE:DATA
4	COM2:RI	COM2:DTR	COM2:CTS	COM2:TX	KB:DATA
5	VGA:BLUE	VGA:HSYNC	VGA:VSYNC	VGA:SCL	KB:CLK
6	VGA:RED	VGA:GREEN	VGA:SDA	POST:CLK	POST:DATA
7	ID0	ID2	ID3	ID4	SPEAKER
8	USB0:DATA-	USB0:DATA+	RSV	RSV	RSV
9	USB1:DATA-	USB1:DATA+	RSV	RSV	RSV
10	USB1:VCC	USB0:VCC	RSV	RSV	RSV
11	RSV	RSV	RSV	RSV	RSV
12	RSV	RSV	RSV	RSV	RSV
13	LAN0:ACT	LAN1:ACT	RSV	RSV	RSV
14	LAN0:LINK	LAN1:LINK	LAN:CT	RSV	RSV
15	LAN1:DB+	LAN1:DB-	GND	LAN1:DD+	LAN1:DD-
16	LAN1:DA+	LAN1:DA-	GND	LAN1:DC+	LAN1:DC-
17	LAN0:DB+	LAN0:DB-	GND	LAN0:DD+	LAN0:DD-
18	LAN0:DA+	LAN0:DA-	GND	LAN0:DC+	LAN0:DC-
19	VCC	VCC	VCC3	+12V	-12V

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D.5 J4 cPCI Bus (PIM)

		ROW A	ROW B	ROW C	ROW D	ROW E
1		PIM:61	PIM:63	GND	PIM:62	PIM:64
2		PIM:57	PIM:59	GND	PIM:58	PIM:60
3		GND	GND	GND	GND	GND
4		PIM:53	PIM:55	GND	PIM:54	PIM:56
5		PIM:49	PIM:51	GND	PIM:50	PIM:52
6		GND	GND	GND	GND	GND
7		PIM:45	PIM:47	GND	PIM:46	PIM:48
8		PIM:41	PIM:43	GND	PIM:42	PIM:44
9		GND	GND	GND	GND	GND
10		PIM:37	PIM:39	GND	PIM:38	PIM:40
11		PIM:33	PIM:35	GND	PIM:34	PIM:36
12 13 14		**KEY AREA**				
15		PIM:29	PIM:31	GND	PIM:30	PIM:32
16		PIM:25	PIM:27	GND	PIM:26	PIM:28
17		GND	GND	GND	GND	GND
18		PIM:21	PIM:23	GND	PIM:22	PIM:24
19		PIM:17	PIM:19	GND	PIM:18	PIM:20
20		GND	GND	GND	GND	GND
21		PIM:13	PIM:15	GND	PIM:14	PIM:16
22		PIM:9	PIM:11	GND	PIM:10	PIM:12
23		N.C.	VCC	GND	N.C.	VCC3
24		PIM:5	PIM:7	GND	PIM:6	PIM:8
25		PIM:1	PIM:3	GND	PIM:2	PIM:4

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D.6 J4 cPCI Bus (SCSI)

	ROW A	ROW B	ROW C	ROW D	ROW E
1	D12+	D12-	GND	D13+	D13-
2	D14+	D14-	GND	D15+	D15-
3	GND	GND	GND	GND	GND
4	DPH+	DPH-	GND	D0+	D0-
5	D1+	D1-	GND	D2+	D2-
6	GND	GND	GND	GND	GND
7	D3+	D3-	GND	D4+	D4-
8	D5+	D5-	GND	D6+	D6-
9	GND	GND	GND	GND	GND
10	D7+	D7-	GND	DPL+	DPL-
11	DIFFSENS	TERMPWR7	GND	TERMPWR8	TERMPWR9
12 13 14					
15	TERMPWR3	TERMPWR4	GND	TERMPWR5	TERMPWR6
16	TERMPWR1	TERMPWR2	GND	ATN+	ATN-
17	GND	GND	GND	GND	GND
18	BSY+	BSY-	GND	ACK+	ACK-
19	RST+	RST-	GND	MSG+	MSG-
20	GND	GND	GND	GND	GND
21	SEL+	SEL-	GND	CD+	CD-
22	REQ+	REQ-	GND	IO+	IO-
23	N.C.	VCC	GND	N.C.	VCC3
24	D8+	D8-	GND	D9+	D9-
25	D10+	D10-	GND	D11+	D11-

Active Low

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D.7 J5 cPCI Bus

		ROW A	ROW B	ROW C	ROW D	ROW E
1		RSV	RSV	GND	RSV	RSV
2		RSV	RSV	GND	RSV	RSV
3		RSV	RSV	GND	RSV	RSV
4		RSV	RSV	GND	RSV	RSV
5		RSV	RSV	GND	RSV	RSV
6		RSV	RSV	GND	RSV	RSV
7		RSV	RSV	GND	RSV	RSV
8		RSV	RSV	GND	RSV	RSV
9		RSV	RSV	GND	RSV	RSV
10		FD:MSEN0	FD:MSEN1	GND	RSV	RSV
11		FD: MTR0#	FD: INDEX#	GND	FD: FDEDIN#	FD: DENSEL#
12		FD: DIR#	FD: MTR1#	GND	FD: DSEL0#	FDE: DSEL1#
13		FD: TRK0#	FD: WGATE#	GND	FD: WDATA#	FD: STEP#
14		FD: DSKCHG#	FD: HDSEL#	GND	FD: RDATA#	FD: WRPROT#
15		IDE1:D6	IDE1:D8	GND	IDE1:D7	IDE1:RESET#
16		IDE1:D4	IDE1:D10	GND	IDE1:D5	IDE1:D9
17		IDE1:D2	IDE1:D12	GND	IDE1:D3	IDE1:D11
18		IDE1:D0	IDE1:D14	GND	IDE1:D1	IDE1:D13
19		IDE1:IOR#	IDE1:IOW#	GND	IDE1:DMARQ	IDE1:D15
20		IDE1:IOCS16#	IDE1:IRQ	GND	IDE1:DMACK#	IDE1:IORDY
21		IDE1:A2	IDE1:A0	GND	IDE1:A1	IDE1:PDIAG#
22		IDE1:ACT#	IDE1:CS1#	GND	IDE1:CS0#	RSV

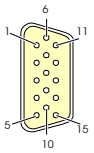
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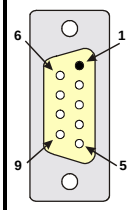
D.8 J10, VIDEO (VGA)

Signal		Signal		Signal	
RED	1	Analog GND	6	N/C	11
GREEN	2	Analog GND	7	SDATA	12
BLUE	3	Analog GND	8	HSYNC	13
N/C	4	N/C	9	VSYNC	14
GND	5	GND	10	SCLK	15

Top View



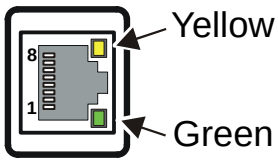
D.9 J11, SERIAL PORT 1 - RS-232

Pin Number		Top View	Pin Number	
Signal				Signal
DSR	6		1	DCD
RTS	7		2	RXD
CTS	8		3	TXD
RI	9		4	DTR
			5	GND

D.10 J12, J13, ETHERNET LAN 2 AND LAN 1

Signal	
DA+	1
DA-	2
DB+	3
DC+	4
DC-	5
DB-	6
DD+	7
DD-	8

Top View



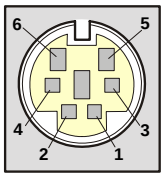
Note
These two LEDs might be reversed.

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D.11 J14, PS/2 MOUSE & KEYBOARD

Signal	Pin
KB:DATA	1
MOUSE:DATA	2
GND	3
VCC	4
KB:CLK	5
MOUSE:CLK	6

Front View

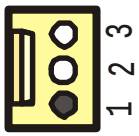


(Connector front view)

D.12 J15, HOT SWAP SWITCH

Signal	Pin
VCC3E	1
SW_OPEN#	2
SW_CLOSE#	3

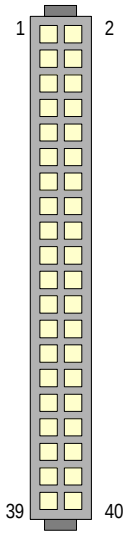
Top View



D.13 J16, COMPACTFLASH DISK

Pin Number	Signal
1	D11
3	D12
5	D13
7	D14
9	D15
11	CS1#
13	DMACK#
15	DMARQ
17	PDIAG#
19	IRQ14
21	VCC
23	GND
25	RESET#
27	CSEL
29	A1
31	A0
33	D0
35	D1
37	D2
39	IOCS16#

Top View



Pin Number	Signal
2	GND
4	D3
6	D4
8	D5
10	D6
12	D7
14	CS0#
16	DIOR#
18	DIOW#
20	VCC
22	VCC
24	GND
26	GND
28	A2
30	ACT#
32	IORDY
34	D8
36	D9
38	D10
40	GND

Active Low

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D.14 J17 – IDE MEZZANINE

Pin Number	Signal	Top View	Pin Number	Signal
1	P64GNT#_MEZ2		2	IPMB0_SDA
3	GND		4	IPMB0_SCL
5	CLK66_MEZ		6	GND
7	GND		8	CLK66_PMC_8HP
9	P64REQ#_MEZ		10	GND
11	P64GNT#_MEZ		12	INTB_P64MEZZ#
13	INT_BRDG_MEZ		14	INTA_P64MEZZ#
15	INTD_P64MEZZ#		16	MEZZ_ENUM#
17	INTC_P64MEZZ#		18	IDE0:MS#/SLV
19	P64REQ#_MEZ2		20	IDE0:ACT#
21	IDE0:CS1#		22	GND
23	IDE0:DA2		24	IDE0:CS0#
25	GND		26	IDE0:DA0
27	IDE0:PDIAG#		28	GND
29	IDE0:DA1		30	IDE0:IRQ
31	GND		32	IDE0:DMACK#
33	IDE0:IORDY		34	GND
35	IDE0:IOR#		36	IDE0:IOW#
37	BD_SEL_MEZZ#		38	IDE0:DMARQ
39	IDE0:D0		40	HEALTHY#_BP
41	IDE0:D1		42	IDE0:D15
43	VCC		44	IDE0:D14
45	IDE0:D2		46	VCC
47	IDE0:D3		48	IDE0:D13
49	VCC		50	IDE0:D12
51	IDE0:D4		52	VCC
53	IDE0:D5		54	IDE0:D11
55	VCC		56	IDE0:D10
57	IDE0:D6		58	VCC
59	IDE0:D7		60	IDE0:D9
61	VCC		62	IDE0:D8
63	IDE:RESET#		64	VCC

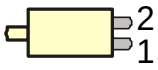
Active Low

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D.15 SW1 – RESET SWITCH

Signal	Pin
GND	1
RESET#	2

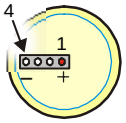
Side View



D.16 BT1, CMOS BATTERY BACKUP CONNECTOR

Signal	Pin
Battery (+)	1
Battery (-)	4

Front View

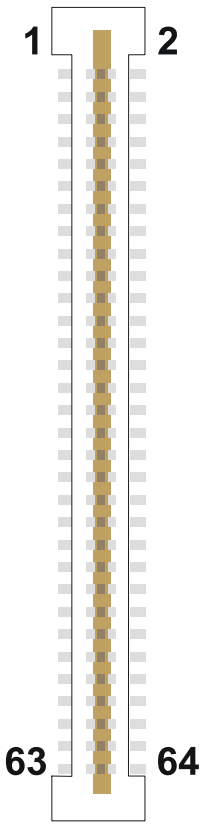


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D.17 JN1 – PIM (PCM64, J1)

Pin Number	Signal
1	N.C.
3	GND
5	INTB_P64PMC#
7	BUSMODE1#
9	INTD_P64PMC#
11	GND
13	CLK66_PMC
15	GND
17	P64REQ#_PMC
19	VCC
21	P64AD28
23	P64AD25
25	GND
27	P64AD22
29	P64AD19
31	VCC
33	P64FRAME#
35	GND
37	P64DEVSEL#
39	GND
41	RSV
43	P64PAR
45	VCC
47	P64AD12
49	AD9
51	GND
53	P64AD6
55	P64AD4
57	VCC
59	P64AD2
61	P64AD0
63	GND

Top View



Pin Number	Signal
2	-12V
4	INTA_P64PMC#
6	INTC_P64PMC#
8	VCC
10	N.C.
12	VCC3E
14	GND
16	P64GNT#_PMC
18	VCC
20	P64AD31
22	P64AD27
24	GND
26	P64C/BE#3
28	P64AD21
30	VCC
32	P64AD17
34	GND
36	P64IRDY#
38	VCC
40	P64LOCK#
42	SB0#
44	GND
46	P64AD15
48	P64AD11
50	VCC
52	P64C/CBE0#
54	P64AD5
56	GND
58	P64AD3
60	P64AD1
62	VCC
64	P64REQ64#

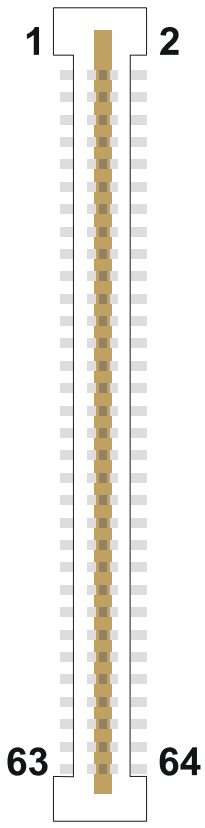
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D.18 JN2 – PIM (PCM64, J2)

Pin Number	Signal
1	+12V
3	RSV
5	RSV
7	GND
9	N.C.
11	BMODE2#
13	PCIRST#
15	VCC3
17	N.C.
19	P64AD30
21	GND
23	P64AD24
25	IDSEL_PMC
27	VCC3
29	P64AD18
31	P64AD16
33	GND
35	P64TRDY#
37	GND
39	P64PERR#
41	VCC3
43	P64C/BE1#
45	P64AD14
47	P64M66EN
49	P64AD8
51	P64AD7
53	VCC3
55	N.C.
57	N.C.
59	GND
61	P64ACK64#
63	GND

Top View



Pin Number	Signal
2	RSV
4	N.C.
6	GND
8	N.C.
10	N.C.
12	VCC3
14	BMODE3#
16	BMODE4#
18	GND
20	P64AD29
22	P64AD26
24	VCC3
26	P64AD23
28	P64AD20
30	GND
32	P64C/BE2#
34	N.C.
36	VCC3
38	P64STOP#
40	GND
42	P64SERR#
44	GND
46	P64AD13
48	P64AD10
50	VCC3
52	N.C.
54	N.C.
56	GND
58	N.C.
60	N.C.
62	VCC3
64	N.C.

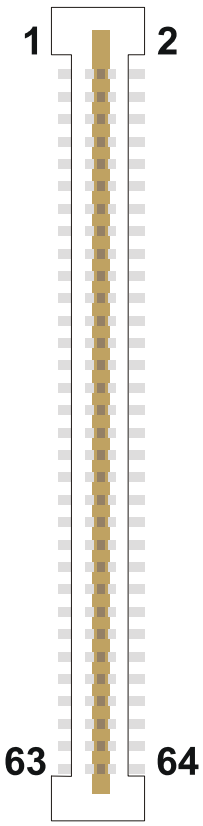
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D.19 JN3 – PIM (PCM64, J3)

Pin Number	Signal
1	N.C.
3	GND
5	P64C/BE6#
7	P64C/BE4#
9	VCC3
11	P64AD63
13	P64AD61
15	GND
17	P64AD59
19	P64AD57
21	VCC3
23	P64AD55
25	P64AD53
27	GND
29	P64AD51
31	P64AD49
33	GND
35	P64AD47
37	P64AD45
39	VCC3
41	P64AD43
43	P64AD41
45	GND
47	P64AD39
49	P64AD37
51	GND
53	P64AD35
55	P64AD33
57	VCC3
59	N.C.
61	N.C.
63	GND

Top View



Pin Number	Signal
2	GND
4	P64C/BE7#
6	P64C/BE5#
8	GND
10	P64PAR64
12	P64AD62
14	GND
16	P64AD60
18	P64AD58
20	GND
22	P64AD56
24	P64AD54
26	GND
28	P64AD52
30	P64AD50
32	GND
34	P64AD48
36	P64AD46
38	GND
40	P64AD44
42	P64AD42
44	GND
46	P64AD40
48	P64AD38
50	GND
52	P64AD36
54	P64AD34
56	GND
58	P64AD32
60	N.C.
62	GND
64	N.C.

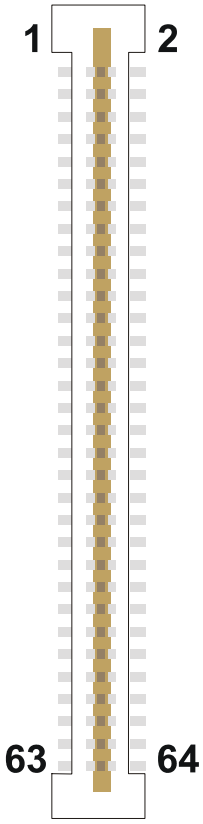
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D.20 JN4 – PIM (PCM64, J4)

Pin Number	Signal
1	P1+
3	P1-
5	P3+
7	P3-
9	P5+
11	P5-
13	P7+
15	P7-
17	P9+
19	P9-
21	P11+
23	P11-
25	P13+
27	P13-
29	P15+
31	P15-
33	P17+
35	P17-
37	P19+
39	P19-
41	P21+
43	P21-
45	P23+
47	P23-
49	P25+
51	P25-
53	P27+
55	P27-
57	P29+
59	P29-
61	P31+
63	P31-

Top View



Pin Number	Signal
2	P2+
4	P2-
6	P4+
8	P4-
10	P6+
12	P6-
14	P8+
16	P8-
18	P10+
20	P10-
22	P12+
24	P12-
26	P14+
28	P14-
30	P16+
32	P16-
34	P18+
36	P18-
38	P20+
40	P20-
42	P22+
44	P22-
46	P24+
48	P24-
50	P26+
52	P26-
54	P28+
56	P28-
58	P30+
60	P30-
62	P32+
64	P32-

Active Low

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E. BIOS SETUP ERROR CODES

E.1 POST BEEP

Recoverable POST Errors
Whenever a recoverable error occurs during POST, *Phoenix* BIOS displays an error message describing the problem.
Phoenix BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero.
An external ROM module (e. g. VGA) can also issue audible errors, usually consisting of one long tone followed by a series of short tones.

Terminal POST Errors
There are several POST routines that issue a **POST Terminal Error** and shut down the system if they fail. Before shutting down the system, the terminal- error handler issues a beep code signifying the test point error, writes the error to port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both mono and color adapters).
The routine drives the beep code from the test point error as follows:

1. The 8- bit error code is broken down to four 2- bit groups (Discard the most significant group if it is 00).
2. Each group is made one- based (1 through 4) by adding 1.
3. Short beeps are generated for the number in each group.

Example:
Test point 01Ah = 00 01 10 10 = 1- 2- 3- 3 beeps

Test Points and Beep Codes
At the beginning of each POST routine, the BIOS outputs the test point error code to I/ O address 80h. Use this code during trouble shooting to establish at what point the system failed and what routine was being performed.
If the BIOS detects a terminal error condition, it halts POST after issuing a terminal error beep code (See above) and attempting to display the error code on upper left corner of the screen and on the port 80h LED display.
If the system hangs before the BIOS can process the error, the value displayed at the port 80h is the last test performed. In this case, the screen does not display the error code.

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E.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

1. If it's the first boot, check for the onboard battery jumper W1. The board is shipped with W1 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.
2. CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the POST Errors halt condition in Setup to Disabled. This will cause BIOS to ignore all warning errors and continue the boot.

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OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When the BIOS detects an NMI (Non Maskable Interrupt) condition, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

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F. BIOS UPDATE & EMERGENCY PROCEDURE

BIOS UPDATE PROCEDURE

The BIOS update procedure is detailed in a ReadMe file included with the BIOS package as well as the update utility. This package can be downloaded from our website www.kontron.com or from our FTP site ftp://ftp.kontron.ca/Support

EMERGENCY PROCEDURE

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS has detected a corrupted BIOS CRC prior POST and fallen back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

The Emergency Recovery procedure is detailed in a ReadMe file included with the Emergency BIOS package as well as the update utility. This package can be downloaded from our website www.kontron.com or from our FTP site ftp://ftp.kontron.ca/Support

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G. GETTING HELP

At Kontron, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You can also contact us at the following address:

Kontron Canada, Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

Kontron Canada, Inc, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

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RETURNING DEFECTIVE MERCHANDISE

If your Kontron product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:

   - The Kontron Invoice number
   - Your purchase order number
   - The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:

   - Make a copy of the request form on the following page.
   - Fill out the form and be as specific as you can about the board's problem.
   - Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.

6) When returning a Kontron board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron Canada, Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

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kontron

RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name : _____

Company Name : _____

Street Address : _____

City : _____ Province/State: _____

Country : _____ Postal/Zip Code: _____

Phone Number : _____ Extension : _____

Fax Number : _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Kontron Canada, Inc., 616 Curé Boivin, Boisbriand, Québec, J7G 2A7 Canada

Fax this form to Kontron's Technical Support department in Canada at (450) 437-8053

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