

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *Kontron / Gespac PCISYS-PIIIM* at our website: *Click HERE*

	PCISYS-PII / PIII
	PROCESSOR

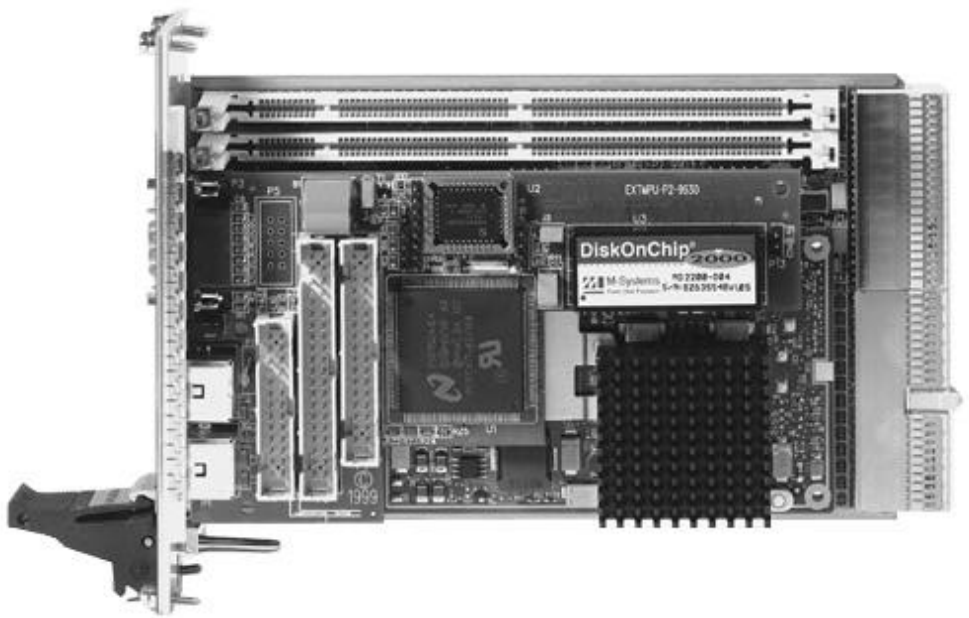
Revision 0.3

HIGH PERFORMANCE *CompactPCI*® PENTIUM II SYSTEM

The PCISYS-PII is a very high performance, highly integrated Mobile Pentium II assembly built on a compact 3U Eurocard format. It uses a Mobile Pentium II (MMC2), two standard 168-pin DIMM modules for up to 512MB of SDRAM. This combination of power and rugged industrial packaging makes the board an ideal choice for industrial automation, real-time machine control, telecommunication or medical systems applications. The ***CompactPCI*®** bus provides the features and benefits of the PCI bus specification 2.1 (32 or 64 bit, 132 or 264 MB/s bandwidth, Plug & Play) on a 3U or 6U Eurocard and an IEC-1076 compliant shielded, high density connector, allowing up to 8 boards to be connected in the same backplane.
The PCISYS-PII includes basic PC functions, COM1/2, LPT1, keyboard, mouse, USB, floppy, EIDE (UDMA/33), Fast Ethernet, Ultra Wide SCSI on rear I/O, DiskOnChip and VGA for CRT. The PCISYS-PII is fully compatible with the PC architecture and can run any PC based operating system: DOS, WINDOWS, WINDOWS 95, WINDOWS 98, WINDOWS™ NT, OS/2™, or any other operating system and application designed for the PC platform.

Technical features

- Mobile Pentium II (MMC2) @ 233 to 333 MHz
- Fan unit and Temp sensor
- 512 Kbytes L2 Pipelined Burst cache on the 512Mbytes SDRAM range
- INTEL 440BX Pentium II Chipset
- Enhanced IDE interface (UDMA/33)
- FLASH EPROM BIOS
- 3U format (100x160mm)
- Fully compatible with CompactPCI®
- Power supply: +3.3V, +5V, +12V
- 32-bit CompactPCI® bus interface (5 Volt or 3.3V)
- Watchdog timer, Real Time Clock
- COM1&2 serial port (16550)
- Optional Infrared on COM2
- USB support
- LPT1 parallel interface (EPP/ECP)
- Floppy disk interface
- Keyboard and mouse controller
- Fast Ethernet 10Base-T / 100Base-Tx
- DiskOnChip 2000 support
- Ultra Wide SCSI on rear I/O
- SVGA controller on AGP for CRT
  Up to 1600x1200 (4MB integrated SDRAM)



References

PCISYS-PII: Mobile Pentium II-based CompactPCI® Assembly

© GESPAC S.A., 2001

TABLE OF CONTENTS

1. GENERAL INFORMATION 5
1.1 PCIMPU-P2 CPU MODULE 5
1.2 EXTMPU-P2 PERIPHERAL MODULE 5
1.3 TECHNICAL FEATURES 5
1.4 MEMORY MAP 6
1.4.1 INTERNAL MEMORY MAP 6
1.5 INTERNAL I/O MAP 6
1.6 FUNCTIONAL DESCRIPTION 7
1.6.1 PC ENGINE LOGIC 7
1.6.2 8259 INTERRUPT CONTROLLER 7
1.6.3 DMA AND MEMORY MAPPER 7
1.6.4 TIMER/COUNTER 7
1.6.5 16C550 UART'S 7
1.6.6 KEYBOARD CONTROLLER 7
1.6.7 PC SPEAKER INTERFACE 8
1.6.8 FAST IDE INTERFACE 8
1.6.9 REAL TIME CLOCK 8
1.6.10 ADDITIONAL REGISTERS 8
1.6.10.1 WATCHDOG CONTROL REGISTER 8
1.6.10.2 STATUS REGISTER 8
1.6.10.3 CONTROL REGISTER 8
2. PREPARATION FOR USE AND INTER-CONNECTION 10
2.1 JUMPER AND CONNECTOR IDENTIFICATION 10
2.2 JUMPERS DESCRIPTION 11
2.2.1 J1: VIDEO STANDBY MODE 11
2.2.2 J2: AGP SETTING 11
2.2.3 J3: JTAG INPUT PORT 11
2.2.4 J4: WATCHDOG FUNCTION 11
2.2.5 J5: IRQ SETTING 11
2.2.6 J6: EXTERNAL RESET 11
2.3 CONNECTORS DESCRIPTION 12
2.3.1 P1: CPCI CONNECTOR 12
2.3.2 P2: FACTORY HEADER 13
2.3.3 P3: CONNECTOR TO EXTMPU-P2 13
2.3.4 P4: MOBILE PENTIUM II – MMC2 CONNECTOR 13
2.3.5 P6/P7: SDRAM DIMM SOCKET 13
2.3.6 P9: MOBILE PENTIUM II JTAG 13
2.3.7 P10: USB HEADER 13
2.3.8 P11: FAST ETHERNET 10-BASET/100-BASETX 13
2.3.9 P12: VGA CRT CONNECTOR 14
3. EXTMPU-P2 JUMPERS AND CONNECTORS 15
3.1 EXTMPU-P2 JUMPER AND CONNECTOR IDENTIFICATION 15
3.2 JUMPERS DESCRIPTION 16
3.2.1 J1: RTC BACKUP/RESET 16
3.2.2 J2: BIOS PROTECTION MODE 16
3.3 CONNECTORS DESCRIPTION 16
3.3.1 P1: PS/2 MOUSE CONNECTOR 16
3.3.2 P2: KBD CONNECTOR 16
3.3.3 P3: COM1 (DB9 male Connector) 16
3.3.4 P4: LPT1 CONNECTOR 16
3.3.5 P5: COM2 CONNECTOR (HE10) 17
3.3.6 P6: EIDE INTERFACE 17
3.3.7 P7: FLOPPY CONNECTOR 17
3.3.8 P8: POWER MAMAGEMENT CONNECTOR 17
3.3.9 P9: IRDA HEADER 17
3.3.10 P10: SPEAKER CONNECTOR 18
3.3.11 P11: I2C HEADER 18
3.3.12 P12: CONNECTOR TO PCIMPU-P2 18
3.3.13 P13: FAN UNIT HEADER 18
4. FUNCTIONAL DESCRIPTION 19
4. FUNCTIONAL DESCRIPTION 19
4.1 VGA VIDEO CONTROLLER 19
4.2 FAST ETHERNET CONTROLLER 19
4.3 SCSI CONTROLLER 19
4.4 DiskOnChip 2000 19
4.5 TEMPERATURE, VOLTAGE AND FAN MONITORING 19
4.6 PRECAUTION FOR USE 19

REVISION HISTORY

Rev	Date (m/d/y)	By	Modification
0.1	05/18/99	HE	Preliminary version
0.2	06/06/00	HE	Adding
0.3	11/20/01	VD/ HE	Page setting and adding

Updated revision of this document can be obtained on the Gespac Web sites:
`http://www.gespac.com` (USA site)
`http://www.gespac.ch` (European site)

CompactPCI® and CompactPCI® logo are registered trademarks of the PCI Industrial Computers Manufacturers Group.

IMPORTANT NOTICE

Gespac reserves the right to change products or specifications detailed in this documentation at any time without notice, and assumes no responsibility for any errors within this document. Gespac does not make any commitment to update this information. Gespac assumes no responsibility for the use of any products described in this documentation, nor does the Company assume responsibility for the functioning of undescribed features or parameters.

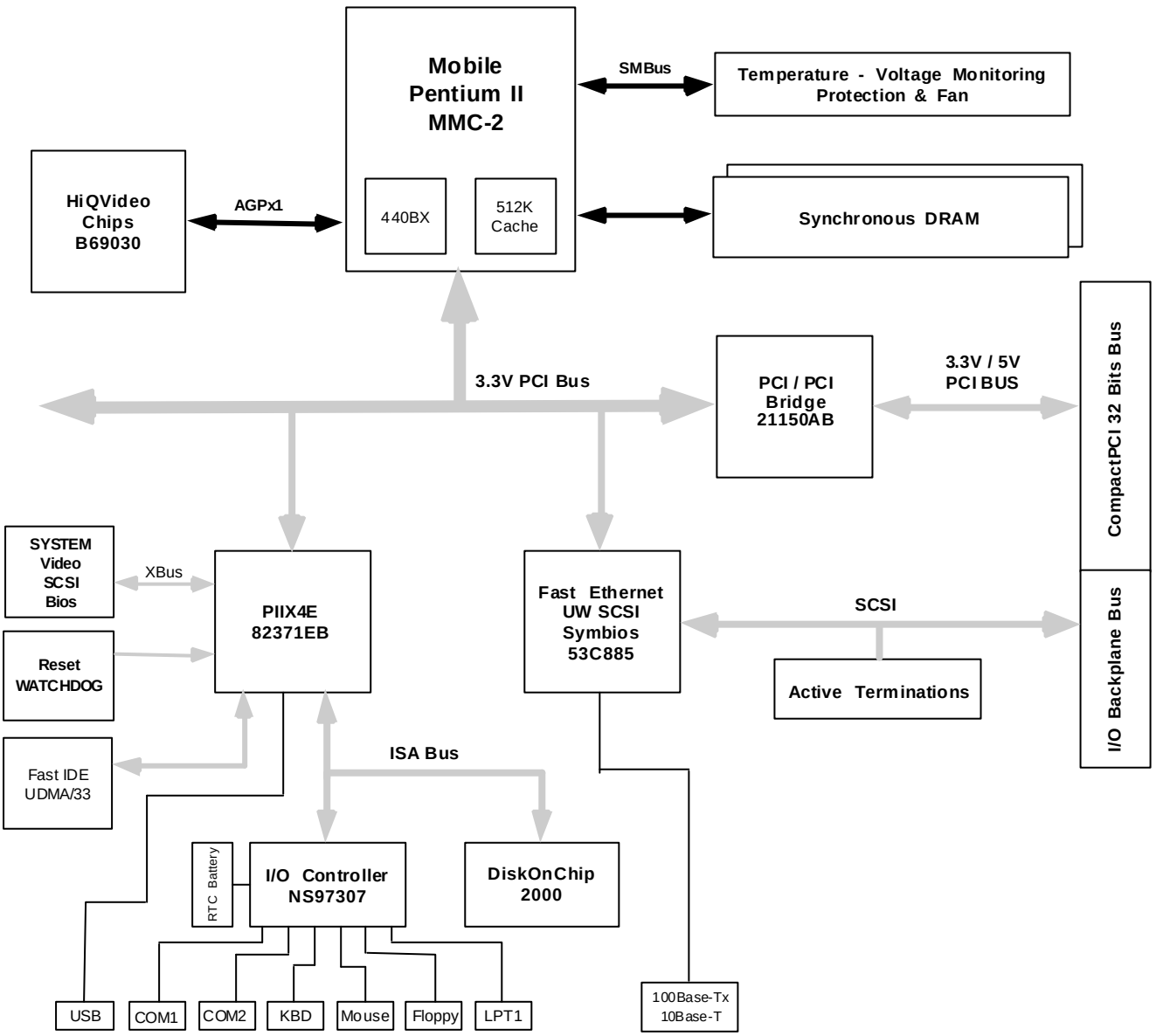


Figure 1.1 Block diagram

1. GENERAL INFORMATION

1.1 PCIMPU-P2 CPU MODULE

The PCIMPU-P2 board is the core CPU board of the PCISYS-PII CompactPCI® System. It includes the Mobile Pentium II processor, Two sockets for DIMM memory modules allowing for up to 512Mb of DRAM, and the video and SCSI/Ethernet controllers. This module supports the fully Synchronous 33 MHz PCI Bus Interface on the 8 slots CompactPCI® Bus. The PCI Bus Arbiter supports the ISA BRIDGE (PIIX4E) and seven PCI Bus Masters.

1.2 EXTMPU-P2 PERIPHERAL MODULE

The EXTMPU-P2 module is the peripheral board of the PCIMPU-P2. It includes the I/O controller and a DiskOnChip (Flash Disk) module. The I/O controller provides the Real time clock, COM1, COM2, LPT1 ports and the keyboard and mouse controller.

1.3 TECHNICAL FEATURES

CPU Type	Intel Mobile Pentium II (MMC-2).
Cache memory	Depend on processor
Memory	Up to 512MB of DRAM. Two DIMM modules of SDRAM.
FLASH EPROM	Up to 256KB BIOS, programmable on board
Intel 440BX Chip set	82433BX system controller, 82371EB PCI / ISA / IDE accelerator bridge:
BIOS	Phoenix Plug & Play BIOS
Safety	Watchdog timer, CPU Fan Unit , CPU Temperature and voltage monitoring.
Bus interface	CompactPCI® revision 1.0. PCI interface 2.1 compliant
Video interface	Chips & Technology (Intel) B69030 controller with 4Mb onboard video SDRAM. Compatible with CRT, VESA DPMS and DDC 1/2. Frame AGP 1.x Rev 2.0 Bus interface
Internal Peripherals	EIDE – UDMA/33 USB 1.0 Fast Ethernet 10/100Mb Ultra Wide SCSI
I/O controller	National Semiconductor 97307 I/O chip Floppy LPT1 RTC Keyboard Mouse COM1, COM2 IR
Power supply	+3.3, +5, +12Volt from PCI bus
Typical Power requirements	+5Vdc : 1.1A +3.3Vdc : 1.3 A +12Vdc : 0.1A
Max Power requirements	+5Vdc : Up to 6A +3.3Vdc : Up to 4A +12Vdc : Up to 0.2A
Operating temperature	0 to 55 Degrees Celsius with forced-air cooled CPU
Storage temperature	-40° to +85°C
EMC	EMC compliant
Electrical and mechanical specifications	PC/AT, PCI 2.1 and CompactPCI® 1.0 specifications
Dimensions	PCIMPU-P2 100x160 mm

1.4 MEMORY MAP

There are several types of RAM memory access in this processor card:

- Conventional
- Upper
- Extended
- High
- Expanded
- Shadowed

They are described in this section.
Conventional memory is the first 640Kbytes of memory. Under MS-DOS operating system, applications can only run in the first 640 Kbytes of memory. Other areas of memory can be used in a limited way.
Any memory addresses between 640 Kbytes and 1 Mbyte is known as UPPER memory (384 Kbytes). Some sections of upper memory are reserved for use by various parts of MPU card, like the video display, and also the ROMBIOS.
MS-DOS can enable the use of this memory to load installable device drivers, into portions of memory that are not being used, or reserved.
Intel 8086-based computers are limited to a maximum of 1 Mbyte of RAM. However INTEL 80386/486/Pentium can address more than this, and the memory above 1 Mbyte is referred to as EXTENDED memory. Normally INTEL 386/486/Pentium CPU run in real mode, which means they are simply running as fast 8086 based computer. To access extended memory INTEL processor has to be set into a special mode of operation called Protected mode.
HIGH Memory is the first 64 Kbytes of extended memory. It begins at address 10000. It is usually used by HIMEM driver on MS-DOS system.
EXPANDED Memory is another way to go beyond the 640 Kbyte conventional memory limit. This type of access memory enables to run programs that manipulate large amount of data, and that would otherwise not run efficiently in conventional memory.
Expanded memory is sometimes called paged memory, because it is divided up into 16 Kbyte memory pages. These memory pages are accessed through a block of four 16 Kbyte pages in upper memory, known as a page frame. Thus a 64 Kbyte area of upper memory is reserved for the page frame if access to expanded memory is required.
With MS-DOS, EMM386 managers permits managing and access to expanded and extended memory.
The processor module offers several address mapping and decoding options for better system performance and flexibility.
For better performance data from slow or 8-bit memory device like ROM, is copied into RAM to speed up memory accesses. This is called SHADOWING. This card support shadowing of all portion of the 256 Kbytes BIOS EPROM.
Video Bios and ROMBIOS can be shadowed on request with BIOS setup.

1.4.1 INTERNAL MEMORY MAP

A compatible PC normally includes 640K DRAM located at the address from 00000 to 9FFFF and 128K rom residing from E0000 to FFFFF. If a graphic controller is present, memory A0000 to C7FFF is reserved for video buffer and video BIOS and C8000 to DFFFF is usage free.
Inside the module one socket is provided. This socket is dedicated to BIOS ROM. This 256k*8 Flash eprom socket respond to any address selected within the range between E0000-FFFFF.
The bios is located at E0000 to FFFFF.
The memory range C8000-CFFFF is dedicated to SCSI Bios (if enable in the bios options).
The memory range DE000-DFFFFF is dedicated to internal DiskOnChip 2000.

1.5 INTERNAL I/O MAP

The X86 CPUs supports 8-bit and 16-bit peripherals. A 64 Kbytes segment is reserved to access I/O with four special Input/Output instructions. The PCISYS-PII module uses this special addressing scheme to address the onboard peripheral devices. On the PC-AT and ISA platform, it has been historically assumed that only 1k on the total 64K I/O address space is used. The first 256 bytes are reserved for I/O platform, the remaining 768 bytes are available to "general I/O Card". In that only 1K of the address space was supported, PC-104 add-on I/O cards only decode the first 10 ADDRESS signal lines ; consequently, the SA<10-15>addresses lines on the ISA BUS can be any value, the result of not decoding all ADDRESS is a repetition on 1K address boundaries.

DEVICES	Address Range(HEX)
DMA Controller 1: 8237(Slave)	0000-000F
Int.Controller 1: (master)	0026-0027
Counter: 8254	0040-0043
Keyboard controller	0060-0064
port B logic	0061
Real Time Clock: 146818A	0070-0071
DMA Page register: 74ls162	0080-008F
Int.Controller 2: (slave)	00A0-00A1
DMA Controller 2: (Master)	00C0-00DE
Fixed Disk 1: (Secondary IDE)	170-177
Fixed Disk 1: (Primary IDE)	1F0-1F7
Additional Registers	200-203
Serial Port 2: COM2	2F8-2FF
Fixed Disk 2: (Secondary IDE)	376-377
Serial Port 1: COM1	3F8-3FF
External VGA	3B0-3DF
Floppy Disk	3F0-3F5
Fixed Disk 2: (Primary IDE)	3F6-3F7

Table 1.1 lists of devices and addresses.

1.6 FUNCTIONAL DESCRIPTION

1.6.1 PC ENGINE LOGIC

The 82371EB (PIIX3) PCI ISA IDE Xcelerators are multi-function PCI devices implementing a PCI-to-ISA bridge function and an PCI IDE function. In addition, the PIIX4E implements a Universal Serial Bus host/hub function and a SMBus to control the system management. As a PCI-to-ISA bridge, the PIIX4E integrates many common I/O functions found in ISA-based PC systems, two 82C59 interrupt controllers, a serial interrupt input, two 82C37 DMA controllers, an 82C54 timer/counter. The PIIX4E supports IDE connectors providing an interface for IDE hard disks and CD ROMs.

The NS97307 (Super I/O) is a ISA peripheral. It incorporates a Floppy Disk Controller, a Keyboard and mouse controller, a Real Time Clock (RTC), two fast full function UARTs, infrared support, and a parallel port.

1.6.2 8259 INTERRUPT CONTROLLER

There are two fully compatible 82C59 interrupt controllers in the 82371EB ISA Bridge controller, providing up to 14 external interrupts. IRQ0 is always connected internally to the 82C54's counter 0 output. IRQ1, IRQ8, and IRQ10 can also be optionally driven internally from the keyboard controller, the RTC, and the internal watchdog timer respectively.

Table 1.2 show the interrupt-level assignments between the internal and external peripherals (PC-104).

Master	Slave	Internal Function	ISA BUS
IRQ0		Timer 0	
IRQ1		KBD	
	IRQ8	RTC	
	IRQ9		IRQ9
	IRQ10		IRQ10
IRQ2	IRQ11		IRQ11
	IRQ12	Mouse	
	IRQ13	Math-Coproc	
	IRQ14	IDE (primary)	
	IRQ15		IRQ15
IRQ3		COM2	
IRQ4		COM1	
IRQ5			IRQ5
IRQ6		Floppy	
IRQ7		LPT1	

Table 1.2 Hardware interrupt assignments

The internal registers of the two 8259 megacells are written to in the same way as in the standard chip. Before normal operation, each 8259 must been initialized. For more information on programming the 8259, please refer to data-sheet from INTEL, AMD, HARRIS...

1.6.3 DMA AND MEMORY MAPPER

The 82371EB contains two fully compatible 8237 DMA controllers that provide up to 4 eight-bit DMA channels and 3 16-bit DMA channels. For more information on programming the 8259, please refer to data-sheet from INTEL.

1.6.4 TIMER/COUNTER

The internal registers of the 82C54 megacell are written to in the same way as in the standard part.
Table 1.3 shows the addressing registers for each counter/timer. Refer to the 82C54 data sheet for more information on programming these chips.

Address	IOR	IOW	Register Function
40H	1	0	Write initial count to counter 0
40H	0	1	Read Count/status from Counter 0
41H	1	0	Write initial Count to Counter 1
41H	0	1	Read Count/status from Counter 1
42H	1	0	Write Initial count to Counter 2
42H	0	1	Read Count/status from Counter 2
43H	1	0	Write Control Word
43H	0	1	No Operation

Table 1.3 Counter/Timer Registers.

1.6.5 16C550 UART'S

The NS97307 (Super I/O) includes two 16C550 UARTs can be configured as COM1 and COM2 ports.
The port COM2 can also be configured as an Infrared Interface that support : IrDA 1.0 SIR, ASK-IR, DASK-IR or Consumer-Ir modes.

1.6.6 KEYBOARD CONTROLLER

The Super I/O contains a PC/AT compatible keyboard controller with PS/2 compatible mouse controller extensions. If it is not needed or an external keyboard is desired, it may be disabled (see power-up options and Miscellaneous configuration register) and so that the keyboard and mouse pins can be used for other functions or so that an external keyboard can be supported.

The keyboard controller responds to the following I/O addresses 0x60 (data) and 0x64 (Command/status). An I/O write to 0x60 will fill the keyboard controller's "Input Buffer". An I/O read from 0x60 will return the contents of the keyboard controller's "Output Buffer".

1.6.7 PC SPEAKER INTERFACE

The 97307 SUPER I/O contains a speaker output (SPKROUT), that is the logical AND of bit 1 of the port B register and the integral 82C54's OUT2 timer 2 signal.

1.6.8 FAST IDE INTERFACE

The PCISYS-PII board provide all the necessary control signals to support the integrated Drive bus (EIDE Interface).
This interface allows the connection of IDE Hard Disk, CD ROMs, LS 120 and other IDE peripherals. The IDE interface supports PIO IDE transfers up to 14 Mbytes/sec and Ultra DMA/33 transfers up to 33 Mbytes/sec. It does not consume any ISA DMA resources. The IDE interface integrates 16x32 bits buffers for optimal transfers.

1.6.9 REAL TIME CLOCK

The PCISYS-PII contains an integrated real-time clock, providing the PC function of the date/time clock, alarm, programmable periodic interrupt, 242 bytes of additional battery backed CMOS RAM, I/O registers 070h and 071h, and crystal and battery input.

1.6.10 ADDITIONAL REGISTERS

The PCISYS-PII contain two internal registers that are pre-programmed at reset, and that can be changed by the host to provide additional functionality to the card.

1.6.10.1 WATCHDOG CONTROL REGISTER

This register control the watchdog activity. On reset the watchdog is disabled. Writing $55 at **address 201** enable *permanently* the watchdog monitoring activity. Writing byte $7F with a period < 1.2 sec retrigger the watchdog timer. Breaking this sequence cause the watchdog output to goes low. If J14 is positioned on 2-3, a hardware reset is activated. If J14 is positioned on 1-2 an NMI interrupt is generated.
T

1.6.10.2 STATUS REGISTER

This register is a read only register.

Bit D5	Bit D4	Bit D0	Address
Read only	Read only	Read only	**$ 200**
0			DiskOnChip access is disable
1			DiskOnChip access is enable
	0		CPU Overtemp detected
	1		CPU Temp is ok
		0	Permanent Watchdog is disable
		1	Permanent Watchdog is enable

Bit D4 shows the status from Mobile Pentium 2 module Thermal_IRQ interrupt. This bit is low when the module is overheated.

1.6.10.3 CONTROL REGISTER

This register is a write only register.

Bit D4	Bit D0	Address
Write only	Write only	**$ 202**
0		DiskOnChip access is disable
1		DiskOnChip access is enable
	0	Processor Thermal interrupt is disable
	1	Processor Thermal interrupt is enable

Processor Thermal interrupt description :

The Mobile Pentium II Module has an internal thermal sensor. The thermal sensor is composed of control electronics, SMBus interface electronics, and a precision analog to digital convertor. Software running on the processor can use the thermal sensor to thermally manage the system. If the processor Thermal interrupt is enable, the thermal sensor could drive the SMBALERT# signal described in the SMBus specification.
It can be programmed to assert SMBALERT# if the temperature of the processor core thermal diode or internal thermal diode exceeds an upper or lower threshold. The thresholds are individually programmable for either thermal diode.

The temperature of either thermal diode can be digitally read using a SMBus read command.

For more details see Intel Mobile Pentium II Module datasheet.

2. PREPARATION FOR USE and INTERCONNECTION

Table 2.1 identifies jumpers and connectors of the PCIMPU-56A. Figure 2.1 shows their locations on the printed circuit.

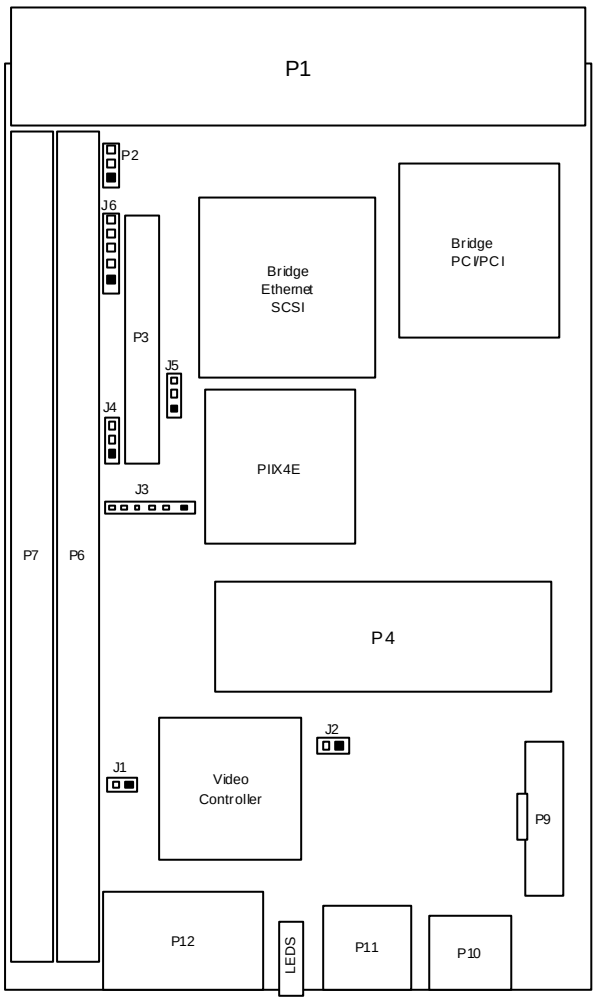


Figure 2.1 Jumper and Connector locations on the PCIMPU-P2.

2.1 JUMPER AND CONNECTOR IDENTIFICATION

Designation	Function
P1	CPCI CONNECTOR
P2	Factory header
P3	Connector to EXTMPU-P2
P4	Mobile Pentium II MMC2 Connector
P6	168 pins DIMM Connector
P7	168 pins DIMM Connector
P9	Mobile Pentium II JTAG
P10	USB Header
P11	Fast Ethernet 10-BaseT / 100-BaseTx
P12	VGA
J1	Video standby mode
J2	AGP setting
J3	JTAG Configuration
J4	WATCHDOG Function
J5	IRQ settings
J6	External Reset

Table 2.1 Connector and Jumper Identification

2.2 JUMPERS DESCRIPTION

2.2.1 J1: VIDEO STANDBY MODE

This jumper set the video controller in a standby mode. See also J2 configuration.

2.2.2 J2: AGP SETTING

This jumper enables or disables the onboard Video controller on AGP.
If J2 is set, the controller is disable, to reduce the board consumption it's possible to set the video controller in a standby mode (see J1).
If J2 is open the onboard controller is activated.

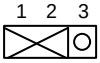
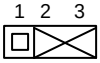
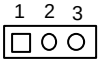
2.2.3 J3: JTAG INPUT PORT

These header is only used for the internal EPLD, factory programming.

PIN	Designation
1	TDI
2	TMS
3	TCK
4	GND
5	VCC
6	TDO

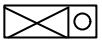
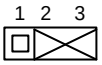
2.2.4 J4: WATCHDOG FUNCTION

The PCIMPU-P2 can be programmed with a watchdog timer in order to continuously monitor the activity of the CPU Board. If for some reason the CPU is stopped, an NMI or RESET is generated 1.2 seconds later. The NMI operation can be software programmed if desired and position 1-2 can be left open.

J4 Position	Operation mode
	Watchdog NMI enabled
	Watchdog HardReset enabled
	Watchdog NMI and HardReset disabled

2.2.5 J5: IRQ SETTING

This jumper is used to configure The IRQ on INTS (Compact PCI connector, pin 1E4).

J5 Position	Operation mode: IRQ on INTS
	IRQ 15
	SERIRQ

2.2.6 J6: EXTERNAL RESET

An external Reset switch can be mounted not the system. This switch should be directly connected on to this connector between pin 1-2.

PIN	Signal Name
1	RESET (active low)
2	GND
3	Nc
4	Nc
5	VCC

2.3 CONNECTORS DESCRIPTION

2.3.1 P1: CPCI CONNECTOR

All the PCI signals of the CompactPCI® connector are included in this IEEC-1076-4 standard connector. The distribution of the different signals of the PCI bus have been engineered to minimize the cross-talk. This connector also provide external shielding in order to maximize the signal to noise ratio on the CPCI BUS.
Complete details on the CompactPCI® are available in the CompactPCI® specification.

The lower part of the connector P1 connects the PCISYS-PII board to the CompactPCI® Bus. The upper part of the connector P1 provides the SCSI Bus on the backplane I/O connector. The signal names and pin assignment of connector P1 are defined in table 2.2.

Pin	A	B	C	D	E	F
2-22	NC	NC	NC	NC	NC	GND[1]
2-21	PCLK6	GND	NC	NC	NC	GND[1]
2-20	PCLK5	GND	NC	GND	NC	GND[1]
2-19	GND	GND	LED	NC	NC	GND[1]
2-18	SD13	/RST_SCSI	/Sense 1	GND	NC	GND[1]
2-17	SD12	GND	/EXTR	/REQ6	/GNT6	GND[1]
2-16	SD11	/SACK	/DEG	GND	NC	GND[1]
2-15	SD10	GND	/FAL	/REQ5	/GNT5	GND[1]
2-14	SD9	/SBSY	/Sense 2	GND	NC	GND[1]
2-13	SD8	GND	NC	NC	NC	GND[1]
2-12	SD7	/SATN	/SI_O	GND	NC	GND[1]
2-11	SD6	GND	NC	NC	NC	GND[1]
2-10	SD5	/SDP1	/SREQ	GND	NC	GND[1]
2-9	SD4	GND	NC	NC	NC	GND[1]
2-8	SD3	/SDP0	/SC_D	GND	NC	GND[1]
2-7	SD2	GND	NC	NC	NC	GND[1]
2-6	SD1	SD15	/SSEL	GND	NC	GND[1]
2-5	SD0	GND	NC	NC	NC	GND[1]
2-4	V(I/O)	SD14	/SMSG	GND	NC	GND[1]
2-3	CLK4	GND	/GNT3	/REQ4	/GNT4	GND[1]
2-2	CLK2	CLK3	/SYSEN	/GNT2	/REQ3	GND[1]
2-1	CLK1	GND	/REQ1	/GNT1	/REQ2	GND[1]
1-25	5V	/REQ64	/ENUM	3.3V	5V	GND[1]
1-24	AD1	5V	V(I/O)	AD0	/ACK64	GND[1]
1-23	3.3V	AD4	AD3	5V	AD2	GND[1]
1-22	AD7	GND	3.3V	AD6	AD5	GND[1]
1-21	3.3V	AD9	AD8	M66EN	/C/BE0	GND[1]
1-20	AD12	GND	V(I/O)	AD11	AD10	GND[1]
1-19	3.3V	AD15	AD14	GND	AD13	GND[1]
1-18	/SERR	GND	3.3V	PAR	/C/BE1	GND[1]
1-17	3.3V	SDONE	/SB0	GND	/PERR	GND[1]
1-16	/DEVSEL	GND	V(I/O)	/STOP	/LOCK	GND[1]
1-15	3.3V	/FRAME	/IRDY	GND	/TRDY	GND[1]
1-14	KEY AREA					
1-13						
1-12						
1-11	AD18	AD17	AD16	GND	/C/BE2	GND[1]
1-10	AD21	GND	3.3V	AD20	AD19	GND[1]
1-9	/C/BE3	IDSEL	AD23	GND	AD22	GND[1]
1-8	AD26	GND	V(I/O)	AD25	AD24	GND[1]
1-7	AD30	AD29	AD28	GND	AD27	GND[1]
1-6	/REQ	GND	3.3V	CLK	AD31	GND[1]
1-5	BRSV	BRSV*	/RST	GND	/GNT	GND[1]
1-4	BRSV	NC	V(I/O)	INTP	INTS	GND[1]
1-3	/INTA	/INTB	/INTC	5V	/INTD	GND[1]
1-2	TCK*	5V	TMS*	TDO*	TDI*	GND[1]
1-1	5V	-12V	/TRST*	+12V	5V	GND[1]

Note: * Not used by the PCISYS-PII board.
[1] Connected to the connector shield.

Table 2.2 CompactPCI® and I/O Extension connector pin assignment

2.3.2 P2: FACTORY HEADER

Don't use this header.

2.3.3 P3: CONNECTOR TO EXTMPU-P2

This connector is provided to plug the EXTMPU-P2 module for Mouse, Keyboard, Serial ports, LPT, IDE connector and the DiskOnChip 2000.

2.3.4 P4: MOBILE PENTIUM II – MMC2 CONNECTOR

This connector is provided to plug the mobile Pentium II module using the Intel MMC2 (400-pin) connector.
Complete details on the MMC2 connector are available in the *'Intel Pentium II processor mobile module (MMC2)'*© datasheet.

2.3.5 P6/P7: SDRAM DIMM SOCKET

Two standard 168-Pin DIMM socket P6/P7 are provided for up to 512-Mbytes of SDRAM (PC100).

2.3.6 P9: MOBILE PENTIUM II JTAG

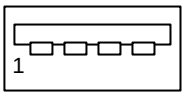
This connector is the ITP/JTAG port from the Intel Mobile module.

PIN	Designation
1	/FS_RESET
3	/DBRESET
5	TCLK
7	TMS
8	TDI
9	VTT
10	TDO
11	Pull-up 2.5V *
12	/TRST
14	2.5V *
16	/FS_PREQ
18	/FS_PRDY
20	NC
22	Pull-up 2.5V *
24	NC
26	Pull-up 2.5V *
28	NC
29	ITPCLK
30	2.5V *
2,4,6,13,15,17,19, 21,23,25,27	GND

Note: * Not used by the PCISYS-PII board.

2.3.7 P10: USB HEADER

The P10 connector (USB type A) is used to connect a USB (Universal Serial Bus) device to the PCIMPU-P2 board. This USB 1.0 support transfer s rate at 12 or 1.5Mbit/sec. The following figure shows the connector layout and the following table shows the connector pinning.



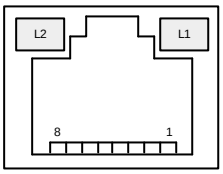
PIN	SIGNALS
1	VCC (1.1A Fuse)
2	USBD0-
3	USBD0+
4	GND

Note: Legacy keyboard and mouse aren't supported by the PCISYS-PII bios.

2.3.8 P11: FAST ETHERNET 10-BASET/100-BASETX

P11 connects the PCIMPU-P2 to a 10Base-T or 100Base-Tx network via an 8-pin RJ45 connector. A Category 5 UTP cable is necessary if the 100Base-Tx protocol is used. The maximum length from the PCIMPU-P2 board to the hub is 150 meters. The table and figure below describe the 10Base-T/100Base-Tx connector signal name and pin assignment.

Pin	Function
1	Tx+
2	Tx-
3	Rx+
4	Chassis GND
5	Chassis GND
6	Rx-
7	Chassis GND
8	Chassis GND



10Base-T/100Base-Tx front view

L1: Green Led: 10/100 selection
L2: Yellow Led: Collision Led

2.3.9 P12: VGA CRT CONNECTOR

This 15-pin mini SUB-D female connector provides standard pin assignment for video adapter.
It includes DDC control for CRT Plug & Play Display control.

Pin	Signal Name
1	ROUT
2	GOUT
3	BOUT
9	+5 Pull-up
12	DDCDATA
13	HSYNC
14	VSYNC
15	DDCLK
5,6,7,8,10	GND

3. EXTMPU-P2 JUMPERS AND CONNECTORS

Table 3.1 identifies connectors of the EXTMPU-P2. Figure 3.1 shows their locations on the printed circuit.

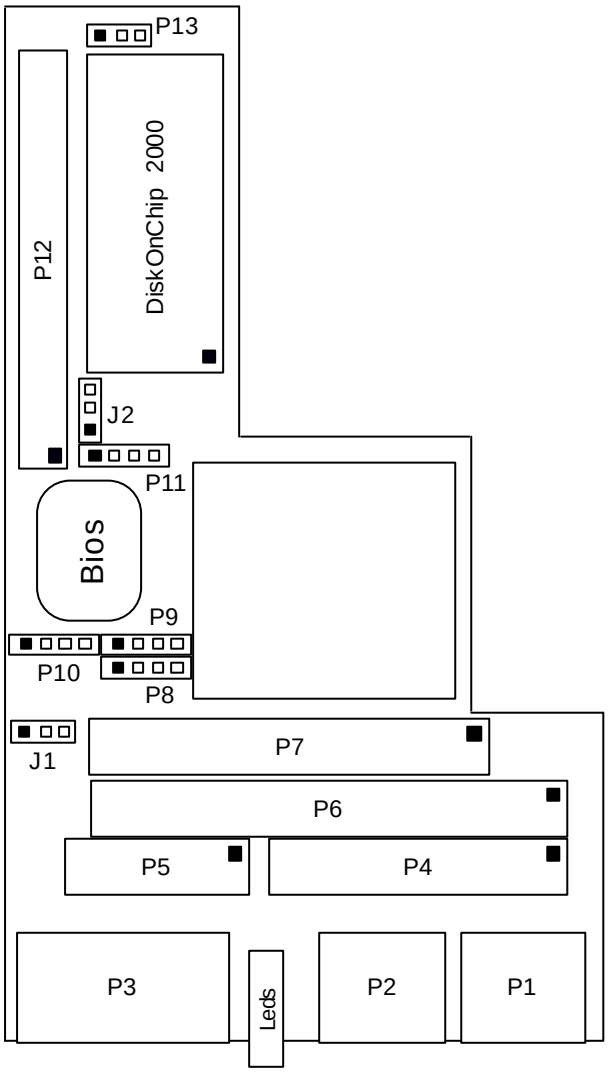


Figure 3.1 Jumper and Connector locations on the GESPCI-2.

3.1 EXTMPU-P2 JUMPER AND CONNECTOR IDENTIFICATION

Designation	Function
P1	PS/2 Mouse Connector
P2	Keyboard Connector
P3	COM1 Connector
P4	LPT Connector
P5	COM2 Header
P6	IDE Connector
P7	Floppy Connector
P8	Power Management Header
P9	IRDA Header
P10	Speaker Header
P11	I2C Header
P12	Connector to PCIMPU-P2
P13	Fan Header
J1	RTC Backup/Reset
J2	Bios operating mode

Table 3.1 Connector and Jumper Identification

3.2 JUMPERS DESCRIPTION

3.2.1 J1: RTC BACKUP/RESET

This jumper enables to power the internal Real time clock.
When J1 is removed, the EXTMPU-P2 RTC is set in its no power mode. The purpose of this jumper position is to save the Lithium battery if it is need.
When J1 is set, on position 1-2, the internal Lithium battery is connected to the internal RTC megacell.
The J1 position 2-3 must be used with caution. The purpose of this function is to discharge the residual tension available on the RTC Power input. This jumper must be shorted only if the EXTMPU-P2 is OFF. These action resets all battery backed RAM on RTC and SETUP must be run if necessary.

3.2.2 J2: BIOS PROTECTION MODE

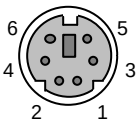
This jumper set the A17 bit on the Flash eprom for the bios configuration.

J2 position	Mode
1-2	/SA17
2-3	SA17

3.3 CONNECTORS DESCRIPTION

3.3.1 P1: PS/2 MOUSE CONNECTOR

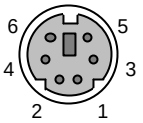
The P1 connector is used to connect a PS/2 type mouse to the EXTMPU-P2. The following figure shows the connector layout and the following table shows the connector pinning.



Pin	Signal	I/O	Description
1	MDATA	I/O	Mouse data
2	NC	-	Not connected
3	GND	-	Signal ground
4	VCCF	-	+5V fused
5	MCLK	I/O	Mouse clock
6	NC	-	Not connected
Shell	PGND	-	Chassis ground

3.3.2 P2: KBD CONNECTOR

The P2 connector is used to connect a PS/2 type keyboard to the EXTMPU-P2 board. The following figure shows the connector layout and the following table shows the connector pinning.



Pin	Signal	I/O	Description
1	KDATA	I/O	Keyboard data
2	NC	-	Not connected
3	GND	-	Signal ground
4	VCCF	-	+5V fused
5	KCLK	I/O	Keyboard clock
6	NC	-	Not connected
Shell	PGND	-	Chassis ground

3.3.3 P3: COM1 (DB9 male Connector)

Pin	Signal Name
1	DCD
2	Serial In - (SIN)
3	Serial Out - (SOUT)
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI
10	N.C.

3.3.4 P4: LPT1 CONNECTOR

Signal Name	Pin	Pin	Signal Name
STROBE-	1	2	AUTO FEED-
Data Bit 0	3	4	ERROR-
Data Bit 1	5	6	INIT-
Data Bit 2	7	8	SLCT IN-
Data Bit 3	9	10	Ground
Data Bit 4	11	12	Ground
Data Bit 5	13	14	Ground
Data Bit 6	15	16	Ground
Data Bit 7	17	18	Ground
ACK-	19	20	Ground
BUSY	21	22	Ground
PE (Paper End)	23	24	Ground
SLCT	25	26	N.C.

3.3.5 P5: COM2 CONNECTOR (HE10)

Pin	Signal Name
1	DCD
2	DSR
3	Serial In - (SIN)
4	RTS
5	Serial Out - (SOUT)
6	CTS
7	DTR
8	RI
9	GND
10	N.C.

3.3.6 P6: EIDE INTERFACE

Up to 2 IDE Hard Disk drive (UDMA/33) units (or other IDE standard interfaces) can be interfaced to the EXTMPU-P2 board using the 40-pin IDC connectors. The following table identifies the pin numbers of the P6 connector and the corresponding signal names and functions.

Signal Name	Pin	Pin	Signal Name
Reset IDE	1	2	Ground
Host Data 7	3	4	Host Data 8
Host Data 6	5	6	Host Data 9
Host Data 5	7	8	Host Data 10
Host Data 4	9	10	Host Data 11
Host Data 3	11	12	Host Data 12
Host Data 2	13	14	Host Data 13
Host Data 1	15	16	Host Data 14
Host Data 0	17	18	Host Data 15
Ground	19	20	Key
DRQ	21	22	Ground
I/O Write	23	24	Ground
I/O Read	25	26	Ground
IOCHRDY	27	28	BALE
DACK	29	30	Ground
IRQ14	31	32	NC
Addr 1	33	34	NC
Addr 0	35	32	Addr 2
Chip Select 0	37	38	Chip Select 1
Activity	39	40	Ground

3.3.7 P7: FLOPPY CONNECTOR

Signal Name	Pin	Pin	Signal Name
Ground	1	2	FDHDIN
Ground	3	4	Reserved
Key	5	6	FDEDIN
Ground	7	8	Index-
Ground	9	10	Motor Enable A-
Ground	11	12	Drive Select B-
Ground	13	14	Drive Select A-
Ground	15	16	Motor Enable B-
Ground	17	18	DIR-
Ground	19	20	STEP-
Ground	21	22	Write Data-
Ground	23	24	Write Gate-
Ground	25	26	Track 00-
Ground	27	28	Write Protect-
Ground	29	30	Read Data-
Ground	31	32	Side 1 Select-
Ground	33	34	Diskette Change-

3.3.8 P8: POWER MAMAGEMENT CONNECTOR

Future application: This connector can be used to control an ATX power supply. The APC (Advanced Power supply Control) can power on the system when the RTC reach a pre-determinated date and time.

Pin	Signal
1	SWITCH
2	ONCTL
3	RING
4	GND

3.3.9 P9: IRDA HEADER

This connector is used to plug an external IRDA module. This facility is very useful in industrial system for collecting data, maintenance information and software upgrade.
It Use the COM2 port that can be configured as an Infrared Interface that support: IrDA 1.0 SIR, ASK-IR, DASK-IR or Consumer-Ir modes.

Pin	Signals
1	GND
2	IRRX
3	IRTX
4	VCC

3.3.10 P10: SPEAKER CONNECTOR

The external speaker can be connected to this connector between pin 1 and 4.

Pin	Signal
1	HP OUT
2	NC
3	GND
4	VCC

3.3.11 P11: I2C HEADER

The EXTMPU-P2 can drive an I2C (Inter Integrated Circuit, conform with Philips® specifications) bus with the suited software.

Pin	Signal
1	SDA
2	GND
3	SCL
4	VCC

3.3.12 P12: CONNECTOR TO PCIMPU-P2

This connector is provided to plug the EXTMPU-P2 to the PCIMPU-P2 board.

3.3.13 P13: FAN UNIT HEADER

The Mobile Pentium II must be equipped with a fan unit. This fan unit should be powered in order to cool the CPU. Fan unit power connector should be mounted on to header P13 (or P2 on PCIMPU-P2).

Pin	Designation
1	GND
2	+12V
3	RPM SENSE

4. FUNCTIONAL DESCRIPTION

4.1 VGA VIDEO CONTROLLER

The CHIPS and Technology 69030 video graphic controller is 100% Hardware and Software compatible with the IBM standard VGA. Graphic BIOS is in 32Kbytes EPROM at C0000-C7FFF and is accessed via 8-bit internal data path. In terms of access time, no penalty is added since the chipset controller supports shadow memory on the video BIOS.

The video controller is equipped with 4Mb on chip DRAM. The video buffer supports standard resolution from 640x480 and 1024x768 in 16M Colors to 1280x1024 in 65K Colors or 1600x1200 in 256 Colors.

4.2 FAST ETHERNET CONTROLLER

The PCISYS-PII provides a multipoint network controller using collision detection (CSMA/CD) corresponding to the ISO/ANSI/IEEE 802.3. Its function is to interface a 10 or 100 Mbit/s network, such as Ethernet, Cheapernet, Fast Ethernet on a CompactPCI® system.

The RJ45 connector on the front panel allows the connection of 10Base-T or 100Base-Tx protocols.

4.3 SCSI CONTROLLER

The PCISYS-PII module provides a Single-Ended SCSI controller operating at transfers rates up to 40 MB/s. The different transfers rates and SCSI protocol supported by this controller are defined on table 4.3.

The SCSI Bus is provided on the CompactPCI® I/O backplane connector. An external module can be used on Rear I/O to provide SCSI connectors: RPICSI

Plug and Play active termination are implemented on the boards, which means that this termination automatically disconnected themselves if the bus is already correctly terminated. Therefore, users don't have to set jumpers to enable or disable bus termination on the board.

SCSI Protocol	Bus Width (bits)	Bus Throughput (MB/s)
SCSI-1	8	5
Fast SCSI	8	10
Fast Wide SCSI	16	20
Ultra SCSI	8	20
Ultra Wide SCSI	16	40

Table 4.1 SCSI Bus widths and throughput

4.4 DiskOnChip 2000

A DiskOnChip can be used with PCISYS-PII (capacities of 2 to 288Mbytes). The DiskOnChip 2000 contains a built-in copy of the M-Systems industry-standard TrueFFS software, which makes the DiskOnChip operate as a standard disk drive. The DiskOnChip can contain the operating system in it to allow systems without a hard disk. It can also be configured as the boot device in systems.

For more information (utilities, drivers and documentation) see *DiskOnChip 2000 utilities* floppy disk or M-Sytems web site : www.m-sys.com

Note : The memory range DE000-DFFFF is dedicated to DiskOnChip 2000

4.5 TEMPERATURE, VOLTAGE AND FAN MONITORING

The PCISYS-PII is able to monitor the board temperature, different onboard voltage and the Fan (RPM). It use a LM81 (National Semiconductor) chip and could generate an EXTSMI# to the system.
The LM81 is connected on the SMBus. The different thresholds could be software programmed.

Please contact Gespac for more information.

4.6 PRECAUTION FOR USE

Due to the high integration of the PCISYS-PII, it is necessary to provide a good airflow for cooling this module. The Mobile Pentium II processor is designed to operate with a case temperature between 0-85ºC. The integral fan units on top of the Mobile Pentium II chip effects a 30-degrees difference between ambient temperature and case temperature. You must not exceed an ambient temperature of 55 degrees.

If these conditions are not respected, the warranty of the board is lost.

.

Notes

Headquarters
18 Chemin des Aulx
1228 Geneva
Switzerland
Tel: +41 (0)22 706 2100
Fax: +41 (0)22 794 6477

North & South America
574 East Alamo
Suite 40
Chandler, Arizona 85226
Tel: +1 (480) 962 5559
Fax: +1 (480) 962 5750

France
Les Algorithmes
Bât. Epicure
91194 Saint-Aubin Cedex
Tel: +33 (0)1 69 85 33 73
Fax: +33 (0)1 69 85 36 60

Deutschland
Frauenstrasse 32
80469 München
Tel: +49 (0)89 210 2370
Fax: +49 (0)89 210 23714

España
Travesera de Gracia
62 Entresuelo 2A
Barcelona 08006
Tel /Fax: +34 93 414 25 02

Printed in Switzerland

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP