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SB586T Series
Product Manual

MANUAL NUMBER : 00431-220-5B

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FOREWORD

This product manual provides information to install, operate and or program the referenced product(s) manufactured or distributed by ICS Advent. The following pages contain information regarding the warranty and repair policies.

Check our Web site (***http://www.icsadvent.com/techsupport***) for technical information, manual, and BIOS updates. Technical assistance is also available at: **800-480-0044** (U.S. and Canada) or **858-677-0877** (international).

Manual errors, omissions, bugs, and/or comments: A Customer Comments section is included at the end of this manual. If you experience any problems with the manual or just want to give us some feedback, please review the information in this section. It will tell you how to easily access our web site and provide immediate feedback online.

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Guarantee

A thirty day money-back guarantee is provided on all **standard** products sold. **Special order products** are covered by our Limited Warranty, *however they may not be returned for refund or credit. EPROMs, RAM, Flash EPROMs or other forms of solid electronic media are not returnable for credit - but for replacement only. Extended Warranty available. Consult factory.*

Refunds

In order to receive refund on a product purchase price, the product must not have been damaged by the customer or by the common carrier chosen by the customer to return the goods, and the product must be returned complete (meaning all manuals, software, cables, etc.) within 30 days of receipt and in as-new and resalable condition. The **Return Procedure** must be followed to assure prompt refund.

Restocking Charges

Product returned *after* 30 days, and *before* 90 days, of the purchase will be subject to a **minimum** 20% restocking charge and any charges for damaged or missing parts.

Products not returned within 90 days of purchase, or products which are not in as-new and re-saleable condition, are not eligible for credit return and will be returned to the customer.

Limited Warranty

Effective April 1, 1998, all products carry a two-year limited warranty with the exception of the "Performance Series" I/O products, which are warranted to the original purchaser for as long as they own the product, subject to all other conditions below, including those regarding neglect, misuse and acts of God. Within one year of purchase, ICS Advent will repair or replace, at our option, any defective product. At any time after one year, we will repair or replace, at our option, any defective "Performance Series" I/O product sold. This does not include products damaged in shipment, or damaged through customer neglect or misuse. ICS Advent will service the warranty for all standard catalog products for the first year from the date of shipment. After the second year, for products not manufactured by ICS Advent, the remainder of the manufacturer's warranty, if any, will be serviced by the manufacturer directly.

The **Return Procedure** must be followed to assure repair or replacement. ICS Advent will normally return your replacement or repaired item via Second Day Air. *Overnight delivery or delivery via other carriers is available at additional charge.*

The limited warranty is void if the product has been subjected to alteration, neglect, misuse, or abuse; if any repairs have been attempted by anyone other than ICS Advent or its authorized agent; or if the failure is caused by accident, acts of God, or other causes beyond the control of ICS Advent or the manufacturer. Neglect, misuse, and abuse shall include any installation, operation, or maintenance of the product other than in accordance with the owners' manual.

No agent, dealer, distributor, service company, or other party is authorized to change, modify, or extend the terms of this Limited Warranty in any manner whatsoever. ICS Advent reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

Shipments not in compliance with this Guarantee and Limited Warranty Return Policy will not be accepted by ICS Advent.

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Return Procedure

For any Limited Warranty or Guarantee return, please contact ICS Advent's Customer Service at **800-480-0044** (U.S. and Canada) or **858-677-0877** (international) and obtain a Return Material Authorization (RMA) Number. All product(s) returned to ICS Advent for service or credit **must** be accompanied by a Return Material Authorization (RMA) Number. Freight on all returned items **must** be prepaid by the customer who is responsible for any loss or damage caused by common carrier in transit. Returns for Warranty **must** include a Failure Report for each unit, by serial number(s), as well as a copy of the original invoice showing date of purchase.

> To reduce risk of damage, returns of product must be in an ICS Advent shipping container. If the original container has been lost or damaged, new shipping containers may be obtained from ICS Advent Customer Service at a nominal cost.

Limitation of Liability

In no event shall ICS Advent be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental, or consequential damages in connection with or arising out of the performance or use of any product furnished hereunder. ICS Advent liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by ICS Advent or its authorized agent.

Some *Sales Items* and *Customized Systems* are **not** subject to the guarantee and limited warranty. However in these instances , any deviations will be disclosed prior to sales and noted in the original invoice. ***ICS Advent reserves the right to refuse returns or credits on software or special order items.***

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Advisories

Three types of advisories are used throughout the manual to stress important points or warn of potential hazards to the user or the system. They are the Note, the Caution, and the Warning. Following is an example of each type of advisory:

Note: The note is used to present information which may provide special instruction or extra information which may help to simplify the use of the product.



CAUTION!



A Caution is used to alert you of a situation which if ignored may cause injury or damage equipment.



WARNING!



A Warning is used to alert you of a situation which if ignored will cause serious injury.

Cautions and Warnings are accented with triangular symbols. The excalmation symbol is used in all cautions and warnings to help alert you to the important instructions. The lightning flash symbol is used on the left hand side of a caution or a warning if the advisory relates to the presence of voltage which may be of sufficient magnitude to cause electrical shock.

Use caution when servicing any electrical component. We have tried to identify the areas which may pose a Caution or Warning condition in this manual; however, ICS Advent does not claim to have covered all situations which might require the use of a Caution or Warning.

You must refer to the documentation for any component you install into a computer system to insure proper precautions and procedures are followed.

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Chapter 1: Introduction

This manual describes the SB586T family of single board computers. A complete list of products covered by this manual appears at the end of this chapter. Chapter 1 provides general information and specifications. Chapter 2 lists the connector pinouts and illustrates the five board layouts in the series. Chapter 3 describes how to install components and set switches. Chapter 4 describes maintenance and troubleshooting. The appendix describes the BIOS.

General

The SB586T series of CPU boards are full featured, industrialized, single board computers supporting the Intel® Pentium®, Pentium with MMX technology, AMD K6®, and AMD K6-2 processors. The SB586T series combines on one board many features normally needed for system operation, including high-speed serial ports, parallel port, and disk controllers. This design reduces the number of slots required on the passive backplane and allows room for additional feature cards. All onboard controllers may be disabled through the system BIOS.

The boards feature an external bus architecture that complies with the ISA standard and includes a PCI bus extension to communicate with onboard functions. This extension supports the DEC PCI-to-PCI bridge chip, allowing additional peripherals on the PCI bus.

The SB586T series supports a full range of processors with speeds ranging from 100 to 300MHz. You may select models with or without MMX support or the similar 3DNow!® technology. All processors fit into a ZIF Socket 7 and include a fan-cooled heat sink. You can upgrade your processor easily by replacing it and making a few adjustments to a jumper and a DIP switch.

Each board has four 72-pin SIMM sockets, arranged in two banks and will accept up to 256MB of DRAM using 32-bit EDO or 36-bit FPM SIMMs. ECC memory is also supported. In addition, a 512K onboard synchronous pipeline burst cache is standard on all models.

Year 2000 Compliance

ICS Advent warrants that the SB586T series has been tested for Year 2000 compliance. The boards have been verified to "roll over" to the year 2000 properly and to indicate the proper date for the leap year. This warranty applies to the feature board only and does not guarantee that improperly written application software will report the year correctly.

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Features

Table 1-1 lists the major features of each model in the SB586T series.

Table 1-1: SB586T Models

Model Number	Base Model	Universal Serial Bus	SCSI 3	Ethernet	SVGA Video
SB586T	X				
SB586TU		X			
SB586TS			X		
SB586T2V					X
SB586TS2V			X		X
SB586TT				X	X

Onboard Controllers

Onboard controllers for disk drives, serial ports, and parallel ports are incorporated into the design of the SB586T series. SCSI and video controllers are options at the time of purchase. All onboard controllers are individually enabled or disabled through the system BIOS. Unless indicated, the following controllers are present in all models of the SB586T series.

Display Controller (SB586T2V, SB586TS2V, and SB586TT)

The SVGA controller offers 2MB of DRAM and resolutions up to 1600 x 1200 with 256 colors. **Table 1-2** lists the refresh rates and maximum colors available for the supported resolutions. The display portion includes a VESA feature connector (J11), allowing other peripherals to share signals and control of the VGA circuitry. In addition, the board has a set of diskettes containing video display drivers and display-enhancement utilities. The diskettes also contain documentation for installing and configuring the drivers.

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Table 1-2: Video Resolutions, Refresh Rates, and Colors

Resolution	Refresh Rates (Hz)	Maximum Colors
640 x 480	60, 72, 75, 85	24-bit true color (16M)
800 x 600	56, 60, 76, 75, 85	24-bit true color (16M)
1024 x 768	43i*, 60, 70, 72, 75, 85	16-bit (65K)
1152 x 864	70, 75	256
1280 x 1024	43i*, 60, 75	256
1600 x 1200	48i*	256
i* = interlaced		

Ultra Wide SCSI Controller (SB586TS and SB586TS2V)

The SCSI connector at J9 is a single-ended SCSI-3 ultra-wide interface based on the 7880 Adaptec AIC controller. The 8- or 16-bit autoselectable bus width maintains maximum compatibility. With the 16-bit bus width selected (ultra-wide SCSI), throughputs of up to 40MB/sec are possible. You can easily customize your host adapter with the built-in BIOS-based configuration utility.

A single-ended, 68-pin "P" connector attaches the SCSI controller to a high-density 68-pin SCSI cable. This cable allows full use of 16-bit wide bus transfers. A 68-pin–to–50-pin adapter is available to channel the SCSI bus signals to an 8-bit, 50-pin connection for older SCSI peripherals.

Normal SCSI and SCSI wide devices may be used on the same SCSI bus via an optional adapter. If you mix these devices, ICS Advent recommends ***a terminated SCSI wide device at the end of the cable*** to ensure proper termination of all SCSI signals.

Refer to the SCSI Connection section in Chapter 3 for more information.

Dual EIDE Disk Drive Controller

Two interfaces are provided for EIDE fixed disk drives at J1 and J8. The two EIDE connectors are located on the PCI local bus and support two drives each. The interface includes LBA and PIO mode 4 support, allowing up to 16.6MB/sec throughput speeds.

Diskette Drive Controller

The diskette drive controller at J3 supports up to two drives. The diskette drives may range in density from 360K to 2.88MB.

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I/O Ports

Two serial ports, J5 and J13, are available, each compatible with the 16550 UART. The serial port at J13 is extended through a 10-pin header on the board to a bracket-mounted DB-9 connector. Both serial ports are isolated for protection up to 1500V on signal lines.

Note: The SB586TU and SB586TT have a 9-pin header at J18 instead of the DB-9 connector.

An enhanced parallel port at J4 is also included, which is capable of bidirectional communication. The parallel port is extended through a 26-pin header on the board to a bracket-mounted DB-25 connector.

Watchdog Circuit

The watchdog circuit is a hardware timer that resets the CPU if the timer is not refreshed periodically. The circuit is refreshed by a trigger pulse provided by the onboard MACH 211 programmable logic device. This timer is enabled by a switch setting on the back of the board, which, when set, writes a "1" to I/O address 351h, data bit "0". When enabled, software needs to toggle bit "0" at I/O address 350h once every 650msec to prevent the timer from resetting the CPU. The watchdog circuit will also reset the CPU if the +5VDC power input falls below 4.75VDC.

Ethernet Connector (SB586TT)

The SB586TT provides a 10/100 BASE-T DEC 21140-AE controller that complies with IEEE 802.3 and ANSI 8802-3 Ethernet standards. The controller features full-duplex operation, onchip DMA to minimize CPU access, and external/internal loopback capability. An RJ45 connector is provided at J20 and an Ethernet LED at J21 (to indicate TX and RX links).

Universal Serial Bus (SB586TU)

The SB586TU, with the high-speed, high-capacity Universal Serial Bus (USB), supports ISA/PCI passive backplanes with up to 16 PCI expansion slots.

Specifications

Unless indicated, the following specifications apply to all models in the SB586T series.

Processors Supported

- Intel Pentium, AMD K-6, or AMD K6-2 in a ZIF Socket 7

Processor Clock Rate

- 100, 133, 166, 200, 233, 266, or 300MHz

ISA Bus Clock Rate

- 8.33MHz, 24mA line drivers

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PCI Bus Clock Rate

- 33MHz

Crystal Clock Rate

- 14.31818MHz±100ppm

Chip Set

- Triton II (Intel 430HX)

BIOS

- Hi-Flex Pentium AMIBIOS, Flash EPROM support, Plug-and-Play compatible
- Full support for Year 2000 and leap-year date functions

Memory Capacity

- 256MB maximum onboard

SIMM Support

- 2 banks, 2 sockets each, 72-pin, 32-bit EDO or 36-bit FPM (with parity) SIMMs
- ECC memory supported

Memory Speed Required

- 70ns or faster

Video Controller (SB586T2V, SB586TS2V, and SB586TT)

- SVGA Video, Cirrus Logic CL-GD5446
- 2MB DRAM installed
- VESA feature connector
- Rear panel DB-15, high density, 15-pin connector, female

Cache Memory

- 16K internal Pentium chip cache (32K on MMX)
- 512K synchronous pipeline burst L2 cache onboard

EIDE Disk Controller

- Four fixed disk drives supported (two each on primary and secondary PCI buses)
- LBA and PIO Mode 4 support

SCSI Disk Controller (SB586TS and SB586TS2V)

- SCSI-3 Ultra-Wide controller, located on PCI local bus
- Autosensed 8-bit or 16-bit bus
- To 40MB/sec throughput
- Adaptec AIC-7880 single-chip host adapter

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Ethernet Controller (SB586TT)

- Complies with IEEE 802.3 and ANSI 8802-3 Ethernet standards
- 10/100 BASE-T twisted-pair cable with full-duplex operation
- RJ45 connector included
- DEC 21140-AE controller

Diskette Controller

- 2 diskette drives, up to 2.88MB supported

Serial Ports

- Two, RS232, 16550-compatible, FIFO buffer
- Isolated to ±1500V ESD
- MAX211E component incorporated for enhanced ESD protection

Parallel Port

- One, Centronics-compatible, bidirectional compatibility
- EPP and ECP enhanced port modes

Speaker, Keyboard, Keylock, and Reset Port

- Single 8-pin header connector for system interface

Note: The keyboard may be selected as *absent* or *present* by the system BIOS. This option allows the system to boot without a keyboard attached.

Watchdog Timer

- Reset CPU automatically if CPU stops operating
- Reset CPU automatically if +5VDC varies more than 5%

CMOS Battery

- Onboard, included in Dallas 12887A chip (U18 in **Figures 2-1** through **2-6**)

Supported Operating Systems

- Windows NT™ V4.0 Workstation and Server
- Windows '95™ OSR2
- SCO Unix™ V5.0 and later
- SCO UnixWare™ V2.1 and later
- Solaris™ V2.5.1 with driver update patches 9 and 10
- MS-DOS™ 6.22
- Windows 3.11™
- OS/2™ V2.0 and later
- QNX 4.24

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Operating Environment

Temperature

- 0°C to 70°C

Humidity

- 5% to 90% RHNC

Storage Environment

Temperature

- -40°C to 85°C

Humidity

- 5% to 90% RHNC

MTBF

- >90,000 P.O.H. @ 25°C

Power Requirements

- 1.6A @ +5V
- <100mA @ +12V

Note: The onboard +3.3 V is regulated down from the +5V source.

Agency Approvals

FCC conformity with:

47 CFR Part 15, Subpart B, Class A

CE conformity with:

EU EMC Directive 89/336/EEC

EU Low Voltage Directive 72/23/EEC

UL/cUL Recognized to

Ul 1950, 2nd Ed: 1993

cUL/CAN/CSA-C22.2 No. 950.93

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Products Covered by this Manual

This manual covers the following products:

SB586T100
SB586T133
SB586T166
SB586T166X
SB586T200
SB586T200X
SB586T233X
SB586T266K
SB586T300K

SB586TT100
SB586TT133
SB586TT166X
SB586TT200X
SB586TT233X
SB586TT266K
SB586TT300K

SB586TS100
SB586TS133
SB586TS166
SB586TS166X
SB586TS200
SB586TS200X
SB586TS233X
SB586TS266K
SB586TS300K

SB586T2V100
SB586T2V133
SB586T2V166
SB586T2V166X
SB586T2V200X
SB586T2V233X
SB586T2V266K
SB586T2V300K

SB586TS2V100
SB586TS2V133
SB586TS2V166
SB586TS2V166X
SB586TS2V200X
SB586TS2V233X
SB586TS2V266K
SB586TS2V300K

SB586TU100
SB586TU133
SB586TU166
SB586TU166X
SB586TU200X
SB586TU233X
SB586TU266K
SB586TU300K

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Chapter 2: Connectors and Layouts

This chapter lists the connectors and shows the layouts of the six models in the SB586T series.

Connectors

Each model has several rear panel and onboard connectors. Silkscreened numbers identify the connectors. Square pads mark each pin 1 to prevent improper connection. Pins that supply power to an external connection are fused for protection. **Except where indicated, connectors are common to all six models.**

Note: The # symbol in the following pinouts indicates an active low signal.

J1: Primary EIDE Hard Drive Port

40-pin dual row header, Amp 103308-8

The J1 connector supplies signals from an onboard EIDE controller to interface up to two EIDE hard drives.

1	RESET	21	DRQ
2	GND	22	GND
3	DATA7	23	LOC IOW
4	DATA8	24	GND
5	DATA6	25	LOC IOR
6	DATA9	26	GND
7	DATA5	27	IORDY
8	DATA10	28	BALE
9	DATA4	29	DACK
10	DATA11	30	GND
11	DATA3	31	IRQ14
12	DATA12	32	LOCIOCS16
13	DATA 2	33	ADD1
14	DATA13	34	N/C
15	DATA1	35	ADD0
16	DATA14	36	ADD2
17	DATA0	37	CS0
18	DATA15	38	CS1
19	GND	39	LED
20	N/C (Key)	40	GND

J2: Speaker, Keyboard, Keylock, Reset

8-pin single row header, Molex 22-23-2081

The J2 connector supplies speaker, keyboard, keylock, and system reset signals. If you purchased the SB586T with a chassis, J2 will be connected to the chassis speaker, keyboard connector, and reset switch. For more details, see the chassis wiring diagram in your chassis product manual.

1	RESET	5	KBDDATA
2	GND	6	KLOCK
3	N/C	7	+5VDC (fused)
4	KBDCLOCK	8	SPKDATA

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J3: Floppy Drive Connector

34-pin dual row header, Amp 103308-7

The J3 connector supplies the signal from an onboard diskette drive controller for one or two diskette drives.

1	GND	18	DIR#
2	DRVEN0	19	GND
3	GND	20	STEP#
4	N/C	21	GND
5	GND	22	WRDATA#
6	DRVEN1	23	GND
7	GND	24	WRGATE#
8	INDEX#	25	GND
9	GND	26	TRK0#
10	FDME0#	27	GND
11	GND	28	WRPROTECT#
12	FDSEL1#	29	GND
13	GND	30	RDDATA#
14	FDSEL 0#	31	GND
15	GND	32	HDSEL#
16	FDME1#	33	GND
17	GND	34	DSKCHG#

J4: Parallel Port Connector

26-pin dual row header, Amp 103308-6

The J4 connector allows the use of parallel devices, typically printers. Your SB586T will be delivered with this port already connected to a slot filler bracket for easier access.

1	STROBE#	14	GND
2	AUTOFEED#	15	DATABIT 6
3	DATABIT0	16	GND
4	FAULT#	17	DATABIT 7
5	DATABIT1	18	GND
6	INIT#	19	ACK#
7	DATABIT2	20	GND
8	SLCTIN#	21	BUSY
9	DATABIT3	22	GND
10	GND	23	PERR
11	DATABIT4	24	GND
12	GND	25	SELECT
13	DATABIT5	26	N/C

J5: COM2

10-pin dual row header, Amp 103308-1

The J5 connector is the second system serial port, which allows the use of serial devices or serial communications.Your SB586T will be delivered with this port already connected to a slot filler bracket for easier access.

1	CD	6	CTS
2	DSR	7	DTR
3	RX	8	RI
4	RTS	9	GND
5	TX	10	N/C

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J6: IDE Hard Drive LED Connector

2-pin header, Molex 22-23-2021

The J6 connector provides the IDE hard drive access signal. This connector has a 5V differential to activate any IDE hard drive access LED used in the chassis.

1	LED–	2	LED+

J7: SCSI Hard Drive LED Connector (SB586T, SB586TS, SB586T2V, SB586TS2V)

2-pin header, Molex 22-23-2021

The J7 connector provides the SCSI hard drive access signal. This connector has a 5V differential to activate any SCSI hard drive access LED used in the chassis.

1	LED–	2	LED+

J8: Secondary EIDE Hard Drive Port

40-pin dual row header, Amp 103308-8

The J8 connector supplies the signals from an onboard EIDE controller to interface one or two EIDE hard drives.

1	RESET	21	DRQ
2	GND	22	GND
3	DATA7	23	LOCIOW
4	DATA8	24	GND
5	DATA6	25	LOC IOR
6	DATA9	26	GND
7	DATA5	27	IORDY
8	DATA10	28	BALE
9	DATA4	29	DACK
10	DATA11	30	GND
11	DATA3	31	IRQ 15
12	DATA12	32	LOCIOCS16
13	DATA2	33	ADD1
14	DATA13	34	N/C
15	DATA1	35	ADD0
16	DATA14	36	ADD2
17	DATA0	37	CS0
18	DATA 15	38	CS1
19	GND	39	LED
20	N/C (Key)	40	GND

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J9: SCSI-3 Port (SB586TS, SB586TS2V)

68-pin Amp 749069-7

The SB586TS and SB586TS2V boards have Adaptec AIC-7880 SCSI processors that automatically support up to 7 narrow or 15 wide SCSI devices.

1	GND	35	DATA12#
2	GND	36	DATA13#
3	GND	37	DATA14#
4	GND	38	DATA15#
5	GND	39	SCDPH#
6	GND	40	SCD0#
7	GND	41	SCD1#
8	GND	42	SCD2#
9	GND	43	SCD3#
10	GND	44	SCD4#
11	GND	45	SCD5#
12	GND	46	SCD6#
13	GND	47	SCD7#
14	GND	48	SCDPL#
15	GND	49	GND
16	GND	50	GND
17	TRMPWR	51	TRMPWR
18	TRMPWR	52	TRMPWR
19	N/C	53	N/C
20	GND	54	GND
21	GND	55	SCATN#
22	GND	56	GND
23	GND	57	SCBSY#
24	GND	58	SCACK#
25	GND	59	SCRST#
26	GND	60	SCMSG#
27	GND	61	SCSEL#
28	GND	62	SCC/D#
29	GND	63	SCREQ#
30	GND	64	SCI/O#

J9 : SCSI-3 Port (continued)

31	GND	65	SCD8#
32	GND	66	SCD9#
33	GND	67	SCD10#
34	SCSIW#	68	SCD11#

J10: ISP Header

6-pin single row header, Amp 103327-6

The J10 connector is used for field upgrades to the MACH211-SP Programmable Logic Device, which has in-system programming (ISP) capabilities.

1	TDI	4	TDO
2	TCK	5	VCC
3	TMS	6	GND

J11: VESA Feature Connector (SB586T2V, SB586TSV, SB586TT)

26-pin dual row header, Amp 1-103328-3

The J11 connector improves performance by bypassing the local PCI bus.

1	GND	14	PXLDATA6
2	PXLDATA 0	15	GND
3	GND	16	PXLDATA7
4	PXLDATA1	17	GND
5	GND	18	PXLCLK
6	PXLDATA2	19	GND
7	EVIDEO#	20	BLANKING
8	PXLDATA3	21	GND
9	ESYNC#	22	HSYNC
10	PXLDATA 4	23	N/C
11	EDCLK#	24	VSYNC
12	PXLDATA5	25	DDCDAT
13	DDCCLK	26	GND

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J12: Fan Power Connector

2-pin single row friction lock,
Molex 22-23-2021

The SB586T models are delivered with a fan appropriate for the microprocessor. This fan is powered through the J12 connector with +12VDC.

1	+12V	2	GND

J13: COM1 (SB586T, SB586TS, SB586T2V, SB586TS2V)

DB9 connector, Amp 869436-2

The J13 connector is the first system serial port. Typically it provides connection for a serial mouse or for serial communications.

1	CD	6	DSR
2	RX	7	RTS
3	TX	8	CTS
4	DTR	9	RI
5	GND		

J14: P/S-2 Connector

6-pin mini-DIN, Amp 749231-1

The J14 connector allows you to connect a P/S-2–type mouse.

1	MDATA	4	+5V (fused)
2	N/C	5	MCLOCK
3	GND	6	N/C

J15: SVGA (SB586T2V, SB586TS2V, SB586TT)

15-pin high density D, Amp 869427-2

The J15 connector allows you to connect an SVGA monitor.

1	RED	9	N/C
2	GREEN	10	GND
3	BLUE	11	N/C
4	N/C	12	DDCDAT
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	DDCCLK
8	GND		

J16: USB (SB586TU)

Single USB connector, Amp 787616-1

The J16 connector is the first system Universal Serial Bus port. Typically it provides connection for USB peripherals.

1	FVCC0	3	FP0+
2	FP0-	4	FGND

J17: USB (SB586TU)

Single USB connector, Amp 787616-1

The J17 connector is the second system Universal Serial Bus port. Like J16, it typically provides connection for USB peripherals.

1	FVCC1	3	FP1+
2	FP1-	4	FGND

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J18: COM1 (SB586TU, SB586TT)

10-pin dual row header, Amp 103308-1

The J18 connector is the first system serial port on the SB586TU. Typically it provides connection for a serial mouse or for serial communications.

1	CD	6	CTS
2	DSR	7	DTR
3	RX	8	RI
4	RTS	9	GND
5	TX	10	N/C

J19: PS/2 Keyboard Connector (SB586TT, SB586TU)

6-pin mini-DIN connector, Amp 749231-1

The SB586TU has a separate keyboard pinout at J19.

1	KBDDATA	4	VCC (fused)
2	N/C	5	KBDCLOCK
3	GND	6	N/C

J20: Ethernet Connector (SB586TT)

8-pin RJ45, Amp 555133-3

The J20 connector provides an Ethernet connection for network communications.

1	TX+	5	CTTX2
2	TX-	6	TX-
3	RX+	7	CTRX1
4	CTTX1	8	CTRX2

J21: Ethernet LED Connector (SB586TT)

4-pin friction lock header, Molex 22-23-2041

The J21 connector serves the Ethernet LED.

1	LINK LED	3	RX LED
2	TX LED	4	GND

Board Layouts

Figures 2-1 through **2-6** illustrate the six models in the SB586T series. Standard PICMG dimensions are used for all boards. Notice in particular the connectors listed in the previous section.

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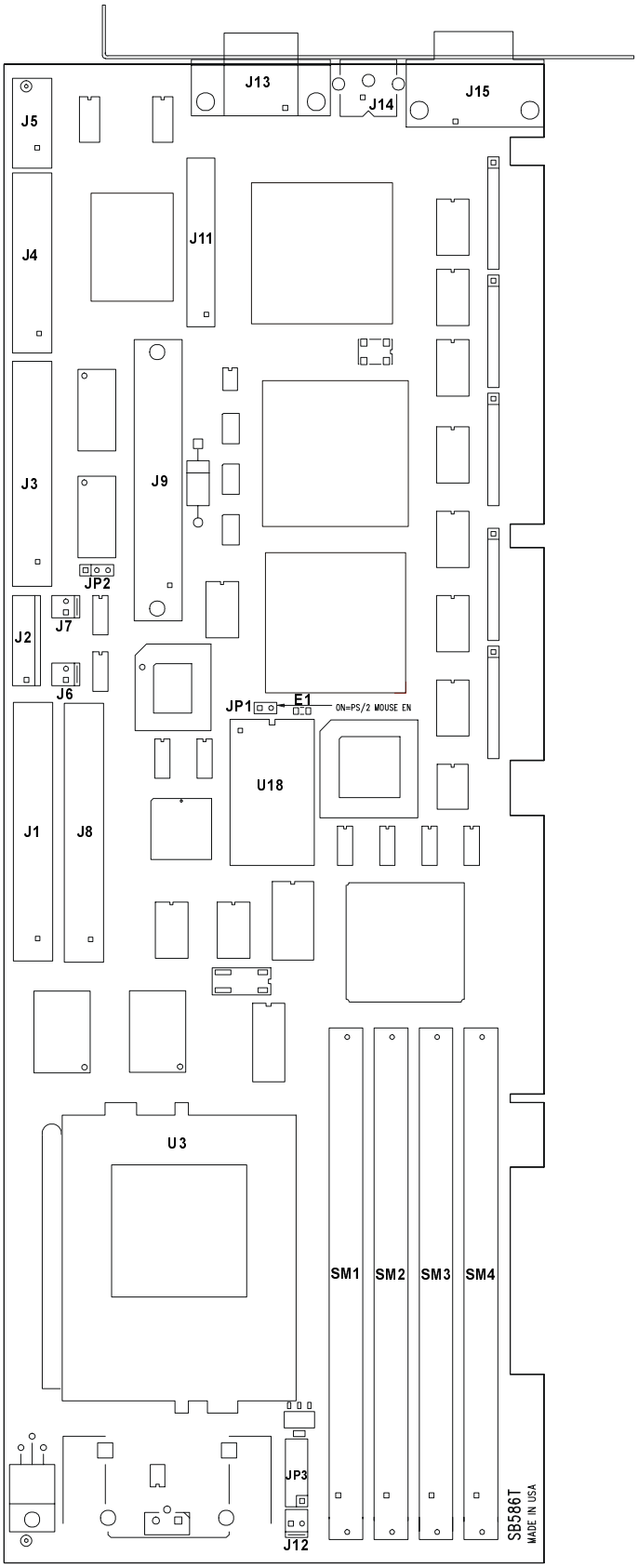


Figure 2-1: SB586T (Base Model)

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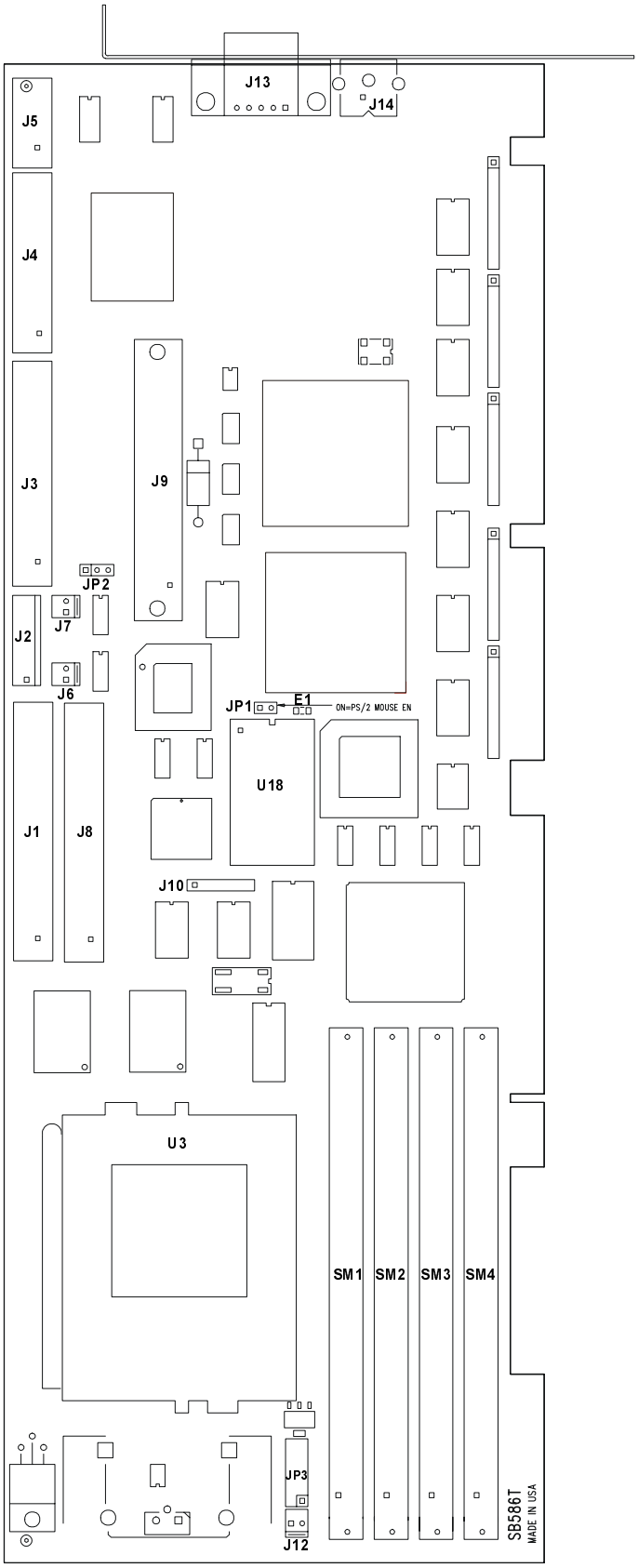


Figure 2-2: SB586TS (SCSI 3)

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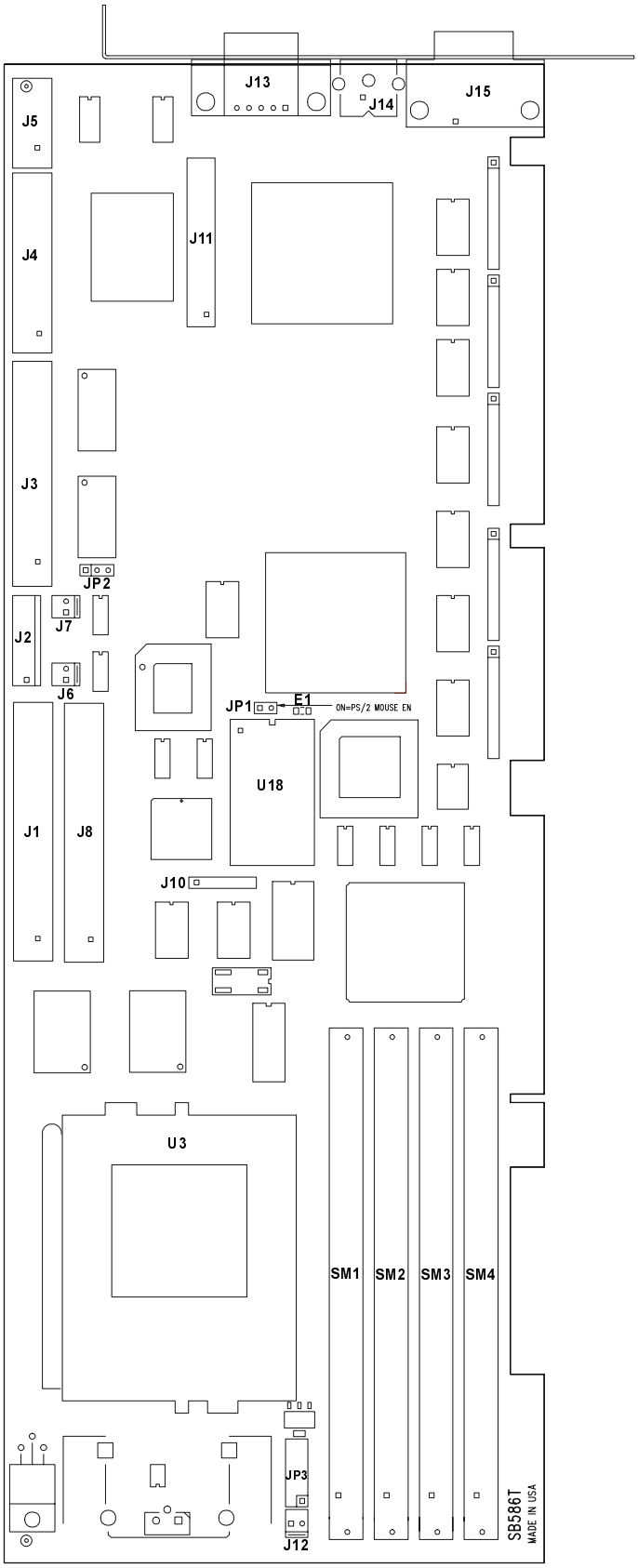


Figure 2-3: SB586T2V(SVGA Video)

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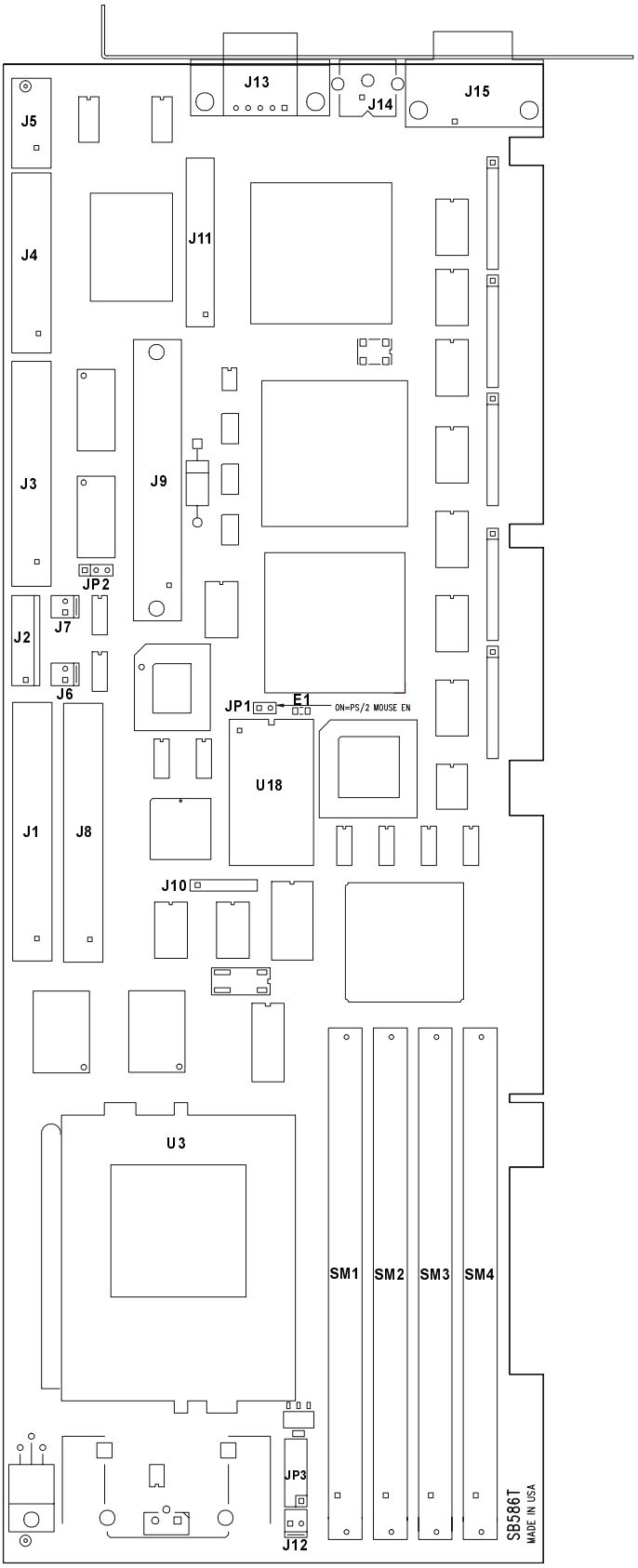


Figure 2-4: SB586TS2V (SCSI 3 and SVGA Video)

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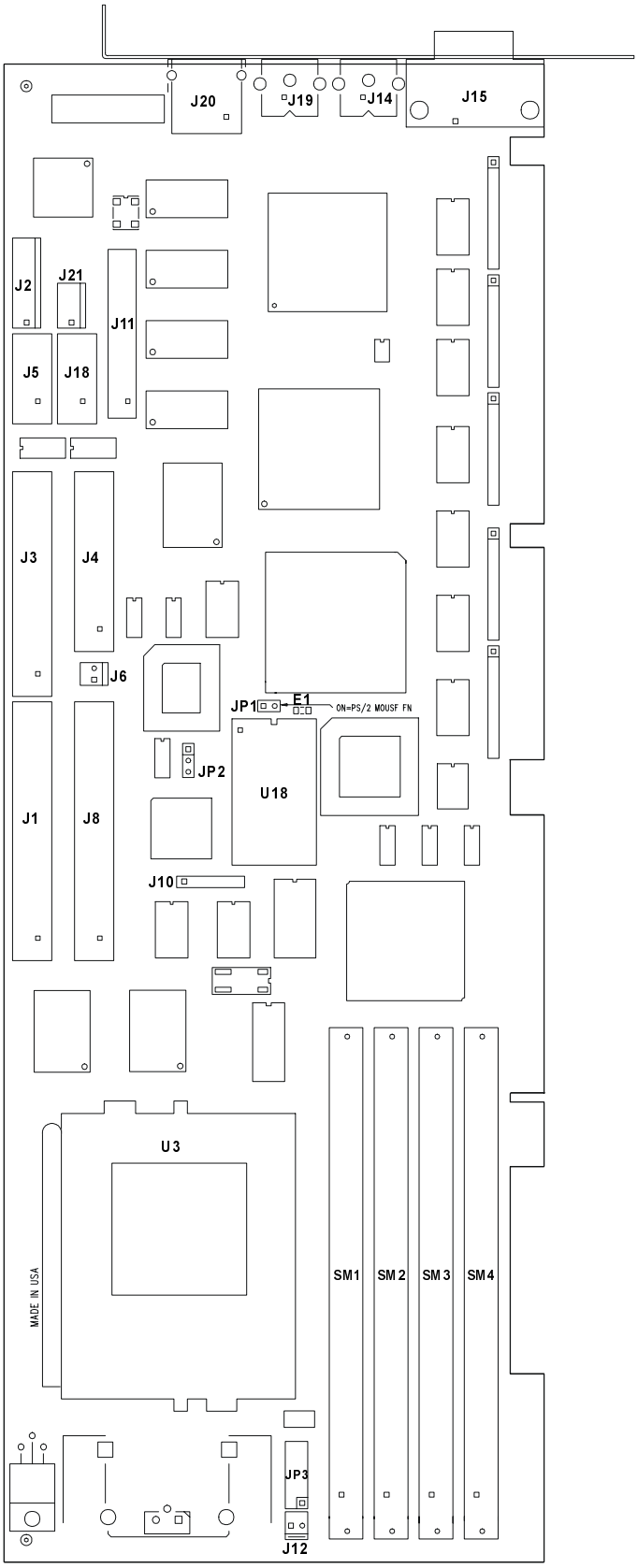


Figure 2-5: SB586TT (Ethernet and SVGA Video)

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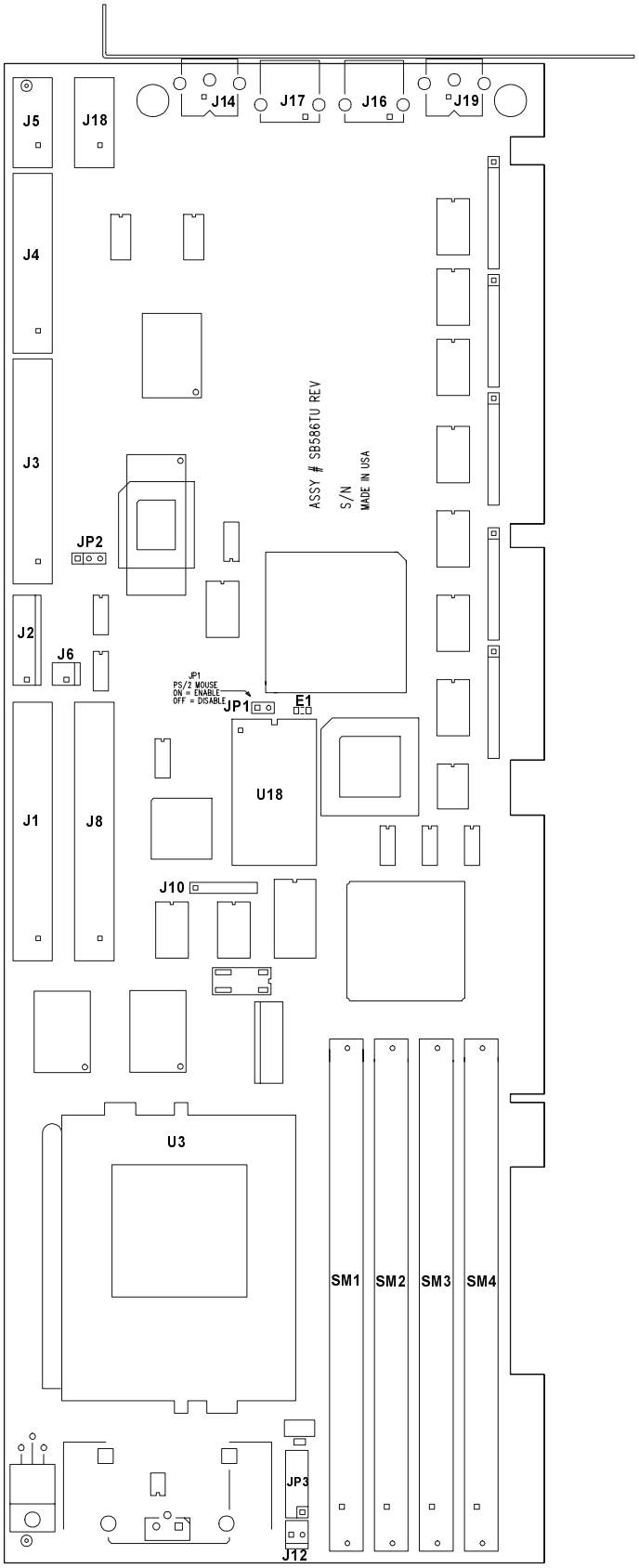


Figure 2-6: SB586TU (USB Port)

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Chapter 3: Installation

If you purchased your SB586T single board computer with a chassis, the board and its associated components will already be installed and tested. If you purchased your board separately or purchased it as an add-on, this chapter will cover the steps necessary to add the board to your existing system.

Installing the board may involve connecting input/output devices, adding components (such as memory), upgrading the processor, setting jumpers and switches, and setting up the operating system.

Depending on your system, you may only need to do some of these steps. However, since all components of the computer are interdependent, check this chapter whenever you need to install or replace components.

EIDE and Floppy Device Connection

The SB586T series has onboard controllers for EIDE and diskette drives. The primary and secondary EIDE connectors are J1 and J8, respectively. They both support LBA mode, and each will connect up to two devices. The diskette-drive connector is J3, and it will also connect up to two devices. The connectors are keyed so the cables will only connect in the correct direction.

SCSI Device Connection

The SB586TS and SB586TS2V have an onboard Adaptec AIC-7880 SCSI I/O processor to support ultra-wide SCSI data transfer rates of up to 40MB. This SCSI processor interfaces the PCI bus to an ultra-wide SCSI bus.

The SCSI controller at J9 supports up to 7 narrow or 15 wide SCSI devices. These SCSI devices may be connected in three configurations: 8-bit bus, 16-bit bus, or a combination of the two. If you plan to use SCSI 16-bit devices, you will need a 68-pin cable. If you plan to use both 8- and 16-bit devices, you must use an adapter.

A 68-pin–to–50-pin male-to-male adapter, ICS Advent P/N 50313-01, is available for a straight 8-bit SCSI bus chain. A 68-pin–to–50-pin female-to-female adapter, ICS Advent P/N 50314-01, may be used to place an 8-bit SCSI device on a 16-bit SCSI Wide bus.



CAUTION!



Use only SCSI adapters approved by ICS Advent, which performs extensive testing on its products. Use of other SCSI adapters to connect SCSI peripherals to the CPU board could damage the board, its components, or your equipment.

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In 16-bit SCSI wide chains, connect one end of the 68-pin cable to the CPU board, then connect the SCSI wide devices anywhere else on the cable. To add an 8-bit SCSI device to this chain, place the appropriate adapter on the cable connector and connect the narrow SCSI device to the adapter (**Figure 3-1**). The necessary signals for the 8-bit device are channeled through the adapter to the SCSI device. The additional 16-bit signals are not carried through the adapter and are sent down the SCSI chain. Because of these extra signals, you must place a 16-bit device with termination resistors at the end of the chain to ensure proper termination of all SCSI signals.

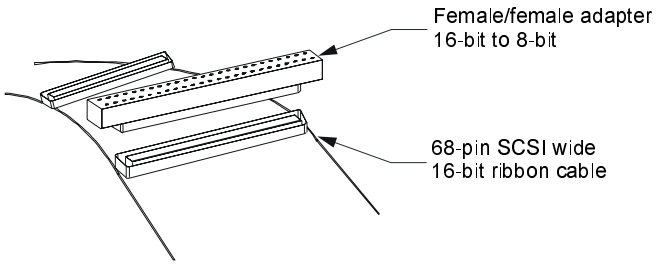


Figure 3-1: 68-to 50-Pin Adapter

If you need a straight 8-bit SCSI chain, place the 68-pin–to–50-pin male-to-male adapter on the 68-pin connector on the CPU board. From there, you may run a standard 50-pin ribbon cable to connect the 8-bit SCSI devices as needed (**Figure 3-2**).

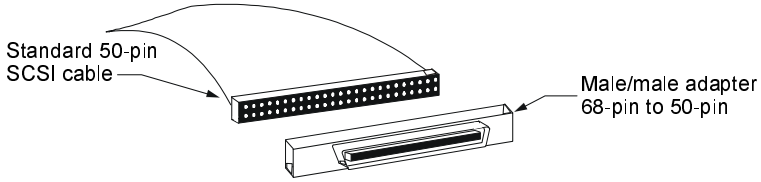


Figure 3-2: Straight 8-Bit SCSI Chain

The SCSI controller is assigned SCSI ID 7. It is not permanently terminated and therefore may appear anywhere on the SCSI cable. A SCSI device at each end of the cable must be terminated using termination resistors to insure the integrity of the SCSI signals. If the controller is at an end of the cable, you must terminate the device using SCSI utility software.

If your system does not already have a driver for the new SCSI device, you will need to install one as described in the following section.

SCSI Device Drivers

The SB586TS and SB586TS2V both have an onboard SCSI controller. This controller comes with supporting SCSI utility software that manages such details as controller termination. When booting your system, you have the option to configure the drivers or to boot normally.

Most operating systems automatically recognize devices properly installed in the SCSI port. This recognition allows you to install the operating system from a SCSI-type CD ROM. After installing the operating system, follow the instructions accompanying the SCSI device(s) to install any required drivers.

If your system does not recognize the SCSI CD ROM, carefully check for ID conflicts and proper device termination.

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Adding/Removing Board Components

Board components may need to be added, removed, and/or configured for your system. User-changeable board components include RAM, the CPU, and the CPU fan. The instructions below describe how to install or change these components.

Installing RAM

The SB586T series accepts up to 256MB of RAM. The four 72-pin RAM SIMM sockets will accept 32- and 36-bit SIMM modules in pairs. (**Figure 3-5** shows a basic board layout, or you can refer to the layouts in Chapter 2.)

Use only tinned lead SIMMs on your single board computer. Install 70ns (or faster) SIMMs to ensure reliable operation at zero-wait states. Memory SIMMs must be the same size in both sockets of a bank, and must be installed as a pair. ICS Advent recommends that the SIMMS be of the same manufacturer and speed.

Note: If you are installing DRAM, you may use FPM or EDO RAM, with or without parity. While EDO SIMMs are supported, FPM SIMMs with parity or ECC SIMMs are recommended for critical applications.



CAUTION!



SIMM sockets are rugged, but they can be broken. Use extreme care when removing a SIMM from its socket. Never force a SIMM into a socket and make sure the SIMM is in the correct orientation before installation. **SIMM sockets broken due to ABUSE, MISHANDLING, or ACCIDENT are not covered under the warranty.**

Follow these instructions to install RAM on your SB586T:

1. Take proper ESD precautions ***before*** starting any work.

2. Turn the SIMM so that the notched corner of the SIMM is closest to the edge of the board. The notch fits over a post at one end of the socket. This post allows the SIMM to be installed only in the correct direction (**Figure 3-3**).

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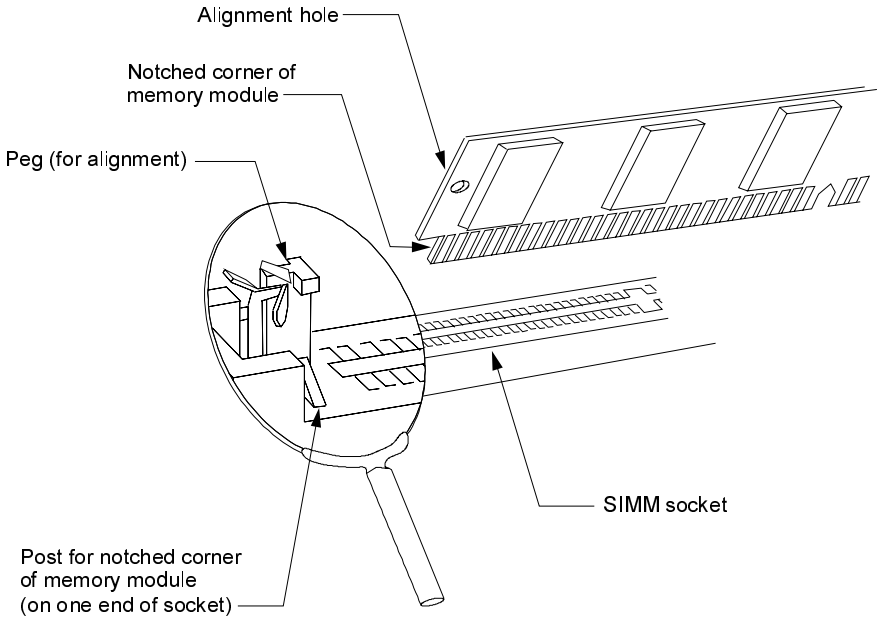


Figure 3-3: RAM Installation

3. Insert the SIMM into the socket at a 45-degree angle (approximately). Make sure the SIMM is completely seated in the socket (**Figure 3-4**).

4. Using both hands and applying equal pressure on each end of the module, push the module forward until it "clicks." This locks the SIMM into position. The pegs of the socket should be in the alignment holes of the SIMM.

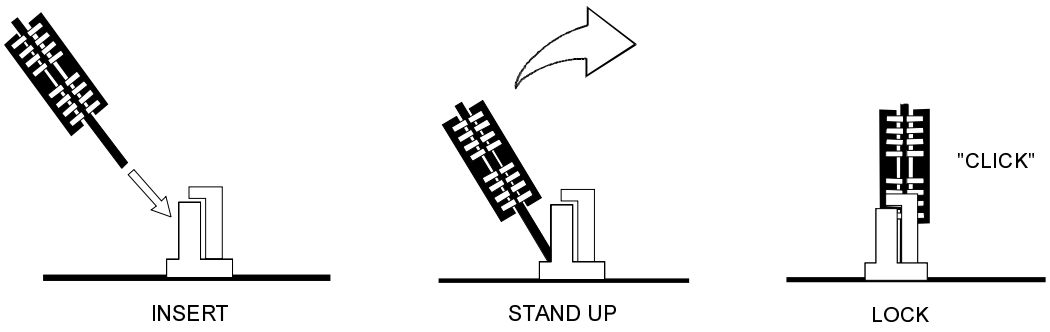


Figure 3-4: SIMM Installation

Installing the CPU and Fan

The SB586T series supports 100 to 300MHz processors. Model numbers ending with -166X, -200X, -233X, and -300 support MMX or 3DNow! technology.

SB586T boards are delivered with a CPU and a heatsink fan assembly. If you are installing a new CPU, ICS Advent recommends that you also use a heatsink fan assembly.

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CAUTION!

To avoid damage to your single-board computer when changing processors, you must adjust the settings on **both** S1 and JP3 (described later in this chapter).

Follow the steps below to install a new CPU onto your board.

1. Push the lever arm of the ZIF socket down and away from the socket. Then lift the arm to a vertical position.
2. Align the CPU with the ZIF socket so that pin 1 of the CPU is above pin 1 on the socket. When properly aligned, the angled corner of the CPU aligns with the angled corner of the socket.
3. Place the CPU in the socket. When properly positioned, the CPU will drop into place.
4. Lower the ZIF socket lever to its original position to lock the CPU into place.
5. Make sure that S1 and JP3 are correctly set for the new processor. Otherwise, your system may run more slowly than required or the processor may be damaged. Refer to the sections on jumper settings and processor speed settings, later in this chapter.
6. Refer to instructions provided with your heatsink fan assembly to install the CPU fan.
7. Connect the fan to the power connector at J12 (**Figure 3-5**).

Jumper Settings

The SB586T series has three jumpers and a DIP switch that may require adjustment. **Figure 3-5** shows the jumper locations. (JP2 has different locations in the SB586TT and SB586TU boards, but this jumper presently requires no customer attention on any board in the SB586T series.)

JP1

JP1 allows you to enable IRQ12 and disable a PS/2 mouse. If you need the interrupt, but do not need the mouse, just remove the shunt.

JP2

JP2 is for factory use only.

JP3

JP3 sets voltage levels for different processors. If you change the processor, you must change the settings on S1 **and** JP3. Both S1 and JP3 are discussed in more detail later in this chapter.

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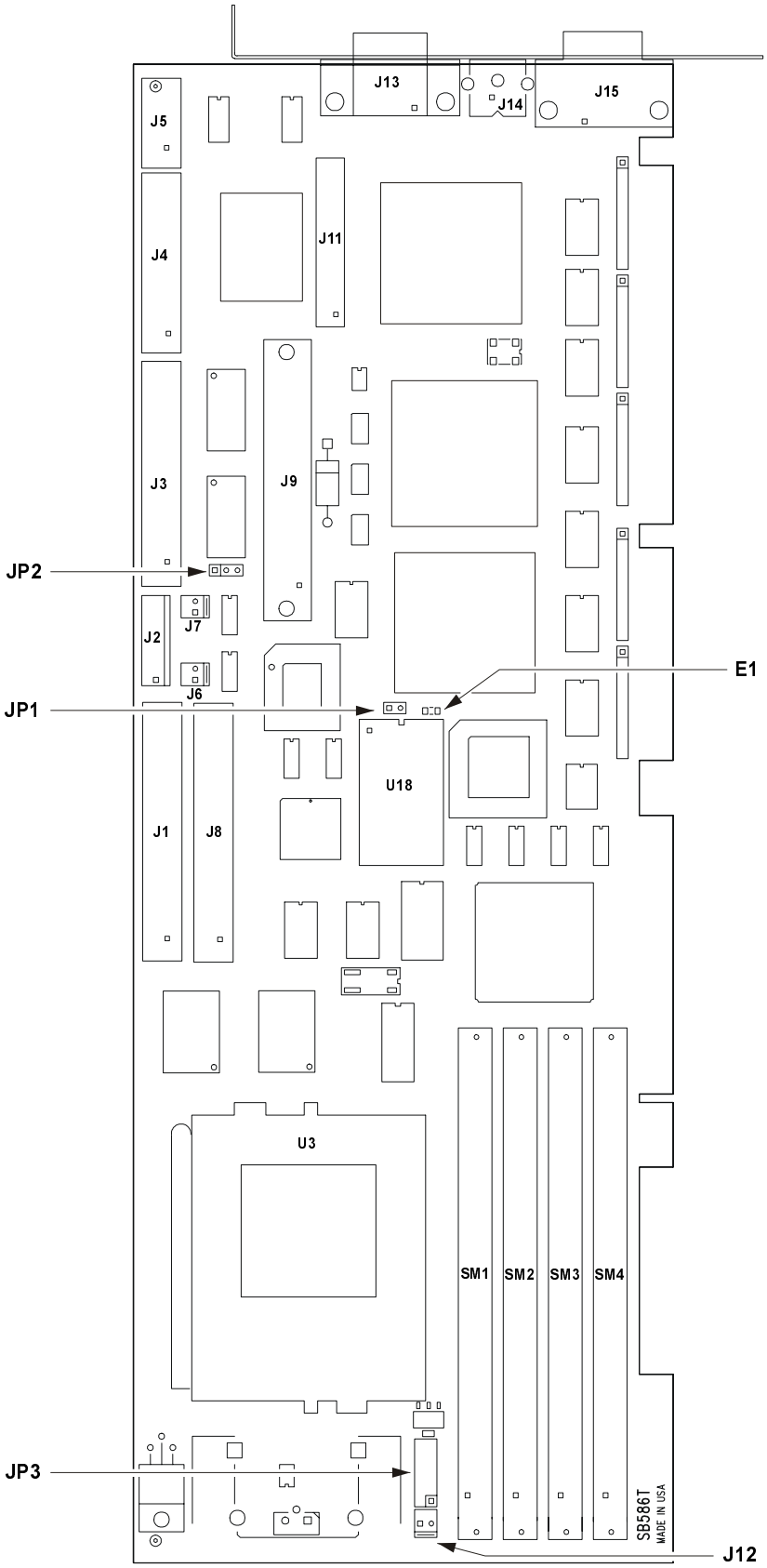


Figure 3-5: Component Locations

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DIP Switch

S1, located on the *back* of the SB586T board, lets you clear the CMOS password, enable the onboard watchdog timer, and set the bus speed for the CPU. **Figure 3-6** shows the location and functions of S1. This switch is discussed in more detail later in this chapter.

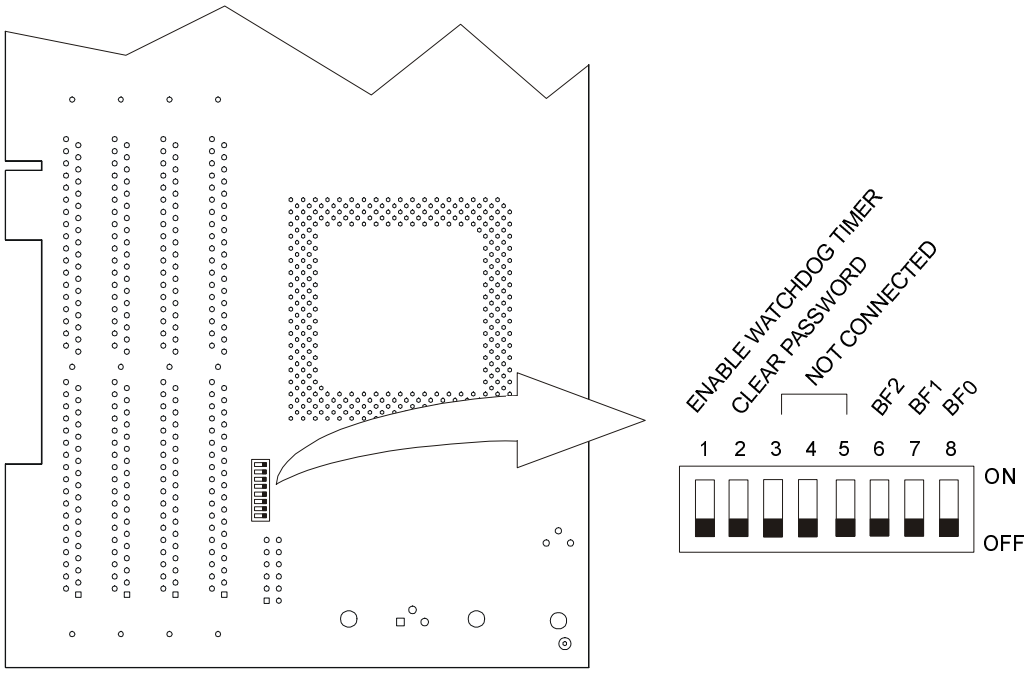


Figure 3-6: S1 Location and Functions

Note: To clear CMOS settings with the power **off**, short across the two pads at E1, next to the CMOS chip at U18, shown in **Figure 3-5**.

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Processor Speed Settings

When you receive your SB586T single board computer, it will be correctly set for the processor installed at the time of purchase. If you upgrade to a different processor, you must adjust the voltage level on JP3 and the processor speed on S1.

CAUTION!

To avoid damage to your single-board computer when changing processors, you must adjust the settings on **both** JP3 and S1.

Figure 3-7 shows how to set the voltage level on JP3.

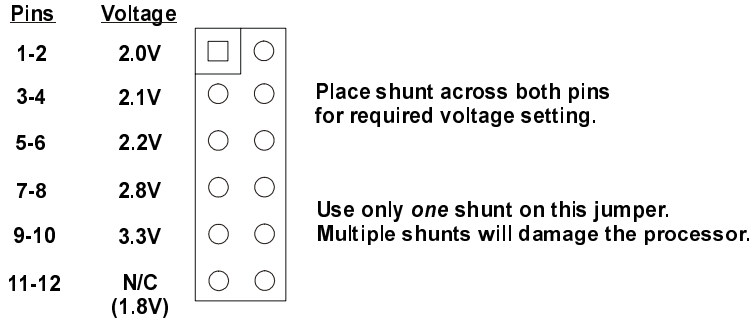


Figure 3-7: JP3 Voltage Settings

CAUTION!

To avoid damaging your processor, use only ***one*** shunt on JP3.

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Table 3-1 shows the processor speeds on S1 and the voltage levels on JP3. You need to match these values to your new processor. (Check your invoice or contact Industrial Computer Source at 800-480-0044 if you have any questions about your new processor type or speed.)

Table 3-1: S1 Base Fraction and JP3 Voltage Settings

		S1			JP3 PINS					
	MHz	BF0	BF1	BF2	1-2	3-4	5-6	7-8	9-10	11-12
INTEL	100	OFF	OFF	OFF	OPEN	OPEN	OPEN	OPEN	SHORT	OPEN
	133	ON	OFF	OFF	OPEN	OPEN	OPEN	OPEN	SHORT	OPEN
	166	ON	ON	OFF	OPEN	OPEN	OPEN	OPEN	SHORT	OPEN
	200	OFF	ON	OFF	OPEN	OPEN	OPEN	OPEN	SHORT	OPEN
INTEL WITH MMX	166	ON	ON	OFF	OPEN	OPEN	OPEN	SHORT	OPEN	OPEN
	200	OFF	ON	OFF	OPEN	OPEN	OPEN	SHORT	OPEN	OPEN
	233	OFF	OFF	OFF	OPEN	OPEN	OPEN	SHORT	OPEN	OPEN
AMD-K6-2	266	ON	OFF	ON	OPEN	OPEN	SHORT	OPEN	OPEN	OPEN
	300	ON	ON	ON	OPEN	OPEN	SHORT	OPEN	OPEN	OPEN

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Chapter 4: Maintenance and Troubleshooting

This chapter provides minimal maintenance and troubleshooting information for your SB586T single board computer. If you would like assistance with these procedures, please call Technical Support at **800-480-0044** (U.S.) or **858-677-0877** (international).

Troubleshooting

All components of a computer are interrelated. That is, a "video" problem may be caused by the disk controller. The simplest diagnostic technique involves replacing the suspect card with a new one. If that doesn't fix the problem, remove all cards except for the minimum required by the system. Then run the system, replacing each card until the problem occurs.

FCC Compliance Statement for FCC Class A Devices

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and radiates radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: The assembler of a personal computer system may be required to test the system and/or make necessary modifications if a system is found to cause harmful interference or to be non-compliant with the appropriate standards for its intended use.

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How to Remain CE Compliant

The SB586T Series boards are designed to be CE compliant when used in CE compliant chassis. Maintaining CE compliance also requires proper cable and cabling techniques. Although ICS Advent offers accessories, the customer must ensure that these products are installed with proper shielding to maintain CE compliance. ICS Advent does not offer engineering services for designing cabling systems. In addition, ICS Advent will not retest or recertify systems or components that have been reconfigured by customers.



WARNING!



The following procedures involve working with high voltage. Contact with this voltage may cause serious injury. Accidental shorting of the circuits can damage the computer.



CAUTION!



The following procedures involve working with a device that is sensitive to static electricity. Use proper precautions to protect against electrostatic discharge (ESD). Only qualified personnel should attempt these procedures.

CPU does not boot, there is no beep, and no video.

A. Ensure that the CPU is fully seated in the CPU socket and is correctly oriented to pin 1.

B. With power off, clear CMOS by shorting across E1 as discussed at the end of Chapter 3, then try booting your system again.

C. Contact Customer Service at **800-480-0044** (U.S. and Canada) or **858-677-0877** (international) to receive the latest BIOS flash file. Refer to Appendix A for BIOS upgrade instructions.

When booting, system reports 'No SCSI Boot Device Found'.

A. This message appears if there is no bootable device on the SCSI bus. Disable the SCSI controller in CMOS setup if no SCSI devices are being used.

B. If a SCSI hard drive is installed, make sure that all cables and power connectors are attached to the SCSI peripherals.

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C. Ensure that SCSI signals are properly terminated. Only the last physical SCSI device on the bus should be terminated. (Refer to Chapter 3 for more information on connecting SCSI devices.)

Hard Disk Drive Controller failure on bootup.

A. If you are using an IDE hard drive to boot, ensure that the power connector and the ribbon cable are properly connected.

B. Check that the drive is configured properly as Master or Slave by jumpers on the drive.

C. Check that the HDD parameters are set up correctly in the CMOS Setup. (You can use auto-detect on the hard disk to find the correct HDD parameters.)

When booting, the SCSI BIOS banner does not appear.

A. Either the onboard SCSI is not enabled in CMOS or no interrupts are allocated to PCI devices in the CMOS chipset setup. At least one IRQ must be allocated for each PCI device on the bus. You can get an extra IRQ by disabling a jumper at JP1. However, when you disable the jumper, you will not be able to use a mouse with your system.

Non-Plug-and-Play ISA card is not functioning properly.

A. If this card uses an IRQ, make sure that the particular IRQ is reserved to the 'ISA' bus in the CMOS chipset setup.

When booting, CPU reports No ROM BASIC.

A. The system cannot find a proper bootable sector on either drive A or C. You need to install an operating system on the hard drive or insert a bootable diskette in the A drive.

When booting, system gives eight beeps.

A. These beeps indicate a video adapter problem. Try the video card in a different slot.

B. Try a different video card.

C. If you are installing an external video card, check whether the CPU has onboard video. If it does, you need to disable the onboard PCI video in the CMOS chipset setup before installing the external video card.

D. If the problem persists, clear CMOS and reflash the BIOS as discussed in Appendix A.

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Note: If you have the SB586T2V or the SB586TS2V and you are using a separate video card, clear CMOS to enable the onboard PCI Video option in the CMOS chipset setup.

When booting, system gives two beeps.

A. Two beeps signify a parity error. Reseat the memory SIMMs into the SIMM sockets and reboot.

B. If the problem persists, swap SIMMs from one memory bank to the other. If the problem resolves after swapping, then swap the memory back to the original installation and see if the original error occurs.

C. If the problem still persists after swapping, install spare memory modules in the CPU.

D. If the problem still persists after installing new memory, then the CPU board may have faulty SIMM sockets and may need to be returned for repair.

System runs very slowly.

A. The system runs significantly slower if the cache memory has been disabled in advanced CMOS setup. (Cache memory is automatically disabled when you choose the Fail-Safe option in CMOS Setup.)

B. Check that S1 and JP3 are set correctly for the processor speed and voltage as discussed in Chapter 3.

Returns

If you need to return a product to ICS Advent for any reason, follow the steps below:

1. Call Customer Service at **800-480-0044** (U.S.) or **858-677-0877** (international) for a Return Material Authorization (RMA) number. The RMA number must be visible on the outside of the box in which you pack the product. Shipments without an RMA number will not be accepted by Customer Service Receiving.
2. Properly pack the product. Put the board in a bag to protect against moisture and dirt.
3. Provide adequate packaging and use standard electrostatic discharge (ESD) precautions. If possible, use the original box and packing in which the product arrived. A minimum of four inches of proper packing material is required around all sides of computer products. Double-thick cardboard is preferred. **Do not use styrofoam peanuts or loose fill to pack.** Assume the box will be dropped several feet during shipping.
4. Use a reputable carrier such as Burlington, Airborne, or Federal Express.

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Appendix A: AMIBIOS 95

For the Intel 82430HX Triton II ISA Chipset

For PCI PnP ISA Systems

With Flash ROM Support *User's Guide*

Based on the Enhanced 7/15/95 Core AMIBIOS (Version 6.30)

TritonIIISA715

3/3/96

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American Megatrends, Inc.
6145-F Northbelt Parkway
Norcross, GA 30071

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Revision History

3/3/96	Initial release for AMIBIOS 95 (Enhanced 7/15/95 Core AMIBIOS and 7/15/95 Core AMIBIOS).

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Preface

Technical Support

If AMIBIOS fails to operate as described or you need more information, call technical support at 770-246-8645. Make sure you have the following information before calling:

- Serial number and revision number of the BIOS
- System BIOS reference number
- A clear description of the problem.

Acknowledgments

This manual was written and edited by Paul Narushoff. The writer gratefully acknowledges the assistance of the BIOS engineers.

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Chapter 1: Introduction

This manual documents the AMIBIOS for the Intel 82430HX Triton II PCI Chipset based on the AMIBIOS 95 Core AMIBIOS. This AMIBIOS is designed for a Pentium-based ISA computer system. This AMIBIOS also supports IDE on the PCI local bus.

Plug and Play Support

This AMIBIOS supports the Plug and Play Version 1.0A specification.

PCI Bus Support

This AMIBIOS also supports the Intel PCI (Peripheral Component Interconnect) local bus specification. Please see the Intel technical documentation for additional information.

SRAM Cache Memory Support

This AMIBIOS supports asynchronous and burst SRAM. This AMIBIOS automatically detects the cache memory type and size.

DRAM Support

EDO (Extended Data Out), FPM (Fast Page Mode), and ECC (Error Correction Code) DRAM memory is supported.

Flash ROM Support

Flash ROM support is also included in this AMIBIOS.

The Intel 28F001BXT flash EEPROM is supported. To reprogram the flash ROM, make an update BIOS ROM file and name the file AMIBOOT.ROM. Copy this file to a floppy. The end user can insert the floppy drive in drive A: and press <Ctrl> <Home> while powering on.

PCI SCSI BIOS Support

The Adaptec 7880 PCI SCSI support is included in the system BIOS for the onboard SCSI PCI controller. This AMIBIOS gains control if a Adaptec 7880 SCSI device is detected.

System BIOS

The BIOS is the basic input output system used in all IBM® PC-, XT™-, AT®-, and PS/2®-compatible computers. The AMIBIOS is a high-quality example of a system BIOS.

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Configuration Data

AT-Compatible systems, also called ISA (Industry Standard Architecture), must have a place to store system information when the computer is turned off. The original IBM AT had 64 bytes of nonvolatile memory storage in CMOS RAM. All AT-Compatible systems have at least 64 bytes of CMOS RAM, which is usually part of the Real Time Clock. Many systems have 128 bytes of CMOS RAM.

How Data Is Configured

AMIBIOS provides a Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup configures data in CMOS RAM.

The AMIBIOS Setup utility included in the AMIBIOS for the Intel Triton II ISA Chipset can also be executed via a hot key.

Types of AMIBIOS Setup

Types of Setup	Description
Standard Setup	Sets time, date, hard disk type, types of floppy drives, monitor type, and if keyboard is installed.
Advanced Setup	Sets Typematic Rate, Memory Test, Hit <Del> Message Display, Boot Up Sequence, and many others.
Chipset Setup	Sets chipset-specific options and features.
PCI/PnP Setup	Sets options related to the PCI bus and Plug and Play features.
Peripheral Setup	Controls I/O Controller-related options.

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Chapter 2: Standard CMOS Setup

The Setup options described in this section are displayed by choosing Standard CMOS Setup icon from the AMIBIOS HIFLEX Setup Utility main menu. All Standard Setup options are described in this section.

Default Settings

Every option in AMIBIOS Setup contains two default values: an Fail-Safe default and the Optimal default value.

Optimal Defaults

The Optimal default values provide optimum performance settings for all devices and system features.

Fail-Safe Defaults

The Fail-Safe default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

Date/Time

Select the Date/Time option to change the date or time. The current date and time are displayed. Enter new values with the PageUp and PageDown keys.

Floppy Drive A, B

Choose the Floppy Drive A or B icon to specify the floppy drive type. The settings are *360 KB 5¼”*, *1.2 MB 5¼”*, *720 KB 3½”*, *1.44 MB 3½”*, or *2.88 MB 3½”*.

Pri Master

Pri Slave

Sec Master

Sec Slave

Choose these entries to configure the hard disk drive named in the option. When you select an entry, the following parameters are listed: Type, LBA/Large Mode, Block Mode, 32Bit Mode, and PIO Mode. All parameters relate to IDE drives except **Type.**

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Configuring an MFM Drive

If configuring an old MFM hard disk drive, you must know the drive parameters (number of heads, number of cylinders, number of sectors, the starting write precompensation cylinder, and drive capacity). Choose **Type** and choose the appropriate hard disk drive type (1 - 46). The old MFM hard drive types are listed on page **A-5**. If the drive parameters of your MFM drive do not match any drive type listed on page **A-5**, select *User* in the **Type** field and enter the drive parameters on the screen that appears.

User-Defined Drive

If you are configuring a SCSI drive or an MFM, RLL, ARLL, or ESDI drive with drive parameters that do not match drive types 1-46, you must select *User* in the **Type** field. You must then enter the drive parameters on the screen that appears. The drive parameters include:

Parameter	Description
Type	The number for a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
Write Precompensation	The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where write precompensation begins.
Landing Zone	This number is the cylinder location where the heads will normally park when the system is shut down.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drives have more sectors per track.
Capacity	The formatted capacity of the drive is (Number of heads) x (Number of cylinders) x (Number of sectors per track) x (512 bytes per sector)

Configuring IDE Drives

If the hard disk drive to be configured is an IDE drive, select the appropriate drive (Pri Master, Pri Slave, Sec Master, or Sec Slave). Choose the **Type** parameter and select Auto.

AMIBIOS automatically detects the IDE drive parameters and displays them. Click on the OK button to accept these parameters.

Select **LBA/Large Mode** and choose *On* to enable support for IDE drives with capacities greater than 528 MB.

Select **Block Mode** and choose *On* to support IDE drives that use Block Mode.

Select **32Bit Mode** and click on *On* to support IDE drives that permit 32-bit accesses.

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Configuring a CD-ROM Drive

Select the appropriate drive icon (Pri Master, Pri Slave, Sec Master, or Sec Slave). Choose the **Type** parameter and select CDROM. You can boot the computer from a CD-ROM drive.

Hard Disk Drive Types

Type	Cylinders	Heads	Write Precompensation	Landing Zone	Sectors	Capacity
1	306	4	128	305	17	10 MB
2	615	4	300	615	17	20 MB
3	615	6	300	615	17	31 MB
4	940	8	512	940	17	62 MB
5	940	6	512	940	17	47 MB
6	615	4	65535	615	17	20 MB
7	462	8	256	511	17	31 MB
8	733	5	65535	733	17	30 MB
9	900	15	65535	901	17	112 MB
10	820	3	65535	820	17	20 MB
11	855	5	65535	855	17	35 MB
12	855	7	65535	855	17	50 MB
13	306	8	128	319	17	20 MB
14	733	7	65535	733	17	43 MB
16	612	4	0	663	17	20 MB
17	977	5	300	977	17	41 MB
18	977	7	65535	977	17	57 MB
19	1024	7	512	1023	17	60 MB
20	733	5	300	732	17	30 MB
21	733	7	300	732	17	43 MB
22	733	5	300	733	17	30 MB
23	306	4	0	336	17	10 MB
24	925	7	0	925	17	54 MB
25	925	9	65535	925	17	69 MB
26	754	7	754	754	17	44 MB
27	754	11	65535	754	17	69 MB
28	699	7	256	699	17	41 MB
29	823	10	65535	823	17	68 MB
30	918	7	918	918	17	53 MB
31	1024	11	65535	1024	17	94 MB
32	1024	15	65535	1024	17	128 MB
33	1024	5	1024	1024	17	43 MB
34	612	2	128	612	17	10 MB
35	1024	9	65535	1024	17	77 MB
36	1024	8	512	1024	17	68 MB
37	615	8	128	615	17	41 MB
38	987	3	987	987	17	25 MB
39	987	7	987	987	17	57 MB
40	820	6	820	820	17	41 MB
41	977	5	977	977	17	41 MB
42	981	5	981	981	17	41 MB
43	830	7	512	830	17	48 MB
44	830	10	65535	830	17	69 MB
45	917	15	65535	918	17	114 MB
46	1224	15	65535	1223	17	152 MB
USER-DEFINED HARD DRIVE - Enter user-supplied parameters.						

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Chapter 3: Advanced CMOS Setup

The AMIBIOS Setup options described in this section are displayed by choosing Advanced CMOS Setup from the AMIBIOS HIFLEX Setup Utility main menu. All Advanced Setup options are described in this section.

Quick Boot

Set this option to ENABLED to permit AMIBIOS to boot within 5 seconds. This option replaces the old **Above 1 MB Memory Test** option. The optimal and fail-safe default settings are *DISABLED.*

Setting	Description
DISABLED	AMIBIOS tests all system memory. AMIBIOS wait up to 40 seconds for a READY signal from the IDE drive. AMIBIOS waits up to .5 seconds after sending a RESET signal to the IDE drive to permit the IDE drive to send a READY signal. AMIBIOS checks if the <Del> key was pressed. Setup is executed if <Del> was pressed.
ENABLED	AMIBIOS does not test any system memory above 1 MB. AMIBIOS does not wait for a READY signal from the IDE drive. If a READY signal is not received immediately, AMIBIOS does not configure the drive. AMIBIOS does not wait .5 seconds after sending a RESET signal to the IDE drive. AMIBIOS does not check if the <Del> key was pressed.

Boot Up Num Lock

When this option is set to ON, AMIBIOS turns off the NUM LOCK key when the system is powered on so the end user can use the arrow keys on both the numeric keypad and the keyboard. The settings are ON or OFF. The optimal default and fail-safe default settings are *ON.*

1st Boot Device

This option sets the sequence of boot drives for the first boot device that AMIBIOS attempts to boot from after POST completes. The settings are DISABLED, IDE-0, IDE-1, IDE-2, IDE-3, FLOPPY, FLOPTICAL, SCSI, CD-ROM, or NETWORK. The optimal and fail-safe default settings are *FLOPPY.*

2nd Boot Device

These options set the sequence of boot drives for boot devices. The 2nd Boot Device settings are DISABLED, IDE-0, FLOPPY, FLOPTICAL, OR CDROM. The optimal and fail-safe default settings are *IDE-0.*

3rd Boot Device

The settings are DISABLED, IDE-0, FLOPPY, FLOPTICAL, OR CDROM. The optimal and fail-safe default settings are *CD-ROM.*

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Try other Boot Devices

This option requests BIOS to search for other boot devices. The settings are YES or NO. The optimal and fail-safe default settings are *YES*.

Floppy Access Control

This option controls access to the floppy drive(s). The settings are READ-WRITE or READ-ONLY. The optimal and fail-safe default settings are *READ-WRITE*.

Hard Disk Access Control

This option controls access to the hard drive(s). The settings are READ-WRITE or READ-ONLY. The optimal and fail-safe default settings are *READ-WRITE*.

S.M.A.R.T. for Hard Disks

Set this option to ENABLED to permit AMIBIOS to use the S.M.A.R.T. (Self-Monitoring, Analysis and Reporting Technology). S.M.A.R.T. can help prevent data loss and unscheduled computer downtime. It provides advance warning of certain types of drive failures, allowing the user of data-management software to back up the data. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED*.

BootUp Num-Lock

Set this option to OFF to turn the Num Lock key off when the computer is booted so you can use the arrow keys on both the numeric keypad and the keyboard. The settings are ON or OFF. The optimal and fail-safe default settings are *ON*.

Floppy Drive Swap

Set this option to ENABLED to permit drives A: and B: to be swapped. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *DISABLED*.

System Keyboard

This option does not specify whether or not a keyboard is attached to the computer. Rather, it specifies whether error messages are displayed if a keyboard is not attached. This option permits you to configure workstations with no keyboards. The settings are ABSENT or PRESENT. The optimal and fail safe default settings are *PRESENT*.

Primary Display

This option configures the primary display subsystem in the computer. The settings are MONO (monochrome), 40CGA, 80CGA, or VGA/EGA. The optimal and fail-safe default settings are *VGA/EGA*.

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Password Check

This option specifies the type of AMIBIOS password protection that is implemented. The optimal and fail-safe default settings are SETUP. The settings are:

Setting	Description
SETUP	The password prompt appears only when an end user attempts to run WINBIOS Setup.
ALWAYS	A password prompt appears every time the computer is powered on or rebooted.

The AMIBIOS password does not have to be enabled. The end user sets the password by choosing the Password icon on the Setup screen.

Boot to OS/2

Set this option to YES to permit AMIBIOS to run properly if OS/2 or any other operating system that does not support Plug and Play is to be run on this computer. The settings are YES or NO. The optimal and fail-safe default settings are *NO*.

Wait for 'F1' If Error

AMIBIOS POST runs system diagnostic tests that can generate a message followed by:

Press <F1> to continue.

If this option is set to ENABLED, AMIBIOS waits for the user to press <F1> before continuing bootup. If this option is set to DISABLED, AMIBIOS continues the boot process without waiting for <F1> to be pressed. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED*.

Internal Cache

This option selects the type of caching algorithm used by AMIBIOS and the CPU for L1 cache memory (internal to the CPU). The settings are:

Setting	Description
WRITEBACK	A write-back algorithm is used.
DISABLED	AMIBIOS does not specify the type of caching algorithm. The algorithm is set by the CPU.

The optimal and fail-safe default settings are *WRITEBACK*.

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External Cache

This option selects the type of caching algorithm used by AMIBIOS and the CPU for L2 secondary (external) cache memory. The settings are:

Setting	Description
WRITEBACK	A write-back algorithm is used.
WRITE-THROUGH	A write-through algorithm is used.
DISABLED	AMIBIOS does not specify the type of caching algorithm.

The optimal default setting is *WRITEBACK*. The fail-safe default setting is *DISABLED*.

System BIOS Cacheable

AMIBIOS always copies the system BIOS from ROM to RAM for faster execution. Set this option to ENABLED to permit the contents of the F0000h RAM memory segment to be written to and read from cache memory. The settings are ENABLED or DISABLED. The optimal default setting is *ENABLED*. The fail-safe default setting is *DISABLED*.

C000, 16K Shadow

C400, 16K Shadow

These options specify how the contents of the video ROM are handled. The settings are:

Setting	Description
DISABLED	The Video ROM is not copied to RAM.
CACHED	The contents of the video ROM area from C0000h - C7FFFh are not only copied from ROM to RAM, the contents of the C0000h - C7FFFh RAM area can be written to or read from cache memory.
SHADOW	The contents of the video ROM area from C0000h - C7FFFh are copied (shadowed) from ROM to RAM for faster execution.

The optimal default setting is *CACHED*. The fail-safe default setting is *DISABLED*.

C800,16K Shadow

CC00,16K Shadow

D000,16K Shadow

D400,16K Shadow

D800,16K Shadow

DC00,16K Shadow

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These options specify how the contents of the adaptor ROM named in the option title are handled. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards. The settings are:

Setting	Description
DISABLED	The specified ROM is not copied to RAM.
CACHE	The contents of the ROM area are not only copied from ROM to RAM for faster execution, the contents of the RAM area can be written to or read from cache memory.
SHADOW	The contents of the ROM area are copied from ROM to RAM for faster execution.

The optimal and fail-safe default settings are *DISABLED*.

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Chapter 4: Advanced Chipset Setup

Choose Advanced Chipset Setup from the AMIBIOS HIFLEX Utility Setup main menu. All Chipset Setup options are then displayed and are described in this chapter.

Global Triton2 Enable

Set this option to ENABLED to enable the Triton II chipset. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED.*

Memory Hole

This option allows the end user to specify the location of a memory hole. The settings are DISABLED, 512-640K, or 15-16M (from 15 MB to 16 MB). The optimal and fail-safe default settings are *DISABLED.*

IRQ12/M Mouse Function

Set this option to ENABLED to have AMIBIOS support the onboard PS/2-type mouse. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED.*

If you need to use IRQ12 for other hardware in the system, you must disable the IRQ12/M mouse function and remove the JP1 jumper.

8-Bit I/O Recovery Time

This option specifies the length of a delay inserted between consecutive 8-bit I/O operations. The settings are DISABLED, 1 (SYSCLK), 2 (SYSCLKs), 3 (SYSCLKs), 4 (SYSCLKs), 5 (SYSCLKs), 6 (SYSCLKs), or 7 SYSCLKs. The optimal and fail-safe default settings are *1.*

16-Bit I/O Recovery Time

This option specifies the length of a delay inserted between consecutive 16-bit I/O operations. The settings are DISABLED, 1 (SYSCLK), 2 (SYSCLKs), 3 (SYSCLKs), or 4 (SYSCLKs). The optimal and fail-safe default settings are *1.*

DRAM Timings

This option specifies the RAS access time for the DRAM used in the computer for system memory. The settings are 60ns, MANUAL, or 70ns. The optimal and fail-safe default settings are *60ns.*

Refresh Rate

This option specifies the system memory refresh rate. The settings are 50 MHz, 60 MHz, or 66 MHz. The optimal and fail-safe default settings are *66 MHz.*

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Turbo Read Leadoff

The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are DISABLED.

Read Burst Timing

This option sets the timing for system memory burst mode read operations. The settings are x222, x333, or x444. The optimal and fail-safe default settings are *x333.*

Write Burst Timing

This option sets the timing for system memory burst mode write operations. The settings are x222, x333, or x444. The optimal and fail-safe default settings are *x333.*

Fast RAS To CAS Delay (Clocks)

This option specifies the length of a delay inserted between the system memory RAS and CAS pulses in CPU clock cycles. The settings are 2 or 3. The optimal and fail-safe default setting is *3.*

Leadoff Timing

This option sets the leadoff timings. The settings are 6/5/3/4, 6/5/4/5, 7/6/3/4, or 7/6/4/5. The optimal and fail-safe default settings are *7/6/3/4.*

Speculative Leadoff

The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are DISABLED

Turnaround Insertion

The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are DISABLED

Memory Address Drive Strength

This option sets the signal strength for system memory banks 0 and 1. The settings are 8ma/8ma, 8ma/12ma, 12ma/8ma, or 12ma/12ma. The Optimal and Fail-Safe default settings are *8ma/8ma.*

TypeF DMA Buffer Control1

TypeF DMA Buffer Control2

These options specify the DMA channel that uses Type F DMA buffer control. The settings are DISABLED, CHANNEL 0, CHANNEL 1, CHANNEL 2, CHANNEL 3, CHANNEL5, CHANNEL 6, or CHANNEL 7. The optimal and fail-safe default settings are *DISABLED.*

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NA Disabled (NAD) for Ext Cache

Set this option to ENABLED to disable NAD for L2 secondary (external) cache memory. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED.*

Peer Concurrency

Set this option to ENABLED to enable PCI peer-to-peer concurrency. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED.*

DRAM Integrity Mode

Use this option to set the system memory integrity mode. The settings are PARITY, ECC LEVEL1, ECC LEVEL2, or DISABLED. The PARITY setting allows parity checking for system memory. LEVEL 1 ECC provides the minimal level of ECC support using the system's standard NMI (non-maskable interrupt) routine. LEVEL2 ECC adds error scrubbing of correctable errors using operating-system-independent mechanisms such as SMIs (system management interrupts). The optimal and fail-safe default settings are *DISABLED*.

PCI 2.1 Passive Release Enable

Set this option to ENABLED to enable the PCI passive release feature defined in Version 2.1 of the PCI specification. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED.*

Delayed Transaction Enable

Set this option to ENABLED to enable the delayed transaction feature. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED.*

North Bridge Retry Enable

The 430HX chipset involves the TXC (North Bridge chip) and the PIIX3 (South Bridge chip). North Bridge Retry Enable is used to enable delayed transactions between the North and South Bridge chips of the chipset. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED.*

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Chapter 5: PCI/PnP Setup

Choose PCI/Plug and Play Setup entry from the AMIBIOS HIFLEX Setup screen to display the PCI and Plug and Play Setup options, described below.

Plug and Play-Aware OS

Set this option to YES if the operating system in this computer is aware of and follows the Plug and Play specification. Currently, only Windows 95 is PnP-aware. The settings are YES or NO. The optimal and fail-safe default settings *NO.*

PCI Latency Timer (PCI Clocks)

This option specifies the latency timings (in PCI clocks) for all PCI devices on the PCI bus. The settings are 32, 64, 96, 128, 160, 192, 224, or 248. The Optimal and Fail-Safe default settings are *64.*

PCI VGA Palette Snoop

When this option is set to ENABLED, multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled). For example, if there are two VGA devices in the computer (one PCI and one ISA) and the:

VGA Palette Snoop Bit Setting	Action
DISABLED	Data read and written by the CPU is only directed to the PCI VGA device's palette registers.
ENABLED	Data read and written by the CPU is directed to the both the PCI VGA device's palette registers and the ISA VGA device palette registers, permitting the palette registers of both devices to be identical.

This option must be set to ENABLED if any ISA adapter card installed in the system requires VGA palette snooping. The settings are ENABLED or DISABLED. The Optimal and Fail-Safe default settings are *DISABLED.*

PCI IDE Bus Master

Set this option to ENABLED to specify that the IDE controller on the PCI local bus includes a bus mastering capability. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *DISABLED.*

Offboard PCI IDE Card

This option specifies if an offboard PCI IDE controller adapter card is installed in the computer. You must specify the PCI expansion slot on the motherboard where the offboard PCI IDE controller is installed. If an offboard PCI IDE controller is used, the onboard IDE controller is automatically

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disabled. The settings are AUTO (AMIBIOS automatically determines where the offboard PCI *IDE* controller adapter card is installed), SLOT1, SLOT2, SLOT3, or SLOT4. The optimal and fail-safe default settings are *AUTO.*

In the AMIBIOS for the Intel Triton II ISA chipset, this option forces IRQ14 and IRQ15 to a PCI slot on the PCI Local bus. This is necessary to support non-compliant ISA IDE controller adapter cards.

If an offboard PCI IDE controller adapter card is installed in the computer, you must also set the **Offboard PCI IDE Primary IRQ** and **Offboard PCI IDE Secondary IRQ** options.

Offboard PCI IDE Primary IRQ

Offboard PCI IDE Secondary IRQ

These options specify the PCI interrupt used by the Primary (or secondary) IDE channel on the offboard PCI IDE controller. The settings are *Disabled, Hardwired, INTA, INTB, INTC,* or *INTD.* The optimal and fail-safe default settings are *Disabled.*

DMA Channel 0

DMA Channel 1

DMA Channel 3

DMA Channel 5

DMA Channel 6

DMA Channel 7

These options specify the bus for each DMA Channel. These options allow you to reserve DMA Channels for legacy ISA adapter cards. The settings are PnP or ISA/EISA. The optimal and fail-safe settings are PnP.

IRQ3

IRQ4

IRQ5

IRQ7

IRQ9

IRQ10

IRQ11

IRQ12

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IRQ14

IRQ15

These options specify the bus that the specified IRQ line is used on. These options allow you to reserve IRQs for legacy ISA adapter cards.

These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to devices that are configurable by the system BIOS. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an ISA/EISA setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are configured as PCI/PNP. IRQ14 and 15 will not be available if the onboard Triton II ISA PCI IDE is enabled. If all IRQs are set to ISA/EISA and IRQ14 and 15 are allocated to the onboard PCI IDE, IRQ9 will still be available for PCI and PNP devices, because at least one IRQ must be available for PCI and PnP devices. The settings are ISA/EISA or PCI/PNP. The optimal and fail-safe default settings for all IRQs are PCI/PNP.

Reserved Memory Size

This option specifies the size of the memory area reserved for legacy ISA adapter cards. The settings are DISABLED, 16K, 32K, or 64K. The optimal and fail-safe default settings are *DISABLED.*

Reserved Memory Address

This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards.

The settings are C0000, C4000, C8000, CC000, D0000, D4000, D8000, or DC000. The optimal and fail-safe default settings are *C4000.*

Onboard SCSI

This setting enables or disables the onboard SCSI controller for those models that have the SCSI controller integrated on the board. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED.*

Onboard VGA

This setting enables or disables the onboard VGA controller for those models that have the VGA controller integrated on the board. The settings are ENABLED or DISABLED. The optimal and fail-safe default settings are *ENABLED.*

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Chapter 6: Peripheral Setup

Choose the Peripheral Setup entry from the AMIBIOS HIFLEX Setup screen to display the Peripheral Setup options, described below.

Onboard FDC

This option specifies whether the onboard floppy disk controller is enabled. The settings are AUTO, ENABLED, and DISABLED. The optimal and fail-safe default settings are *AUTO*.

Onboard Serial Port 1

Onboard Serial Port 2

These options specify the base I/O port address for the serial ports. The settings are 3E8h, 3F8h, 2E8H, 2F8H, AUTO, or DISABLED. The optimal and fail-safe default settings are *AUTO*.

Onboard Parallel Port

This option specifies the base I/O port address for the parallel port. The settings are 378H, 278H, 3BCH, AUTO, or DISABLED. The optimal and fail-safe settings are *AUTO*.

Parallel Port Mode

This setting sets up the mode of the parallel port. The settings are NORMAL, EPP, or ECP. The optimal and fail-safe default settings are *ECP*.

EPP Version

This setting sets the EPP standards when the Parallel Port Mode is set to EPP. The settings are 1.7 or 1.9. The optimal and fail-safe default settings are *N/A*.

Parallel Port IRQ

This setting allows selection of the IRQ to assist to the parallel port when applicable. The settings are 5 or 7. The optimal and fail-safe default settings are *AUTO*.

Parallel Port DMA Channel

This setting allows selection of the DMA channel to assist to the parallel port when applicable. The settings are 0, 1, 3, or 5. The optimal and fail-safe default settings are *AUTO*.

Onboard IDE

This option specifies the channel used by the IDE controller on the motherboard. The settings are DISABLED, PRIMARY, SECONDARY, or BOTH. The optimal and fail-safe default settings are *BOTH*.

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Declaration of Conformity

(according to ISO/IEC Guide 22 and EN 45014)

6260 Sequence Drive
San Diego, CA 92121-4371
(800) 523-2320

declares that the product:

SB586T100	SB586T133	SB586T166	SB586T166X	SB586T200
SB586T200X	SB586T233X	SB586T266K	SB586T300K	SB586TT100
SB586TT133	SB586TT166X	SB586TT200X	SB586TT233X	SB586TT266K
SB586TT300K	SB586TS100	SB586TS133	SB586TS166	SB586TS166X
SB586TS200	SB586TS200X	SB586TS233X	SB586TS266K	SB586TS300K
SB586T2V100	SB586T2V133	SB586T2V166	SB586T2V166X	SB586T2V200X
SB586T2V233X	SB586T2V266K	SB586T2V300K	SB586TS2V100	SB586TS2V133
SB586TS2V166	SB586TS2V166X	SB586TS2V200X	SB586TX2V233X	SB586TS2V266K
SB586TS2V300K	SB586TU100	SB586TU133	SB586TU166	SB586TU166X
SB586TU200X	SB586TU233X	SB586TU266K	SB586TU300K	

to which this declaration relates, meets the essential health and safety requirements and is in conformity with the relevant EU Directives listed below:

EU EMC Directive 89/336/EEC
EU Low Voltage Directive 73/23/EEC

using the relevant section of the following EU standards and other normative documents:

N 50081-1:1992 Emissions, Generic Requirements.
-EN 55022 Measurement of radio interference characteristics of information technology equipment.

EN 50082-1:1992 Immunity, Generic Requirements.
-IEC 1000-4-2:1995 Immunity for radiated electromagnetic fields.
(Supersedes IEC 801-2)
-IEC 1000-4-3:1995 Immunity for radiated RF electromagnetic fields.
(Supersedes IEC 801-3)
-IEC 1000-4-4:1995 Immunity for AC and I/O lines, fast transients common mode.
(Supersedes IEC 801-4)

EN 60950:1992 Safety of Information Technology Equipment.

Mr. Jim Jameson
President & Chief Executive Officer

July 30, 1999
San Diego, CA

Information supporting this declaration is contained in the applicable Technical Construction file available from:

ICS Advent Europe
Ben Turner Industrial Road
Oving Road
Chichester, West Sussex
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