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PB-DOUT2

INDUSTRIAL DIGITAL OUTPUT

PIGGYBACK FOR THE VMOD-2

ID: 03086 Index: 0300

USER'S MANUAL

PRODUCT HISTORY:

INDEX:	COMMENT:	DATE:
1	FIRST ISSUE	OCTOBER 1991
2	NEW STRUCTURE	APRIL 1995
3	ERRATA 30.08.95	AUGUST 1997
0300	TITLEPAGE UPDATED	SEPTEMBER 1997

Unpacking and Special Handling Instructions

This PEP product is carefully designed for a long and fault-free life; nonetheless, its life expectancy can be drastically reduced by improper treatment during unpacking and installation.

Observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. These can cause shorts and damage to the batteries or tracks on the board.

When installing piggybacks, switch off the power mains.

Furthermore, do not exceed the specified operational temperature ranges of the board version ordered. If batteries are present, their temperature restrictions must be taken into account.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, re-pack it as it was originally packed.

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1. INTRODUCTION

1.1 Product Overview

In automotive and industrial applications, drivers with common Vcc are extensively used to switch power to ground referred loads. The major advantage of these types of drivers is that if a load is inadvertently shorted to ground, it is protected from being activated. Common Vcc drivers have the ability to sense a short and consequently open the power switch and disable the load.

1.2 Ordering Information

Name	Description	Order Number	
PB-DOUT2	Industrial piggyback, 16 digital optoisolated outputs, 1A/24V, short circuit and overload protection, diagnostics	5230-29 3082	*Old* *New*

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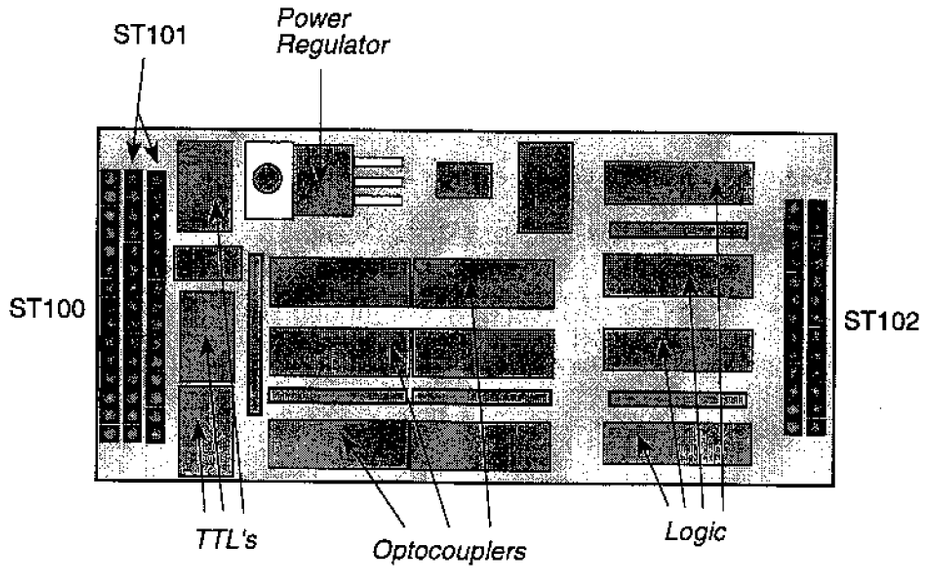
1.3 Specifications

ID code	$ED
Digital output	16 channels, optoisolated, common Vcc
Maximum operating voltage	28 volts
Over voltage shutdown	35 volts
Maximum voltage peak	80 volt transient
Maximum voltage DC	35V DC
Maximum current per channel	1A
Maximum transient current per channel	3.75A
Maximum transient current for all channels	6A
t_{on} rise time	15µs
t_{off} fall time	2µs
R_{ON}	1.3Ω
Error flags	1 x error (common) / 4 channels 1 x thermal error / 4 channels, with
Protective features	overload; overvoltage; short circuit; high temperature; inductive load
Isolation voltage	500V
Power consumption	5V/200mA
Temperature range	-40°C to +85°C
Piggyback size	Width: 48mm Length: 100mm Depth: 12mm
VMOD-2 interface	Two sets of twin row header pins providing all necessary communication paths and a mechanical mounting method

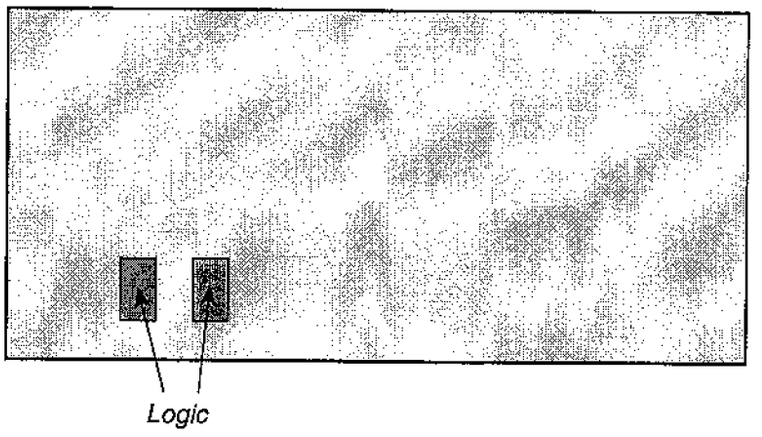
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1.4 Board Overview

Component Side



Solder Side



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1.5 Features

- 16 optoisolated channels, common Vcc.
- Driver device which provides each power switch with individual ON/OFF control.
- Maximum operating voltage of 28V, transients up to 80V.
- Extensive protection - overload, over voltage, high temperature, inductive load.
- Easy maintenance (quick to replace) in the unlikely event of failure/damage.
- Full electronic and mechanical compatibility with the VMOD-2 board.
- Full electrical and mechanical compatibility with the extensive range of VMOD-2 piggybacks.
- All necessary VMEbus lines are available on the piggyback.
- Galvanically optoisolated VME to external, and external to external interfaces.

1.6 Advantages

- High current output, 1A continuous per channel.
- Short load protection.
- Over voltage protection.
- Diagnostic.

1.7 Typical Applications

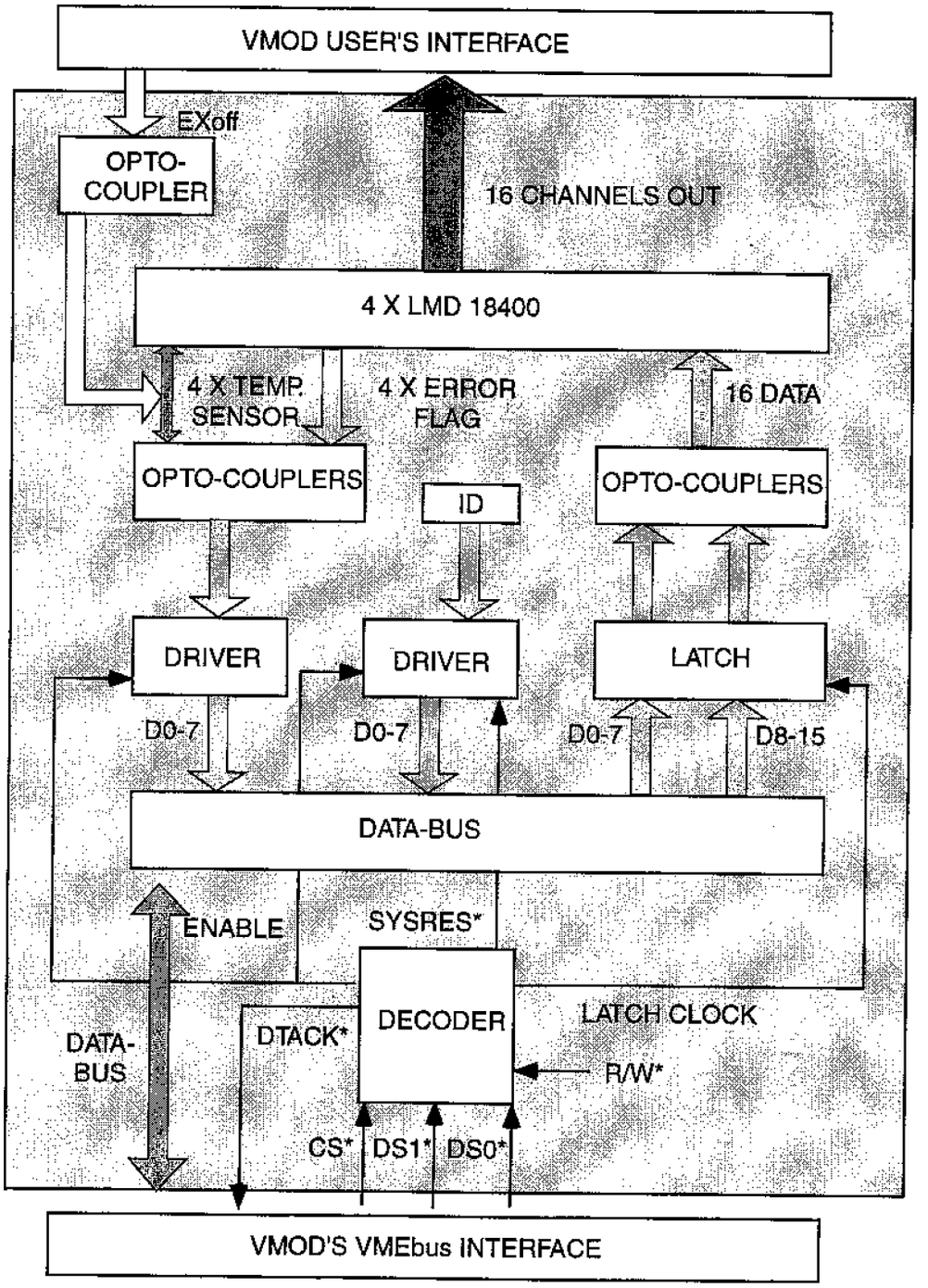
The PB-DOUT2 is typically used where loads have to be protected from being energized.

1.8 Related Publications

VMEbus Specifications Revision C1
LMD 18400 Data Sheet - reprinted at the end of this manual with kind permission of National Semiconductor
VMOD-2 Users Manual from PEP

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1.9 Block Diagram



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2. CONFIGURATION

There are no jumpers to configure on the PB-DOUT2 board itself.

2.1 VMOD-2/IMOD Jumper Configuration

In order for the PB-DOUT2 to be put into use on either the VMOD-2 or IMOD boards, the IRQ and Base Address jumper settings on these boards must be correctly configured.

For more details on these jumper configurations, please refer to the VMOD-2 or IMOD user manuals.

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3. PROGRAMMING

The base address of the PB-DOUT2 in the upper piggyback position (location A) is the same as that set for the VMOD-2/IMOD used (default: $87FE2400/$F70000), whereas the base address in the lower piggyback position (location B) is +$80 of that set for the VMOD-2/IMOD (default: $87FE2480/$F70080).

3.1 PB-DOUT2 Address Map

Address	Byte/Word	Access	Function
BASE+$00	Word	Write	Output Register
BASE+$00	Byte	Read	Status Register
BASE+$40	Byte	Read	ID Byte

3.1.1 Output Register ($00)

The output port of the PB-DOUT2 consists of sixteen unidirectional lines. Access to each line is made by writing a word to the output register. The input function is a read back of the status register. The output function sets the relevant bits. A logical "1" (high) switches the relevant output on.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE+$00	OUT15	OUT14	OUT13	OUT12	OUT11	OUT10	OUT9	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0

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3.1.2 Status Register ($00)

This register contains the error status of the output port. If the status is read as $FF no error has occurred. A logical "0" is returned for the corresponding error bit.

	7	6	5	4	3	2	1	0
BASE+$00	*TS4*	*E4*	*TS3*	*E3*	*TS2*	*E2*	*TS1*	*E1*

Error Description

Name	Description
Ex	Error on output device
TSx	Thermal error on output device
E1	Outputs 00 to 03
E2	Outputs 04 to 07
E3	Outputs 08 to 11
E4	Outputs 12 to 15
TS1	Thermal error outputs 00 to 03
TS2	Thermal error outputs 04 to 07
TS3	Thermal error outputs 08 to 11
TS4	Thermal error outputs 12 to 15

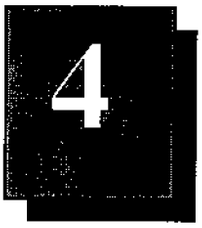
If required an emergency off switch can be configured by applying a typical voltage of 24V to EXoff+ (pin 5) and EXoff- (pin 6), which switches off all outputs (00 to 15) simultaneously.

3.1.3 ID Register ($40)

This register contains the ID byte, allowing automatic recognition of the piggyback fitted to the VMOD-2 or IMOD. This feature is particulary useful in a system with several piggybacks fitted. The ID byte is read using a byte read access.

PD-DOUT2 ID byte = $ED

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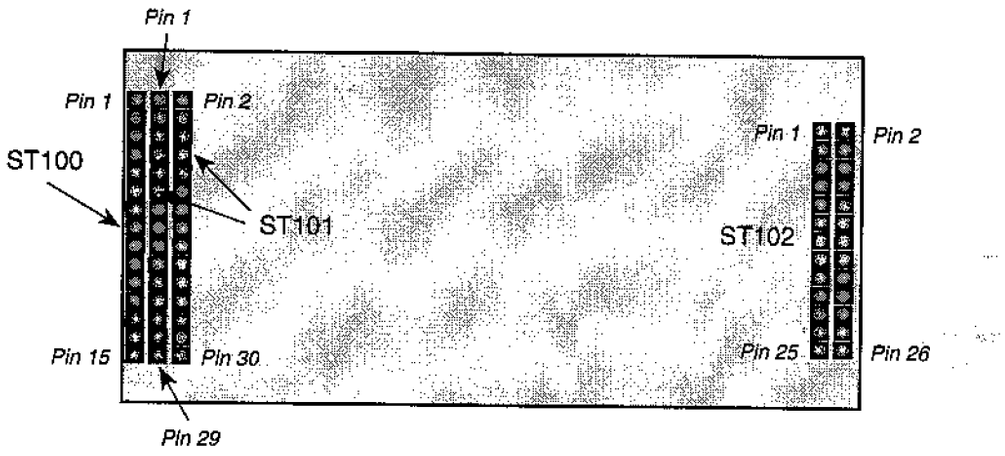


4. PINOUTS

The PB-DOUT2 has three sets of connectors. ST100 is the rearmost row of 15 pins directly next to ST101 with 30 pins. At the front end of the piggyback there is ST102 with 26 pins.

4.1 Main Board

Figure 4.1.0.1: Board Connector Overview



4.1.1 ST100 Connector

The ST100 connector is fitted into the socket row BU0A or BU0B on the IMOD and VMOD-2, depending if there is one or two piggybacks to be fitted.

Pin #	Signal
1	GND
2	Vcc
3	N/C
4	N/C
5	N/C
6	DS1*
7	ID15
8	ID14
9	ID13
10	ID12
11	ID11
12	ID10
13	ID09
14	ID08
15	GND

* *Active Signal Low*

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4.1.2 ST101 Connector

The ST101 connector is fitted into the socket row BU1A or BU1B on the IMOD and VMOD-2 (depending if there is one or two piggybacks to be fitted) to the VMEbus interface logic. Not all of the pins shown are used by the PB-DOUT2.

Pin#	Signal	Pin#	Signal
1	N/C	2	N/C
3	N/C	4	N/C
5	R/W*	6	N/C
7	RESET*	8	DTACK*
9	N/C	10	CS*
11	N/C	12	N/C
13	ID7	14	DS0*
15	ID6	16	N/C
17	ID5	18	A6
19	ID4	20	N/C
21	ID3	22	N/C
23	ID2	24	N/C
25	ID1	26	N/C
27	ID0	28	N/C
29	GND	30	Vcc

** Active Signal Low*

4.1.3 ST102 Connector

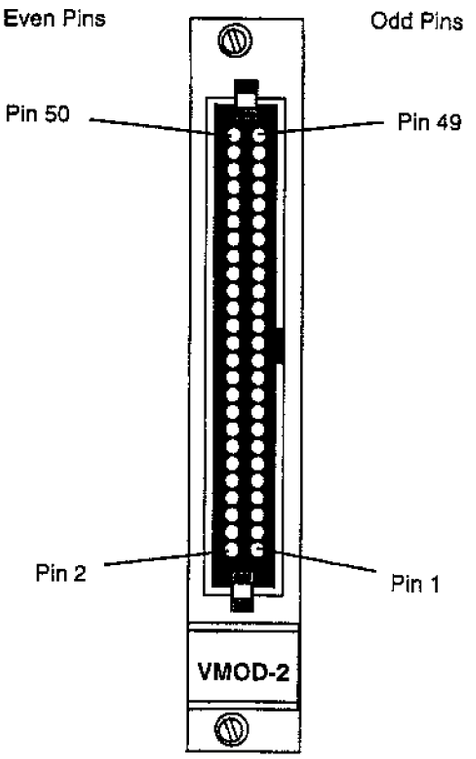
The ST102 connector is fitted into the socket row BU2A or BU2B on the IMOD and VMOD-2 (depending if there is one or two piggybacks to be fitted), directly to half of the 50-way VMOD-2 front panel connector, and ultimately to the user's external interfaces.

Pin#	Signal	Pin#	Signal
1	Vext	2	Vext
3	Vext	4	Vext
5	EXoff+	6	EXoff-
7	OUT0	8	OUT1
9	OUT2	10	OUT3
11	OUT4	12	OUT5
13	OUT6	14	OUT7
15	OUT8	16	OUT9
17	OUT10	18	OUT11
19	OUT12	20	OUT13
21	OUT14	22	OUT15
23	GNDext	24	GNDext
25	GNDext	26	GNDext

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4.2 VMOD-2/IMOD Front Panel

Figure 4.2.0.1: VMOD-2/IMOD Front Panel



Piggyback A

Pin #	Signal	Pin #	Signal
50	Vext	49	GNDext
48	Vext	47	Vext
46	EXoff+	45	EXoff-
44	OUT0	43	OUT1
42	OUT2	41	OUT3
40	OUT4	39	OUT5
38	OUT6	37	OUT7
36	OUT8	35	OUT9
34	OUT10	33	OUT11
32	OUT12	31	OUT13
30	OUT14	29	OUT15
28	GNDext	27	GNDext
26	Reset +Vcc	25	Reset GND

Piggyback B

Pin #	Signal	Pin #	Signal
24	Vext	23	GNDext
22	Vext	21	Vext
20	EXoff+	19	EXoff-
18	OUT0	17	OUT1
16	OUT2	15	OUT3
14	OUT4	13	OUT5
12	OUT6	11	OUT7
10	OUT8	9	OUT9
8	OUT10	7	OUT11
6	OUT12	5	OUT13
4	OUT14	3	OUT15
2	GNDext	1	GNDext

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The relevant half of the VMOD-2 and IMOD front panel 50-way connector (pins 1..24 for lower position and pins 27..50 for upper) assumes the relationship of PB-DOUT2 signals and its ST102.

An optional 50-way header behind the front panel connector has an identical pin-out to the front panel connector. It is provided for applications where the flat band cable is to be routed internally, or where an alternative front panel is to be fitted and used. In some cases, cables can be routed through the systems interior i.e. to the back panel (from this optional connector) and some from the external connector on the front panel. In doing so take care not to exceed the fan out ability of the piggyback's driver circuits.

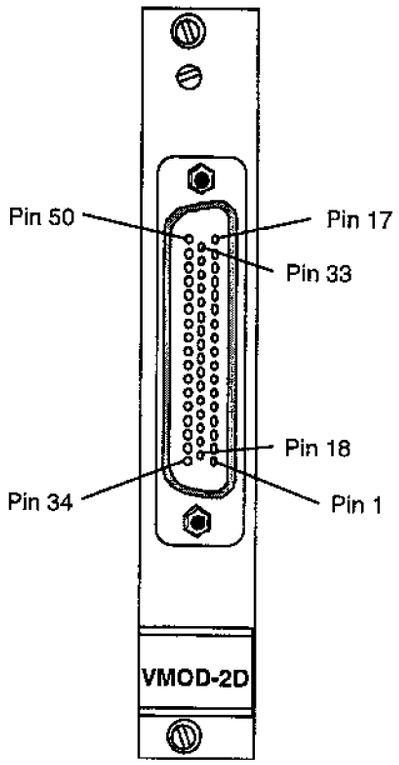
Note

With systems that have more than one of this type of connector , or which use several VMOD-2 or IMODs with various piggybacks, it is advisable to put a drop of paint on the back of the mating connector and on the front panel of the VMOD-2 or IMOD, for correct connection. The connector splits virtually in half (pins 1-24 and 27-50) for connection to the rear piggyback location.

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4.3 VMOD-2D Front Panel

Figure 4.3.0.1: VMOD-2D Front Panel



Piggyback A

Pin #	Signal	Pin #	Signal	Pin #	Signal
50	Vext	33	Vext	17	GNDext
49	Vext	32	EXoff-	16	EXoff+
48	OUT0	31	OUT2	15	OUT1
47	OUT3	30	OUT5	14	OUT4
46	OUT6	29	OUT8	13	OUT7
45	OUT9	28	OUT11	12	OUT10
44	OUT12	27	OUT14	11	OUT13
43	OUT15	26	GNDext	10	GNDext
42	Reset +Vcc			9	Reset GND

Piggyback B

Pin #	Signal	Pin #	Signal	Pin #	Signal
		25	Vext		
41	GNDext	24	Vext	8	Vext
40	EXoff+	23	OUT0	7	EXoff-
39	OUT1	22	OUT3	6	OUT2
38	OUT4	21	OUT6	5	OUT5
37	OUT7	20	OUT9	4	OUT8
36	OUT10	19	OUT12	3	OUT11
35	OUT13	18	OUT15	2	OUT14
34	GNDext			1	GNDext

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4.4 VMOD-2 / VMOD-2D Pinout Relationship

Piggyback A

Signal	VMOD-2 Pin #	VMOD-2D Pin #	Signal	VMOD-2 Pin #	VMOD-2D Pin #
Vext	50	50	GNDext	49	17
Vext	48	33	Vext	47	49
EXoff+	46	16	EXoff-	45	32
OUT0	44	48	OUT1	43	15
OUT2	42	31	OUT3	41	47
OUT4	40	14	OUT5	39	30
OUT6	38	46	OUT7	37	13
OUT8	36	29	OUT9	35	45
OUT10	34	12	OUT11	33	28
OUT12	32	44	OUT13	31	11
OUT14	30	27	OUT15	29	43
GNDext	28	10	GNDext	27	26

Signal	VMOD-2 Pin #	VMOD-2D Pin #	Signal	VMOD-2 Pin #	VMOD-2D Pin #
Reset +Vcc	26	42	Reset GND	25	9

Piggyback B

Signal	VMOD-2 Pin #	VMOD-2D Pin #	Signal	VMOD-2 Pin #	VMOD-2D Pin #
Vext	24	25	GNDext	23	41
Vext	22	8	Vext	21	24
EXoff+	20	40	EXoff-	19	7
OUT0	18	23	OUT1	17	39
OUT2	16	6	OUT3	15	22
OUT4	14	38	OUT5	13	5
OUT6	12	21	OUT7	11	37
OUT8	10	4	OUT9	9	20
OUT10	8	36	OUT11	7	3
OUT12	6	19	OUT13	5	35
OUT14	4	2	OUT15	3	18
GNDext	2	34	GNDext	1	1

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5. INSTALLATION

5.1 VMEbus Connection

Caution!

Before installing or removing any VMEbus boards, always turn off the power to the bus and any external peripherals.

Inserting or removing modules, while the power is on, could result in damage to the VME module or peripherals interface.

Please refer to VMOD-2/IMOD user's manual for details on installing or removing.

Note

The VMEbus backplane uses automatic daisy-chaining (no BG/IACK jumpers), therefore does not need to be configured by the user.

For users with VBP backplanes, please refer to the *VBP Users Manual* for configuration information.

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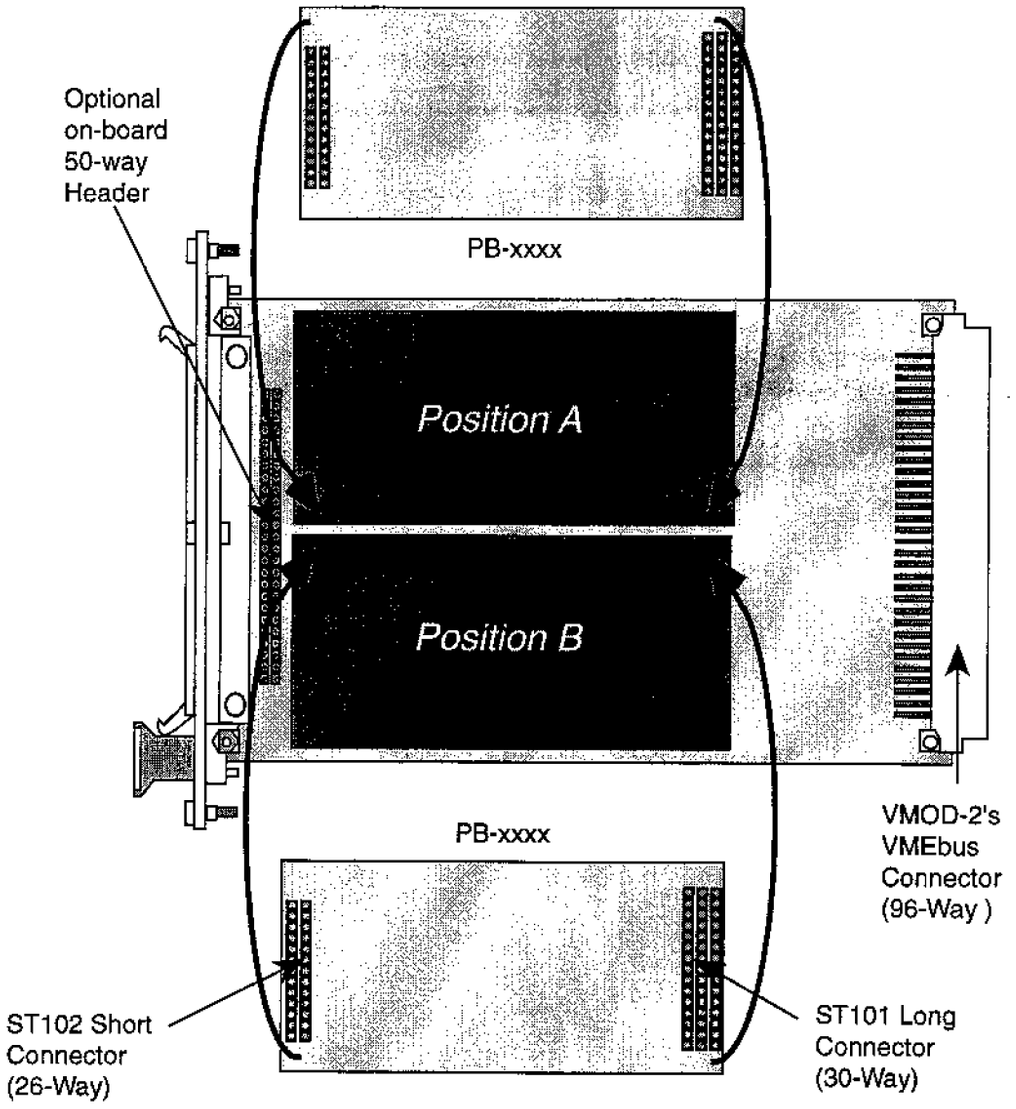
5.2 Installing the PB-DOUT2

The PB-DOUT2 may be plugged into any free piggyback position (A or B) on the VMOD-2 or IMOD. Please ensure the correct location before fitting.

Note

1. One connector on the PB-DOUT2 has fewer pins than the other.
2. ST101 has two-rows which are to fit the front two-rows of the VMOD-2 amd IMOD three-row interface socket. Take care to ensure that the piggyback is in its correct position.

Figure 5.2.0.1: PB-DOUT2 Installation Overview



Mechanical fastening and support is provided by the two interface connectors. In addition, the piggyback can be attached to the motherboard by screws and stand-off pillars at the front end of the piggyback, and at the corresponding location on the VMOD-2 and IMOD at the two holes provided for this purpose.

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5.3 Troubleshooting

This section is intended to assist users of the PB-DOUT2 piggybacks to quickly resolve any problems they may encounter in their application.

Problem	Possible Cause or Solution
None of the externally connected devices have communications with the PB-DOUT2's outputs	1) The external interface connector has been connected to the wrong half of the front panel connector (i.e. pins 1 to 24 instead of pins 27 to 50 for upper piggyback position). Move the piggyback to another location and test from there before rewiring the interface cable. See Chapter 5 for precise pinouts. 2) The piggyback has been accidently set back one whole pin-row so that only half of its output connectors are connected to the external interface, and its inputs are wrongly connected to the VMOD-2's logic interface or power. *Check the physical board configuration.* 3) The piggyback has been displaced on the ST1 and ST2 connectors by 180 degrees. *Check the physical board configuration.* If such a connection as 2) or 3) have been made then the piggyback has been designed in such a way that no damage to it or the VMOD-2 should occur. If, however, the piggyback or VMOD-2 has become damaged through misconnections of this kind, the PEP warrenty is invalidated. 4) An optoisolated version of the board has been fitted anf the external supply is not provided or the external power supply unit has been turned off, has exceeded the current limit, or has had a fuse failure. *Check the power supply unit.*
An unknown problem prevents the VMOD-2/PB-DOUT2 configuration from functioning.	If the VMOD-2 functioned previously and has been reconfigured for a PB-SIO4A, the following can determine the fault. 1) Test the PB-DOUT2 at another location or on another VMOD-2. 2) If the piggyback functions after trying 1), check for damaged or burnt tracks. 3) If the piggyback does not function after 1), the fault probably lies with the piggyback or application software. 4) Check that the serial channels are correctly terminated at the external end, and have a ground reference.

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5.4 General Notes for Using the System

Having designed a system, it is necessary to keep it in good working order. The three biggest risks to the system occur when:

- Connecting peripherals, disk-drives, printers, terminals and external power sources;
- Adding or changing modules, address settings and locations, etc;
- Becoming complacent and not referring to the manuals when altering or adding modules.

These risks can be reduced by:

- Checking the electrical compatibility of all devices to be connected;
- Ensuring that they are powered from the same mains supply branch (phase) and grounded to the same reference point;
- Shutting down all power before making or breaking any connections to modules or attachments to the system, including power to the peripherals;
- Observing sensible static protection procedures before handling any modules, piggybacks or memory IC's;
- Keeping all manuals available by the system and refer to them when required.

Some tips are:-

PEPCards are not over sensitive to static, but it is generally advisable to observe normal antistatic procedures.

When configuring the module, it should not be taken out of the original packing unless necessary. The clear packs can be opened and the jumpers set, piggybacks added, etc. without removing the card. This prevents inadvertent shorting of any on-board devices.

When inserting modules into a system, the power should be turned off and the mains lead not removed! The ground wire prevents the rack floating with dangerous static voltages, which could destroy circuits on the module being inserted.

The front panel of the module and the shell of the connector should be touched to any part of the rack before fitting. This discharges any static from the user.

Modules should not be pulled straight out of a rack and the back of the front panel checked to see if there are cables to unplug (such as the VSBC-1's 40-pin parallel on-board headers). Any leads should be disconnected from a module before unscrewing the front panel and removing from the rack. It should be ensured that, when fitted, these cables have enough play to allow the modules to be removed far enough to detach these cables. Modules should be put into the rack before connecting any front-panel connectors.

The "pulled" jumpers should be parked on to one of the pins they would normally bridge, so they can be quickly replaced.

It should be remembered to check the mains input voltage selector switch before installing or using any PSU!

A record should be kept of settings and a copy forwarded with any board returned to PEP for failure analysis.

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System Configuration Record

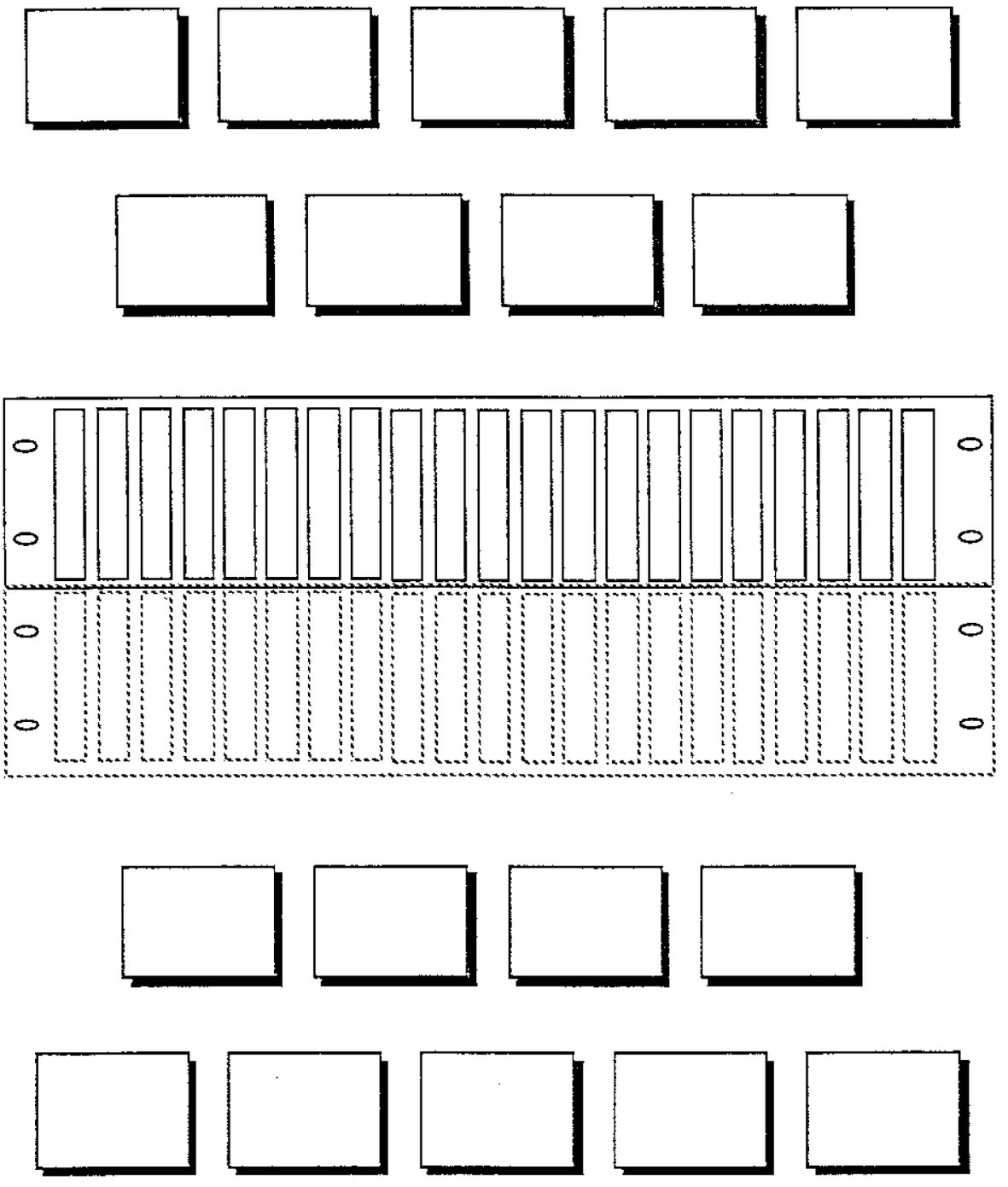
Use this form to keep an up to date record of your systems configuration

RACK #	MODULE (OR TYPE)	BASE ADDRESS	IRQ LEVEL & VECTOR	BACKPLANE JUMPERING BG0* BG1* BG2* BG3* IACK*
POWER SUPPLY	MAKE	POWER OUTPUT	VOLTAGE INPUT	
VMEbus BACKPLANE	MAKE	SIZE	TERMINATION	
SLOT 1				
SLOT 2				
SLOT 3				
SLOT 4				
SLOT 5				
SLOT 6				
SLOT 7				
SLOT 8				
SLOT 9				
SLOT 10				
SLOT 11				
SLOT 12				
SLOT 13				
SLOT 14				
SLOT 15				
SLOT 16				
SLOT 17				
SLOT 18				
SLOT 19				
SLOT 20				
SLOT 21				
IOC BACKPLANE	MAKE	SIZE		
FDD #0	MAKE	SIZE	FLOPPIES USED	
FDD #1	MAKE	SIZE	FLOPPIES USED	
HDD #0	MAKE	SIZE		
HDD #1	MAKE	SIZE		
SOFTWARE USED	TYPE	REVISION		

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System Configuration Record

Use this side to keep an up to date record of your systems externaly connected peripherals



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Lit #108384

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July 1990

LMD18400
Quad High Side Driver

General Description

The LMD18400 is a fully protected quad high side driver. It contains four common-drain DMOS N-channel power switches, each capable of switching a continuous 1 Amp load (>3 Amps transient) to a common positive power supply. The switches are fully protected from excessive voltage, current and temperature. An instantaneous power sensing circuit calculates the product of the voltage across and the current through each DMOS switch and limits the power to a safe level. The device can be disabled to produce a "sleep" condition reducing the supply current to less than 10 μA. Separate ON/OFF control of each switch is provided through standard LSTLL/CMOS logic compatible inputs.

A MICROWIRE™ compatible serial data interface is built in to provide extensive diagnostic information. This information includes switch status readback, output load fault conditions and thermal and overvoltage shutdown status. There are also two direct-output error flags to provide an immediate indication of a general system fault and an indication of excessive operating temperature.

The LMD18400 is packaged in a special power dissipating leadframe that reduces the junction to case thermal resistance to approximately 20°C/W.

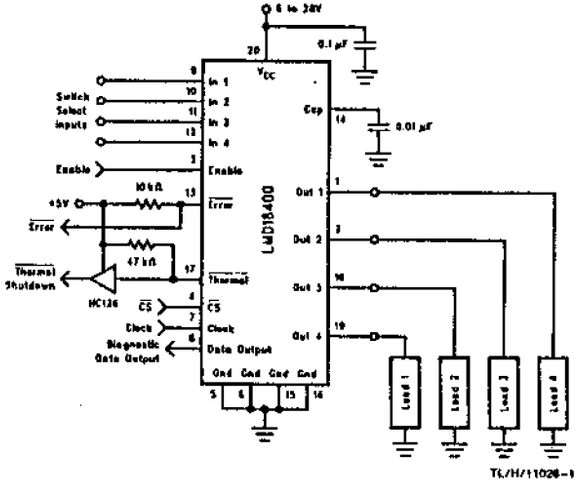
Features

- Four independent outputs with >3A peak, 1A continuous current capability
- 1.3Ω maximum ON resistance over temperature
- True instantaneous power limit for each switch
- High survival voltage (60 V_{DC}, 80V transient)
- Shorted load (to ground and supply) protection
- Overvoltage shutdown at V_{CC} > 35V
- LS TTL/CMOS compatible logic inputs and outputs
- <10 μA supply current in "sleep" mode
- −5V output clamp for discharging inductive loads
- Serial data interface for 11 diagnostic checks:
  - — Switch ON/OFF status
  - — Open or shorted load
  - — Operating temperature
  - — Excessive supply voltage
- Two direct-output error flags

Applications

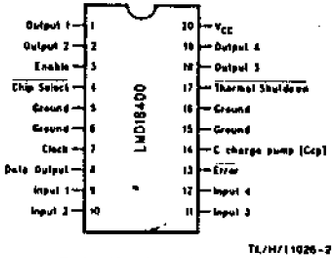
- Relay and solenoid drivers
- High impedance automotive fuel injector drivers
- Lamp drivers
- Power supply switching
- Motor drivers

Typical Application



TL/H/11026–1

Connection Diagram



TL/H/11026–2

Order Number LMD18400N
See NS Package Number N20A

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LMD18400 Quad High Side Driver

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Survival Voltage (Pin 20)	
Transient (t_r = 10 ms)	80V
Continuous	−0.5V to +60V
Output Transient Current (Each Switch)	3.75A
Output Transient Current (Total, All Switches)	6A
Output Steady State Current (Each Switch)	1A
Logic Input Voltage (Pins 3, 9, 10, 11, 12)	−0.3V to +16V
Logic Input Voltage (Pins 4, 7)	−0.3V to +6V
Error Flag Voltage	16V
ESD Susceptibility (Note 2)	2000V
Power Dissipation (Note 3)	5W
	Internally Limited
Junction Temperature ($T_{J_{Max}}$)	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	+260°C

Operating Ratings (Note 1)

Ambient Temperature Range (T_A)	−40°C to +125°C
Supply Voltage Range	6V to 28V

Electrical Characteristics V_{CC} = 12V, C_{CP} = 0.01 µFd, unless otherwise indicated. **Boldface** limits apply over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for $T_A = T_J$ = +25°C.

Parameter	Conditions	Typical (Note 4)	Limit (Note 5)	Units (Limit)
DC CHARACTERISTICS				
Supply Current	Enable Input = 0V	0.04	10	µA (Max)
	Enable Input = 5V, Inputs = 0V	7.5	15	mA (Max)
	Enable Input = 5V, Inputs = 5V Open Loads	7.5	15	mA (Max)
Output Leakage	Enable Input = 5V, Inputs = 0V (Pins 1, 2, 18, 19)	0.01	10	µA (Max)
Rds ON	I_{OUT} = 1A, (Note 6)	0.8	**1.3**	Ω (Max)
Short Circuit Current	V_{CC} = 12V, (Note 6)	1.2	0.6	A (Min)
	V_{CC} = 6V, (Note 6)	2.4		A
	V_{CC} = 28V, (Note 6)	0.6		A
Maximum Output Current	$V_{CC} - V_O$ = 4V, (Note 6)	3.75		A
Load Error Threshold Voltage	Pins 1, 2, 18, 19	4.1		V
Open Load Detection Current	Pins 1, 2, 18, 19	150		µA
Negative Clamp Output Voltage	I_O = 1A, (Note 8)	−5		V
Overvoltage Shutdown Threshold		35	40	V (Max)
Overvoltage Shutdown Hysteresis		0.75		V
Error Output Leakage Current	$V_{Pin\ 13}$ = 12V	0.001	10	µA (Max)
Thermal Warning Temperature	$V_{Pin\ 13}$ < 0.8V	145		°C
Thermal Shutdown Temperature	$V_{Pin\ 17}$ < 0.8V	170		°C

Electrical Characteristics V_{CC} = 12V, C_{CP} = 0.01 µF, unless otherwise indicated. **Boldface** limits apply over the entire operating temperature range, −40°C ≤ T_A ≤ +125°C, all other limits are for $T_A = T_J$ = +25°C. (Continued)

Parameter	Conditions	Typical (Note 4)	Limit (Note 5)	Units (Limit)
AC CHARACTERISTICS				
Switch Turn-On Delay ($t_{d(ON)}$)	Enable (Pin 3) = 5V, I_{OUT} = 1A	5	10	µs (Max)
Switch Turn-On Rise Time (t_{ON})	I_{OUT} = 1A	7	15	µs (Max)
Switch Turn-Off Delay (t_{dOFF})	Enable (Pin 3) = 5V, I_{OUT} = 1A	0.5	2	µs (Max)
Switch Turn-Off Fall Time (t_{OFF})	I_{OUT} = 1A	0.15	1	µs (Max)
Enable Time (t_{EN})	Measured with Switch 1, Pin 9 = 5V	30	50	µs (Max)
Error Reporting Delay (t_{Error})	Enable (Pin 3) = 5V, Switch 1 Load Opened	75	150	µs (Max)
Data Setup Time (t_{DS})	C_L = 30 pF	200	500	ns (Min)
TRI-STATE® Control (t_{1H}, t_{OH})	Pin 8, Hi-Z Enable Time	2		µs
Data Clock Frequency		3	1	MHz (Max)
DIGITAL CHARACTERISTICS				
Logic "1" Input Voltage	Pins 3, 4, 7, 9, 10, 11, 12		**2.0**	V (Min)
Logic "0" Input Voltage	Pins 3, 4, 7, 9, 10, 11, 12		**0.8**	V (Max)
Logic "1" Input Current	Pins 4, 7	0.001	**1**	µA (Max)
Logic "0" Input Current	Pins 4, 7	−0.001	**−1**	µA (Max)
TRI-STATE Output Current	Pin 8, Pin 4 = 5V	0.05	10	µA (Max)
	Pin 8 = 0V	−0.05	−10	µA (Max)
Enable Input Current	Pin 3 = 2.4V	12	**25**	µA (Max)
Channel Input Resistance	Pins 9, 10, 11, 12	75	**25**	kΩ (Min)
Error Output Sink Current	Pin 13 = 0.8V	4	**1.6**	mA (Min)
Logic "1" Output Voltage	Pin 8			
	I_{OUT} = −360 µA	4.4	**2.4**	V (Min)
	I_{OUT} = −10 µA	5.1	**4.5**	V (Min)
	I_{OUT} = −10 µA		**5.5**	V (Max)
Logic "0" Output Voltage	Pin 8 I_{OUT} = 100 µA		**0.4**	V (Max)
Thermal Shutdown Output Source Current	Pin 17 = 2.4V	5	3	µA (Min)
Thermal Shutdown Output Sink Current	Pin 17 = 0.8V	360	250	µA (Min)

Electrical Characteristics Notes

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model, 100 pF discharge through a 1.5 kΩ resistor. All pins except pins 3 and 8 which are protected to 1000V and pins 1, 2, 18 and 19 which are protected to 500V.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A and is limited by thermal shutdown. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the device will eventually go into thermal shutdown. For the LMD18400 the junction-to-ambient thermal resistance, θ_{JA}, is 50°C/W. With sufficient heatsinking the maximum continuous power dissipation for the package will be, $I_{OC(Max)}^2 \times R_{ON(Max)} \times 4$ switches $(1A^2 \times 1.3\Omega) \times 4 = 5.2W$).

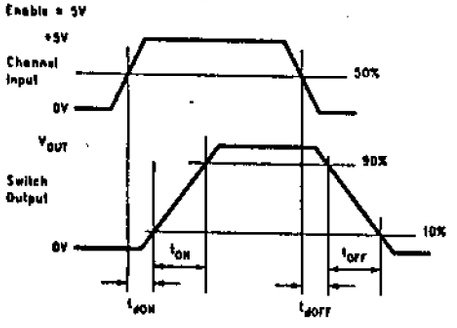
Note 4: Typical values are at $T_J = +25°C$ and represent the most likely parametric norm.

Note 5: All limits are 100% production tested at +25°C. Limits at temperature extremes are guaranteed through correlation and accepted Statistical Quality Control (SQC) methods.

Note 6: Pulse Testing techniques used. Pulse width is < 5 ms with a duty cycle < 1 %.

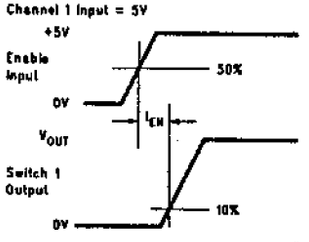
Timing Specification Definitions

Switching Turn ON/OFF



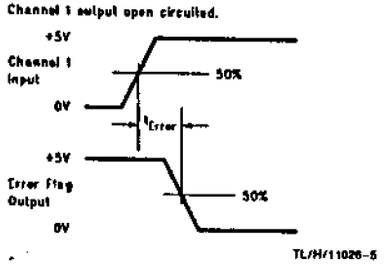
TL/H/11026-3

Enable Turn-ON



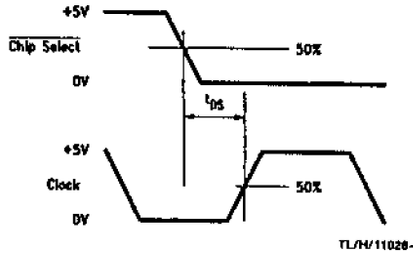
TL/H/11026-4

Error Reporting Delay



TL/H/11026-5

Data Setup Time

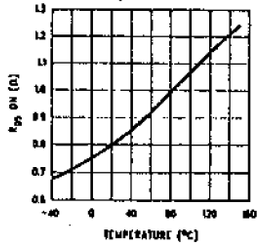


TL/H/11026-6

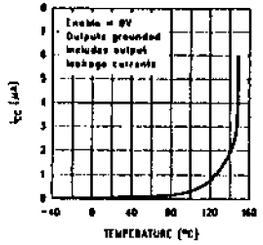
Typical Performance Characteristics

For all curves, V_{CC} = 12V, Temperature is the junction temperature unless otherwise noted.

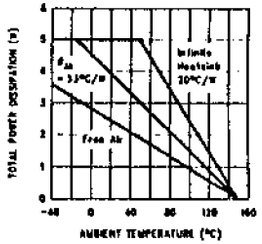
Switch ON Resistance vs Temperature



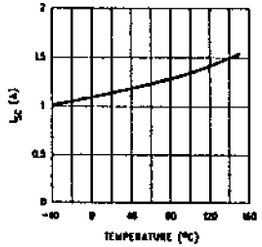
"Sleep" Mode Supply Current vs Temperature



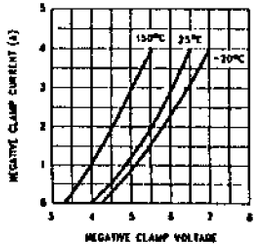
Maximum Power Dissipation vs Ambient Temperature



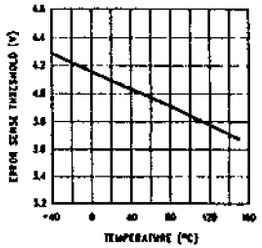
Short Circuit Current vs Temperature



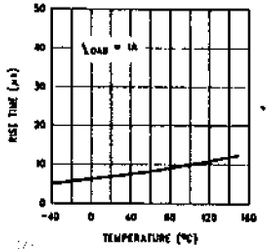
Clamp Characteristics vs Temperature



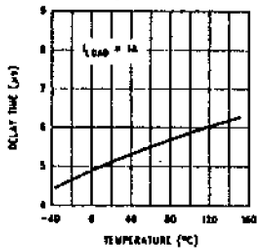
Error Sense Threshold Voltage vs Temperature



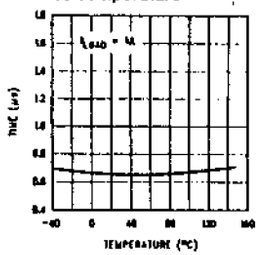
Turn ON Rise Time vs Temperature



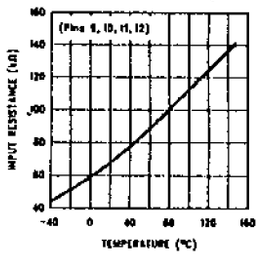
Turn ON Delay Time vs Temperature



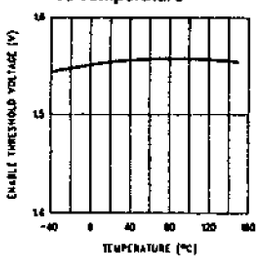
Turn OFF Time vs Temperature



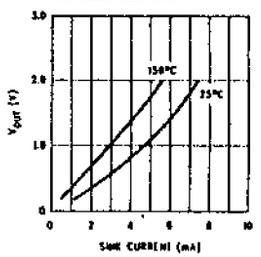
Switch Select Logic Input Resistance vs Temperature



Enable Threshold Voltage vs Temperature

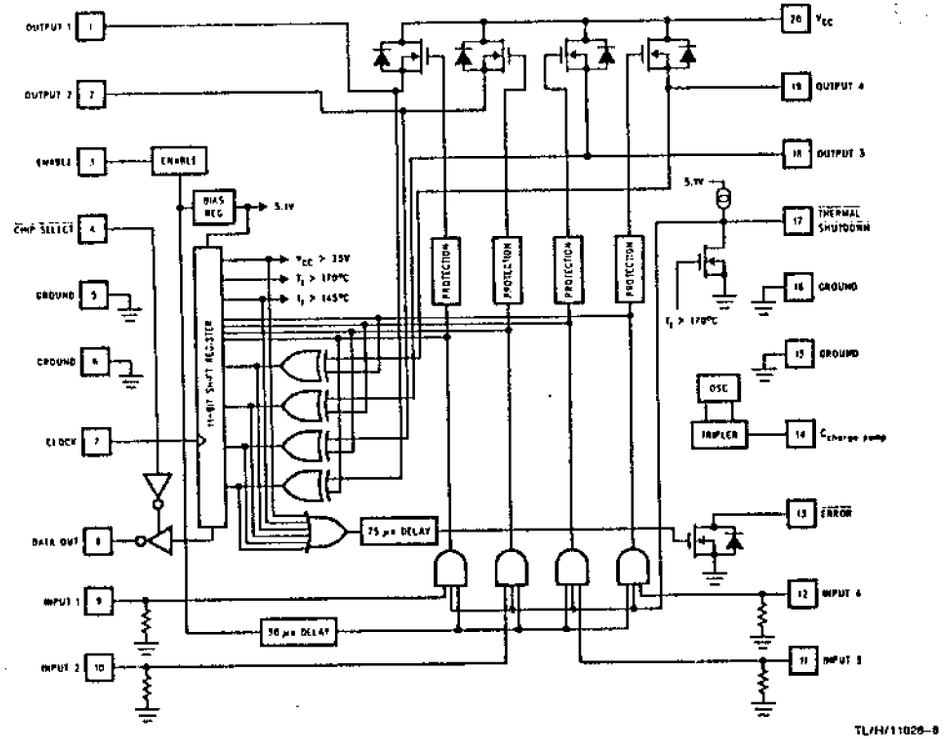


Error Output Voltage vs Sink Current



TL/H/11026-7

Functional Block Diagram



TL/H/11026–8

Truth Table

Enable Input (Pin 3)	Chip Select Input (Pin 4)	Switch Control Input (Pins 8, 9, 10, 11)	Error Output (Pin 13)	Thermal SD Output (Pin 17)	Conditions
0	X	X	0	0	"Sleep" Mode, $I_{Supply} < 10\ \mu A$
1	X	0	1	1	Selected Switch is OFF
1	X	1	1	1	Selected Switch is ON, Normal Operation
1	X	0	0	1	Switch is OFF but: a. Load is Open Circuited, or b. Load is Shorted to V_{CC}, or c. $T_J > +145°C$, or d. $V_{CC} > +35V$
1	X	1	0	1	Switch is ON, but; a. Load is Shorted to Ground, or b. Switch is in Power Limit, or c. $T_J > +145°C$, or d. $V_{CC} > +35V$ and Switch is Actually OFF
1	X	1	0	0	$T_J > +170°C$, All Switches are OFF
1	1	X	X	X	Data Output Pin is TRI-STATE
1	0	X	X	X	Data Output Pin is Enabled and Ready to Output Diagnostic Information

Applications Information

BASIC OPERATION

High-side drivers are used extensively in automotive and industrial applications to switch power to ground referred loads. The major advantage of using high-side drive, as opposed to low-side drive, is to protect the load from being energized in the event that the load drive wire is inadvertently shorted to ground as shown in *Figure 1*. A high-side driver can sense a shorted condition and open the power switch to disable the load and eliminate the excessive current drain on the power supply. The LMD18400 can control and protect up to four separate ground referenced loads.

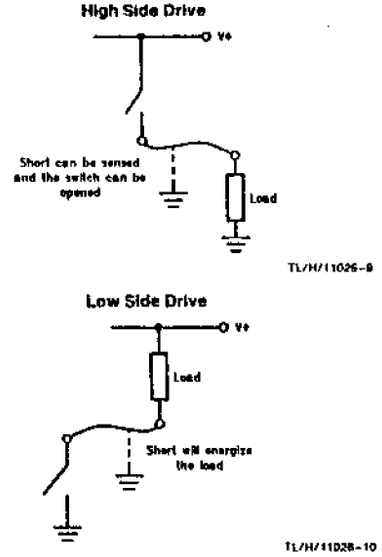
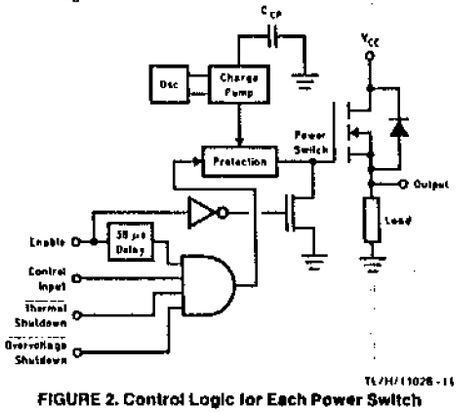


FIGURE 1. High-Side vs Low-Side Drive

The LMD18400 combines low voltage CMOS logic control circuitry with a high voltage DMOS process. Each DMOS power switch has an individual ON/OFF control input. When commanded ON, the output of the switch will connect the load to the V_{CC} supply through a maximum resistance of 1.3Ω (the ON resistance of the DMOS switch). The voltage applied to the load will depend upon the load current and the designed current capability of the LMD18400. When a switch is commanded OFF, the load will be disconnected from the supply except for a small leakage current of typically less than 0.01 μA.

The LMD18400 can be continually connected to a live power source, a car battery for example, while drawing less than 10 μA from the power source when put into a "sleep" condition. This "sleep" mode is enacted by taking the Enable input (pin 3) low. During this mode the supply current for the device is typically only 0.04 μA. Special low current consumption standby circuitry is used to hold the DMOS switches OFF to eliminate the possibility of supply voltage transients from turning on any of the loads (a common problem with MOS power devices). When in the "sleep" mode, all diagnostic and logic circuitry is inactive. When the Enable input is taken to a logic 1, the switches become "armed" and ready to respond to their control input after a short, 30 μs, enable delay time. This delay interval prevents the switches from transient turn-on. *Figure 2* shows the switch control logic.



TL/H/11026–11

FIGURE 2. Control Logic for Each Power Switch

Each DMOS switch is turned ON when its gate is driven approximately 3.5V more positive than its source voltage. Because the source of the switch is the output terminal to the load it can be taken to a voltage very near the V_{CC} supply potential. To ensure that there is sufficient voltage available to drive the gates of the DMOS device a charge pump circuit is built in. This circuit is controlled by an internal 300 kHz oscillator and using an external 10 nF capacitor connected from pin 14 to ground generates a voltage that is approximately 20V greater than the V_{CC} supply voltage. This provides sufficient gate voltage drive for each of the switches which is applied under command of standard 5V logic input levels.

The turn-on time for each switch is approximately 12 μs when driving a 1A load current. This relatively slow switching time is beneficial in minimizing electromagnetic interference (EMI) related problems created from switching high current levels.

Applications Information (Continued)

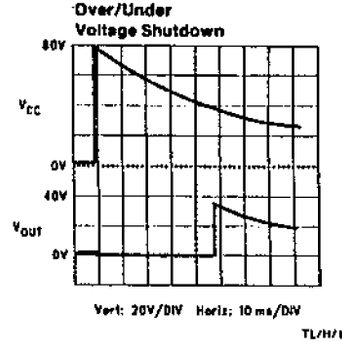
PROTECTION CIRCUITRY

The LMD18400 has extensive protection circuitry built in. With any power device, protection against excessive voltage, current and temperature conditions is essential. To achieve a "fail-safe" system implementation, the loads are deactivated automatically by the LMD18400 in the event of any detected overvoltage or over-temperature fault conditions.

Voltage Protection

The V_{CC} supply can range from −0.5V to +60 V_{DC} without any damage to the LMD18400. The CMOS logic circuitry is biased from an internal 5.1V regulator which protects these lower voltage transistors from the higher V_{CC} potentials. In order to protect the loads connected to the switch outputs however, an overvoltage shutdown circuit is employed. Should the V_{CC} potential exceed 35V all of the switches are turned OFF thereby disconnecting the loads. This 35V threshold has 750 mV of hysteresis to prevent potential oscillations.

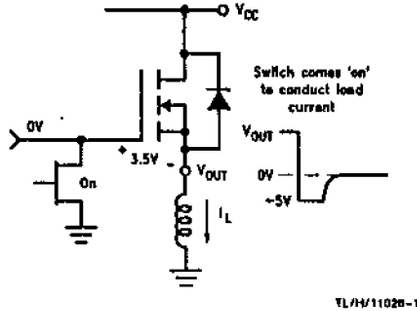
Additionally, there is an undervoltage lockout feature built in. With V_{CC} less than 5V it becomes uncertain whether the logic circuitry can hold the switches in their commanded state. To avoid this uncertainty, all of the switches are turned OFF when V_{CC} drops below approximately 5V. *Figure 3* illustrates the shutoff of an output during a 0V to 80V V_{CC} supply transient.



TL/H/11026–12

FIGURE 3. Overvoltage/Undervoltage Shutdown

The LMD18400 has been designed to drive all types of loads. When driving a ground referenced inductive load such as a relay or solenoid, the voltage across the load will reverse in polarity as the field in the inductor collapses when the power switch is turned OFF. This will pull the output pin of the LMD18400 below ground. This negative transient voltage is clamped at approximately −5V to protect the IC. This clamping action is not done with diodes but rather the power DMOS switch turning back on momentarily to conduct the inductor current as it de-energizes as shown in *Figure 4*.



TL/H/11026–13

FIGURE 4. Turn-OFF Conditions with an Inductive Load

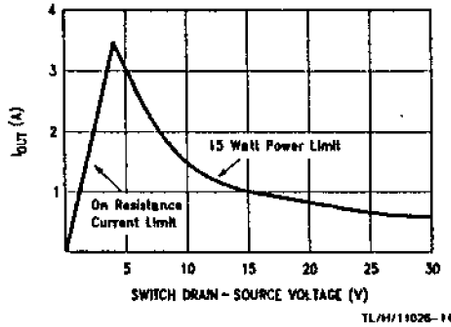
When the output inductance produces a negative voltage, the gate of the DMOS transistor is clamped at 0V. At −3.5V, the source of the power device is less than the gate by enough to cause the switch to turn ON again. During this negative transient condition the power limiting circuitry to protect the switch is disabled due to the gate being held at 0V. The maximum current during this clamping interval, which is equal to the steady state ON current through the inductor, should be kept less than 1A. Another concern during this interval has to do with the size of an inductive load and the amount of time required to de-energize it. With larger inductors it may be possible for the additional power dissipation to cause the die temperature to exceed the thermal shutdown limit. If this occurs all of the other switches will turn OFF momentarily (see section on Thermal Management).

Power Limiting

The LMD18400 utilizes a true instantaneous power limit circuit rather than simple current limiting to protect each switch. This provides a higher transient current capability while still maintaining a safe power dissipation level. The power dissipation in each switch (the product of the Drain-to Source voltage and the output current, $V_{ds} \times I_{OUT}$) is continually monitored and limited to 15W by varying the gate voltage and therefore the ON resistance of the switch. Basically the ON resistance will be as low as possible until 15W is being dissipated. To maintain 15W, the ON resistance increases to reduce the load current. This results in a decrease of the output voltage. For resistive loads, the output voltage when in power limit will be:

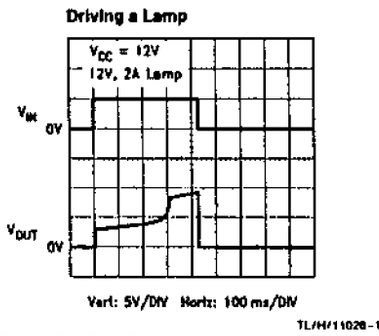
$$V_{OUT}\ (\text{in Power Limit}) = \frac{V_{CC} - \sqrt{V_{CC}^2 - 60\,R_L}}{2}$$

This provides a maximum transient current and drain-to-source voltage characteristic as shown in *Figure 5*.



TL/H/11026–14

FIGURE 5. Maximum Output Current with Instantaneous Power Limiting



TL/H/11026–15

FIGURE 6. Soft Turn-On of a Lamp Load

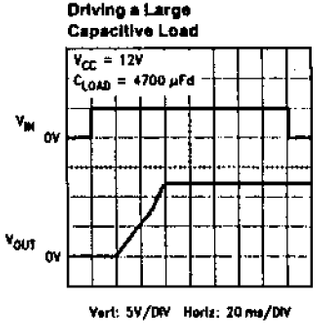
The steady state current to the load is limited by the package power dissipation, ambient temperature and the ON resistance of the switch which has a positive temperature coefficient as shown in the Typical Performance Characteristics.

This dynamic current limiting of the switches is beneficial when driving lamp and large capacitive loads. Lamps require a large inrush current, on the order of 10 times the normal operating current, when first switched on with a cold filament. The LMD18400 will limit this initial current to the level where 15W is dissipated in the switch. As the filament warms up the voltage across the lamp increases thereby decreasing the voltage across the switch which permits more current to fully light the lamp. With limited inrush current the lifetime of a lamp load is increased significantly. *Figure 6* illustrates the soft turn-on of a lamp load.

The same principle of increasing output current as the voltage across the load increases allows large capacitive loads to be charged more quickly by an LMD18400 driver than as opposed to a driver with a fixed 1A current limit protection scheme. *Figure 7* shows the output response while driving a large capacitive load.

Thermal Protection

The die temperature of the LMD18400 is continually monitored. Should any conditions cause the die temperature to rise to +170°C, all of the power switches are turned OFF automatically to reduce the power dissipation. It is important to realize that the thermal shutdown affects all four of the switches together. That is, if just one switch load is enough to heat the die to the thermal shutdown threshold, all of the other switches, regardless of their power dissipation conditions, will be switched OFF. All of the switches will be re-enabled when the die temperature has cooled to approximately +160°C. Until the high temperature forcing conditions have been removed the switches will cycle ON and OFF thus maintaining an average die temperature of +165°C. The LMD18400 will signal that excessive temperatures exist through several diagnostic output signals (see Diagnostics).



TL/H/11026–16

FIGURE 7. Driving a Large Capacitive Load

Applications Information (Continued)

DIAGNOSTICS

The LMD18400 has extensive circuit diagnostic information reporting capability. Use of this information can produce systems with intelligent feedback of switch status as well as load fault conditions for troubelshooting purposes. All of the diagnostic information is contained in an 11-bit word. This data can be clocked out of the LMD18400 in a serial fashion as shown in *Figure 8*. The shift register is parallel loaded with the diagnostic data whenever the Chip Select Input is at a Logic 1 and changes to the serial shift mode when Chip Select is taken to a Logic 0. The Data Output line (pin 8) is biased internally from a 5.1V regulator which sets the Logic 1 output voltage. This pin has low current sourcing capability so any load on this pin will reduce the Logic 1 output level which is guaranteed to be at least 2.4V with a 360 µA load.

The data interface is MICROWIRE compatible in that data is clocked out of the LMD18400 on the falling edge of the clock, to be clocked into the controlling microprocessor on the rising edge. Any number of devices can share a common data output line because the data output pin is held in a high impedance (TRI-STATE) condition until the device is selected by taking its Chip Select Input low. Following Chip Select going low there is a short data setup time interval (500 ns Min) required. This is necessary to allow the first data bit of information to be established on the data output line prior to the first rising clock edge which will input the data bit into the controller. When all 11 bits of diagnostic data have been shifted out the data output goes to a Logic 1 level until the Chip Select line is returned high.

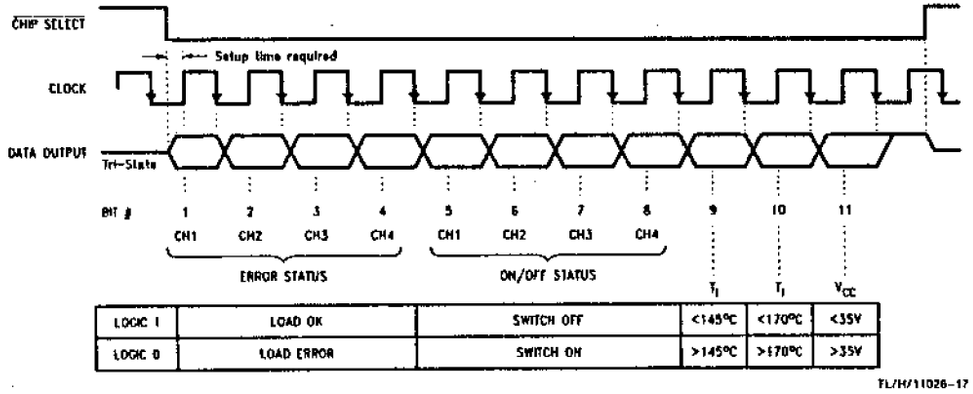
Figure 8 also indicates the significance of the diagnostic data bits. The first 4 bits indicate an output load error condition, one for each channel in succession (see Load Error Detection).

Bits 5 through 8 provide a readback of the commanded ON/OFF status of each switch.

A unique feature of the LMD18400 is that it provides an early warning of excessive operating temperature. Should the die temperature exceed + 145°C, bit 9 will be set to a Logic 0. Acting on this information a system can be programmed to take corrective action, shutting OFF specific loads perhaps, while the LMD18400 is still operating normally (not yet in thermal shutdown). If this early warning is ignored and the device continues to rise in temperature, the thermal shutdown circuitry will come into action at a die temperature of + 170°C. Should this occur bit 10 of the diagnostic data stream will be set to a Logic 0 indicating that the device is in thermal shutdown and all of the outputs have been shut OFF.

The final data bit, bit 11, indicates an overvoltage condition on the V_{CC} supply (V_{CC} is greater than 35V) and again indicates that all of the drivers are OFF.

The diagnostic data can be read periodically by a controller or only in the event of a general system error indication to determine the cause of any system problem. This general indication of a fault is provided by an Error Flag output (pin 13). This pin goes low whenever any type of error is detected. There is a built-in delay of approximately 75 µs from the time an error is detected until pin 13 is taken low. This is to help mask short duration error conditions such as may be caused by driving highly capacitive loads (> 2 µF). A lamp load may generate a shorted load error for several hundred milliseconds as it turns on which should be ignored.



LOGIC 1	LOAD OK	SWITCH OFF	<145°C	<170°C	<35V
LOGIC 0	LOAD ERROR	SWITCH ON	>145°C	>170°C	>35V

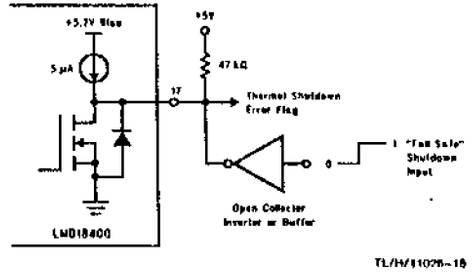
TL/H/11026–17

FIGURE 8. Serial Diagnostic Data Assignments

Applications Information (Continued)

The Error Flag output pin is an open drain transistor which requires a pull-up resistor to a positive voltage of up to 16V. Typically this pull-up is to the same 5V supply which is biasing the Enable input and any other external logic circuitry. The Error Flag pins of several LMD18400 packages can be connected together with just one pull-up resistor to provide an all-encompassing general system error indication. Upon detection of an error, each device could then be polled for diagnostic information to determine the source of the fault condition.

A second direct output error flag is for an indication of Thermal Shutdown (pin 17). This active low flag provides an immediate indication that the die temperature has reached + 170°C and that the drive to all four switches has been removed. This output is pulled up to the internal 5.1V logic regulator through a small (5 µA) current source so use of a buffer on this pin is recommended.



TL/H/11026–18

FIGURE 9. Thermal Shutdown Flag and Shutdown Input

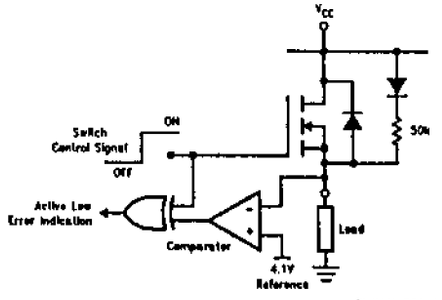
A useful feature of pin 17 is that it can also be used as a shutdown input. Driving this pin low immediately switches all of the drivers OFF, just the same as if thermal shutdown temperatures has been reached, yet all of the control logic and diagnostic circuits remain active. This is useful in designing "fail-safe" systems where the loads can be disabled under any sort of externally detected system fault condition. The diagnostic logic however does not distinguish between normal thermal shutdown or the fact that pin 17 has been driven low. As such, various switch errors and an over-temperature indication will be reported in the diagnostic data stream.

Figure 9 illustrates the use of pin 17 as both an output thermal shutdown flag and as an input to shut down only the switches. Directly tying pin 17 to + 5V will prevent the internal thermal shutdown circuitry from disabling the switches. For reliability purposes however this is not recommended as there will then be no limit to the maximum die temperature.

Refer to the Truth Table for a summary of the action of these direct-output error flags.

LOAD ERROR DETECTION

An important feature of the LMD18400 is the ability to detect open or shorted load connections. *Figure 10* illustrates the detection circuit used with each of the drivers.



TL/H/11026–19

FIGURE 10. Detection Circuitry for Open/Shorted Loads

A voltage comparator monitors the voltage to the load and compares it to a fixed 4.1V reference level. When a switch is OFF, the ground referenced load should have no voltage across it. Under this condition, an internal 50 kΩ resistor connected to V_{CC} will provide a small amount of current to the load. If the load resistance is large enough to create a voltage greater than 4.1V an Open Load Error will be indicated for that switch. The maximum load resistance that will not generate an Open Load Error when a switch is OFF can be found by:

$$R_{Max} = \frac{4.1V}{V_{CC} - 4.6V} \times 50\ k\Omega;\ \text{for no Open Load Indication}$$

To make this Open Load Error threshold more sensitive, an external pull-up resistor can be added from the output to the V_{CC} supply.

Also when a switch is commanded OFF, should the load be shorted to the V_{CC} supply, this same circuitry will again indicate an error.

When a switch is commanded ON, the load is expected to have a voltage across it that approaches the V_{CC} potential. If the output voltage is less than the 4.1V threshold an error will again be reported, indicating that the load is either shorted to ground or that the driver is in power limit and not able to pull the output voltage any closer to V_{CC}. The minimum load resistance that will not generate a Shorted Load Error when a switch is ON can be found by:

$$R_{Min} = \frac{4.1V\ (V_{CC} - 4.1V)}{15W};\ \text{for no Shorted Load Error}$$

Applications Information (Continued)

Figure 11 indicates the range of load resistance for normal operation, open load, and shorted load or power limit indication.

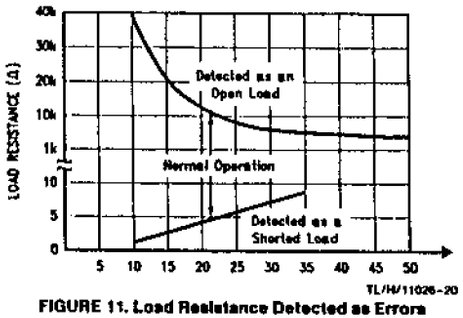


FIGURE 11. Load Resistance Detected as Errors

THERMAL MANAGEMENT

It is particularly important to consider the total amount of power being dissipated by all four switches in the LMD18400 at all times. Any combination of the switches driving loads will cause an increase in the die temperature. Should the die temperature reach the thermal shutdown threshold of +170°C, all of the switches will be disabled.

Careful calculation of the worst case total power dissipation required at any point in time, together with providing sufficient heatsinking will prevent this from occurring.

The LMD18400 is packaged with a special leadframe that helps dissipate heat through the two ground pins on each side of the package. The thermal resistance from junction-to-case (θ_{JC}) for this package is approximately 20°C/W. The thermal resistance from junction-to-ambient (θ_{JA}), without any heatsinking, is approximately 50°C/W. *Figure 12* illustrates how the copper foil of a printed circuit board can be designed to provide heatsinking and reduce the overall junction-to-ambient thermal resistance.

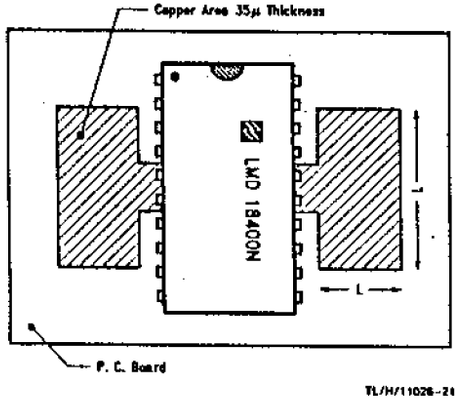
The power dissipation in each switch is equal to:

$$P_{D\ (Each\ Switch)} = I_{Load}^2 \times R_{ON} \quad or \quad \frac{(V_{CC} - V_{OUT})^2}{R_{ON}}$$

where R_{ON} is the ON resistance of the switch (1.3Ω maximum). These equations hold true until the power dissipation reaches the maximum limit of 15W. With resistive loads, the 15W power limit threshold will be reached when:

$$R_L \leq \frac{V_{CC}^2}{60W}$$

Inductive loads will create additional power dissipation when switched OFF. *Figure 13* shows the idealized voltage and current waveforms for an inductive load.



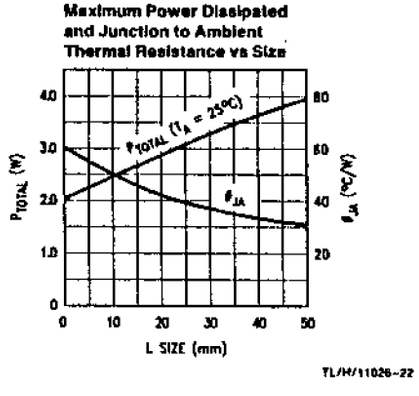


FIGURE 12. Recommended PC Board Layout to Reduce the Thermal Resistance from Junction-to-Ambient

Applications Information (Continued)

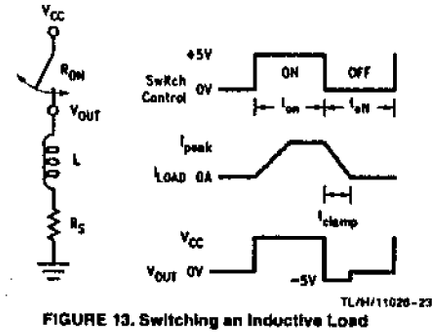


FIGURE 13. Switching an Inductive Load

When switched ON, the worst case power dissipation is:

$$P_{D(ON)} = I_{Peak}^2 \times R_{ON};\ where\ I_{Peak} = \frac{V_{CC}}{R_{ON} + R_S}$$

The steady-state ON current of the inductor should be kept less than 1A per power switch.

The additional power dissipation during turn-off, as the inductor is de-energized and the voltage across the inductor is clamped to −5V, can be found by:

$$P_{D(OFF)} = \frac{(V_{CC} + 5V) \times I_{Peak}}{2}$$

for the time interval, t_{Clamp}, which is the time required for the inductor current to fall to zero;

$$t_{Clamp} = \frac{I_{Peak} \times L}{5V}$$

The size of the inductor will determine the time duration for this additional power dissipation interval. Even though the peak current is kept less than 1A, the switch during this interval will see a voltage across it of V_{CC} + 5V with no power limit protection. If the inductor is too large, the time interval may be long enough to heat the die temperature to +170°C thereby shutting OFF all other loads on the package.

The total average power dissipation during a full ON/OFF switching cycle of an inductive load will be:

$$P_{D(tot)} = \left[I_{Peak}^2 R_{ON} t_{ON} + \frac{I_{Peak}^2 L (V_{CC} + 5V)}{10} \right] \frac{1}{t_{ON} + t_{OFF}}$$

Due to the common cut-off of all loads forced by thermal shutdown, the thermal time constants of the package become a concern. *Figure 14* provides an indication of the time it takes to heat the die to thermal shutdown with a step increase in package power dissipation from an initial junction temperature of +25°C. This data was measured using a PC board layout providing a thermal resistance from junction to ambient of approximately 35°C/W. Less heatsinking will, of course, result in faster thermal shutdown of the power switches.

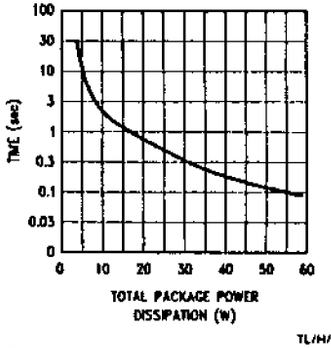
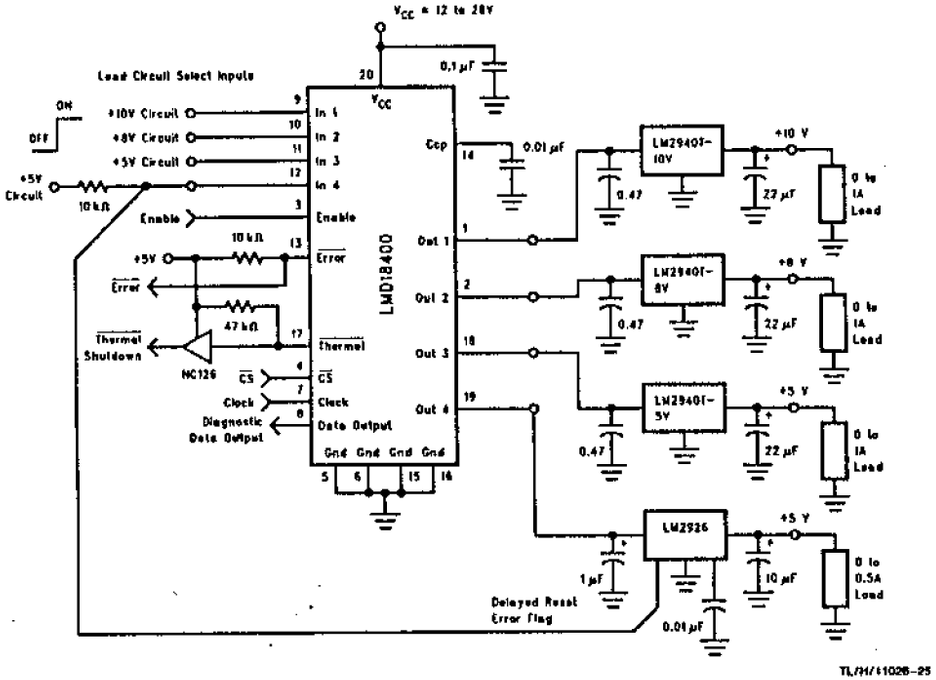


FIGURE 14. Approximate time required for the die to reach the 170°C thermal shutdown point from 25°C for different total package power dissipation levels.

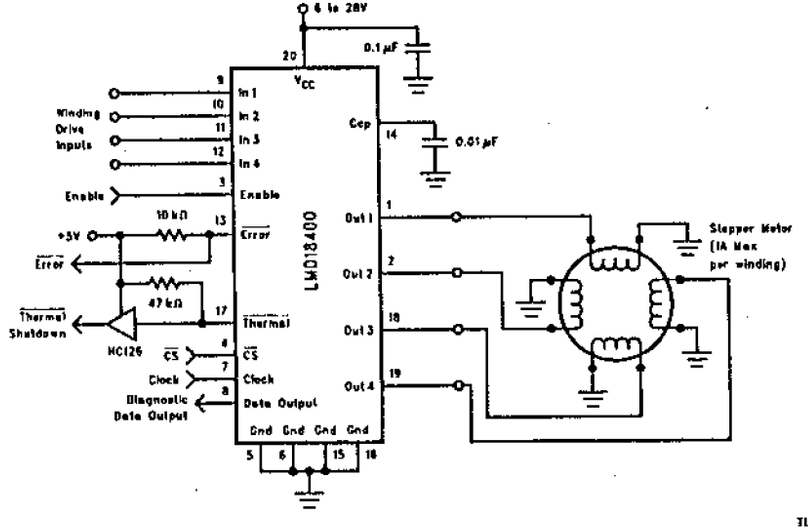
Applications

ON/OFF Switching of multiple voltage regulated circuit loads. Reset flag feedback from the LM2926 as shown connected to Output 4 makes the LMD18400 act as an electronic fuse for load faults.



TL/H/11026-25

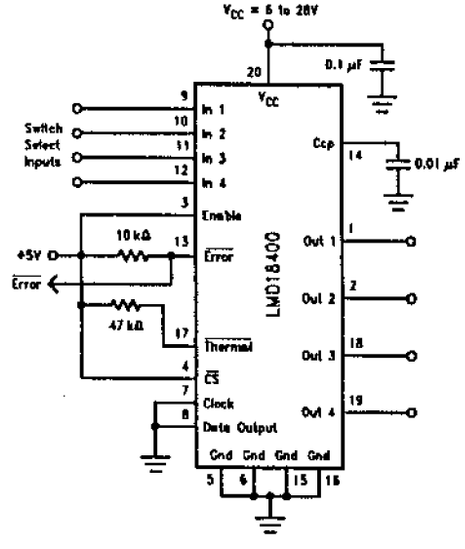
Unipolar Drive for a 4-Phase Stepper Motor



TL/H/11026-26

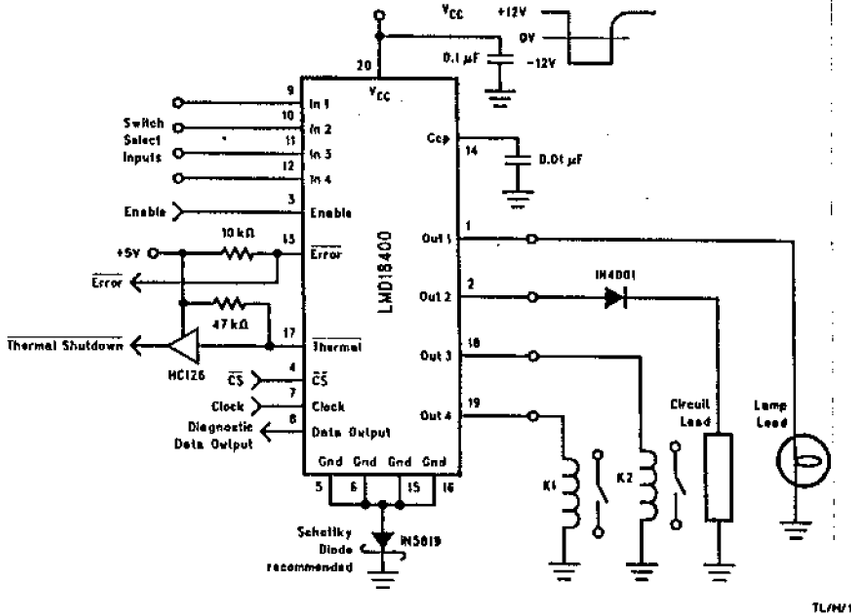
Applications (Continued)

Recommended Connection If No Diagnostics are Required



TL/H/11026-27

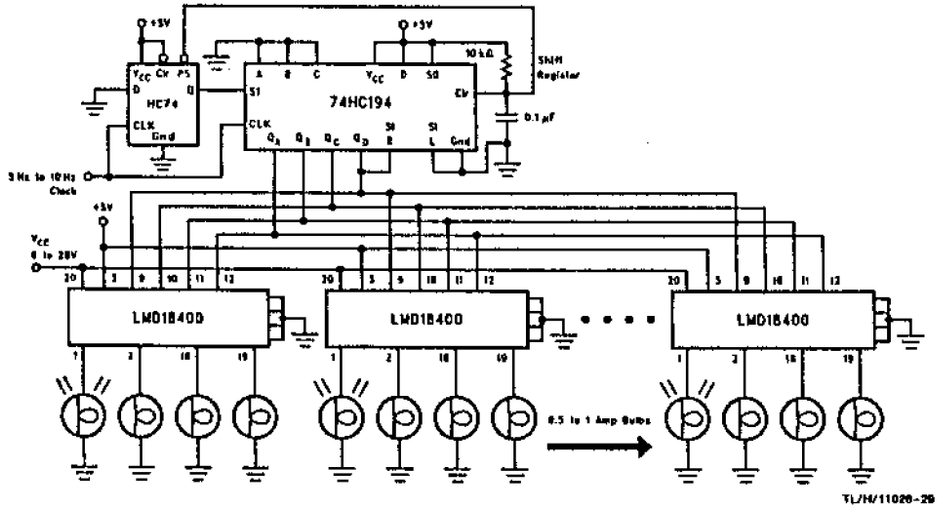
Simple protection of the LMD18400 against supply voltage reversal. Loads will be energized through the intrinsic diodes in parallel with the power switches. The Schottky diode will add approximately 0.2V to the logic input switching thresholds and the logic output low levels.



TL/H/11026-28

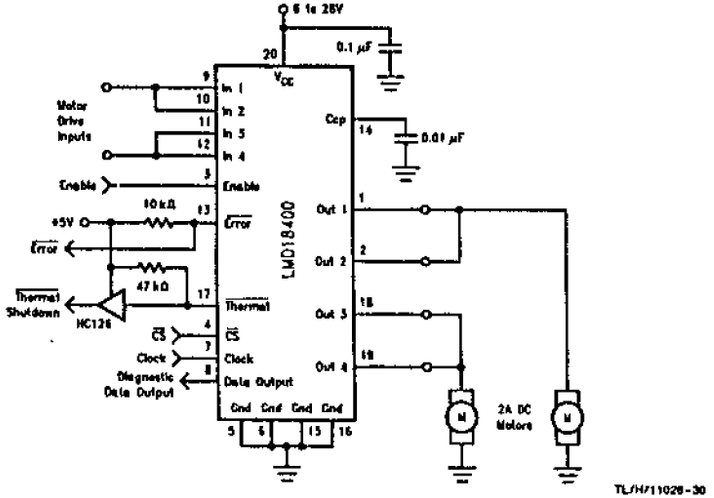
Applications (Continued)

Simple Light "Chaser"



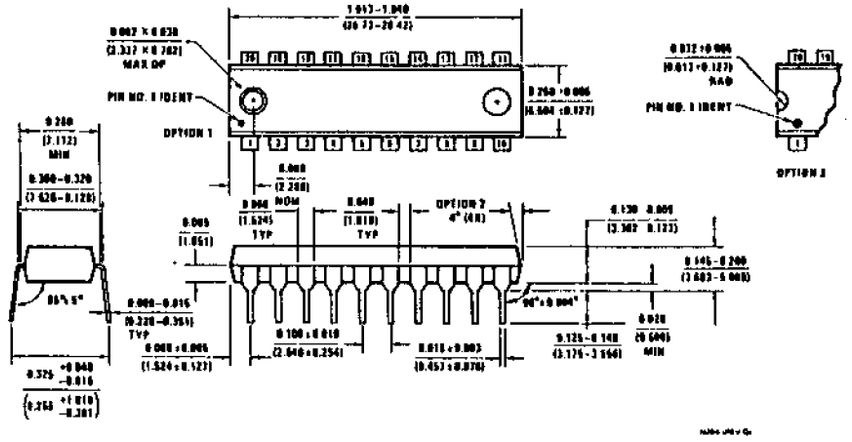
TL/H/11026-29

Paralleling switches for higher current capability. Positive temperature coefficient of the switch ON resistance provides ballasting to evenly share the load current between the switches. Any combination of switches can be paralleled. Required peak load current will depend upon the motor load. Motor speed control can be provided by a PWM signal of up to 20 kHz applied to the motor drive input lines.

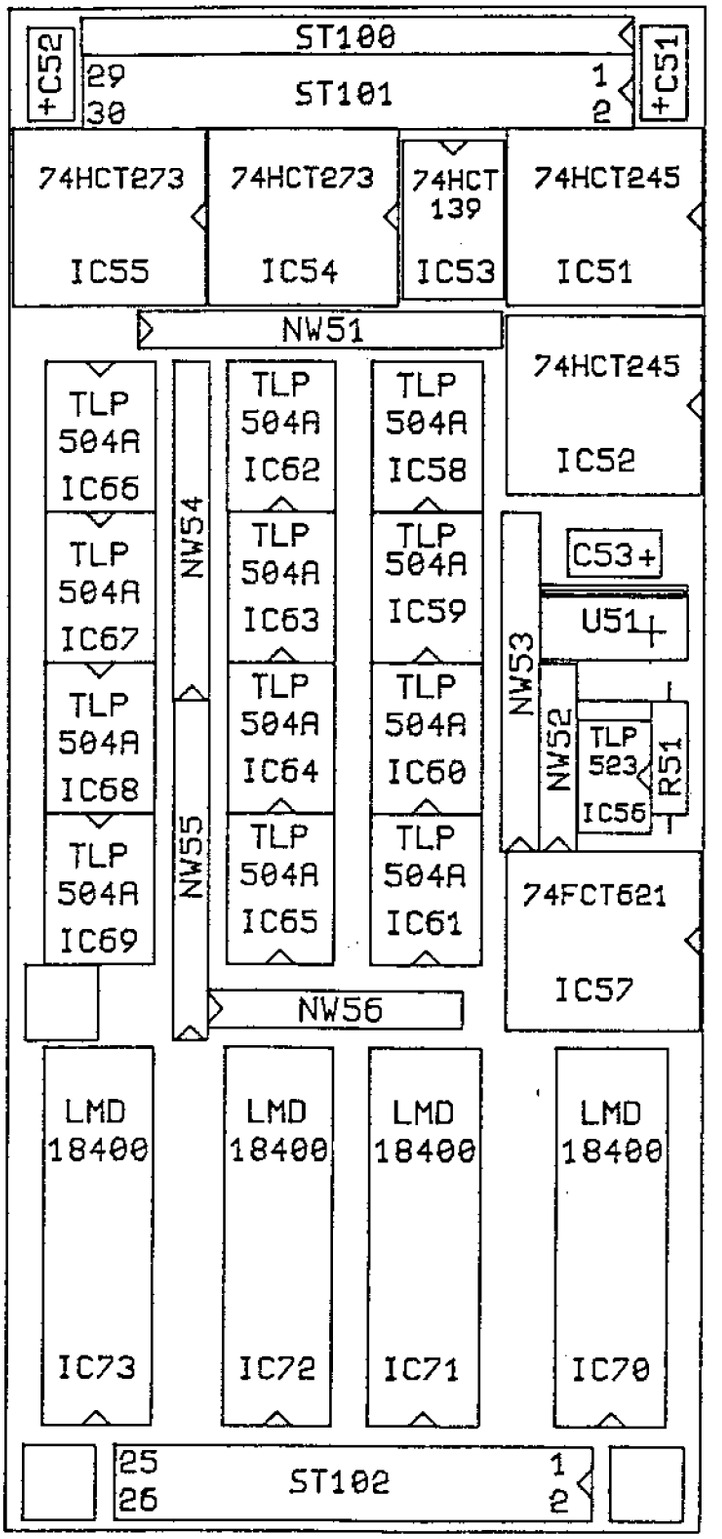


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Physical Dimensions inches (millimeters)



Order Number LMD18400N
NS Package Number N20A



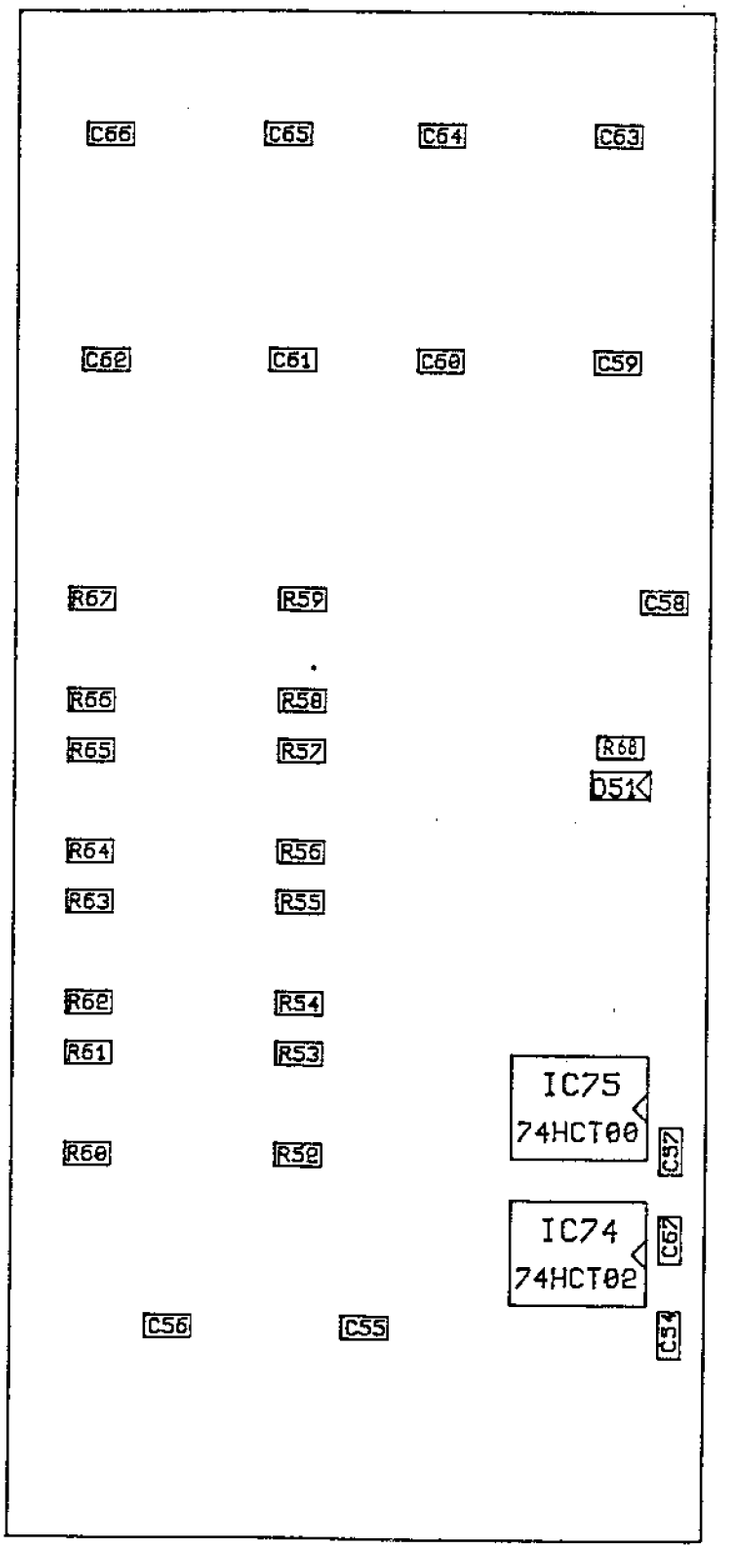
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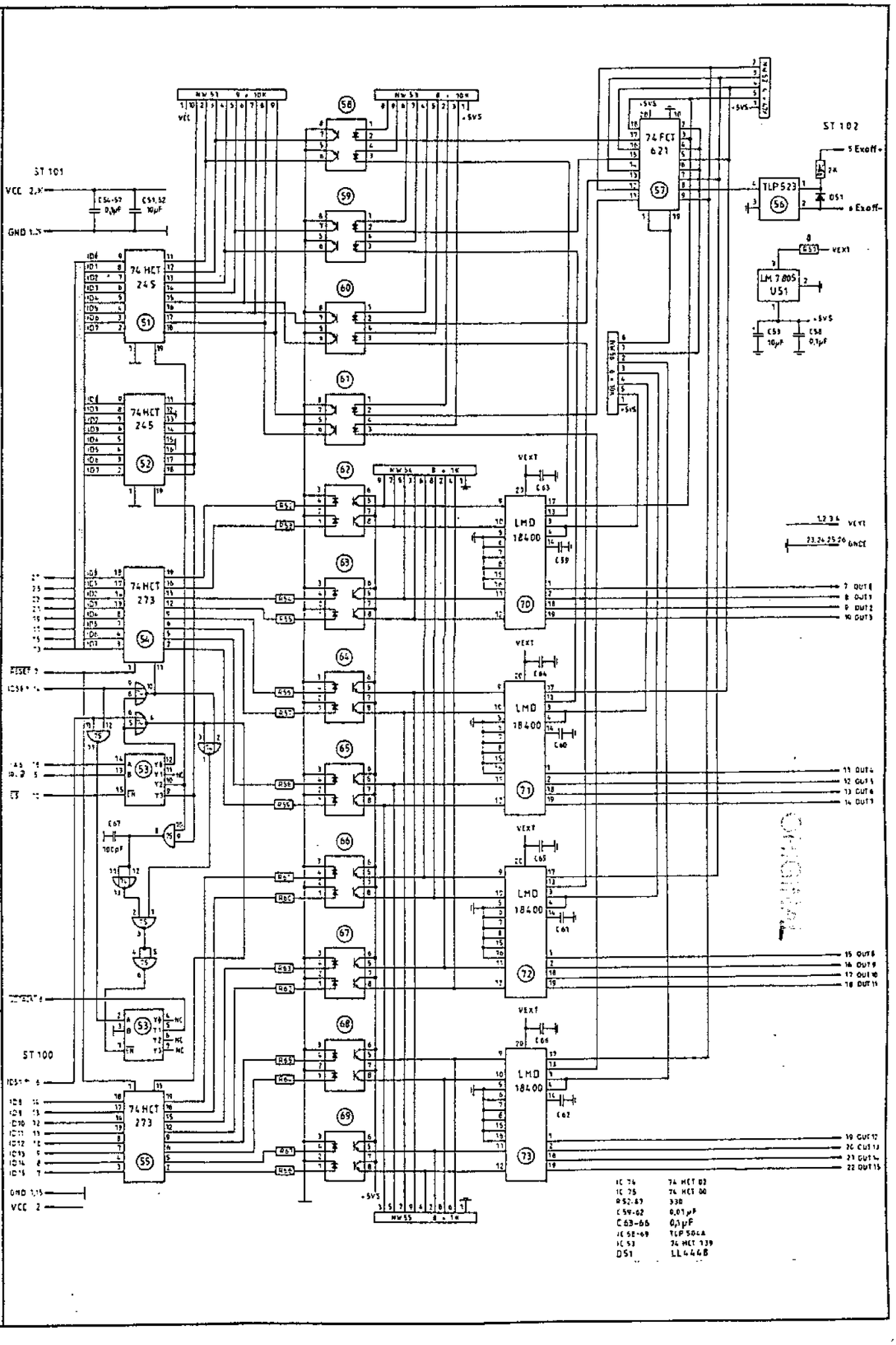
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IC 74	74 HCT 02
IC 75	74 HCT 00
R52-67	330
C59-62	0,01 µF
C63-66	0,1 µF
IC 58-69	TLP 504A
IC 53	74 HCT 139
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