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PCI-DAS6031 and PCI-DAS6033

Analog Input and Digital I/O

Specifications

Document Revision 1.3
December 2012
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MEASUREMENT COMPUTING™

PCI-DAS6031 and PCI-DAS6033 Specifications

All specifications are subject to change without notice.
Typical for 25 °C unless otherwise specified.
Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

Parameter	Specification
A/D converter	Successive Approximation type
Resolution	16-its, 1 in 65536
Maximum sample rate	100 kS/s
Number of channels	64 single-ended / 32 differential; software-selectable
Input ranges	Bipolar: ±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V, ±0.2 V, ±0.1 V Unipolar: 0 to 10 V, 0 to 5 V, 0 to 2 V, 0 to 1 V, 0 to 0.5 V, 0 to 0.2 V, 0 to 0.1 V Software-selectable
A/D pacing	Internal counter – ASIC. Software-selectable time base: ▪ Internal 40 MHz, 50 ppm stability ▪ External source via AUXIN<5:0>; software-selectable.
	External convert strobe: A/D CONVERT
	Software paced
Burst mode	Software-selectable option; burst rate = 10 µS
A/D gate sources	External digital: A/D GATE
	External analog: ATRIG input CH0 IN through CH63 IN
A/D gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Refer to the Analog Trigger section on page 8
A/D trigger sources	External digital: A/D START TRIGGER A/D STOP TRIGGER
	External analog: ATRIG input CH0 IN through CH63 IN
A/D triggering modes	External digital: Software-configurable for rising or falling edge
	External analog: Refer to the Analog Trigger section on page 8
	Pre-/Post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples
ADC pacer out	Available at user connector: A/D PACER OUT
RAM buffer size	8 K samples
Data transfer	DMA
	Programmed I/O
DMA modes	Demand or non-demand using scatter-gather
Configuration memory	Up to 8 k elements. Programmable channel, gain, and offset
Streaming-to-disk rate	100 kS/s, system dependent

Accuracy

100 kS/s sampling rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within ±1°C of internal calibration temperature and ±10°C of factory calibration temperature. Calibrator test source high side tied to Channel 0 High and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 2. Absolute Accuracy

Range	Absolute Accuracy
±10 V	±3.76 LSB
±5 V	±13.61 LSB
±2 V	±13.70 LSB
±1 V	±13.83 LSB
±500 mV	±14.09 LSB
±200 mV	±16.71 LSB
±100 mV	±19.99 LSB
0 V to 10 V	±6.40 LSB
0 V to 5 V	±26.11 LSB
0 V to 2 V	±26.28 LSB
0 V to 1 V	±26.54 LSB
0 mV to 500 mV	±27.13 LSB
0 mV to 200 mV	±32.11 LSB
0 mV to 100 mV	±38.67 LSB

Table 3. Absolute Accuracy Components – All values are (±)

Range	% of Reading	Offset (µV)	Noise +Quantization (µV)		Temp Drift (%/ºC)	Absolute Accuracy at FS (mV)
			Single Pt	Averaged (Note 1)		
±10 V	0.0061	479.2	634.1	54.9	0.0001	1.147
±5 V	0.0361	243.6	317.1	27.5	0.0006	2.077
±2 V	0.0361	102.2	126.8	11.0	0.0006	0.836
±1 V	0.0361	55.1	63.4	5.5	0.0006	0.422
±500 mV	0.0361	31.6	36.8	3.2	0.0006	0.215
±200 mV	0.0411	17.4	22.5	2.0	0.0006	0.102
±100 mV	0.0461	12.7	19.6	1.8	0.0006	0.061
0 V to 10 V	0.0061	326.6	417.8	36.6	0.0001	0.976
0 V to 5 V	0.0361	167.3	208.9	18.3	0.0006	1.992
0 V to 2 V	0.0361	71.7	83.6	7.3	0.0006	0.802
0 V to 1 V	0.0361	39.9	41.8	3.7	0.0006	0.405
0 mV to 500 mV	0.0361	23.9	28.1	2.5	0.0006	0.207
0 mV to 200 mV	0.0411	14.4	19.6	1.8	0.0006	0.098
0 mV to 100 mV	0.0461	11.2	18.1	1.7	0.0006	0.059

Note 1: Averaged measurements assume averaging of 100 single-channel readings.
Each PCI-DAS6031 and PCI-DAS6033 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 2.

Table 4. Relative Accuracy specifications – All values are (±)

Range	Relative Accuracy (µV)	
	Single Point	**Averaged (Note 2)**
±10 V	723.3	72.3
±5 V	361.6	36.2
±2 V	144.7	14.5
±1 V	72.3	7.2
±500 mV	42.2	4.2
±200 mV	26.5	2.7
±100 mV	24.1	2.4
0 to 10 V	482.2	48.2
0 to 5 V	241.1	24.1
0 to 2 V	96.4	9.6
0 to 1 V	48.2	4.8
0 to 500 mV	33.1	3.3
0 to 200 mV	24.1	2.4
0 to 100 mV	22.9	2.3

Note 2: Averaged measurements assume averaging of 100 single-channel readings.
Relative accuracy is the measured deviation from a straight line drawn between measured endpoints of the transfer function. ADC resolution, noise and front-end non-linearity are included in this measurement.

Table 5. Differential non-linearity

All ranges	±0.5 LSB typ	±1.0 LSB max

Settling time

Settling time is the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at the specified rate. A –FS DC signal is presented to Channel 1; a +FS DC signal is presented to Channel 0.

Table 6. Settling time specifications

Condition	Range	±0.00076% (±0.5 LSB)	±0.0015% (±1 LSB)	±0.0061% (±4 LSB)	±0.012% (±8 LSB)
Same range to same range	±10 V	50 µS max	25 µS max	10 µS max	5 µS typ
	±5 V	50 µS max	25 µS max	10 µS max	5 µS typ
	±2 V	50 µS max	25 µS max	10 µS max	5 µS typ
	±1 V	50 µS max	25 µS max	10 µS max	5 µS typ
	±500 mV	50 µS max	25 µS max	10 µS max	5 µS typ
	±200 mV	50 µS max	25 µS max	10 µS max	5 µS typ
	±100 mV	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 10 V	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 5 V	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 2 V	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 1 V	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 500 mV	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 200 mV	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 100 mV	50 µS max	25 µS max	10 µS max	5 µS typ

Parametrics

Table 7. Parametric specifications

Parameter	Specification
Max working voltage (signal + common-mode)	±11 V
CMRR @ 60 Hz	±10 V range and 0 to 10 V: 92 dB
	±5 V range and 0 to 5 V: 97 dB
	±2 V range and 0 to 2 V: 101 dB
	±1 V range and 0 to 1 V: 104 dB
	±0.5 V range and 0 to 0.5 V: 105 dB
	±0.2 V range and 0 to 0.2 V: 105 dB
	±0.1 V range and 0 to 0.1 V: 105 dB
Small signal bandwidth, all ranges	*255 kHz*
Input coupling	*DC*
Input impedance	*100 GΩ in normal operation*
Input bias current	*±200 pA*
Input offset current	*±100 pA*
Absolute maximum input voltage	*Power ON: ±25 V, Power OFF: ±15 V (±20 mA Note 3)* *Protected inputs:* ▪ *CH<63:0> IN* ▪ *AISENSE*
Power on and reset state	CH0 IN, single-ended mode, 0 V to 0.1 V input range (Note 4)
Crosstalk	Adjacent channels: –75 dB
	All other channels: –90 dB

Note 3: The analog input sink/source current must be limited to an maximum of ±20 mA in the power OFF state to prevent damage to the board. A 1000 Ω (¼ W) current limiting resistor should be placed in series with each analog input channel being used in applications where the power OFF state sink/source current into the board can exceed ±20 mA. Resistance values >1000 Ω may adversely affect the noise and settling time performance of the board.

Note 4: Care should be taken to avoid the application of an input voltage to CH0 IN that could overdrive the analog input circuit. Any unused analog input channel should be connected to LLGND.

Noise performance

Table 8 summarizes the noise performance for the PCI-DAS6031 and PCI-DAS6033. Noise distribution is determined by gathering 50 k samples with inputs tied to ground at the user connector. Samples are gathered 100 kS/s sampling rate. The specification applies to both single-ended and differential modes of operation.

Table 8. Analog input noise performance specifications

Range	LSBrms	Typical Counts
±10 V	0.6	8
±5 V	0.6	8
±2 V	0.6	8
±1 V	0.6	8
±500 mV	0.7	8
±200 mV	1.1	11
±100 mV	2.0	17
0 V to 10 V	0.8	8
0 V to 5 V	0.8	8
0 V to 2 V	0.8	8
0 V to 1 V	0.8	8
0 mV to 500 mV	1.1	11
0 mV to 200 mV	2.0	17
0 mV to 100 mV	3.8	25

Analog output (PCI-DAS6031 only)

Table 9. PCI-DAS6031 analog output specifications

Parameter	Specification
D/A converter type	Double-buffered, multiplying
Resolution	16-bits, 1 in 65,536
Number of channels	2 voltage output
Voltage range	±10 V, 0 to 10 V, software-selectable
Monotonicity	*16-bits, guaranteed*
Slew rate	5 V/µs typ
Settling time (full scale step)	10 µs max to ±1 LSB
Noise	60 µVrms, DC to 1 MHz BW
Current drive	±5 mA
Output short-circuit duration	*Indefinite @ 25 mA*
Output coupling	*DC*
Output impedance	0.1 Ω max
Power up and reset	DACs cleared to 0 volts ±20 mV max

Table 10. Analog output absolute accuracy specifications

Range	Absolute Accuracy
±10 V	±4.7 LSB
0 to 10 V	±7.9 LSB

Table 11. Absolute accuracy components - All values are (±)

Range	% of Reading	Offset (µV)	Temp Drift (%/ºC)	Absolute Accuracy at FS (mV)
±10 V	0.0062	813	0.0001	1.430
0 to 10 V	0.0062	584	0.0001	1.201

Each PCI-DAS6031 is tested at the factory to assure that the board overall error does not exceed the values specified in Table 10.

Table 12. Relative accuracy specifications

Range	Relative Accuracy	
All ranges	±0.5 LSB, typ	±1.0 LSB, max

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

Analog output pacing and triggering

Table 13. Analog output pacing and triggering specifications

Parameter	Specification
DAC pacing (software programmable)	Internal counter – ASIC. Selectable time base: ▪ Internal 40 MHz, 50 ppm stability. ▪ External Source via AUXIN<5:0>, SW selectable.
	External convert strobe: D/A UPDATE
	Software paced
DAC gate sources (software programmable)	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH63 IN
	Software gated
DAC gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Refer to the Analog Trigger section on page 8
DAC trigger sources	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH63 IN
	Software triggered
DAC triggering modes	External digital: Software-configurable for rising or falling edge.
	External analog: Software-configurable for positive or negative slope.
DAC pacer Out	Available at user connector D/A PACER OUT
RAM buffer Size	16 K samples
Data transfer	DMA
	Programmed I/O
	Update DACs individually or simultaneously; software-selectable.
DMA modes	Demand or non-demand using scatter gather.
Waveform generation throughput	100 kS/s max per channel, 2 channels simultaneous

Analog trigger

Table 14. Analog trigger specifications

Parameter	Specification	
Analog trigger sources Software-selectable	External: ATRIG input CH0 IN through CH63 IN, first channel in scan	
Analog trigger levels	ATRIG input: ±10 V	
	CH0 IN through CH63 IN: Full-scale, range dependent	
Analog trigger modes	External analog: Software-configurable for: ▪ Positive or negative slope	
Analog gate modes	External analog: Software-configurable for: ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window	
Resolution	12-bits, 1 in 4,096	
Accuracy	±1% of full-scale range max	
Bandwidth (-3 dB)	ATRIG input	4 MHz
	CH0 IN through CH63 IN	255 kHz

Analog input / output calibration

Table 15. Analog I/O calibration specifications

Parameter	Specification
Recommended warm-up time	15 minutes
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Onboard calibration reference	*DC Level: 5.000 V± 1 mV. Actual measured values stored in EEPROM.*
	Tempco: 0.6 ppm/°C max
	Long-term stability: ±6 ppm/sqrt (1000 hrs)
Calibration interval	1 year

Digital input/output

Table 16. Digital I/O specifications

Parameter	Specification
Digital type	Discrete, 5 V/TTL compatible
Number of I/O	8
Configuration	8-bits, independently programmable for input or output. All pins pulled up to +5 V via 47 k resistors (default). Positions available for pull-down to ground. Hardware selectable via zero Ohm resistors.
Input high voltage	2.0 V min, 7.0 V absolute max
Input low voltage	0.8 V max, –0.5 V absolute min
Output high voltage (IOH = -32 mA)	3.80 V min, 4.20 V typ
Output low voltage (IOL = 32 mA)	0.55 V max, 0.22 V typ
Data transfer	Programmed I/O
Power-up / reset state	Input mode (high impedance)

Interrupts

Table 17. Interrupt specifications

Parameter	Specification	
Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time	
Interrupt enable	Programmable through PLX9080	
ADC Interrupt sources (software programmable)	DAQ_ACTIVE:	Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP:	Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE:	Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL:	Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE:	Interrupt is generated after each conversion completes.
	DAQ_EOSCAN:	Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ:	Interrupt is generated after each interval delay during multi-channel scans.
DAC Interrupt sources (software programmable)	DAC_ACTIVE:	Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE:	Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY:	Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL:	Interrupt is generated when the DAC high channel output is updated.

Counters

Table 18. Counter specifications

Parameter	Specification
User counter type	82C54
Number of channels	2
Resolution	16-bits
Compatibility	5 V/TTL
CTRn base clock source	Software-selectable: ▪ Internal 10 MHz ▪ Internal 100 kHz ▪ External connector (CTRn CLK)
Internal 10 MHz clock source stability	50 ppm
Counter n gate	Available at connector (CTRn GATE)
Counter n output	Available at connector (CTRn OUT)
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*15 ns min*
Low pulse width (clock input)	*25 ns min*
Gate width high	*25 ns min*
Gate width low	*25 ns min*
Input low voltage	*0.8 V max*
Input high voltage	*2.0V min*
Output low voltage	*0.4V max*
Output high voltage	*3.0V min*

Configurable AUXIN<5:0>, AUXOUT<2:0> external trigger/clocks

The PCI-DAS6031 and PCI-DAS6033 provide nine user-configurable trigger/clock pins available at the 100-pin I/O connector. Of these, six are configurable as inputs, while three are configurable as outputs.

Table 19. Configurable triggers/clocks specifications

Parameter	Specification	
AUXIN<5:0> sources (Software-selectable)	A/D CONVERT:	External ADC convert strobe
	A/D TIMEBASE IN:	External ADC pacer time base
	A/D START TRIGGER:	ADC Start Trigger
	A/D STOP TRIGGER:	ADC Stop Trigger
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER:	DAC trigger/gate
	D/A UPDATE:	DAC update strobe
	D/A TIMEBASE IN:	External DAC pacer time base
AUXOUT<2:0> sources (Software-selectable)	STARTSCAN:	A pulse indicating start of conversion
	SSH:	Active signal that terminates at the start of the last conversion in a scan.
	A/D STOP:	Indicates end of scan
	A/D CONVERT:	ADC convert pulse
	SCANCLK:	Delayed version of ADC convert
	CTR1 CLK:	CTR1 clock source
	D/A UPDATE:	D/A update pulse
	CTR2 CLK:	CTR2 clock source
	A/D START TRIGGER:	ADC Start Trigger Out
	A/D STOP TRIGGER:	ADC Stop Trigger Out
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER:	DAC Start Trigger Out
Default selections	AUXIN0:	A/D CONVERT
	AUXIN1:	A/D START TRIGGER
	AUXIN2:	A/D STOP TRIGGER
	AUXIN3:	D/A UPDATE
	AUXIN4:	D/A START TRIGGER
	AUXIN5:	A/D GATE
	AUXOUT0:	D/A UPDATE
	AUXOUT1:	A/D CONVERT
	AUXOUT2:	SCANCLK
Compatibility	5 V/TTL	
Minimum pulse width	37.5 ns	

DAQ-Sync inter-board triggers/clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

Table 20. DAQ-Sync signals

Parameter	Specification
DAQ-Sync signals:	DS A/D START TRIGGER
	DS A/D STOP TRIGGER
	DS A/D CONVERT
	DS D/A UPDATE
	DS D/A START TRIGGER
	SYNC CLK

Power consumption

Table 21. Power consumption specifications

Parameter	Specification
+5 V	PCI-DAS6031/32: 1.3 A typ, 1.5 A max Does not include power consumed through the I/O connector.
+5 V available at I/O connector	1 A max, protected with a resettable fuse

Environmental

Table 22. Environmental specifications

Parameter	Specification
Operating temperature range	0 °C to 55 °C
Storage temperature range	–20 to 70 °C
Humidity	0% to 90% non-condensing

Mechanical

Table 23. Mechanical Specifications

Parameter	Specification
Card dimensions (L × W × H)	PCI half card: 174.4 (6.87) × 106.9 (4.21) × 11.65 mm (0.46 in.)

DAQ-Sync connector and pinout

Table 24. DAQ-Sync connector specifications

Parameter	Specification
Connector type	14-pin right-angle 100 mil box header
Compatible cables	MCC p/n: CDS-14-x, 14-pin ribbon cable. x = number of boards (2 to 5)

Table 25. DAQ-Sync connector pinout

Pin	Signal Name
1	DS A/D START TRIGGER
2	GND
3	DS A/D STOP TRIGGER
4	GND
5	DS A/D CONVERT
6	GND
7	DS D/A UPDATE
8	GND
9	DS D/A START TRIGGER
10	GND
11	RESERVED
12	GND
13	SYNC CLK
14	GND

SCSI connector

Table 26. SCSI connector specifications

Parameter	Specification
Connector type	Shielded SCSI 100 D-type
Compatible cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet
	C100MMS-x, shielded round cable. x = 1, 2, or 3 meters
Compatible accessory products (with C100HD50-x cable)	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50
Compatible accessory products (with C100MMS-x cable)	SCB-100 BNC-16DI-FE

Table 27. 32-channel differential mode pinout

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	LLGND
2	CH0 IN HI	52	CH16 IN HI
3	CH0 IN LO	53	CH16 IN LO
4	CH1 IN HI	54	CH17 IN HI
5	CH1 IN LO	55	CH17 IN LO
6	CH2 IN HI	56	CH18 IN HI
7	CH2 IN LO	57	CH18 IN LO
8	CH3 IN HI	58	CH19 IN HI
9	CH3 IN LO	59	CH19 IN LO
10	CH4 IN HI	60	CH20 IN HI
11	CH4 IN LO	61	CH20 IN LO
12	CH5 IN HI	62	CH21 IN HI
13	CH5 IN LO	63	CH21 IN LO
14	CH6 IN HI	64	CH22 IN HI
15	CH6 IN LO	65	CH22 IN LO
16	CH7 IN HI	66	CH23 IN HI
17	CH7 IN LO	67	CH23 IN LO
18	LLGND	68	LLGND
19	CH8 IN HI	69	CH24 IN HI
20	CH8 IN LO	70	CH24 IN LO
21	CH9 IN HI	71	CH25 IN HI
22	CH9 IN LO	72	CH25 IN LO
23	CH10 IN HI	73	CH26 IN HI
24	CH10 IN LO	74	CH26 IN LO
25	CH11 IN HI	75	CH27 IN HI
26	CH11 IN LO	76	CH27 IN LO
27	CH12 IN HI	77	CH28 IN HI
28	CH12 IN LO	78	CH28 IN LO
29	CH13 IN HI	79	CH29 IN HI
30	CH13 IN LO	80	CH29 IN LO
31	CH14 IN HI	81	CH30 IN HI
32	CH14 IN LO	82	CH30 IN LO
33	CH15 IN HI	83	CH31 IN HI
34	CH15 IN LO	84	CH31 IN LO
35	AISENSE	85	DIO0
36	D/A OUT 0 *	86	DIO1
37	D/A GND	87	DIO2
38	D/A OUT1 *	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT / ATRIG	93	CTR1 CLK
44	N/C	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = N/C on PCI-DAS6033

Table 28. 64-channel single-ended mode pinout

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	LLGND
2	CH0 IN	52	CH16 IN
3	CH32 IN	53	CH48 IN
4	CH1 IN	54	CH17 IN
5	CH33 IN	55	CH49 IN
6	CH2 IN	56	CH18 IN
7	CH34 IN	57	CH50 IN
8	CH3 IN	58	CH19 IN
9	CH35 IN	59	CH51 IN
10	CH4 IN	60	CH20 IN
11	CH36 IN	61	CH52 IN
12	CH5 IN	62	CH21 IN
13	CH37 IN	63	CH53 IN
14	CH6 IN	64	CH22 IN
15	CH38 IN	65	CH54 IN
16	CH7 IN	66	CH23 IN
17	CH39 IN	67	CH55 IN
18	LLGND	68	LLGND
19	CH8 IN	69	CH24 IN
20	CH40 IN	70	CH56 IN
21	CH9 IN	71	CH25 IN
22	CH41 IN	72	CH57 IN
23	CH10 IN	73	CH26 IN
24	CH42 IN	74	CH58 IN
25	CH11 IN	75	CH27 IN
26	CH43 IN	76	CH59 IN
27	CH12 IN	77	CH28 IN
28	CH44 IN	78	CH60 IN
29	CH13 IN	79	CH29 IN
30	CH45 IN	80	CH61 IN
31	CH14 IN	81	CH30 IN
32	CH46 IN	82	CH62 IN
33	CH15 IN	83	CH31 IN
34	CH47 IN	84	CH63 IN
35	AISENSE	85	DIO0
36	D/A OUT 0 *	86	DIO1
37	D/A GND	87	DIO2
38	D/A OUT1 *	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT / ATRIG	93	CTR1 CLK
44	N/C	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = N/C on PCI-DAS6033

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