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PCI-DAS6031 and PCI-DAS6033

Analog and Digital I/O

User's Guide

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MEASUREMENT COMPUTING™

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About this User's Guide

What you will learn from this user's guide

This user's guide describes the Measurement Computing PCI-DAS6031 and PCI-DAS6033 data acquisition devices and lists device specifications.

Conventions in this user's guide

For more information

Text presented in a box signifies additional information related to the subject matter.

Caution! Shaded caution statements present information to help you avoid injuring yourself and others, damaging your hardware, or losing your data.

bold text — **Bold** text is used for the names of objects on a screen, such as buttons, text boxes, and check boxes.

italic text — *Italic* text is used for the names of manuals and help topic titles, and to emphasize a word or phrase.

Where to find more information

Additional information about PCI-DAS6031 and PCI-DAS6033 hardware is available on our website at www.mccdaq.com. You can also contact Measurement Computing Corporation by phone, fax, or email with specific questions.

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com
- Knowledgebase: kb.mccdaq.com

If you need to program at the register level in your application, refer to the *STC Register Map for the PCI-DAS6000 Series*. This document is available at www.mccdaq.com/registermaps/RegMapSTC6000.pdf.

Introducing the PCI-DAS6031 and PCI-DAS6033

Overview: PCI-DAS6031 and PCI-DAS6033 features

This manual explains how to install and use the PCI-DAS6031 and PCI-DAS6033 boards.

The PCI-DAS6031 and PCI-DAS6033 boards provide either 32 differential or 64 single-ended analog inputs with 16 bit resolution. Input ranges are software selectable as either Bipolar or Unipolar.

- Bipolar input ranges: ±10V, ±5V, ±2.0V, ±1V, ±0.5V, ±0.2V, and ±0.1V.
- Unipolar input ranges: 0 to 10V, 0 to 5V, 0 to 2V, 0 to 1V, 0 to 0.5V, 0 to 0.2V and 0 to 0.1V.

The PCI-DAS6031 and PCI-DAS6033 have eight lines of digital I/O. The PCI-DAS6031 also provides two digital-to-analog outputs.

Each board has nine user-configurable trigger/clock/gate pins that are available at a 100-pin I/O connector. Six pins are configurable as inputs and three are configurable as outputs. Refer to Chapter 3 ("Functional Details") and Chapter 5 ("Specifications") for more information.

The PCI-DAS6031 and PCI-DAS6033 provide triggering and synchronization capability. There are five trigger/strobes and a synchronizing clock provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction can be set. Refer to Chapter 2 ("Installing the Board") and Chapter 5 ("Specifications") for more information on these signals.

Interrupts can be generated by up to seven ADC sources and four DAC sources. Interrupt sources are listed in Chapter 5 ("Specifications").

The PCI-DAS6031 and PCI-DAS6033 boards contain an 82C54 counter chip, which consists of three 16-bit counters. Clock, gate, and output signals from two of the three counters are available on the 100-pin I/O connector. The third counter is used internally.

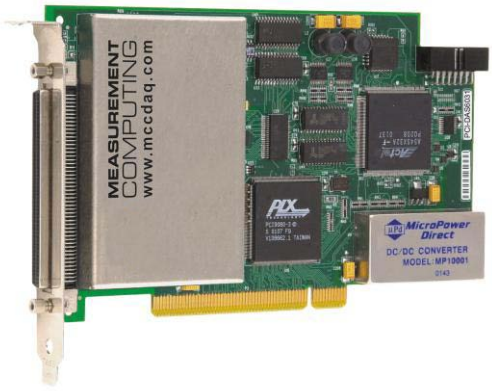
Installing the PCI-DAS6031 and PCI-DAS6033

What comes with your shipment?

As you unpack your board, make sure each of the items shown below is included.

Hardware

- PCI-DAS6031 or PCI-DAS6033



PCI-DAS6031



PCI-DAS6033

Documentation

In addition to this hardware user's guide, you should also receive the *Quick Start Guide*. This booklet provides an overview of the MCC DAQ software you received with the device, and includes information about installing the software. Please read this booklet completely before installing any software or hardware.

Optional components

If you ordered any of the following products with your board, they should be included with your shipment.

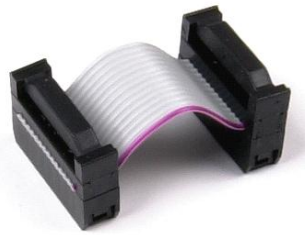
- Cables



C100HD50-x



C100MMS-x



CDS-14-*x*

- Signal termination and conditioning accessories

  MCC provides signal termination products for use with the PCI-DAS6031 and PCI-DAS6033. Refer to the "Field wiring, signal termination and conditioning" section on page 14 for a complete list of compatible accessory products.

Unpacking the hardware

As with any electronic device, you should take care while handling to avoid damage from static electricity. Before removing the PCI-DAS6031 and PCI-DAS6033 from its packaging, ground yourself using a wrist strap or by simply touching the computer chassis or other grounded object to eliminate any stored static charge.

If any components are missing or damaged, notify Measurement Computing Corporation immediately by phone, fax, or e-mail:

- Phone: 508-946-5100 and follow the instructions for reaching Tech Support.
- Fax: 508-946-9500 to the attention of Tech Support
- Email: techsupport@mccdaq.com

For international customers, contact your local distributor. Refer to the International Distributors section on our web site at www.mccdaq.com/International.

Installing the software

Install the MCC DAQ software before you install your board. The driver needed to run the board is installed with the MCC DAQ software. Refer to the *Quick Start Guide* for instructions on installing the software on the MCC DAQ CD. This booklet is available in PDF at www.mccdaq.com/PDFmanuals/DAQ-Software-Quick-Start.pdf.

Installing the hardware

The PCI-DAS6031 and PCI-DAS6033 boards are completely plug-and-play, with no switches or jumpers to set. Configuration is controlled by your system's BIOS. To install your board, follow the steps below.

Install the MCC DAQ software before you install your board

The driver needed to run your board is installed with the MCC DAQ software. Therefore, you need to install the MCC DAQ software before you install your board. Refer to the *Quick Start Guide* for instructions on installing the software.

1. Turn your computer off, open it up, and insert your board into an available PCI slot.
2. Close your computer and turn it on.

   If you are using an operating system with support for plug-and-play, a dialog box notifies you that new hardware has been detected. If the information file for this board is not already loaded onto your PC, you will be prompted for the disk containing this file. The MCC DAQ software contains this file. If required, insert the MCC DAQ CD and click **OK**.
3. To test your installation and configure your board, run the *Insta*Cal utility you installed in the previous section. Refer to the *Quick Start Guide* that came with your board for information on how to initially set up and load InstaCal.

If your board has been powered-off for more than 10 minutes, allow your computer to warm up for at least 15 minutes before acquiring data. This warm-up period is required for the board to achieve its rated accuracy. The high speed components used on the board generate heat, and it takes this amount of time for a board to reach steady state if it has been powered off for a significant amount of time.

Configuring the hardware

All hardware configuration options on the PCI-DAS6031 and PCI-DAS6033 are software controlled. You can select some of the configuration options using InstaCal, such as the analog input configuration (64 single-ended or 32 differential channels), the edge used for triggering when using an external pacer, and the source for the two independent counters.

Once configured, any program that uses the Measurement Computing Universal Library™ will initialize the hardware according to these selections.

Following is an overview of the available hardware configuration options for these boards. There is additional general information regarding analog signal connection and configuration in the *Guide to DAQ Signal Connections* (available on our web site at www.mccdaq.com/signals/signals.pdf).

Differential input mode

When all channels are configured for differential input mode, 32 analog input channels are available. In this mode, the input signal is measured with respect to the low input. The input signal is delivered through three wires:

- The wire carrying the signal to be measured connects to CH# IN HI.
- The wire carrying the reference signal connects to CH# IN LO.
- The third wire is connected to LLGND.

Differential input mode is the preferred configuration for applications in noisy environments, or when the signal source is referenced to a potential other than PC ground.

Single-ended input mode

When all channels are configured for single-ended input mode, 64 analog input channels are available. In this mode, the input signal is referenced to the board's signal ground (LLGND). The input signal is delivered through two wires:

- The wire carrying the signal to be measured connects to CH# IN HI.
- The other wire is connected to LLGND.

Non-referenced single-ended input mode

Non-referenced single-ended mode is a compromise between differential and single-ended modes. It offers some of the advantages of each mode. You can still get noise rejection with this mode, but not the limitation in the number of channels resulting from a fully differential configuration. A possible downside is that the external reference input must be the same for every channel. It is equivalent to configuring the inputs for differential mode and then tying all of the low inputs together and using that node as the reference input.

In non-referenced single-ended input mode, 64 analog input channels are available. In this mode, each input signal is referenced to a common reference signal (AISENSE), and not to the board's ground. The input signal is delivered through three wires:

- The wire carrying the signal to measure connects to CH# IN HI.
- The wire carrying the reference signal connects to AISENSE.
- The third wire is connected to LLGND.

This mode is useful when the application calls for differential input mode but the limitation on channel count prevents it.

DAQ-Sync configuration

You can interconnect multiple boards in the PCI-DAS6000 series to synchronize data acquisition or data output. To do this, order and install a CDS-14-*x* cable at the DAQ-Sync connectors (P2) between the boards to be synchronized. Each system can have one master and up to four slaves.

The "x" in the CDS-14-x part number specifies the number of connectors available on the cable, and therefore, the number of boards you can interconnect. Using a CDS-14-2, you can connect two PCI-DAS6000 series boards together for I/O synchronization. Using a CDS-14-3, you can synchronize three boards, and so on. You can connect up to five PCI-DAS6000 series boards. A CDS-14-3 cable is shown in Figure 3 on page 14.

By default, all DAQ-Sync connectors are configured as inputs (slave mode). In order to be useful, use software to configure one board as the master and to define the signal sources of the slave boards. Refer to DAQ-Sync signals on page 16 for more information.

Connecting the board for I/O operations

Connectors, cables – main I/O connector

The table below lists the board connectors, applicable cables and compatible accessory boards.

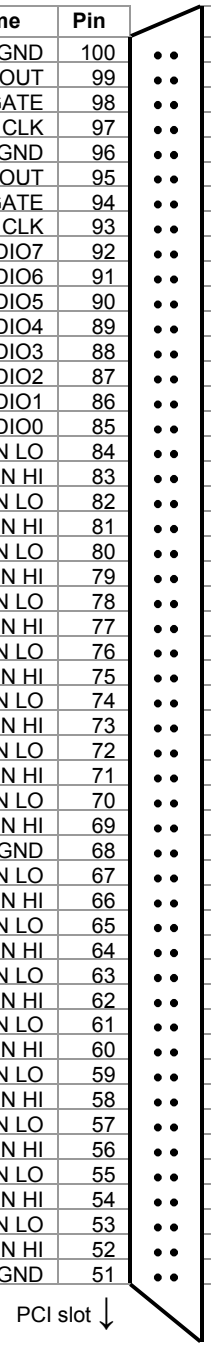
Board connectors, cables, accessory equipment

Connector type	Shielded SCSI 100 D-type
Compatible cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet (Figure 1)
	C100MMS-x, shielded round cable. x = 1, 2, or 3 meters (Figure 2)
Compatible accessory products with the C100HD50-x cable	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50
Compatible accessory products with the C100MMS-x cable	SCB-100 BNC-16DI-FE

Pin out – main I/O connector

32-channel differential mode pin out

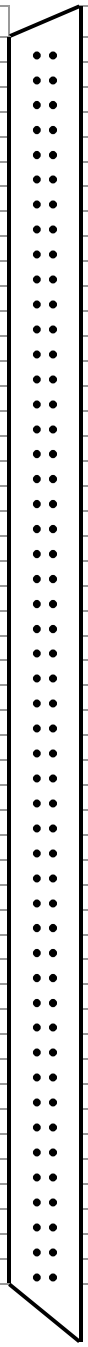
Signal Name	Pin	Pin	Signal Name
GND	100	50	GND
CTR2 OUT	99	49	AUXIN5 / A/D PACER GATE
CTR2 GATE	98	48	AUXIN4 / D/A START TRIGGER
CTR2 CLK	97	47	AUXIN3 / D/A UPDATE
GND	96	46	AUXIN2 / A/D STOP TRIGGER
CTR1 OUT	95	45	AUXIN1 / A/D START TRIGGER
CTR1 GATE	94	44	N/C
CTR1 CLK	93	43	AUXIN0 / A/D CONVERT / ATRIG
DIO7	92	42	AUXOUT2 / SCANCLK
DIO6	91	41	AUXOUT1 / A/D PACER OUT
DIO5	90	40	AUXOUT0 / D/A PACER OUT
DIO4	89	39	PC +5 V
DIO3	88	38	D/A OUT1 *
DIO2	87	37	D/A GND
DIO1	86	36	D/A OUT 0 *
DIO0	85	35	AISENSE
CH31 IN LO	84	34	CH15 IN LO
CH31 IN HI	83	33	CH15 IN HI
CH30 IN LO	82	32	CH14 IN LO
CH30 IN HI	81	31	CH14 IN HI
CH29 IN LO	80	30	CH13 IN LO
CH29 IN HI	79	29	CH13 IN HI
CH28 IN LO	78	28	CH12 IN LO
CH28 IN HI	77	27	CH12 IN HI
CH27 IN LO	76	26	CH11 IN LO
CH27 IN HI	75	25	CH11 IN HI
CH26 IN LO	74	24	CH10 IN LO
CH26 IN HI	73	23	CH10 IN HI
CH25 IN LO	72	22	CH9 IN LO
CH25 IN HI	71	21	CH9 IN HI
CH24 IN LO	70	20	CH8 IN LO
CH24 IN HI	69	19	CH8 IN HI
LLGND	68	18	LLGND
CH23 IN LO	67	17	CH7 IN LO
CH23 IN HI	66	16	CH7 IN HI
CH22 IN LO	65	15	CH6 IN LO
CH22 IN HI	64	14	CH6 IN HI
CH21 IN LO	63	13	CH5 IN LO
CH21 IN HI	62	12	CH5 IN HI
CH20 IN LO	61	11	CH4 IN LO
CH20 IN HI	60	10	CH4 IN HI
CH19 IN LO	59	9	CH3 IN LO
CH19 IN HI	58	8	CH3 IN HI
CH18 IN LO	57	7	CH2 IN LO
CH18 IN HI	56	6	CH2 IN HI
CH17 IN LO	55	5	CH1 IN LO
CH17 IN HI	54	4	CH1 IN HI
CH16 IN LO	53	3	CH0 IN LO
CH16 IN HI	52	2	CH0 IN HI
LLGND	51	1	LLGND



* = N/C on the PCI-DAS6033

64-channel single-ended mode pin out

Signal Name	Pin	Pin	Signal Name
GND	100	50	GND
CTR2 OUT	99	49	AUXIN5 / A/D PACER GATE
CTR2 GATE	98	48	AUXIN4 / D/A START TRIGGER
CTR2 CLK	97	47	AUXIN3 / D/A UPDATE
GND	96	46	AUXIN2 / A/D STOP TRIGGER
CTR1 OUT	95	45	AUXIN1 / A/D START TRIGGER
CTR1 GATE	94	44	N/C
CTR1 CLK	93	43	AUXIN0 / A/D CONVERT / ATRIG
DIO7	92	42	AUXOUT2 / SCANCLK
DIO6	91	41	AUXOUT1 / A/D PACER OUT
DIO5	90	40	AUXOUT0 / D/A PACER OUT
DIO4	89	39	PC +5 V
DIO3	88	38	D/A OUT1 *
DIO2	87	37	D/A GND
DIO1	86	36	D/A OUT 0 *
DIO0	85	35	AISENSE
CH63 IN	84	34	CH47 IN
CH31 IN	83	33	CH15 IN
CH62 IN	82	32	CH46 IN
CH30 IN	81	31	CH14 IN
CH61 IN	80	30	CH45 IN
CH29 IN	79	29	CH13 IN
CH60 IN	78	28	CH44 IN
CH28 IN	77	27	CH12 IN
CH59 IN	76	26	CH43 IN
CH27 IN	75	25	CH11 IN
CH58 IN	74	24	CH42 IN
CH26 IN	73	23	CH10 IN
CH57 IN	72	22	CH41 IN
CH25 IN	71	21	CH9 IN
CH56 IN	70	20	CH40 IN
CH24 IN	69	19	CH8 IN
LLGND	68	18	LLGND
CH55 IN	67	17	CH39 IN
CH23 IN	66	16	CH7 IN
CH54 IN	65	15	CH38 IN
CH22 IN	64	14	CH6 IN
CH53 IN	63	13	CH37 IN
CH21 IN	62	12	CH5 IN
CH52 IN	61	11	CH36 IN
CH20 IN	60	10	CH4 IN
CH51 IN	59	9	CH35 IN
CH19 IN	58	8	CH3 IN
CH50 IN	57	7	CH34 IN
CH18 IN	56	6	CH2 IN
CH49 IN	55	5	CH33 IN
CH17 IN	54	4	CH1 IN
CH48 IN	53	3	CH32 IN
CH16 IN	52	2	CH0 IN
LLGND	51	1	LLGND



* = N/C on the PCI-DAS6033

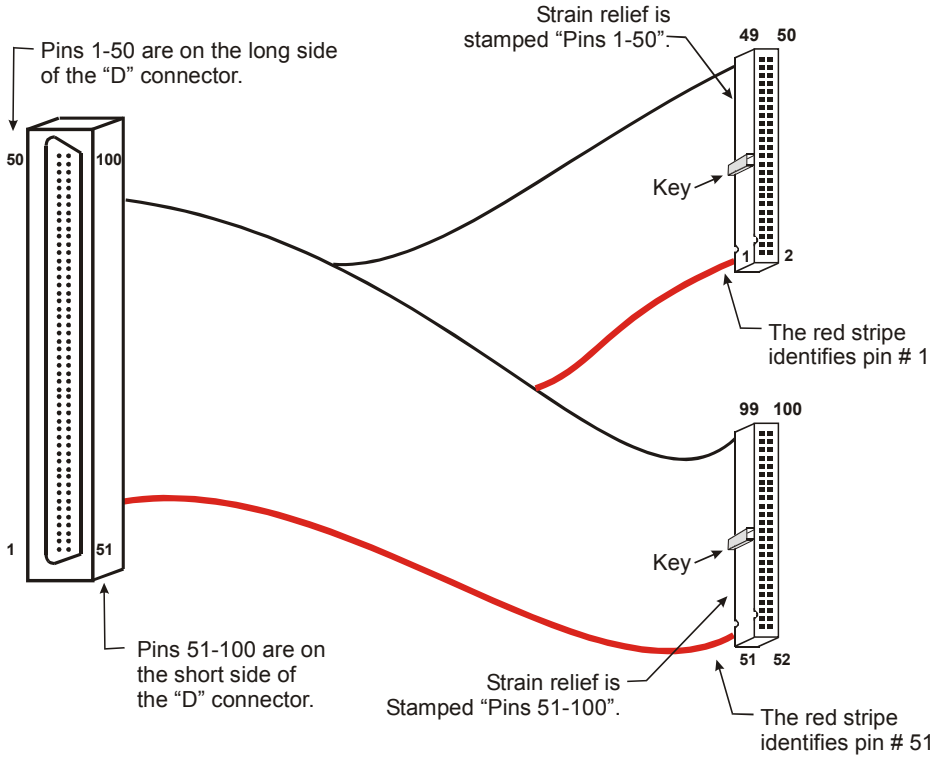


Figure 1. C100HD50-*x* cable connections

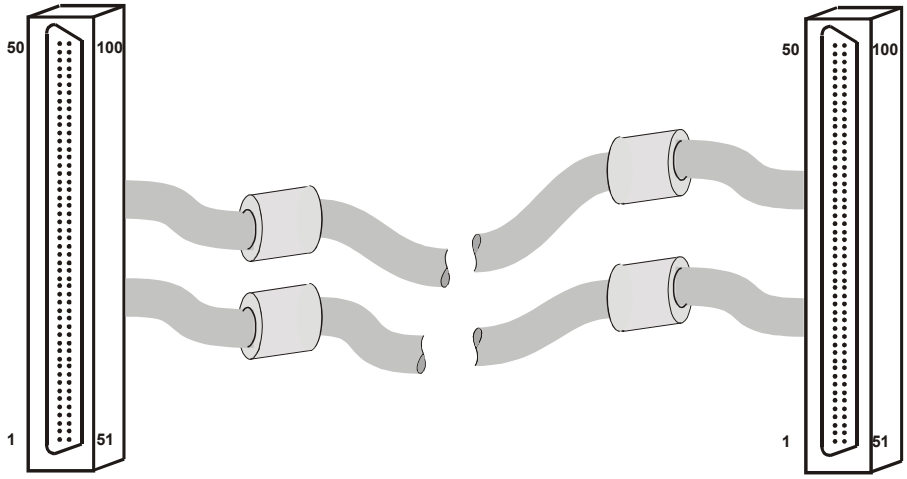


Figure 2. C100MMS-*x* cable

Details on these cables are available on our web site at www.mccdaq.com/products/accessories.aspx.

DAQ-Sync connector and pinout

DAQ-Sync Connector & Cable Types

Connector type	14-pin right-angle 100 mil box header
Compatible cables	MCC p/n CDS-14-x, 14-pin ribbon cable for board-to board DAQ-Sync connection; x = number of boards (from 2 - 5). See Figure 3.

DAQ-Sync connector pinout (view from top)

Signal Name	Pin		Pin	Signal Name
DS A/D START TRIGGER	1	■ ■	2	GND
DS A/D STOP TRIGGER	3	■ ■	4	GND
DS A/D CONVERT	5	■ ■	6	GND
DS D/A UPDATE	7	■ ■	8	GND
DS D/A START TRIGGER	9	■ ■	10	GND
RESERVED	11	■ ■	12	GND
SYNC CLK	13	■ ■	14	GND

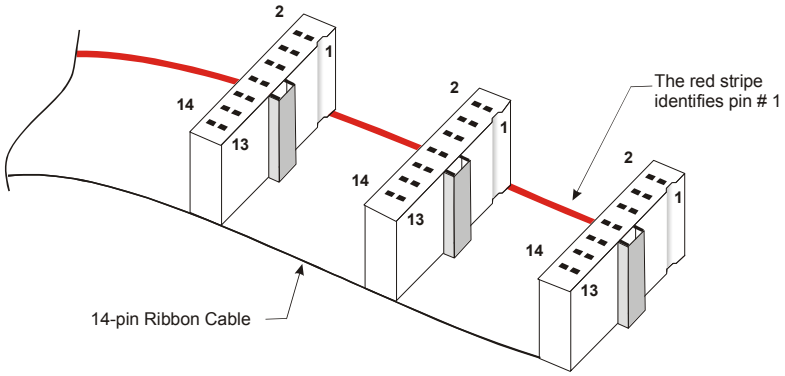


Figure 3. CDS-14-3 cable

Field wiring, signal termination and conditioning

You can use the following accessory boards with the C100HD50-*x* cable.

- ISO-RACK16/P – 16-channel, 5B module rack
- ISO-DA02/P – 2-channel, 5B module rack
- BNC-16SE – 16-channel single-ended BNC connector box
- BNC-16DI – 8-channel differential BNC connector box
- CIO-MINI50 – 50-pin screw terminal board
- CIO-TERM100 – 100-pin screw terminal board with positions for pull-up resistors
- SCB-50 – 50-conductor, shielded signal connection box

You can use the following accessory boards with the C100MMS-*x* cable

- SCB-100 – 100-conductor, shielded signal connection box
- BNC-16DI-FE – 16-channel BNC connector box

Details on screw terminal boards and BNC connector boxes are available on our web site at www.mccdaq.com/products/screw_terminal_bnc.aspx.

Details on ISO-5B module racks are available on our web site at www.mccdaq.com/products/signal_conditioning.aspx.

Functional Details

Basic architecture

Figure 4 on page 17 shows a simplified block diagram of the PCI-DAS6031 and PCI-DAS6033. These boards provide all of the functional elements shown in the diagram.

The System Timing and Control (STC) is the logical center for all DAQ, DIO, and DAC (if applicable) operations. It communicates over two major busses: a local bus and a memory bus.

The local bus carries digital I/O data and software commands from the PCI Bus Master. There are two Direct Memory Access (DMA) channels provided for data transfers to the PC.

Primarily, the memory bus carries A/D and D/A related data and commands. There are three buffer memories provided on the memory bus:

- The *queue buffer* (8K configuration memory) stores programmed channel numbers, gains, and offsets.
- The *ADC buffer* (8K FIFO [First In, First Out]) temporarily stores scanned and converted analog inputs.
- The *DAC 16K buffer* stores data to be output as analog waveforms.

Auxiliary input & output interface

The board's 100-pin I/O connector provides six software-selectable inputs and three software-selectable outputs. The signals are user-configurable clocks, triggers and gates.

Refer to "DAQ signal timing" on page 17 for information about these signals and their timing requirements.

The following table lists the possible signals and the default signals of the nine pins.

Auxiliary I/O Signals

I/O Type	Signal Name	Function
AUXIN<5:0> sources (SW selectable)	A/D CONVERT	External ADC Convert Strobe (default)
	A/D TIMEBASE IN	External ADC Pacer Time Base
	A/D START TRIGGER	ADC Start Trigger (default)
	A/D STOP TRIGGER	ADC Stop Trigger (default)
	A/D PACER GATE	External ADC Gate (default)
	D/A START TRIGGER	DAC Trigger/Gate (default)
	D/A UPDATE	DAC Update Strobe (default)
	D/A TIMEBASE IN	External DAC Pacer Time Base
AUXOUT<2:0> sources (SW selectable)	STARTSCAN	A pulse indicating the start of conversion.
	SSH	An active signal that terminates at the start of the last conversion in a scan.
	A/D STOP	Indicates the end of a scan
	A/D CONVERT	ADC convert pulse (default)
	SCANCLK	Delayed version of ADC convert (default)
	CTR1 CLK	CTR1 clock source
	D/A UPDATE	D/A update pulse (default)
	CTR2 CLK	CTR2 clock source
	A/D START TRIGGER	ADC Start Trigger Out
	A/D STOP TRIGGER	ADC Stop Trigger Out
	A/D PACER GATE	External ADC gate
	D/A START TRIGGER	DAC Start Trigger Out
Default selections summary	AUXIN0	A/D CONVERT
	AUXIN1	A/D START TRIGGER
	AUXIN2	A/D STOP TRIGGER
	AUXIN3	D/A UPDATE
	AUXIN4	D/A START TRIGGER
	AUXIN5	A/D PACER GATE
	AUXOUT0	D/A UPDATE
	AUXOUT1	A/D CONVERT
	AUXOUT2	SCANCLK

DAQ-Sync signals

With DAQ-Sync hardware, you can trigger or clock up to four slave boards from a master board to synchronize data input and/or output.

The PCI-DAS6031 and PCI-DAS6033 boards provide the capability of inter-board synchronization between boards in the PCI-DAS6000 Series family. There are five trigger/strobes and a synchronizing clock provided on a 14-pin header. The following signals are available:

- DS A/D START TRIGGER
- DS A/D STOP TRIGGER
- DS A/D CONVERT
- DS D/A UPDATE
- DS D/A START TRIGGER
- SYNC CLK

Except for the SYNC CLK signal, the DAQ-Sync timing and control signals are a subset of the AUXIO signals available at the 100-pin I/O connector. These versions of the signals are used for board-to-board synchronization and have the same timing specifications as their I/O connector counterparts. Refer to "DAQ signal timing" on page 17 for explanations of signals and timing.

Use the SYNC CLCK signal to determine the master/slave configuration of a DAQ-Sync-enabled system. Each system can have one master and up to four slaves. SYNC CLK is the 40 MHz time-base used to derive all board

timing and control. The master provides this clock to the slave boards so that all boards in the DAQ-Sync-enabled system are timed from the same clock.

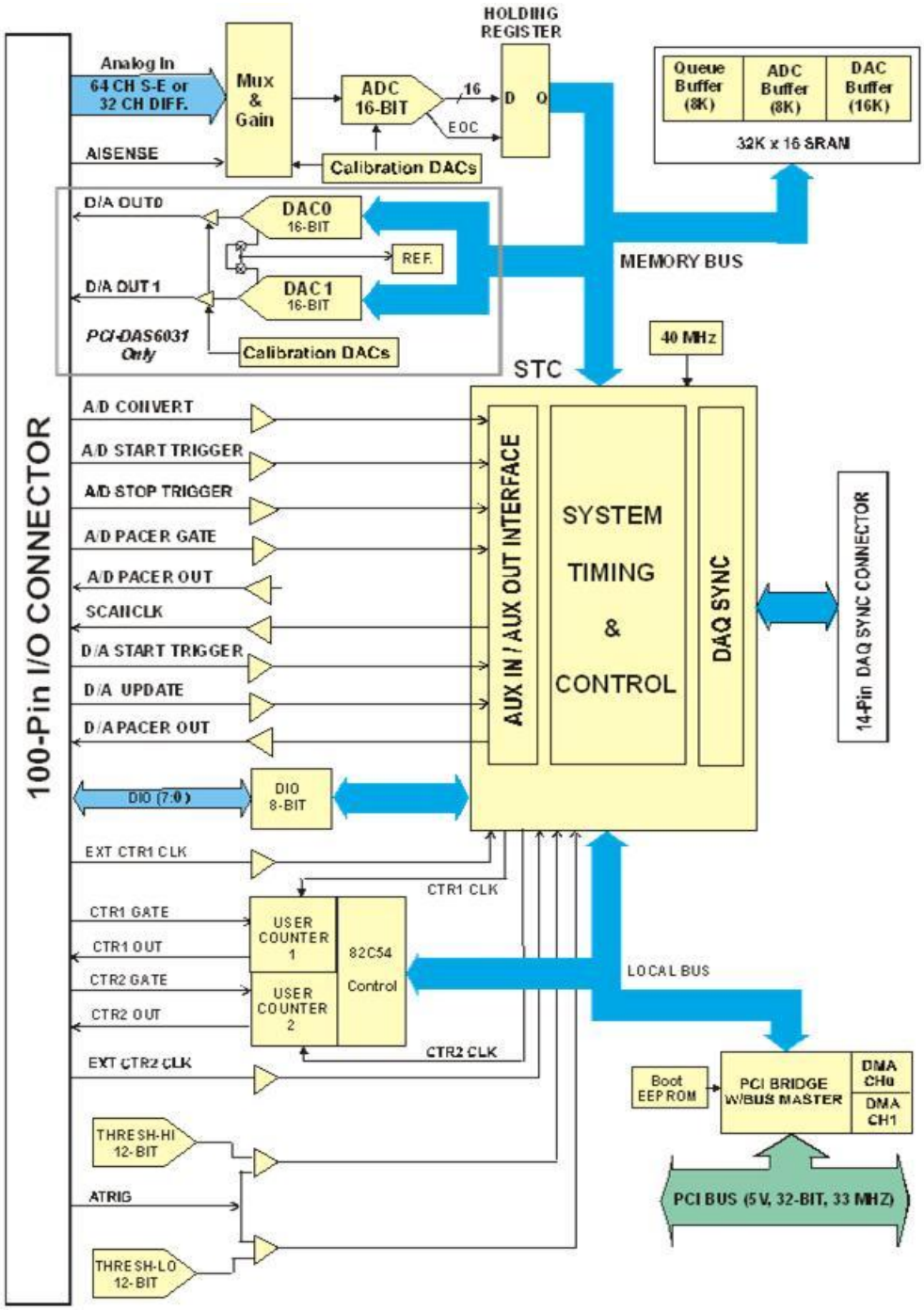


Figure 4. Block diagram – PCI-DAS6031 and PCI-DAS6033

DAQ signal timing

The DAQ timing signals are:

- SCANCLK
- A/D START TRIGGER
- A/D STOP TRIGGER

- STARTSCAN
- SSH
- A/D CONVERT
- A/D PACER GATE
- A/D EXTERNAL TIME BASE
- A/D STOP
- ATRIG

SCANCLK signal

SCANCLK is an output signal that may be used for switching external multiplexers. It is a 400 ns wide pulse that follows the CONVERT signal after a 50 ns delay. This is adequate time for the analog input signal to be acquired so that the next signal may be switched in. The polarity of the SCANCLK signal is programmable. The default output pin for the SCANCLK signal is AUXOUT2, but any of the AUXOUT pins may be programmed as a SCANCLK output.

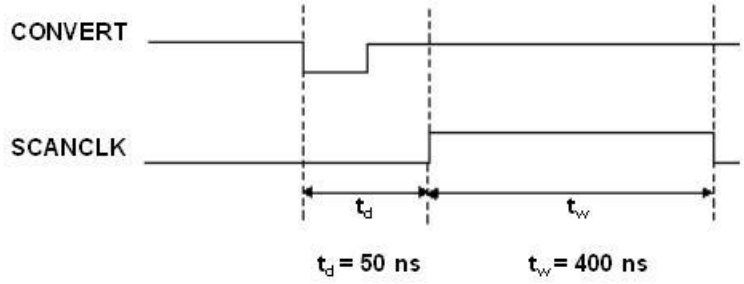


Figure 5. SCANCLK signal timing

A/D START TRIGGER signal

Use the A/D START TRIGGER signal for conventional triggering (when you only need to acquire data after a trigger event). Figure 6 shows the A/D START TRIGGER signal timing for a conventionally triggered acquisition.

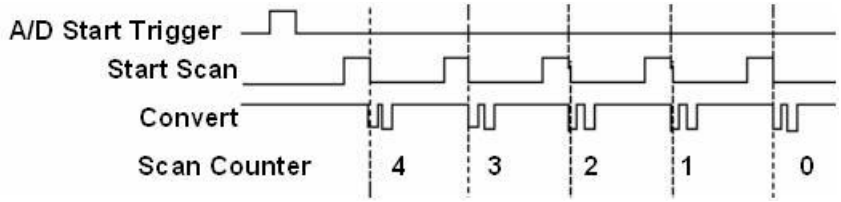


Figure 6. Data acquisition example for conventional triggering

The A/D START TRIGGER source is programmable for any of the AUXIN inputs or to the DAQ-Sync DS A/D START TRIGGER input. The polarity of this signal is also programmable to trigger acquisitions on either the positive or negative edge.

The A/D START TRIGGER signal is also available as an output and can be programmed to appear at any of the AUXOUT outputs. Refer to Figure 7 and Figure 8 for A/D START TRIGGER input and output timing requirements.

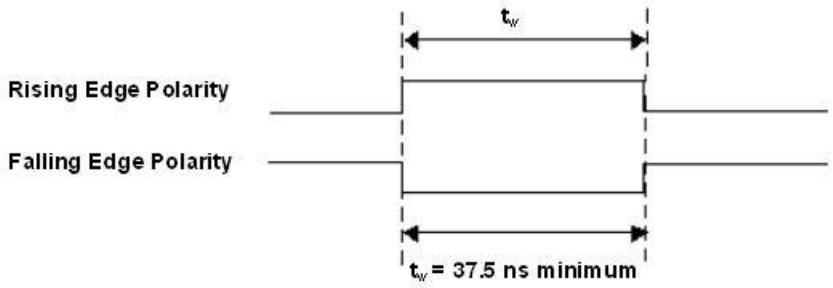


Figure 7. A/D START TRIGGER input signal timing

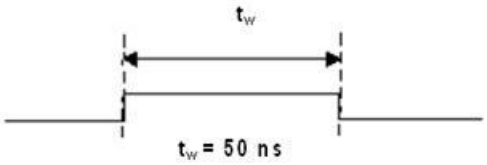


Figure 8. A/D START TRIGGER output signal timing

Use the A/D START TRIGGER signal to initiate pre-triggered DAQ operations (when you need to acquire data just before a trigger event). In most pre-triggered applications, the A/D START TRIGGER signal is generated by a software trigger. The use of A/D START TRIGGER and A/D STOP TRIGGER in pre-triggered DAQ applications is explained next.

A/D STOP TRIGGER signal

Pre-triggered data acquisition continually acquires data into a circular buffer until a specified number of samples have been collected after the trigger event. Figure 9 illustrates a typical pre-triggered DAQ sequence.

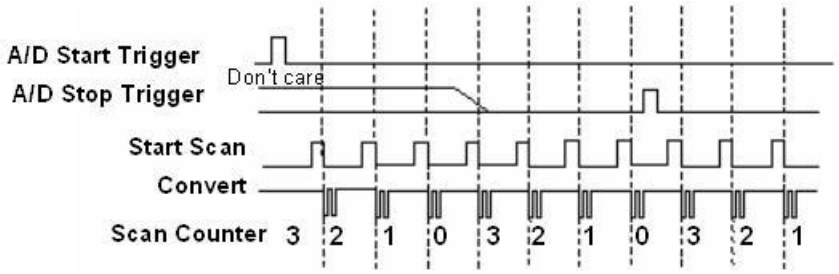


Figure 9. Pre-triggered data acquisition example

The A/D STOP TRIGGER signal signifies when the circular buffer should stop and when the specified number of post trigger samples should be acquired. It is available as an output and an input. By default, it is available at AUXIN2 as an input but may be programmed for access at any of the AUXIN pins or the DAQ-Sync "DS A/D STOP TRIGGER" input. It may be programmed for access at any of the AUXOUT pins as an output.

When using the A/D STOP TRIGGER signal as an input, the polarity may be configured for either rising or falling edge. The selected edge of the A/D STOP TRIGGER signal initiates the post-triggered phase of a pre-triggered acquisition sequence.

As an output, the A/D STOP TRIGGER signal indicates the event separating the pre-trigger data from the post-trigger data. The output is an active high pulse with a pulse width of 50 ns. Figure 10 and Figure 11 show the input and output timing requirements for the A/D STOP TRIGGER signal.

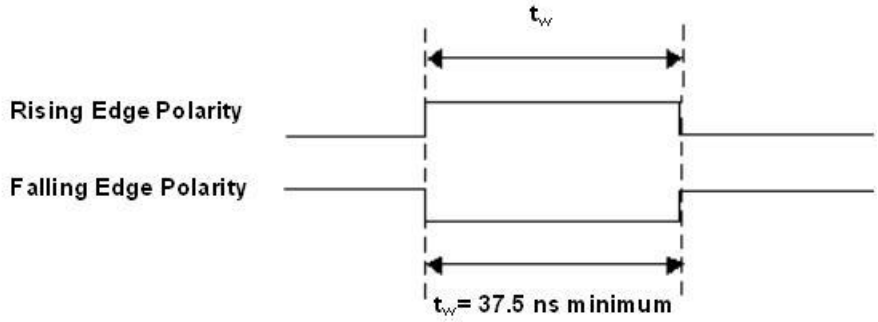


Figure 10. A/D STOP TRIGGER input signal timing

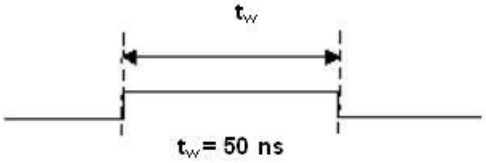


Figure 11. A/D STOP TRIGGER output signal timing

STARTSCAN signal

The STARTSCAN output signal indicates when a scan of channels has been initiated. You can program this signal to be available at any of the AUXOUT pins. The STARTSCAN output signal is a 50 ns wide pulse the leading edge of which indicates the start of a channel scan. Figure 12 shows the timing for the STARTSCAN signal.

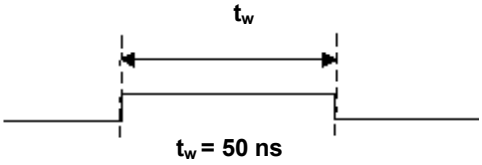


Figure 12. STARTSCAN Start of Scan timing

SSH signal

You can use the SSH signal as a control signal for external sample/hold circuits. The SSH signal is a programmable polarity pulse that is asserted throughout a channel scan. The state of this signal changes after the start of the last conversion in the scan. The SSH signal may be routed via software selection to any of the AUXOUT pins. Figure 13 shows the timing for the SSH signal.

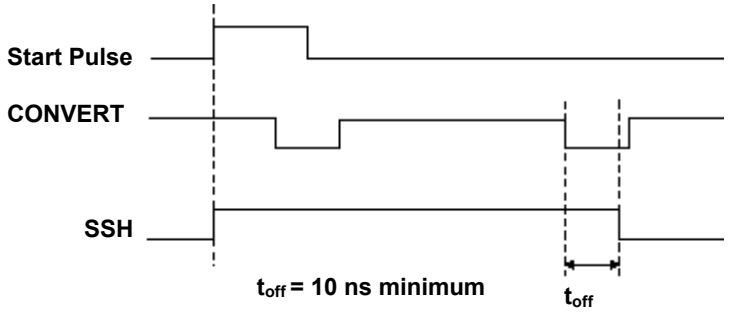


Figure 13. SSH signal timing

A/D CONVERT signal

The A/D CONVERT signal indicates the start of an A/D conversion. It is available through software selection as an input to any of the AUXIN pins (defaulting to AUXIN0) or the DAQ-Sync DS A/D CONVERT input and as an output to any of the AUXOUT pins.

When used as an input, the polarity is software selectable. The A/D CONVERT signal starts an acquisition on the selected edge. The selected edge (either rising of falling) of the convert pulses must be separated by a minimum of 10 μs to remain within the 100 kS/s conversion rate specification.

Refer to Figure 6 and Figure 9 for the relationship of A/D CONVERT to the DAQ sequence. Figure 14 and Figure 15 show the input and output pulse width requirements for the A/D CONVERT signal.

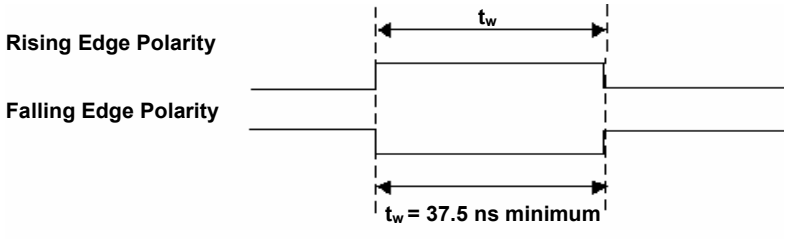


Figure 14. A/D CONVERT signal input timing requirement

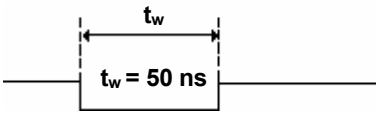


Figure 15. A/D CONVERT signal output timing requirement

The A/D CONVERT signal is generated by the on-board pacer circuit unless the external clock option is in use. This signal may be gated by hardware (A/D PACER GATE) or software.

A/D PACER GATE signal

Use the A/D PACER GATE signal to disable scans temporarily. You can program this signal for input at any of the AUXIN pins.

If the A/D PACER GATE signal is active, no scans can occur. If the A/D PACER GATE signal becomes active during a scan in progress, the current scan is completed and scans are then held off until the gate is de-asserted.

A/D EXTERNAL TIME BASE signal

The A/D EXTERNAL TIME BASE signal can serve as the source for the on-board pacer circuit rather than using the 40 MHz internal time base. Any AUXIN pin can be set programmatically as the source for this signal. The polarity is programmable.

The maximum frequency for the A/D EXTERNAL TIME BASE signal is 20 MHz. The minimum pulse width is 23 ns high or low. There is no minimum frequency specification.

Figure 16 shows the timing specifications for the A/D EXTERNAL TIME BASE signal.

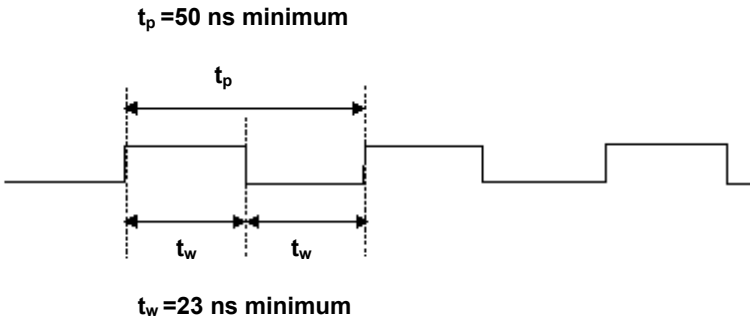


Figure 16. A/D EXTERNAL TIME BASE signal timing

A/D STOP signal

The A/D STOP signal indicates a completed acquisition sequence. You can program this signal to be available at any of the AUXOUT pins. The A/D STOP output signal is a 50 ns wide pulse whose leading edge indicates a DAQ done condition. Figure 17 shows the timing for the A/D STOP signal.

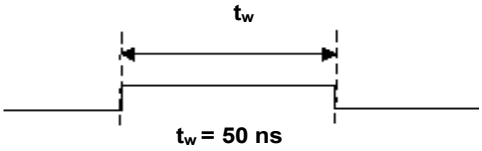


Figure 17. A/D STOP signal timing

ATRIG signal

In addition to standard digital trigger features, the PCI-DAS6031 and PCI-DAS6033 also provide analog triggering capability. When using the analog trigger, acquisitions may be started and controlled via an analog signal. There are four trigger/gate modes available using the analog trigger feature:

- Trigger – positive or negative slope
- Gate – above reference or below reference
- Hysteresis – positive or negative hysteresis
- Window – inside or outside window

The trigger mode is used to start an acquisition sequence. The remaining modes provide gating functions during an acquisition sequence which start and stop the acquisition based on the gate condition.

There are two possible inputs for the analog trigger source (see Figure 18). The first is the AUXIN0/ATRIG pin on the 100-pin I/O connector. This is a software selectable dual-purpose pin that supports either digital or analog trigger inputs. The source selection defaults to analog trigger on power-up and may be modified at any time using *Insta*Cal. The input range on the ATRIG pin is always ±10 V. 12-bit DACs are used to set the HI and LO levels for the threshold(s). The threshold resolution in this mode is 4.88 mV per step.

Caution! Remove all analog inputs before configuring this pin as a digital input. Any voltage levels above ±15 V in this configuration may cause damage to the product!

The second possible analog trigger source is the post-gain version of any one of the 64 analog inputs. In this mode, the voltage present on the first channel in the scan may be used to initiate the acquisition sequence.

Since the input to the analog trigger circuit has been scaled by the selected range, the effective resolution of the thresholds is equal to the A/D's full-scale-range (±2.5 V) divided by 4096. For example, the ±2.5 V range allows for 5 V/4096, or 1.2 mV of threshold resolution.

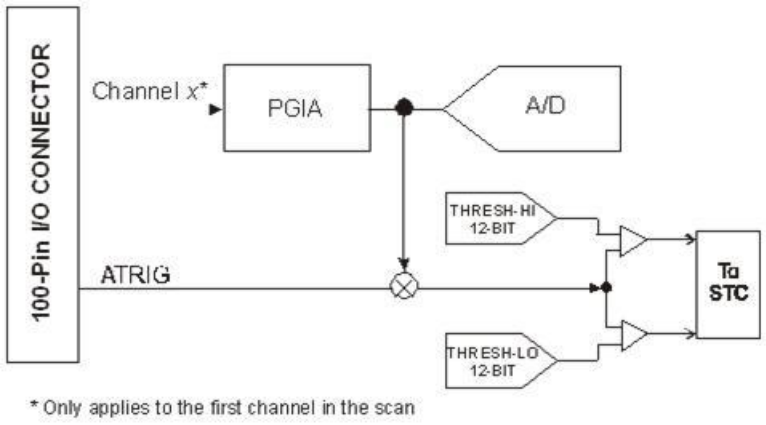


Figure 18. ATRIG circuit

The next section includes a detailed description of each mode of operation. In each case, a ±2 V triangle waveform is used as the ATRIG input source. The THRESH_HI is set to 1.0 V and the THRESH_LO signal is set to -1.0 V.

In the following analog trigger signal diagrams, the **bold** portion of the waveform indicates the data acquired for the given ATRIG mode.

Trigger Above

The acquisition will begin when the ATRIG signal first goes above the THRESH_HI. This mode is non-retriggerable.

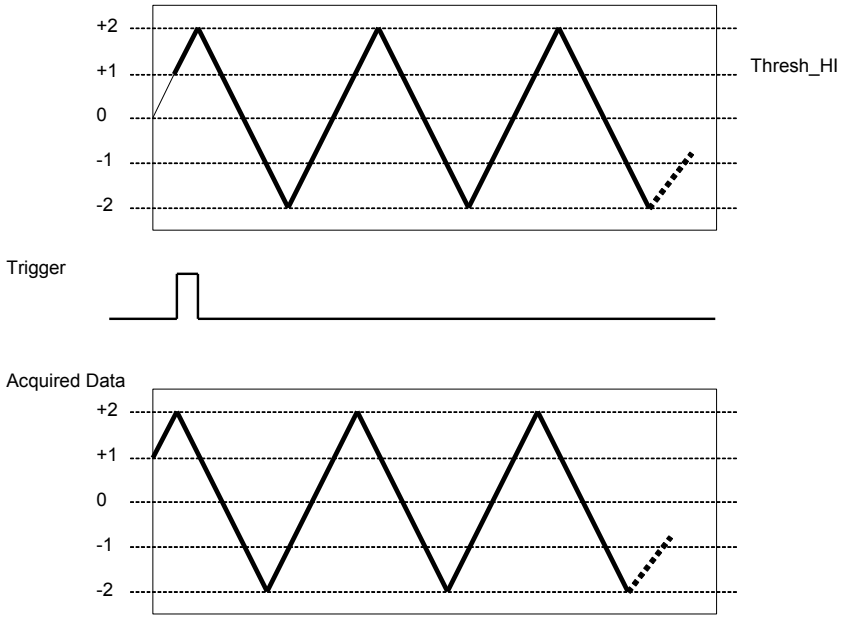


Figure 19. Trigger positive slope

Trigger Below

The acquisition will begin when ATRIG signal first goes below the THRESH_LO level. This mode is non-retriggerable.

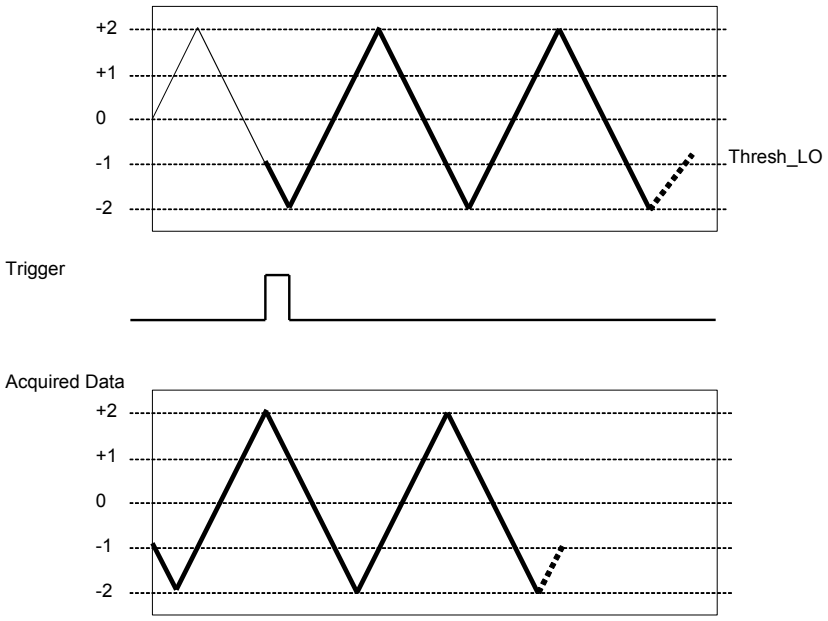


Figure 20. Trigger negative slope

Gate Above

Data acquisition is enabled whenever ATRIG goes above the THRESH_HI level. Acquisition is suspended whenever the ATRIG signal goes below the THRESH_HI level. This is a level-sensitive gating mode.

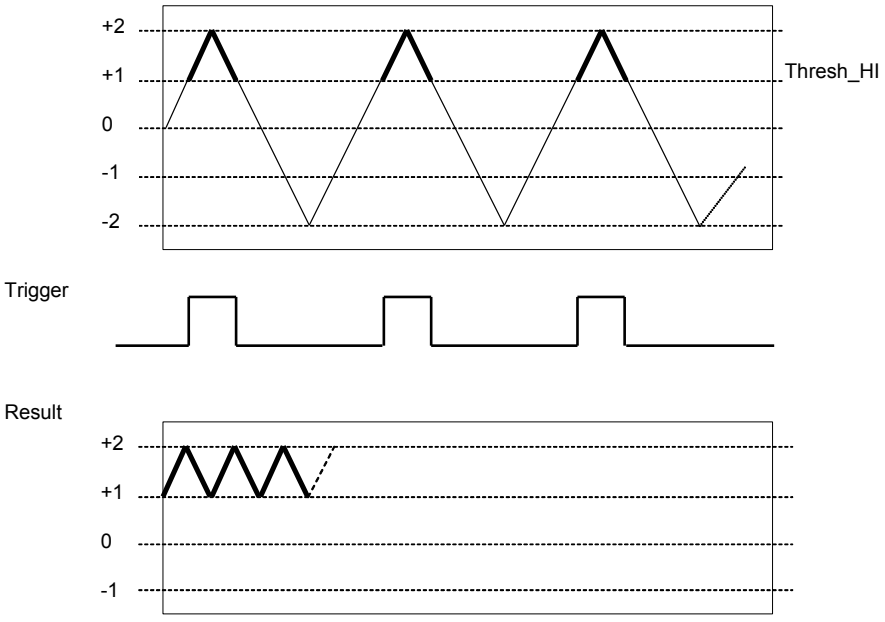


Figure 21. Gate Above

Gate Below

Data acquisition is enabled whenever ATRIG goes below the THRESH_LO level. Acquisition is suspended whenever the ATRIG signal goes above the THRESH_LO level. This is a level-sensitive gating mode.

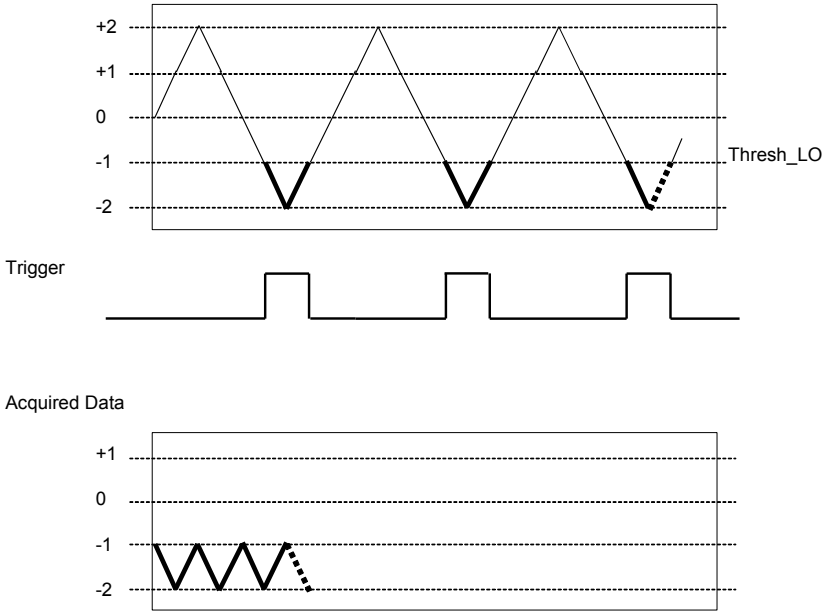


Figure 22. Gate Below

Gate Negative Hysteresis

Data acquisition is enabled whenever ATRIG goes above the THRESH_HI level. Acquisition is suspended whenever the ATRIG signal goes below the THRESH_LO level. The hysteresis level is set by THRESH_LO. This is a level-sensitive gating mode.

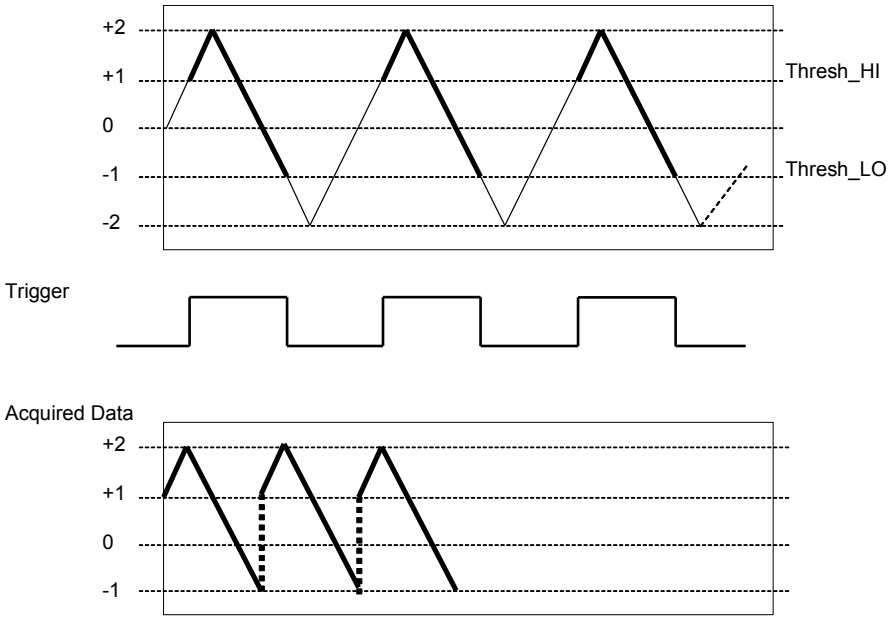


Figure 23. Gate Negative Hysteresis

Gate Positive Hysteresis

Data acquisition is enabled whenever ATRIG goes below the THRESH_LO level. Acquisition is suspended whenever the ATRIG signal goes above the THRESH_HI level. The hysteresis level is set by THRESH_HI. This is a level-sensitive gating mode.

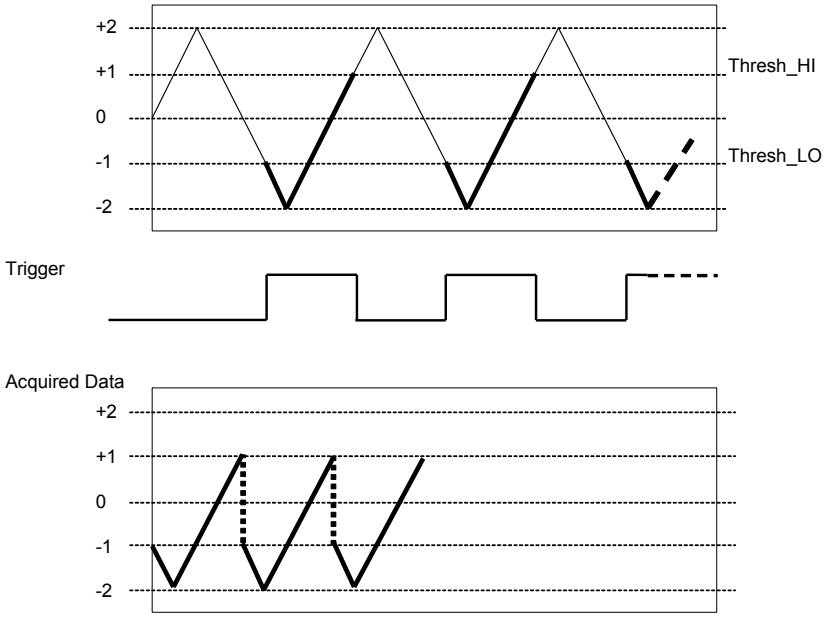


Figure 24. Gate Positive Hysteresis

Gate Inside Window

Data acquisition is enabled whenever ATRIG is below the THRESH_HI level and above the THRESH_LO level. Acquisition is suspended whenever the ATRIG signal is outside of this region. This is a level-sensitive gating mode

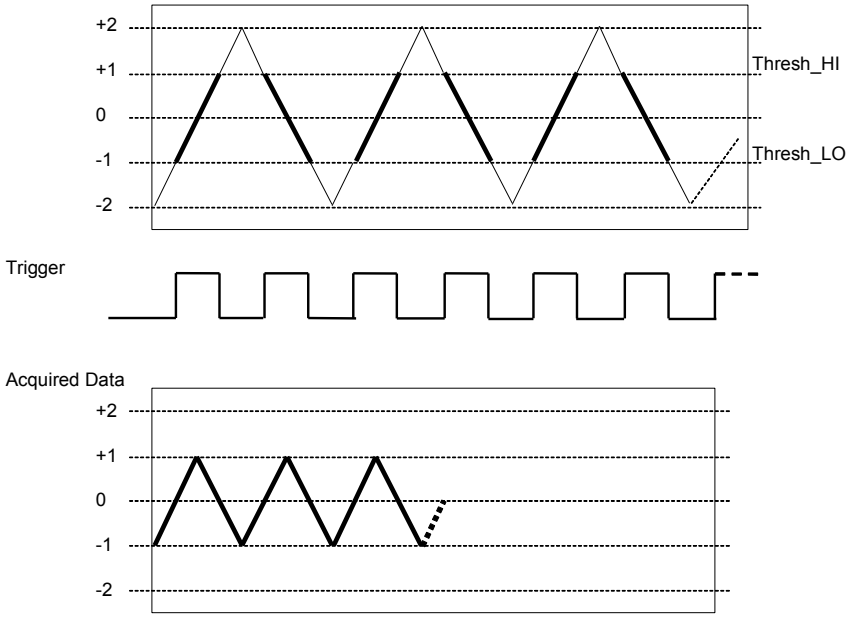


Figure 25. Gate Inside Window

Gate Outside Window

Data acquisition is enabled whenever ATRIG is above the THRESH_HI level or below the THRESH_LO level. Acquisition is suspended whenever the ATRIG signal is between the THRESH_HI and THRESH_LO levels. This is a level-sensitive gating mode

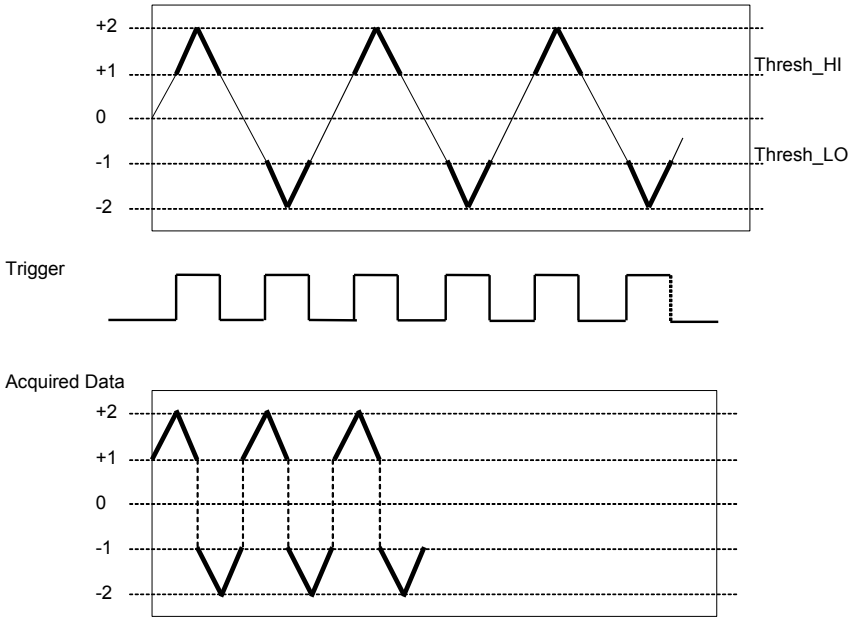


Figure 26. Gate Outside Window

Waveform generation timing signals

The signals that control the timing for the analog output functions on the PCI-DAS6031 are listed below.

- D/A START TRIGGER
- D/A UPDATE
- D/A EXTERNAL TIME BASE

D/A START TRIGGER signal

The D/A START TRIGGER signal is used to hold off output scans until after a trigger event. The DAQ-Sync "DS D/A START TRIGGER" input or any AUXIN pin can be programmed to serve as the D/A START TRIGGER signal. It is also available as an output on any AUXOUT pin.

When used as an input, the D/A START TRIGGER signal may be software selected as either a positive or negative edge trigger. The selected edge of the D/A START TRIGGER signal causes the DACs to start generating the output waveform.

The D/A START TRIGGER signal can be used as an output to monitor the trigger that initiates waveform generation. The output is an active-high pulse having a width of 50 ns.

Figure 27 and Figure 28 show the input and output timing requirements for the D/A START TRIGGER signal.

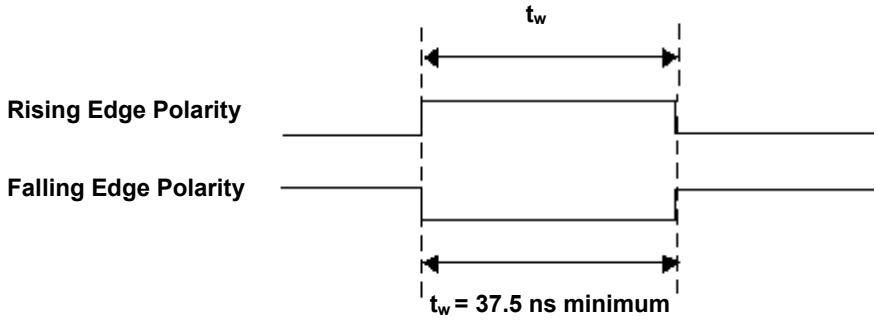


Figure 27. D/A START TRIGGER input signal timing

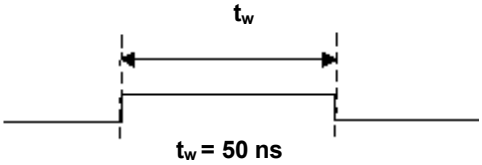


Figure 28. D/A START TRIGGER output signal timing

D/A CONVERT signal

The D/A CONVERT signal causes a single output update on the D/A converters. You can program the DAQ-Sync DS D/A UPDATE input or any AUXIN pin to accept the D/A CONVERT signal. It is also available as an output on any AUXOUT pin.

The D/A CONVERT input signal polarity is software selectable. DAC outputs update within 100ns of the selected edge. The D/A CONVERT pulses should be no less than 100 µs apart.

When used as an output, the D/A CONVERT signal may be used to monitor the pacing of the output updates. The output has a pulse width of 225 ns with selectable polarity.

Figure 29 and [illegible] signal.

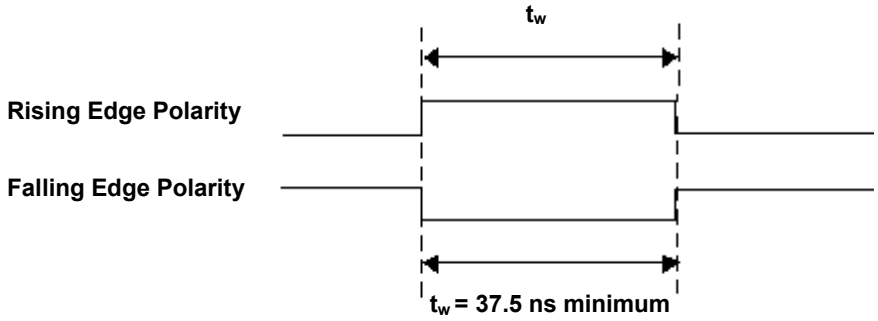


Figure 29. D/A CONVERT input signal timing

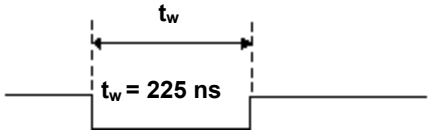


Figure 30. D/A CONVERT output signal timing

D/A EXTERNAL TIME BASE signal

The D/A EXTERNAL TIME BASE signal can serve as the source for the on-board DAC pacer circuit rather than using the internal time base. Any AUXIN pin can be set programmatically as the source for this signal. The polarity is programmable.

The maximum frequency for the D/A EXTERNAL TIME BASE signal is 20 MHz. The minimum pulse width is 23 ns high or low. There is no minimum frequency specification.

Figure 31 shows the timing requirements for the D/A EXTERNAL TIME BASE signal.

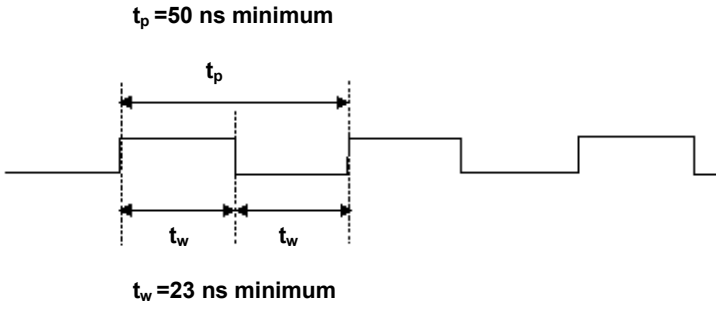


Figure 31. D/A EXTERNAL TIME BASE signal timing

General-purpose counter signal timing

The general-purpose counter signals are:

- CTR1 CLK
- CTR1 GATE
- CTR1 OUT
- CTR2 CLK
- CTR2 GATE
- CTR2 OUT

CTR1 CLK signal

The CTR1 CLK signal can serve as the clock source for independent user counter 1. It can be selected through software at the CTR1 CLK pin rather than using the on-board 10 MHz or 100 kHz sources. It is also polarity programmable. The maximum input frequency is 10 MHz. There is no minimum frequency specified. Figure 32 shows the timing requirements for the CTR1 CLK signal.

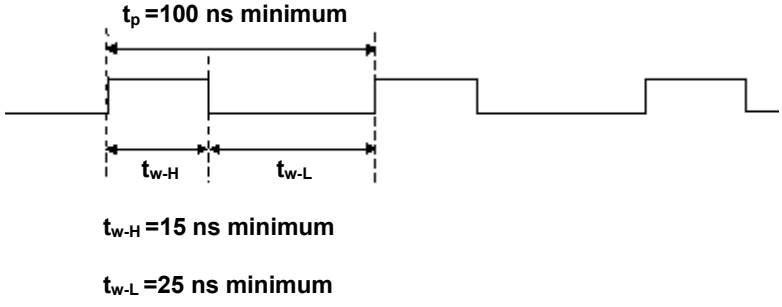


Figure 32. CTR1 CLK signal timing

CTR1 GATE signal

You can use the CTR1 GATE signal for starting and stopping the counter, saving counter contents, etc. It is polarity programmable and is available at the CTR1 GATE pin.

Figure 33 shows the minimum timing requirements for the CTR1 GATE signal.

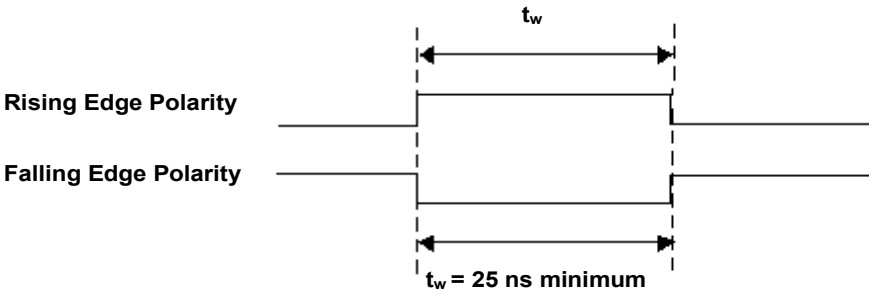


Figure 33. CTR1 GATE signal timing

CTR1 OUT signal

This signal is present on the CTR1 OUT pin. The CTR1 OUT signal is the output of one of the two user's counters in an industry-standard 82C54 chip. For detailed information on counter operations, please refer to the 82C54 data sheet on our web site at www.mccdaq.com/PDFmanuals/82C54.pdf. Figure 34 shows the timing requirements for the CTR1 OUT signal for counter mode 0 and mode 2.

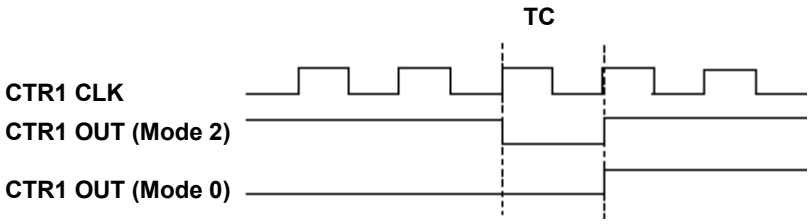
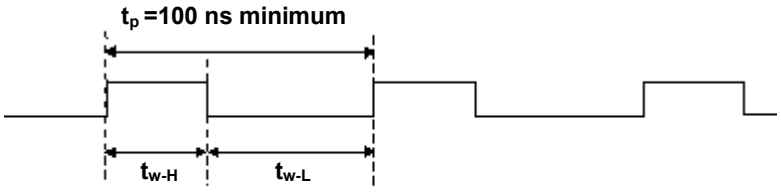


Figure 34. CTR1 OUT signal timing

CTR2 CLK signal

The CTR2 CLK signal can serve as the clock source for independent user counter 2. It can be selected through software at the CTR2 CLK pin rather than using the on-board 10 MHz or 100 kHz sources. It is also polarity programmable. The maximum input frequency is 10 MHz. There is no minimum frequency specified. Figure 35 shows the timing requirements for the CTR2 CLK signal.



t_{w-H} =15 ns minimum

t_{w-L} =25 ns minimum

Figure 35. CTR2 CLK signal timing

CTR2 GATE signal

You can use the CTR2 GATE signal for starting and stopping the counter, saving counter contents, etc. It is polarity programmable and is available at the CTR2 GATE pin. Figure 36 shows the timing requirements for the CTR2 GATE signal.

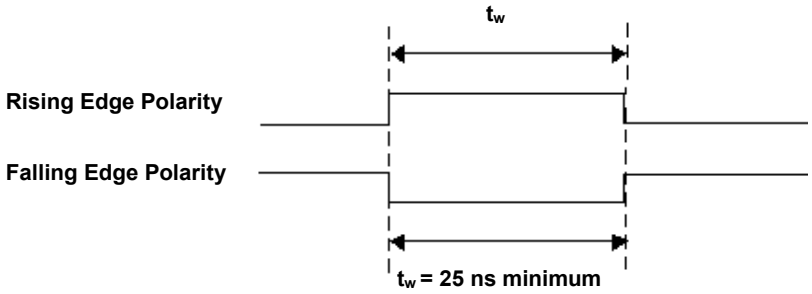


Figure 36. CTR2 GATE signal timing

CTR2 OUT signal

This signal is present on the CTR2 OUT pin. The CTR2 OUT signal is the output of one of the two user's counters in an industry-standard 82C54 chip.

For detailed information on counter operations, please refer to the data sheet on our web site at www.measurementcomputing.com/PDFmanuals/82C54.pdf.

Figure 37 shows the timing of the CTR1 OUT signal for mode 0 and for mode 2.

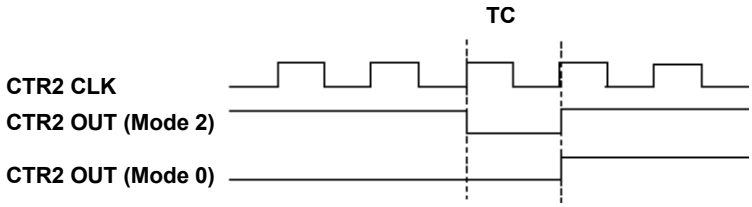


Figure 37. CTR2 OUT signal timing

Calibrating the PCI-DAS6031 and PCI-DAS6033

Introduction

You should calibrate the board (using the InstaCal utility) after the board has fully warmed up. The recommended warm-up time is 15 minutes. For best results, calibrate the board immediately before making critical measurements. The high resolution analog components on the board are somewhat sensitive to temperature. Pre-measurement calibration ensures that your board is operating at optimum calibration values.

Calibration theory

Analog inputs are calibrated for offset and gain. Offset calibration for the analog inputs is performed directly on the input amplifier (PGIA) with coarse and fine trim DACs acting on the amplifier.

For input gain calibration, a precision calibration reference is used with coarse and fine trim DACs acting on the ADC (see Figure 38).

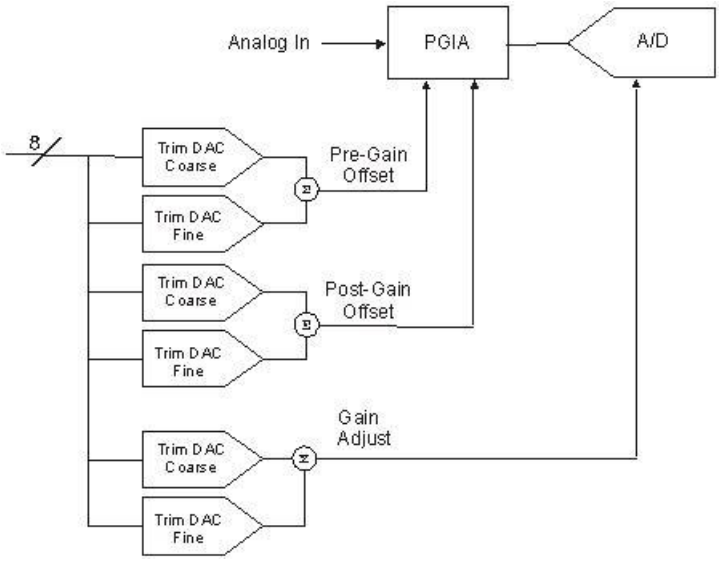


Figure 38. Analog input calibration - basic elements

A similar method is used to calibrate the analog output components. A trim DAC is used to adjust the gain of the DAC. A separate DAC is used to adjust offset on the final output amplifier. The calibration circuits are duplicated for both analog outputs (see Figure 39).

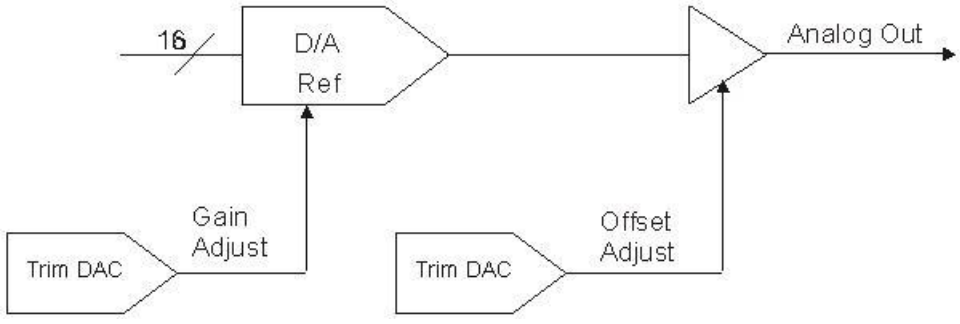


Figure 39. Analog output calibration – basic elements

Specifications

All specifications are subject to change without notice.
Typical for 25 °C unless otherwise specified.
Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

Parameter	Specification
A/D converter	Successive Approximation type
Resolution	16-its, 1 in 65536
Maximum sample rate	100 kS/s
Number of channels	64 single-ended / 32 differential; software-selectable
Input ranges	Bipolar: ±10 V, ±5 V, ±2 V, ±1 V, ±0.5 V, ±0.2 V, ±0.1 V Unipolar: 0 to 10 V, 0 to 5 V, 0 to 2 V, 0 to 1 V, 0 to 0.5 V, 0 to 0.2 V, 0 to 0.1 V Software-selectable
A/D pacing	Internal counter – ASIC. Software-selectable time base: ▪ Internal 40 MHz, 50 ppm stability ▪ External source via AUXIN<5:0>; software-selectable.
	External convert strobe: A/D CONVERT
	Software paced
Burst mode	Software-selectable option; burst rate = 10 µS
A/D gate sources	External digital: A/D GATE
	External analog: ATRIG input CH0 IN through CH63 IN
A/D gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Refer to the Analog Trigger section on page 39
A/D trigger sources	External digital: A/D START TRIGGER A/D STOP TRIGGER
	External analog: ATRIG input CH0 IN through CH63 IN
A/D triggering modes	External digital: Software-configurable for rising or falling edge
	External analog: Refer to the Analog Trigger section on page 39
	Pre-/Post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples
ADC pacer out	Available at user connector: A/D PACER OUT
RAM buffer size	8 K samples
Data transfer	DMA
	Programmed I/O
DMA modes	Demand or non-demand using scatter-gather
Configuration memory	Up to 8 k elements. Programmable channel, gain, and offset
Streaming-to-disk rate	100 kS/s, system dependent

Accuracy

100 kS/s sampling rate, single channel operation and a 15-minute warm-up. Accuracies listed are for measurements made following an internal calibration. They are valid for operational temperatures within ±1°C of internal calibration temperature and ±10°C of factory calibration temperature. Calibrator test source high side tied to Channel 0 High and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 2. Absolute Accuracy

Range	Absolute Accuracy
±10 V	±3.76 LSB
±5 V	±13.61 LSB
±2 V	±13.70 LSB
±1 V	±13.83 LSB
±500 mV	±14.09 LSB
±200 mV	±16.71 LSB
±100 mV	±19.99 LSB
0 V to 10 V	±6.40 LSB
0 V to 5 V	±26.11 LSB
0 V to 2 V	±26.28 LSB
0 V to 1 V	±26.54 LSB
0 mV to 500 mV	±27.13 LSB
0 mV to 200 mV	±32.11 LSB
0 mV to 100 mV	±38.67 LSB

Table 3. Absolute Accuracy Components – All values are (±)

Range	% of Reading	Offset (µV)	Noise +Quantization (µV)		Temp Drift (%/ºC)	Absolute Accuracy at FS (mV)
			Single Pt	Averaged (Note 1)		
±10 V	0.0061	479.2	634.1	54.9	0.0001	1.147
±5 V	0.0361	243.6	317.1	27.5	0.0006	2.077
±2 V	0.0361	102.2	126.8	11.0	0.0006	0.836
±1 V	0.0361	55.1	63.4	5.5	0.0006	0.422
±500 mV	0.0361	31.6	36.8	3.2	0.0006	0.215
±200 mV	0.0411	17.4	22.5	2.0	0.0006	0.102
±100 mV	0.0461	12.7	19.6	1.8	0.0006	0.061
0 V to 10 V	0.0061	326.6	417.8	36.6	0.0001	0.976
0 V to 5 V	0.0361	167.3	208.9	18.3	0.0006	1.992
0 V to 2 V	0.0361	71.7	83.6	7.3	0.0006	0.802
0 V to 1 V	0.0361	39.9	41.8	3.7	0.0006	0.405
0 mV to 500 mV	0.0361	23.9	28.1	2.5	0.0006	0.207
0 mV to 200 mV	0.0411	14.4	19.6	1.8	0.0006	0.098
0 mV to 100 mV	0.0461	11.2	18.1	1.7	0.0006	0.059

Note 1: Averaged measurements assume averaging of 100 single-channel readings.
Each PCI-DAS6031 and PCI-DAS6033 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 2.

Table 4. Relative Accuracy specifications – All values are (±)

Range	Relative Accuracy (µV)	
	Single Point	**Averaged (Note 2)**
±10 V	723.3	72.3
±5 V	361.6	36.2
±2 V	144.7	14.5
±1 V	72.3	7.2
±500 mV	42.2	4.2
±200 mV	26.5	2.7
±100 mV	24.1	2.4
0 to 10 V	482.2	48.2
0 to 5 V	241.1	24.1
0 to 2 V	96.4	9.6
0 to 1 V	48.2	4.8
0 to 500 mV	33.1	3.3
0 to 200 mV	24.1	2.4
0 to 100 mV	22.9	2.3

Note 2: Averaged measurements assume averaging of 100 single-channel readings.
Relative accuracy is the measured deviation from a straight line drawn between measured endpoints of the transfer function. ADC resolution, noise and front-end non-linearity are included in this measurement.

Table 5. Differential non-linearity

All ranges	±0.5 LSB typ	±1.0 LSB max

Settling time

Settling time is the time required for a channel to settle to within a specified accuracy in response to a full-scale (FS) step. Two channels are scanned at the specified rate. A –FS DC signal is presented to Channel 1; a +FS DC signal is presented to Channel 0.

Table 6. Settling time specifications

Condition	Range	±0.00076% (±0.5 LSB)	±0.0015% (±1 LSB)	±0.0061% (±4 LSB)	±0.012% (±8 LSB)
Same range to same range	±10 V	50 µS max	25 µS max	10 µS max	5 µS typ
	±5 V	50 µS max	25 µS max	10 µS max	5 µS typ
	±2 V	50 µS max	25 µS max	10 µS max	5 µS typ
	±1 V	50 µS max	25 µS max	10 µS max	5 µS typ
	±500 mV	50 µS max	25 µS max	10 µS max	5 µS typ
	±200 mV	50 µS max	25 µS max	10 µS max	5 µS typ
	±100 mV	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 10 V	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 5 V	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 2 V	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 1 V	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 500 mV	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 200 mV	50 µS max	25 µS max	10 µS max	5 µS typ
	0 to 100 mV	50 µS max	25 µS max	10 µS max	5 µS typ

Parametrics

Table 7. Parametric specifications

Parameter	Specification
Max working voltage (signal + common-mode)	±11 V
CMRR @ 60 Hz	±10 V range and 0 to 10 V: 92 dB
	±5 V range and 0 to 5 V: 97 dB
	±2 V range and 0 to 2 V: 101 dB
	±1 V range and 0 to 1 V: 104 dB
	±0.5 V range and 0 to 0.5 V: 105 dB
	±0.2 V range and 0 to 0.2 V: 105 dB
	±0.1 V range and 0 to 0.1 V: 105 dB
Small signal bandwidth, all ranges	*255 kHz*
Input coupling	*DC*
Input impedance	*100 GΩ in normal operation*
Input bias current	*±200 pA*
Input offset current	*±100 pA*
Absolute maximum input voltage	*Power ON: ±25 V, Power OFF: ±15 V (±20 mA Note 3)* *Protected inputs:* ▪ *CH<63:0> IN* ▪ *AISENSE*
Power on and reset state	CH0 IN, single-ended mode, 0 V to 0.1 V input range (Note 4)
Crosstalk	Adjacent channels: –75 dB
	All other channels: –90 dB

Note 3: The analog input sink/source current must be limited to an maximum of ±20 mA in the power OFF state to prevent damage to the board. A 1000 Ω (¼ W) current limiting resistor should be placed in series with each analog input channel being used in applications where the power OFF state sink/source current into the board can exceed ±20 mA. Resistance values >1000 Ω may adversely affect the noise and settling time performance of the board.

Note 4: Care should be taken to avoid the application of an input voltage to CH0 IN that could overdrive the analog input circuit. Any unused analog input channel should be connected to LLGND.

Noise performance

Table 8 summarizes the noise performance for the PCI-DAS6031 and PCI-DAS6033. Noise distribution is determined by gathering 50 k samples with inputs tied to ground at the user connector. Samples are gathered 100 kS/s sampling rate. The specification applies to both single-ended and differential modes of operation.

Table 8. Analog input noise performance specifications

Range	LSBrms	Typical Counts
±10 V	0.6	8
±5 V	0.6	8
±2 V	0.6	8
±1 V	0.6	8
±500 mV	0.7	8
±200 mV	1.1	11
±100 mV	2.0	17
0 V to 10 V	0.8	8
0 V to 5 V	0.8	8
0 V to 2 V	0.8	8
0 V to 1 V	0.8	8
0 mV to 500 mV	1.1	11
0 mV to 200 mV	2.0	17
0 mV to 100 mV	3.8	25

Analog output (PCI-DAS6031 only)

Table 9. PCI-DAS6031 analog output specifications

Parameter	Specification
D/A converter type	Double-buffered, multiplying
Resolution	16-bits, 1 in 65,536
Number of channels	2 voltage output
Voltage range	±10 V, 0 to 10 V, software-selectable
Monotonicity	*16-bits, guaranteed*
Slew rate	5 V/µs typ
Settling time (full scale step)	10 µs max to ±1 LSB
Noise	60 µVrms, DC to 1 MHz BW
Current drive	±5 mA
Output short-circuit duration	*Indefinite @ 25 mA*
Output coupling	*DC*
Output impedance	0.1 Ω max
Power up and reset	DACs cleared to 0 volts ±20 mV max

Table 10. Analog output absolute accuracy specifications

Range	Absolute Accuracy
±10 V	±4.7 LSB
0 to 10 V	±7.9 LSB

Table 11. Absolute accuracy components - All values are (±)

Range	% of Reading	Offset (µV)	Temp Drift (%/ºC)	Absolute Accuracy at FS (mV)
±10 V	0.0062	813	0.0001	1.430
0 to 10 V	0.0062	584	0.0001	1.201

Each PCI-DAS6031 is tested at the factory to assure that the board overall error does not exceed the values specified in Table 10.

Table 12. Relative accuracy specifications

Range	Relative Accuracy	
All ranges	±0.5 LSB, typ	±1.0 LSB, max

Relative accuracy is defined as the measured deviation from a straight line drawn between measured endpoints of the transfer function.

Analog output pacing and triggering

Table 13. Analog output pacing and triggering specifications

Parameter	Specification
DAC pacing (software programmable)	Internal counter – ASIC. Selectable time base: ▪ Internal 40 MHz, 50 ppm stability. ▪ External Source via AUXIN<5:0>, SW selectable.
	External convert strobe: D/A UPDATE
	Software paced
DAC gate sources (software programmable)	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH63 IN
	Software gated
DAC gating modes	External digital: Programmable, active high or active low, level or edge
	External analog: Refer to the Analog Trigger section on page 39
DAC trigger sources	External digital: D/A START TRIGGER
	External analog: ATRIG input CH0 IN through CH63 IN
	Software triggered
DAC triggering modes	External digital: Software-configurable for rising or falling edge.
	External analog: Software-configurable for positive or negative slope.
DAC pacer Out	Available at user connector D/A PACER OUT
RAM buffer Size	16 K samples
Data transfer	DMA
	Programmed I/O
	Update DACs individually or simultaneously; software-selectable.
DMA modes	Demand or non-demand using scatter gather.
Waveform generation throughput	100 kS/s max per channel, 2 channels simultaneous

Analog trigger

Table 14. Analog trigger specifications

Parameter	Specification	
Analog trigger sources Software-selectable	External: ATRIG input CH0 IN through CH63 IN, first channel in scan	
Analog trigger levels	ATRIG input: ±10 V	
	CH0 IN through CH63 IN: Full-scale, range dependent	
Analog trigger modes	External analog: Software-configurable for: ▪ Positive or negative slope	
Analog gate modes	External analog: Software-configurable for: ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window	
Resolution	12-bits, 1 in 4,096	
Accuracy	±1% of full-scale range max	
Bandwidth (-3 dB)	ATRIG input	4 MHz
	CH0 IN through CH63 IN	255 kHz

Analog input / output calibration

Table 15. Analog I/O calibration specifications

Parameter	Specification
Recommended warm-up time	15 minutes
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Onboard calibration reference	*DC Level: 5.000 V± 1 mV. Actual measured values stored in EEPROM.*
	Tempco: 0.6 ppm/°C max
	Long-term stability: ±6 ppm/sqrt (1000 hrs)
Calibration interval	1 year

Digital input/output

Table 16. Digital I/O specifications

Parameter	Specification
Digital type	Discrete, 5 V/TTL compatible
Number of I/O	8
Configuration	8-bits, independently programmable for input or output. All pins pulled up to +5 V via 47 k resistors (default). Positions available for pull-down to ground. Hardware selectable via zero Ohm resistors.
Input high voltage	2.0 V min, 7.0 V absolute max
Input low voltage	0.8 V max, –0.5 V absolute min
Output high voltage (IOH = -32 mA)	3.80 V min, 4.20 V typ
Output low voltage (IOL = 32 mA)	0.55 V max, 0.22 V typ
Data transfer	Programmed I/O
Power-up / reset state	Input mode (high impedance)

Interrupts

Table 17. Interrupt specifications

Parameter	Specification	
Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time	
Interrupt enable	Programmable through PLX9080	
ADC Interrupt sources (software programmable)	DAQ_ACTIVE:	Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP:	Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE:	Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL:	Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE:	Interrupt is generated after each conversion completes.
	DAQ_EOSCAN:	Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ:	Interrupt is generated after each interval delay during multi-channel scans.
DAC Interrupt sources (software programmable)	DAC_ACTIVE:	Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE:	Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY:	Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL:	Interrupt is generated when the DAC high channel output is updated.

Counters

Table 18. Counter specifications

Parameter	Specification
User counter type	82C54
Number of channels	2
Resolution	16-bits
Compatibility	5 V/TTL
CTRn base clock source	Software-selectable: ▪ Internal 10 MHz ▪ Internal 100 kHz ▪ External connector (CTRn CLK)
Internal 10 MHz clock source stability	50 ppm
Counter n gate	Available at connector (CTRn GATE)
Counter n output	Available at connector (CTRn OUT)
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*15 ns min*
Low pulse width (clock input)	*25 ns min*
Gate width high	*25 ns min*
Gate width low	*25 ns min*
Input low voltage	*0.8 V max*
Input high voltage	*2.0V min*
Output low voltage	*0.4V max*
Output high voltage	*3.0V min*

Configurable AUXIN<5:0>, AUXOUT<2:0> external trigger/clocks

The PCI-DAS6031 and PCI-DAS6033 provide nine user-configurable trigger/clock pins available at the 100-pin I/O connector. Of these, six are configurable as inputs, while three are configurable as outputs.

Table 19. Configurable triggers/clocks specifications

Parameter	Specification	
AUXIN<5:0> sources (Software-selectable)	A/D CONVERT:	External ADC convert strobe
	A/D TIMEBASE IN:	External ADC pacer time base
	A/D START TRIGGER:	ADC Start Trigger
	A/D STOP TRIGGER:	ADC Stop Trigger
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER:	DAC trigger/gate
	D/A UPDATE:	DAC update strobe
	D/A TIMEBASE IN:	External DAC pacer time base
AUXOUT<2:0> sources (Software-selectable)	STARTSCAN:	A pulse indicating start of conversion
	SSH:	Active signal that terminates at the start of the last conversion in a scan.
	A/D STOP:	Indicates end of scan
	A/D CONVERT:	ADC convert pulse
	SCANCLK:	Delayed version of ADC convert
	CTR1 CLK:	CTR1 clock source
	D/A UPDATE:	D/A update pulse
	CTR2 CLK:	CTR2 clock source
	A/D START TRIGGER:	ADC Start Trigger Out
	A/D STOP TRIGGER:	ADC Stop Trigger Out
	A/D PACER GATE:	External ADC gate
	D/A START TRIGGER:	DAC Start Trigger Out
Default selections	AUXIN0:	A/D CONVERT
	AUXIN1:	A/D START TRIGGER
	AUXIN2:	A/D STOP TRIGGER
	AUXIN3:	D/A UPDATE
	AUXIN4:	D/A START TRIGGER
	AUXIN5:	A/D GATE
	AUXOUT0:	D/A UPDATE
	AUXOUT1:	A/D CONVERT
	AUXOUT2:	SCANCLK
Compatibility	5 V/TTL	
Minimum pulse width	37.5 ns	

DAQ-Sync inter-board triggers/clocks

The DAQ-Sync bus provides inter-board triggering and synchronization capability. Five trigger/strobe I/O pins and one clock I/O pin are provided on a 14-pin header. The DAQ-Sync signals use dedicated pins. Only the direction may be set.

Table 20. DAQ-Sync signals

Parameter	Specification
DAQ-Sync signals:	DS A/D START TRIGGER
	DS A/D STOP TRIGGER
	DS A/D CONVERT
	DS D/A UPDATE
	DS D/A START TRIGGER
	SYNC CLK

Power consumption

Table 21. Power consumption specifications

Parameter	Specification
+5 V	PCI-DAS6031/32: 1.3 A typ, 1.5 A max Does not include power consumed through the I/O connector.
+5 V available at I/O connector	1 A max, protected with a resettable fuse

Environmental

Table 22. Environmental specifications

Parameter	Specification
Operating temperature range	0 °C to 55 °C
Storage temperature range	–20 to 70 °C
Humidity	0% to 90% non-condensing

Mechanical

Table 23. Mechanical Specifications

Parameter	Specification
Card dimensions (L × W × H)	PCI half card: 174.4 (6.87) × 106.9 (4.21) × 11.65 mm (0.46 in.)

DAQ-Sync connector and pinout

Table 24. DAQ-Sync connector specifications

Parameter	Specification
Connector type	14-pin right-angle 100 mil box header
Compatible cables	MCC p/n: CDS-14-x, 14-pin ribbon cable. x = number of boards (2 to 5)

Table 25. DAQ-Sync connector pinout

Pin	Signal Name
1	DS A/D START TRIGGER
2	GND
3	DS A/D STOP TRIGGER
4	GND
5	DS A/D CONVERT
6	GND
7	DS D/A UPDATE
8	GND
9	DS D/A START TRIGGER
10	GND
11	RESERVED
12	GND
13	SYNC CLK
14	GND

SCSI connector

Table 26. SCSI connector specifications

Parameter	Specification
Connector type	Shielded SCSI 100 D-type
Compatible cables	C100HD50-x, unshielded ribbon cable. x = 3 or 6 feet
	C100MMS-x, shielded round cable. x = 1, 2, or 3 meters
Compatible accessory products (with C100HD50-x cable)	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50
Compatible accessory products (with C100MMS-x cable)	SCB-100 BNC-16DI-FE

Table 27. 32-channel differential mode pinout

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	LLGND
2	CH0 IN HI	52	CH16 IN HI
3	CH0 IN LO	53	CH16 IN LO
4	CH1 IN HI	54	CH17 IN HI
5	CH1 IN LO	55	CH17 IN LO
6	CH2 IN HI	56	CH18 IN HI
7	CH2 IN LO	57	CH18 IN LO
8	CH3 IN HI	58	CH19 IN HI
9	CH3 IN LO	59	CH19 IN LO
10	CH4 IN HI	60	CH20 IN HI
11	CH4 IN LO	61	CH20 IN LO
12	CH5 IN HI	62	CH21 IN HI
13	CH5 IN LO	63	CH21 IN LO
14	CH6 IN HI	64	CH22 IN HI
15	CH6 IN LO	65	CH22 IN LO
16	CH7 IN HI	66	CH23 IN HI
17	CH7 IN LO	67	CH23 IN LO
18	LLGND	68	LLGND
19	CH8 IN HI	69	CH24 IN HI
20	CH8 IN LO	70	CH24 IN LO
21	CH9 IN HI	71	CH25 IN HI
22	CH9 IN LO	72	CH25 IN LO
23	CH10 IN HI	73	CH26 IN HI
24	CH10 IN LO	74	CH26 IN LO
25	CH11 IN HI	75	CH27 IN HI
26	CH11 IN LO	76	CH27 IN LO
27	CH12 IN HI	77	CH28 IN HI
28	CH12 IN LO	78	CH28 IN LO
29	CH13 IN HI	79	CH29 IN HI
30	CH13 IN LO	80	CH29 IN LO
31	CH14 IN HI	81	CH30 IN HI
32	CH14 IN LO	82	CH30 IN LO
33	CH15 IN HI	83	CH31 IN HI
34	CH15 IN LO	84	CH31 IN LO
35	AISENSE	85	DIO0
36	D/A OUT 0 *	86	DIO1
37	D/A GND	87	DIO2
38	D/A OUT1 *	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT / ATRIG	93	CTR1 CLK
44	N/C	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = N/C on PCI-DAS6033

Table 28. 64-channel single-ended mode pinout

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	LLGND
2	CH0 IN	52	CH16 IN
3	CH32 IN	53	CH48 IN
4	CH1 IN	54	CH17 IN
5	CH33 IN	55	CH49 IN
6	CH2 IN	56	CH18 IN
7	CH34 IN	57	CH50 IN
8	CH3 IN	58	CH19 IN
9	CH35 IN	59	CH51 IN
10	CH4 IN	60	CH20 IN
11	CH36 IN	61	CH52 IN
12	CH5 IN	62	CH21 IN
13	CH37 IN	63	CH53 IN
14	CH6 IN	64	CH22 IN
15	CH38 IN	65	CH54 IN
16	CH7 IN	66	CH23 IN
17	CH39 IN	67	CH55 IN
18	LLGND	68	LLGND
19	CH8 IN	69	CH24 IN
20	CH40 IN	70	CH56 IN
21	CH9 IN	71	CH25 IN
22	CH41 IN	72	CH57 IN
23	CH10 IN	73	CH26 IN
24	CH42 IN	74	CH58 IN
25	CH11 IN	75	CH27 IN
26	CH43 IN	76	CH59 IN
27	CH12 IN	77	CH28 IN
28	CH44 IN	78	CH60 IN
29	CH13 IN	79	CH29 IN
30	CH45 IN	80	CH61 IN
31	CH14 IN	81	CH30 IN
32	CH46 IN	82	CH62 IN
33	CH15 IN	83	CH31 IN
34	CH47 IN	84	CH63 IN
35	AISENSE	85	DIO0
36	D/A OUT 0 *	86	DIO1
37	D/A GND	87	DIO2
38	D/A OUT1 *	88	DIO3
39	PC +5 V	89	DIO4
40	AUXOUT0 / D/A PACER OUT	90	DIO5
41	AUXOUT1 / A/D PACER OUT	91	DIO6
42	AUXOUT2 / SCANCLK	92	DIO7
43	AUXIN0 / A/D CONVERT / ATRIG	93	CTR1 CLK
44	N/C	94	CTR1 GATE
45	AUXIN1 / A/D START TRIGGER	95	CTR1 OUT
46	AUXIN2 / A/D STOP TRIGGER	96	GND
47	AUXIN3 / D/A UPDATE	97	CTR2 CLK
48	AUXIN4 / D/A START TRIGGER	98	CTR2 GATE
49	AUXIN5 / A/D PACER GATE	99	CTR2 OUT
50	GND	100	GND

* = N/C on PCI-DAS6033

CE Declaration of Conformity

Manufacturer:	Measurement Computing Corporation
Address:	10 Commerce Way Suite 1008 Norton, MA 02766 USA
Category:	Electrical equipment for measurement, control and laboratory use.

Measurement Computing Corporation declares under sole responsibility that the product

PCI-DAS6031 and PCI-DAS6033

to which this declaration relates is in conformity with the relevant provisions of the following standards or other documents:

EC EMC Directive 2004/108/EC: General Requirements, EN 61326-1:2006 (IEC 61326-1:2005).

Emissions:

- EN 55011 (2007) / CISPR 11(2003): Radiated emissions: Group 1, Class A
- EN 55011 (2007) / CISPR 11(2003): Conducted emissions: Group 1, Class A

Immunity: EN 61326-1:2006, Table 3.

- IEC 61000-4-2 (2001): Electrostatic Discharge immunity.
- IEC 61000-4-3 (2002): Radiated Electromagnetic Field immunity.
- IEC 61000-4-4 (2004): Electric Fast Transient Burst Immunity.
- IEC 61000-4-5 (2001): Surge Immunity.
- IEC 61000-4-6 (2003): Radio Frequency Common Mode Immunity.
- IEC 61000-4-11 (2004): Voltage Interrupts.

To maintain compliance to the standards of this declaration, the following conditions must be met.

- The host computer, peripheral equipment, power sources, and expansion hardware must be CE compliant.
- All I/O cables must be shielded, with the shields connected to ground.
- I/O cables must be less than 3 meters (9.75 feet) in length.
- The host computer must be properly grounded.
- Equipment must be operated in a controlled electromagnetic environment as defined by Standards EN 61326-1:2006, or IEC 61326-1:2005.

Declaration of Conformity based on tests conducted by Chomerics Test Services, Woburn, MA 01801, USA in July, 2004. Test records are outlined in Chomerics Test Report #EMI3931.04. Further testing was conducted by Chomerics Test Services, Woburn, MA. 01801, USA in December, 2008. Test records are outlined in Chomerics Test report #EMI5216.08.

We hereby declare that the equipment specified conforms to the above Directives and Standards.



Carl Haapaoja, Director of Quality Assurance

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