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CP605

6U CompactPCI
Pentium 4 Based CPU Board

Manual ID: 25095, Rev. Index 07
October 2004

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The product described in this manual is in compliance with all applied CE standards.

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Kontron Modular Computers GmbH may be contacted via the following:

MAILING ADDRESS

Kontron Modular Computers GmbH
Sudetenstraße 7
D - 87600 Kaufbeuren Germany

TELEPHONE AND E-MAIL

+49 (0) 800-SALESKONTRON
sales@kontron.com

For further information about other Kontron Modular Computers' products, please visit our Internet web site: **www.kontron.com**

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Explanation of Symbols

CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.

Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

Before installing your new Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

- Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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General Instructions on Usage

- In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron Modular Computers GmbH and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Kontron Modular Computers GmbH warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long-term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron Modular Computers GmbH or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

Kontron provides for repair or replacement of any part, assembly or sub-assembly at their own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to Kontron Modular Computers GmbH, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by Kontron with the repaired or replaced item.

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Chapter 1

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the home page of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to Kontron Modular Computers CompactPCI systems may be found described in the Kontron CompactPCI System Manual. Due to its size, this manual cannot be downloaded via the internet. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine Kontron’s racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of Kontron CompactPCI boards, such as functionality, hot swap capability. In addition, an overview is given for all existing Kontron CompactPCI boards with links to the relating data sheets.
- Generic information on the Kontron CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the Kontron CompactPCI standard backplane family.
- Generic information on the Kontron CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the Kontron CompactPCI standard power supply unit family.

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1.2 Board Overview

1.2.1 Board Introduction

The CP605 is an advanced 64-bit / 33 MHz CompactPCI system controller board. It has been designed to support the latest Intel® Pentium® processors:

- **Pentium 4**
- **Mobile Pentium 4 Processor-M**

Both processors have a 512 KB L2 cache whereby the Pentium 4 comes in the FCPGA2 package (Desktop version) and the Mobile Pentium 4 Processor-M in the µFCPGA package (Mobile version).

The Pentium 4 Processor-M version has the advantage of very low power consumption, whilst at the same time providing impressive processor speeds ranging from 1.2 GHz through 2.2 GHz with a PSB running at 400 MHz. The desktop Pentium 4 processor version offers very high processor speeds ranging from 2 GHz through 2.4 GHz with a PSB running at 400 MHz and 533 MHz. The CP605 utilizes the Intel 845GV and ICH4 I/O Controller Hub (ICH4) chipset.

The board includes up to 1 GB of soldered Double Data Rate (DDR) memory. In addition, there is one SODIMM socket (200-pin) available to add up to 1 GB of DDR memory whereby the maximum memory configuration is 2 GB. The memory is operated either at 200 or 266 MHz.

System features include two Gigabit Ethernet ports, one Fast Ethernet port (82559-style), one PMC slot to support further PCI devices, and one optional Network Security processor. The board also includes a built-in Intel 2D/3D Graphics accelerator with up to 64 MB memory for enhanced graphics performance with a VGA CRT-display interface.

The CP605 comes with the following PC interfaces including: five USB 2.0 ports, four COM ports, two EIDE ATA100 interfaces, one CompactFlash socket, one Floppy port, one parallel I/O interface, and the rear I/O CompactPCI bus connectors J3, J4, and J5. In addition, there is an optional Intelligent Platform Management Interface (IPMI) available.

The board supports one configurable 64-bit, 33 MHz, hot swap CompactPCI interface. In the System Master slot the bridge is enabled, and if installed in a peripheral slot, the CP605 is isolated from the CompactPCI bus.

One of the more important features of the CP605 is its support of the PICMG CompactPCI Packet Switching Backplane Specification 2.16. When installed in a backplane which supports packet switching, the CP605 can communicate via both of its Gigabit Ethernet interfaces with other boards which also support packet switching.

Designed for stability, the board fits into all applications situated in industrial environments making it a perfect core technology for long life applications.

The components which make up the CP605 have been carefully selected from embedded technology programs to ensure long-term availability.

The board is compatible with the Microsoft® Windows® 2000, Windows® XP and Windows® XP Embedded operating systems. However, the performance of CompactPCI can be tailored to suit real-time applications and operating systems such as Linux®, or VxWorks® which are instrumental to the success of CompactPCI in these market sectors.

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1.2.2 Board-Specific Information

The CP605 is a CompactPCI Pentium 4 processor based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP605's outstanding features are:

- Intel microprocessors up to 2.4 GHz available:
  - **Pentium 4 Processor up to 2.4 GHz**
  - **Mobile Pentium 4 Processor-M up to 2.2 GHz or higher***
- FC-PGA2 and µFCPGA packages respectively
- Up to 512 kB L2 cache on-die running at CPU speed
- 82845GV GMCH and 82801 ICH4 chipset
- 400 MHz and 533 MHz processor system bus
- Up to 2 GB of DDR SDRAM memory running at 200 or 266 MHz
- PCI local bus: 32-bit / 33 MHz
- CompactPCI bus interface: 64-bit / 33 MHz
- Integrated 3D high performance VGA controller
- Analog display support up to 2048 x 1536 pixels at 16 bits and 60 Hz
- Two Gigabit Ethernet interfaces
  - 10Base-T, 100Base-TX, and 1000Base-T
  - Configurable for front panel or rear I/O / CPCI backplane packet switching (PICMG 2.16, R1.0) interfacing
- One integrated, configurable Fast Ethernet interface (82559-style), 10Base-T, 100Base-TX
- PMC interface (32-bit, 5 V signal voltage) with rear I/O support and bezel cutout on front panel
- Two EIDE Ultra ATA/100 interfaces
- Onboard CompactFlash type II socket
- Optional socket for 2.5" hard disk or Flash Disk instead of the PMC interface
- Four serial ports
- Five USB 2.0 ports
- PS/2 keyboard and mouse interface
- Floppy disk interface
- Parallel I/O interface
- Hardware monitor (LM81 and MAX1617)
- Watchdog timer
- Real-time clock
- Two, 1 MB onboard FWHs (1 MB for BIOS and 1 MB for OS)
- I/O extension connector with Low Pin Count interface (LPC)
- 4HP, 6U CompactPCI
- Hot swap capability: as system controller or as peripheral device
- Supports PICMG Packet Switching Backplane Specification
- Rear I/O on J3 and J5; optionally on J4
- IPMI compliant Baseboard Management Controller (optional)
- Network security processor (optional)
- Passive heat sink solution
- Phoenix BIOS

* subject to availability from Intel

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1.3 System Expansion Capabilities

1.3.1 PMC Modules

The CP605 has one, 32-bit, 33 MHz, 5 V signal voltage, rear I/O capable, PMC mezzanine interface. This interface supports a wide range of available PMC modules including all of Kontron's PMC modules and provides an easy and flexible way to configure the CP605 for various application requirements.

1.3.2 CP-RIO6-05 Rear I/O Module

The CP-RIO6-05 rear I/O module has been designed for use with the CP605 6U CompactPCI board from Kontron Modular Computers. This module provides comprehensive rear I/O functionality and may also be configured for use in other applications.

For further information concerning the CP-RIO6-05 module please refer to Appendix A.

1.4 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP605.

Table 1-1: System Relevant Information

SUBJECT	INFORMATION
System Slot / System Master Functionality	The CP605 is designed to for use as a System Master board whereby it can support up to 7 peripheral boards with 64-bit and 33 MHz. It may, however, be operated in a peripheral slot in which case it does not support the CompactPCI bus interface.
Peripheral Slot Functionality	When installed in a peripheral slot, the CP605 is electrically isolated for the CompactPCI bus. It receives power from the backplane and supports rear I/O and, if the system supports it, packet switching (in this case up to two channels of Gigabit Ethernet).
Hot Swap Compatibility	When operated as a System Master, the CP605 supports individual clocks for each slot and ENUM signal handling is in compliance with the PICMG 2.1 Hot Swap Specification. When operated in a peripheral slot the CP605 supports basic hot swap.
Operating Systems	The CP605 can be operated under the following operating systems: • Microsoft® Windows® 2000 • Microsoft® Windows® XP • Microsoft® Windows® XP Embedded • Linux® • VxWorks® Please contact Kontron Modular Computers for further information concerning other operating systems.

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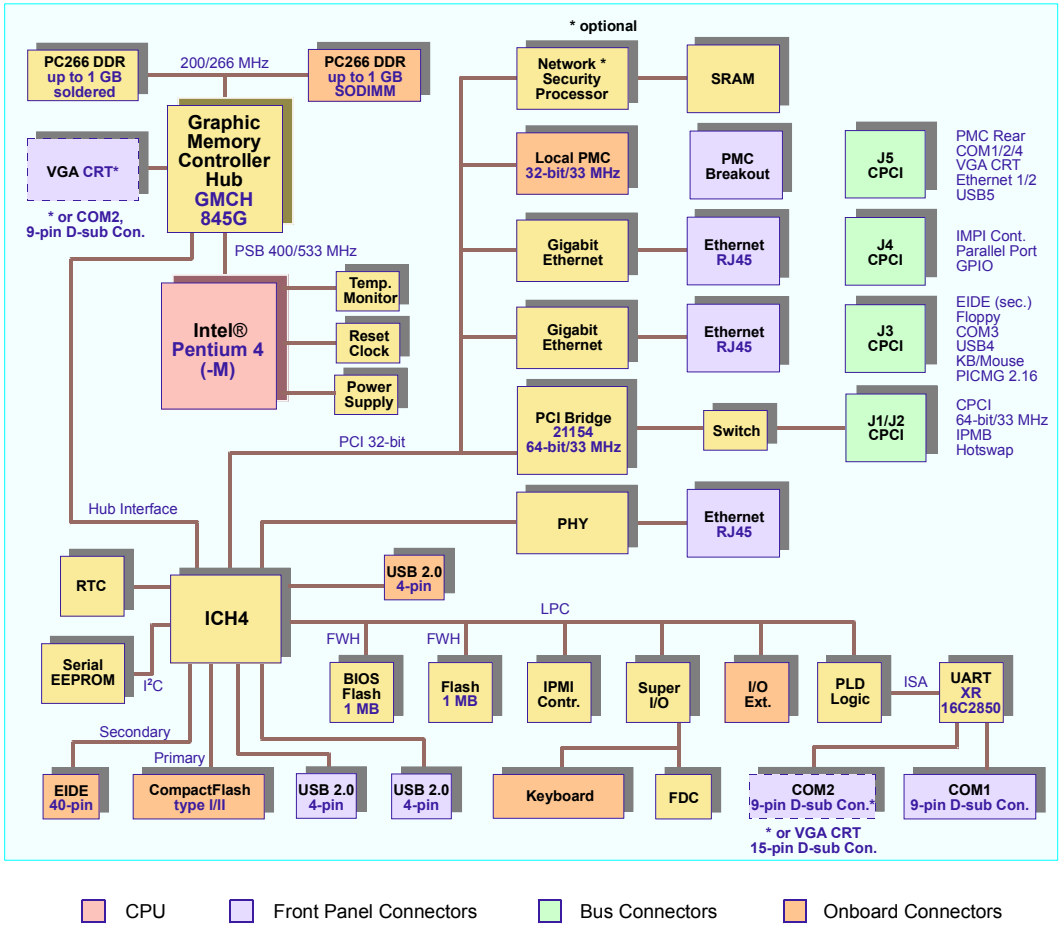
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1.5 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

1.5.1 Functional Block Diagram

Figure 1-1: CP605 Functional Block Diagram



NOTE: Population of the VGA CRT connector or the COM2 port connector is dependent on application requirements.

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1.5.2 Front Panels

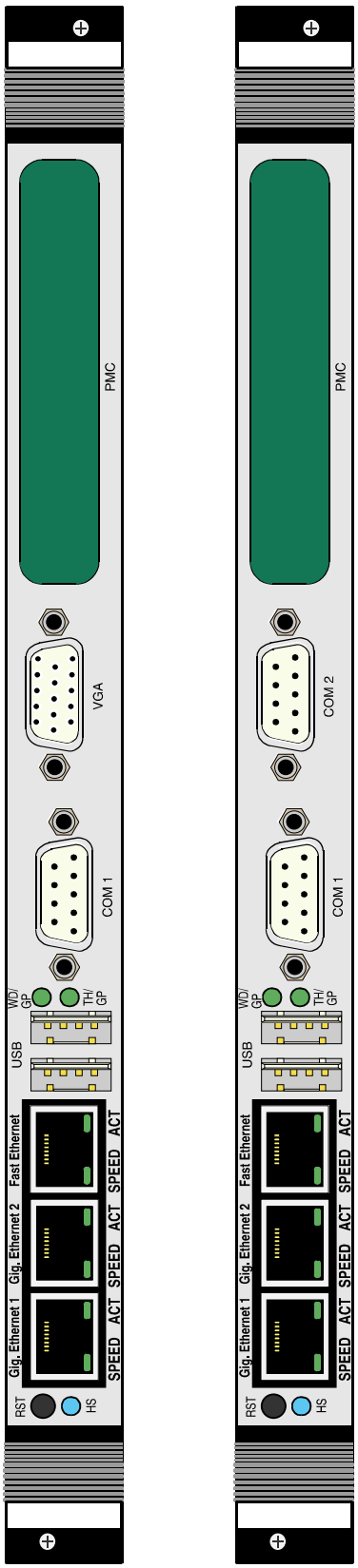


Figure 1-2:CP605 4HP Front Panels

Legend:

Left CP605: 4HP VGA version

Right CP605: 4HP COM version

General Purpose (GP) LEDs

WD/GP (green): Watchdog or General Purpose, when lit during bootup, it indicates that PCI reset is active.

TH/GP (green): Overtemperature Status or General Purpose, when lit during bootup, it indicates a power failure.

HS (blue): Hot Swap Control

Integrated Fast Ethernet LEDs

ACT (green): Ethernet Link/Activity

SPEED (green): Ethernet Speed: on = 100 MBit

Integrated Gigabit Ethernet LEDs

ACT (green): Ethernet Link/Activity

SPEED (green): Ethernet Speed: on = 1000 MBit

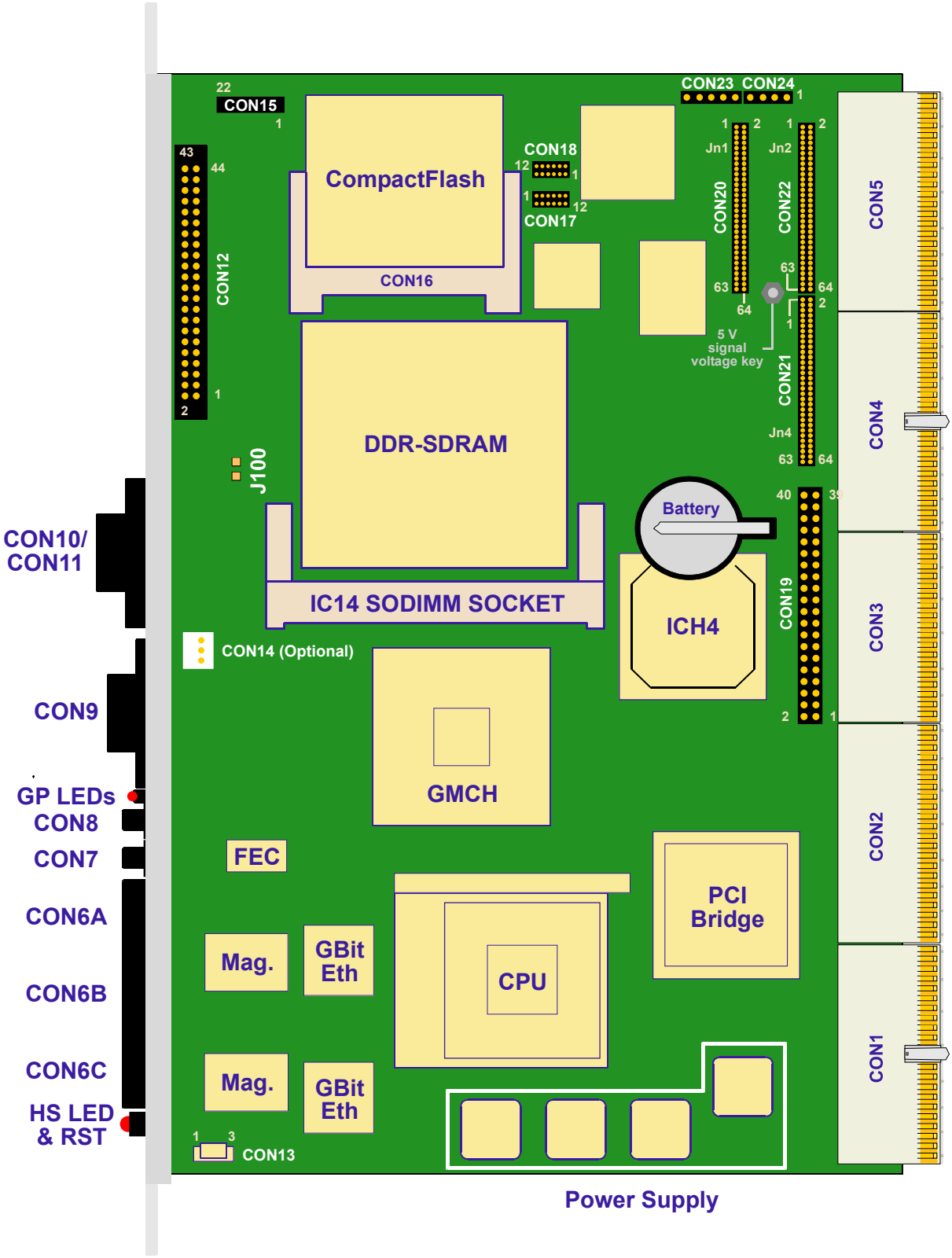
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1.5.3 Board Layout

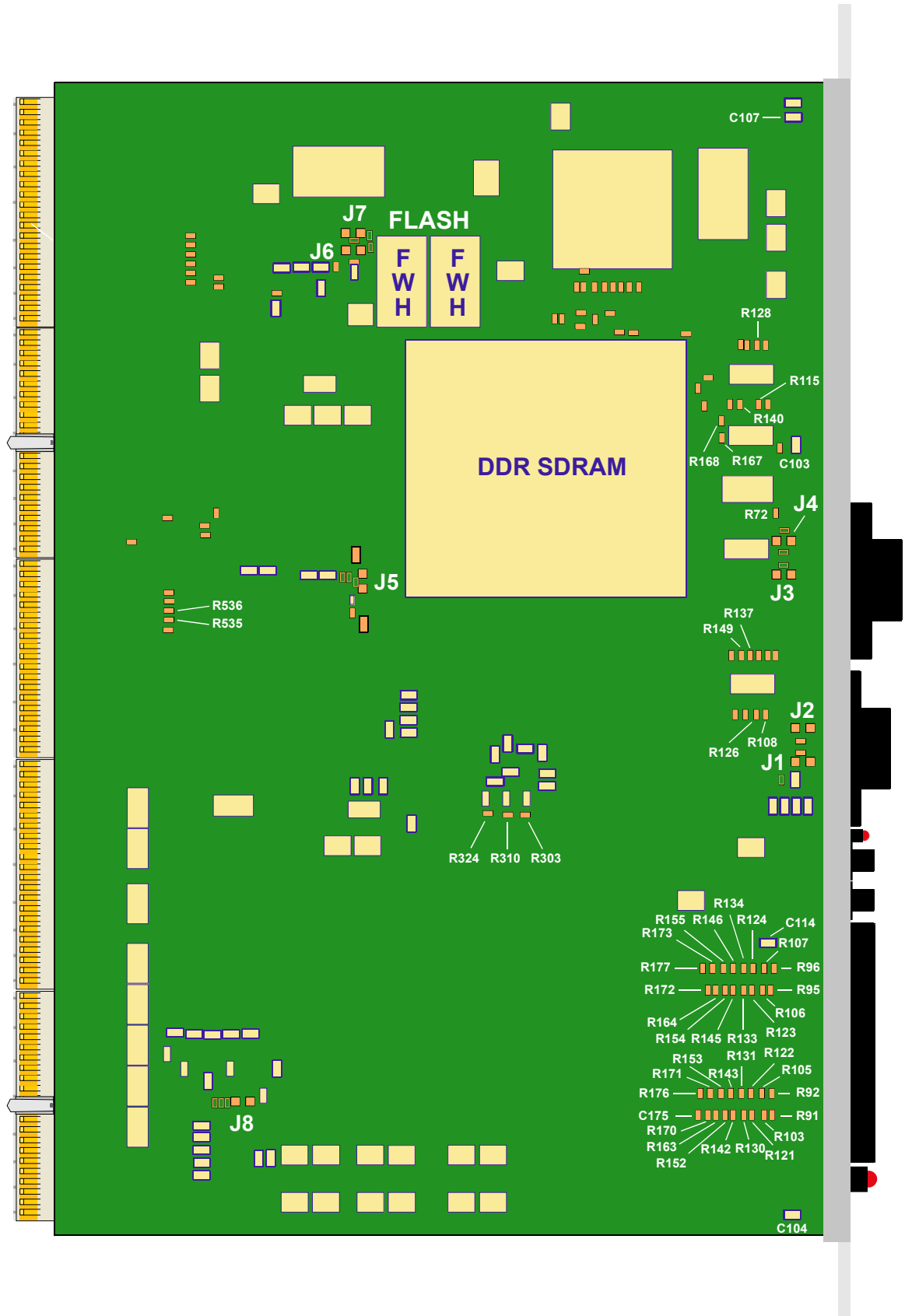
Figure 1-3: CP605 Board Layout (Front View)



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Figure 1-4: CP605 Board Layout (Reverse View)



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1.6 Technical Specifications

Table 1-2: CP605 4HP Version Main Specifications

	CP605	SPECIFICATIONS
PROCESSOR AND MEMORY	CPU	The CP605 supports one or the other of the following Intel processor types: **Pentium 4 Processor** • Up to 2.4 GHz • 512 kB L2 on-die cache • 400 and 533 MHz PSB • 478-pin FC-PGA2 package **Mobile Pentium 4 Processor-M** • Up to 2.2 or higher GHz • 512 kB L2 on-die cache • 400 and 533 MHz PSB • Supports SpeedStep® II for low power mode • 478-pin µFCPGA package
	Memory	Main memory: • Up to 1 GB soldered DDR SDRAM memory • Up to 1 GB of additional memory capacity via a 200-pin SODIMM socket • Memory frequency: 200 MHz or 266 MHz Flash memory: • Two Firmware Hub Flash memory • 1 MB FWH for BIOS • 1 MB FWH extension for OS or user EEPROM: • Two 256 byte EEPROMs for storing CMOS data when operating without battery • Two 256 byte EEPROM's for user purposes
CHIPSET	Intel 845GV Chipset	82845GV Graphics Memory Controller Hub (GMCH): • Support for a single Pentium 4 microprocessor • 64-bit AGTL/AGTL+ based System Bus interface at 400 MHz and 533 MHz • 64-bit System Memory interface with optimized support for DDR SDRAM memory at 200 MHz or 266 MHz • Integrated 2D and 3D Graphics Engines with 200 MHz core frequency • Integrated H/W Motion Compensation Engine • Integrated 350 MHz DAC • Integrated Digital Video Out Port • AGP 1X/2X/4X Controller

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Table 1-2: CP605 4HP Version Main Specifications (cont'd)

	CP605	SPECIFICATIONS
CHIPSET (cont'd)	Intel 845GV Chipset	82801DB I/O Controller Hub (ICH4) • PCI Rev. 2.2 compliant with support for 32-bit/33 MHz PCI operations • Power management logic support • Enhanced DMA controller, interrupt controller, and timer functions • Integrated IDE controller Ultra ATA/100/66/33 • USB 2.0 host interface with up to five USB ports available on the CP605 • One integrated LAN controller (82559 style) • System Management Bus (SMBus) compatible with most I²C® devices • Low Pin Count (LPC) interface • Firmware Hub (FWH) interface support
EXTERNAL INTERFACES	CompactPCI Bus Interface	Compliant with CompactPCI Specification PICMG 2.0 R3.0 • System Master operation • 64-bit / 33 MHz master interface • 3.3V / 5.0V compatible (default configuration is 5.0V) • When the CP605 is operated in a peripheral slot, the CPCI bus is electrically isolated from the CP605.
	Serial	COM1 and COM2: • Dual UART, 16C550 compatible • RS-232, RS-422, or RS-485 configurable • COM1, 9-pin, D-sub connector on the front panel • Optionally COM2, 9-pin, D-sub connector on the front panel Either the COM2 connector is populated or the VGA CRT-display connector, depends on application requirements.
		COM3 and COM4: • 16C550 compatible UARTs • Rear I/O interfacing only • TTL level signals
	Parallel	Multi-Mode™ Parallel I/O Interface • Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bidirectional parallel I/O interface • TTL level signals • Rear I/O interfacing only
	USB Interface	Five USB 2.0 ports supporting UHCI and EHCI: • Two USB type connectors on the front panel • Two rear I/O interfaces • One onboard port connector

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Table 1-2: CP605 4HP Version Main Specifications (cont'd)

	CP605	SPECIFICATIONS
EXTERNAL INTERFACES	Gigabit Ethernet	Two 10/100/1000 MB/s Gigabit Ethernet interfaces based on the Intel 82540EM (Kenai-32) Ethernet PCI bus controller. • Two RJ45 connectors on the front panel • Support for two Gigabit Ethernet channels on packet switching backplane (PICMG 2.16, R1.0 compliant) • Any given channel may only be operated at one or the other of the above interfacing points • Automatic mode recognition • Automatic cabling configuration recognition Cabling requirement: Category 5, UTP, four-pair cabling
	Fast Ethernet	One 10Base-T/100Base-TX Fast Ethernet port integrated within the ICH4 controller (82559-style): • One RJ45 connector on the front panel • Support for one channel of rear I/O interfacing • May only be operated at one or the other of the above interfacing points • Automatic mode recognition Cabling requirement: Category 5, UTP, two-pair cabling.
INTERNAL INTERFACES	VGA Interface	Built-in Intel 3D Graphics accelerator for enhanced graphics performance. • Supports resolutions of up to 2048 x 1536 by 16 bit at 60 Hz refresh rate • Hardware motion compensation for software MPEG2 and MPEG4 decoding • Flexible allocation of video memory up to 64 MB • 15-pin D-sub VGA CRT-display connector with analog video signals
	Keyboard and Mouse	Super I/O support for a keyboard and a mouse: • Rear I/O interfacing for both keyboard and mouse • Separate onboard keyboard connector (5-pin), requires adaptor to connect regular keyboard
	Mass Storage	EIDE Ultra ATA/100/66/33 • Two interfaces • Up to four devices (hard disks or CD-ROMs) • 40-pin, 2.54 mm, male pin row connector (standard) • Optional 44-pin, 2.0 mm, male pin row connector for mounting a 2.5" disk drive onboard.
		CompactFlash: • CompactFlash type II socket (true IDE mode) • Supports type I and II CompactFlash cards and Microdrive

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Table 1-2: CP605 4HP Version Main Specifications (cont'd)

	CP605	SPECIFICATIONS
INTERNAL INTERFACES	Mass Storage	Floppy Disk: • Rear I/O interfacing only • Supports 5.25 or 3.5 inch floppy drives • 1.44 or 2.88 MB, 3.5 inch floppy disks
	LPC	I/O extension interface: • 22-pin, female, pin row connector • Supports up to two LPC devices • Designed to support custom, fixed mounted, mezzanine boards
	PMC	CMC / PMC P1386 / Draft 2.4a compliant mezzanine interface: • Jn1, Jn2, and Jn4 PCI mezzanine connectors for standard PMC modules • 32-bit / 33 MHz master interface • 5.0 V signal voltage (3.3 V on request) • Rear I/O supported through CompactPCI connector J5
	Encryption	Optional network security processor: • 7951 Network Security Processor from HIFN • High performance data encryption / compression / authentication processor • PCI interface • local SRAM (128 kB) memory
	Rear I/O	To optimize cabling rear I/O is available via the J3, J5, and, optionally, J4 connectors in conjunction with the rear I/O transition module CP-RIO6-05. • J3: floppy, COM3, keyboard, mouse, USB4, and either one EIDE port or PICMG 2.16 support. • J5: VGA-CRT, two Ethernet channels without LEDs, USB5, COM1, COM2, COM4, control signals, PMC rear I/O connectivity • J4: parallel I/O interface, GPIO, IPMI fan control signals Note: If the CP605 is to be used with a H.110 CompactPCI backplane, connector J4 must not be populated.
MONITOR AND CONROL	LEDs	System status: • TH/GP: green: overtemperature status or general purpose, when remains lit during bootup, it indicates a power failure. • WD/GP: green: Watchdog or general purpose, when remains lit during bootup, it indicates that PCI reset is active. • HS: blue: Hot swap control Gigabit Ethernet status (1 and 2): • ACT: green: network activity • SPEED: green: network speed Fast Ethernet status: • ACT: green: network activity • SPEED: green: network speed

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Table 1-2: CP605 4HP Version Main Specifications (cont'd)

	CP605	SPECIFICATIONS
MONITOR AND CONTROL	Switches	Reset switch (RST): • Initiates cold restart of CP605 • Recessed to prevent accidental activation Hot swap switch: • When activated initiates local interrupt • Interrupt handling is a function of the CP605 application software • Integrated as part of the lower ejector handle
	Watchdog	Software configurable Watchdog generates IRQ, NMI, or hardware reset.
	Thermal Management	CPU over temperature protection is provided by: • Internal processor temperature control unit • CPU shut down via hardware monitor • Custom designed heat sinks
	System Monitor	LM81 hardware monitor for supervision of: • System power voltages: +12V, -12V, +5V, +3.3V, and VCORE • RTC battery voltage • Up to two fan speed inputs
	CPU Temperature Monitor	MAX 1617 hardware monitor for supervision of: • On-die CPU temperature • CPU surrounding board temperature
	IPMI	Optional IPMI compliant Qlogic Zircon Lite Baseboard Management Controller (BMC) for supervision of: • System power voltages: +12V, -12V, +5V, +3.3V, +2.5V, VCORE, VIO • CPU surrounding board temperature • Up to four fan speed inputs • Up to two fan speed control outputs • Supports IPMI compliant interfacing via the rear I/O connectors: J1, J3, and J4
	Hot Swap Compatible	The CP605 supports System Master hot swap functionality and application dependent hot swap functionality when used in a peripheral slot. When used as a System Master the CP605 supports individual clocks for each slot and ENUM signal handling is in compliance with the PICMG 2.1 Hot Swap Specification.
GENERAL	Mechanical	6U, 4HP, CompactPCI compliant form factor
	Power Consumption	See Chapter 5 for details
	Temperature Range	Operational: 0°C to +60°C Standard (only with designated CPU types) -25°C to +75°C E1 (optional; only with designated CPU types) Storage: -55°C to +85°C Without hard disk -40°C to +65°C With hard disk
	Climatic Humidity	93% RH at 40 °C, non-condensing (acc. to IEC60068-2-78)

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Table 1-2: CP605 4HP Version Main Specifications (cont'd)

	CP605	SPECIFICATIONS
GENERAL	Dimensions	233.35 mm x 160 mm
	Board Weight	546 g (4HP variants with heat sink and without mezzanine boards)
	Battery	3.0V lithium battery for RTC with battery socket. Recommended types: • VARTA CR2025 • PANASONIC BR2020
SOFTWARE	Software BIOS	Phoenix BIOS with 1 MB of Flash memory and having the following features: • QuickBoot • QuietBoot • BootBlock • MultiBoot III • LAN boot capability for diskless systems • Boot from USB floppy • BIOS boot support for USB keyboards • Software enable/disable function for the rear I/O, Ethernet, and COM port configuration • Plug & Play capability • BIOS parameters are saved in the EEPROM • Board serial number is saved within the EEPROM • PC Health Monitoring
	Operating System	Operating systems supported: • Microsoft® Windows® 2000 • Microsoft® Windows® XP • Microsoft® Windows® XP Embedded • Linux® • VxWorks® Please contact Kontron Modular Computers for further information concerning other operating systems.

1.7 Software Support

As a real-time operating system, VxWorks® is supported. The standard PC features supported by the BIOS also allow for PC operating systems such as Microsoft® Windows® 2000, Windows® XP and Windows® XP Embedded and Linux®.

1.7.1 Kontron Support

Kontron is one of the few CompactPCI and VME vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, customers possessing a maintenance agreement with Kontron can be guaranteed hotline software support and are supplied with regular software updates. A dedicated web site is also provided for online updates and release downloads.

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1.8 Applied Standards

The *Kontron Modular Computers'* CompactPCI systems comply with the requirements of the following standards:

Table 1-3: Applied Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL (Ruggedized Version)
CE	Emission	EN50081-1, EN55022	--
	Immission	EN61000-6-2, EN55024	--
	Electrical Safety	EN60950	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental Aspects	Vibration (Sinusoidal)	IEC60068-2-6	2g/12-300Hz/10 acceleration / frequency range / test cycles per axis
	Permanent Shock	IEC60068-2-29	15g/11ms/500/1s peak acceleration / shock duration half sine / number of shocks / recovery time
	Single Shock	IEC60068-2-27	30g/9ms/18/5s peak acceleration / shock duration / number of shocks / recovery time in seconds
	Climatic Humidity	IEC60068-2-78	--



Note ...

The values in the above table are valid for boards which are ordered with the ruggedized service. For more information please contact your local Kontron office.

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1.9 Related Publications

The following publications contain information relating to this product.

Table 1-4: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification 2.0, Rev. 3.0 CompactPCI Packet Switching Backplane Specification PICMG 2.16 Rev. 2.0 CompactPCI System Management Specification PICMG 2.9 Rev. 1.0 CompactPCI Hot Swap Specification PICMG 2.1 Rev. 2.0
	Kontron Modular Computers' CompactPCI System Manual, ID 19954
PMC Add-on Modules and Carriers	Draft standard for Common Mezzanine Card Family: P1386, Draft 2.4a
	Draft standard for Physical and Environment Layers for PCI Mezzanine Cards: P1386.1, Draft 2.4
CompactFlash Cards	CF+ and CompactFlash Specification Revision 1.4

1.10 Trademarks

- CompactPCI is a trademark of the PCI industrial Computers Manufacturers Group
- Ethernet is a registered trademark of Xerox Corporation
- IEEE is a registered trademark of the Institute of Electrical and Electronics Engineers Inc.
- VxWorks is a registered trademark of WindRiver Systems Inc.
- Intel is a trademark of Intel Corporation
- Pentium 4 and Pentium 4 Processor-M are trademarks of Intel Corporation
- Microsoft is a trademark of the Microsoft Corporation
- Other trademarks are the property of their respective owners

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Chapter 2

Functional Description

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2. Functional Description

2.1 CPU

The CP605 board is based on the latest Intel Pentium 4 and Mobile Pentium 4 Processor-M in the FCPGA2 (Desktop version) and uFCPGA (Mobile version) packages.

The Intel Mobile Pentium 4 Processor-M supports the enhanced Intel SpeedStep® technology, which enables real-time dynamic switching of the voltage and frequency between two modes, the "Maximum Performance Mode" or the "Battery Optimized Mode". This occurs by switching the bus ratios, core operating voltage, and core processor speeds without resetting the system. The frequency for the Pentium 4-M processor can be selected in the BIOS.

Key performance features of the Intel Pentium 4 Processor include 512 kB on-die L2 Cache and Intel NetBurst™ Micro-Architecture, consisting of a 400 MHz and 533 MHz processor system bus, Hyper Pipelined Technology, new Execution Trace Cache, Rapid Execution Engine, and 144 new Streaming SIMD instruction extensions.

The CP605 is available with a variety of Intel processors as indicated in the following table.

Table 2-1: Supported Intel Processors on the CP605

PROCESSOR	PACKAGE	SPEED	L2 CACHE	CORE VOLTAGE	PROCESSOR SIDE BUS
Pentium 4	FCPGA2	2 GHz	512 kB	1.5 V	400 MHz
Pentium 4	FCPGA2	2.4 GHz	512 kB	1.5 V	533 MHz
Pentium 4-M	uFCPGA	1.2 / 1.7 GHz	512 kB	1.2 V / 1.3 V	400 MHz
Pentium 4-M	uFCPGA	1.2 / 2.2 GHz	512 kB	1.2 V / 1.3 V	400 MHz
Plus future Intel Pentium 4 and Mobile Pentium 4 Processor-M microprocessors					



Note ...

Use only the processors listed above. Use of unsupported processors can damage the board, the processor, and the power supply.

2.2 Memory

The CP605 has two locations for installing memory; up to 1 GB may be soldered and a further 1 GB may be added by means of the onboard DDR SODIMM socket. The board supports a maximum of 2 GB. All installed memory will be automatically detected, so there is no need to set any jumpers. The CP605 supports all PC200 and PC266 compliant DDR SDRAMs on 200-pin SODIMMs offered by Kontron Modular Computers. All memory components and SODIMMs used with this board must comply with the following PC DDR SDRAM memory specifications:

- PC DDR SDRAM Memory Specification PC200 and PC266
- PC Serial Presence Detect Specification

Only qualified DDR SDRAMs from Kontron Modular Computers can be used with the CP605.

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Table 2-2: Memory Options Utilizing SODIMM Sockets

ONBOARD	SODIMM	TOTAL
512 MB *	--	512 MB
512 MB *	512 MB	1 GB
1 GB	--	1 GB
1 GB	1 GB	2 GB



Note ...

The memory options marked with a * are the standard product configuration.

It is recommended to use only DDR memory.



Note ...

When the CP605 is ordered for the extended temperature range E1 (-25 °C to + 75°C), SODIMM DDR SDRAM modules are not supported due to their being unavailable for this temperature range.

2.3 Chipset

The Intel 845GV chipset consists of the following devices:

- 82845GV Graphics and Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- 82801 I/O Controller Hub 4 (ICH4) with AHA bus
- Firmware Hub (FWH)

The GMCH provides the processor interface for the Pentium 4 microprocessor, the memory bus, the AGP 4x bus in the case of an external graphics controller, and includes a high performance graphics accelerator. The ICH4 is a centralized controller for the boards' I/O peripherals, such as the PCI, USB 2.0, EIDE, LAN and AUDIO ports. The Firmware Hub (FWH) provides the non-volatile storage of the BIOS.

2.3.1 Graphics and Memory Controller Hub (845GV)

The 845GV Graphics Memory Controller Hub (GMCH) is a highly integrated hub that provides the CPU interface, the DDR SDRAM system memory interface, a hub link interface to the ICH4 and an AGP interface for an external VGA controller or high performance internal graphics.

Host Interface

The 845GV is optimized for the Intel Pentium 4 microprocessors. The chipset supports a Processor Side Bus (PSB) frequency of 400 MHz and 533 MHz with AGTL+ signaling. Single ended AGTL termination is supported for single processor configurations. It supports 32 bit host addressing for decoding up to 4 GB memory address space.

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System Memory Interface

The 845GV integrates a system memory DDR SDRAM controller with a 64 bit wide interface without ECC. The chipset supports PC200 and PC266 Double Data Rate (DDR) SDRAM for system memory.

845GV Graphics Controller

The 845GV includes a highly integrated graphics accelerator and H/W Motion Compensation engines for software MPEG2 decoding, delivering high performance 2D and 3D video capabilities. The internal graphics controller provides interfaces to a standard CRT display. These interfaces are only active when running in internal graphics mode.

2.3.2 I/O Controller Hub ICH4

The ICH4 is a highly integrated multifunctional I/O Controller Hub that provides the interface to the PCI Bus and integrates many of the functions needed in today's PC platforms, for example, Ultra DMA 100/66/33 controller, USB host controller supporting USB 2.0, LPC interface, FWH Flash BIOS interface controller, LAN interface and an AC'97 digital controller. The ICH4 communicates with the host controller over a dedicated hub interface.

I/O Controller Hub Feature set comprises:

- PCI 2.2 interface with eight IRQ inputs
- Bus Master EIDE controller UltraDMA 100/66/33
- Three USB controllers with up to six USB 1.1 or USB 2.0 ports
- Hub interface with 845GV
- FWH interface
- LPC interface
- AC 97 2.1 interface
- Integrated LAN controller, 82559 style
- RTC controller
- Multimedia timer (additional timer)

2.4 Peripherals

The following standard peripherals are available on the CP605 board:

2.4.1 Timers

The CP605 is equipped with the following timers:

- Real-Time Clock

  The ICH4 contains a MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM.

  The real-time clock performs timekeeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar. All battery-backed CMOS RAM data remains stored in an additional EEPROM. This prevents data loss.

- Counter/Timer

  Three 8254-style counter/timers are included on the CP605 as defined for the PC/AT.

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2.4.2 Watchdog Timer

The CP605 employs a watchdog timer, which forces either an IRQ5, NMI, or Reset condition (configurable in the watchdog register). The watchdog time can be programmed in 12 steps ranging from 125 msec up to 256 seconds. If the watchdog timer is enabled, it cannot be stopped.

2.4.3 Battery

The CP605 utilizes a 3.0V “coin cell” lithium battery for the RTC.

2.4.4 Reset

The CP605 is automatically cold reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.725 V for the 5 V line and below 3.0 V for the 3.3 V line, or in the event of a power failure of the DC/DC converter. Other reset sources include the watchdog timer and the local push-button switch. The CP605 responds to any of these sources by initializing local peripherals.

A reset will be generated by the following conditions:

- +5 V supply falls below +4.75 V
- +3.3 V supply falls below +3.0 V
- Power failure of the DC/DC converter for the processor
- Push button "RESET" pressed
- Watchdog timeout
- CompactPCI backplane PRST input

2.4.5 Local SMBus Devices

The CP605 provides a System Management Bus (SMBus) for access to several system monitoring and configuration functions. The SMBus consists of a two-wire I²C-bus interface and several serial devices. The following table describes the function and address of every onboard SMBus device.

Table 2-3: SMBus Device Addresses

DEVICE	SMBUS ADDRESS
Temperature Sensor MAX1617	0011000Xb
Hardware Monitor LM81	0101100Xb
EEPROM	1010XXXXb

2.4.6 Thermal Management / System Monitoring

The LM81 can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds and temperatures; all of which are very important for the proper operation and stability of a high-end computer system. The LM81 provides an I²C serial bus interface.

The voltages of the onboard power supply, which are: +12 V, -12 V, +5 V, +3.3 V, VCore, and the battery voltage are supervised. Two fan tachometer outputs can be measured using the LM81’s FAN1 and FAN2 inputs.

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The integrated MAX1617 temperature sensors monitor the CPU temperature and the ambient temperature around the CPU to make sure that the system is operating at a safe temperature level. If the temperature is too high, the sensors automatically reduce the CPU clock frequency, depending on the mode chosen in the BIOS set.

2.4.7 Serial EEPROM

A serial EEPROM is provided, organized into 4 blocks with 256 bytes per block (24LC08). This EEPROM is connected to the I²C-bus provided by the ICH4.

Table 2-4: EEPROM Address Map

ADDRESS	FUNCTION
1010000xb	Onboard DDR SDRAM memory
1010001xb	SODIMM DDR SDRAM memory
1010010xb	Reserved
1010011xb	Reserved
1010100xb	VxWorks® parameter
1010101xb	Free for user purposes
1010110xb	Free for user purposes
1010111xb	CMOS backup and board serial number



Note ...

It is strongly recommended that users access only the two free EEPROM banks.

2.4.8 BIOS FLASH (Firmware Hub)

For simple BIOS updating a standard onboard 1 MB Firmware Hub device is used.

The FWH stores both the system BIOS and video BIOS. It can be updated as new versions of the BIOS become available. You may easily upgrade your BIOS using the Phoenix Phlash16 utility.

2.4.9 User FLASH

For small flash extensions an additional 1 MB Firmware Hub flash memory is available.

2.4.10 Dual BIOS

Dual BIOS means that there are two chips for the BIOS on the CP605 board (BIOS Flash and the User Flash). One chip is intended to act as a backup in the event that the other one gets corrupted. These chips are soldered on to the board.

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If the primary BIOS is corrupted due to physical damage or a faulty flash upgrade, the solder jumper J6 must be set; the system will switch over to the secondary chip and boot with default settings.



Note ...

The Dual BIOS feature cannot be used if the second Flash chip is used for VxWorks® bootup.

2.4.11 Network Security Processor

The CP605 provides an optional network security processor from the company HIFN.

The HIFN 7951 network security processor is a high performance data encryption processor designed for use in a variety of data communication applications. The device supports several data compression, data encryption and data authentication algorithms.

The HIFN 1791 network processor has a PCI interface and a local SRAM memory.

2.5 Board Interfaces

2.5.1 General Purpose LED Output

The CP605 provides two software programmable GP LEDs. After reset, the default configuration for the two front LEDs is Overtemperature and Watchdog status. Additionally, if the TH LED remains on during bootup, it indicates a power failure, and if the WD LED remains on during bootup, it indicates that PCI reset is active. In this case, please check the power supply. If the power supply appears to be functional and this LED remains on, please contact Kontron Support. The LED's can be configured via two onboard registers. For more information please see Chapter 4.



Note ...

If the overtemperature LED flashes on and off at regular intervals it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Upon assertion of Thermtrip, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature.

Once activated, Thermtrip remains latched until a cold restart of the CP605 is undertaken (all power off and then on again).

2.5.2 Keyboard/Mouse Interface

The onboard keyboard controller is 8042 software compatible.

The keyboard and mouse port is routed to the CompactPCI rear I/O interface. There is no front I/O connector available. To connect a keyboard a connector is available. **The mouse port is only available on the CompactPCI rear I/O interface.**

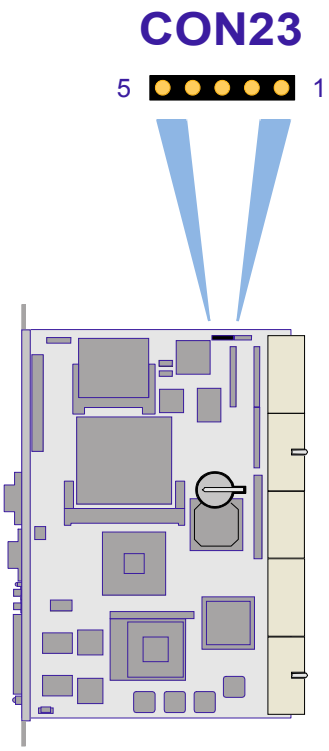
The CP605 has a 5-pin male pinrow connector for the keyboard interface.

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Figure 2-1: Keyboard Connector CON23



The following table indicates the pinout for the keyboard connector CON23.

Table 2-5: Keyboard Connector CON23 Pinout

PIN	NAME	FUNCTION	IN/OUT
1	KDATA	Keyboard data	IN/OUT
2	--	--	--
3	GND	Ground	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	OUT

2.5.3 USB Interfaces

The CP605 supports five USB 2.0 ports (two front I/O, one onboard interface and two on the rear I/O). All five ports are high-speed, full-speed, and low-speed capable. High-speed USB 2.0 allows data transfers of up to 480 Mb/s - 40 times faster than a full-speed USB (USB 1.1).

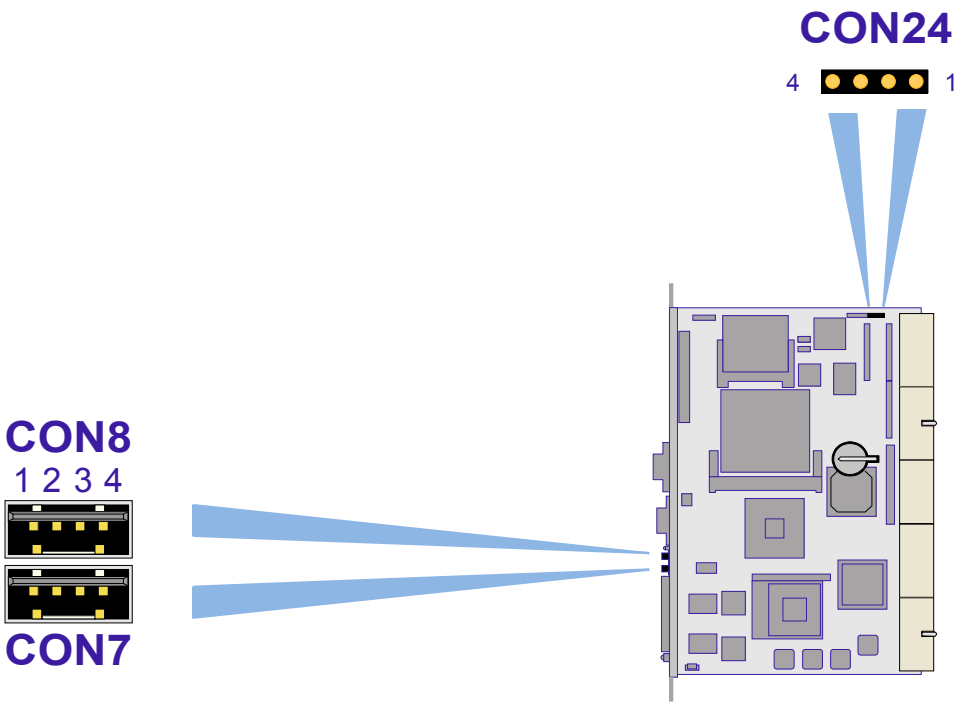
One USB peripheral may be connected to each port. To connect more than five USB devices an external hub is required.

The USB power supply is protected by a self-resettable 500 mA fuse on each channel (CON7/CON8). Short circuit current 0.9 A per channel.

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Figure 2-2: USB Connectors CON7, CON8 and CON24



The following table indicates the pinout for the USB Connectors CON7 and CON8 (External Connection) and CON24 (Internal Connection).

Table 2-6: USB Connectors CON7 and CON8 Pinouts

PIN	SIGNAL	FUNCTION	IN/OUT
1	VCC	VCC signal	--
2	UV0-	Differential USB-	IN/OUT
3	UV0+	Differential USB+	IN/OUT
4	GND	GND signal	--

Table 2-7: USB Connector CON24 Pinout

PIN	SIGNAL	FUNCTION	IN/OUT
1	VCC	VCC signal	--
2	UV0-	Differential USB-	IN/OUT
3	UV0+	Differential USB+	IN/OUT
4	GND	GND signal	--

Note ...

There is no current limitation circuit for the USB power on CON24. The power line is directly connected to VCC (5V).

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2.5.4 Graphics Controller

The 845GV chipset includes a highly integrated graphics accelerator delivering high performance 2D and 3D video capabilities. The internal graphics controller provides interfaces to a standard progressive scan monitor.

Integrated 2D/3D Graphics:

- 3D Setup and Render Engine
- High Quality Texture Engine
- 3D Graphics Rasterization Enhancements
- Full 2D hardware acceleration
- Intel 845GV D.V.M. Technology graphics core

Intelligent Memory Management

- Integrated 350 MHz DAC
- Resolution up to 1920x1080 at 85 Hz and 2048x1536 at 60 Hz.

2.5.4.1 Video Memory Usage

The 845GV chipset supports the new Dynamic Video Memory Technology (DVMT). This new technology ensures the most efficient use of all available memory for maximum 3D graphics performance. DVMT dynamically responds to application requirements allocating display and texturing memory resources as required.

The operating system requires up to 1 MB of system memory to support legacy VGA. System properties will display up to 1 MB less than physical system memory available to the operating system.

The graphics driver for the Intel 845GV configuration will request up to 64 MB of memory from the OS. By reallocating memory to the system, memory is freed up for other applications when not needed by the graphics subsystem. Thus, efficient memory usage is ensured for optimal graphics and system memory performance.

2.5.4.2 Video Resolution

The 845GV has an integrated 350 MHz RAMDAC that can directly drive a progressive scan analog monitor up to a resolution of 1920x1080 at 85 Hz and 2048x1536 at 60 Hz.

Table 2-8: Partial List of Display Modes Supported

RESOLUTION	COLOR RESOLUTION AT FREQUENCY		
	8-BIT	16-BIT	24-BIT
640x480	60, 75, 85,120	60, 75, 85,120	60, 75, 85,120
800x600	60, 75, 85,120	60, 75, 85,120	60, 75, 85,120
1024x768	60, 75, 85,120	60, 75, 85,120	60, 75, 85,100
1280x1024	60, 75, 85,120	60, 75, 85,120	60, 75, 85,100
1600x1200	60, 75, 85,100	60, 75, 85,100	60, 75, 85
1920 x 1440	60, 75	60, 75	--
2048 x 1536	60	60	--

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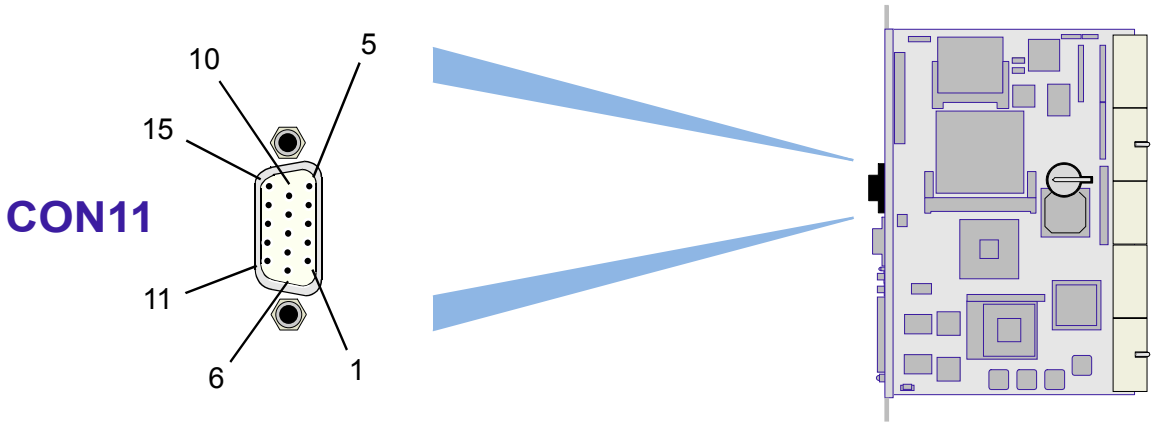
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2.5.4.3 CRT Interface and Connector CON11

Version of board with VGA-CRT interface

Figure 2-3: D-Sub CRT Connector CON11



The 15-pin female connector CON11 is used to connect a CRT monitor to the CP605 board.

Table 2-9: CRT Connector CON11 Pinout

PIN	SIGNAL	FUNCTION	IN/OUT
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL out
14	Vsync	Vertical sync.	TTL out
12	Sdata	I²C data	In/Out
15	Sclk	I²C clock	Out
9	VCC	Power +5V 200 mA, no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

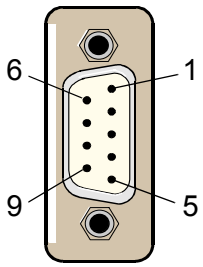
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2.5.5 Serial Port Interfaces COM1 and COM2

Figure 2-4: Serial Connectors CON9 (COM1) and CON10 (COM2)



Two PC-compatible serial 9-pin D-sub ports are available, which are fully compatible with the 16550 controller and include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 460.8 kB/s.

Serial Ports COM1 and COM2 can be enabled/disabled under SW control. Selection can be made inside the BIOS or via the rear I/O configuration register. The standard software configuration is front I/O.

The two COM interfaces may be configured as either RS-232, RS-422 or RS-485 ports by setting the appropriate solder jumpers. The standard setting of the two COM ports envisages the RS-232 configuration.

RS-422 configuration:

The RS-422 interface uses two differential data lines RX and TX for communication (Full-Duplex)

RS-485 configuration:

The RS-485 interface uses one differential data line. It differs from the RS-422 mode in that it provides the ability to transmit and receive over the same wire. The RTS signal is used to enable the RS-485 transmitter.

The following table indicates the pinout of the Serial Port Connectors CON9 (COM1) and CON10 (COM2). The pinout of the 9-pin D-sub connectors depends on the configuration.

Table 2-10: Serial Port Connectors CON9 (COM1) and CON10 (COM2) Pinout

PIN	RS-232 (Standard PC)	RS-422	RS-485
1	DCD	+RXD	NC
2	RXD	NC	NC
3	TXD	+TXD	+TRXD
4	DTR	NC	NC
5	GND	GND	GND
6	DSR	-RXD	NC
7	RTS	NC	NC
8	CTS	-TXD	-TRXD
9	RIN	NC	NC

2.5.6 Serial Port Interfaces COM3 and COM4

Additionally, two PC-compatible serial ports with TTL signal level are available. These two COM ports, which are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer. **The COM3 and COM4 ports are only available on the CompactPCI rear I/O interface**.

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2.5.7 Parallel I/O Interface

The CP605 is provided with an IEEE1284, ECP/EPP-compatible parallel I/O interface. **The parallel I/O interface is only available on the CompactPCI rear I/O**.

2.5.8 Floppy Drive Interface

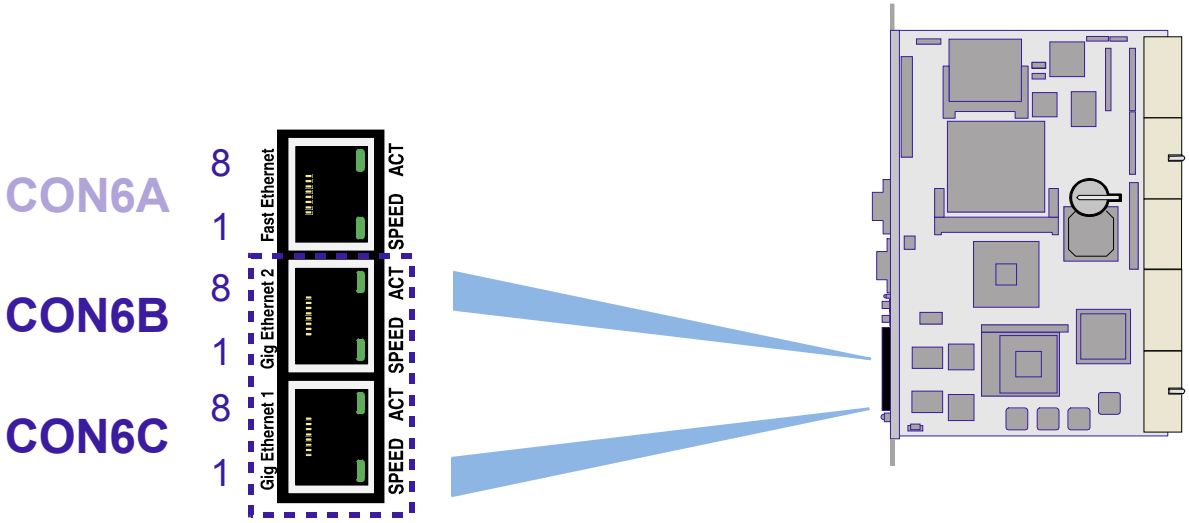
The onboard floppy disk controller supports either 5.25 inch or 3.5 inch (1.44 or 2.88 MB) floppy disks. **The floppy disk port is only available on the CompactPCI rear I/O interface**.

2.5.9 Gigabit Ethernet

The CP605 board includes two 10Base-T/100Base-TX/1000Base-T Ethernet ports based on the Intel 82540EM Gigabit Ethernet PCI Bus Controller. The Intel 82540EM Gigabit Ethernet Controller architecture is optimized to deliver high performance with the lowest power consumption. The controller's architecture includes independent transmit and receive queues to limit PCI bus traffic, and a PCI interface that maximizes the use of bursts for efficient bus usage.

The Boot from LAN feature is supported. For details please refer to Chapter 5.

Figure 2-5: Gigabit Ethernet Connectors CON6B and CON6C



The Ethernet connectors are realized as RJ45 connectors. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission. Auto-wire switching for crossed cables is supported. The two Ethernet channels may be configured via solder jumpers for the rear I/O PICMG 2.16 configuration or front I/O.

Note ...

If the Ethernet channel is configured for PICMG 2.16, the front panel Gigabit connector will have no functionality.

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The CON6B and CON6C connectors supply the 10Base-T, 100Base-TX and 1000Base-T interfaces to the Ethernet controller. The following table indicates the pinout of these connectors.

Table 2-11: Pinouts of CON6B and CON6C Based on the Implementation

MDI / STANDARD ETHERNET CABLE						PIN	MDIX / CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	RX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

2.5.10 Gigabit Ethernet LED Status

Green: ACT: This LED monitors network connection and activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit it means that either the computer is not sending or receiving network data or that the cable connection is faulty.

Green: SPEED: This LED lights up to indicate a successful 1000Base-T connection. When not lit the connection is operating at 100Base-TX or 10Base-T.

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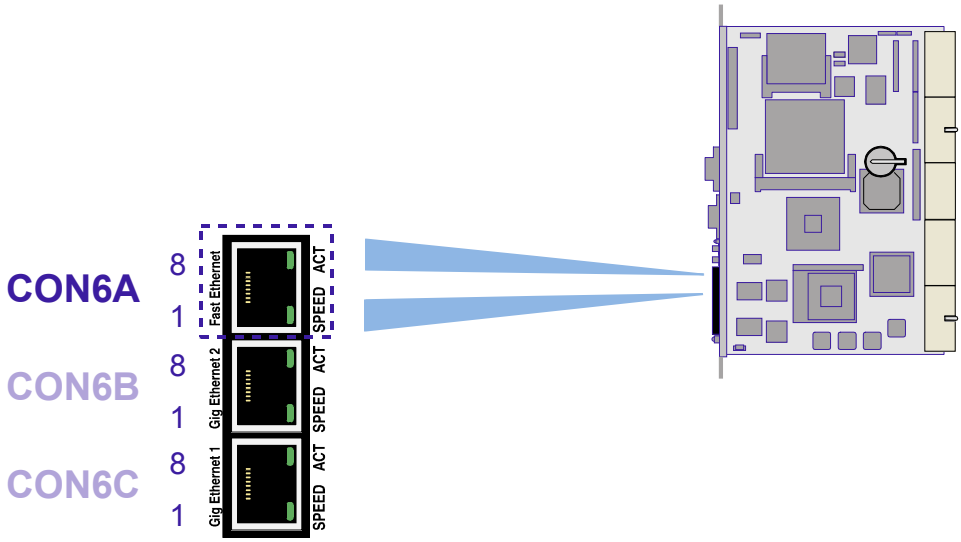
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2.5.11 Fast Ethernet

The CP605 board includes one 10Base-T/100Base-TX Ethernet port integrated within the ICH4 chipset (82559 style).

The Boot from LAN feature is supported; for details please refer to section 5.5, BIOS Features Setup, in chapter 5, CMOS Setup.

Figure 2-6: Fast Ethernet Connector CON6A



The Ethernet connector is realized as an RJ45 connector. The interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission. The Ethernet channel may be configured via the BIOS setting or the rear I/O Configuration Register for front I/O or rear I/O. The standard software configuration is front I/O.

The CON6A connector supplies the 10Base-T/100Base-TX interfaces to the Ethernet controller. The following table indicates the pinout of the RJ45 Connector CON6A.

Table 2-12: RJ45 Connector CON6A Pinout

PIN	SIGNAL	FUNCTION	IN/OUT
1	TX+	Transmit +	Out
2	TX-	Transmit -	Out
3	RX+	Receive +	In
4	NC	--	--
5	NC	--	--
6	RX-	Receive -	In
7	NC	--	--
8	NC	--	--

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2.5.12 Fast Ethernet LED Status

Green: ACT: This LED monitors network connection and activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit it means that either the computer is not sending or receiving network data or that the cable connection is faulty.

Green: SPEED: This LED lights up to indicate a successful 100Base-TX connection. When not lit the connection is operating at 10Base-T.

2.5.12.1 CompactFlash Socket

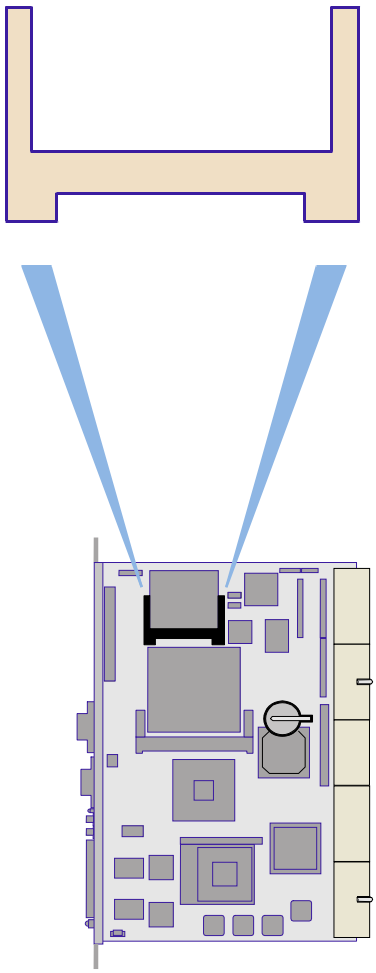
To enable flexible flash extension a CompactFlash (CF) type II socket, CON16, is available.

CF is a very small removable mass storage device. It provides true IDE functionality compatible with the 16 bit ATA/ATAPI-4 interface. CF cards are also available for data storage using the Microdrive hard disk.

The primary EIDE port is connected to the onboard CompactFlash socket.

The board supports both CF types (type I and type II). CompactFlash is available in both CF type I and CF type II cards. The Microdrive is a CF type II card.

Figure 2-7: CompactFlash Socket Connector CON16



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Note ...

The CompactFlash can be configured for Master/Slave operating mode.

The CompactFlash can be configured for 5V/3.3V supply voltage; R266 closed for 5V, R274 closed for 3.3V.

Table 2-13: CompactFlash Connector CON16 Pinout

I/O	FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION	I/O
--	Ground signal	GND	1	2	D03	Data 3	I/O
I/O	Data 4	D04	3	4	D05	Data 5	I/O
I/O	Data 6	D06	5	6	D07	Data 7	I/O
O	Chip select 0	IDE_CS0	7	8	GND (A10)	--	--
--	--	GND (ATASEL)	9	10	GND (A09)	--	--
--	--	GND (A08)	11	12	GND (A07)	--	--
--	5 V power	5 V	13	14	GND (A06)	--	--
--	--	GND (A05)	15	16	GND (A04)	--	--
--	--	GND (A03)	17	18	A02	Address 2	O
O	Address 1	A01	19	20	A00	Address 0	O
I/O	Data 0	D00	21	22	D01	Data 1	I/O
I/O	Data 2	D02	23	24	NC (IOCS16)	--	--
--	--	NC (CD2)	25	26	NC (CD1)	--	--
I/O	Data 11	D11	27	28	D12	Data 12	I/O
I/O	Data 13	D13	29	30	D14	Data 14	I/O
I/O	Data 15	D15	31	32	IDE_CS1	Chip select 1	O
--	--	NC (VS1)	33	34	DIOR	I/O read	O
O	I/O write	DIOW	35	36	5 V (WE)	5 V power	--
I	Interrupt	INTRQ	37	38	5 V	5 V power	--
O	Master/Slave	CSEL (GND pull-up)	39	40	NC (VS2)	--	--
O	Reset	Reset	41	42	IORDY	I/O ready	I
O	Acknowledge	INPACK	43	44	5 V (REG)	5 V power	--
--	--	NC (ACTIVE)	45	46	NC (PDIAG)	--	--
I/O	Data 08	D08	47	48	D09	Data 09	I/O
I/O	Data 10	D10	49	50	GND	--	--

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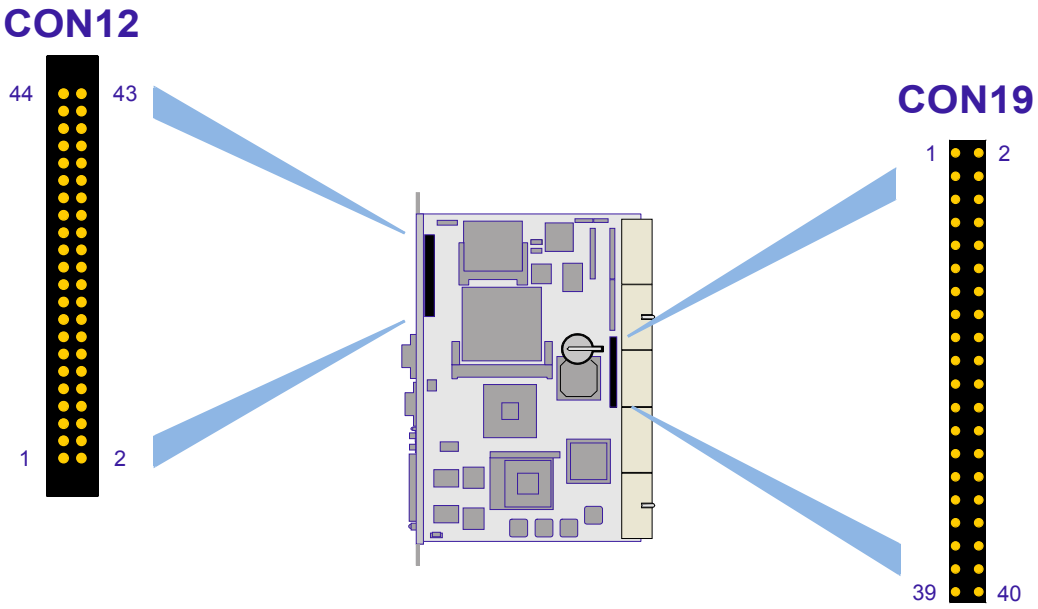
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2.5.13 EIDE Interfaces

The EIDE interface supports the following modes:

- Programmed I/O (PIO): CPU controls data transfer.
- 8237-style DMA: DMA offloads the CPU, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH4 ATA-100 logic can achieve read transfer rates of up to 100 MB/sec and write transfer rates up to 88 MB/sec.

Figure 2-8: EIDE Interface Connectors CON12 and CON19



There are two independent EIDE ports available. The primary port is connected to the optional 44-pin, 2-row male connector, CON12, and to the onboard CompactFlash socket, CON16. The secondary EIDE interface is a 40-pin, 2-row male connector, CON19, AT standard interface for an EIDE hard disk. The secondary port is also connected to the CompactPCI rear I/O interface.

If CON19 is connected to an EIDE device, it is not allowed to connect an EIDE device to the REAR I/O connector CON7 at the same time, and vice versa, if an EIDE device is connected to the REAR I/O connector CON7, CON 19 must not be connected to an EIDE device.

Each EIDE interface provides support for two devices (one master and one slave) and the two EIDE interfaces together, therefore, support a maximum of 4 devices. All hard disks can be used in cylinder head sector (CHS) mode with the BIOS also supporting the logical block addressing (LBA48) mode. LBA48 supports hard disks with a capacity greater than 137 GB.

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Note ...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable will also support all legacy IDE drives.

The blue end of the ATA-100 cable must be connected to the motherboard, the gray connector to the UltraDMA/100 slave device and the black connector to the UltraDMA/100 master device.

2.5.13.1 CON12 — ATA 44-Pin Connector

A 2.5” hard disk or Flash disk may be mounted directly onto the CP605 board using the optional 44-pin connector CON12.

Table 2-14: Pinout of CON12

I/O	FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION	I/O
O	Reset HD	IDERESET	1	2	GND	Ground signal	--
I/O	HD data 7	HD7	3	4	HD8	HD data 8	I/O
I/O	HD data 6	HD6	5	6	HD9	HD data 9	I/O
I/O	HD data 5	HD5	7	8	HD10	HD data 10	I/O
I/O	HD data 4	HD4	9	10	HD11	HD data 11	I/O
I/O	HD data 3	HD3	11	12	HD12	HD data 12	I/O
I/O	HD data 2	HD2	13	14	HD13	HD data 13	I/O
I/O	HD data 1	HD1	15	16	HD14	HD data 14	I/O
I/O	HD data 0	HD0	17	18	HD15	HD data 15	I/O
--	Ground signal	GND	19	20	N/C	--	--
I	DMA request	IDEDRQ	21	22	GND	Ground signal	--
O	I/O write	IOW	23	24	GND	Ground signal	--
O	I/O read	IOR	25	26	GND	Ground signal	--
I	I/O channel ready	IOCHRDY	27	28	GND	Ground signal	--
O	DMA Ack	IDEDACKA	29	30	GND	Ground signal	--
I	Interrupt request	IDEIRQ	31	32	N/C	--	--
O	Address 1	A1	33	34	ATA66	Detect ATA66	I
O	Address 0	A0	35	36	A2	Address 2	O
O	HD select 0	HCS0	37	38	HCS1	HD select 1	O
I	LED driving	LED	39	40	GND	Ground signal	--
--	5V power	VCC	41	42	VCC	5V power	--
--	Ground signal	GND	43	44	N/C	--	--

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2.5.13.2 CON19 — ATA 40-Pin Connector

The following table sets out the pinout of the CON19 connector, giving the corresponding signal names. The maximum length of cable that may be used is 35 cm.

Table 2-15: Pinout of the ATA 40-pin Connector CON19

I/O	FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION	I/O
O	Reset HD	IDERESET	1	2	GND	Ground signal	--
I/O	HD data 7	HD7	3	4	HD8	HD data 8	I/O
I/O	HD data 6	HD6	5	6	HD9	HD data 9	I/O
I/O	HD data 5	HD5	7	8	HD10	HD data 10	I/O
I/O	HD data 4	HD4	9	10	HD11	HD data 11	I/O
I/O	HD data 3	HD3	11	12	HD12	HD data 12	I/O
I/O	HD data 2	HD2	13	14	HD13	HD data 13	I/O
I/O	HD data 1	HD1	15	16	HD14	HD data 14	I/O
I/O	HD data 0	HD0	17	18	HD15	HD data 15	I/O
--	Ground signal	GND	19	20	N/C	--	--
I	DMA request	IDEDRQ	21	22	GND	Ground signal	--
O	I/O write	IOW	23	24	GND	Ground signal	--
O	I/O read	IOR	25	26	GND	Ground signal	--
I	I/O channel ready	IOCHRDY	27	28	GND	Ground signal	--
O	DMA Ack	IDEDACKA	29	30	GND	Ground signal	--
I	Interrupt request	IDEIRQ	31	32	N/C	--	--
O	Address 1	A1	33	34	ATA66	Detect ATA66	I
O	Address 0	A0	35	36	A2	Address 2	O
O	HD select 0	HCS0	37	38	HCS1	HD select 1	O
I	LED driving	LED	39	40	GND	Ground signal	--

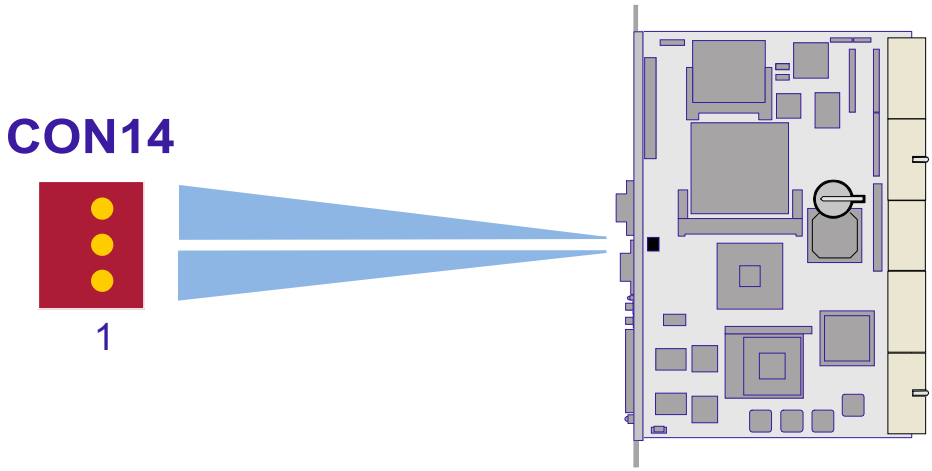
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2.5.14 Fan Power Supply (Optional)

A fan for CPU cooling may be connected via the optional power connector CON14.

Figure 2-9: Fan Power Supply Connector CON14



The following table indicates the pinout of the fan power supply connector CON14.

Table 2-16: Fan Power Supply Connector CON14 Pinout

PIN	SIGNAL	FUNCTION	IN/OUT
1	GND	Signal Ground	--
2	+12V	Power	--
3	Sense input	Sense input	In

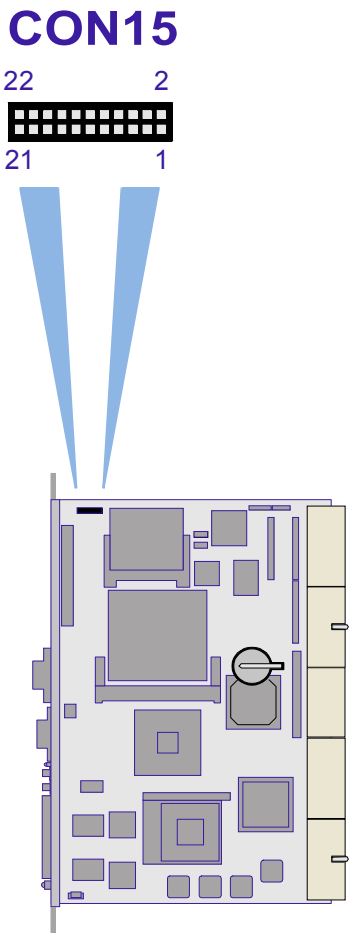
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2.5.15 Extension Connector CON15

The I/O extension connector provides cost-effective, flexible configuration options. To provide flexible configuration of additional low speed PC devices, e.g. Super I/O, IPMI or CAN controller, the LPC port is connected to the I/O extension connector. The I/O extension interface contains all the signals necessary to connect up to two LPC devices.

Figure 2-10: Extension Connector CON15

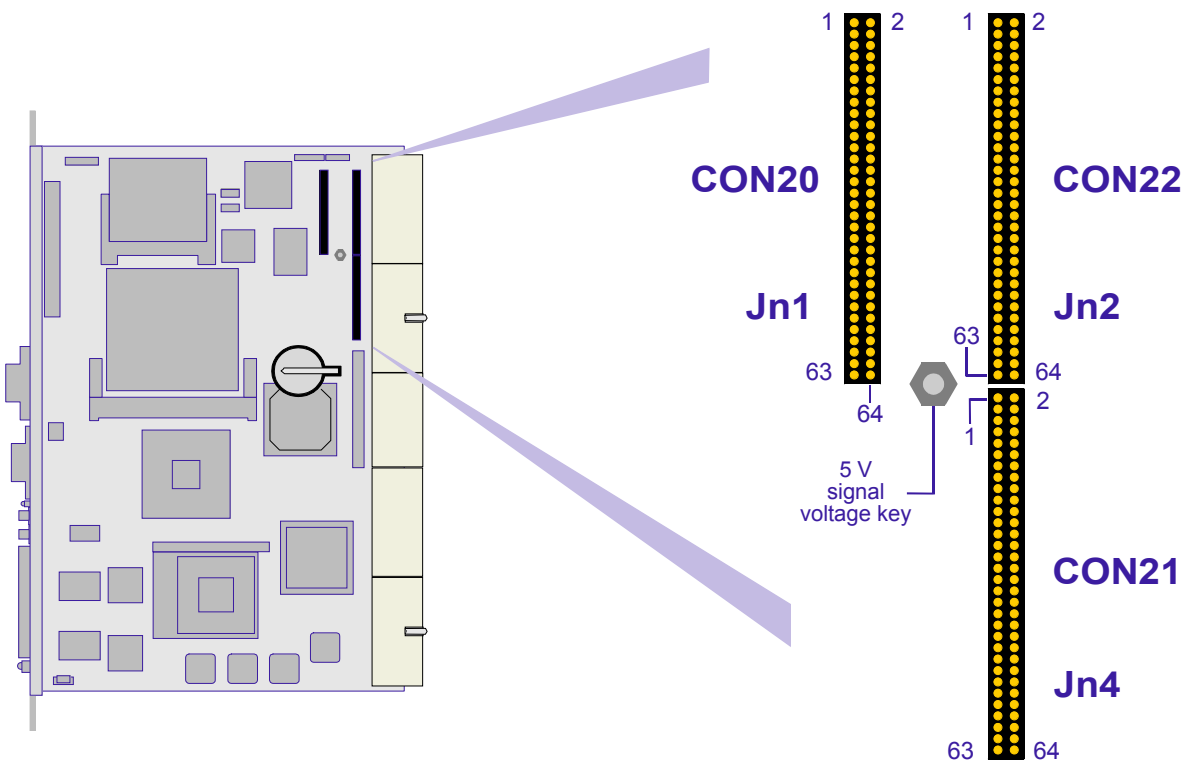


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2.5.16 PMC Interface

Figure 2-11: PMC Connectors CON20, 21 and 22



For flexible and easy configuration one onboard PMC socket is available. The Jn1 and Jn2 connectors provide the signals for the 32-bit PCI Bus. The 64-bit interface for the PMC interface is not implemented. User defined I/O signals are supported (Jn4) and are connected to the CompactPCI rear I/O connector J5.

This interface has been designed to comply with the IEEEP1386.1 specification which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. The CP605 provides a 5V PMC PCI signaling environment.

Note ...

The PMC rear I/O signals from CON21 are routed to CompactPCI connector J5, whose pinout is described later in this chapter.

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The following table indicates the pinout of the PMC connectors CON20 and CON22.

Table 2-17: PMC Connectors CON20 and CON22 Pinouts

Jn1 (CON20)				Jn2 (CON22)			
PIN	SIGNAL NAME	SIGNAL NAME	PIN	PIN	SIGNAL NAME	SIGNAL NAME	PIN
1	Signal	-12V	2	1	+12V	Signal	2
3	Ground	Signal	4	3	Signal	Signal	4
5	Signal	Signal	6	5	Signal	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	Signal	8
9	Signal	Signal	10	9	Signal	Signal	10
11	Ground	Signal	12	11	BUSMODE2#	+3.3V	12
13	Signal	Ground	14	13	Signal	BUSMODE3#	14
15	Ground	Signal	16	15	+3.3V	BUSMODE4#	16
17	Signal	+5V	18	17	Signal	Ground	18
19	V (I/O)	Signal	20	19	Signal	Signal	20
21	Signal	Signal	22	21	Ground	Signal	22
23	Signal	Ground	24	23	Signal	+3.3V	24
25	Ground	Signal	26	25	Signal	Signal	26
27	Signal	Signal	28	27	+3.3V	Signal	28
29	Signal	+5V	30	29	Signal	Ground	30
31	V (I/O)	Signal	32	31	Signal	Signal	32
33	Signal	Ground	34	33	Ground	Signal	34
35	Ground	Signal	36	35	Signal	+3.3V	36
37	Signal	+5V	38	37	Ground	Signal	38
39	Ground	Signal	40	39	Signal	Ground	40
41	Signal	Signal	42	41	+3.3V	Signal	42
43	Signal	Ground	44	43	Signal	Ground	44
45	V (I/O)	Signal	46	45	Signal	Signal	46
47	Signal	Signal	48	47	Ground	Signal	48
49	Signal	+5V	50	49	Signal	+3.3V	50
51	Ground	Signal	52	51	Signal	Signal	52
53	Signal	Signal	54	53	+3.3V	Signal	54
55	Signal	Ground	56	55	Signal	Ground	56
57	V (I/O)	Signal	58	57	Signal	Signal	58
59	Signal	Signal	60	59	Ground	Signal	60
61	Signal	+5V	62	61	Signal	+3.3V	62
63	Ground	Signal	64	63	Ground	Signal	64

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2.5.17 CompactPCI Interface

The CP605 supports a flexibly configurable, hot swap CompactPCI interface. In the System Master slot the bridge is in the transparent mode and in the peripheral slot the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus. This mode is known as the "passive mode".

2.5.17.1 System Master Configuration

In a system slot, the CP605 can communicate with all other CompactPCI boards through a 64-bit, 33 MHz, transparent, PCI-to-PCI bridge from Intel, the 21154.

The 21154 bridge supports up to seven CompactPCI loads through a passive backplane.

The 21154 is fully compliant with the PCI Local Bus Specification Rev. 2.1. The 64-bit interface interoperates transparently with either 64-bit or 32-bit devices.

2.5.17.2 Peripheral Master Configuration (Passive Mode)

In a peripheral slot, the board receives power but does not communicate on the CompactPCI bus; all CompactPCI signals are isolated.

In this configuration the communication is achieved via the two Gigabit Ethernet ports as defined in the PICMG 2.16 specification. In the passive mode the board may be hot-swapped.

2.5.17.3 Packet Switching Backplane (PICMG 2.16)

The CP605 supports a dual Gigabit Ethernet link port (Node) on the J3 connector in accordance with the CompactPCI Packet Switching Backplane Specification PICMG 2.16, Version 1.0. The two nodes are connected in the chassis via the CompactPCI Packet Switching backplane to the Fabric slots "A" and "B".

The PICMG 2.16 feature can be used in the system slot and in the peripheral slot.

2.5.17.4 Hot Swap Support

To ensure that a board may be removed and replaced in a working bus without disturbing the system it requires the following additional features.

- Power ramping
- Precharge
- Hot swap control and status register bits
- Automatic interrupt generation whenever a board is about to be removed or replaced
- An LED to indicate that the board may be safely removed

2.5.17.5 Power Ramping

On the CP605, a special hot swap controller is used to ramp up the onboard supply voltage. This is done to avoid transients on the +3.3V, +5V, +12V and -12V power supplies from the hot swap system. When the power supply is stable, the hot swap controller generates an onboard reset to put the board into a definite state.

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2.5.17.6 Precharge

Precharge is provided on the CP605 by a resistor on each signal line (PCI bus), connected to a +1V reference voltage. If the board is configured in the System Master configuration the reference voltage is disabled.

2.5.17.7 Handle Switch

The CP605 can be delivered with or without an IPMI controller. In both cases a microswitch is situated in the extractor handle and routed to CON13 on the board.

If the CP605 does not have an IPMI controller integrated, a local interrupt produced by the onboard logic is generated when the extractor handle is opened. In addition, the status of the microswitch can be read in the I/O Status 2 Register, table 4-23.

If the CP605 does have an IPMI controller integrated, an IPMI event is initiated when the extractor handle is opened or closed. In addition, the status of the microswitch can be read either in the I/O Status 2 Register, table 4-23 or via the IPMI controller.

2.5.17.8 ENUM# Interrupt

The onboard logic generates a low active interrupt signal to indicate that the board is about to be extracted from the system or inserted into the system. This interrupt is only generated in the peripheral master configuration. In System Master configuration the ENUM signal is an input.

2.5.17.9 Blue LED

On the CP605 without IPMI controller, a blue LED can be switched on or off by software. It may be used, for example, to indicate that the shutdown process is finished and the board is ready for extraction. The blue LED may also be used for general purposes. For information concerning switching on and off the blue LED, refer to table 4-28, LED Control Register.

On the CP605 with IPMI controller, the blue LED can be switched on and off only by the IPMI controller. The blue LED cannot be used for general purposes.

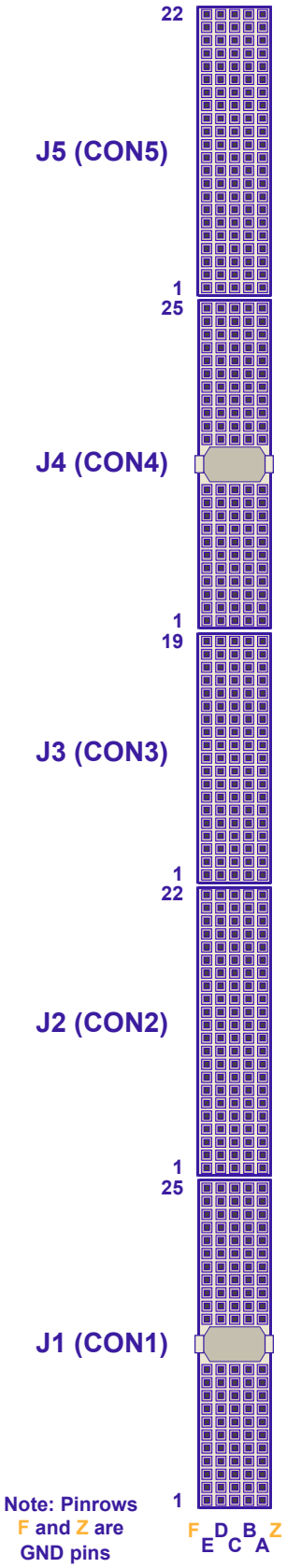
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2.5.18 CompactPCI Bus Connector

Figure 2-12: CompactPCI Connectors J1-J5 (CON1-CON5)



The complete CompactPCI connector configuration comprises five connectors named J1 to J5. Their functions are as follows:

- J1/J2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power.
- J3 and J5 has rear I/O interface functionality.
- J4 only has optional rear I/O interface functionality.

The CP605 is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

2.5.18.1 CompactPCI Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating. A proper mating is further assured by the use of color coded keys for 3.3V and 5V operation.

Color coded keys prevent inadvertent installation of a 5V peripheral board into a 3.3V slot. The CP605 board is a 5V version. Backplane connectors are always keyed according to the signaling (VIO) level. Coding key colors are defined as follows:

Table 2-18: Coding Key Colors

SIGNALING VOLTAGE	KEY COLOR
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	None

To prevent plugging a 5V CP605 version into a 3.3V VI/O backplane slot, a blue key is installed in J1.

To prevent plugging the CP605 into an H.110 backplane slot, a brown key is installed in J4.

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The CP605 is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2. The following table indicates the pinout of these connectors.

Table 2-19: CompactPCI Bus Connector J1 (CON1) System Slot Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN#	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	GND	DEVSEL	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12-14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	NC	AD[23]	GND	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	GND	REQ0#	GND	3.3V	CLK0	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0#	GND
4	GND	IPMB PWR	Healthy#	V(I/O)	INTP	INTS	GND
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND

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Table 2-20: CompactPCI Bus Connector J1 (CON1) Peripheral Slot Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
25	GND	5V	*	ENUM#	3.3V	5V	GND
24	GND	*	5V	V(I/O)	*	*	GND
23	GND	3.3V	*	*	5V	*	GND
22	GND	*	GND	3.3V	*	*	GND
21	GND	3.3V	*	*	M66EN#	*	GND
20	GND	*	GND	V(I/O)	*	*	GND
19	GND	3.3V	*	*	GND	*	GND
18	GND	*	GND	3.3V	*	*	GND
17	GND	3.3V	IPMB SCL	IPMB SDA	GND	*	GND
16	GND	*	GND	V(I/O)	*	*	GND
15	GND	3.3V	*	*	GND	*	GND
12-14	Key Area						
11	GND	*	*	*	GND	*	GND
10	GND	*	GND	3.3V	*	*	GND
9	GND	*	NC	*	GND	*	GND
8	GND	*	GND	V(I/O)	*	*	GND
7	GND	*	*	*	GND	*	GND
6	GND	*	GND	3.3V	*	*	GND
5	GND	BRSVP1A5	BRSVP1B5	*	GND	*	GND
4	GND	IPMB PWR	Healthy#	V(I/O)	INTP	INTS	GND
3	GND	*	*	*	5V	*	GND
2	GND	TCK	5V	TMS	TDO	TDI	GND
1	GND	5V	-12V	TRST#	+12V	5V	GND



Note ...

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP605 is inserted in a peripheral slot.

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Table 2-21: 64-bit CompactPCI Bus Connector J2 (CON2) System Slot Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	RSV	RSV	RSV	GND
20	GND	CLK5	GND	RSV	GND	RSV	GND
19	GND	GND	GND	RSV	RSV	RSV	GND
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	GND	BRSVP2A17	GND	PRST#	REQ6#	GNT6#	GND
16	GND	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND
15	GND	BRSVP2A15	GND	FAL#	REQ5#	GNT5#	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#]	GND	V(I/O)	C/BE[4]#]	PAR64	GND
4	GND	V(I/O)	BRSVP2B4	C/BE[7]#]	GND	C/BE[6]#]	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

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Table 2-22: 64-bit CompactPCI Bus Connector J2 (CON2) Peripheral Slot Pinout

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	*	GND	RSV	RSV	RSV	GND
20	GND	*	GND	RSV	GND	RSV	GND
19	GND	GND	GND	RSV	RSV	RSV	GND
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND
17	GND	BRSVP2A17	GND	PRST#	*	*	GND
16	GND	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND
15	GND	BRSVP2A15	GND	FAL#	*	*	GND
14	GND	*	*	*	GND	*	GND
13	GND	*	GND	V(I/O)	*	*	GND
12	GND	*	*	*	GND	*	GND
11	GND	*	GND	V(I/O)	*	*	GND
10	GND	*	*	*	GND	*	GND
9	GND	*	GND	V(I/O)	*	*	GND
8	GND	*	*	*	GND	*	GND
7	GND	*	GND	V(I/O)	*	*	GND
6	GND	*	*	*	GND	*	GND
5	GND	*	GND	V(I/O)	*	*	GND
4	GND	V(I/O)	BRSVP2B4	*	GND	*	GND
3	GND	*	GND	*	*	*	GND
2	GND	*	*	SYSEN#	*	*	GND
1	GND	*	GND	*	*	*	GND



Note ...

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP605 is inserted in a peripheral slot.

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2.5.18.2 CompactPCI Rear I/O Connectors J3-J5 (CON3-CON5)

The CP605 conducts all I/O signals through the rear I/O connectors J3, J4 and J5. The CP605 board provides optional rear I/O connectivity for peripherals for special compact systems. All standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connectors J3, J4 and J5 (CON3, CON4 and CON5).

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system rear I/O feature a special backplane is necessary. The CP605 with rear I/O is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support on the system slot.

The CP605 conducts all I/O signals through the rear I/O connectors J3, J4 and J5.

The following tables indicates the pinouts of the J3-J5 connectors and their signal descriptions.

Table 2-23: Backplane J3 Pinout

PIN	Z	A	B	C	D	E	F
19	GND	RIO_+2.5 V	reserved	reserved	reserved	SIDEATADET	GND
18	GND	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	GND	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	GND	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	GND	LPb_DB+	LPb_DB-	reserved	LPb_DD+	LPb_DD-	GND
14	GND	reserved	reserved	reserved	reserved	reserved	GND
13	GND	IDERST 8)	SIDEIRQ 8)	SIDEDAK 8)	SIDEICHRDY 8)	SIDEDRQ 8)	GND
12	GND	FDDS0 7)	FDDENSEL1 7)	FDMTR0 7)	FDINDEX 7)	FDWDATA 7)	GND
11	GND	FDDS1 7)	FDDSKCHG 7)	FDMTR1 7)	FD.DENSEL0 7)	FDRDATA 7)	GND
10	GND	FDWP 7)	FDHDSEL 7)	FDDIR 7)	FDTRK0 7)	FDSTEP 7)	GND
9	GND	FDWGATE 7)	SIDED15 8)	SIDED14 8)	SIDED13 8)	USB0+ 2)	GND
8	GND	SIDED12 8)	SIDEIOW 8)	RIO_VCC	SIDEIOR 8)	USB0- 2)	GND
7	GND	SIDEA2 8)	SIDEA1 8)	SIDEA0 8)	SIDED0 8)	SIDED1 8)	GND
6	GND	SIDED2 8)	SIDED3 8)	SIDED4 8)	SIDED5 8)	SIDED6 8)	GND
5	GND	SIDECS0 8)	PMDAT 5)	SPKR 1)	KDAT 5)	SIDECS1 8)	GND
4	GND	PRST 1)	PMCLK 5)	RIO_VCC	KCLK 5)	S3RXD 3)	GND
3	GND	S3CTS 3)	S3RTS 3)	S3DSR 3)	S3DCD 3)	S3TXD 3)	GND
2	GND	SIDED7 8)	SIDED8 8)	S3RIN 3)	S3DTR 3)	S4RXD 4)	GND
1	GND	SIDED9 8)	SIDED10 8)	SIDED11 8)	BATT 1)	S4TXD 4)	GND

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Warning!

The RIO_XXX signals are power supply outputs from the CPU board to supply the RIO board with power and must not be supplied with external power.

Failure to comply with the above may result in damage to your board.

Legend for Backplane J3 Table

Table 2-24: Backplane J3 Signal Functions

SIGNAL	DESCRIPTION
CONTROL SIGNALS	
SPKR 1)	Speaker output signal; TTL level
BATT 1)	Battery input signal for RTC; max. 3.3V
PRST 1)	Reset input signal; TTL level
USB PORT 0	
USB0+/- 2)	USB data differential data signals
SERIAL PORT 3	
S3* 3)	Serial port signals; TTL level
SERIAL PORT 4	
S4* 4)	Serial port signals; TTL level
MOUSE + KEYBOARD	
KDAT 5), KCLK 5)	Keyboard data and clock
PMDAT 5), PMCLK 5)	Mouse data and clock
FD* 7)	Floppy signals
SIDE*8	IDE secondary signals
LPA* LPB*	Gigabit Ethernet Link A Gigabit Ethernet Link B
reserved	Reserved for future use

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Table 2-25: Backplane J4 Pinout

PIN	Z	A	B	C	D	E	F
25	GND	RIO_VCC	reserved	reserved	RIO_+3.3V	RIO_VCC	GND
24	GND	reserved	PD0 1)	INIT 1)	reserved	reserved	GND
23	GND	RIO_+3.3V	reserved	reserved	RIO_VCC	reserved	GND
22	GND	reserved	PD1 1)	reserved	reserved	reserved	GND
21	GND	RIO_+3.3V	reserved	AUTOFD 1)	reserved	J2ALERT 2)	GND
20	GND	reserved	PD2 1)	SLCTIN 1)	J2SCL 2)	J2SDA 2)	GND
19	GND	RIO_+3.3V	PD3 1)	STROBE 1)	reserved	IPMIGPIO2 2)	GND
18	GND	reserved	PD4 1)	reserved	PWM1 2)	PWM0 2)	GND
17	GND	RIO_+3.3V	PD5 1)	BUSY 1)	reserved	TACH_IN3 2)	GND
16	GND	reserved	PD6 1)	reserved	TACH_IN2 2)	TACH_IN1 2)	GND
15	GND	RIO_+3.3V	PD7 1)	ACK 1)	reserved	TACH_IN0 2)	GND
12-14	GND						GND
11	GND	reserved	IPMI VCC 1)	PE 1)	reserved	CONN_ID_DRV 2)	GND
10	GND	reserved	reserved	reserved	ID_XMIT_EN 2)	CONN_ID1 2)	GND
9	GND	reserved	IPMI VCC	SLCT 1)	reserved	CONN_ID0 2)	GND
8	GND	reserved	GND	reserved	XMIT_EN 2)	UART0_RI 2)	GND
7	GND	GND	reserved	ERROR 1)	reserved	UART0_RTS 2)	GND
6	GND	reserved	reserved	reserved	UART0_DCD2)	UART0_CTS 2)	GND
5	GND	GND	GND	reserved	UART0_DOUT 2)	UART0_DIN 2)	GND
4	GND	reserved	GND	reserved	GND	GND	GND
3	GND	reserved	reserved	GND	reserved	reserved	GND
2	GND	reserved	reserved	GND	reserved	reserved	GND
1	GND	RIO_VCC	RIO_-12V	GND	RIO_+12V	RIO_VCC	GND



Warning!

The RIO_XXX signals are power supply outputs from the CPU board to supply the RIO board with power and must not be supplied with external power.

Failure to comply with the above may result in damage to your board.

Legend for Backplane J4 Table

1) Parallel I/O interface signals

2) IPMI control signals

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Table 2-26: Backplane J5 Pinout

PIN	Z	A	B	C	D	E	F
22	GND	PMCR4	PMCR3	PMCR2	PMCR1	PMCR0	GND
21	GND	PMCR9	PMCR8	PMCR7	PMCR6	PMCR5	GND
20	GND	PMCR14	PMCR13	PMCR12	PMCR11	PMCR10	GND
19	GND	PMCR19	PMCR18	PMCR17	PMCR16	PMCR15	GND
18	GND	PMCR24	PMCR23	PMCR22	PMCR21	PMCR20	GND
17	GND	PMCR29	PMCR28	PMCR27	PMCR26	PMCR25	GND
16	GND	PMCR34	PMCR33	PMCR32	PMCR31	PMCR30	GND
15	GND	PMCR39	PMCR38	PMCR37	PMCR36	PMCR35	GND
14	GND	PMCR44	PMCR43	PMCR42	PMCR41	PMCR40	GND
13	GND	PMCR49	PMCR48	PMCR47	PMCR46	PMCR45	GND
12	GND	PMCR54	PMCR53	PMCR52	PMCR51	PMCR50	GND
11	GND	PMCR59	PMCR58	PMCR57	PMCR56	PMCR55	GND
10	GND	RIO_+3.3V	PMCR63	PMCR62	PMCR61	PMCR60	GND
9	GND	reserved	reserved	S1RXD 4)	TDN1 2)	RDN1 2)	GND
8	GND	reserved	reserved	S1TXD 4)	TDP1 2)	RDP1 2)	GND
7	GND	COM2_ENABLE 1)	COM1_ENABLE 1)	S1RTS 4)	USB1+ 3)	RIO_+3.3V	GND
6	GND	S1DTR 4)	S1CTS 4)	S1DSR 4)	S1DCD 4)	S1RIN 4)	GND
5	GND	S2RXD 5)	S2TXD 5)	S2RTS 5)	S2DTR 5)	ROUT 8)	GND
4	GND	S2DSR 5)	S2DCD 5)	S2RIN 5)	S2CTS 5)	HSYNC 8)	GND
3	GND	S4DTR 6)	S4CTS 6)	S4DSR 6)	GPLED 1)	BOUT 8)	GND
2	GND	S4RTS 6)	S4RIN 6)	FANSENSE2 7)	FANPWM 7)	VSYNC 8)	GND
1	GND	S4DCD 6)	RIOPRESENT 1)	FANSENSE1 7)	USB1- 3)	GOUT 8)	GND



Warning!

The RIO_XXX signals are power supply outputs from the CPU board to supply the RIO board with power and must not be supplied with external power.

Failure to comply with the above may result in damage to your board.

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Legend for Backplane J5 Table

Table 2-27: CompactPCI Connector Signal Descriptions

SIGNAL TYPE	DESCRIPTION
ETHERNET 1 (SIGNALS FROM ETHERNET CHIP WITHOUT MAGNETICS)	
TDP1 2)	Ethernet high transmit Data line
TDN1 2)	Ethernet low transmit Data line
RDP1 2)	Ethernet high receive Data line
RDN1 2)	Ethernet low receive Data line
USB PORT	
USB1+/- 3)	USB data differential data signals
SERIAL PORT 1	
S1* 4)	Serial port signals; TTL level
SERIAL PORT 2	
S2* 5)	Serial port signals; TTL level
SERIAL PORT 4	
S4* 6)	Serial port signals; TTL level
CONTROL SIGNALS	
FANPWM 7)	DAC output that can be used to control fan speed; 0V to +1.25V output
FANSENSE1/2 7)	Schmitt Trigger fan tachometer inputs; TTL level
COM1_ENABLE 1)	Serial port 1 enable signal for front I/O and rear I/O Low = Front I/O High = Rear I/O
COM2_ENABLE 1)	Serial port 2 enable signal for front I/O and rear I/O Low = Front I/O High = Rear I/O
GPLED 1)	General purpose LED output (TH/GP or LED2, depending on configuration, see table 4-24, I/O Configuration Register)
RIOPRESENT 1)	Low = rear I/O module is present High = rear I/O module is not present This signal must be set on the rear I/O module to GND
VGA CRT SIGNALS	
ROUT 8)	Red signal
GOUT 8)	Green signal
BOUT 8)	Blue signal
HSYNC 8)	Horizontal Sync.
VSYNC 8)	Vertical Sync.
PMC REAR I/O SIGNALS	PMCR0 to PMCR63 (Spec.) carry the signals from PMC rear I/O connector CON21 pins 1 to 64

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2.5.18.3 Rear I/O Configuration

Rear I/O interfaces are only available on the rear I/O version of the board.

Ethernet Interfaces

The Fast Ethernet interface is available on the front panel at CON6A and on the rear I/O interface.

The combination of both front and rear I/O is not supported. The Fast Ethernet channel is decoupled, but enabled separately. It is not possible to operate both the rear and front I/O at the same time. Switching over from front to rear I/O or vice versa is effected under BIOS control without the need to plug/unplug Ethernet cables.

Gigabit Ethernet signals are available on the front panel connector and on the rear I/O interface (PICMG 2.16 pinout). Configuration of the Gigabit Ethernet ports for rear I/O requires the installation of zero ohm resistors on the board in order to connect the signals to the J3 connector.

VGA CRT Interface

The VGA signals are available on both rear I/O and front I/O. In this configuration both interfaces are active. The 75 ohm termination resistor for the red, green and blue video signals are equipped on the CP605

To enable the rear I/O port, the installation of zero ohm resistors is necessary.



Note ...

Both VGA ports are electrically identical and not separated. Do not connect devices at both connectors (front I/O and rear I/O) at the same time.

Serial Interfaces COM1 and COM2

Only one interface may be used (rear I/O or front I/O). If the rear I/O interface is enabled, the RS-232, RS-485, RS-422 drivers for the COM1 and COM2 port on the front I/O must be disabled. The configuration can be accomplished via the BIOS.

Serial Interfaces COM3 and COM4

The serial interfaces COM3 and COM4 are only available via the rear I/O.

Parallel I/O Interface

The Parallel I/O Interface is only available via the rear I/O. In order to use the Parallel I/O Interface as LPT interface, additional termination resistors (pull-up resistors) are required.

Keyboard/Mouse Interface

The keyboard interface is available onboard and via the rear I/O. The combination of the onboard and the rear I/O is not supported. The mouse interface is only available via the rear I/O.

USB Interface

The two USB 1.1 interfaces are available only via the rear I/O.

Secondary EIDE Interface

Only one EIDE connector may be used at any one time through the same port; connecting both EIDE devices to the CP605 baseboard and the rear I/O simultaneously will result in malfunction and data loss.

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Floppy Interface

The floppy interface is only available via the rear I/O.

2.6 Intelligent Platform Management Interface (IPMI)

2.6.1 Technical Background of IPMI

The CP605 has been designed to support the "Intelligent Platform Management Interface" (IPMI) subsystem which is another step in providing high availability platforms. Intelligent Platform Management means monitoring the health of the entire system beyond the confines of the board itself, so that the status of the complete system is available to be used, for example, for control and intervention purposes. A range of variables is monitored on every board, to provide information on the system status, e.g. voltages, temperature, powergood signals, reset signals etc. Additionally, the IPMI Baseboard controller can intervene, regulating the operating status of the system by controlling fans, shutting down systems and generating alarm signals as and when fault conditions occur. These fault conditions are simultaneously logged in non-volatile memory for analysis and for fault recovery. IPMI also defines a protocol (software stack) for exchanging the status messages of the board, so that "IPMI ready" boards/systems from different suppliers can be monitored. In addition, a clear interface (registers, addresses etc.) is defined for guaranteeing that System Management software can work with every compliant IPMI hardware.

The electrical interconnection between IPMI capable boards is an I²C interface (IPMB). On CompactPCI systems, this interface is provided on IPMI prepared backplanes and guarantees the data path between the boards.

The devices which handle the measurements and the protocol stack are microcontrollers which are named Baseboard Management Controller (BMC) and Peripheral Management Controller (PM) depending on their position in a CompactPCI backplane. The IPMI microcontroller which is on the System Master board in a CompactPCI system is called BMC and the IPMI controller which is on a Peripheral board is named PM.

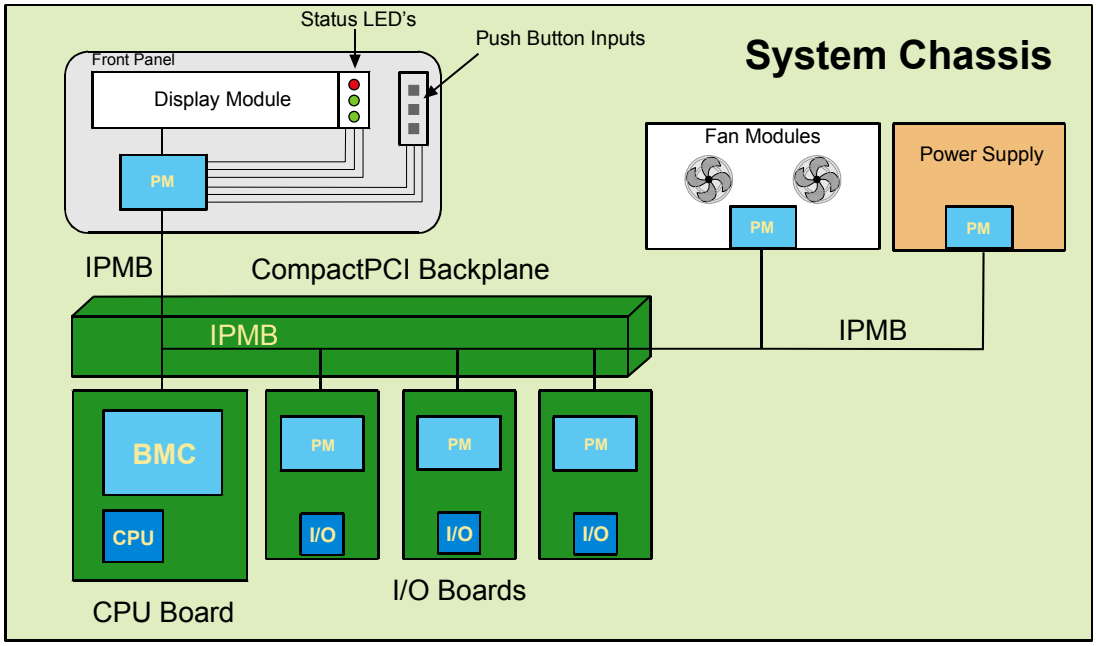
The interface between the system controller CPU’s System Management software and the BaseBoard Management Controller can be realized in two different ways, a keyboard controller style interface (KCS) or a block transfer interface (BT) which can be found in the System Master’s I/O space.

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Figure 2-13: IPMI Functional Block Diagram



2.6.2 IPMI Implementation on the CP605

On the CP605, the IPMI functionality is realized using the ZIRCON-Lite controller from QLogic, which is an ARM7TDMI core-based IPMI controller. Due to the fact that this controller can act as BMC and as PM on all versions of the CP605, the same controller can be used. All the information collected by the ZIRCON-Lite is then accessible by software through a keyboard-style Interface (see IPMI-Intelligent Platform Management Interface Specification V.1.0 for more information) whose address space is available in the I/O space of the Intel CPU's address map, or via the IPMB-Bus.

2.6.3 Measurement of Onboard Voltages

On the CP605 all voltages are monitored by the ZIRCON-Lite. This means 5V, 3.3V, 2.5V, VCORE, VIO, 12V and -12V.

2.6.4 Measurement of Temperatures

An onboard sensor measures the temperature in the vicinity of the CPU (positioned below the heat sink).

2.6.5 Fan Control

Four Tacho inputs and two PWM outputs are routed to the rear I/O connector. These make it possible to control the fan speed to regulate system cooling.

2.6.6 Data Repositories

All the data gathered by the BMC is stored in a non-volatile memory providing the possibility to obtain information about working conditions and failure situations.

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Chapter 3

Installation

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3. Installation

The CP605 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the CP605. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.



Caution!

If your board type is not specifically qualified as being hot swap capable, switch off the CompactPCI system power before installing the board in a free CompactPCI slot. Failure to do so could endanger your life or health and may damage your board or system.



Note ...

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.



ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

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3.2 CP605 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP605 in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the CP605 in a system proceed as follows:

1. Ensure that the safety requirements indicated Chapter 3.1 are observed.



Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP605 refer to Chapter 4. For the installation of CP605 specific peripheral devices and rear I/O devices refer to the appropriate chapters in Chapter 3.



Warning!

Care must be taken when applying the procedures below to ensure that neither the CP605 nor other system boards are physically damaged by the application of these procedures.

3. To install the CP605 perform the following:
   1. Ensure that no power is applied to the system before proceeding.



Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
   3. Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
   4. Fasten the two front panel retaining screws.
   5. Connect all external interfacing cables to the board as required.
   6. Ensure that the board and all required interfacing cables are properly secured.

4. The CP605 is now ready for operation. For operation of the CP605, refer to appropriate CP605 specific software, application, and system documentation.

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3.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!



Warning!

Care must be taken when applying the procedures below to ensure that neither the CP605 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Dispose of the board as required.

3.4 Hot Swap Procedures

The CP605 is designed for hot swap operation. When installed in the system slot it is capable of supporting peripheral board hot swapping. When installed in a peripheral slot, its hot swap capabilities depend on the type of backplane in use and the system controller's capabilities. The reason for this being that communications with the system controller requires either front panel Ethernet I/O or use of a packet switching backplane. In any event, hot swap is also a function of the application running on the CP605.

3.4.1 System Master Hot Swap

Hot swapping of the CP605 itself when used as the system controller is possible, but will result in any event in a cold start of the CP605 and consequently a reinitialization of all peripheral boards. Exactly what transpires in such a situation is a function of the application and is not addressed in this manual. The user must refer to appropriate application documentation for applicable procedures for this case. In any event, the safety requirements above must be observed.

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3.4.2 Peripheral Hot Swap Procedure

This procedure assumes that the board to be hot swapped has undergone an initial board installation and is already installed in an operating system, and that the system supports hot swapping of the board.

To hot swap the CP605 proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!



Warning!

Care must be taken when applying the procedures below to ensure that neither the CP605 nor other system boards are physically damaged by the application of these procedures.

2. Unlock both board ejection handles ensuring that the bottom handle has activated the hot swap switch (this occurs with a very small amount of movement of the handle).



Note ...

What transpires at this time is a function of the application. If hot swap is supported by the application, then the blue HS LED should light up after a short time period. This indicates that the system has recognized that the CP605 is to be hot swapped and now indicates to the operator that hot swapping of the CP605 may proceed.

If the blue HS LED does not light up after a short time period, either the system does not support hot swap or a malfunction has occurred. In this event, the application is responsible for handling this situation and must provide the operator with appropriate guidance to remedy the situation.

3. After approximately 1 to 15 seconds, the blue HS LED should light up. If the LED lights up, proceed with the next step of this procedure. If the LED does not light up, refer to appropriate application documentation for further action.
4. Disconnect any interfacing cables that may be connected to the board.
5. Unscrew the front panel retaining screws.



Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

6. Using the ejector handles, disengage the board from the backplane and carefully remove it from the system.
7. Dispose of the “old” board as required observing the safety requirements indicated in Chapter 3.1.

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8. Obtain the replacement CP605 board.



Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

9. Carefully insert the “new” board into the “old” board slot until it makes contact with the backplane connectors.
10. Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
11. Fasten the front panel retaining screws.
12. Connect all required interfacing cables to the board. Hot swap of the CP605 is now complete.

3.5 Installation of CP605 Peripheral Devices

The CP605 is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following chapters provide information regarding installation aspects and not detailed procedures.

3.5.1 CompactFlash Installation

The CompactFlash socket supports all available CompactFlash ATA cards type I and type II with 3.3V.



Note ...

The CP605 does not support removal and reinsertion of the CompactFlash storage card while the board is in a powered-up state. Connecting the CompactFlash cards while the power is on, which is known as "hot plugging", may damage your system.

3.5.2 USB Device Installation

The CP605 supports all USB Plug & Play computer peripherals (e.g. keyboard, mouse, printer, etc.).



Note ...

All USB devices may be connected or removed while the host or other peripherals are powered up.

3.5.3 Rear I/O Device Installation

To ensure proper functioning of the rear I/O serial interfaces, the drivers for the COM1 and COM2 ports must be disabled via software.

Using the Fast Ethernet port on the Rear I/O the interface can be re-routed via a BIOS software switch.

To ensure proper functioning of the rear I/O VGA interface and the Gigabit Ethernet ports, the solder jumpers on the CP605 must be configured for the rear I/O. See Chapter 4 for configuration details.

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For physical installation of rear I/O devices, refer to the documentation provided with the device itself.

3.5.4 Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. Suitable batteries include the VARTA CR2025 and PANASONIC BR2020



Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

The typical life expectancy of a 170 mAh battery (VARTA CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 4 - 5 years.

3.5.5 Hard Disk Installation

The following information pertains to hard disks which may be connected to the CP605 via normal cabling. To install a hard disk, it is necessary to perform the following operations in the given order:

1. Install the hardware.



Warning!

The incorrect connection of power or data cables may damage your hard disk unit and/or CP605 board.

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Note...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable will also support all legacy IDE drives.

The blue end of the ATA-100 cable must connect to the motherboard, the gray connector to the UltraDMA/100 slave device, and the black connector to the UltraDMA/100 master device.

Some symptoms of incorrectly installed HDDs are:

- Hard disk drives are not auto-detected: may be a Master / Slave problem or a bad IDE cable. Contact your vendor.
- Hard Disk Drive Fail message at bootup: may be a bad cable or lack of power going to the drive.
- No video on bootup: usually means the cable is installed backwards.
- Hard drive lights are constantly on: usually means bad IDE cable or defective drives / motherboard. Try another HDD.
- Hard drives do not power up: check power cables and cabling. May also result from a bad power supply or IDE drive.

2. Initialize the software necessary to run the chosen operating system.

3.6 Software Installation

The installation of the Ethernet and all other onboard peripheral drivers is described in detail in the relevant Driver Kit files.

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.



Note ...

Users working with pre-configured operating system installation images for Plug and Play compliant operating systems, for example Windows® 95/98/ME, Windows® 2000, Windows® XP, Windows® XP Embedded, must take into consideration that the stepping and revision ID of the chipset and/or other onboard PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the Plug and Play configuration rules.

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Chapter 4

Configuration

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4. Configuration

4.1 Jumper Description

4.1.1 Processor Configuration

The CP605 supports all Intel Pentium 4 and Mobile Pentium 4 Processor-M processors. Due to the different core voltages of the two processors the onboard DC/DC converter must be configured via jumper J8.

Table 4-1: Processor Configuration

J8	PROCESSOR TYPE
Open	Pentium 4 support
Closed	Pentium 4-M support



Note ...

If the jumper setting is incorrect, the board will not function.

4.1.2 CompactFlash Configuration

Table 4-2: CompactFlash Configuration

J100 or R72	DESCRIPTION
Closed	Configured for slave
Open	***Configured for master***

The default setting is indicated by using italic bold.

4.1.3 Dual BIOS Configuration

Dual BIOS means that there are two chips for the BIOS on the CP605 board (BIOS Flash and the User Flash). One chip is intended to provide a backup in the event that the other gets corrupted. These chips are soldered to the board.

If the primary BIOS is corrupted due to physical damage or a faulty flash upgrade, the solder jumper J6 should be set and the system switched over to the secondary chip and booted with default settings.

Table 4-3: Dual BIOS Configuration

J6	DESCRIPTION
Open	***Normal boot from the on-board BIOS***
Closed	Boot from the second BIOS chip

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The default setting is indicated by using italic bold.



Note ...

The Dual BIOS feature cannot be used if the second Flash chip is used for booting VxWorks®.

4.1.4 Clearing BIOS CMOS Setup

If the system does not boot (due to, for example, the wrong BIOS configuration or incorrect password setting) the CMOS setting may be cleared using jumper J5.

Procedure for clearing CMOS setting:

The system is booted with the jumper in the new, closed position, then powered down again. The jumper is reset back to the normal position, then the system is rebooted.

Table 4-4: Clearing BIOS CMOS Setup

J5	DESCRIPTION
Open	***Normal boot using the CMOS settings***
Closed	Clear the CMOS settings and use the default values

The default setting is indicated by using italic bold.

4.1.5 Shorting Chassis GND (Shield) to Logic GND

The front panel and front panel connectors are isolated to the logic ground.

To enable the connection between the chassis GND and logic GND the capacitors must be exchanged with zero ohm resistors.

Table 4-5: Shorting Chassis GND (Shield) to Logic GND

CAPACITOR	SETTING	DESCRIPTION
C103, C104, C107, C114	***Closed 470pF 2KV capacitors***	***Connectors are isolated to logic GND with four 470pF 2KV capacitors***
	Closed zero ohm resistors	Connectors are connected to logic GND and chassis GND

The default setting is indicated by using italic bold.

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4.1.6 VGA CRT Rear I/O Configuration

The VGA CRT signals are available on the rear I/O and on the front I/O. To configure the VGA CRT port for rear I/O requires the installation of zero Ohm resistors on the board to connect the signals to the rear I/O connector J3.

Table 4-6: VGA-CRT Jumper Setting

RESISTORS R303, R310, R324	DESCRIPTION
Open	***Only front I/O***
Closed	Front I/O and rear I/O

The default setting is indicated by using italic bold.



Note ...

Both VGA ports are electrically identical and not separated. Do not connect devices at both connectors (front I/O and rear I/O) at the same time.

4.1.7 PICMG 2.16 Rear I/O Configuration

The Gigabit Ethernet signals are available on the rear I/O and the front I/O. To configure the two Ethernet ports for rear I/O requires the installation of zero Ohm resistors on the board to connect the signals to the rear I/O connector.

4.1.7.1 PIGMG 2.16 Rear I/O Configuration for Port 1

Table 4-7: PICMG 2.16 Rear I/O Configuration for Port 1

CONFIGURATION	FRONT I/O	REAR I/O
R95, R106 R123, R133 R145, R154 R164, R172	Closed	Open
R96, R107 R124, R134 R146, R155 R173, R177	Open	Closed



Note ...

The simultaneous operation of the Gigabit Ethernet Port 1 via the front and rear I/O ports is not supported.

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4.1.7.2 PICMG 2.16 Rear I/O Configuration for Port 2

Table 4-8: PICMG 2.16 Rear I/O Configuration for Port 2

CONFIGURATION	FRONT I/O	REAR I/O
R91, R103 R121, R130 R142, R152 R163, R170	Closed	Open
R92, R105 R122, R131 R143, R153 R171, R176	Open	Closed



Note ...

The simultaneous operation of the Gigabit Ethernet Port 2 via the front and rear I/O ports is not supported.

4.1.8 Serial Port Jumper and Resistor Setting

4.1.8.1 COM1 Jumper and Resistor Setting

The serial interfaces CON9 (COM1) and CON11 (COM2) on the CP605 may be configured for either RS-232, RS-422 or RS-485 by setting solder jumpers.

Table 4-9: Resistor Setting to Configure COM1

Resistor	RS-232	RS-422	RS-485
R137	***Open***	Closed	Closed
R126	***Open***	Open	Closed
R108	***Closed***	Closed	Open
R149	***Open***	Closed	Open

The default setting is indicated by using italic bold.



Note ...

The serial port may be disabled by the BIOS.

RS-422 and RS-485 COM1 Termination

When the CP605 is using the onboard RS-485 interface and is the last device on the RS-422 or RS-485 bus, then the RS-422 or RS-485 interface must provide termination resistance. The purpose of jumpers J1 and J2 is to enable this line termination resistor (120 R).

The default setting is indicated by using italic bold.

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Table 4-10: Jumper Setting for RS-422 RXD Termination (COM1)

TERMINATION	J2
ON	Closed
OFF	***Open***

Table 4-11: Jumper Setting for RS-422 TXD and RS-485 Termination (COM1)

TERMINATION	J1
ON	Closed
OFF	***Open***

The default setting is indicated by using italic bold.

4.1.8.2 COM2 Jumper and Resistor Setting

Table 4-12: Resistor Setting to Configure COM2

Resistor	RS-232	RS-422	RS-485
R128	***Open***	Closed	Closed
R167	***Open***	Open	Closed
R168	***Closed***	Closed	Open
R115	***Open***	Closed	Open

The default setting is indicated by using italic bold.

RS-422 and RS-485 COM2 Termination

When the CP605 is using the onboard RS-485 interface and is the last device on the RS-422 or RS-485 bus, then the RS-422 or RS-485 interface must provide termination resistance. The purpose of jumpers J3 and J4 is to enable this line termination resistor (120 R).

Table 4-13: Jumper Setting for RS-422 RXD Termination (COM2)

TERMINATION	J4
ON	Closed
OFF	***Open***

The default setting is indicated by using italic bold.

Table 4-14: Jumper Setting for RS-422 TXD and RS-485 Termination (COM2)

TERMINATION	J3
ON	***Closed***
OFF	Open

The default setting is indicated by using italic bold.

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4.1.9 Reserved Jumpers

The J7 jumper is reserved for future configurations.

4.2 Interrupts

The CP605 board uses the standard AT IRQ routing (8259 controller).

This interrupt routing is the default, but can be modified via the BIOS.

Table 4-15: Interrupt Setting

IRQ	PRIORITY	STANDARD FUNCTION
IRQ0	1	System Timer
IRQ1	2	Keyboard Controller
IRQ2	--	Input of the second IRQ controller (IRQ8-IRQ15)
IRQ3	11	COM2
IRQ4	12	COM1
IRQ5	13	Watchdog
IRQ6	14	Floppy Disk Controller
IRQ7	15	Free reserved for COM3 or COM4
IRQ8	3	System Real Time Clock
IRQ9	4	PCI or ACPI
IRQ10	5	PCI
IRQ11	6	PCI
IRQ12	7	PCI or PS/2 mouse
IRQ13	8	Coprocessor error
IRQ14	9	Primary hard disk
IRQ15	10	Secondary hard disk
NMI	--	Watchdog



Warning!

IRQ5 should normally have only **one** source enabled, otherwise improper system operation may result.

If more than one source is required to be enabled, contact Kontron's Technical Support before implementing the IRQs.

For events that are not time critical, such as ENUM, DERATE, etc., polling should be considered instead of using an IRQ.

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4.3 Onboard PCI Interrupt Routing

The ICH4 provides up to 8 PCI interrupt inputs. The table below describes the connection of these IRQ signals:

Table 4-16: PCI Interrupt Routing

ICH4 IRQ INPUT	PCI DEVICE	FUNCTION INTERNAL ICH4
PIRQA	PCI to PCI Bridge IRQA	USB 1 controller
PIRQB	PCI to PCI Bridge IRQB	AC97 + MODEM + SMBUS
PIRQC	PCI to PCI Bridge IRQC	USB 2 controller
PIRQD	PCI to PCI Bridge IRQD	USB 3 controller
PIRQE	PMC IRQB	LAN controller IRQA
PIRQF	PMC IRQC + Gigabit Ethernet	free
PIRQG	PMC IRQD + Gigabit Ethernet	free
PIRQH	PMC IRQA + Security	USB 2.0 controller

For more information please see the INTEL ICH4 data sheet.

4.4 Memory Map

The CP605 board uses the standard AT ISA memory map.

4.4.1 Memory Map for the 1st Megabyte

The following table sets out the memory map for the first megabyte:

Table 4-17: Memory Map for the 1st Megabyte

MEMORY RANGE	SIZE	FUNCTION
0xE0000 – 0xFFFFF	128 k	BIOS implemented in FWH Reset vector 0xFFFF0
0xD0000 – 0xDFFFF	64 k	Free
0xCC000 – 0xCFFFF	16 k	Free
0xC0000 – 0xCBFFF	48 k	BIOS of the VGA card.
0xA0000 – 0xBFFFF	128 k	Normally used as video RAM as follows: CGA video: 0xB8000-0xBFFFF Monochrome video: 0xB0000-0xB7FFF EGA/VGA video: 0xA0000-0xAFFFF
0x000000 – 0x9FFFF	640 k	DOS reserved memory space

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4.4.2 I/O Address Map

The following table sets out the memory map for the I/O memory:

Table 4-18: I/O Address Map

ADDRESS	DEVICE
000,00F	DMA controller #1
020,021	Interrupt controller #1
022,02F	Reserved
040,043	Timer
060,063	Keyboard interface
070,071	RTC port
080,08F	DMA page register
0A0,0A	Interrupt controller #2
0C0,0DF	DMA controller #2
0E0,0EF	Reserved
0F0,0FF	Math coprocessor
170,17F	Hard disk secondary
1F0,1FF	Hard disk primary
278,27F	Parallel port LPT2
280	Watchdog trigger
282	Watchdog timer
284	Watchdog, CPCI IRQ routing
286	I/O status 1
287	I/O configuration
288	Board version
289	Hardware index
28A	I/O status 2
28B	Logic index
28D	LED control
2E8,2EF	Serial port COM4
2F8,2FF	Serial port COM2
378,37F	Parallel printer port LPT1
3BC,3BF	Parallel printer port LPT3
3E8,3EF	Serial port COM3
3F0,3F7	Floppy Disk + Super-I/O #1 Com.
3F8,3FF	Serial port COM1



Note ...

The yellow (shaded on a printout) table cells indicate CP605-specific registers.

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4.5 Special Registers Description

The following registers are special registers which the CP605 uses to watch the onboard hardware special features and the CompactPCI control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required.



Note ...

Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

4.5.1 Watchdog

The CP605 has one watchdog timer. This timer is provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to strobe the watchdog timer within a set time period results in a system reset, NMI or an interrupt. This can be configured via the register 0x284.

To enable the watchdog, bit ”4” of the register 0x282 must be set. If the watchdog is enabled via bit ”4” this bit cannot later be cleared.

With a write access to the register 0x280 the watchdog is retriggered. Once the watchdog is enabled, it must be continuously strobed within the terminal count period to avoid resetting the system hardware.

The watchdog can be configured in several modes, one of which is the dual stage configuration. If the NMI and the reset configuration bit are set (0x284 = 0x84) the watchdog has two stages. The first stage timeout generates an NMI interrupt. If the NMI handler does not reconfigure the watchdog, the watchdog switches to the second stage and generates a master reset after the configured timeout elapses.

4.5.2 Watchdog Trigger

A write access triggers the watchdog.

The I/O location for the watchdog trigger is 0x280.

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4.5.3 Watchdog Timer

Table 4-19: Watchdog Timer

REGISTER NAME		WATCHDOG TIMER						ACCESS	
ADDRESS		0x282						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	WDEN	WDT3	WDT2	WDT1	WDT0
DEFAULT		0	0	0	0	0	0	0	0

BIT	NAME	VAL	DESCRIPTION
0 1 2 3	WDT[3:0]		Timeout Period: Bits: 3 2 1 0 Setting: 0 0 0 0 = 0 = 000.125 sec 0 0 0 1 = 1 = 000.250 sec 0 0 1 0 = 2 = 000.500 sec 0 0 1 1 = 3 = 001 sec 0 1 0 0 = 4 = 002 sec 0 1 0 1 = 5 = 004 sec 0 1 1 0 = 6 = 008 sec 0 1 1 1 = 7 = 016 sec 1 0 0 0 = 8 = 032 sec 1 0 0 1 = 9 = 064 sec 1 0 1 0 = 10 = 128 sec 1 0 1 1 = 11 = 256 sec 1 1 0 0 = 12 = res. 1 1 0 1 = 13 = res. 1 1 1 0 = 14 = res. 1 1 1 1 = 15 = res.
4	WDEN	0	Watchdog timer disabled
		1	Watchdog timer enabled ***Note ...*** Once the watchdog timer is enabled it cannot be disabled except by resetting the system.
5	WDR	0	System reset has been generated by power-on reset
		1	Reset generated by Watchdog
6		0	Reserved
7		0	Reserved

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4.5.4 Watchdog, CompactPCI Interrupt Configuration Register

The interrupt configuration register holds a series of bits defining the interrupt routing for the watchdog, the power control derate signal and the CompactPCI enumeration signal. If the watchdog timer fails, it can generate three independent hardware events: reset, NMI and IRQ5 interrupt.

The enumeration signal is generated by a hot swap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board. The derate signal indicates that the power supply is beginning to derate its power output.



Note ...

To enable the dual stage watchdog the NMI and the reset bit must be set. At the first stage the watchdog generates an NMI and at the second stage the system will be reset.

Table 4-20: Watchdog, CompactPCI Interrupt Configuration Register

REGISTER NAME		INTERRUPT CONFIGURATION REGISTER						ACCESS	
ADDRESS		0x284						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WNMI	CFNMI	CFIRQ	CEIRQ	CDIRQ	WRST	WIRQ	HSIRQ
DEFAULT		0	0	0	0	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	HSIRQ	0	Disable hot swap handle IRQ5 routing						
		1	Enable hot swap handle IRQ5 routing						
1	WIRQ	0	Disable Watchdog IRQ5 routing						
		1	Enable Watchdog IRQ5 routing						
2	WRST	0	Disable Watchdog hardware reset						
		1	Enable Watchdog hardware reset						
3	CDIRQ	0	Disable CPCI derate signal to IRQ5 routing						
		1	Enable CPCI derate signal to IRQ5 routing						
4	CEIRQ	0	Disable CPCI enum signal to IRQ5 routing						
		1	Enable CPCI enum signal to IRQ5 routing						
5	CFIRQ	0	Disable CPCI fail signal to IRQ5 routing						
		1	Enable CPCI fail signal to IRQ5 routing						
6	CFNMI	0	Disable CPCI fail signal to NMI routing						
		1	Enable CPCI fail signal to NMI routing						
7	WNMI	0	Disable Watchdog NMI routing						
		1	Enable Watchdog NMI routing						

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4.5.5 I/O Status 1 Register

This register describes the local and CompactPCI control signals. The watchdog status bit indicates the status of the watchdog timer. If the timer is not retriggered within the previously set time period, the bit is set to ”0” and the watchdog LED lights. The fail signal is an output of the power supply and indicates a power supply failure. For the description of the derate and enumeration signals please see the Interrupt Routing Register.

Table 4-21: I/O Status 1 Register

REGISTER NAME		I/O STATUS 1 REGISTER						ACCESS	
ADDRESS		0x286						R	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WST	Res.	Res.	Res.	CSLOT	CENUM	CFAIL	CDER
DEFAULT		1	0	0	0	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	CDER	0	Indicates power derating (CPCI DEG signal)						
		1	Power normal						
1	CFAIL	0	Indicates a power supply failure (CPCI FAIL signal)						
		1	Power normal						
2	CENUM	0	Indicates the insertion or removal of a hot swap system board (CPCI ENUM)						
		1	No hot swap event						
3	CSLOT	0	Indicates that the board is installed in a system slot						
		1	Indicates that the board is installed in a peripheral slot						
4		0	Reserved						
5		0	Reserved						
6		0	Reserved						
7	WST	0	Indicates that a Watchdog timeout has occurred						
		1	Indicates that no Watchdog timeout has occurred						

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4.5.6 I/O Status 2 Register

Table 4-22: I/O Status 2 Register

REGISTER NAME		I/O STATUS 2 REGISTER						ACCESS	
ADDRESS		0x28A						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	HSH	Res.	Res.	Res.	Res.	Jmp1	Jmp0
DEFAULT		0	0	0	0	0	0	0	0

BIT	NAME	VAL	DESCRIPTION
0	Jmp0	0	Jumper J6 closed
		1	Jumper J6 open
1	Jmp1	0	Jumper J7 closed
		1	Jumper J7 open
2	Res.	0	Reserved
3		0	Reserved
4		0	Reserved
5		0	Reserved
6	HSH	0	Hot swap handle in closed position
		1	Hot swap handle in open position
7	Res.	0	Reserved

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4.5.7 I/O Configuration Register

The I/O configuration register holds a series of bits defining the on-board configuration for the two COM ports and the general purpose LEDs.

Table 4-23: I/O Configuration Register

REGISTER NAME		I/O CONFIGURATION REGISTER						ACCESS	
ADDRESS		0x287						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	DBIOS	ELED2	ELED1	Res.	ESIOE	ECOM2	ECOM1
DEFAULT		0	0	0	0	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0		0	Reserved						
1		0	Reserved						
2		0	Reserved						
3		0	Reserved						
4	ELED1	0	Enable WD/GP LED for watchdog						
		1	Enable WD/GP LED for GP (LED1)						
5	ELED2	0	Enable TH/GP for over temperature						
		1	Enable TH/GP for GP (LED2)						
6	DBIOS	0	Default boot from 1st Firmware Hub						
		1	Boot from 2nd Firmware Hub						
7		0	Reserved						

4.5.8 Board Version

This register describes the hardware and the board version. The content of this register is unique for each Kontron CompactPCI board.

Table 4-24: Board ID Register

REGISTER NAME	BOARD VERSION						ACCESS	
ADDRESS	0x288						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0
DEFAULT	0	1	1	0	0	0	0	0

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4.5.9 Hardware Index

The hardware index will signal to the software when differences in the hardware require different handling by the software. It starts with the value 0 and will be incremented with each change in hardware as development continues.

Table 4-25: Hardware Index Register

REGISTER NAME	HARDWARE INDEX						ACCESS	
ADDRESS	0x289						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	HWI7	HWI6	HWI5	HWI4	HWI3	HWI2	HWI1	HWI0
DEFAULT	0	0	0	0	0	0	0	0

4.5.10 Logic Version

The logic version register may be used to identify the logic status of the board by software. It starts with the value 0 and will be incremented with each logic update.

Table 4-26: Logic Version Register

REGISTER NAME	Logic Version						ACCESS	
ADDRESS	0x28B						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0
DEFAULT	0	0	0	0	0	0	0	0

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4.5.11 LED Control

With the LED Control register the LED on the front panel can be switched on and off.

Table 4-27: LED Control Register

REGISTER NAME		LED CONTROL REGISTER						ACCESS	
ADDRESS		0x28D						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		ENUM	Res.	Res.	Res.	Res.	HSLED	LED2	LED1
DEFAULT		0	0	0	0	0	0	0	0
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	LED1	0	LED off						
		1	LED on						
1	LED2	0	LED off						
		1	LED on						
2	HSLED	0	Hot swap LED off						
		1	Hot swap LED on						
3		0	Reserved						
4		0	Reserved						
5		0	Reserved						
6		0	Reserved						
7	ENUM	0	No ENUM signal						
		1	Generate ENUM signal						

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Chapter 5

Phoenix BIOS

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5. Phoenix BIOS

5.1 The Setup Guide

With the PhoenixBIOS Setup program, you can modify BIOS settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off.



Note ...

The menus shown here are from a typical system. Depending on the hardware and the features installed in your computer, and due to the fact that Kontron constantly provides the latest BIOS versions, the actual menus displayed on your screen may differ from the screen displays shown in this manual. For more accurate information about your BIOS Setup program, contact Kontron's Technical Support.

5.1.1 Introduction to Setup

This manual describes the Phoenix BIOS Setup program. The Setup program lets you modify basic system configuration settings. The settings are then stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off. A special feature of Kontron's CompactPCI boards is that all Setup information is additionally saved in a non-volatile serial EEPROM. This feature provides the user with enhanced data security in comparison with a standard PC board, because setup data will not be lost should the battery fail.

The Phoenix BIOS in your computer is a customized version of an industry-standard BIOS for IBM PC AT–compatible personal computers. It supports the Intel®x86 and compatible processors. The BIOS provides critical low-level support for the system central processing, memory, and I/O subsystems.

The rest of this manual is intended to guide you through the process of configuring your system using Setup.

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5.1.2 The Main Menu

To start the ***Phoenix*BIOS** Setup utility:

Turn on or reboot your system. PhoenixBIOS displays this message:

Press <F2> to enter SETUP

Pressing <F2> displays the Main Menu, which looks like this:

Figure 5-1: Main Menu — Screen Display

```
                    PhoenixBIOS Setup Utility
  Main    Advanced    Power    Boot    OEMFeatures    Exit

                                                  Item Specific Help

  System Time              [16:19:20]
  System Date:             [04/02/2004]          <Tab>, <Shift-Tab>, or
                                                 <Enter> selects field
  Legacy Diskette A:       [1.44/1.25  MB 3½"]

Primary Master             6449 MB
▶ Secondary Slave          None
▶ Secondary Master         CD-ROM
▶ Secondary Slave          None

Hard Disk Pre-Delay        [Disabled]

▶ Memory Cache
▶ Boot Features

  System Memory              640 kB
  Extended Memory          31744 kB

  F1  Help  ↑↓ Select Item    -/+ Change Values        F9  Setup Defaults
  ESC Exit  ↔ Select Menu     Enter Select ▶ Sub-Menu  F10 Save and Exit
```

5.1.3 The Menu Bar

The Menu Bar at the top of the window lists these selections:

Table 5-1: The Menu Bar

MENU	PURPOSE
Main	Basic system configuration
Advanced	Use to set the Advanced Features available on your system's chipset
Power	Configuration of Power Management features
Boot	Boot sequence configuration
OEM Features	Configuration of special board features
Exit	Exits the current menu

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Use the left and right (->, <-) arrow keys to make a selection.

See the section below, "Exiting Setup," for a description on exiting the Main Menu.

5.1.4 The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates.

Table 5-2: The Legend Bar

KEY	FUNCTION
<F1> or <Alt-H>	General Help window (See below).
<Esc>	Exit this menu.
↔ arrow keys	Select a different menu.
↑↓ arrow keys	Move cursor up and down.
<Tab> or <Shift-Tab>	Cycle cursor in the Time and Date field.
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<F6> or <+> or <Space>	Select the Next Value for the field.
<F9>	Load the Default Configuration values for the complete BIOS.
<F10>	Save and exit.
<Enter>	Execute Command or Select *P* Submenu.
<Alt-R>	Refresh screen.

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. The Save Values commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub menu, use the arrow keys to move the cursor to the sub menu you want. Then press **<Enter>**.
A pointer ► marks all sub menus.

5.1.5 The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

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5.1.6 The General Help Window

Pressing **<F1>** or **<Alt-H>** on any menu brings up the General Help window that describes the legend keys and their alternates:

Figure 5-2: General Help Window — Screen Display

```
                        General Help

Setup changes system behavior by modifying the BIOS
Configuration parameters.  Selecting incorrect values
may cause system boot failure; load Setup Default values
to recover.

<Up/Down> arrows select fields in current menu.
<PgUp/PgDn> moves to previous/next page on scrollable menus.
<Home/End> moves to top/bottom item of current menu.

Within a field, <F5> or <-> selects next lower value and
<F6>, <+>, or <Space> selects next higher value.

<Left/Right> arrows select menus on menu bar.
<Enter> displays more options for items marked with a ▶,
<Enter> also displays an option list on some fields.

<F9> loads factory-installed Setup Default values.
<F10> restores previous values from CMOS.

<ESC> or <Alt-X> exits Setup: in sub-menus, pressing these
keys returns to the previous menu.

<F1> or <Alt-H> displays General Help (this screen).

                          [Continue]
```

The scroll bar on the right of any window indicates that there is more than one page of information in the window. Use **<PgUp>** and **<PgDn>** to display all the pages. Pressing **<Home>** and **<End>** displays the first and last page. Pressing **<Enter>** displays each page and then exits the window.

Press **<Esc>** to exit the current window.

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5.1.7 Main Menu Selections

You can make the following selections on the Main Menu itself. Use the sub-menus for other selections.

Table 5-3: Main Menu Selections

FEATURE	OPTIONS	DESCRIPTION
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.
Diskette A	360 kB, 5 ¼" 1.2 MB, 5 ¼" 720 kB, 3 ½" 1.44/1.25 MB, 3 ½" 2.88 MB, 3 ½" Disabled	Select the type of floppy disk drive installed in your system. 1.25 MB is a Japanese media format that requires a 3½" 3-Mode Diskette drive.
Hard Disk Pre-Delay	Disabled 3 seconds 6 seconds 9 seconds 12 seconds 15 seconds 21 seconds 30 seconds	Select a delay before the BIOS gains access to the hard disk.
System Memory	N/A	Displays amount of conventional memory detected during boot up.
Extended Memory	N/A	Displays the amount of extended memory detected during boot up.

5.1.8 Master and Slave Sub-Menus

The **Master** and **Slave** sub-menus accessed from the Main Menu control these types of devices:

- Hard disk drives
- Removable disk drives such as Zip drives
- CD-ROM drives

*Phoenix*BIOS 4.0 supports up to two **IDE disk adapters**, called **primary** and **secondary** adapters. Each adapter supports one **master drive** and one optional **slave drive** in these possible combinations:

- 1 Master
- 1 Master, 1 Slave
- 2 Masters
- 2 Masters, 1 Slave
- 2 Masters, 2 Slaves

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There is one IDE connector for each adapter on your machine, usually labeled "Primary IDE" and "Secondary IDE." There are usually two connectors on each ribbon cable attached to each IDE connector. In a two drive configuration, the order of placement of Device 0 and Device 1 on the ATA interface cable is not significant to the operation of the interface. If only a single device is attached via the ATA interface to a host, it is recommended that the host and the device be placed at the two ends of the cable.

If you need to change your drive settings, selecting one of the Master or Slave drives on the Main Menu displays a sub-menu, as follows:

Figure 5-3: Master/Slave Sub-Menu — Screen Display

```
                    PhoenixBIOS Setup Utility
        Main
┌──────────────────────────────┬──────────────────────────────┐
│       Primary Master         │      Item Specific Help      │
│                              │                              │
│ Type:                 [User] │ Select the drive type        │
│ Cylinders:            [ 13328]│ of the fixed disk           │
│ Heads:                [  15] │ installed in your sys-       │
│ Sectors               [  63] │ tem. If type User is         │
│ Maximum Capacity:     6449 MB│ selected, Cylinders,         │
│                              │ Heads, and Sectors can       │
│ Total Sectors        40031712│ be edited directly.          │
│ Maximum Capacity      20496MB│ Auto attempts to auto-       │
│                              │ matically detect the         │
│ Multi Sector Transfer; [16 Sectors]│ drive type for drives  │
│ LBA Mode Control:     [Enabled]│ that comply with ANSI     │
│ 32-bit I/O:           [Enabled]│ specifications.           │
│ Transfer Mode:        [Fast PIO 4]│                         │
│ Ultra DMA Mode        [Enabled]│                           │
├──────────────────────────────┴──────────────────────────────┤
│ F1  Help   ↑↓ Select Item   -/+ Change Values   F9  Setup Defaults │
│ ESC Exit   ↔ Select Menu    Enter Select ▶ Sub-Menu  F10 Save and Exit │
└─────────────────────────────────────────────────────────────┘
```

Use the legend keys listed on the bottom to make your selections and exit to the Main Menu. Use the following chart to configure the hard disk.

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Table 5-4: Master/Slave Sub-Menu Options

FEATURE	OPTIONS	DESCRIPTION
Type	None User Auto IDE Removable CD-ROM ATAPI Removable other ATAPI	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = You supply the hard disk drive information in the following fields. Auto = Autotyping, the drive itself supplies the correct drive information. IDE Removable = Removable read-and-write media (e.g., IDE Zip drive). CD-ROM = Readable CD-ROM drive. ATAPI Removable = Read-and-write media (e.g., LS120)
Cylinders	0 to 65,535	Number of cylinders.
Heads	1 to 16	Number of read/write heads.
Sectors	0 to 63	Number of sectors per track.
Multi-Sector Transfers	Disabled 2 sectors 4 sectors 8 sectors 16 sectors	Any selection except Disabled determines the number of sectors transferred per block.
LBA Mode Control	Enabled Disabled	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, & Sectors.
32-Bit I/O	Enabled Disabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO3/DMA1 FPIO4/DMA2	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
Ultra DMA Mode	Disabled Mode 0 up to Mode 5	Selects the Ultra DMA mode used for moving data to /from the drive.

When you enter Setup, the Main Menu usually displays the results of **Autotyping** information each drive provides about its own parameters (e.g., cylinders, heads, and sectors)–and how the drives are arranged as Masters or Slaves on your machine.

Some older drives, however, do not use Autotyping and require selecting type User and entering a pre-defined fixed disk type value (e.g., 1 to 39) or specifying the drive parameters separately with the User type selected. You can find the correct parameters for hard disk drives in the drive manual or written on the casing of the drive itself.

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Note ...

- Exiting this menu keeps your selections but loses internal autotyping information, which may not be selected. If you exit this menu and re-enter it, press <Enter> on Autotype again to restore the Autotype information.
- Do not attempt to change these settings unless you have an older drive that does not support autotyping.
- Before changing the contents of this menu, **write them down**. Once you have established correct parameters for your drive, **write them down and store them in a safe place** (e.g., tape them to the disk drive) for use in case these values are lost in CMOS or if autotyping fails. If these hard disk parameters are not correctly entered in CMOS, you cannot access the data on your drive.



Warning!

Incorrect settings can cause your system to malfunction. To correct mistakes, return to Setup and restore the Setup Defaults with <F9> and re-enter the correct drive parameters.

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5.1.9 Memory Cache

Enabling **cache** saves time for the CPU by holding data most recently accessed in regular memory (dynamic RAM or DRAM) in a special storage area of static RAM (SRAM), which is faster. Before accessing regular memory, the CPU first accesses the cache. If it does not find the data it is looking for there, it accesses regular memory. Selecting "Memory Cache" from the Main menu displays a menu like the one shown here. The actual features displayed depend on your system's hardware.

Figure 5-4: Memory Cache — Screen Display

```
                    PhoenixBIOS Setup Utility
          Main
+-------------------------------------+-------------------------------+
|          Memory Cache               |    Item Specific Help         |
|                                     |                               |
| Cache System BIOS area:    [Write Protect]  | Sets the state of the  |
| Cache Video BIOS area:     [Write Protect]  | external system memory |
| Cache Base 0-512k    :     [Write Back]     | cache.                 |
| Cache Base  512k-640k:     [Write Back]     |                        |
| Cache Extended Memory Area:[Write Back]     |                        |
| Cache A000 - AFFF:         [Disabled]       |                        |
| Cache B000 - BFFF:         [Disabled]       |                        |
| Cache C800 - CBFF:         [Disabled]       |                        |
| Cache CC00 - CFFF:         [Disabled]       |                        |
| Cache D000 - D3FF:         [Disabled]       |                        |
| Cache D400 - D7FF:         [Disabled]       |                        |
| Cache D800 - DBFF:         [Disabled]       |                        |
| Cache DC00 - DFFF:         [Disabled]       |                        |
| Cache E000 - E3FF:         [Disabled]       |                        |
| Cache E400 - E7FF:         [Disabled]       |                        |
| Cache E800 - EBFF:         [Disabled]       |                        |
| Cache EC00 - EFFF:         [Disabled]       |                        |
+-------------------------------------+-------------------------------+
 F1  Help   ↑↓ Select Item   -/+ Change Values      F9  Setup Defaults
 ESC Exit   ↔ Select Menu   Enter Select ▶ Sub-Menu  F10 Save and Exit
```

Use the legend keys listed on the bottom to make your selections and exit to the Main Menu. Use this chart to configure the memory cache.

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Table 5-5: Memory Cache Configuration

FEATURE	OPTIONS	DESCRIPTION
Cache System BIOS area	Write Protect Uncached	Controls caching of system BIOS area. Improves performance only for Dos and WIN 3.11
Cache Video BIOS area	Write Protect Uncached	Caches the video BIOS. Improves performance only for Dos and WIN 3.11
Cache Base 0- 512k	Uncached Write Through Write Protect Write Back	Controls caching of 512k memory
Cache Base 512k-640k	Uncached Write Through Write Protect Write Back	Controls caching of 512k- 640k base memory
Cache Extended Memory Area	Uncached Write Through Write Protect Write Back	Controls caching of system memory above one megabyte
Cache segments, e.g., A000-EFFF	Disabled USWC Caching Write Through Write Protect Write Back	Controls caching of individual segments of memory usually reserved for shadowing system or option ROMs



Warning!

Incorrect settings can cause your system to malfunction. To correct mistakes, return to Setup and restore the Setup Defaults with <F9>.

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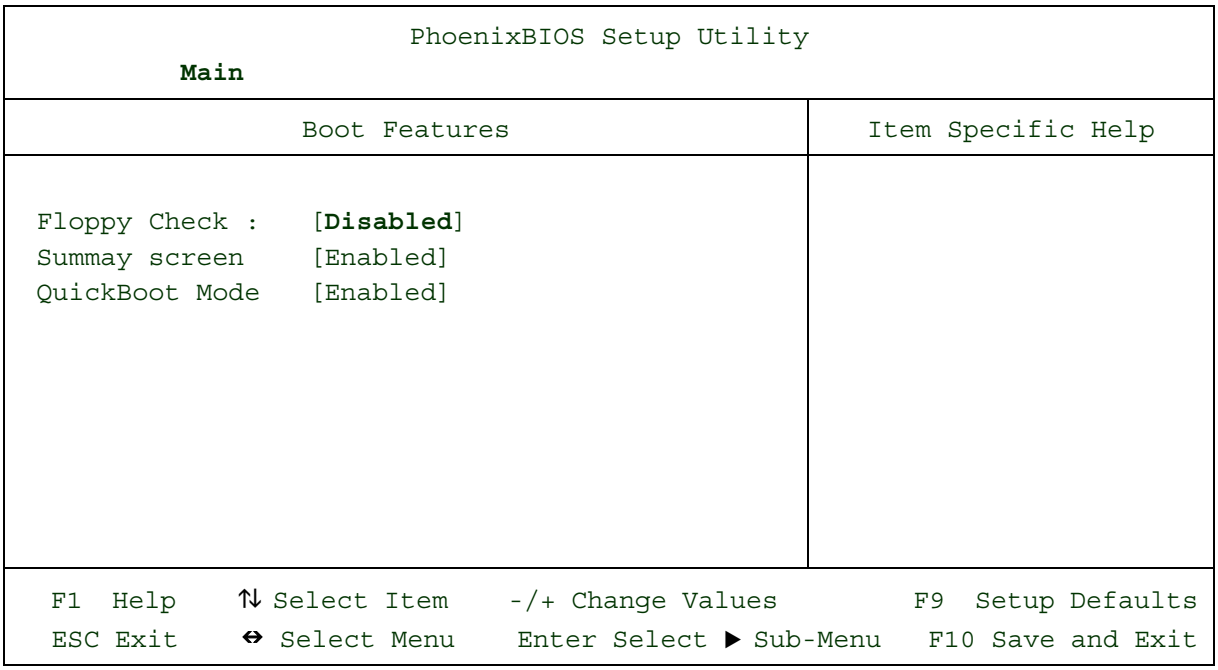
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5.1.10 Boot Features

Selecting "Boot Features" on the Main Menu displays the Boot Features menu.

Figure 5-5: Boot Features — Screen Display



Use the legend keys to make your selections and exit to the Main Menu.

Use the following chart to select your boot options.

Table 5-6: Boot Options

FEATURE	OPTIONS	DESCRIPTION
Floppy Check	Enabled Disabled	Check Floppy during POST
Summary screen	Enabled Disabled	Displays system summary screen during boot up.
QuickBoot Mode	Enabled Disabled	Enable these Function, the system test memory only up to 1MB

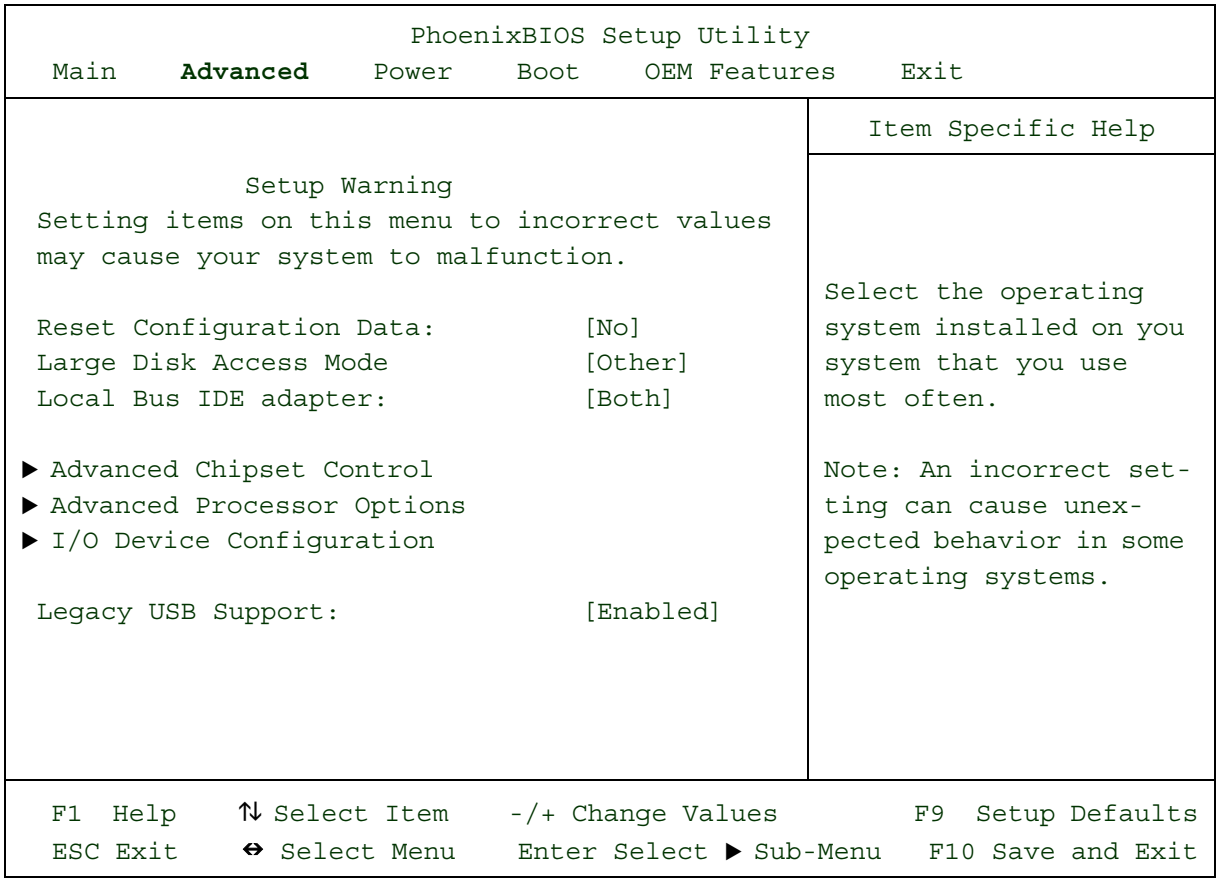
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5.2 The Advanced Menu

Selecting "Advanced" from menu bar on the Main Menu displays a menu like this

Figure 5-6: Advanced Menu — Screen Display



Use the legend keys to make your selections and exit to the Main Menu.

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Table 5-7: Advanced Menu Options

FEATURE	OPTIONS	DESCRIPTION
Reset Configuration Data	Yes No	The Yes option erases all configuration data in a section of memory for **ESCD** (Extended System Configuration Data) which stores the configuration settings for non-PnP plug-in devices. Select Yes when required to restore the manufacturer's defaults.
Large Disk Access Mode	DOS Other	Select DOS if you have DOS. Select Other if you have another operating system such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads, or more than 63 tracks per sector.
Local Bus IDE adapter	Disabled Primary Secondary Both	Enable the integrated local bus IDE adapter
Legacy USB Support	Disabled Enabled	Enables support for legacy USB bus.



Warning!

Incorrect settings can cause your system to malfunction. To correct mistakes, return to Setup and restore the Setup Defaults with <F9>.

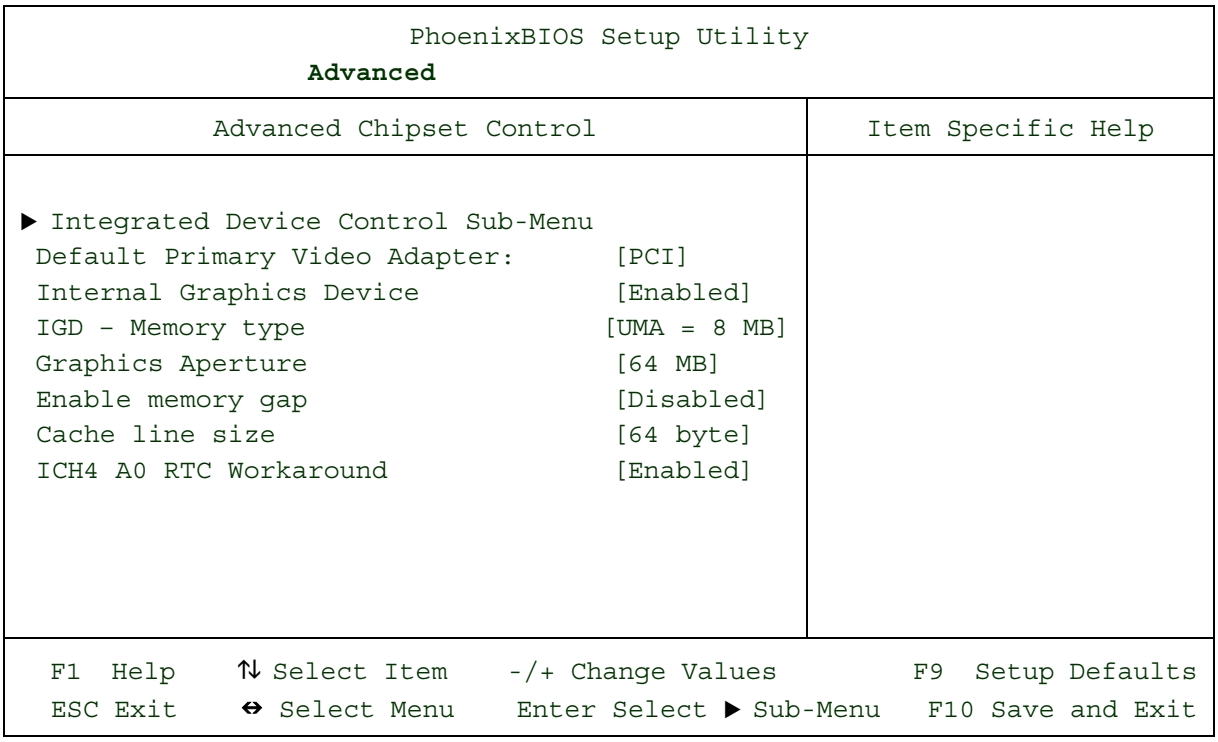
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5.2.1 Advanced Chipset Control Menu

When “Advanced Chipset Control” is selected at the menu bar, the following menu appears:

Figure 5-7: Advanced Chipset Control — Screen Display



Use the legend keys to make your selections, display the sub menus, and exit to the Main Menu.

Table 5-8: Advanced Chipset Control Options

FEATURE	OPTIONS	DESCRIPTION
Default Primary Video Adapter	PCI AGP	Select which installed video card is used for the boot display device
Internal Graphics Device	Enabled Disabled	Enable or Disable the Internal Graphics Device.
IGD – Memory type	NONE UMA = 512KB UMA = 1MB UMA = 8MB	Select the amount of Main Memory that the Internal Graphics Device will use. Let UMA = the amount of pre-allocated Memory made available
Graphics Aperture	256 MB 128 MB 64 MB 32 MB	Select the size of the Graphics Aperture for the AGP video device.

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Table 5-8: Advanced Chipset Control Options

FEATURE	OPTIONS	DESCRIPTION
Enable memory gap	Disabled Extended	If enabled, turn system RAM off to free address space for use with an option card. Either a 128KB conventional memory gap, starting at 512KB, or a 1MB extended memory gap, starting at 15MB, will be created in system RAM
Cache line size	64 byte 32 byte	Determines the PCI performance
ICH4 A0 RTC Workaround	Enabled Disabled	If enabled for ICH4 A0 Silicon, 1.5ms SMI is generated.

5.2.2 Integrated Device Control Sub-Menu

Figure 5-8: Integrated Device Control Sub-Menu — Screen Display

```
                    PhoenixBIOS Setup Utility
                         Advanced
┌──────────────────────────────────────┬──────────────────────────────┐
│  Integrated Device Control Sub-Menu  │  Item Specific Help          │
│                                      │                              │
│  USB Device 29, Function 2:  [Enabled]                              │
│  USB Device 29, Function 1& 2:  [Enabled]                           │
│  USB Device 29, Function 0 & 1 & 2:  [Enabled]                      │
│  USB Device 29, Function 7:  [Enabled]                              │
│                                      │                              │
├──────────────────────────────────────┴──────────────────────────────┤
│ F1  Help   ↑↓ Select Item   -/+ Change Values   F9  Setup Defaults  │
│ ESC Exit   ↔ Select Menu    Enter Select ▶ Sub-Menu  F10 Save and Exit│
└─────────────────────────────────────────────────────────────────────┘
```

Use the legend keys to make your selections, display the sub menus, and exit to the Main Menu.

Table 5-9: USB Device 29 Functions

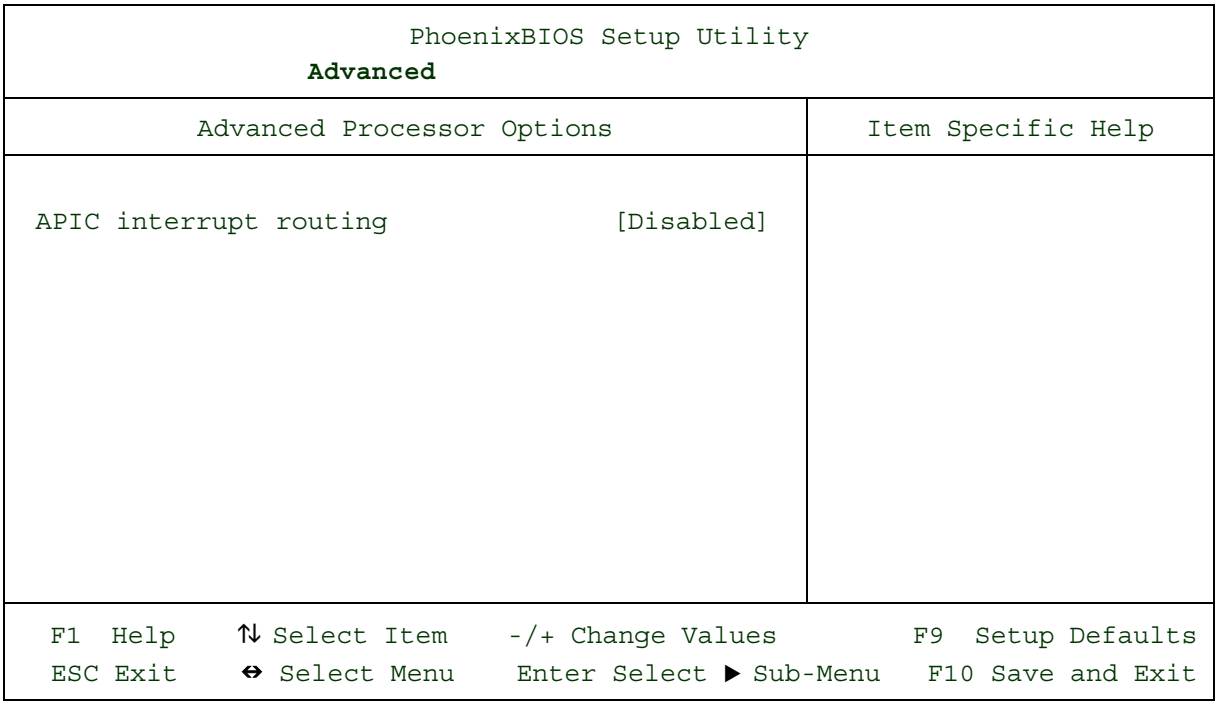
FEATURE	OPTIONS	DESCRIPTION
USB Device 29, Function 2 USB Device 29, Function1&2 USB Device 29, Function 0-2 USB Device 29, Function 7	Enabled Disabled	Enable or Disable this USB Device by setting item to the desired value

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5.2.3 Advanced Processor Options

Figure 5-9: Advanced Processor Options — Screen Display



Use the legend keys to make your selections, display the sub menus, and exit to the Main Menu.

Table 5-10: Advanced Processor Options

FEATURE	OPTIONS	DESCRIPTION
APIC interrupt routing	Enabled Disabled	This item is only valid for WIN2000. A fresh install must occur when APIC Mode is desired. Only used for Multi-Processor Systems.

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5.2.4 I/O Device Configuration Menu

The CPU communicates with external devices such as printers through devices called **Input/Output (I/O) ports** such as serial and parallel ports. These I/O devices require the use of system resources such as I/O addresses and interrupt lines. If these devices are Plug and Play, either the BIOS can allocate the devices during POST, or the operating system can do it. If the I/O devices are not Plug and Play, they may require manually setting them in Setup.

On some systems, the **chipset** manages the communication devices. Other systems have, instead, a separate **I/O chip** on the motherboard for configuring and managing these devices.

Many systems allow you to control the configuration settings for the I/O ports. Select "I/O Device Configuration" on the Advanced Menu to display this menu and specify how you want to configure these I/O Devices:

Figure 5-10: I/O Device Configuration Menu — Screen Display

```
                    PhoenixBIOS Setup Utility
          Advanced
+-------------------------------+-------------------------------+
|  I/O Device Configuration     |  Item Specific Help           |
|                               |                               |
|  Serial Port A:      [3F8/IRQ4]|  Enable support for           |
|  Serial Port B:      [2F8/IRQ3]|  Legacy Universal Serial      |
|                               |  Bus                          |
| Serial Port C:       [Disabled]|                              |
|                               |                               |
| Serial Port D:       [Disabled]|                              |
|                               |                               |
| Parallel Port:       [Enabled] |                              |
|    Mode:             [Bi-directional]                         |
|    Base I/O address  [378]     |                              |
|    Interrupt         [IRQ7]    |                              |
|                               |                               |
| Floppy disk controller: [Enabled]                            |
|   Base I/O address   [Primary] |                              |
|                               |                               |
+-------------------------------+-------------------------------+
| F1  Help   ⇅ Select Item   -/+ Change Values    F9  Setup Defaults |
| ESC Exit   ⇔ Select Menu   Enter Select ▶ Sub-Menu  F10 Save and Exit |
+-------------------------------------------------------------------+
```

Use the legend keys to make your selections and exit to the Main Menu.

Use the following chart to configure the Input/Output settings:

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Table 5-11: I/O Device Configuration Options

FEATURE	OPTIONS	DESCRIPTION
Serial port A Serial port B:	always Enabled	Serial port A I/O Address fixed to 3F8/IRQ4 Serial port B I/O Address fixed to 2F8/IRQ3
Serial Port C Serial Port D	Disabled Enabled Auto	Enabled requires you to enter the base Input/Output address and the Interrupt number for the SIO-Com Ports. Auto makes the BIOS configure the port automatically during POST.
Parallel Port	Disabled Enabled Auto	Disabled turns off the port. Enabled requires you to enter the base Input/Output address and the Interrupt number below. Auto makes the BIOS auto configure the port during POST.
Mode	Output only Bi-directional EPP ECP EPP&ECP	Set the mode for the parallel port using options. Output only is standard one-way protocol for a parallel device. Bi-directional uses two-way protocol of an Extended Capabilities Port (ECP).
Base I/O Address	378 278 3BC	If you select Enabled for the Parallel Port, choose one of these I/O addresses.
Interrupts	IRQ5 IRQ7	If you select Enabled for the Parallel Port, choose one of these interrupt options.
Floppy disk controller	Auto Disabled Enabled	Enables the on-board legacy diskette controller. Disabled turns off all legacy diskette drives.
Base I/O Address	Primary Secondary	If you select Enabled for the Diskette Controller, choose Primary for one diskette drive installed or Secondary for two diskette drives installed.

Use this menu to specify how the I/O (Input and Output) ports are configured:

- Manually by you.
- Automatically by the BIOS during Post



Warning!

If you choose the same I/O address or Interrupt for more than one port, the menu displays an asterisk (*) at the conflicting settings. It also displays this message at the bottom of the menu:

* Indicates a DMA, Interrupt, I/O, or memory resource conflict with another device.

Resolve the conflict by selecting another settings for the devices.

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5.3 The Power Menu

Selecting "Power" from the menu bar displays a menu like this:

Figure 5-11: Power Menu — Screen Display

```
                    PhoenixBIOS Setup Utility
  Main    Advanced    Power    Boot    OEM Features    Exit

                                                  Item Specific Help

Power Savings                 [Disabled]          Select Power Manage-
                                                  ment Mode. Choosing
Resume On Modem Ring:         [Off]               modes changes system
Resume On Time:               [Off]               power management set-
Resume Time                   [00:00:00]          tings. Maximum Power
                                                  Savings conserves the
Power Button Behavior         [On/Off]            greatest amount of sys-
Suspend Mode                  [Suspend]           tem power while Maxi-
After Power Failure           [Last State]        mum Performance
                                                  conserves power but
                                                  allows greatest system
                                                  performance. To alter
                                                  these settings, choose
                                                  Customize. To turn off
                                                  power management,
                                                  choose Disable.

  F1  Help    ↑↓ Select Item    -/+ Change Values      F9  Setup Defaults
  ESC Exit    ↔ Select Menu     Enter Select ▶ Sub-Menu  F10 Save and Exit
```

Use this menu to specify your settings for Power Management. Remember that the options available depend upon the hardware installed in your system. Those shown here are from a typical system.

A power-management system reduces the amount of energy used after specified periods of inactivity. The Setup menu pictured here supports a **Full On** state, a **Standby** state with partial power reduction, and a **Suspend** state with full power reduction.

Use the Advanced Options on this menu to specify whether or not the activity of interrupts can terminate a Standby or Suspend state and restore Full On. Do not change these settings without knowing which devices use the interrupts.

Use the legend keys to make your selections and exit to the Main Menu. Use the following chart in making your selections:

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Table 5-12: Power Menu Options

FEATURE	OPTIONS	DESCRIPTION
Power Savings	Disabled Customize Maximum Power Savings Maximum Performance	Maximum options: pre-defined values. Select Customize to make your own selections from the following fields. Disabled turns off all power management.
Timeout	Standby: OFF/16sec/32/48/1min/2/4/8	Amount of time the system needs to be in idle mode before entering the standby mode. Standby mode turns off various devices in the system, including the screen, until the computer is used again.
	Auto suspend: 5min/10/15/20/30/40/60/OFF	Amount of time the system needs to be in standby mode before entering the suspend mode.
Resume On Modem Ring	Off On	Wakes up system when an incoming call is detected on the modem.
Resume On Time	Off On	Wakes up system at predetermined time.
Resume Time	00:00:00	Enter acceleration Time for Resume Timer Function
Power Button Behavior	On/Off Wake/Sleep	Select the desired system power state after press power button
Suspend Mode	Suspend Save To Disk	Select the type of Suspend Mode. Save to Disk means the System will save its state to disk and power off. Suspend means the system will save its state but remain in a low power mode.
After Power Failure	Stay Off Last State Power On	Sets the mode of operation if an AC/Power Loss occurs.

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5.4 Boot Menu

After you turn on your computer, it will attempt to load the operating system (such as Windows 2000) from the device of your choice. If it cannot find the operating system on that device, it will attempt to load it from one or more other devices in the order specified in the Boot Menu. Boot devices (i.e., with access to an operating system) can include: hard drives, floppy drives, CD-ROMs, removable devices (e.g., Iomega Zip drives), and network cards.



Note ...

Specifying any device as a boot device on the Boot Menu requires the availability of an operating system on that device. Most PCs come with an operating system already installed on hard drive C.

Selecting "Boot" from the Menu Bar displays the Boot menu, which looks like this:

Figure 5-12: Boot Menu — Screen Display

```
                    PhoenixBIOS Setup Utility
 Main    Advanced    Power    Boot    OEM Features    Exit

                                                  Item Specific Help

     CD-ROM Drive
     +Removable Devices
     +Hard Drive
     Network Boot                                 Use these keys to set
                                                  the boot order in which
                                                  the BIOS attempts to
                                                  boot the OS:
                                                  <+> or <-> moves device
                                                  up or down.
                                                  <Enter> expands or col-
                                                  lapses devices marked
                                                  with + or -.
                                                  <Ctrl+Enter> expands
                                                  all
                                                  <Shift+1> enables or
                                                  disables a device.
                                                  <n> moves a removable
                                                  device between hard or
                                                  removable disk.

 F1  Help    ↑↓ Select Item    -/+ Change Values      F9  Setup Defaults
 ESC Exit    ↔ Select Menu     Enter Select ▶ Sub-Menu  F10 Save and Exit
```

Use this menu to arrange to specify the priority of the devices from which the BIOS will attempt to boot the Operating System. In the example above, the BIOS will attempt first to boot from the CD-ROM drive. Failing that, it will attempt to boot from the removable device and then from the Primary Master hard disk, and so on down the list.

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Removable Devices, **Hard Drive**, and **Network Boot** are the generic types of devices on your system from which you can boot an operating system. You may have more than one device of each type. If so, the generic type is marked with a plus or minus sign. Use the <Enter> key to expand or collapse the devices marked with <+> or <->. Press <Ctrl+Enter> to expand all such devices.

This BIOS includes a feature for booting from LAN using the BOOTP / DHCP protocol.

Lan-Boot is based on Etherboot-5.0.7, a LAN-Boot implementation, which is covered by the GNU public license. It has been adopted for use with Kontron CompactPCI Hardware. As required by the GNU public license, the complete source code and further information are available via the internet (www.sourceforge.net).

Using this option requires an understanding of the BOOTP and/or DHCP mechanisms and knowledge in configuring a BOOTP or DHCP server. These topics are not described within this-manual.



Note ...

Floppy drives are not managed on this menu as part of Removable Devices.

To change a device's priority on the list, first select it with the up-or-down arrows, and move it up or down using the <+> and <-> keys. Pressing <n> moves a device between the Removable Devices and Hard Drive.

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5.5 OEM Features Menu

Selecting "OEM Features" from the menu bar displays a menu like this

Figure 5-13: OEM Features Menu — Screen Display

```
                    PhoenixBIOS Setup Utility
  Main    Advanced    Power    Boot    OEM Features    Exit

                                                    Item Specific Help

▶ PC Health
▶ Watchdog Settings
▶ Temperature Management
▶ Front-Rear I/O
▶ System Info

Clock StepUp enabled          High frequency /
                              normal frequency

Bootrom OS-Loader              [Disabled]
Spread Spectrum Modulation     [Disabled]
PCI Wakeup Delay               [Disabled]
Reset PCI-to-PCI bridges       [Disabled]
Delay after P2P Reset          [Disabled]
Delay for PCI Config Cycle     [Disabled]
Power-On delay for USB Devices [Disabled]
Accept CL.FFh for PCI-Dev      [YES]
Onboard lan RPL ROM            [Disabled]
Load JRC BIOS Extension        [YES]

 F1  Help    ⇅ Select Item    -/+ Change Values      F9  Setup Defaults
 ESC Exit    ⇔ Select Menu    Enter Select ▶ Sub-Menu  F10 Save and Exit
```

Use the legend keys to make your selections and exit to the Main Menu. Use the following chart in making your selections:

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Table 5-13: OEM Features Options

FEATURE	OPTIONS	DESCRIPTION
Clock StepUp Enabled	High Frequ. Normal Frequ.	The CPU frequency should be stepped up for mobile CPUs
Bootrom OS-Loader	Disabled Enabled	Loading for VxWorks or other OS Bootimages from Flash.
Spread Spectrum Modulation	Disabled 0.5%	Enable clock spreading. Spread spectrum typically reduces system EMI.
PCI Wakeup Delay	Disabled 2 seconds 4 seconds 8 seconds	Select the delay to be inserted before any PCI access is performed.
Reset PCI-to-PCI Bridges	Disabled Enabled	The BIOS may reset the PCI-to-PCI bridges in the system using a software reset mechanism. Especially when the board is used in conjunction with hots wap compatible boards elsewhere in the system, it should be disabled. Default is disabled.
Delay after P2P Reset	Disabled 1 ms 5 ms 10 ms	Select delay after PCI-to-PCI reset.
Delay for PCI Config Cycle	Disabled 100 ms 200 ms 300 ms 500 ms 800 ms	Select the delay time before each PCI Config Cycle.
Power-On Delay for USB Devices	Disabled 5 seconds	This feature is not available yet and is intended to be made available in future board indexes.
Onboard LAN RPL ROM	Disabled Enabled	Enable LAN BOOT
Accept Cl.FFh for PCI-Dev	Disabled Enabled	Some PCI boards use the class code 0FFh. Boards with class code FF are distributed by some vendors in the knowledge that there will be different handling of such devices. The PCI standard does not define configuration rules for class code FF. By setting this field to “Yes”, these non-standard boards will also be configured by the BIOS and made operable.
Load JRC BIOS Extension	Yes No	For saving space in the ROM area. Select No: JRC extension will not be loaded. Refer to section 5.8.5 for further information regarding the JRC BIOS extension.

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5.5.1 PC Health

Figure 5-14: PC Health — Screen Display

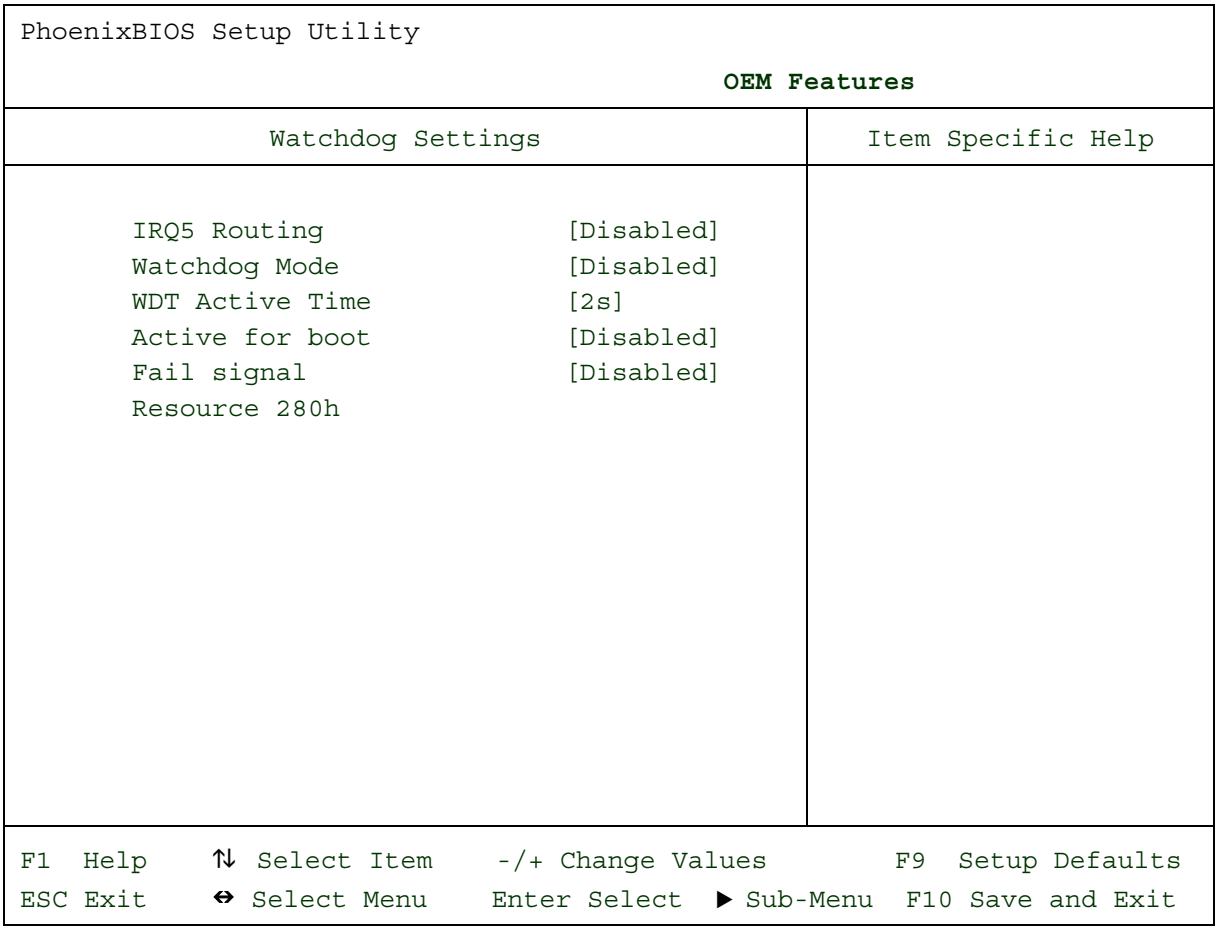
```
                    PhoenixBIOS Setup Utility
                                          OEM Features
+-------------------------------------+-------------------------+
|              PC Health              |  Item Specific Help     |
|                                     |                         |
| T(MAX1617) = 127°C/   261°F         |                         |
| T (CPU)    =  62°C/ 143°F           |                         |
|                                     |                         |
| IN0(V)                   1.2 V      |                         |
| IN1(V)                   3.0 V      |                         |
| IN2(V)                   3.2 V      |                         |
| IN3(V)                   5.0 V      |                         |
| IN4(V)                   11.8 V     |                         |
| IN5(V)                   -12.0 V    |                         |
| Fan1          speed      0 RPM      |                         |
| Fan2          speed      0 RPM      |                         |
+-------------------------------------+-------------------------+
F1  Help    ↑↓ Select Item    -/+ Change Values      F9  Setup Defaults
ESC Exit    ↔ Select Menu     Enter Select ▶ Sub-Menu F10 Save and Exit
```


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5.5.2 Watchdog Settings

Figure 5-15: Watchdog Settings — Screen Display



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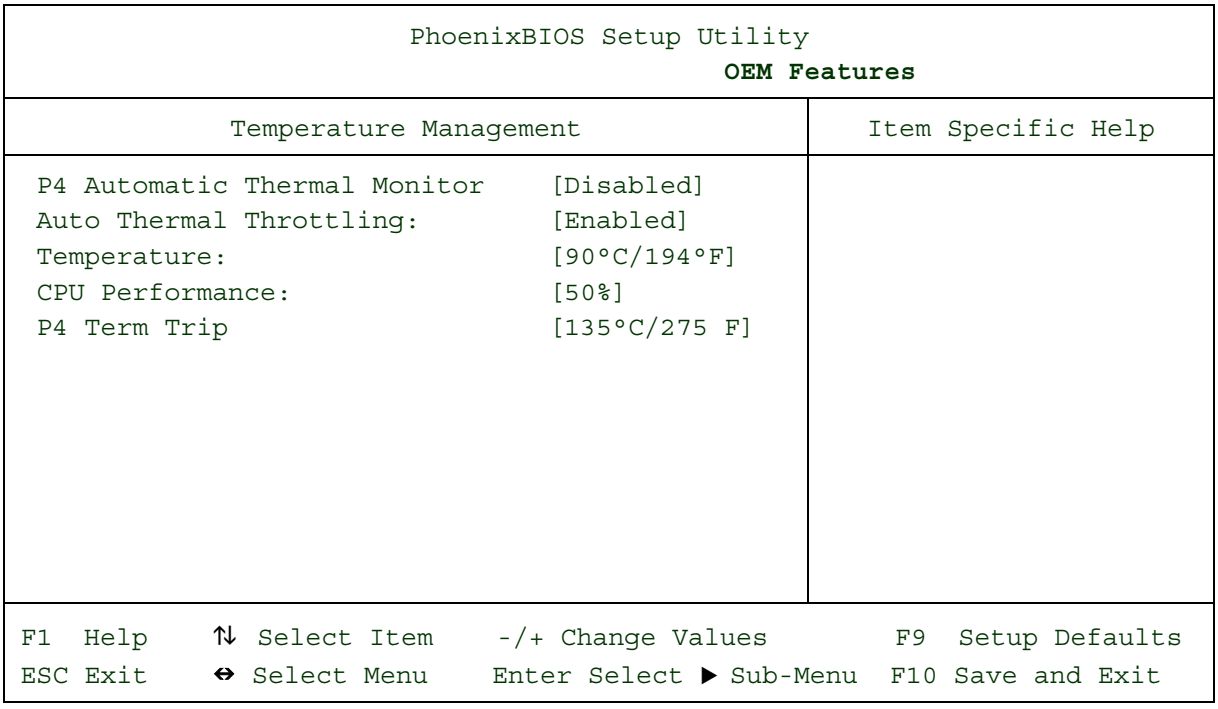
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Table 5-14: Watchdog Settings Options

FEATURE	OPTIONS	DESCRIPTION
IRQ5 routing	Disabled Watchdog Derate Signal Enum Signal Fail Signal	Reserve resource 280h and IRQ5 for watchdog, derate, Enum or Fail signal. Fail signal from the power supply. Enum signal is generated by a hot swap compatible board after insertion and prior to removal. Derate signal indicates that the power supply is beginning to derate its power output.
Watchdog mode	Disabled NMI Reset Cascade (NMI + Reset)	Watchdog routing to NMI, NMI + Reset or Reset
WDT Active Time	125ms, 250 ms, 500ms, 1s, 2s, 4s, 8s, 16s, 32s, 64s, 128s, 256s	Select the time after which the action selected occurs, if the watchdog timer is not retriggered.
Active for boot	Disabled Enabled	Select Enable if the watchdog timer requires to be started before the operating system is booted from the BIOS.
Fail Signal	Disabled NMI	Fail signal from the power supply. If this signal is to used inside an application, it may be routed to NMI here.

5.5.3 Temperature Management

Figure 5-16: Temperature Management — Screen Display



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Table 5-15: Temperature Management Options

FEATURE	OPTIONS	DESCRIPTION
P4 Automatic Thermal Monitor	Disabled Enabled	Thermal Monitor is enabled and when the die temperature is very near to the temperature limits of the processor, the clocks will be modulated by alternately turning the clocks off and on at a duty cycle of 50%.
Auto Thermal Throttling	Enabled Disabled	Reduces CPU speed to avoid overheating
Temperature	75°C – 110°C	CPU clock throttling starts when select Temperature is reached.
CPU Performance	12.5% 25% 50% 75%	The CPU performance will be reduced to the selected value when reaching the temperature threshold
P4 Term Trip	N/A	Shows the P4 max Temperature

5.5.4 Front-Rear I/O

Figure 5-17: Front-Rear I/O — Screen Display

```
                    PhoenixBIOS Setup Utility
                                        OEM Features
┌──────────────────────────────────┬──────────────────────────────┐
│        Front-Rear I/O            │      Item Specific Help      │
│                                  │                              │
│ Serial Port A          [Front]   │ Enable support for           │
│ Serial Port B          [Front]   │ Legacy Universal Serial      │
│ Ethernet Port 3        [Front]   │ Bus                          │
│ RIO BOARD installed    [Yes]     │                              │
│                                  │                              │
│                                  │                              │
│                                  │                              │
│                                  │                              │
│                                  │                              │
└──────────────────────────────────┴──────────────────────────────┘
F1  Help   ⇅ Select Item   -/+ Change Values     F9  Setup Defaults
ESC Exit   ⇔ Select Menu   Enter Select ▶ Sub-Menu  F10 Save and Exit
```

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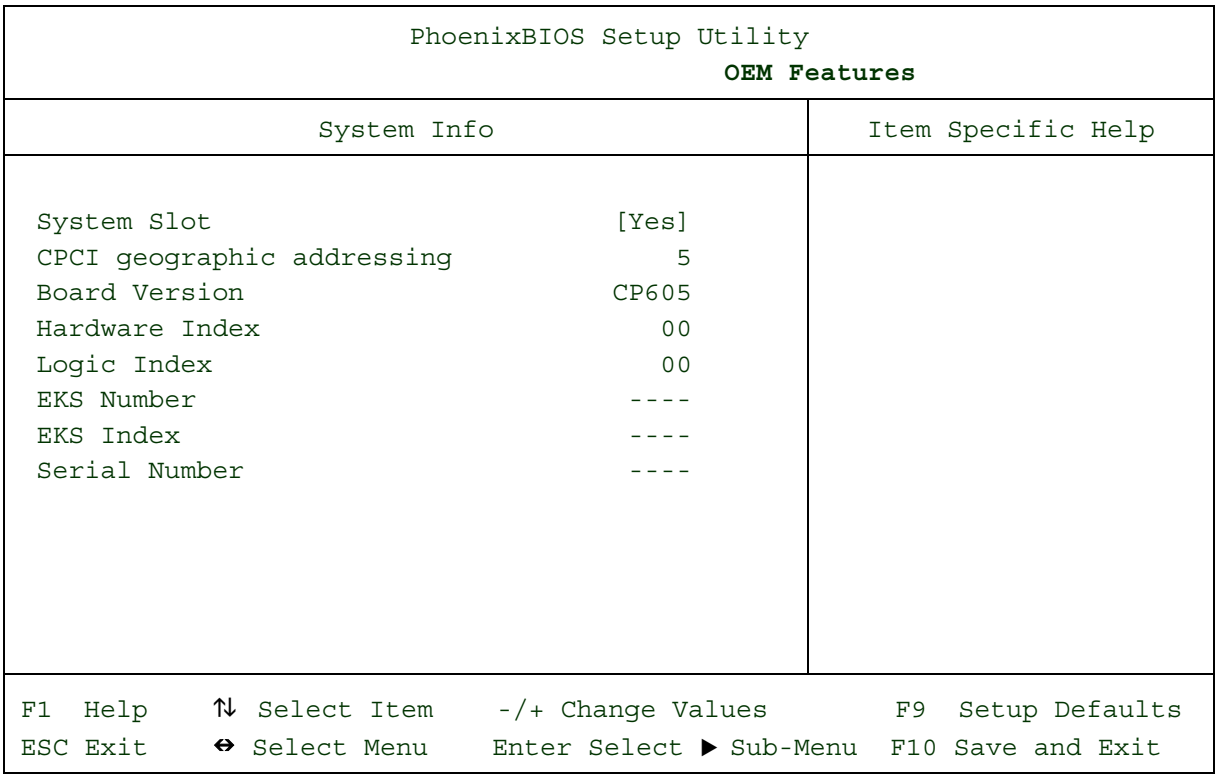
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Table 5-16: Front-Rear I/O Options

FEATURE	OPTIONS	DESCRIPTION
Serial Port A Serial Port B	Front Rear	This item allows Serial Port A and Serial Port B to be configured, wether they should be connected physically to the front panel (Front) or to the Rear IO-Connector (BACK)
Ethernet Port 3	Front Rear Auto	Configures the Ethernet Port 3 to the front panel or to the rear I/O connector. The Auto option detects the connecting cable and configures the Ethernet Port 3 automatically.
RIO BOARD installed	N/A	This is a display only field, which shows, if a RIO board is installed in the system

5.5.5 System Info

Figure 5-18: System Info — Screen Display



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Table 5-17: System Info Options

FEATURE	OPTIONS	DESCRIPTION
System Slot	Yes No	Displays whether the board is in a system slot or not.
CPCI Geographic Addressing	N/A	Displays the slot in which the card is placed starting on the left side with address 0.
Board Version	N/A	This is a display only field, which reflects the value of an onboard register. This must always correspond with the CPU on which the BIOS is installed.
Hardware Index	N/A	This is a display only field, which reflects the value of an onboard register. It shows the index of the hardware.
Logic Index	N/A	This is a display only field, which reflects the value of an onboard register. It shows the index of the onboard logic. When the Board Index is 00 this item is not displayed.
EKS Number EKS Index Serial Number	N/A	This is a display only field, which shows Kontron internal information about the board. EKS number and EKS index refer to the production number and version respectively. The serial number is unique to each board produced by Kontron. It could be used also by the customer to identify specific boards.

5.6 The Exit Menu

Selecting "Exit" from the menu bar displays this menu:

Figure 5-19: Exit Menu — Screen Display

```
                    PhoenixBIOS Setup Utility
        Main    Advanced    Security    Power    Boot    Exit

                                                  Item Specific Help

Exit Saving Changes                               Exit System Setup and
Exit Discarding Changes                           save your changes to
Load Setup Defaults                               CMOS.
Discard Changes
Save Changes

  F1  Help    ↑↓ Select Item    -/+ Change Values        F9  Setup Defaults
  ESC Exit    ↔ Select Menu     Enter Select ▶ Sub-Menu  F10 Save and Exit
```


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The following sections describe each of the options on this menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit

5.6.1 Saving Values

After making your selections on the Setup menus, always select either "Saving Values" or "Save Changes." Both procedures store the selections displayed in the menus in **CMOS** (short for "battery-backed CMOS RAM") a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS.

After you save your selections, the program displays this message

Values have been saved to CMOS!
Press <space> to continue

If you attempt to exit without saving, the program asks if you want to save before exiting.

During boot up, *Phoenix*BIOS attempts to load the values saved in CMOS. If those values cause the system boot to fail, reboot and press **<F2>** to enter Setup. In Setup, you can get the Default Values (as described below) or try to change the selections that caused the boot to fail.

5.6.2 Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

5.6.3 Load Setup Defaults

To display the default values for all the Setup menus, select "Load Setup Defaults" from the Main Menu. The program displays this message

ROM Default values have been loaded!
Press <space> to continue

If, during boot up, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages:

System CMOS checksum bad - run SETUP

Press <F1> to resume, <F2> to Setup

The CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.

Press **<F1>** to resume the boot or **<F2>** to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.

5.6.4 Discard Changes

If, during a Setup Session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS

Selecting “Discard Changes” on the Exit menu updates all the selections and displays this message:

CMOS values have been loaded!
Press <space> to continue

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5.6.5 Save Changes

Selecting “Save Changes” saves all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

5.7 Phoenix BIOS Messages

The following is a list of the messages that the BIOS can display. Most of them occur during POST. Some of them display information about a hardware device, e.g., the amount of memory installed. Others may indicate a problem with a device, such as the way it has been configured. Following the list are explanations of the messages and remedies for reported problems.

* If your system displays one of the messages marked below with an asterisk (*), write down the message and contact your dealer. If your system fails after you make changes in the Setup menus, reset the computer, enter Setup and install Setup defaults or correct the error.

0200 Failure Fixed Disk

Fixed disk is not working or not configured properly. Check to see if fixed disk is attached properly. Run Setup. Find out if the fixed disk type is correctly identified.

0210 Stuck key

Stuck key on keyboard.

0211 Keyboard error

Keyboard not working.

***0212 Keyboard Controller Failed**

Keyboard controller failed test. May require replacing keyboard controller.

0213 Keyboard locked - Unlock key switch

Unlock the system to proceed.

0220 Monitor type does not match CMOS - Run SETUP

Monitor type not correctly identified in Setup

***0230 Shadow Ram Failed at offset: nnnn**

Shadow RAM failed at offset: <nnnn> of the 64k block at which the error was detected.

***0231 System RAM Failed at offset: nnnn**

System RAM failed at offset: <nnnn> of in the 64k block at which the error was detected.

***0232 Extended RAM Failed at offset: nnnn**

Extended memory not working or not configured properly at offset: <nnnn>.

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0250 System battery is dead - Replace and run SETUP

The CMOS clock battery indicator shows the battery is dead. Replace the battery and run Setup to reconfigure the system.

0251 System CMOS checksum bad - Default configuration used

System CMOS has been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS. The BIOS installed Default Setup Values. If you do not want these values, enter Setup and enter your own values. If the error persists, check the system battery or contact your dealer.

*0260 System timer error

The timer test failed. Requires repair of system board.

*0270 Real time clock error

Real-Time Clock fails BIOS hardware test. May require board repair.

0271 Check date and time settings

BIOS found date or time out of range and reset the Real-Time Clock. May require setting legal date (1991-2099).

0280 Previous boot incomplete - Default configuration used

Previous POST did not complete successfully. POST loads default values and offers to run Setup. If the failure was caused by incorrect values and they are not corrected, the next boot will likely fail. On systems with control of **wait states**, improper Setup settings can also terminate POST and cause this error on the next boot. Run Setup and verify that the wait-state configuration is correct. This error is cleared the next time the system is booted.

0281 Memory Size found by POST differed from CMOS

Memory size found by POST differed from CMOS.

02B0 Diskette drive A error

02B1 Diskette drive B error

Drive A: or B: is present but fails the BIOS POST diskette tests. Check to see that the drive is defined with the proper diskette type in Setup and that the diskette drive is attached correctly.

02B2 Incorrect Drive A type - run SETUP

Type of floppy drive A: not correctly identified in Setup.

02B3 Incorrect Drive B type - run SETUP

Type of floppy drive B: not correctly identified in Setup.

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02D0 System cache error - Cache disabled

RAM cache failed and BIOS disabled the cache. On older boards, check the cache jumpers. You may have to replace the cache. See your dealer. A disabled cache slows system performance considerably.

02F0: CPU ID:

CPU socket number for Multi-Processor error.

***02F4: EISA CMOS not writeable**

ServerBIOS2 test error: Cannot write to EISA CMOS.

***02F5: DMA Test Failed**

ServerBIOS2 test error: Cannot write to extended **DMA** (Direct Memory Access) registers.

***02F6: Software NMI Failed**

ServerBIOS2 test error: Cannot generate software NMI (Non-Maskable Interrupt).

***02F7: Fail-Safe Timer NMI Failed**

ServerBIOS2 test error: Fail-Safe Timer takes too long.

device Address Conflict

Address conflict for specified: <device>

`Allocation Error for:` <device>

Run ISA or EISA Configuration Utility to resolve resource conflict for the specified: <device>

CD ROM Drive

CD ROM Drive identified.

Entering SETUP ...

Starting Setup program

***Failing Bits: nnnn**

The hex number: <nnnn> is a map of the bits at the RAM address which failed the memory test. Each 1 (one) in the map indicates a failed bit. See errors 230, 231, or 232 above for offset address of the failure in System, Extended, or Shadow memory.

Fixed Disk n

Fixed disk n (0-3) identified.

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Invalid System Configuration Data

Problem with NVRAM (CMOS) data.

I/O device IRQ conflict

I/O device IRQ conflict error.

PS/2 Mouse Boot Summary Screen:

PS/2 Mouse installed.

nnnn kB Extended RAM Passed

Where: <nnnn> is the amount of RAM in kilobytes successfully tested.

nnnn Cache SRAM Passed

Where: <nnnn> is the amount of system cache in kilobytes successfully tested.

nnnn kB Shadow RAM Passed

Where: <nnnn> is the amount of shadow RAM in kilobytes successfully tested.

nnnn kB System RAM Passed

Where: <nnnn> is the amount of system RAM in kilobytes successfully tested.

One or more I2O Block Storage Devices were excluded from the Setup Boot Menu

There was not enough room in the IPL table to display all installed I2O block-storage devices.

Operating system not found

Operating system cannot be located on either drive A: or drive C:. Enter Setup and see if fixed disk and drive A: are properly identified.

***Parity Check 1 nnnn**

Parity error found in the system bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays: ????. Parity is a method for checking errors in binary data. A parity error indicates that some data has been corrupted.

***Parity Check 2 nnnn**

Parity error found in the I/O bus. BIOS attempts to locate the address and display it on the screen. If it cannot locate the address, it displays ????.

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Press <F1> to resume, <F2> to Setup, <F3> for previous

Displayed after any recoverable error message. Press <F1> to start the boot process or <F2> to enter Setup and change the settings. Press <F3> to display the previous screen (usually an initialization error of an **Option ROM**, i.e., an add-on card). Write down and follow the information shown on the screen.

Press <F2> to enter Setup

Optional message displayed during POST. Can be turned off in Setup.

PS/2 Mouse

PS/2 mouse identified.

Run the I2O Configuration Utility

One or more unclaimed block storage devices have the Configuration Request bit set in the LCT. Run an I2O Configuration Utility (e.g. the SAC utility).

System BIOS shadowed

System BIOS copied to shadow RAM.

UMB upper limit segment address: <nnnn>

Displays the address: <nnnn> of the upper limit of **Upper Memory Blocks**, indicating released segments of the BIOS which can be reclaimed by a virtual memory manager.

Video BIOS shadowed

Video BIOS successfully copied to shadow RAM.

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5.8 Phoenix Phlash16

Phoenix Phlash16 gives you the ability to update your BIOS from a floppy disk without having to install a new ROM BIOS chip.

Phoenix Phlash16 is a utility for "flashing" (copying) a BIOS to the Flash ROM installed on your computer from a floppy disk. A Flash ROM is a Read-Only Memory chip that you can write to using a special method called "flashing." Use Phoenix Phlash16 for updating the current BIOS with a new version.

5.8.1 Installation

Phoenix Phlash16 is available in the respective KIT as a compressed file called CRISDISK.ZIP that contains the following files:

CRISDISK.BAT	Executable file for creating the Crisis Recovery Diskette.
PHLASH16.EXE	Programs the flash ROM.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.WPH	Actual BIOS image to be programmed into flash ROM.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.

5.8.2 Create the Crisis Recovery Diskette

If the OEM or dealer from whom you purchased your system has not provided you with one, then you should create a **Crisis Recovery Diskette** before you use the Phlash16 utility. There are several methods that you can use to create the Crisis Recovery Diskette. Below is one recommended procedure.

1. Be sure you have successfully installed the Phlash16 utility onto your hard disk.
2. Insert a clean diskette into drive A: or B:
3. From the local directory, enter the following:

   CRISDISK [drive]:

   where [*drive*] is the letter of the drive into which you inserted the diskette. For help, type **/?** or **/h**.

   CRISDISK.BAT formats the diskette, then copies MINIDOS.SYS, VGABIOS.EXE (if available), PHLASH16.EXE, PLATFORM.BIN and BIOS.WPH to the diskette, and creates the required custom boot sector.

4. Write protect and label the Crisis Recovery Diskette.



Note ...

You can only supply a volume label after the Crisis Recovery Diskette has been formatted and the necessary files copied because MINIDOS.SYS must occupy the first directory entry for the diskette to boot properly.

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5.8.3 Updating the Crisis Recovery Diskette

If the BIOS image (BIOS.WPH) changes due to an update or bug fix, you can easily update the Crisis Recovery Diskette. Simply copy the new BIOS.WPH image onto the Crisis Recovery Diskette. No further action is necessary.

5.8.4 Executing Phoenix Phlash16

Phoenix Phlash16 is operated in the Command Line mode.



Warning!

For your own protection, be sure you have a Crisis Recovery Diskette ready to use before executing Phlash16.

5.8.4.1 Command Line Mode

Use this mode to update or replace your current BIOS. To execute Phlash16 in this mode, move to the directory into which you have installed Phoenix Phlash16 and type the following:

phlash16

Phoenix Phlash16 will automatically update or replace the current BIOS with the one which your OEM or dealer supplies you.

Phlash16 may fail if your system is using memory managers, in which case the utility displays the following message:

Cannot flash when memory managers are present.

If you see this message after you execute Phlash16, you must disable the memory manager on your system. To do so, follow the instructions in the following sections.

Disabling Memory Managers

To avoid failure when flashing, you must disable the memory managers that load from CONFIG.SYS and AUTOEXEC.BAT. There are two recommended procedures for disabling the memory managers. One consists of pressing the <F5> key (only if you are using DOS 5.0 or above), and the other requires the creation of a boot diskette.

DOS 5.0 (or later version)

For DOS 5.0 and later, follow the two steps below to disable any memory managers on your system. If you are not using at least DOS 5.0, then you must create a boot diskette to bypass any memory managers (See Create a Boot Diskette, below).

1. Boot DOS 5.0 or later version. (In Windows 95, at the boot option screen, choose Option 8, "Boot to a previous version of DOS.")
2. When DOS displays the “Starting MS-DOS” message, press <F5>.

After you press <F5>, DOS bypasses the CONFIG.SYS and AUTOEXEC.BAT files, and therefore does not load any memory managers.

You can now execute Phlash16.

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Create a Boot Diskette

To bypass memory managers in DOS versions previous to 5.0, follow this recommended procedure:

1. Insert a diskette into your A: drive.
2. Enter the following from the command line:

   Format A: /S

3. Reboot your system from the A: drive.

Your system will now boot without loading the memory managers, and you can then execute Phlash16.



Note ...

The boot diskette you create here is distinct from a Crisis Recovery Diskette. See 5.8.2 on page 5-39 for details about creating the Crisis Recovery Diskette.

5.8.5 JRC JUMP*tec*® Remote Control

The JUMP*tec*® Remote Control (JRC) is an extension of the PC BIOS that provides a way to intercept and reroute certain BIOS functionality over a serial port at an early stage during the system's boot process.

Requirements:-

- Regular PC (host PC) running either
  - Windows with jrc.exe installed
  - MS-DOS with jrcd.exe installed
- Serial cable that connects either of the two PC com ports

Table 6-18: COM Ports Pinout

X_1			X_2
SIGNAL	Pin	Pin	**SIGNAL**
Receive data	2	3	Transmit data
Transmit data	3	2	Receive data
GND	5	5	GND

Operating Instructions:

- Open a command prompt window on the host PC when running Windows
- Issue a connect command with the appropriate COM port and the desired baud rate.

  jrc server.<com port><max baud rate>

- You can exit the server mode by pressing both control keys on the keyboard simultaneously.

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Chapter 6

System Considerations

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6. System Considerations

6.1 Thermal Management

The total power dissipation of the new generation of Intel Pentium 4 processors has been rapidly increasing, pushing cooling technology close to its limits. This requires a new technology to keep the processor's die temperature within factory specifications. The following chapters provide system integrators with the necessary information to satisfy thermal requirements when implementing CP605 applications.

6.1.1 Passive Thermal Regulation

The thermal management architecture implemented on the CP605 can be described as being three separate but related functions. The goal of all three functions is to protect the processor and reduce processor power consumption. Enabling the thermal control circuit allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

The three thermal protection functions provided by the processor are:

1. Pentium 4 internal thermal monitor:

   This function controls the processor temperature by modulating the processor core clocks.

2. External (MAX1617) thermal monitor:

   This function controls via the processor Stopclock signal the power consumption. While asserted, it has the effect of stopping the clock to many internal elements of the processor.

3. Thermtrip:

   In the event of a cooling failure resulting in extreme overheating, the processor will automatically shut down when the die temperature has reached approximately 135 °C. This event is known as "Thermtrip".

6.1.1.1 CPU Internal Thermal Supervision

This function can be enabled and disabled in the BIOS, whereby the default value is: disabled. When the internal thermal control circuit has been enabled and a high temperature situation occurs, the internal clocks are modulated by alternately turning the clocks off and on with a duty cycle dependent on the processor type (typically 30-50%). This results in the processor power dissipation being reduced accordingly. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. The thermal control circuit is automatically deactivated when the temperature goes below the internal thermal supervision point. The internal temperature sensor is located near on the hottest area of the processor die. Each processor is individually calibrated during manufacturing to eliminate any potential manufacturing variations.



Note ...

The duty cycle and the internal thermal supervision point is factory configured and cannot be modified. For all Mobile Pentium 4-M processor the internal thermal supervision point is 100 °C.

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6.1.1.2 CPU External Thermal Supervision

This function can be enabled and disabled in the BIOS, whereby the default value is: enabled. There are two independent and isolated thermal sensors in the Pentium 4 processor. One is the on-die thermal diode. The other is the temperature sensor used for the Thermal Monitor and for Thermtrip. The measured temperature of both sensors can vary significantly, whereby the temperature of the external measured on-die sensors is always lower.

When the external thermal control circuit has been enabled and a high temperature situation occurs, the front panel “TH” LED will be switched on and the external Stopclock signal of the processor will be modulated by alternately turning the clocks off and on at a duty cycle specified in the BIOS (12.5% - 75%) and the processor power dissipation will be reduced.

The thermal control circuit does not automatically go inactive once the temperature goes below the selected external thermal supervision point. Explicit software action is necessary to switch back to normal mode.



Note ...

The duty cycle and the external thermal supervision point can be configured in the BIOS. The default external thermal supervision point is 85 °C.

6.1.1.3 CPU Emergency Thermal Supervision

This function can not be enabled and disabled in the BIOS. It is always enabled to ensure that the processor is protected in any event.

Assertion of “Thermtrip” (Thermal Trip) indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C. Upon assertion of Thermtrip, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. Once activated, Thermtrip remains latched until the CP605 undergoes a cold restart is performed (all power off and then on again).



Note ...

Upon assertion of “Thermtrip”, the front panel overtemperature LED flashes at regular intervals.

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6.1.1.4 Thermal Management Recommendations

If the CP605 is operated in a properly configured CompactPCI environment with enough air flow, there is no need to enable the Thermal Management function. However, sometimes the system environment is not optimized for a Pentium 4 processor board and this requires thermal protection to guarantee a stable system. The Thermal Management feature allows system designers to design lower cost thermal solutions without compromising system integrity or reliability.

In this case both the internal and the external Thermal Monitor should be enabled. These two monitors protect the processor and the system against excessive temperatures. In this configuration the clocks will be switched on and off. At a 50% duty cycle, for example, the average power dissipation can drop by up to 50%. In this case, the processor performance also drops by about 50% since program execution halts when the clocks are removed.



Warning!

For Benchmarks and performance tests all Thermal Management functions should be disabled, if enabled the results will be erroneous due to the thermal power reduction.

6.1.2 Active Thermal Regulation

The thermal management concept of the CP605 also encompasses active thermal regulation. For both processor types, specifically designed heat sinks are employed to ensure the best possible basis for operational stability and long term reliability. Coupled together with system chassis which provide variable configurations for forced air flow, controlled active thermal energy dissipation is guaranteed.

6.1.2.1 Heat Sinks

All versions of the CP605 are fitted with optimally designed heat sinks. Their physical size, shape, and construction ensures best possible thermal resistance (R_{th}) coefficients. In addition, they are specifically designed to efficiently support forced air flow concepts as found in modern CompactPCI system chassis.

Even though the CP605 is fitted with an optimally designed heat sink, the thermal energy dissipated by high performance Pentium 4 and Mobile Pentium 4-M processors exceeds the thermal capabilities of the heat sinks except for very low performance applications which still require the outstanding features offered by these processors. For the higher performance applications, the CP605 must be operated with forced air flow.

6.1.2.2 Forced Air Flow

When developing applications using the CP605, the system integrator must be aware of the overall system thermal requirements. System chassis must be provided which satisfy these requirements. As an aid to the system integrator, processor characteristics graphs are provided for both the Pentium 4 and the Mobile Pentium 4-M processors.

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The values have been measured using typical applications running under Windows® 2000. In worst case situations, the values vary and the temperature range must be reduced. In all situations the maximum case temperature of the Pentium 4 processor and Mobile Pentium 4 processor must be kept below the maximum allowable temperature. This temperature value can be measured with the onboard remote temperature sensor. To ensure functionality at the maximum temperature, the BIOS supports a temperature control feature. In instances of overtemperature the hardware monitor will reduce the processor clock speed to reduce power consumption.

Note ...

For higher temperatures it is highly recommended to use only the Pentium 4-M processor family. These processors have a lower power consumption and support higher case temperatures (100°C) and also support the SpeedStep II technology. With the Speedstep feature the mobile processor can be dynamically switched between the low power mode (with 1.2 GHz standard performance) and the high performance mode (2.2 GHz).

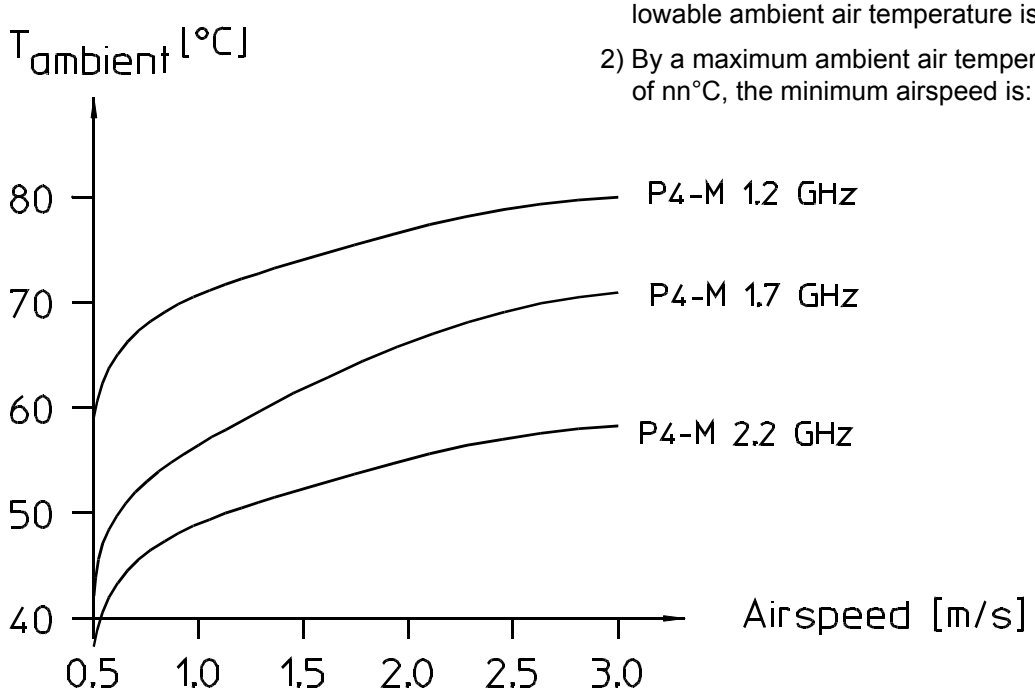
The maximum case temperatures for both processor types is a follows:

- Pentium 4-M: all versions: 100 °C
- Pentium 4: 2 GHz: 68 °C
- Pentium 4: 2.4 GHz: 71 °C

Figure 6-1: Mobile Pentium 4-M Temperature Vs. Airspeed Graph

1) By fixed airspeed of n.n, the maximum allowable ambient air temperature is:

2) By a maximum ambient air temperature of nn°C, the minimum airspeed is:

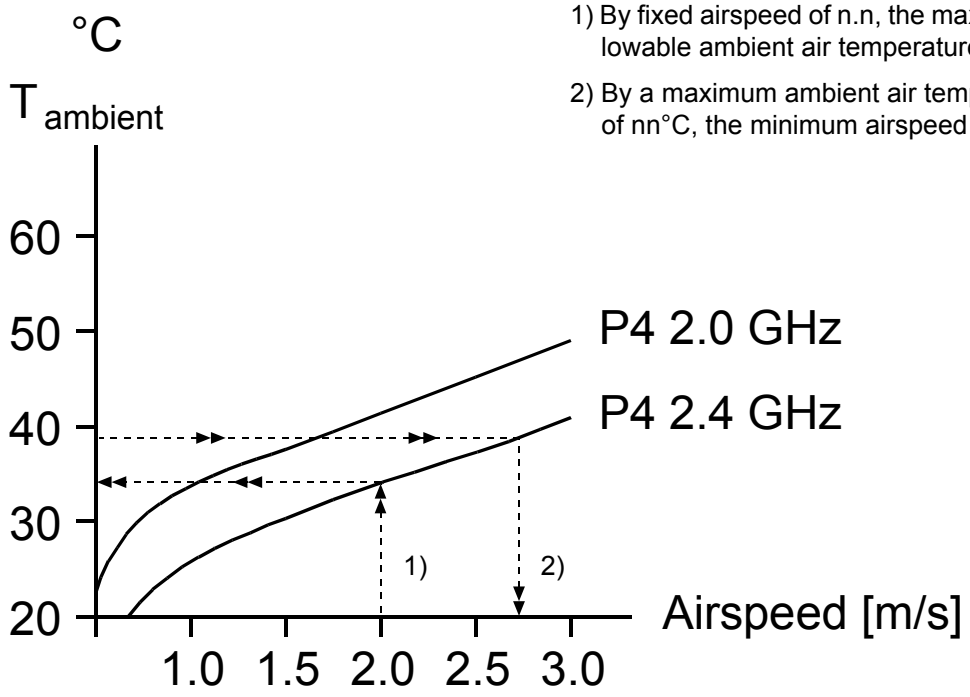


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Figure 6-2: Desktop Pentium 4 Temperature Vs. Airspeed Graph



1) By fixed airspeed of n.n, the maximum allowable ambient air temperature is:

2) By a maximum ambient air temperature of nn°C, the minimum airspeed is:

As individual processor characteristics vary as well as the system environment of the CP605, the information contained in Figures 6-1 and 6-2 must be viewed as a guide and not as an absolute specification. It is the responsibility of the system integrator to ensure that system requirements are specified accordingly.

An airflow of 1.0 m/s is a typical value for a standard Kontron ASM rack (6U CompactPCI rack with a 1U cooling fan tray). Newer ASMs from Kontron will have an airspeed of 2.0 m/s or more. For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient operating temperature, the processor junction (case) temperature must never exceed the specified limit for the involved processor type.

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6.1.2.3 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the CP605 must also be considered. Devices such as hard disks, PMC modules, etc. which are directly attached to the CP605 must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions. In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.



Warning!

As Kontron assumes no responsibility for any damage to the CP605 or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP605 complies with the thermal considerations set forth in this document.

6.2 System Power

The new Intel Pentium 4 processor family requires substantially more power than earlier Pentium processors. This results in special requirements for the power supply and the backplane. The considerations presented in the ensuing chapters must be taken into account by system integrators when specifying the CP605 system environment.

6.2.1 CP605 Baseboard

The CP605 baseboard itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP605 should be carefully tested to ensure compliance with these ratings.

Table 6-1: Maximum Input Power Voltage Limits

SUPPLY VOLTAGE	MAXIMUM PERMITTED VOLTAGE
+3.3 V	+3.6 V
+5 V	+5.5 V
+12 V	+14.0 V
-12 V	-14.0 V



Warning!

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

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The following table specifies the ranges for the different input power voltages within which the board is functional. The CP605 is not guaranteed to function if the board is not operated within the prescribed limits.

Table 6-2: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.
+12 V	11.4 V min. to 12.6 V max.	—
-12 V	-11.4 V min. to -12.6 V max.	—



Note ...

Due to the high power consumption of the Pentium 4 Desktop processor (especially the 2.4 GHz version) it is strongly recommended to use a higher input voltage on the 5 V and 3.3 V lines.

For the Mobile Pentium 4 there is no such limitation.

6.2.2 Backplane

Backplanes to be used with the CP605 must be adequately specified. The backplane must provide optimal power distribution for the +3.3V and the +5V power inputs. It is recommended to use only backplanes which have two power planes for each voltage.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

6.2.3 Power Supply Units

Power supplies must be specified with enough reserve for the remaining system components. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the CP605 has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.



Note ...

Non-industrial ATX PSUs require a greater minimum load than a single CP605 is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP605 may hang up. The solution is to use an industrial PSU or to add more load to the system.

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The start-up behavior of CPCI and PCI (ATX) power supplies is critical for all new CPU boards. These boards require a defined power of sequence and start-up behavior of the power supply. The required behavior is described in the ATX (http://www.formfactors.org/FFDetail.asp?FFID=1&CatID=2) and the CPCI (PICMG, http://www.picmgeu.org/) specification.

6.2.3.1 Start-Up Requirement

Power supplies must comply with the following in order to be used with the CP605.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

6.2.3.2 Power-Up Sequence

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation.

The time from +5 VDC until the output reaches its minimum in regulation level and from +3.3 VDC until the output reaches its minimum in regulation level must be < 20 ms.

6.2.3.3 Tolerance

The tolerance of the voltage lines is described in the CPCI specification (PICMG 2.0 R3.0).The recommended measurement point for the voltage is the CPCI connector on the CPU board.

The following table provides information regarding the required characteristics for each board input voltage.

Table 6-3: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)	REMARKS
5 V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
3.3 V	+3.3 VDC	+5%/-3%	50 mV	
+12 V	+12 VDC	+5%/-5%	240 mV	Required
-12 V	-12 VDC	+5%/-5%	240 mV	Not required
V I/O (PCI) voltage	+3.3 VDC or +5 VDC	+5%/-3%	50 mV	Standard Version +5.0V
GND	Ground, not directly connected to potential earth (PE)			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

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6.2.3.4 Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Note ...

Non-industrial ATX PSUs require a greater minimum load than a single CP605 is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP605 may hang up. The solution is to use an industrial PSU or to add more load to the system.

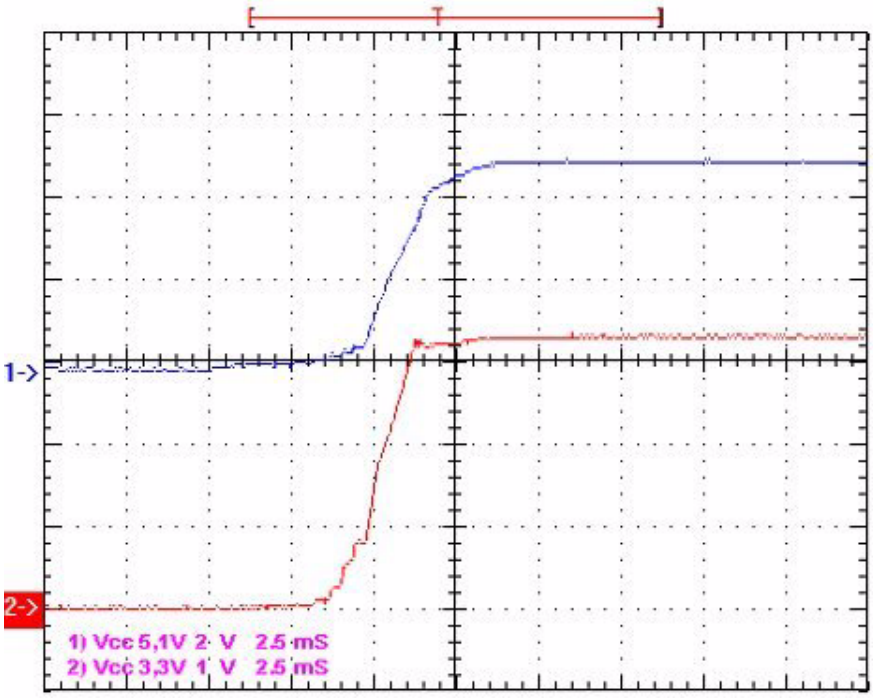
Note ...

If the main power input is switched off, the 3.3V supply voltage will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

6.2.3.5 Rise Time Diagram

The following figure illustrates an example of the recommended start-up ramp of a CPCI power supply for all Kontron boards delivered up to now.

Figure 6-3: Start-Up Ramp of the CP3-SVE180 AC Power Supply



Channel 1: 5 V

Channel 2: 3.3 V

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6.3 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CP605 baseboard and for additional configurations. The Pentium 4 processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and power specifications for the CP605 board and the CP605 accessories. The values were measured using an 8-slot passive CompactPCI backplane with two power supplies: one for the CPU, and the other for the hard disk. The operating systems used were DOS and Windows® 2000. All measurements were conducted at a temperature of 25°C. The measured values varied, because power consumption was dependent on processor activity.

Table 6-4: Power Consumption: DOS

POWER	P4-M 1.2 GHZ 512 MB	P4-M 1.7 GHZ 512 MB	P4-M 2.2 GHZ 512 MB	P4 2 GHZ 512 MB	P4 2.4 GHZ 512 MB
Core	1.2 V	1.3 V	1.3 V	1.5 V	1.5 V
5 V	9 W	14 W	17 W	22.5 W	26 W
3.3 V	8 W	8 W	8 W	8 W	8 W
+12 V	1.2 W	1.2 W	1.2 W	1.2 W	1.2 W
Total	18.2 W	23.2 W	26.2 W	31.7 W	35.2 W

The following table indicates the power consumption using Windows® 2000, IDLE Mode, VGA resolution 1024x768.

Table 6-5: Power Consumption: Windows® 2000, IDLE Mode

POWER	P4-M 1.2 GHZ 512 MB	P4-M 1.7 GHZ 512 MB	P4-M 2.2 GHZ 512 MB	P4 2 GHZ 512 MB	P4 2.4 GHZ 512 MB
Core	1.2 V	1.3 V	1.3 V	1.5 V	1.5 V
5 V	4.3 W	5.6 W	6.4 W	8.3 W	11 W
3.3 V	7.7 W	7.7 W	7.7 W	7.7 W	7.7 W
+12 V	1.2 W	1.2 W	1.2 W	1.2 W	1.2 W
Total	13.2 W	14.5 W	15.3 W	17.2 W	19.9 W

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The following table indicates the power consumption using Windows® 2000, 100% CPU usage, VGA resolution 1024x768: typical application.

Table 6-6: Power Consumption: Windows® 2000, 100% CPU Usage

POWER	P4-M 1.2 GHZ 512 MB	P4-M 1.7 GHZ 512 MB	P4-M 2.2 GHZ 512 MB	P4 2 GHZ 512 MB	P4 2.4 GHZ 512 MB
Core	1.2 V	1.3 V	1.3 V	1.5 V	1.5 V
5 V	12 W	20 W	24 W	31 W	40 W
3.3 V	8 W	8 W	8 W	8 W	8 W
+12 V	1.2 W	1.2 W	1.2 W	1.2 W	1.2 W
Total	21.2 W	29.2 W	33.2 W	40.2 W	49.2 W

The following table indicates the power consumption using Windows® 2000, High Power Tool (Game: 3D-Pinball), VGA resolution 1024x768: maximum power consumption. For further information about the Intel High Power Tool, refer to the Intel web sites.

Table 6-7: Power Consumption: Windows® 2000 High Power Tool

POWER	P4-M 1.2 GHZ 512 MB	P4-M 1.7 GHZ 512 MB	P4-M 2.2 GHZ 512 MB	P4 2 GHZ 512 MB	P4 2.4 GHZ 512 MB
Core	1.2 V	1.3 V	1.3 V	1.5 V	1.5 V
5 V	15 W	24 W	29 W	38 W	46 W
3.3 V	8 W	8 W	8 W	8 W	8 W
+12 V	1.2 W	1.2 W	1.2 W	1.2 W	1.2 W
Total	24.2 W	33.2 W	38.2 W	47.2 W	55.2 W



Note...

The values in the above table are measured using the Intel High Power Tool. This tool serves only for checking the onboard power supplies and does not represent the power consumption of the CP605 during normal operation.

In normal software applications this maximum power consumption level will never be reached.

Table 6-8: Power Consumption Table for CP605 Accessories

MODULE	POWER 5V	POWER 3.3V
Keyboard	100 mW	—
DDR SDRAM SODIMM PC266 256 MB	—	1 to 2 W
DDR SDRAM SODIMM PC266 512 MB	—	1.5 W to 2.5 W
CompactFlash	—	100 mW to 300 mW

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6.3.1 Power Requirement for the CP605

The following table indicates the start-up current of the CP605 during the first 2-3 seconds after the power supply has been switched on. The power consumption of the CP605 during operation is indicated in tables 6-4 to 6-7.

Table 6-9: Start-Up Current of the CP605

POWER		P4-M 1.2 GHZ 512 MB	P4-M 1.7 GHZ 512 MB	P4-M 2.2 GHZ 512 MB	P4 2 GHZ 512 MB	P4 2.4 GHZ 512 MB
5 V	peak	~ 4.0 A	~ 3.4 A	~ 5.5 A	~ 8.5 A	~ 10.0 A
	average	~ 3.0 A	~ 2.5 A	~ 3.2 A	~ 6.5 A	~ 8.0 A
3.3 V	peak	~ 4.8 A	~ 4.8 A	~ 4.8 A	~ 4.8 A	~ 4.8 A
	average	~ 2.2 A	~ 2.2 A	~ 2.2 A	~ 2.2 A	~ 2.2 A
+12 V	peak	~ 0.6 A	~ 0.6 A	~ 0.6 A	~ 0.6 A	~ 0.6 A
	average	~ 0.3 A	~ 0.3 A	~ 0.3 A	~ 0.3 A	~ 0.3 A

For further information on the start-up current, contact Kontron's Technical Support.

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Appendix A

Rear I/O Module CP-RIO6-05

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A. Rear I/O Module CP-RIO6-05

A.1 Introduction

The CP-RIO6-05 rear I/O module has been designed for use with the CP605 6U CompactPCI board from *Kontron Modular Computers*. Designed for use in a PICMG 2.16 environment this rear I/O module provides comprehensive rear I/O functionality.

Everything that can be routed through the front panel may also be routed through the rear I/O. A particular advantage of the rear I/O capability is that there is no cabling on the CPU board which makes it much easier to remove the CPU in the rack.

The rear I/O is plugged in from the back of the system into the backplane connectors P3, P4 and P5 in line with the CPU board.



Note ...

The CP-RIO6-05 board can be used only with the CP605 hardware index 01 (new rear I/O pinout), it cannot be used with the hardware index 00.

A.1.1 Dimensions

The dimensions of the 6U rear I/O module CP-RIO6-05 are as follows:

233.35 mm x 80 mm (6U rear I/O card size).



Note ...

There are two board versions available. The versions can be distinguished by reference to the version number, which is visible on the rear side of the board.

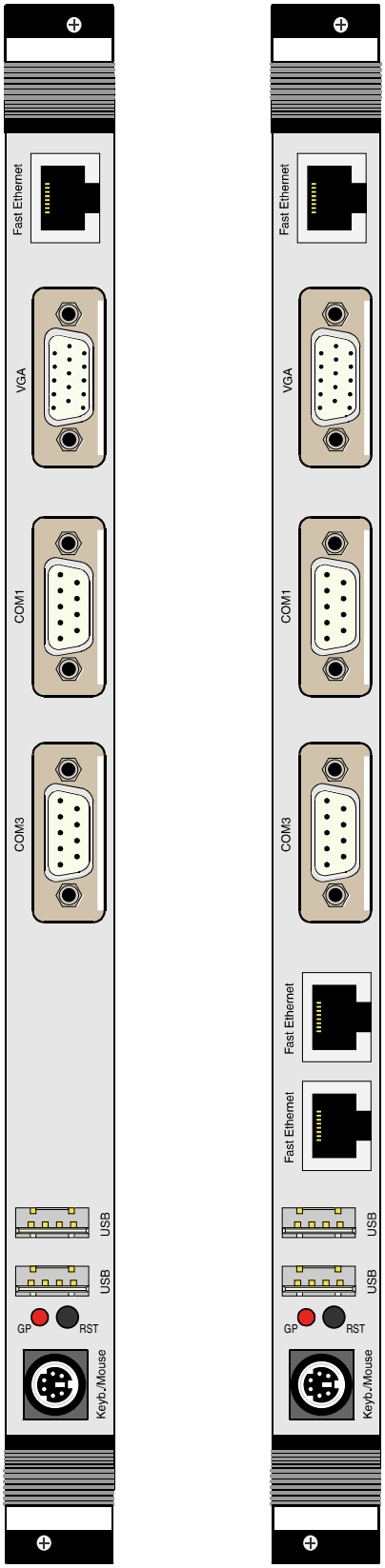
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A.2 Front Panels

Figure A-1: CP-RIO6-05 Front Panels



One variant has one Fast Ethernet connector on the front panel, and the other has three fast ethernet connectors.

There is one board LED on the front panel, situated beneath the USB connectors.

Board LED:

- GP (red) = general purpose LED

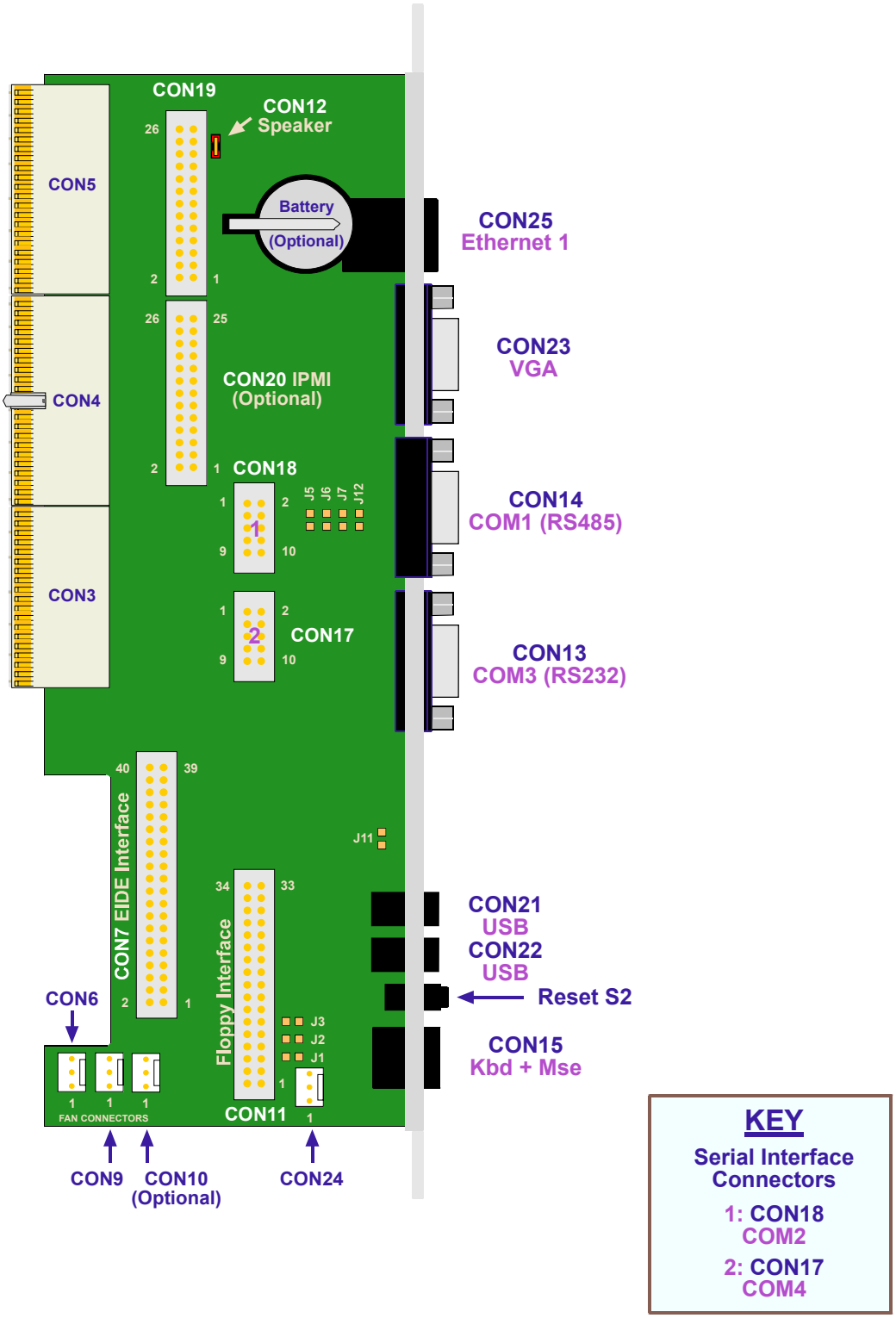
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A.3 Board Layout Variant 1

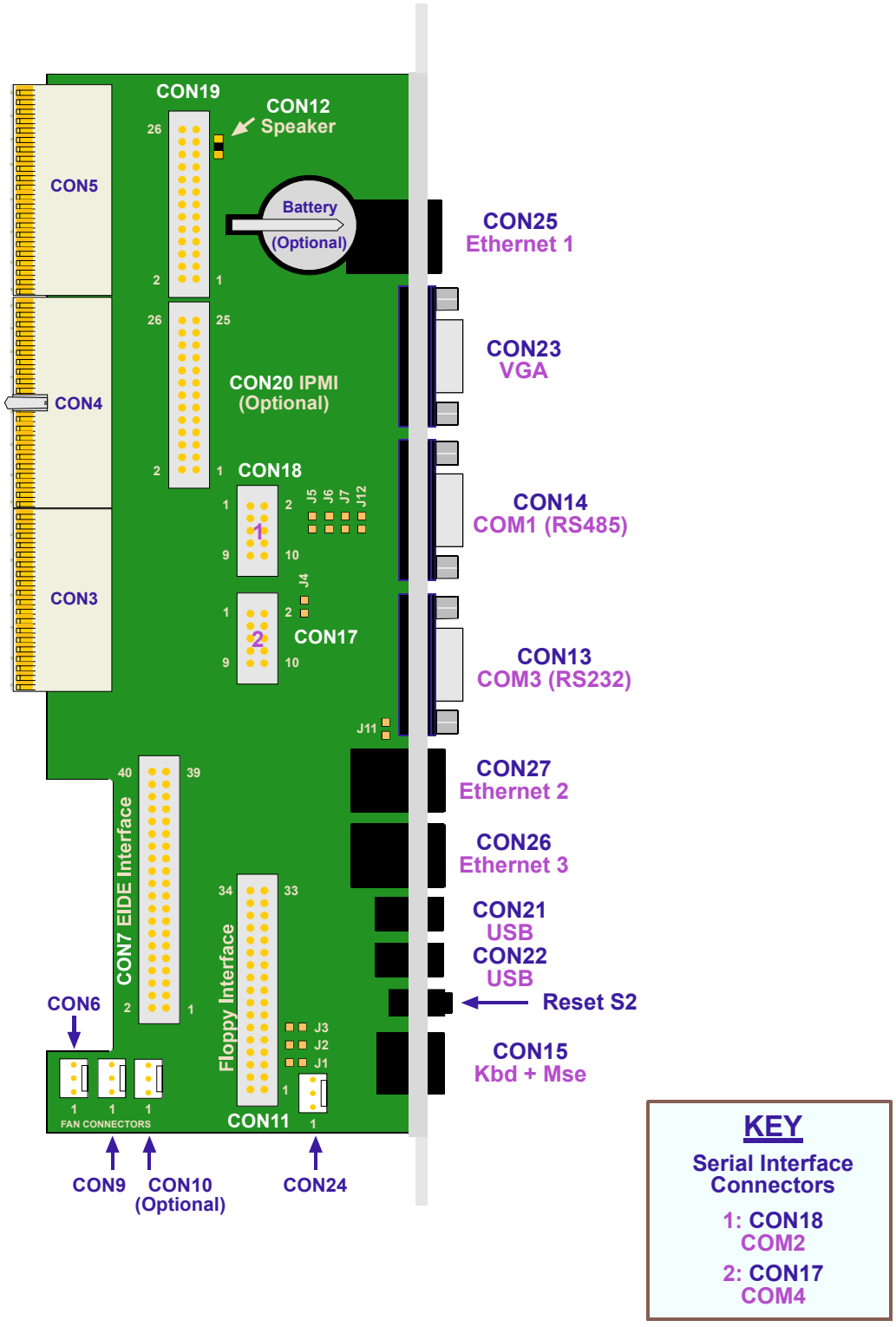
Figure A-2: CP-RIO6-05 Module Board Layout with 1 Ethernet Port



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A.4 Board Layout Variant 2

Figure A-3: CP-RIO6-05 Module Board Layout with 3 Ethernet Ports



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A.5 Overview of Module Interfaces

A.5.1 Overview of Module Interfaces and other Features

A.5.1.1 Front Panel (Width 4HP) Interfaces and Features

Interfaces located directly on the CP-RIO6-05, available via the front panel connectors:-

- One Fast Ethernet channel, with 8-pin RJ45 modular jack (Variant 1)
- Additional Dual Gigabit Ethernet channel if PICMG 2.16 is not used, with 2x8-pin RJ45 modular jack (Variant 2)
- VGA-CRT interface, 15-pin female high-density DSUB
- Two USB ports
- PS/2 Connector for mouse and keyboard, 6-pin MiniDIN
- Reset button
- COM1 interface (RS232)
- COM3 interface (RS232)

A.5.1.2 Internal Interfaces (Accessible via Onboard Connectors)

- CompactPCI specification 6U rear I/O on J3, J4 and J5
- Floppy disk interface with a 34-pin 2.54 mm pinrow connector
- One EIDE interface with 40-pin 2.54 mm pinrow connector (ATA100)
- Optional IPMI interface and a connector for its power supply with differential voltage (selected via Jumpers J1-3)
- Optional serial interface COM2 (RS232)
- Optional serial interface COM4 (RS232)
- Parallel I/O Interface
- Speaker connector
- Fan power connectors
- Optional battery for RTC on the rear I/O

A.6 Detailed Description of Module Interfaces

A.6.1 Keyboard/Mouse Interface

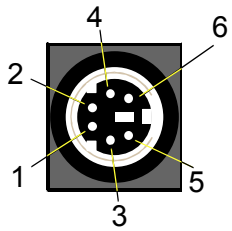


Figure A-4: Keyboard/Mouse Connector

The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded mini-DIN connector.

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A.6.1.1 Keyboard/Mouse Connector CON15 Pinout

Table A-1: Keyboard Connector CON15 Pinout

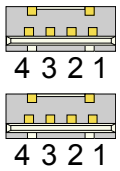
PIN	NAME	FUNCTION	IN/OUT
1	KDATA	Keyboard data	In/Out
2	MDATA	Mouse data	In/Out
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	Out
6	MCLK	Mouse clock	Out

Note ...

The keyboard/mouse power supply units are each protected by a 500 mA fuse. All signal lines are EMI-filtered.

A.6.2 USB Interfaces

Figure A-5: USB Connectors CON21 and CON22



There are two identical USB 2.0 interfaces on the CP-RIO6-05 module each with a maximum transfer rate of 480 Mbit provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more than two USB devices an external hub is required.

A.6.2.1 USB Connectors CON21 and CON22 Pinouts

Table A-2: USB Connector CON21 and CON22 Pinouts

PIN	NAME	FUNCTION	IN/OUT
1	VCC	VCC signal	--
2	UV0-	Differential USB-	IN/OUT
3	UV0+	Differential USB+	IN/OUT
4	GND	GND signal	--

Note ...

The USB power supply is protected by a 0.5 A. All signal lines are EMI-filtered. Self-resettable fuse on each channel (Short circuit current 0.9A per channel).

Note ...

The rear I/O interface supports the USB 1.1 and USB 2.0 standards. For USB 2.0 it is strongly recommended to use a cable length not exceeding 3 metres.

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A.6.3 VGA-CRT Interface

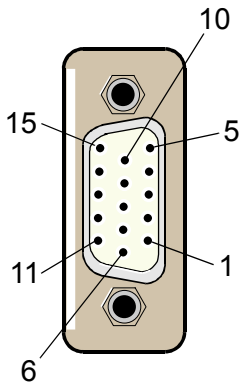


Figure A-6: D-sub VGA-CRT Connector CON23

A.6.3.1 VGA Connector CON23 Pinout

The 15-pin female connector CON23 is used to connect a VGA monitor to the CP-RIO6-05 rear I/O board.

Table A-3: VGA Connector CON23

D-SUB 15	SIGNAL	FUNCTION	IN/OUT
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	I²C data	In/Out
15	Sclk	I²C clock	Out
9	VCC	Power +5V 200 mA no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

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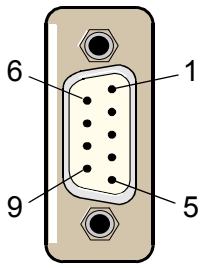
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A.6.4 Serial Port Interfaces

The serial port interfaces COM1 (CON14) and COM3 (CON13) are situated on the front panel of the rear I/O, while COM2 (CON18) and COM4 (CON17) are onboard.

Figure A-7:Serial Connectors CON13 and CON14



Two PC-compatible serial 9-pin D-sub ports are available with 5V charge-pump technology eliminating the need for a +12V and -12V supply. The two COM ports, which are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 460.8 kB/s.

The functions of each serial port interface are shown in the following table:-

Table A-4: Functions of the Serial Port Interfaces

INTERFACE	FUNCTION
COM1	RS232
COM2	RS232
COM3	RS232
COM4	RS232

A.6.4.1 Serial Port Connectors CON18 and CON17 Pinout

The following table gives the pinout of the optional onboard flatcable pinrow connectors CON18 (COM2) and CON17 (COM4).

Table A-5: Serial Port Connectors CON18 (COM2) and CON17 (COM4) Pinout

PIN	RS232
1	DCD
2	DSR
3	RXD
4	RTS
5	TXD
6	CTS
7	DTR
8	RIN
9	GND
10	NC

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A.6.4.2 Serial Port Connectors CON14 and CON13 Pinout

The pinout of the 9-pin D-sub connectors CON14 (COM1) and CON13 (COM3) depends on the configuration.

Table A-6: Serial Port Connectors CON14 (COM1) and CON13 (COM3) Pinout

PIN	RS232
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RIN



Note ...

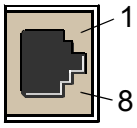
To ensure the proper functioning of the rear I/O serial interfaces, the line drivers for COM1 and COM2 port on the CP605 must be disabled. See chapter 5.5.4 Front-Rear I/O for details).

A.6.5 Fast Ethernet Interfaces

The selection of rear I/O or baseboard front panel Fast Ethernet ports is made via the BIOS setup.

Figure A-8: Ethernet/Fast Ethernet Connectors

The Ethernet connector is realized as an RJ45 twisted-pair connector. The Interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission.



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A.6.5.1 Fast Ethernet Connectors CON25 Pinout

The CON25 connector provides the 10Base-TX/100Base-TX interface to the Ethernet controller. These interfaces are enabled/disabled via the BIOS setting or the rear I/O configuration register.

Table A-7: Fast Ethernet Connectors CON25 Pinout

RJ45	Signal	Function
1	TX+	Transmit +
2	TX–	Transmit –
3	RX+	Receive +
4	NC	--
5	NC	--
6	RX–	Receive –
7	NC	--
8	NC	--

A.6.6 Gigabit Ethernet

A.6.6.1 RJ45 Connectors CON26 and CON27 Pinout

The CON26 and CON27 connectors supply the 10Base-T, 100Base-TX and 1000Base-T interfaces to the Ethernet controller.

Table A-8: Pinouts of CON26 and CON27 Based on the Implementation

MDI / STANDARD ETHERNET CABLE						PIN	MDIX / CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	RX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

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The Ethernet interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission. Auto-wire switching for crossed cables is supported. The two Ethernet channels may be configured via solder jumpers for the rear I/O PICMG 2.16 configuration or front I/O.



Note ...

If the Ethernet channel is configured for PICMG 2.16, the front panel Gigabit connector will have no functionality.

A.6.7 IPMI Interface (Optional)

The Intelligent Platform Management Interface is described in full in section 2.7 in chapter 2. It is accessed from the CP-RIO6-05 by means of the onboard connector, CON20.

A.6.7.1 IPMI Connector CON20 Pinout

Table A-9: IPMI Connector CON20 Pinout

PIN	SIGNAL	SIGNAL	PIN
1	UART0_DIN	UART0_DOUT	2
3	UART0_CTS	UART0_DCD	4
5	UART0_RTS	UART0_RI	6
7	XMIT_EN	ID_XMIT_EN	8
9	CONN_ID0	CONN_ID1	10
11	CONN_ID_DRV	3.3V	12
13	IPMI_VCC	GND	14
15	TACH_IN0	TACH_IN1	16
17	TACH_IN2	TACH_IN3	18
19	PWM0	PWM1	20
21	IPMIGPIO2	GND	22
23	IPMI_VCC	J2ALERT	24
25	J2SDA	J2SCL	26

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A.6.8 Fan Control Interface

A.6.8.1 Fan Control Connector Pinouts

The fan control connectors, CON6, CON9 and CON10, and the optional connector for an external cooling fan, CON24, have the following pinouts:-

Table A-10: Fan Control Connector CON 6 Pinout

PIN	FUNCTION
1	Ground
2	Fan Supply Voltage
3	Fansense (2)

Table A-11: Fan Control Connector CON 9 Pinout

PIN	FUNCTION
1	Ground
2	Fan Supply Voltage
3	Fansense (1)

Table A-12: Fan Control Connector CON 10 (Optional) Pinout

PIN	FUNCTION
1	Ground
2	Fan Supply Voltage
3	Fansense(3)

Table A-13: External Cooling Fan CON24 Pinout

PIN	FUNCTION
1	Ground
2	External Fan Power Input (+12V or +5V)
3	Ground

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A.6.9 EIDE Port

A.6.9.1 EIDE Connectors EIDE1 (CON7)

The EIDE Controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5, and Native Mode IDE on Rear I/O.



Note ...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable also supports all legacy IDE drives.

Due to the rear I/O configuration it is strongly recommended to use only a very short cable length. The maximum cable length should not exceed 45 cm.

The blue end of the ATA-100 cable must be connected to the motherboard, the gray connector to the UltraDMA/100 slave device and the black connector to the UltraDMA/100 master device.

The following table sets out the pinout of connector CON7 and details its corresponding signal names and functions.

Table A-14: Pinout of AT Standard Connector EIDE1 (CON7)

I/O	FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION	I/O
O	Reset HD	IDERESET	1	2	GND	Ground signal	--
I/O	HD data 7	HD7	3	4	HD8	HD data 8	I/O
I/O	HD data 6	HD6	5	6	HD9	HD data 9	I/O
I/O	HD data 5	HD5	7	8	HD10	HD data 10	I/O
I/O	HD data 4	HD4	9	10	HD11	HD data 11	I/O
I/O	HD data 3	HD3	11	12	HD12	HD data 12	I/O
I/O	HD data 2	HD2	13	14	HD13	HD data 13	I/O
I/O	HD data 1	HD1	15	16	HD14	HD data 14	I/O
I/O	HD data 0	HD0	17	18	HD15	HD data 15	I/O
--	Ground signal	GND	19	20	NC	--	--
I	DMA request	IDEDRQ	21	22	GND	Ground signal	--
O	I/O write	IOW	23	24	GND	Ground signal	--
O	I/O read	IOR	25	26	GND	Ground signal	--
I	I/O channel ready	IOCHRDY	27	28	GND	Ground signal	--
O	DMA Ack	IDEDACKA	29	30	GND	Ground signal	--
I	Interrupt request	IDEIRQ	31	32	ATA100	Detect ATA100	--
O	Address 1	A1	33	34	NC	--	--
O	Address 0	A0	35	36	A2	Address 2	O
O	HD select 0	HCS0	37	38	HCS1	HD select 1	O
--	--	NC	39	40	GND	Ground signal	--

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A.6.10 Floppy Drive Interface

The CP-RIO6-05 is provided with a 2-row 34-pin male standard connector, CON11, realized as a connector which provides the signals for up to two floppy drives.



Warning!

If the floppy disk drive connection cable is inverted (pin 1 in place of pin 34), at “power on”, the floppy disk drive will work uninterruptedly, with consequent risk of damage to the floppy disk inserted.

A.6.10.1 Floppy Drive Connector CON11 Pinout

Table A-15: Floppy Drive Connector CON11 Pinout

PIN	SIGNAL	FUNCTION	IN/OUT
2	RWC	Write precompensation	Out
4	NC	--	--
6	NC	--	--
8	INDEX	Index pulse	In
10	MOTEN1	Motor 1 enable	Out
12	DRVSEL2	Driver select 2	Out
14	DRVSEL1	Driver select 1	Out
16	MOTEN2	Motor 2 enable	Out
18	DIRECTION	Step direction	Out
20	STEP	Step pulse	Out
22	WRDATA	Write data	Out
24	WREN	Write enable	Out
26	TRACK0	Track 0 signal	In
28	WRPROT	Write protect	In
30	RDDATA	Read data	In
32	HEADSEL	Head select	Out
34	DSKCHG	Disk change	In
ODD NR.	GND	Ground signal	--

A.6.10.2 Floppy Drive “A+B” Configuration



Note ...

The floppy drive connection cable is suitable for use with two PC-compatible floppy disk drives. Make sure you plug the cable into the connector assigned to floppy drive “A:”. If it is plugged into the drive “B:” connector, no boot from the floppy drive is possible.

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A.6.11 Parallel I/O Interface

The Parallel I/O Interface is routed through the 26-pin connector CON19. In order to use the Parallel I/O Interface as LPT interface, additional termination resistors (pull-up resistors) are required. To use a LPT device, a special adapter is necessary.

Table A-16: Parallel I/O Interface Connector CON19 Pinout

PIN	SIGNAL	PIN	SIGNAL
1	STROBE	14	GND
2	AUTOFD	15	PD6
3	PD0	16	GND
4	ERROR	17	PD7
5	PD1	18	GND
6	INIT	19	ACK
7	PD2	20	GND
8	SLCTIN	21	BUSY
9	PD3	22	GND
10	GND	23	PE
11	PD4	24	GND
12	GND	25	SLCT
13	PD5	26	GND

A.6.12 Speaker Interface

A speaker may be connected using the onboard connector CON12.

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A.6.13 CompactPCI Interface

The standard rear I/O module is equipped with CON3, CON4 and CON5. The availability of the CON4 signals depends on the configuration of the CP605 - whether it is equipped with the J4/CON4 connector.

A.6.13.1 CompactPCI Connectors J3-J5 (CON3-CON5) Pinouts

The CP-RIO6-05 is provided with three female rear I/O connectors J3, J4 and J5. The same pinouts apply to the matching rear I/O connectors P3, P4 and P5 of the CP605 baseboard. For convenience these tables are presented both here and in Chapter 2, “Functional Description and Configuration” of this manual.

Table A-17:Backplane J3 Pin Definitions

PIN	Z	A	B	C	D	E	F
19	GND	RIO_+2.5 V	reserved	reserved	reserved	SIDEATADET	GND
18	GND	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	GND	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	GND	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	GND	LPb_DB+	LPb_DB-	reserved	LPb_DD+	LPb_DD-	GND
14	GND	reserved	reserved	reserved	reserved	reserved	GND
13	GND	IDERST 8)	SIDEIRQ 8)	SIDEDAK 8)	SIDEICHRDY 8)	SIDEDRQ 8)	GND
12	GND	FDDS0 7)	FDDENSEL1 7)	FDMTR0 7)	FDINDEX 7)	FDWDATA 7)	GND
11	GND	FDDS1 7)	FDDSKCHG 7)	FDMTR1 7)	FD.DENSEL0 7)	FDRDATA 7)	GND
10	GND	FDWP 7)	FDHDSEL 7)	FDDIR 7)	FDTRK0 7)	FDSTEP 7)	GND
9	GND	FDWGATE 7)	SIDED15 8)	SIDED14 8)	SIDED13 8)	USB0+ 2)	GND
8	GND	SIDED12 8)	SIDEIOW 8)	RIO_VCC	SIDEIOR 8)	USB0- 2)	GND
7	GND	SIDEA2 8)	SIDEA1 8)	SIDEA0 8)	SIDED0 8)	SIDED1 8)	GND
6	GND	SIDED2 8)	SIDED3 8)	SIDED4 8)	SIDED5 8)	SIDED6 8)	GND
5	GND	SIDECS0 8)	PMDAT 5)	SPKR 1)	KDAT 5)	SIDECS1 8)	GND
4	GND	PRST 1)	PMCLK 5)	RIO_VCC	KCLK 5)	S3RXD 3)	GND
3	GND	S3CTS 3)	S3RTS 3)	S3DSR 3)	S3DCD 3)	S3TXD 3)	GND
2	GND	SIDED7 8)	SIDED8 8)	S3RIN 3)	S3DTR 3)	S4RXD 4)	GND
1	GND	SIDED9 8)	SIDED10 8)	SIDED11 8)	BATT 1)	S4TXD 4)	GND



Warning!

The RIO_XXX signals are power supply outputs from the CPU board to supply the RIO board with power and must not be supplied with external power.

Failure to comply with the above may result in damage to your board.

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Legend for Backplane J3 Table

Table A-18: Backplane J3 Signal Functions

SIGNAL	FUNCTION
CONTROL SIGNALS	
SPKR 1)	Speaker output signal; TTL level
BATT 1)	Battery input signal for RTC; max. 3.3V
PRST 1)	Reset input signal; TTL level
USB PORT 0	
USB0+/- 2)	USB data differential data signals
SERIAL PORT 3	
S3* 3)	Serial port signals; TTL level
SERIAL PORT 4	
S4* 4)	Serial port signals; TTL level
MOUSE + KEYBOARD	
KDAT 5), KCLK 5)	Keyboard data and clock
PMDAT 5), PMCLK 5)	Mouse data and clock
FD* 7)	Floppy signals
SIDE*8	IDE secondary signals
LPA* **LPB***	Gigabit Ethernet Link A Gigabit Ethernet Link B
reserved	Reserved for future use

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Table A-19: Backplane J4 Pinout

PIN	Z	A	B	C	D	E	F
25	GND	RIO_VCC	reserved	reserved	RIO_+3.3V	RIO_VCC	GND
24	GND	reserved	PD0 1)	INIT 1)	reserved	reserved	GND
23	GND	RIO_+3.3V	reserved	reserved	RIO_VCC	reserved	GND
22	GND	reserved	PD1 1)	reserved	reserved	reserved	GND
21	GND	RIO_+3.3V	reserved	AUTOFD 1)	reserved	J2ALERT 2)	GND
20	GND	reserved	PD2 1)	SLCTIN 1)	J2SCL 2)	J2SDA 2)	GND
19	GND	RIO_+3.3V	PD3 1)	STROBE 1)	reserved	IPMIGPIO2 2)	GND
18	GND	reserved	PD4 1)	reserved	PWM1 2)	PWM0 2)	GND
17	GND	RIO_+3.3V	PD5 1)	BUSY 1)	reserved	TACH_IN3 2)	GND
16	GND	reserved	PD6 1)	reserved	TACH_IN2 2)	TACH_IN1 2)	GND
15	GND	RIO_+3.3V	PD7 1)	ACK 1)	reserved	TACH_IN0 2)	GND
12-14	GND						GND
11	GND	reserved	IPMI VCC 1)	PE 1)	reserved	CONN_ID_DRV 2)	GND
10	GND	reserved	reserved	reserved	ID_XMIT_EN 2)	CONN_ID1 2)	GND
9	GND	reserved	IPMI VCC	SLCT 1)	reserved	CONN_ID0 2)	GND
8	GND	reserved	GND	reserved	XMIT_EN 2)	UART0_RI 2)	GND
7	GND	GND	reserved	ERROR 1)	reserved	UART0_RTS 2)	GND
6	GND	reserved	reserved	reserved	UART0_DCD2)	UART0_CTS 2)	GND
5	GND	GND	GND	reserved	UART0_DOUT 2)	UART0_DIN 2)	GND
4	GND	reserved	GND	reserved	GND	GND	GND
3	GND	reserved	reserved	GND	reserved	reserved	GND
2	GND	reserved	reserved	GND	reserved	reserved	GND
1	GND	RIO_VCC	RIO_-12V	GND	RIO_+12V	RIO_VCC	GND



Warning!

The RIO_XXX signals are power supply outputs from the CPU board to supply the RIO board with power and must not be supplied with external power.

Failure to comply with the above may result in damage to your board.

Legend for Backplane J4 Table

1) Parallel I/O interface signals

2) IPMI control signals

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Table A-20: Backplane J5 Pinout

PIN	Z	A	B	C	D	E	F
22	GND	PMCR4	PMCR3	PMCR2	PMCR1	PMCR0	GND
21	GND	PMCR9	PMCR8	PMCR7	PMCR6	PMCR5	GND
20	GND	PMCR14	PMCR13	PMCR12	PMCR11	PMCR10	GND
19	GND	PMCR19	PMCR18	PMCR17	PMCR16	PMCR15	GND
18	GND	PMCR24	PMCR23	PMCR22	PMCR21	PMCR20	GND
17	GND	PMCR29	PMCR28	PMCR27	PMCR26	PMCR25	GND
16	GND	PMCR34	PMCR33	PMCR32	PMCR31	PMCR30	GND
15	GND	PMCR39	PMCR38	PMCR37	PMCR36	PMCR35	GND
14	GND	PMCR44	PMCR43	PMCR42	PMCR41	PMCR40	GND
13	GND	PMCR49	PMCR48	PMCR47	PMCR46	PMCR45	GND
12	GND	PMCR54	PMCR53	PMCR52	PMCR51	PMCR50	GND
11	GND	PMCR59	PMCR58	PMCR57	PMCR56	PMCR55	GND
10	GND	RIO_+3.3V	PMCR63	PMCR62	PMCR61	PMCR60	GND
9	GND	reserved	reserved	S1RXD 4)	TDN1 2)	RDN1 2)	GND
8	GND	reserved	reserved	S1TXD 4)	TDP1 2)	RDP1 2)	GND
7	GND	COM2_ENABLE 1)	COM1_ENABLE 1)	S1RTS 4)	USB1+ 3)	RIO_+3.3V	GND
6	GND	S1DTR 4)	S1CTS 4)	S1DSR 4)	S1DCD 4)	S1RIN 4)	GND
5	GND	S2RXD 5)	S2TXD 5)	S2RTS 5)	S2DTR 5)	ROUT 8)	GND
4	GND	S2DSR 5)	S2DCD 5)	S2RIN 5)	S2CTS 5)	HSYNC 8)	GND
3	GND	S4DTR 6)	S4CTS 6)	S4DSR 6)	GPLED 1)	BOUT 8)	GND
2	GND	S4RTS 6)	S4RIN 6)	FANSENSE2 7)	FANPWM 7)	VSYNC 8)	GND
1	GND	S4DCD 6)	RIOPRESENT 1)	FANSENSE1 7)	USB1- 3)	GOUT 8)	GND



Warning!

The RIO_XXX signals are power supply outputs from the CPU board to supply the RIO board with power and must not be supplied with external power.

Failure to comply with the above may result in damage to your board.

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Legend for Backplane J5 Table

Table A-21: Backplane J5 Signal Functions

SIGNAL	FUNCTION
Control signals	
COM1_ENABLE 1)	Serial port 1 enable signal for front I/O and rear I/O Low = Front I/O High = Rear I/O
COM2_ENABLE 1)	Serial port 2 enable signal for front I/O and rear I/O Low = Front I/O High = Rear I/O
GPLED 1)	General purpose LED output (TH/GP or LED2, depending on configuration, see table 4-24, I/O Configuration Register)
RIOPRESENT 1)	Low = rear I/O module is present High = rear I/O module is not present This signal must be set on the rear I/O module to GND
Ethernet	
TDP1 2)	Ethernet high transmit Data line
TDN1 2)	Ethernet low transmit Data line
RDP1 2)	Ethernet high receive Data line
RDN1 2)	Ethernet low receive Data line
USB port 1	
USB1+/- 3)	USB data differential data signals
Serial Port 1	
S1* 4)	Serial port signals; TTL level
Serial Port 2	
S2* 5)	Serial port signals; TTL level
Serial Port 4	
S4* 6)	Serial port signals; TTL level
FAN control	
FANPWM 7)	DAC output that can be used to control fan speed; 0V to +1.25V output
FANSENSE1/2 7)	Schmitt Trigger fan tachometer inputs; TTL level
VGA CRT signals	
ROUT 8)	Red signal
GOUT 8)	Green signal
BOUT 8)	Blue signal
HSYNC 8)	Horizontal Sync.
VSYNC 8)	Vertical Sync.
PMC Rear I/O signals	

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A.6.13.2 COM3 Jumper Setting

Table A-22: COM3: RS232 ON/OFF

JUMPER	SETTING	DESCRIPTION
J11	***Open***	***RS232 active***
	Closed	RS232 disabled

The default setting is indicated by using italic bold.

A.6.13.3 COM4 Jumper Setting

Table A-23: COM4: RS232 ON/OFF

JUMPER	SETTING	DESCRIPTION
J4	***Open***	***RS232 active***
	Closed	RS232 disabled

The default setting is indicated by using italic bold.

Reserved Jumpers:

J5, J6, J7, J12

A.6.14 Fan Power Supply Voltage Selection

The voltage for the cooling fans may be configured for either 5V or 12V using jumpers J1, J2 and J3.

Table A-24: Fan Power Supply Voltage Setting

JUMPER SETTINGS	VOLTAGE
J1 closed	Enable external cooling fan power
J2 closed	Supply voltage Vcc (5V)
J3 closed	***Supply voltage 12V***

The default setting is indicated by using italic bold.

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