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CP690

Active PMC Carrier Board
for CompactPCI Applications

Manual ID: 20955, Rev. Index 03
May 2003

The product described in this manual is in compliance with all applied CE standards.

Revision History

Manual/Product Title:	CP690		
Manual ID Number:	20955		
Rev. Index	**Brief Description of Changes**	**Board Index**	**Date of Issue**
0100	Initial Issue	0000/0000	Jan. 00
02	Added support signals for 66 MHz operation	0000	Oct. 02
03	Addition of Configuration chapter	0000	May 03

Imprint

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This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

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Explanation of Symbols



CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

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Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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For Your Safety

Your new *PEP* product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

Before installing your new *PEP* product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

- Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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General Instructions on Usage

- In order to maintain *PEP's* product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by *PEP Modular Computers* and described in this manual or received from *PEP* Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 Overview

PMC modules are renowned for their flexibility and versatility of use. They afford the user wide ranging system independent solutions by means of easily interchanged or upgraded mezzanine add-on modules. The *PEP* CP690 has been designed to maximize the advantages provided by PMC modules in a 6U environment. Flexibility, versatility, convenience and ease of use have been keynotes throughout the design process. The result is a board which, although essentially a carrier for PMC modules, also includes a wide range of important features such as a PCI-PCI bridge, Rear I/O capability and (optionally available) the ability to hotswap. Use of the hotswap version means, of course, that all PMC modules employed on the board are effectively hotswapable.

The CP690 is a 6U non-intelligent, active CPCI carrier board with two PMC slots.

Some of the Outstanding Features of the CP690:

- active carrier with PCI-to-PCI bridge: the primary and secondary PCI busses are capable of being operated independently of one another
- 64/32 Bit / 33MHz PCI Bus on the CPCI and on the PMC side (a 66MHz version is under development)
- it supports the Interrupts INTA, INTB, INTC and INTD
- software transparent: the non-hotswap version does not require a software driver.
- it may be configured for 5V or 3.3V signalling on the secondary PCI bus (PMC side)
- it supports all the signals of the PCI Bus on its connectors Jn1 (CON6/CON10), Jn2 (CON4/CON9) and Jn3 (CON7/CON11)
- The two Jn4 connectors CON8 and CON12 provide the possibility to implement Rear I/O through CPCI connectors J3 and J5.
- The connectors which connect the mezzanine board with the carrier include all the signals of a 33MHz, 64/32-bit, multi-master PCI bus, the power rails for 5V, 3.3V, V(I/O) and other specialised signals for Board Detection.
- A PCI-to-PCI bridge provides for coupling of the PMC side to the CompactPCI side, so that two independent PCI busses exist. The PCI-to-PCI bridge is the INTEL 21154. It is software transparent and consequently a software driver is not required to manage data transfer between the PMC module and the CPCI bus.
- The CP690 has been designed to function with all PEP CompactPCI backplanes. The fact that the J4 connector is not present on the CP690 means that this carrier board can also be used in systems employing an H110 backplane.
- The secondary (PMC) side of the board has been prepared for the new 64-bit PMC modules which are now starting to become available.

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Features of the *Kontron Modular Computers*' PMC modules

Kontron Modular Computers' PMC modules are operable in both CompactPCI and VME systems. They offer all the key benefits of PC I/O technology, namely:

- low cost solutions
- high performance
- a processor independent local I/O bus
- a broad range of I/O peripheral devices

PEP Modular Computers' PMC modules may be installed on a variety of different carrier boards, including:

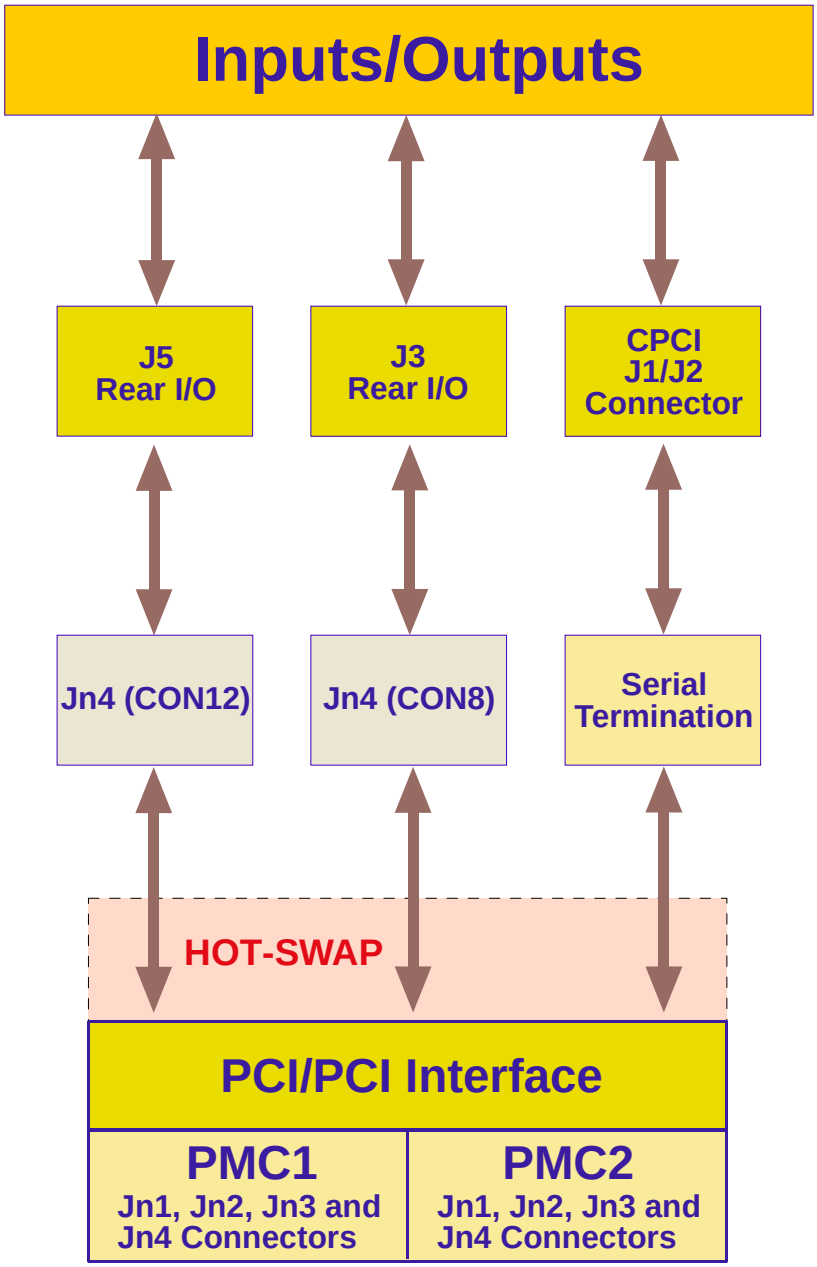
- CompactPCI 3U/6U: CPU CP302 CP600, CP602, CP610, CP611, CP612
- CompactPCI PMC carrier boards such as the CP390 and the CP690

Customers who additionally require the functionality of the CP690 in the smaller 3U Form Factor are referred to *Kontron's* single-height PMC Module carrier board, the CP390.

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1.2 Functional Block Diagram

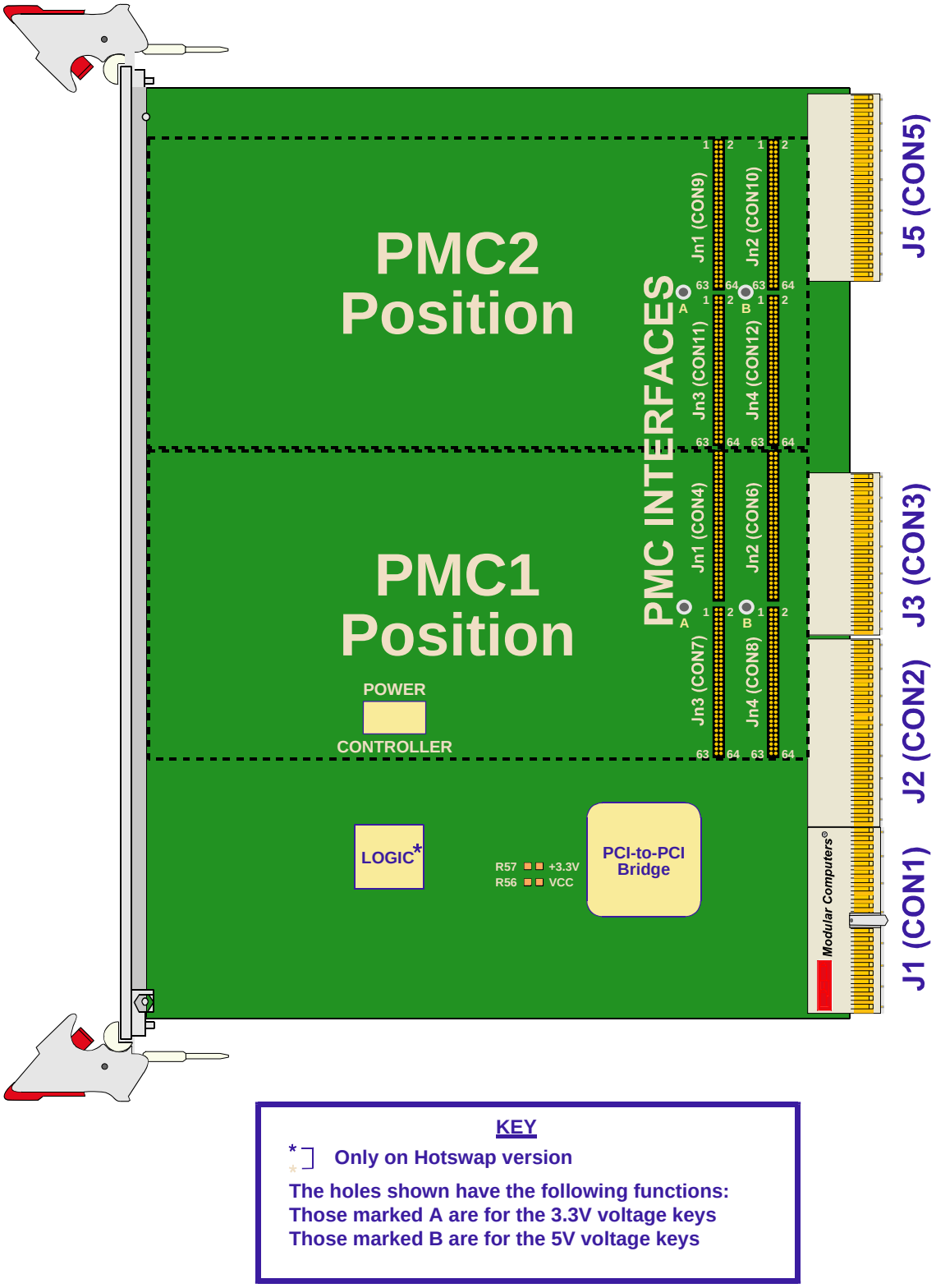
Figure 1-1: Functional Block Diagram



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1.3 Board Layout

Figure 1-2: Board Layout



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1.4 Functions of Onboard Connectors

1.4.1 CompactPCI Connector

The CPCI interface provides all the necessary signals for data transfer as defined by PCI Specification Rev. 2.1.

The CP690 is routed to the CompactPCI backplane using the Intel 21154 PCI-to-PCI bridge which interfaces the board with a data path width of 32 or 64-bit and a speed up to 33 / 66MHz. All the signals are provided on the CPCI connectors J1 and J2 (64-bit extension). In addition to meeting the requirements of the interface definition of the CPCI Specification PICMG 2.0 R2.1, the CP690-HS is additionally designed to comply with the CPCI Hotswap specification PICMG 2.1 R1.0, a consequence of which is that the CPCI interface of the board will be precharged when the board is plugged into a running system.

1.4.2 PMC Interfaces

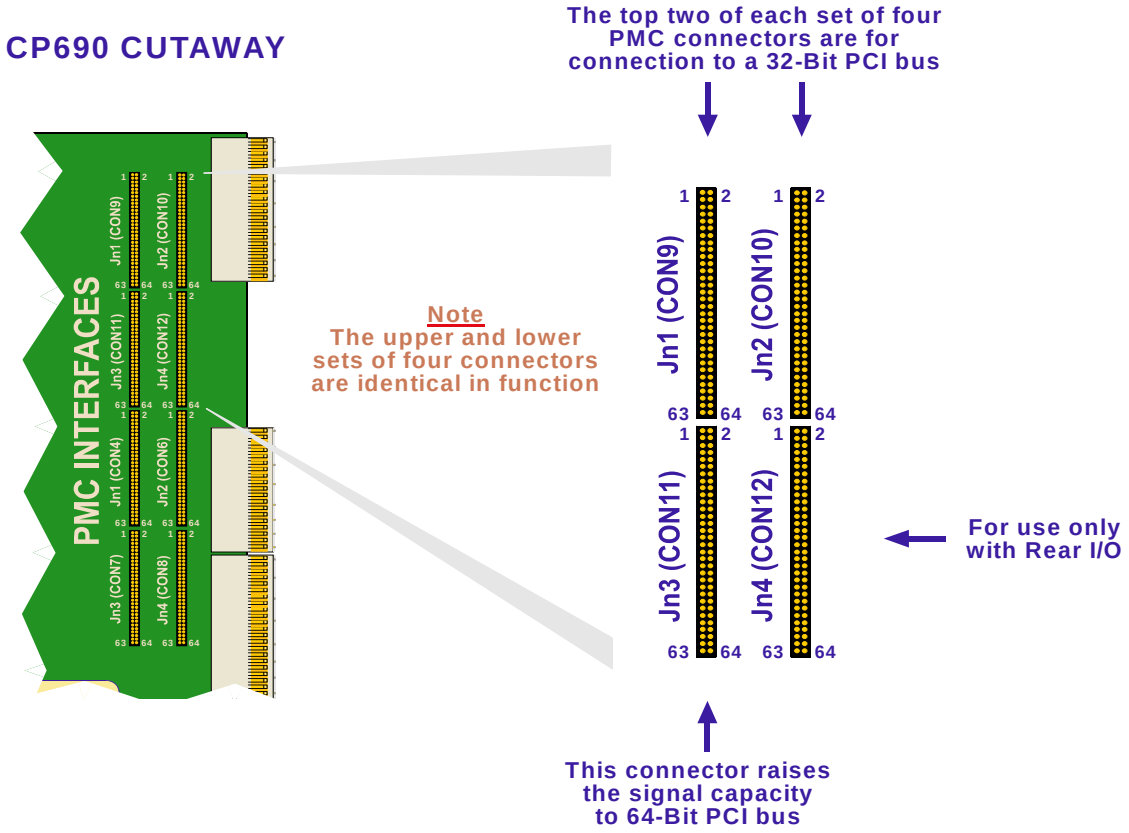
The two PMC interfaces on the CP690 provide an easy way to extend a CPCI system via the wide array of interfaces and functions which are available from all PMC vendors. The secondary (PMC) side of the PCI-to-PCI bridge provides a 32/64-bit wide PCI data path with a speed of up to 66 MHz which is routed to the onboard connectors Jn1, Jn2 and Jn3. These connectors also provide the power supply for the PMC module. The interfaces have been designed to comply with the IEEE 1386.1 specification which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor.

Additionally, the CP690-HS (Hotswap version) has been designed to comply with the CPCI Hotswap specification PICMG 2.1 R1.0, which means that the power supply of the PMC modules will be ramped up and a reset generated whenever the board is plugged into a running system.

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1.4.2.1 Functions of the PMC Interface Connectors

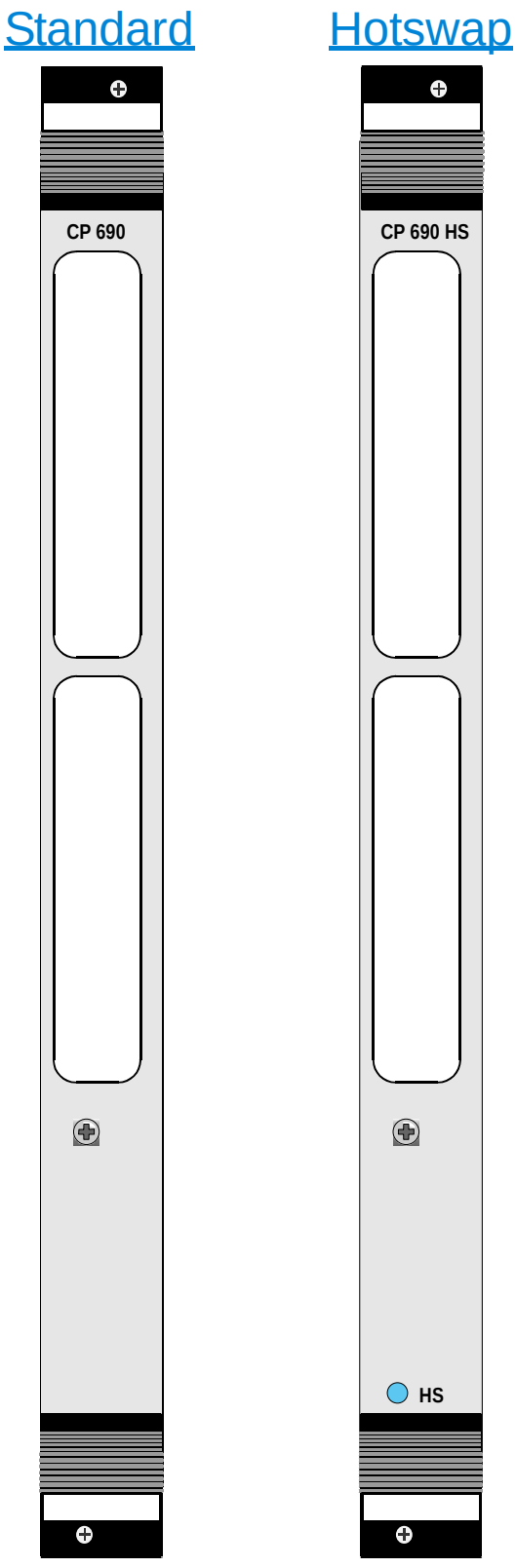
Figure 1-3: PMC Interface Functions



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1.5 Front Panels

Figure 1-4: Front Panels



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1.6 Technical Specifications

Table 1-1: CP690/CP690HS Specifications

CP690/CP690HS	Specifications
PCI-Standard	Compliant with PCI 2.1
Signaling Voltage	CPCI-Side: 3.3V / 5V tolerant PMC-Side: can be jumpered to 5V or 3.3V signaling (default 3.3 V)
Driver Support	A software driver is not required for data transfer
Connectors	PMC connectors: Jn1 (CON4, CON9), Jn2 (CON6, CON10), Jn3 (CON7, CON11), Jn4 (CON8, CON12) CPCI connectors: J1, J2, J3, J5
Mechanical Compliance	IEEE 1101.10 CMC IEEE P1386/Draft 2.0 (with minor exceptions)
Operating Voltage and Current	3.3V / 0.07 A (Core-Supply)
Temperature Range	Operation: • 0° to +60°C (standard) • -25° to +75°C (extended) Storage: • -55° to +85°C
Operating Humidity	5 – 95% (non-condensing)
Vibration and Broad-Band Random Vibration	IEC68-2-6 compliant IEC68-2-64
Shocks: Permanent Shocks Single Shock	 IEC68-2-29 IEC68-2-27
Board Dimensions	Double-height Eurocard: 233,35 mm x 160 mm 1 x 4 HP slot
Board Weight	275 grams

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1.7 Applied Standards

1.7.1 CE Compliance

The *Kontron Modular Computers'* CompactPCI systems comply with the requirements of the following CE-relevant standards:

- EmissionEN50081-1
- ImmissionEN50082-2
- Electrical SafetyEN60950

1.7.2 Mechanical Compliance

- Mechanical DimensionsIEEE 1101.10

1.7.3 Environmental Tests

- VibrationIEC68-2-6
  Random Vibration, BroadbandIEC68-2-64 (3U boards)
- Permanent ShockIEC68-2-29
- Single ShockIEC68-2-27

1.8 Related Publications

1.8.1 CompactPCI Systems/Boards

CompactPCI Specification, V. 2.0, Rev. 2.1

CompactPCI hotswap Specification, PICMG 2.1 R1.0

1.8.2 PMC Add-on Modules/Carriers

- Draft Standard for a Common Mezzanine Card Family, P1386/Draft 2.0
- Draft Standard Physical and Environment Layers for PCI Mezzanine Cards, P1386.1/Draft 2.0

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Chapter 2

Installation

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2. Installation

2.1 Board Installation



Caution!

If your CP690 carrier board is not the hotswap variant, it is essential to switch off the target system before installing the board in a free slot. Failure to do so could endanger your life/health and may damage your board or system.

ESD Equipment!



Your carrier board and PMC module contain electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch components, connector-pins or traces.

If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

PMC Module Installation

1. Place the EMC gasket on the bezel of your PMC-Module.



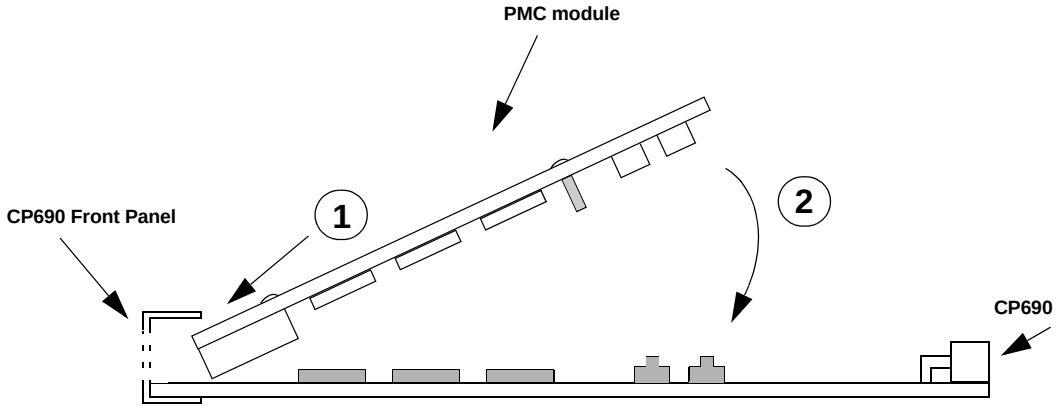
Note:

In order to support an active PMC carrier and thereby comply with the CompactPCI specification, it was necessary to place the PCI-to-PCI bridge in the position where one of the sockets for mounting a stand-off would normally be (PMC specification). There is, therefore, no second stand-off.

2. Push the PMC bezel into the window of the front-panel of the CP690 and plug the connectors together.
3. Use four screws (M2.5 x 6mm) to fix the board.

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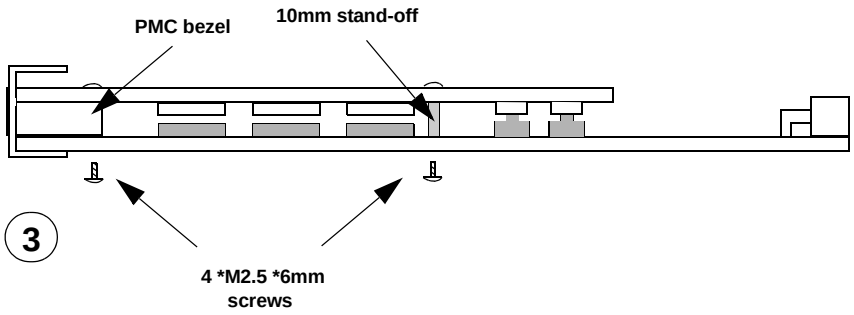
Figure 2-1: Installation Diagrams





Note:

Only one key is present on each carrier board, either 3.3V or 5V, depending on the signaling used. The two PMC modules must both be set to the same voltage, i.e. either both 3.3V or both 5V.



2.1.1 CPCI Signaling Voltage

The primary side of the PCI-to-PCI bridge, i.e. the CPCI side, has buffers for 3.3V signaling but works equally well in a 5V signaling environment.

The secondary (PMC) side of the PCI-to-PCI bridge may be configured either for a 3.3V or a 5V signaling environment. Please refer to chapter 3.2 Jumper Settings.

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Chapter 3

Configuration

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3. Configuration

3.1 Pinouts

3.1.1 CompactPCI J1 (CON1) Connector

Table 3-1: CompactPCI J1 (CON1) Connector Pinout

Pin	Z	A	B	C	D	E	F
25	GND	BE_5V	REQ64#	ENUM#	BE_3.3V	BE_5V	GND
24	GND	AD[1]	BE_5V	E_V(I/O) 2)	AD[0]	ACK64#	GND
23	GND	BE_3.3V	AD[4]	AD[3]	E_5V 2)	AD[2]	GND
22	GND	AD[7]	GND	E_3.3V 2)	AD[6]	AD[5]	GND
21	GND	BE_3.3V	AD[9]	AD[8]	NC	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	BE_3.3V	AD[15]	AD[14]	GND 2)	AD[13]	GND
18	GND	SERR#	GND	BE_3.3V	PAR	C/BE[1]#	GND
17	GND	BE_3.3V	NC	NC	GND 2)	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	BE_3.3V	FRAME#	IRDY#	BD_SEL# 1)	TRDY#	GND
14	--	--	--	--	--	--	--
13	--	--	--	--	--	--	--
12	--	--	--	--	--	--	--
11	GND	AD[18]	AD[17]	AD[16]	GND 2)	C/BE[2]#	GND
10	GND	AD[21]	GND	BE_3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL 1)	AD[23]	GND 2)	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND 2)	AD[27]	GND
6	GND	REQ#	GND	E_3.3V 2)	CLK	AD[31]	GND
5	GND	NC	NC	PCI_RST#	GND 2)	GNT#	GND
4	GND	NC	HEALTHY#	E_V(I/O) 2)	NC	NC	GND
3	GND	INTA#	INTB#	INTC#	E_5V 2)	INTD#	GND
2	GND	NC	BE_5V	NC	TDO	TDI	GND
1	GND	BE_5V	BE_-12V	NC	BE_+12V	BE_5V	GND

1) Indicates pins which connect with the shortest pins on the backplane
2) Indicates pins which connect with the longest pins on the backplane
The different pin lengths are related to Hot-swap functionality

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3.1.2 CompactPCI J2 (CON2) Connector

Table 1-2: CompactPCI J2 (CON2) Connector

Pin	Z	A	B	C	D	E	F
22	GND	NC	NC	NC	NC	NC	GND
21	GND	NC	GND	NC	NC	NC	GND
20	GND	NC	GND	NC	GND	NC	GND
19	GND	GND	GND	NC	NC	NC	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	NC	NC	NC	GND
16	GND	NC	NC	NC	GND	NC	GND
15	GND	NC	GND	NC	NC	NC	GND
14	GND	AD35#	AD34#	AD33#	GND	AD32#	GND
13	GND	AD38#	GND	V(I/O)	AD37#	AD36#	GND
12	GND	AD42#	AD41#	AD40#	GND	AD39#	GND
11	GND	AD45#	GND	V(I/O)	AD44#	AD43#	GND
10	GND	AD49#	AD48#	AD47#	GND	AD46#	GND
9	GND	AD52#	GND	V(I/O)	AD51#	AD50#	GND
8	GND	AD56#	AD55#	AD54#	GND	AD53#	GND
7	GND	AD59#	GND	V(I/O)	AD58#	AD57#	GND
6	GND	AD63#	AD62#	AD61#	GND	AD60#	GND
5	GND	C/BE5	64EN#	V(I/O)	C/BE4#	PAR64	GND
4	GND	V(I/O)	NC	C/BE7#	GND	C/BE6#	GND
3	GND	NC	GND	NC	NC	NC	GND
2	GND	NC	NC	NC	NC	NC	GND
1	GND	NC	GND	NC	NC	NC	GND

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3.1.3 CompactPCI J3 (CON3) Connector

Table 3-3: CompactPCI J3 (CON3) Connector

Pin	A	B	C	D	E	F
19	--	--	--	--	--	GND
18	--	--	--	--	--	GND
17	--	--	--	--	--	GND
16	--	--	--	--	--	GND
15	--	--	--	--	--	GND
14	3.3V	3.3V	3.3V	VCC	VCC	GND
13	PMC1IO5	PMC1IO4	PMC1IO3	PMC1IO2	PMC1IO1	GND
12	PMC1IO10	PMC1IO9	PMC1IO8	PMC1IO7	PMC1IO6	GND
11	PMC1IO15	PMC1IO14	PMC1IO13	PMC1IO12	PMC1IO11	GND
10	PMC1IO20	PMC1IO19	PMC1IO18	PMC1IO17	PMC1IO16	GND
9	PMC1IO25	PMC1IO24	PMC1IO23	PMC1IO22	PMC1IO21	GND
8	PMC1IO30	PMC1IO29	PMC1IO28	PMC1IO27	PMC1IO26	GND
7	PMC1IO35	PMC1IO34	PMC1IO33	PMC1IO32	PMC1IO31	GND
6	PMC1IO40	PMC1IO39	PMC1IO38	PMC1IO37	PMC1IO36	GND
5	PMC1IO45	PMC1IO44	PMC1IO43	PMC1IO42	PMC1IO41	GND
4	PMC1IO50	PMC1IO49	PMC1IO48	PMC1IO47	PMC1IO46	GND
3	PMC1IO55	PMC1IO54	PMC1IO53	PMC1IO52	PMC1IO51	GND
2	PMC1IO60	PMC1IO59	PMC1IO58	PMC1IO57	PMC1IO56	GND
1	V(I/O)	PMC1IO64	PMC1IO63	PMC1IO62	PMC1IO61	GND

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3.1.4 CompactPCI J5 (CON5) Rear I/O Connector

Table 3-4: CompactPCI J5 (CON5) Rear I/O Connector Pinout

Pin	A	B	C	D	E	F
22	--	--	--	--	--	GND
21	--	--	--	--	--	GND
20	--	--	--	--	--	GND
19	--	--	--	--	--	GND
18	--	--	--	--	--	GND
17	--	--	--	--	--	GND
16	--	--	--	--	--	GND
15	--	--	--	--	--	GND
14	--	--	--	--	--	GND
13	PMC2IO5	PMC2IO4	PMC2IO3	PMC2IO2	PMC2IO1	GND
12	PMC2IO10	PMC2IO9	PMC2IO8	PMC2IO7	PMC2IO6	GND
11	PMC2IO15	PMC2IO14	PMC2IO13	PMC2IO12	PMC2IO11	GND
10	PMC2IO20	PMC2IO19	PMC2IO18	PMC2IO17	PMC2IO16	GND
9	PMC2IO25	PMC2IO24	PMC2IO23	PMC2IO22	PMC2IO21	GND
8	PMC2IO30	PMC2IO29	PMC2IO28	PMC2IO27	PMC2IO26	GND
7	PMC2IO35	PMC2IO34	PMC2IO33	PMC2IO32	PMC2IO31	GND
6	PMC2IO40	PMC2IO39	PMC2IO38	PMC2IO37	PMC2IO36	GND
5	PMC2IO45	PMC2IO44	PMC2IO43	PMC2IO42	PMC2IO41	GND
4	PMC2IO50	PMC2IO49	PMC2IO48	PMC2IO47	PMC2IO46	GND
3	PMC2IO55	PMC2IO54	PMC2IO53	PMC2IO52	PMC2IO51	GND
2	PMC2IO60	PMC2IO59	PMC2IO58	PMC2IO57	PMC2IO56	GND
1	V(I/O)	PMC2IO64	PMC2IO63	PMC2IO62	PMC2IO61	GND

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3.1.5 PMC1 and PMC2 Jn1 Connector (CON4 / CON9) Pinout

Table 3-5: PMC1 and PMC2 Jn1 Connector (CON4 / CON9) Pinout

Pin Number	Signal Name	Signal Name	Pin Number
1	TCK	-12V	2
3	Ground	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5V	8
9	INTD#	PCI-RSVD*	10
11	Ground	PCI-RSVD*	12
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5V	18
19	V(I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V(I/O)	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5V	38
39	Ground	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	Ground	44
45	V(I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	Ground	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	V(I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	REQ64#	64

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3.1.6 PMC1 and PMC2 Jn2 Connector (CON6 / CON10) Pinout

Table 3-6: PMC1 and PMC2 Jn2 Connector (CON6 / CON10) Pinout

Pin Number	Signal Name	Signal Name	Pin Number
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	Ground	6
7	Ground	PCI-RSVD*	8
9	PCI-RSVD*	PCI-RSVD*	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE3#	14
15	3.3V	BUSMODE4#	16
17	PCI-RSVD*	Ground	18
19	AD[30]	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[24]	26
27	+3.3V	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]#	32
33	Ground	PCI-RSVD	34
35	TRDY#	+3.3V	36
37	Ground	STOP#	38
39	PERR#	Ground	40
41	+3.3V	SERR#	42
43	C/BE[1]#	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	PCI-RSVD	52
53	+3.3V	PCI-RSVD	54
55	PMC-RSVD	Ground	56
57	PMC-RSVD	PCI-RSVD	58
59	Ground	PCI-RSVD	60
61	ACK64#	+3.3V	62
63	Ground	PCI-RSVD	64

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3.1.7 PMC1 and PMC2 Jn3 64-bit PCI Extension Pinoutt

Table 3-7: Jn3 Connector (CON7 / CON11) Pinout

Pin Number	Signal Name	Signal Name	Pin Number
1	PCI-RSVD	Ground	2
3	Ground	C/BE[7]#	4
5	C/BE[6]#	C/BE[5]#	6
7	C/BE[4]#	Ground	8
9	V(I/O)	PAR64	10
11	AD[63]	AD[62]	12
13	AD[61]	Ground	14
15	Ground	AD[60]	16
17	AD[59]	AD[58]	18
19	AD[57]	Ground	20
21	V(I/O)	AD[56]	22
23	AD[55]	AD[54]	24
25	AD[53]	Ground	26
27	Ground	AD[52]	28
29	AD[51]	AD[50]	30
31	AD[49]	Ground	32
33	Ground	AD[48]	34
35	AD[47]	AD[46]	36
37	AD[45]	Ground	38
39	V(I/O)	AD[44]	40
41	AD[43]	AD[42]	42
43	AD[41]	Ground	44
45	Ground	AD[40]	46
47	AD[39]	AD[38]	48
49	AD[37]	Ground	50
51	Ground	AD[36]	52
53	AD[35]	AD[34]	54
55	AD[33]	Ground	56
57	V(I/O)	AD[32]	58
59	PCI-RSVD	PCI-RSVD	60
61	PCI-RSVD	Ground	62
63	Ground	PCI-RSVD	64

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3.1.8 PMC1: Jn4 Rear I/O Pinout

Table 3-8: Jn4 Connector (CON8) Pin Assignment

Pin Number	Signal Name	Signal Name	Pin Number
1	PMC1IO1	PMC1IO2	2
3	PMC1IO3	PMC1IO4	4
5	PMC1IO5	PMC1IO6	6
7	PMC1IO7	PMC1IO8	8
9	PMC1IO9	PMC1IO10	10
11	PMC1IO11	PMC1IO12	12
13	PMC1IO13	PMC1IO14	14
15	PMC1IO15	PMC1IO16	16
17	PMC1IO17	PMC1IO18	18
19	PMC1IO19	PMC1IO20	20
21	PMC1IO21	PMC1IO22	22
23	PMC1IO23	PMC1IO24	24
25	PMC1IO25	PMC1IO26	26
27	PMC1IO27	PMC1IO28	28
29	PMC1IO29	PMC1IO30	30
31	PMC1IO31	PMC1IO32	32
33	PMC1IO33	PMC1IO34	34
35	PMC1IO35	PMC1IO36	36
37	PMC1IO37	PMC1IO38	38
39	PMC1IO39	PMC1IO40	40
41	PMC1IO41	PMC1IO42	42
43	PMC1IO43	PMC1IO44	44
45	PMC1IO45	PMC1IO46	46
47	PMC1IO47	PMC1IO48	48
49	PMC1IO49	PMC1IO50	50
51	PMC1IO51	PMC1IO52	52
53	PMC1IO53	PMC1IO54	54
55	PMC1IO55	PMC1IO56	56
57	PMC1IO57	PMC1IO58	58
59	PMC1IO59	PMC1IO60	60
61	PMC1IO61	PMC1IO62	62
63	PMC1IO63	PMC1IO64	64

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3.1.9 PMC2: Jn4 Rear I/O Pinout

Table 3-9: Jn4 Connector (CON12) Pin Assignment

Pin Number	Signal Name	Signal Name	Pin Number
1	PMC2IO1	PMC2IO2	2
3	PMC2IO3	PMC2IO4	4
5	PMC2IO5	PMC2IO6	6
7	PMC2IO7	PMC2IO8	8
9	PMC2IO9	PMC2IO10	10
11	PMC2IO11	PMC2IO12	12
13	PMC2IO13	PMC2IO14	14
15	PMC2IO15	PMC2IO16	16
17	PMC2IO17	PMC2IO18	18
19	PMC2IO19	PMC2IO20	20
21	PMC2IO21	PMC2IO22	22
23	PMC2IO23	PMC2IO24	24
25	PMC2IO25	PMC2IO26	26
27	PMC2IO27	PMC2IO28	28
29	PMC2IO29	PMC2IO30	30
31	PMC2IO31	PMC2IO32	32
33	PMC2IO33	PMC2IO34	34
35	PMC2IO35	PMC2IO36	36
37	PMC2IO37	PMC2IO38	38
39	PMC2IO39	PMC2IO40	40
41	PMC2IO41	PMC2IO42	42
43	PMC2IO43	PMC2IO44	44
45	PMC2IO45	PMC2IO46	46
47	PMC2IO47	PMC2IO48	48
49	PMC2IO49	PMC2IO50	50
51	PMC2IO51	PMC2IO52	52
53	PMC2IO53	PMC2IO54	54
55	PMC2IO55	PMC2IO56	56
57	PMC2IO57	PMC2IO58	58
59	PMC2IO59	PMC2IO60	60
61	PMC2IO61	PMC2IO62	62
63	PMC2IO63	PMC2IO64	64

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3.2 Jumper Settings

The secondary side of the PCI-to-PCI bridge (the PMC side) may be configured either for a 3.3V or a 5V signalling environment. Configuration is effected by setting the resistors R57 or R56.

Table 3-10:Resistor Settings

R57	R56	Functions
Closed	Open	3.3V signalling
Open	*Closed*	5V signalling

The default setting is indicated by italics



Important!

No other jumper settings are permitted as serious damage or misoperation will result.



Note:

Care must be taken to ensure correct voltage configuration. Using an incorrect signalling voltage may damage the PMC module.

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Chapter 4

Hotswap

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4. Hotswap

4.1 Technical Background of CompactPCI Hotswap

In many modern application systems downtime is costly and/or unacceptable. Server applications, telecommunications networks and automated systems requiring continuous monitoring call for a system design in which a single card can be inserted or extracted without affecting the rest of the system. The ease with which a board may be removed and replaced is dependent on the mechanical design (form factor), the possibility of deactivating the software drivers for the board (operating system) and the possibilty of removing and inserting the board without disturbing the signal quality on the bus.

CompactPCI hotswap is currently the most effective way to meet this need. Staggered pins on the backplane guarantee controlled power sequencing of the board, while the signals ENUM, BDSEL, HEALTHY and the hotswap control and status register bits may be used to control board access from the software side.

4.1.1 Hotswap System

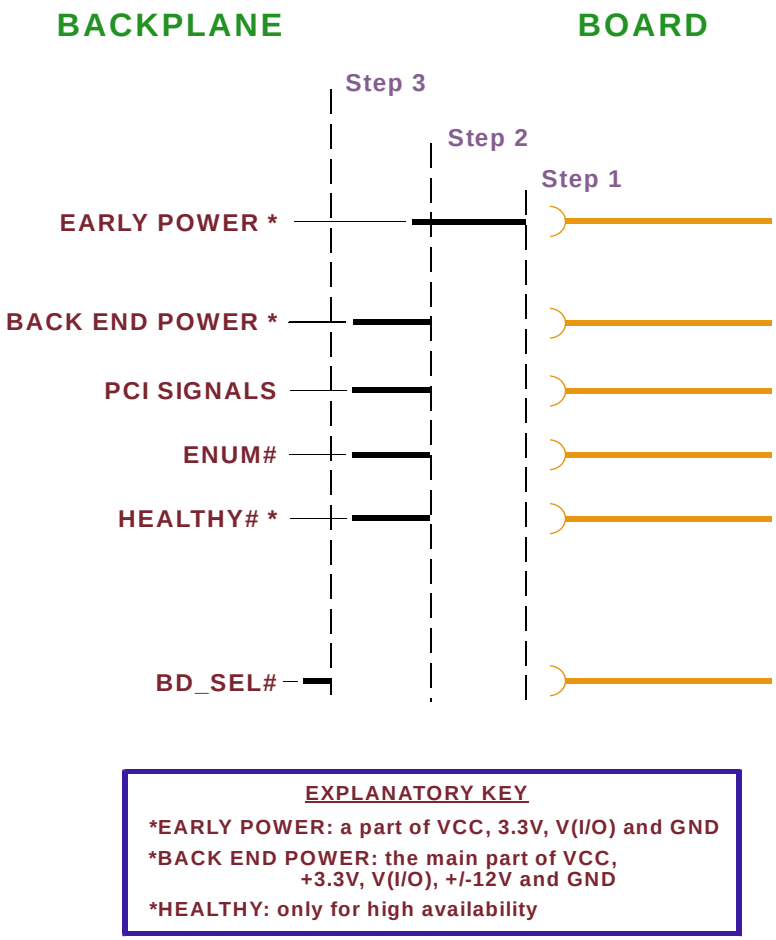
A hotswap system consists of a hotswap platform which comprises a hotswap backplane, the system host (CPU) with hotswap features, cooling, power supplies etc. plus the boards to be hotswapped. Hotswapping is not possible unless the operating system has the capability to enable and disable the board specific driver during normal operation.

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4.1.1.1 The Hotswap Backplane

The hotswap backplane has staggered pins to ensure defined power sequencing.

Figure 4-1: Illustration of Staggered Pinning on the Hotswap Backplane



Note:

Some special signals (e.g. ENUM, HEALTHY, BDSEL...) have particular routing requirements.

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4.1.1.2 The System Host (System Controller)

The System Controller must have the possibility to utilize the special signals defined by the CompactPCI hotswap specification. If a high availability system is used it must additionally be able to control the hardware connection with the peripheral boards (Hardware Connection Control).

4.1.1.3 The Hotswap Board

To ensure that a board may be removed and replaced in a working bus without disturbing the system it requires the following additional features.

- precharge
- power ramping
- hotswap control and status register bits
- automatic interrupt generation whenever a board is about to be removed or replaced.
- an LED to indicate that the board may be safely removed.

4.1.1.4 Software and Operating System

No hotswap support is currently provided by Intel based operating systems. Windows 2000, which is scheduled to become available in February 2000, is expected to provide hotswap support. Special software will require to be developed for other proprietary systems.

In a hotswap environment the software driver and the operating system have the following additional requirements:

- The OS must provide the possibility to initialize PCI devices during normal operation whenever required (allocate resources).
- The OS must provide the possibility to load or unload software drivers during normal operation whenever required.

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4.2 Design Implementation on CP690

4.2.1 Power Ramping

On the CP690, a special hotswap controller is used to ramp up the supply voltage of the PMC modules (Back End Power). This is done to avoid transients on the 3.3V and the 5V power supplies from the Hotswap system. When the power supply is stable, the hotswap controller generates a reset on the PMC slots to put the devices into a definite state.

4.2.2 Precharge

Precharge is provided on the CP690 by a resistor on each signal line (PCI bus), connected to a 1V reference voltage.

4.2.3 Handle Switch

A microswitch is situated in the extractor handle. Opening the handle initiates the generation of the ENUM interrupt (produced by the onboard logic).

4.2.4 ENUM# Interrupt

The onboard logic generates a low active interrupt signal to indicate that the board is about to be extracted from the system or inserted into the system.

4.2.5 Hotswap Control and Status Register / Statemachine

All hotswap peripheral boards provide a Hotswap Control And Status Register which provides information on the current state of the board. The defined bits in this register set are named, as follows:

Table 4-1: Hotswap Control and Status Register / Statemachine

Bit Name	Function
EXT	Indication of extraction process
INS	Indication of insertion process
LOO	Led on
EIM	ENUM mask bit

Due to the fact that no 64-bit transparent PCI-to-PCI bridge currently exists, which would provide built-in hotswap status registers, another way of implementing these bits had to be found.

The solution, therefore, is to put this information into the onboard logic.

Since on-chip registers handle read and write accesses in the same way, it is necessary to exercise care when configuring the PCI-to-PCI GPIOs (general purpose IOs).

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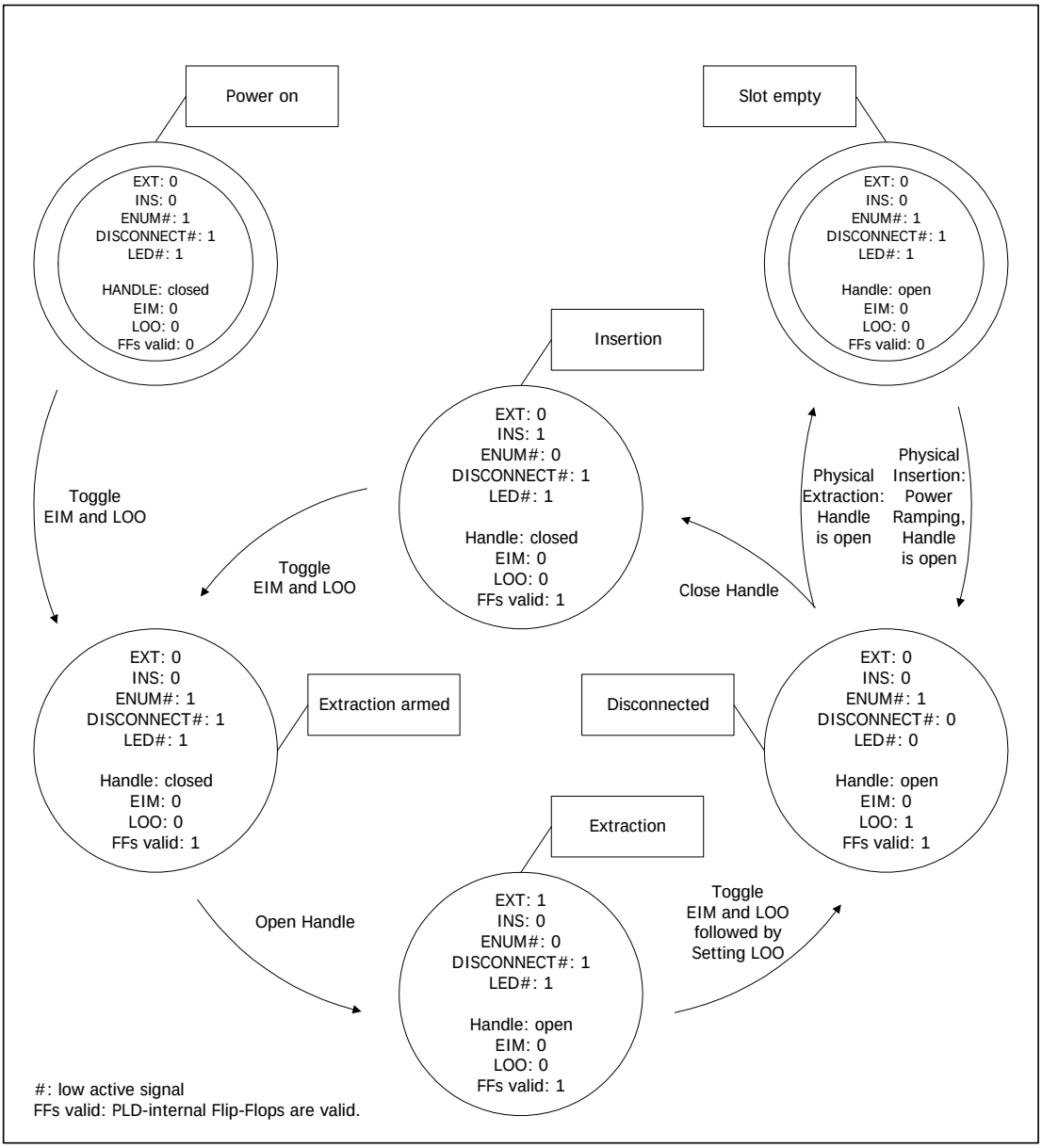
Table 4-2: Hotswap Register Bits

Bit Name	Signal on 21154
EXT	GPIO[2]
INS	GPIO[3]
LOO	GPIO[0]
EIM	GPIO[1]

Attention!

GPIO[2:3] have to be configured as inputs. A different configuration may damage your bridge device.

Figure 4-2: Hotswap State Machine



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4.2.6 Programming the GPIO's

This sub-chapter provides information for programming the GPIO's (General Purpose I/O's) of the PCI-to-PCI bridge.

4.2.6.1 GPIO: Output Enable Control Register - Offset 66h

This section describes the GPIO for the Output Enable Control Register.

Dword address = 64h

Byte enable p_cbe_1<3:0> = x0xxb

Table 4-3: GPIO Output Enable Control Gegister - Offset 66h

Dword Bit	Name	R/W	Description
19:16	GPIO output enable write-1-to-clear	R/W1TC	The gpio<3:0> output enable control write-1-to-clear. Writing 1 to any of these bits configures the corresponding gpio<3:0> pin as an input only; that is, the output driver is tristated. Writing 0 to this register has no effect. When read, reflects the last value written. Reset value: 0 (all pins are input only).
23:20	GPIO output enable write-1-to-set	R/W1TS	The gpio<3:0> output enable control write-1-to-set. Writing 1 to any of these bits configures the corresponding gpio<3:0> pin as bidirectional, that is, enables the output driver and drives the value set in the output data register (65h). Writing 0 to this register has no effect. When read, reflects the last value written. Reset value: 0 (all pins are input only).

4.2.6.2 GPIO Input Data Register - Offset 67h

This section describes the GPIO input data register.

Dword address = 64h

Byte enable p_cbe_1<3:0> = 0xxxb

Table 4-4: GPIO Input Data Register - Offset 67h

Dword Bit	Name	R/W	Description
27:24	Reserved	R	Reserved. Returns 0 when read.
31:28	GPIO input	R	This read-only register reads the state of the gpio<3:0> pins. This state is updated on the PCI clock cycle following a change in the gpio pins.

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4.2.6.3 GPIO Output Data Register - Offset 65h

This section describes the GPIO output data register.

Dword address = 64h

Byte enable p_cbe_1<3:0> = xx0xb

Table 4-5: GPIO Output Data Register - Offset 65h

Dword Bit	Name	R/W	Description
11:8	GPIO output enable write-1-to-clear	R/W1TC	The gpio<3:0> pin output data write-1-to-clear. Writing 1 to any of these bits drives the corresponding bit low on the gpio<3:0> bus if it is programmed as bi-directional. Data is driven on the PCI clock cycle following completion of the configuration write to this register. Bit positions corresponding to gpio pins that are programmed as input only are not driven. Writing 0 to these bits has no effect. When read, reflects the last value written. Reset value: 0.
15:12	GPIO output enable write-1-to-set	R/W1TS	The gpio<3:0> pin output data write-1- to-set. Writing 1 to any of these bits drives the corresponding bit high on the gpio<3:0> bus if it is programmed as bi-directional. Data is driven on the PCI clock cycle following completion of the configuration write to this register. Bit positions corresponding to gpio pins that are programmed as input only are not driven. Writing 0 to these bits has no effect. When read, reflects the last value written. Reset value: 0.

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