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VSBC-32

Combined VMEbus System Controller and Serial Communications Controller Board

Manual ID 21168, Rev. Index 04
Jul 00

The product described in this manual is in compliance with all applied CE standards.

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Imprint

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Preface

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Explanation of Symbols



CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.



Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.



Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.



Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.



Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

PEP Advantage

This symbol and title emphasize advantages or positive aspects of a product and/or procedure.

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For Your Safety

Your new *PEP* product was developed and tested carefully to provide all features necessary to ensure the renown electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interests of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions



Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.



Caution, Electric Shock!

However, serious electrical shock hazards exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable to avoid exposure to hazardous voltage.

Before installing your new *PEP* product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Special Handling and Unpacking Instructions



ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

- Do not handle this product out of its protective enclosure while it is not used for operational purposes, unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where safe work stations are not guaranteed, it is important for the user to be electri-cally discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or tracks on the board.

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General Instructions on Usage

- In order to maintain *PEP's* product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by *PEP Modular Computers* and described in this manual or received from *PEP* Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please, follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the following page of this manual.

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PEP Modular Computers grants the original purchaser of *PEP* products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of *PEP* are valid unless the consumer has the express written consent of *PEP Modular Computers*.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

PEP provides for repair or replacement of any part, assembly or sub-assembly at their own discretion, or to refund the original cost of purchase, if appropriate. In the event of repair, refunding or replacement of any part, the ownership of the removed or replaced parts reverts to *PEP Modular Computers*, and the remaining part of the original guarantee, or any new guarantee to cover the repaired or replaced items, will be transferred to cover the new or repaired items. Any extensions to the original guarantee are considered gestures of goodwill, and will be defined in the "Repair Report" issued by *PEP* with the repaired or replaced item.

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Chapter 1

Introduction

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1. Introduction

1.1 System Overview

The *PEP Modular Computers* product described in this chapter operates with the VMEbus architecture. In addition, some products also support the CXC and/or Enhanced CXC (eCXC) local mezzanine interface standards which represent a streamlined variant of the VMEbus standard itself. Thus a wide range of I/O functions for industrial applications are supplied. Some of the major advantages of the VMEbus standard are:

- internationally accepted VITA standards (VMEbus, CXC, eCXC);
- broad range of available VMEbus solutions
- scalable processor performance

In addition, in combination with (e)CXC technology the VMEbus equipment offers the following advantages:

- lower costs and optimized reliability thanks to reduced design complexity;
- compact I/O sub-systems thanks to easier I/O wiring.

For detailled information concerning the VMEbus and (e)CXC standards, please consult the VMEbus and CXC Specifications which are available via the *VMEbus International Trade Association (VITA): http://www.vita.com*.

Many system-relevant features that are specific for VMEbus systems can be found in the ANSI/VITA VME64 Standard and in the VITA/*PEP* CXC MPI Specification which, despite its name, applies also to VMEbus MPI carriers.

The VME64 Standard includes the following information:

- VMEbus Specification
- Signal Lines, Bus Modules, Typical Operation
- Electrical Specifications
- Mechanical Specifications

The CXC MPI Specification includes the following information:

- Mechanical dimensions
- Electrical specifications
- Interface description
- ID Byte assignment

With reference to the (e)CXC aspects of mixed VMEbus+CXC systems please refer also to the *PEP* CXC Reference Manual.

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1.2 Board Overview

1.2.1 Board-Specific Information

The VSBC-32(E) is a 3U (Enhanced) CXC combined system and communications controller board that can operate in either a VMEbus or a mixed VMEbus+CXC environment. The board is based on the Motorola Quad Integrated Communications Controller “QUICC” MC68(EN)360. Therefore, it is particularly suitable for system control functions within applications with communications requirements. Depending on the controller chip used, there are two board variants with different CPU frequencies. The board’s external interfacing consists of a twin RS232 interface connector, which can be extended by means of a variety of serial interface piggybacks and/or external serial interface modules. Other piggybacks provide DRAM/flash memory.

Some of the outstanding features of the product described in this manual are:

- VMEbus system and communications controller board
- Both VMEbus and eCXC connectivity
- Master/slave system controller functionality
- 32-bit Motorola MC68(EN)360 integrated CPU and communications controller
- 25Hz or 33Hz CPU frequency
- CPU on-chip background debugging
- 1, 4, 16, 32 or 64 MB DRAM
- 0, 0.5, 1, 2 or 4 MB flash memory
- 256kB or 1 MB SRAM
- 2kbit serial EEPROM
- 256kB or 1MB DIP (flash) EPROM
- Real-time clock (backed-up)
- Six different communication standards possible:
  - Serial I/O (RS232, RS485; RS422 on request)
  - Ethernet (10Base2, 10Base5 or 10BaseT Ethernet)
- Up to six frontpanel serial interface connectors
- Compatibility with external serial interface module CXM-SIO3
- Reset and Abort control (frontpanel buttons)
- Halt, watchdog and general-purpose status indicators (frontpanel LED’s)
- OS-9 and VxWorks® drivers

1.2.2 Board Variants

Two basic variants of the VSBC-32(E) with different processors are available. Depending on the controller chip used and the SRAM size, there are four variants of the VSBC-32(E) system and serial communications controller board. The distinctive features of the variants are listed in the following

- Ethernet capability
- CPU frequency
- SRAM size

The following basic board variants are available:

- VSBC-32: MC68360 processor, no Ethernet control capability.
- VSBC-32E: MC68EN360 processor, Ethernet control capability.

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The MC68EN360 processor is also available with two different clock rates:

- 25MHz
- 33MHz (this variant is again supplied with either 256kB or 1MB SRAM).

The below described frontend connectivity and interface expandibility are common to all board variants.

1.2.3 Board Connectivity and Interface Expandibility

The VSBC-32(E) mainboard is provided with the following standard connectors:

- Non-optoisolated RS232 serial interface (two RJ45 connectors, on frontpanel)
- One set of piggyback interface connectors for serial interface (SI) piggybacks (three 7-pin row male connectors)
- One set of memory piggyback interface connectors (two 50-pin row female connectors)
- Two sets of (flash) EPROM DIP sockets (two 32-pin row female sockets)
- Background debug mode (BDM) interface (one 12-pin row male connector)
- VMEbus backplane interface (one 96-pin DIN 41612, style C male connector)
- Enhanced CXC mezzanine interface (one 96-pin DIN 41612, style C male connector)

In addition, the mainboard external interfacing is usually integrated by one of the following piggyback-mounted frontpanel interface options (serial interface piggybacks). The kinds of piggyback that can be used depend on the mainboard variant.

Table 1-1: Serial Interface Piggybacks

Piggyback	Description	Board Variant
SI-PB232	Non-optoisolated RS232 serial interface (two RJ45 connectors)	VSBC-32, VSBC-32E
SI-PB485-ISO	Optoisolated RS485 serial interface (one 9-pin female DSUB connector)	VSBC-32, VSBC-32E
SI-10B2	10Base2 Ethernet interface (one RG58 coaxial connector)	VSBC-32E
SI-10B2	10Base2 Ethernet interface (one RG58 coaxial connector)	VSBC-32E
SI-10BT	10BaseT Ethernet interface (one RJ45 connector)	VSBC-32E

Applications requiring further communication interfaces may be upgraded by means of an external CXM-SIO3 serial interface module which provides the following interface extension possibilities:

- RS232 serial interface connectors (non-optoisolated)
- Serial interface piggyback ports
- Serial communications piggyback port

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Maximum one CXM-SIO3 module can be controlled by a VSBC-32(E) board. The CXM-SIO3 module provides access to internal communication signals of the base board that are transferred to the module via the CXC bus.

For a detailled list and description of the frontpanel interface and serial interface/communication piggybacks please refer to the “Serial Interface Piggybacks” appendix of this manual as well as to the CXM-SIO3 user’s manual and its “Serial Communications Piggybacks” appendix respectively.

1.2.4 Memory Piggybacks

The VSBC-32(E) mainboard is not provided with any on-board DRAM/flash. These are provided by special memory piggybacks (DM60x). By means of these piggybacks the following memory configurations are possible:

- ≤64MB of DRAM
- ≤4MB of flash/EPROM

For a detailled description of the memory piggybacks please refer to the “Memory Piggybacks” appendix of this manual.

1.2.5 System-Relevant Information

System Configuration

Up to twenty-one VSBC-32(E) boards can be installed in a VMEbus 3U rack. Please refer to the description of the VMEbus backplane connector in the Functional Description chapter of this manual. If used as a system controller, the board should be always installed in the system slot.

If a CXM-SIO3 or a CXM-SCSI module is used in combination with the VSBC-32(E), the module can be “sandwiched” with the controller, Communication between the controller and the I/O module being acchieved via the VSBC-32(E)’s on-board CXC connector.

Master/Slave Functionality

The VSBC-32(E) is a combined system and communications controller board provided with both a VMEbus backplane interface which can operate both as a VMEbus master and slave simultaneously. Thanks to this feature all twenty-one VSBC-32(E) boards possible in a VMEbus system can operate as VMEbus masters while at the same time sixteen of them can act as VMEbus slaves. The VSBC-32(E) VMEbus master/slave (or neither) operation is a function of the application software.

Bootstrap Loader

Via the VSBC-32(E) frontend serial interface connectors the flash memory of the board’s memory piggyback can be re-programmed by means of the Bootstrap Loader which is delivered already installed in the DM60x memory piggybacks. This standalone software has the capability of loading flash memory from Motorola S-records or from any absolute address. If the downloaded image does not work properly, the Bootstrap

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Loader can be re-entered, the memory contents analyzed and a further programming cycle initiated.



Warning!

To avoid damaging of your Bootstrap Loader and, consequently, leaving your board unusable, please read the separate Bootstrap Loader manual before re-setting the flash contents of your VSBC-32 board.

Operating Systems

The VSBC-32(E) can operate under the following operating systems:

- OS-9
- VxWorks®

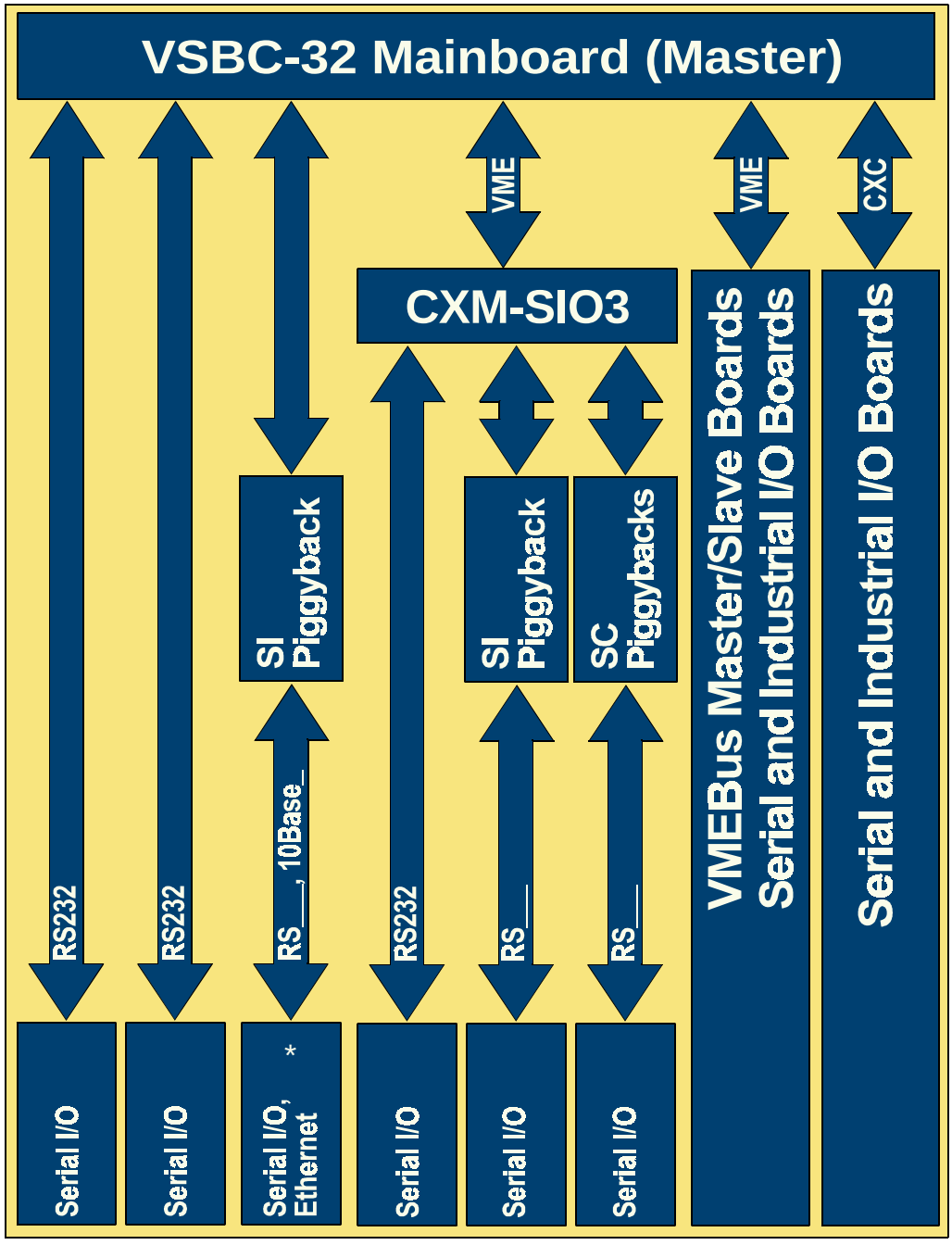
Drivers are available for both operating systems.
Porting to other operating systems on request.

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1.3 Board Diagrams

1.3.1 System-Level Functional Block Diagram

Figure 1-1: VSBC-32(E) System-Level Functional Block Diagram



Legend:

RS__[I]: RS232 non-optoisolated or RS485 optoisolated
10Base_: 10Base2 or 10Base5 or 10BaseT Ethernet

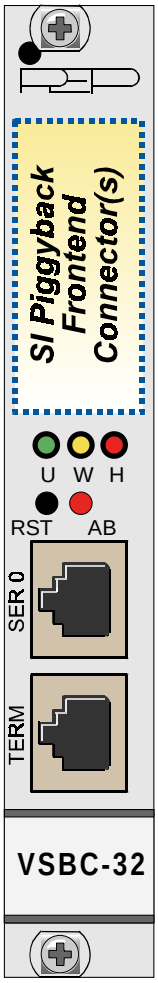
* Serial I/O or Ethernet (Ethernet with VSBC-32E only)

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1.3.2 Frontpanels

Figure 1-2: VSBC-32(E) Frontpanel



LED's:

- Green ("U"): General purpose
- Yellow ("W"): Watchdog
- Red ("H"): Halt

Pushbuttons:

- RST (left): Reset
- AB (right): Abort

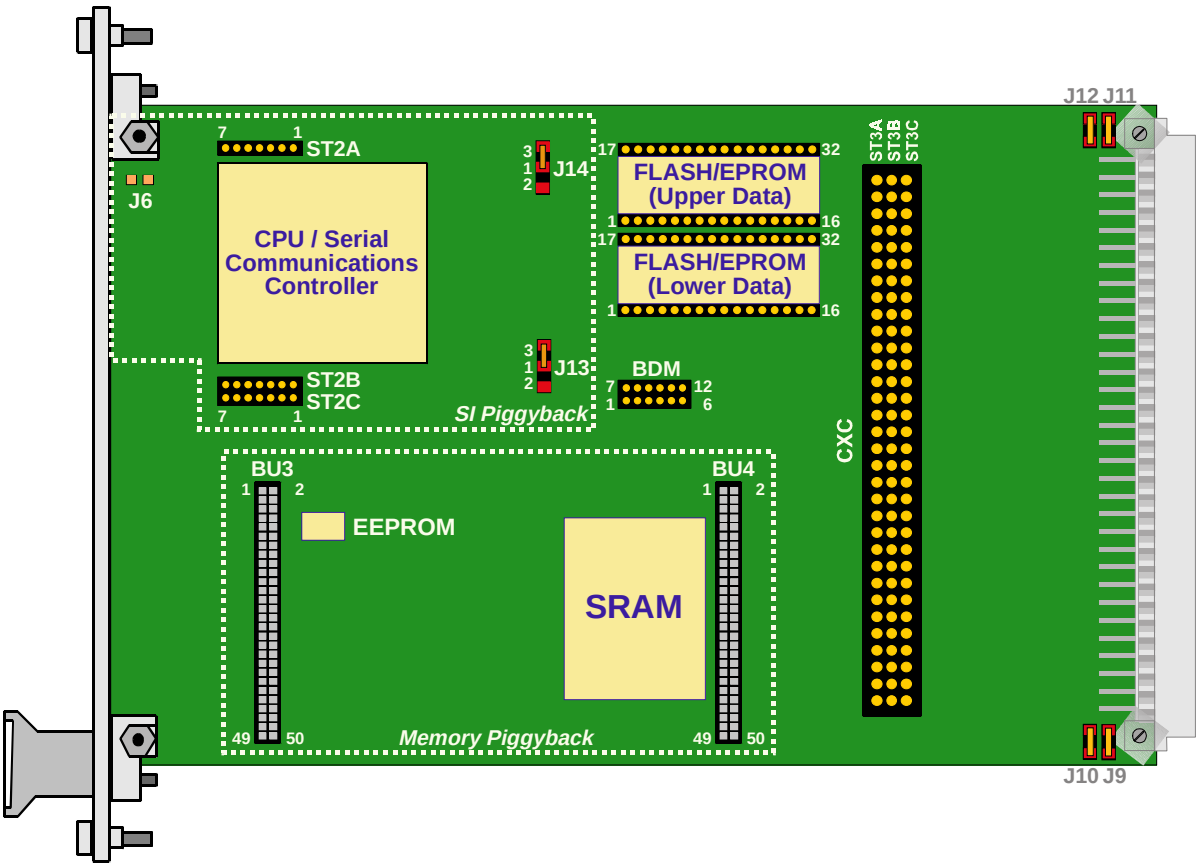
SI Piggyback Frontend Connector(s):

The additional frontend connector(s) depend(s) on the type of serial interface piggyback installed in combination with the VSBC-32(E) mainboard. For any details, please refer to the "Serial Interface Piggybacks" appendix in this manual.

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1.3.3 Board Layouts

Figure 1-3: VSBC-32(E) Board Diagram (front)]



FLASH/EPROM:

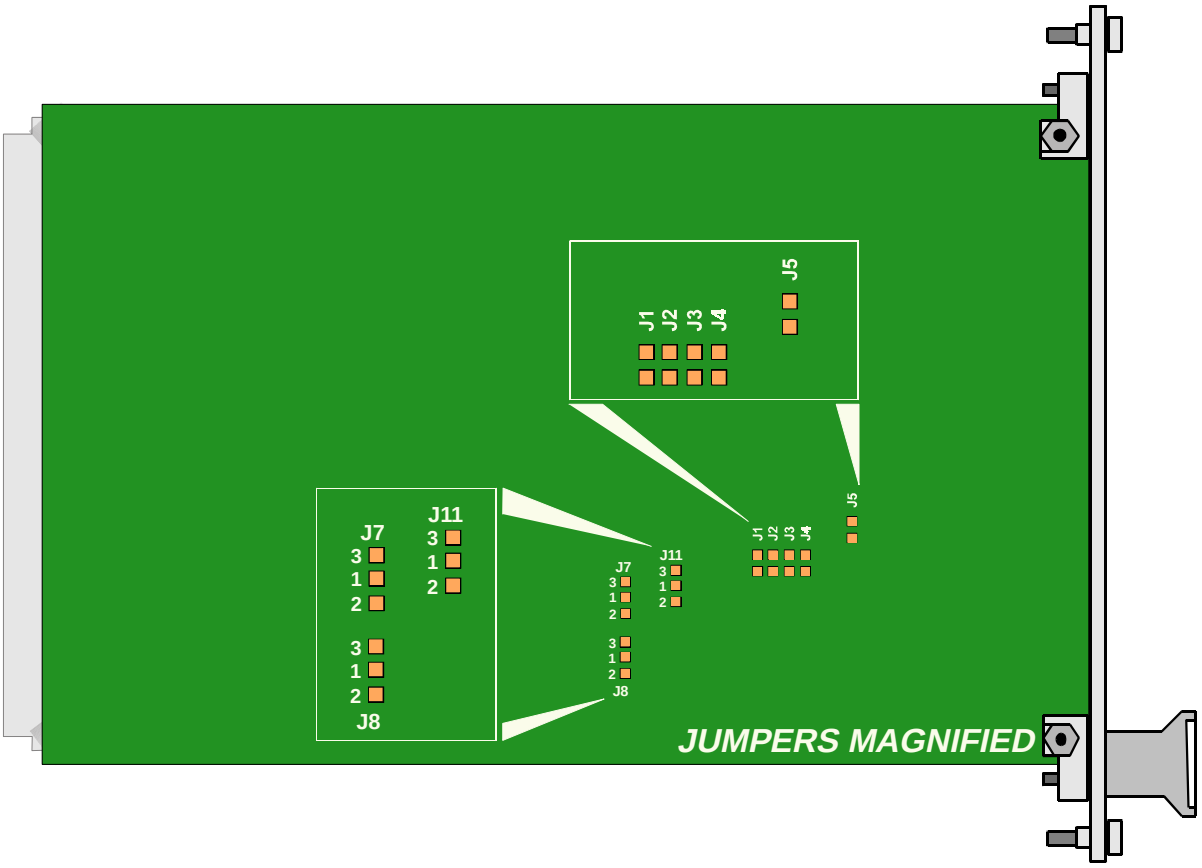
Upper Data: D8-D15, even Byte addresses
Lower Data: D0-D7, odd Byte addresses

BDM: Background Debug Mode.

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Figure 1-4: VSBC-32(E) Board Diagram (reverse)]



Warning!

Solder jumpers are factory-set. To avoid possible damage to your equiment, please do not alter them.

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1.4 Technical Specifications

Table 1-2: VSBC-32(E) Technical Specification (Sheet 1 of 3)

VSBC-32(E)	Specification
Board Variants	• VSBC-32: MC68360 processor, • VSBC-32E: MC68EN360 processor
Combined CPU/Serial Communications Controller	• MC68360: 25 MHz, no Ethernet capability • MC68EN360: 25MHz or 33 MHz, Ethernet capability CPU performance: Equivalent to Motorola CPU32 Serial I/O perform.: RISC, 14 dedicated DMA channels
On-Board Memory	• SRAM 256kB or 1MB (dual-ported, backed-up by means of Gold-Caps) *Note: 1MB with VSBC-32E only.* • EEPROM 2 kbit (serial); 1 kbit available for applications • Flash/EPROM 256kB or 1MB DIP EPROM/flash, 16-bit access Minimum access time - 120ns
Memory on Piggybacks	• DRAM 1, 4, 16 or 32 MB, 32-bit access • Flash 0, 0.5, 1, 2 or 4 MB, 32-bit access
VMEbus Master/Slave Functionality	• Master A24:D16/D8, arbitration, AM codes • Slave A24:D16, dual-port RAM, mailbox IRQ
Interrupt Control	7-level CXC/VME IRQ handler, maskable via CXC/VME interrupt mask register; system vectors: • ACFAIL* (via VME)Level 7 autovectored • Abort Level 7 autovectored • Tick Level 6 autovectored • Mailbox IRQ Level 5 autovectored, maskable • SYSFAIL* Level 3 autovectored 16 on-board interrupters; levels/vectors programmable
Programmable Timers	• Tick: Periodic-interrupt timer • Watchdog: 512ms time-out for reset • On-board bus error:8µs • General-purpose: 4*16 bit or 2*32 bit
Special Functions	*Real-time clock (backed-up):* • Date (year, month, week, day) • Time (hour, minute, second) *2kbit serial EEPROM:* • 1kbit for board specific data (serial number, IP address etc.) • 1kbit for application purposes *DMA:* 2 additional independent channels (transfers between DRAM, FLASH, VME and CXC)

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Table 1-2: VSBC-32(E) Technical Specification (Sheet 2 of 3)

VSBC-32(E)	Specification
Communication Standards	• Serial I/O (RS232, RS422, RS485) • Ethernet (VSBC-32E only)
Mainboard Connectivity	• Non-optoisolated RS232 serial interface (two RJ12 connectors, on frontpanel) • One set of piggyback interface connectors for serial interface (SI) piggybacks (two 13-pin row fe/male connectors) • One set of memory piggyback interface connectors (two 50-pin row fe/male connectors) • Background debug mode (BDM) interface (one 12-pin row male connector) • VMEbus backplane interface (one 96-pin DIN 41612, style C male connector) • Enhanced CXC mezzanine interface (one 96-pin DIN 41612, style C male connector)
Interface Expandibility	*Serial interface piggybacks:* • SI-PB232: non-optoisolated RS232 serial interface (two RJ45 connectors) • SI-PB485-ISO: optoisolated RS485 serial interface (two RJ45 connectors) • SI-10B2: 10Base2 Ethernet interface (one RG58 coaxial connector) • SI-10B5: 10Base5 Ethernet interface (one 15-pin DSUB female connector) • SI-10BT: 10BaseT Ethernet interface (one RJ45 connector) *Note: SI-10B_ with VSBC-32E only.* *External serial interface modules:* • CXM-SIO3 Up to one module.
Front-End Functions	*Pushbuttons:* • Reset button • Abort button *LED's:* • Red: Halt • Yellow Watchdog • Green General purpose
Data Retention	*Short-term backup (RTC and SRAM):* Via on-board gold-cap. Typ. 2µA/3V -> 150 hours *Long-term backup:* Via VME 5V stand-by line; automatic switching between 5V stand-by and internal gold-cap. Typ. 30µA/3V
Power Supply	Typically: 5V With SI-PB5B: 12V

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Table 1-2: VSBC-32(E) Technical Specification (Sheet 3 of 3)

VSBC-32(E)	Specification
Power Consumption	• VSBC-32: typ. 3.0W • VSBC-32E: typ. 3.5W
Temperature Ranges	Operation: 0°C to 70°C (standard) -40°C to +85°C (extended) Storage: -55°C to +125°C
Humidity	0..95%, non-condensing
Dimensions	4HP/3U Eurocard (100mm x 160mm)
Weight	Mainboard: 130g Serial interface piggyback: 20..30g Memory piggyback: 30g

1.5 Applied Standards

1.5.1 CE Compliance

The *PEP Modular Computers'* VMEbus and (e)CXC systems comply with the requirements of the following CE-relevant standards:

- Emission EN50081-1
- Immission EN50082-2
- Electrical Safety EN60950

1.5.2 Mechanical Compliance

- Mechanical Dimensions IEEE 1101.10

1.5.3 Environmental Tests

- Vibration IEC68-2-6
- Permanent Shock IEC68-2-29
- Single Shock IEC68-2-27

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1.6 Related Publications

1.6.1 VMEbus/CXC Systems/Boards

- ANSI/VITA: VME64 Draft Specification 1-1994, Rev. 1.9
- VITA: CXC Specification, Rev. 2.0
- *PEP Modular Computers* CXC MPI Draft Specification, Rev. 3.1 (ID 12190)
- *PEP Modular Computers* CXC Reference Manual, ID 05263
- *PEP Modular Computers* CXM-SIO3 Manual (ID 14411)
- *PEP Modular Computers* CXM-SCCI Manual (ID 03545)

1.6.2 Manufacturers' Component Documentation

- Motorola: MC68EN360 Quad Integrated Communications Controller User's Manual
- EM Microelectronic:V3021 1-Bit Real-Time Clock Datasheet
- XICOR:X25C02 SPI Serial EEPROM Datasheet

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Chapter 2

Functional Description

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2. Functional Description

2.1 General Information

The VSBC-32(E) is a 3U VMEbus combined system and communications controller board based on the Motorola Quad Integrated Communications Controller “QUICC” MC68(EN)360. Depending on the controller chip used and the SRAM size, there are four board variants with different characteristics. The following table provides an overview of the various VSBC-32(E) board variants.

Table 1-1: VSBC-32(E) Board Variants

Board Name	Processor	Ethernet Capability	Processor Frequency	SRAM Size
VSBC-32	MC68360	—	25MHz	256kB
VSBC-32E	MC68EN360	+	25MHz	256kB
		+	33MHz	256kB
		+	33MHz	1MB

Being the MC68(EN)360 a CPU and serial communications controller, it is particularly suitable for system control functions within applications with communications requirements such as LAN, WAN or fieldbusses (CAN, LON, PROFIBUS).

In fact, both the VSBC-32 and the VSBC-32E allow for a wide range of serial interfaces based on the MC68(EN)360 controller which is able to handle up to six serial communications channels. The channels can be configured in the following way:

- Two service / debug interface connectors (SMC interface, RxD/TxD, RS232 only)
- Four full modem interface connectors / multiprotocol channels (SCC interfaces).

Thus, the VSBC-32(E) mainboard comes complete with two non-optoisolated RS232 external interfaces which are located on the lower half of the front panel. However, the external serial interfacing can be extended by means of a variety of serial interface (SI) piggybacks and/or a CXM-SIO3 type external serial interface module. This external module can be either “sandwiched” with the controller or placed to the right of the VSBC-32(E). In the first case, communication between the controller and the I/O module is acchieved via the VSBC-32(E)’s on-board CXC connector, in the second case via the VMEbus.

As the CXM-SIO3 can be used again as a carrier for various serial interface (SI) and serial communications (SC) piggybacks, the VSBC-32/CXM-SIO3 tandem represents a really powerful and versatile sytem control and serial communications control set.

Together with the two service/debug interfaces, a maximum of three (four with the serial interface piggyback fitted) completely configured serial interfaces are available for the base board. Three (two with serial interface piggyback fitted) serial interfaces may be configured via the VMEbus where three of the four full modem Interfaces are routed.

The VSBC-32(E) allows also a significant variety of memory configurations, mainly DRAM and flash memory located on special memory piggybacks, add-on flash/EPROM on DIP sockets, battery backed-up SRAM and EEPROM.

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2.2 Specifics

2.2.1 System Control Functionality

Under the aspect of system control the on-chip 32-bit CPU core of the Motorola MC68(EN)360 provides system integration at different processor frequencies. The processor core acts essentially as a Motorola CPU32 microprocessor operating at 25MHz or 33MHz without cache memory. In addition, the MC68(EN)360 offers background debugging via the on-chip “Background Debug Mode” which allows direct communication with the CPU.

To act as a system controller, the VSBC-32(E) is provided with arbiter, system clock driver, power monitor with system reset driver, IACK daisy chain driver and 7-level VMEbus interrupt controller.

Arbitration is single-level FAIR (compare VME64 Specification Rule 3.14/Observation 3.17). If the VSBC-32(E) is used as a system controller and consequently placed in the VMEbus backplane’s system slot, a special detection function provided by the board makes any “slot 1” jumper setting superfluous. The VSBC-32(E) also provides a bus monitor for the VMEbus.

Interrupt Control

The interrupt control logic of the MC68(EN)360 processes internal interrupt requests alongside with external autovectored interrupt requests and a “mailbox” interrupt request from the VMEbus control/status register. The interrupt control logic is built up using the processor’s internal interrupt control and an external IRQ7 interrupt handler.

Internal requests are related to all interrupt requests caused by the controller sources, including the processor’s system integration functions (watchdog timer, periodic interrupt timer) and the communications processor module (RISC controller, timers, DMA’s, SCC’s etc.).

In order to avoid conflicts regarding the different interrupt levels, it is recommended to use IRQ level 4 for the MC68(EN)360 CPU internal requests and IRQ level 6 for the MC68(EN)360 serial controller internal requests.

In addition, external interrupt sources can generate autovectored interrupts and an external VMEbus master may require an interrupt by setting a “mailbox” IRQ in the VMEbus control/status register.

For any detailled information as well as a complete list of the Motorola® MC68(EN)360 controller signals please refer to the relating Data Sheet.

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Table 2-2: External Autovector and Mailbox Interrupts

Source	Interrupt Source	Interrupt Type
ABORT / ACFAIL	MC68(EN)360, pin IRQ7	Autovector 7
Reserved	MC68(EN)360, pin IRQ6	Autovector 6
Mailbox IRQ	MC68(EN)360, pin IRQ5	Autovector 5
Reserved	MC68(EN)360, pin IRQ4	Autovector 4
SYSFAIL	MC68(EN)360, pin IRQ3	Autovector 3
Reserved	MC68(EN)360, pin IRQ2	Autovector 2
Reserved	MC68(EN)360, pin IRQ1	Autovector 1
Mailbox Pending	Bit P_IRQ5	Control/status register

2.2.2 Memory Configurations

The VSBC-32(E) allows a significant variety of memory configurations. The special DRAM/flash piggybacks (DM60x), for instance, allows the user to take advantage of the on-board programming facility to produce low cost upgrades by simply overwriting existing stored data. This memory can be configured with different memory options allowing remarkable flexibility when customizing memory requirements for real-time applications.

The DM60x piggybacks provide between 1MB and 64MB of DRAM with 32-bit access and up to 4MB of +5V flash memory. In addition, a set of DIP sockets located on the VSBC-32(E) mainboard allows the installation of an additional 1MB of flash/EPROM. Both memory devices can be used for bootstrapping. The selection of the boot memory is achieved by hardware jumpering.



Note...

Physically the DM60x piggybacks provide up to 64MB of DRAM. However, the IUC-32(E) mainboard envisages addressing for up to two memory banks of 64MB each.

Exchange and retention of system relevant data from the VMEbus to the CPU/DMA and viceversa is provided by means of 256kB or 1MB of a 16-bit wide dual-ported SRAM which is backed-up using Gold Caps. Both the VMEbus users and the on-board CPU have access to the SRAM memory.



Note...

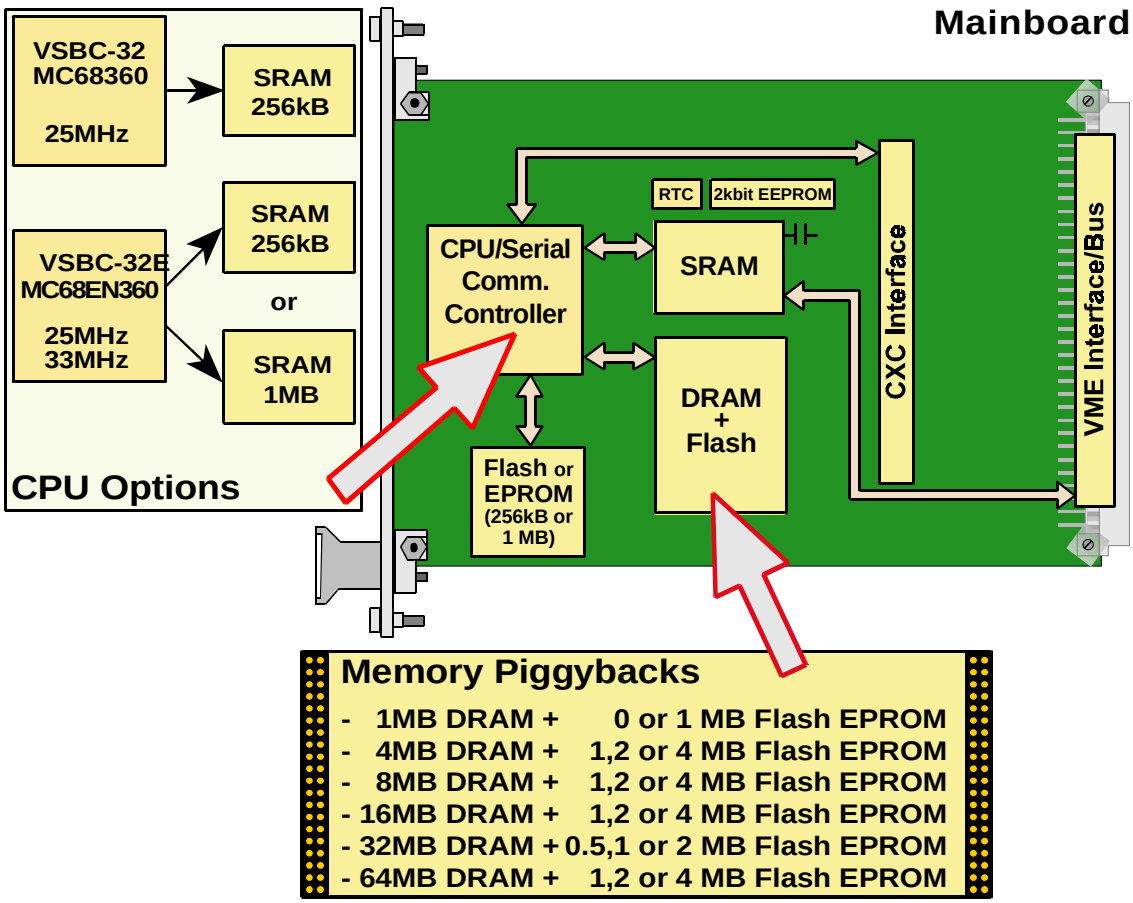
The upper 8kB of dual-ported SRAM are accessed by the VMEbus, the lower 8kB are reserved for mailbox interrupts.

Configuration data are stored in a 2kbit EEPROM. 1kbit is used for factory-specific configuration purposes, and 1kbit is available for application-specific configuration data.

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A schematic overview of all possible memory configurations is given in the figure on the next page.

Figure 2-1: VSBC-32 Memory Configuration Variants



2.2.3 DMA Channels

Two independent channels are provided by the MC68(EN)360 controller chip and can be used by applications requiring data transfer between VMEbus modules (as well as CXC modules, if present), DRAM, flash memory and dual-ported SRAM.

Memory-to-memory transfers with the DMA's of the MC68(EN)360 are possible with any combination of on-board and VMEbus addresses.

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2.2.4 Serial Communications Control

Under the aspect of serial communications control, a major advantage of the MC68(EN)360 serial communications controller core SIM60 is its compatibility with all important communication standards. A detailled description of all control functions is provided on the following pages alongside with a comprehensive list of the possible serial interface piggybacks and their connectors.

For the mainboard interface connector pinouts refer also to the “Board Interfaces” section of this chapter. For a description and pinouts of the connectors of the serial interface/communication piggybacks as well as of the CXM-SIO3 frontpanel interface connectors please refer instead to the “SI Piggybacks” appendix of this manual as well as to the CXM-SIO3 user’s manual and its “Serial Communications Piggybacks” appendix respectively.

Communication Standards and Protocols

Six communication standards are available on the VSBC-32(E):

- Serial I/O (RS232, RS485; RS422)
- Ethernet (10Base2, 10Base5, 10BaseT)

Serial communications using the RS232 standard are available on the VSBC-32(E) mainboard frontpanel as well as on a dedicated piggyback to be connected to its SI Interface. In addition, RS232 communication is possible via a CXM-SIO3 external serial interface module. Communications using the PROFIBUS protocol are supported by an optoisolated, half-duplex RS485 serial I/O interface implemented on a dedicated piggyback to be connected to the SI Interface of either the VSBC-32(E) or the external serial interface module. RS422 is not commonly available on the VSBC-32(E) but can be supplied by *PEP Modular Computers* on special request.

The MC68(EN)360 processor is specified to support also a full set of IEEE 802.3/Ethernet CSMA/CD media access control and channel interface functions. Since the controller requires an external interface adapter and transceiver function, the Ethernet interface can be adapted to all standard Ethernet functions, such as 10BaseT, 10Base5 and 10Base2 via a piggyback connected to the SI Interface on the VSBC-32(E).



Note...

The CXC bus does not support a 12V power supply. Therefore, the 10Base5 Ethernet piggyback SI-10B5 cannot be used on the IUC-32(E) controller board.

Serial I/O Channelling

The VSBC-32(E) mainboard is provided with TxD and RxD signals by the controller’s SMC1 and SMC2 channels and supply RS232 interface software handshake (XON/XOFF) capability. They are configured as service/debug connectors by default.

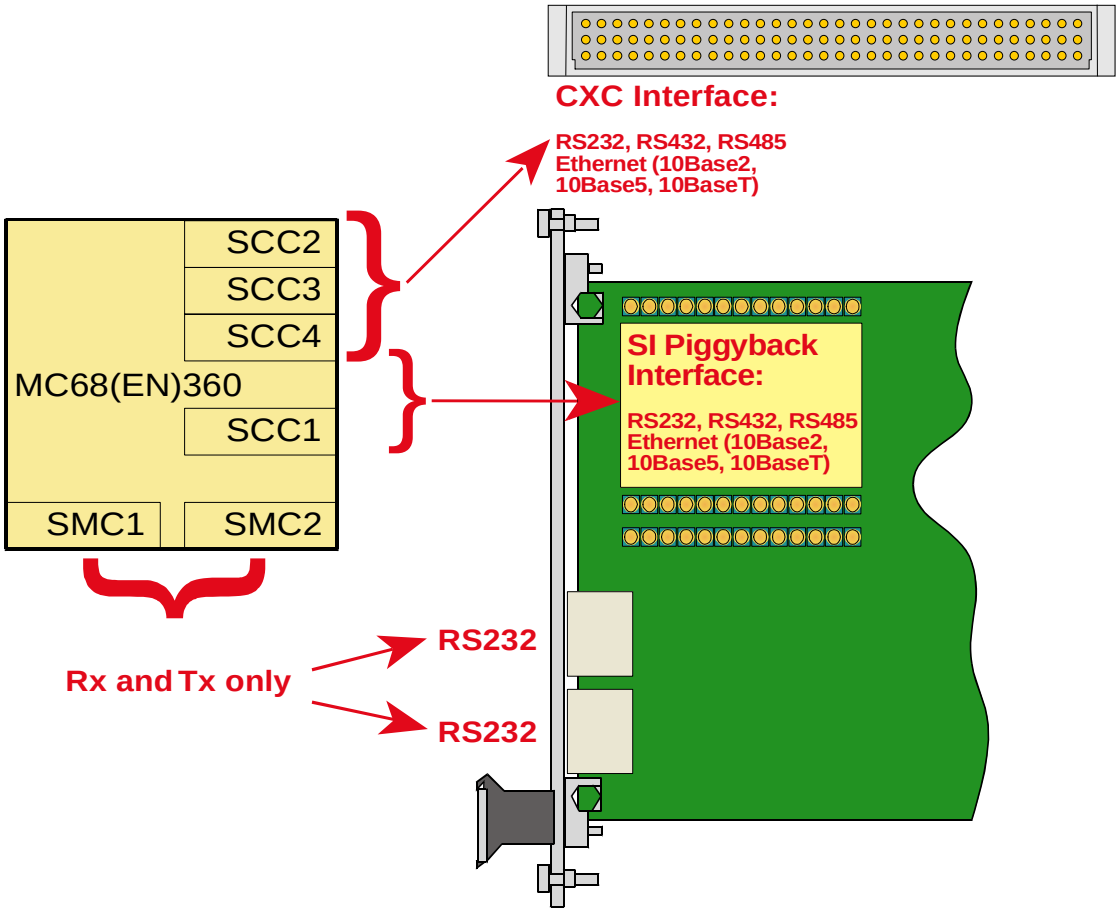
All full modem interfaces located on the piggybacks and/or CXM-SIO3 external serial interface module supply RxD, TxD, RTS, CTS, CD, DTR and RCLK/TCLK. Two of the full modem interfaces can be configured on the piggyback interface with a variety of

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serial interface (SI) piggybacks (RS232, RS485, Ethernet). The SCC1 channel of the MC68(EN)360 provides the interface to the serial interface (SI) piggyback installed on the VSBC-32(E). All other channels of the controller (SCC2, SCC3 and SCC4) are ported to the CXC interface except for the SI-PB232 piggyback which has on-board additional control provided by the SCC4 channel through the piggyback interface for serial interface piggybacks.

Thanks to the fact that three out of four SCC channels are routed to the CXC interface connector, also an CXM-SIO3 external serial interface module can be installed in the system, which therefore becomes a sort of “privileged” serial I/O extension of the VSBC-32(E) board itself. In addition to two non-optoisolated RS232 serial interface connectors the external serial interface module supports again a serial interface piggyback and up to three serial communications piggybacks with the relating interfacing options. Maximum one CXM-SIO3 module can be controlled by an VSBC-32(E) board.

Figure 2-2: MC68(EN)360 Serial Communication Channeling



Note...

The serial channel SCC4 is routed to both the piggyback interface for serial interface piggybacks and the CXC and can be used by either one or the other, not both at the same time.

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Depending on whether the piggyback interface for serial interface (SI) piggybacks is configured as an Ethernet port (board versions with Ethernet piggyback) or not, the serial interfaces channels of the VSBC-32(E) can assume the functions described in the following figure.

Figure 2-3: VSBC-32(E) Serial Interface Channel Configurations

Port	Serial Communication Channel	Interface Location
Service/Debug 1	SMC1	Mainboard, upper RJ12
Service/Debug 2	SMC2	Mainboard, lower RJ12
Ethernet	SCC1	Mainboard, serial interface piggyback
Full MODEM 1		
Full MODEM 2	SCC2	External serial interface module
Full MODEM 3	SCC3	External serial interface module
Full MODEM 4	SCC4	External serial interface module[1]
		Mainboard or Serial interface piggyback or External serial interface module

Legend:

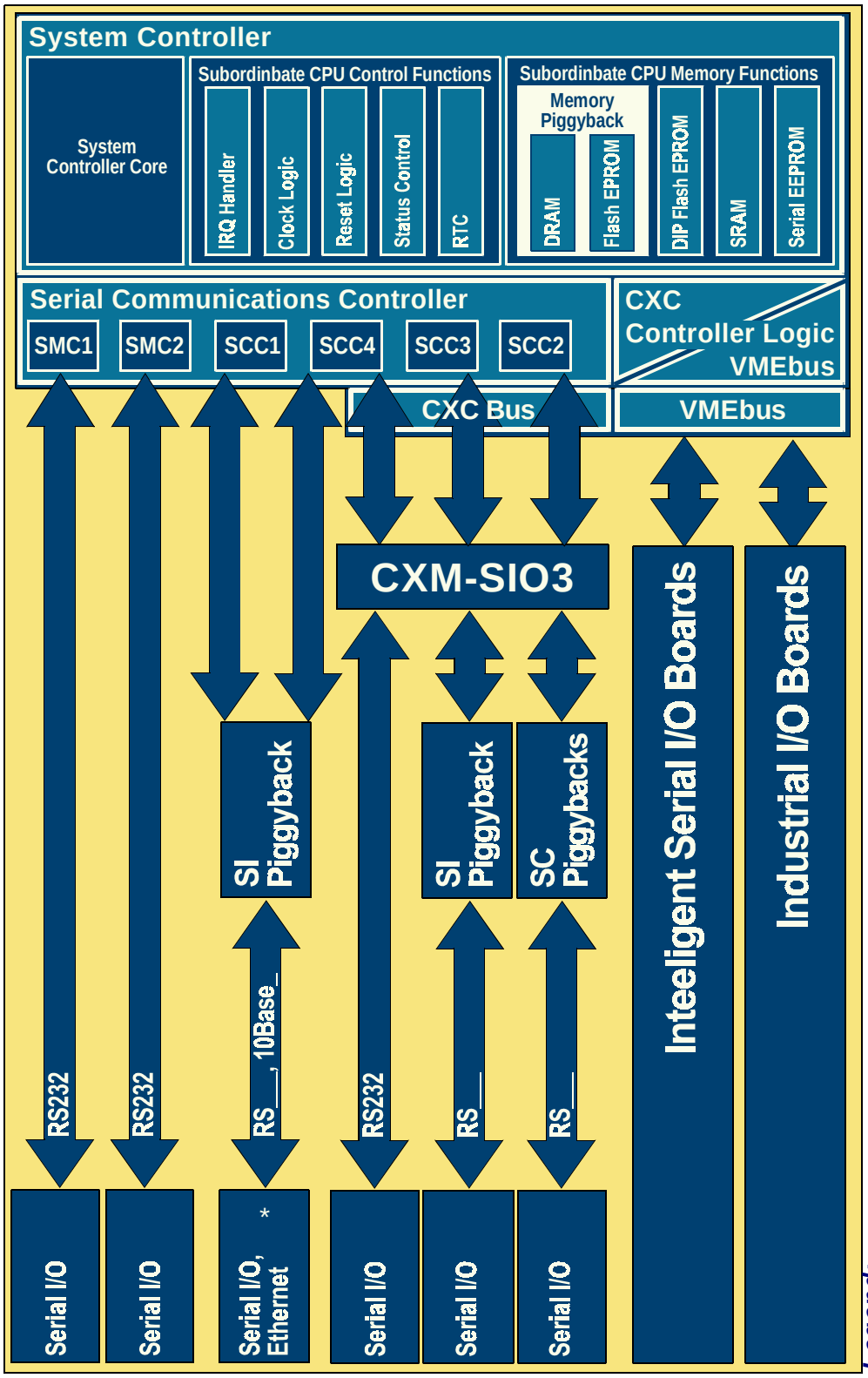
- Board versions with Ethernet port
- Board versions without Ethernet port
- Independent of Ethernet configuration

1 *SCC4 is not used by any of the Ethernet piggybacks. With these piggybacks, SCC4 can be used on the CXC bus.*

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2.3 Functional Block Diagram

Figure 2-4: VSBC-32 Board-Level Functional Block Diagram



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2.4 Board Interfaces

The following section provides a description of the mainboard interface connector pinouts. For a detailled list and description of the connectors of the serial interface/communication piggybacks and of the frontpanel interface connectors please refer to the “SI Piggybacks” appendix of this manual as well as to the CXM-SIO3 user’s manual and its “Serial Communications Piggybacks” appendix respectively.

2.4.1 Serial I/O Interfaces

The mainboard RJ12 RS232 frontpanel connectors BU7 and BU8 of the VSBC-32(E) are provided with TxD and RxD signals by the controller’s SMC1 and SMC2 channels and supply RS232 interface software handshake (XON/XOFF) capability. They are configured as service/debug connectors by default.

The pinouts of the RJ12 connectors are shown in the following table.

Figure 2-5: Orientation of the VSBC-32(E) Mainboard Serial Interfaces

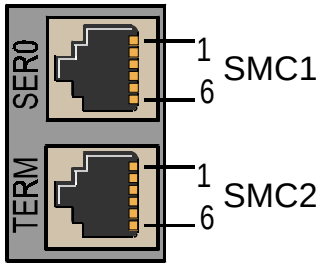


Table 2-3: Pinouts of the Mainboard Serial Interface Connectors BU7/BU8

Pin	Pinouts
1	N/C
2	GND
3	TxD
4	RxD
5	N/C
6	N/C

N/C = Not connected.

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2.4.2 Piggyback Interface Connectors for Serial Interface Piggybacks

The VSBC-32(E) is equipped with a set of piggyback interface connectors for serial interface (SI) piggybacks (three 7-pin row male connectors). The pinout of these piggyback interface connectors includes all signals for serial I/O (RS232), PROFIBUS (RS485) and Ethernet (10BaseT, 10Base5, 10Base2) communication.



Note...

Although physically all piggybacks fit on bott basic board variants (IUC-32 and IUC-32E), the MN68360 processor of the IUC-32 variant does not support Ethernet communication. Therefore, Ethernet piggybacks should be used only on the IUC-32E board variants.

For a detailled description of the pinouts of these piggyback interface connectors please refer to the VITA/*PEP Modular Computers* CXC MPI Specification.

2.4.3 Memory Piggyback Interface Connectors

The VSBC-32(E) is equipped with a set of memory piggyback interface connectors (two 50-pin row female connectors). The pinout of these piggyback interface connectors includes all signals for the connection of up to 128MB of DRAM and up to 4 MB of flash EPROM.

For a detailled description of the pinouts of these piggyback interface connectors please refer to the VITA/*PEP Modular Computers* CXC MPI Specification.

2.4.4 EPROM DIP Sockets

The VSBC-32(E) is equipped with two sets of (flash) EPROM DIP sockets (two 32-pin row female sockets). The pinout of these DIP sockets includes all signals for the connection of up to 1MB of SRAM.

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2.4.5 Background Debug Mode Interface Connector

The VSBC-32(E) is equipped with a background debug mode (BDM) interface connector (one 12-pin row male connector). This connector allows an external debugger to be interfaced to the MC68(EN)360 for controlling purposes. The interface connector is specified by Motorola.

The pinouts of the BDM interface connector are shown in the following table. For any further details, please refer to the Motorola MC68(EN)360 User's Manual.

Table 2-4: BDM Interface Connector Pinouts

Pin	Signal	Pin	Signal
1	GND	2	CLKO1
3	DS*	4	BERR*
5	GND	6	BKPT* / DSCLK
7	GND	8	FREEZE
9	RESETH*	10	IFETCH / DSI
11	VCC	12	IPIPE0 / DSO

2.4.6 VMEbus Backplane Interface

The VSBC-32(E) is equipped with a VMEbus backplane interface connector.

The board is provided with a complete master interface for the VMEbus backplane connector. The VMEbus master interface consists of a VMEbus arbiter, requester, system controller and buffers for data/address/control signals. Simultaneously, the VSBC-32(E) can act as a VMEbus slave, as it is provided with a slave interface which consists of a programmable board address decoder, a dual-ported SRAM access and a mailbox interrupt controller.

To act as a system controller, the VSBC-32(E) is provided with arbiter, system clock driver, power monitor with system reset driver, IACK daisy chain driver and 7-level VMEbus interrupt controller.

Arbitration is single-level FAIR (compare VME64 Specification Rule 3.14/Observation 3.17) on BR3*. If the VSBC-32(E) is used as a system controller, a special detection function provided by the board, which is also readable within the VMEbus control/status register, makes any "slot 1" jumper setting superfluous. The VMEbus interrupt acknowledgement is controlled via a daisy chain driver that is supplied with the board. IACK* is connected via the VMEbus backplane for IACKIN* of the system slot.

The signals SYSCLK* and SYSRES* can be routed from on-board to the VMEbus through the use of jumpers, leaving to the VMEbus user instead of the system controller the initiative of generating these signals. SYSFAIL* generates a maskable on-board autovectored level-3 interrupt (please refer also to the section System Control Functionality (Interrupt Control) of this chapter), whereas ACFAIL* generates a non-maskable on-board level-7 interrupt.

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The VSBC-32(E) also provides a bus monitor for the VMEbus. A 128µs bus error timer monitors the cycle lengths of the VMEbus data transfer and generates a VMEbus BERR* signal on timeout. This timer is enabled and disabled via the VMEbus control/status register which contains alsao a timeout status bit in order to identify the bus errors generated by the bus monitor.

Exchange and retention of system relevant data from the VMEbus to the CPU/DMA and viceversa is provided by means of 256kB or 1MB of a 16-bit wide dual-ported SRAM which is backed-up using Gold Caps. Both the VMEbus users and the on-board CPU have access to the SRAM memory (upper 8kB, i.e. even Byte addresses).



Note...

The dual-ported SRAM cannot be accessed through its own VMEbus interface. A bus monitor timeout would result due to the fact that any access by the VMEbus to the DPRAM would be blocked as long as the VSBC-32(E) is bus master.

An external VMEbus master may interrupt the VSBC-32(E) by setting P_IRQ5 (“mailbox interrupt pending”) in the VMEbus control/status register. Seen from the VMEbus, the address of this dual-ported register is identical to the base address of the dual-ported SRAM (lower 8kB, i.e. odd Byte addresses).



Note...

All bits of the VMEbus control/status register can be read from the VMEbus, but only the bit P_IRQ5 is read/write.

For a complete map of the VMEbus control/status register please refer to the relating section in the Configuration chapter of this manual.

For any general VMEbus information including generic pinouts please refer to Appendix B of the ANSI/VITA VME64 Specification.

2.4.7 CXC Mezzanine Interface

The VSBC-32(E) is equipped with a CXC mezzanine interface connector.

CXC and eCXC both contain a 16-bit data bus, seven address lines and eight decoded chip select lines. In total, there are eight control signals (CXC_CS0...CXC_CS7). The base address of the CXC can be programmed via the CS5 line of the MC68(EN)360. The main difference between the two VITA standards is the amount of address space available for peripheral devices:

- CXC: 8*256Bytes (overall length: 0x400H, 1024Bytes actually available)
- eCXC: 8*16MB (overall length: 0x1000 000, 16MB actually available)

Furthermore, the (e)CXC contains a 4-IRQ capability (4 edge-sensitive interrupt requests), DMA capability (1 channel, DREQ + DACK), serial ports (3 channels, Full MODEM) and a set of parallel port signals. These special CXC functions are based on the MC68(EN)360 controller resources.

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For general CXC information, including generic pinouts and a comparison of the MC68(EN)360 and the MC68302 CPU pinouts on the CXC, please refer to the “CXC” appendix attached to this manual, the *PEP Modular Computers* CXC Reference Manual or to the CXC Specification.

2.5 VSBC-to-VSBC-32 System Upgrading

In the following the porting information required by customers wanting to upgrade their VSBC-based systems to an VSBC-32 based one is supplied.

The VMEbus/CXC ports SER1, SER2 and SER3 of the MC68302 are equivalent to ports SCC2, SCC3 and SCC4 respectively on the MC68(EN)360 controller chip.

With regard to special VMEbus/CXC capabilities, the VMEbus/CXC pinout on the VSBC-32(E) has been developed to provide maximum compatibility between the standard VMEbus/CXC functions. In addition, all signals are available in order to configure two time division multiplexed channels via the VMEbus/CXC (ISDN, PCM, GCI and so on).

Multifunction pins with incompatible functions with regard to the MC68302 and MC68(EN)360, which are called “user-defined” in the generic CXC Specification, are not part of the VSBC-32(E) VMEbus or CXC specification.

Although the SMCs are configured on the mainboard, these ports are also integrated on the VMEbus/CXC because of possible ISDN applications where SMCs can be integrated and other protocols supported by the MC68(EN)360.



Note...

If the RCLK2 signal (VMEbus/CXM pin C16) is required, jumper J4 (24MHz clock) must be opened and the serial drivers delivered by *PEP Modular Computers* must be modified.

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Table 2-5: IUC/IUC-32 Porting Information (Sheet 1 of 2)

CXC Function	Pin	MC68302 HW Comp.	MC68(EN) 360 Port	Comment	See Note
IRQ_1	A1	Yes	PC0	—	
IRQ_2	A2	Yes	PC1	—	
IRQ_3	A3	Yes	PC2	—	
IRQ_4	A4	Yes	PC3	—	
DMA_ACK	C2	Yes	PB5	—	
DMA_REQ	C3	Yes	PB4	—	
SER1_RCLK	B1	Yes	PA8	—	
SER1_TCLK	B2	Yes	PA10	—	
SER1_TXD	B4	Yes	PA3	—	
SER1_RXD	B10	Yes	PA2	—	
SER1_RTS	B5	Yes	PB13	—	
SER1_DTR	A13	Yes	PB17	—	
SER1_CTS	B13	Yes	PC6	—	
SER1_CD	B14	Yes	PC7	—	
SER2_RCLK	C16	Yes	PA13	Cannot be used if J4 is set	3
SER2_TCLK	C15	Yes	PA12	—	
SER2_TXD	C17	Yes	PA5	—	
SER2_RXD	C18	Yes	PA4	—	
SER2_RTS	C12	Yes	PB14	—	
SER2_DTR	A11	Yes	PB16	—	
SER2_CTS	C13	Yes	PC8	—	
SER2_CD	C11	Yes	PC9	—	
SER3_RCLK	C6	Yes	PA15	Not usable if SI piggyback uses SCC4	4
SER3_TCLK	C5	Yes	PA14	—	
SER3_TXD	C8	Yes	PA7	Not usable if SI piggyback uses SCC4	4

Legend:

1 ***Reserved Pin:*** *On a standard VSBC-32 board, this signals is used for UART ports at BU7 and BU8.*

2 ***Reserved Pin:*** *On a standard VSBC-32 board, this signal is used for SPI to which the EEPROM is already connected. PB0 is chip select of the EEPROM.*

3 ***Reserved Pin:*** *On PA13, a 24 MHz clock signal is routed via jumper J4. This signal is always needed for PEP standard software (serial drivers).*

4 ***Dual Functioning Pin:*** *This signal is routed both to the mainboard's interface for serial interface piggybacks (ST5C) and the CXC backplane connector and can be used by either one or the other, but not both at the same time. Due to this, a conflict exists if the SCC4 port is to be used with the SI232 piggyback and CXC boards (such as CXM-SIO3), as both boards access this port. The SCC4 port can, therefore, not be used at the same time by serial interface piggybacks and CXC boards.*

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Table 2-5: IUC/IUC-32 Porting Information (Sheet 2 of 2)

CXC Function	Pin	MC68302 HW Comp.	MC68(EN)360 Port	Comment	See Note
SER3_RXD	C9	Yes	PA6	Not usable if SI piggyback uses SCC4	4
SER3_RTS	B7	Yes	PB15	Not usable if SI piggyback uses SCC4	4
SER3_DTR	A12	Yes	PB9	Not usable if SI piggyback uses SCC4	4
SER3_CTS	B16	Yes	PC10	Not usable if SI piggyback uses SCC4	4
SER3_CD	B8	Yes	PC11	Not usable if SI piggyback uses SCC4	4
User-Defined	A5	No	PB0	Used on board SPI SEL for EEPROM. Cannot be used on CXC	2
	A6	No	PB1	SPI Clk: can be used if an 'SPI SEL' other than PB0 is used.	
	A8	No	PB2	SPI TxD: can be used if an 'SPI SEL' other than PB0 is used.	
	A9	No	PB3	SPI RxD: can be used if an 'SPI SEL' other than PB0 is used.	
	A10	No	PB8	*See MC68360 User Manual*	
	B11	No	PB10	Used on board SMC2 (Transmit)	1
	C1	No	PB6	Used on board SMC1 (Transmit)	1
	C4	No	PB11	Used on board SMC2 (Receive)	1
	C10	No	PB7	Used on board SMC1 (Receive)	1

Legend:

1 ***Reserved Pin:*** *On a standard VSBC-32 board, this signals is used for UART ports at BU7 and BU8.*

2 ***Reserved Pin:*** *On a standard VSBC-32 board, this signal is used for SPI to which the EEPROM is already connected. PB0 is chip select of the EEPROM.*

3 ***Reserved Pin:*** *On PA13, a 24 MHz clock signal is routed via jumper J4. This signal is always needed for PEP standard software (serial drivers).*

4 ***Dual Functioning Pin:*** *This signal is routed both to the mainboard's interface for serial interface piggybacks (ST5C) and the CXC backplane connector and can be used by either one or the other, but not both at the same time. Due to this, a conflict exists if the SCC4 port is to be used with the SI232 piggyback and CXC boards (such as CXM-SIO3), as both boards access this port. The SCC4 port can, therefore, not be used at the same time by serial interface piggybacks and CXC boards.*

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2.6 Special Board Functions

2.6.1 Real-Time Clock

The three-wire serial interface real-time clock V3021 is a 1-bit device which is accessible over the CS6 of the MC68(EN)360. Its time-keeping features include as follows:

- seconds, minutes, hours, day of month, month, year, week day and week number in BCD format;
- leap year and week number correction;
- stand-by supply smaller than 1µA.

For further information please refer also to the “Software Configuration” chapter in this manual and the EM Microelectronic V3021 data sheet.

2.6.2 EEPROM

The serial EEPROM is a 1-bit device which is accessible over the three-wire Interchip SPI Interface of the MC68(EN)360. The first half of the EEPROM (1 kbit) is reserved for factory data, including Board ID codes, Internet/Ethernet addresses, boot information etc. The second half of the EEPROM is available for the user. See also the Software Configuration chapter in this manual.

For further information on the EEPROM, please refer also to the XICOR X25C02 data sheet.

2.6.3 PLL Operation Mode

The MC68(EN)360 inputs EXTAL and CPU clock use the same input frequency. The XTAL input is left open. The clock mode is selected via the hard-wired inputs MODCLK0 and MODCLK1. With the default settings of MODCLK0 = 1 and MODCLK1 = 0, the following configuration is selected:

- no prescaler;
- multiplication factor = 1;
- CLKIN to the prescaler = CPU clock;
- internal frequency (VCO/2) = CPU clock;

2.6.4 Tick Generator

The MC68(EN)360 internal Periodic Interrupt Timer is used by the *PEP* real-time operating system as Tick generator.

For further information please refer also to the Motorola MC68(EN)360 User’s Manual.

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2.6.5 Bus Error Timers

The VSBC-32(E) provides an on-board bus error timer and a VMEbus error timer. There are three cases of bus error:

Table 2-6: Bus Error Types

Cause	Timeout	Enable / Disable
Reserved address *BERR0*	100ns	Permanently enabled
On-board *BERR1*	8µs	Enable / disable possible, set in board control register
VMEbus *BERR2*	128µs	Enable / disable possible, set in VMEbus control register

On-Board Bus Error Timer

An 8µs timeout on-board timer monitors the cycle lengths of data transfers to and from locations beyond the CPU data bus buffer, including on-board I/O, VMEbus, SRAM and CXC. After a timeout occurs, it generates an on-board bus error signal for error termination. This timer is enabled/disabled via the board control/status register, which also supplies a timeout status bit in order to identify bus errors generated by the on-board bus error timer.

During VMEbus cycles the on-board bus error timer is reset as soon as the VSBC-32(E) gains VMEbus ownership, i.e. the time gap between a VMEbus request and the starting of the VMEbus cycle is monitored by the on-board bus error timer. The VMEbus cycles themselves are monitored by the separate VMEbus error timer.



Note...

The internal MC68(EN)360 bus error timer (hardware watchdog timer) is not used on the VSBC-32(E). Therefore, it should remain disabled (default setting).

VMEbus Error Timer

In addition to the on-board bus error timer, the VSBC-32(E) provides a bus monitor for the VMEbus. A 128µs timer monitors VMEbus data transfer cycle lengths and generates a VMEbus bus error signal BERR* for error termination. This error is enabled and disabled via the VMEbus control/status register which also supplies a timeout status bit in order to identify bus errors genrated by the bus monitor.

For a complete map of the VMEbus control/status register please refer to the relating section in the Configuration chapter of this manual.

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2.6.6 Watchdog Timer

A 512ms watchdog timer triggers the on-board reset generator at timeout. Once enabled via the board control/status register, the watchdog timer cannot be reset by software. It must be re-triggered via the corresponding bit in the board control/status register periodically within the timeout period. ‘Watchdog timer running’ is a status that is displayed by the yellow front panel LED.

For the location of the Watchdog LED please refer to the VSBC-32(E) Frontpanel figure in the “Introduction” chapter of this manual.

2.6.7 Reset Sources

The VSBC-32(E) interacts with the following reset sources:

Table 2-7: VSBC-32(E) Reset Sources

Reset Source	Identification
Push Button	No
SYSRES* VME	No
Watchdog	WDG bit on-board (*Board Control/Status Register*)
Power Monitor (4.65V)	Inside the MC68(EN)360

2.6.8 “Slot 1” Detection

During power-up the VSBC-32(E) detects whether it is being used as a system controller (slot 1). This information can be read from the VMEbus control/status register and is valid until the next power-down of the system.

For a complete map of the VMEbus control/status register please refer to the relating section in the Configuration chapter of this manual.

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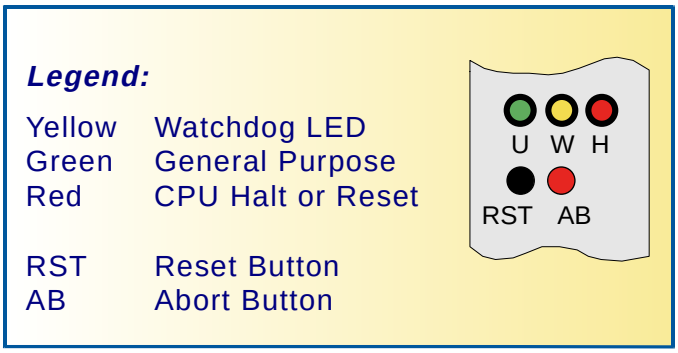
2.7 Frontpanel Functions

The frontpanel status indicators consist of three LED's with the following functions:

- Yellow Watchdog LED
- Green General Purpose
- Red CPU Halt or Reset

The green LED is user-defined by the customer. It is set by the software during startup when the MC68(EN)360 is initialized.

Figure 2-6: VSBC-32(E) Frontpanel LED and Button Locations



A Reset button is fitted to the front panel to avoid false operation. The Reset button triggers the on-board system reset generator. In addition, an Abort button is also fitted to the front panel. The Abort button generates a non-maskable level-7 interrupt which is used for debugging purposes.

2.8 RTC and SRAM Data Retention

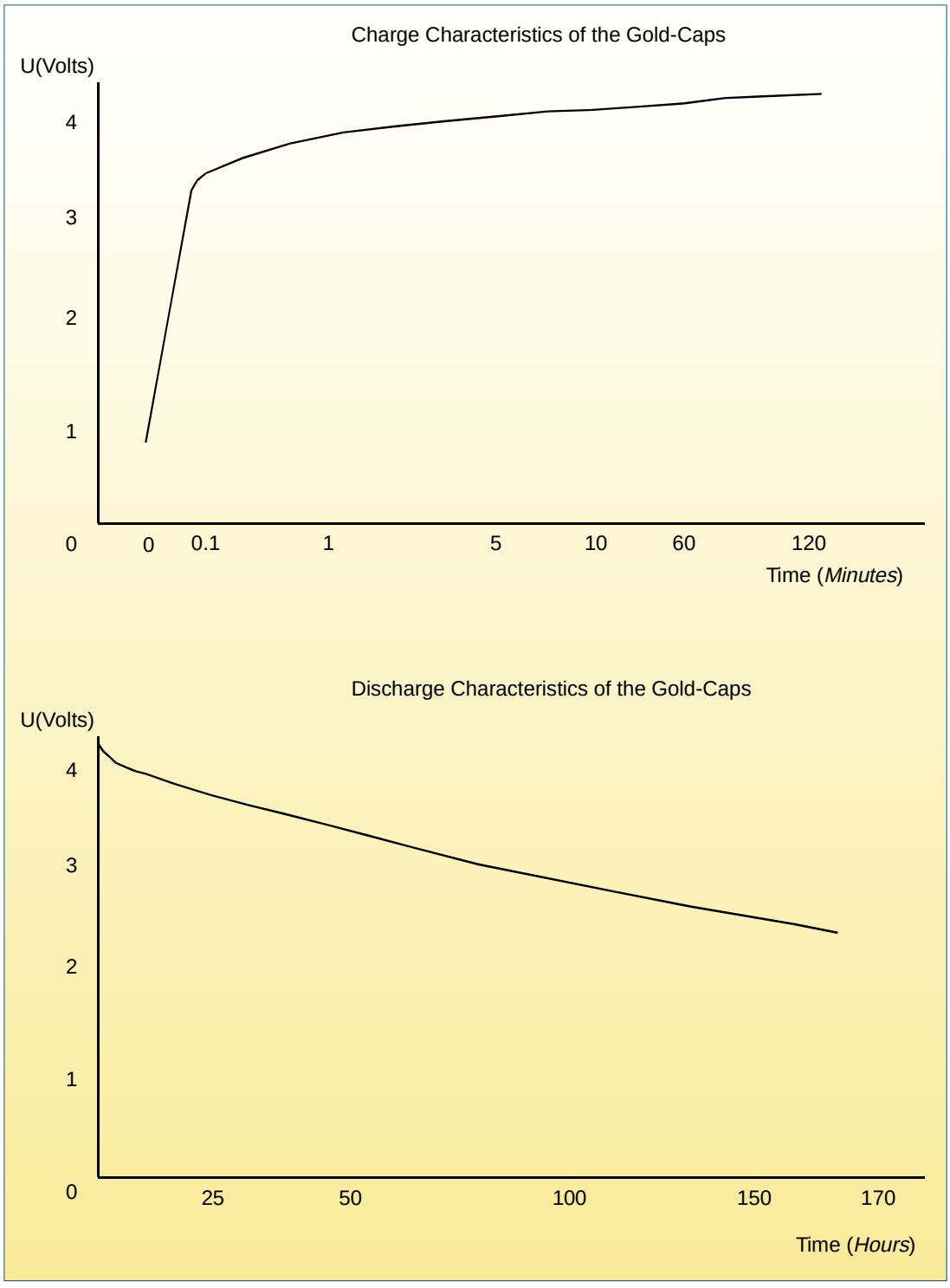
Short-term data retention for RTC and SRAM is gained with two Gold Caps, each with a value of 0.22 Farad. In contrast to Lithium cells, Gold Caps do not require servicing. This short-term backup is intended for short power failures or for reconfiguring systems. An empty Gold Cap needs approximately three hours to charge up, with backup times dependant on the temperature, memory size and memory manufacturer tolerances. A well charged Gold Cap provides a minimum of 10 hours backup time.

Laboratory tests at *PEP* indicate a typical backup time of 1 week for both 256kB and 1MByte SRAM plus RTC (the typical on-board backup current is below 2µA). The charge and discharge behaviour of Gold Caps is documented in the graphics overleaf.

For long-term data retention, 5V standby power supply could be provided via CXC ST3A, pin 5 (user-defined line). This would require special wiring on the CXC backplane or a special battery CXC module.

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Figure 2-7: Gold-Cap Charge and Dischage Characteristics



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2.9 Address Decoder

2.9.1 Basic Structure

The address decoder of the VSBC-32(E) consists of external logic and the MC68(EN)360 internal memory controller. The MC68(EN)360's internal chip select logic decodes all the basic address areas following its initialization. The eight chip select outputs of the processor are connected to the different devices as shown in the following tablle.

Table 2-8: Chip Select Output Connection

Chip Select	Connection	Port Size	Acknowledge
CS0	Flash on memory piggyback or EPROM on flash/EPROM sockets[1]	32/16	Internal
CS1	DRAM on memory piggyback	32	Internal
CS2	VMEbus	16	External
CS3	Flash/EPROM sockets or memory piggyback[1]	16/32	Internal
CS4	SRAM	16	External
CS5	CXC	16	External
CS6	RTC	16	External
CS7	Control/status register	16	External

1 *Chip selects for flash on memory piggybacks and EPROM sockets are exchanged depending on the selected boot device (Jumper J18).*

The external address decoder switches the boot chip select CS0, memory piggyback or EPROM on flash/EPROM sockets depending on the selected boot device. The interrupt acknowledge cycles are also decoded by the external address decoder. Moreover, the external address decoder includes a fast bus error (BERR) generator which monitors the delay between external cycle start and generated CSx line.

2.9.2 Boot Decoding

The type of boot device can be selected from the DRAM/flash memory piggyback or the EPROM devices on the two flash/EPROM sockets. The flash/EPROM sockets can be configured by the user with the EPROM or different flash devices. Please note that regardless of the boot device selected both possible areas can be addressed due to the fact that each area is connected to a seperate CS line of the controller. This means that the CS0 line, which is the global boot select of the controller, is exchanged for the CS3 line by the boot decoder logic.

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Chapter 3

Installation

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3. Installation

3.1 Hardware Installation

The board described in this manual can be installed in the system slot of any VMEbus compatible computer. The frontpanel of the board should be safely secured by screws to the chassis to avoid lossening of the board through vibration and to ensure correct earth connection.



Caution, Electric Shocks!

Switch off the VMEbus system before installing the board in a free VMEbus slot. Failure to do so could endanger your life/health and may damage your board or system.



ESD Equipment!

Your VMEbus board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

To install the board, please proceed as follows:

- Ensure that the safety requirements indicated above are observed
- Ensure that the serial interface piggyback is properly installed and the relating frontpanel secured to the mainboard (see appropriate documentation for configuration)
- Ensure that the flash/DRAM memory piggyback and the DIP flash/EPROM is properly installed, and that the boot memory selection jumper is set correctly
- Ensure that all other wire jumpers are set correctly (DIP socket memory type and size, boot device, system clock and on-board resets ???)



Warning!

Failure to set the wire jumpers correctly may cause damage or malfunctionning to your board. Please refer to the Hardware Configuration section in this manual for any details on jumper settings.

- Install the board in an appropriate slot and engage the retaining mechanism
- Connect external interfacing cables to the board as required
- Ensure that the board and interfacing cables are properly secured.

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To remove the board, please proceed as follows:

- Ensure that the safety requirements indicated above are observed
- Disconnect any interfacing cables that may be connected to the board
- Disengage the board retaining mechanism by pressing down on the board release handle disengaging the board from the backplane connector and pull the board out of the slot.

3.1.1 External Serial Interface Module

Being a combined system and serial communications controller board, the VSBC-32(E) is designed for a possible combined use together with the CXM-SIO3 external serial interface module. If such an interface module is used, all communication signals between the mainboard and the module are transmitted via the CXC bus. For this purpose, the external interface module must be “sandwiched” with the VSBC-32(E) mainboard.

3.2 Software Installation

There are no special requirements for software installation. However, many components of the VSBC-32(E) are controlled by the MC68(EN)360 processor. Due to this fact, the controller requires a special initialization sequence before any other software can be started.

For any details on the initialization sequence and the address list of involved registers please refer to the relevant description in the User’s Manual included with your operating system.

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Chapter 4

Configuration

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4. Configuration

4.1 Hardware Configuration

The VSBC-32(E) has fifteen jumpers fitted to the board. The list of default jumper settings is shown below. A board layout with all jumper locations and pinouts is supplied in the Board Layouts section of the Introduction chapter of this manual.

4.1.1 Wire Jumpers

The following parameters are selected via wire jumpers:

- Boot device selection (J9)
- CXC/Enhanced CXC selection (J10)
- Connection of SYSCLK to VMEbus (J11)
- Connection of on-board reset to VMEbus (J12)
- DIP socket memory type and size (J13/J14)



Note...

Jumpers J9 to J14 are normal wire jumpers that can be configured by the user. The other jumpers are solder jumpers and are factory set.

Table 4-1: ACFAIL, (e)CXC and Boot Device Selection, General Purpose Jumper

Jumper	Settings	Description
J9	*Open*	*Boot from flash on DRAM/Flash piggyback enabled*
	Closed	Boot from flash/EPROM DIP sockets enabled
J10	*Open*	*CXC enabled*
	Closed	Enhanced CXC enabled
J11	Open	SYSCLK disconnected from VMEbus
	Closed	*SYSCLK connected to VMEbus*
J12	Open	On-board RESET generator not to VMEbus
	Closed	*On-board RESET generator to VMEbus*

Table 4-2: DIP Socket Memory Selection

J13	J14	Description
Open	*Open*	*EPROM 256kB/512kB (2x 27C010 or 2x 27C020)*
Open	1-2	EPROM 1MB (2x 27C040)
1-2	1-2	EPROM 2MB (2x 27C080)
Open	1-3	Flash 12V (read only) 256kB/512kB (2x 28F010 or 2x 28F020)
1-3	1-3	Flash 5V (read/write) 256kB/1MB (2x 29F010 or 2x 29F040)

Default settings are in italics.

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4.1.2 Solder Jumpers

The following parameters are selected via solder jumpers:

- CPU/bus clock frequency (J1/J2/J3)
- Communications clock frequency (J4)
- Serial EEPROM write protection (J5)
- Connection of protective and signal Ground (J6)
- CXC interface connector pin A5 function assignment (J11)
- SRAM size (J7/J8)



Warning!

All solder jumpers are factory set. Alteration of their settings can result in damage to the board. Therefore, customers must not alter the settings of these jumpers.

Table 4-3: CPU/Bus Clock Frequency Selection

J3	J2	J1	Description	
Closed	Closed	Open	25MHz	(VSBC-32 and VSBC-32E)
Open	Closed	Open	33.3MHz	(VSBC-32E only)

Table 4-4: Clock Frequencies, EEPROM Write Protection and GND Connection

Jumper	Settings	Description
J4	Open	24MHz communications clock not connected to MC68(EN)360
	Closed	*24MHz communications clock connected to MC68(EN)360* ***Note:*** *This jumper must be set to open if the RCLK2 signal (CXM pin C16) is required.*
J5	*Open*	*EEPROM write protection disabled*
	Closed	EEPROM write protection enabled
J6	*Open*	*Signal GND not connected to Protective GND*
	Closed	Signal GND connected to Protective GND **Note:** If this jumper is set, care must be taken to avoid any grounding currents.

Table 4-5: SRAM Size Selection

J7	J8	Description	
1-2	1-2	1MB	(VSBC-32E only)
1-3	1-3	256kB	(VSBC-32 and VSBC-32E)

Default settings are in italics.

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4.2 Software Configuration

4.2.1 Address Map

Software applications may require to configure data in the VSBC-32(E) registers. For this purpose, the configurable memory is described in the following. The address map in the table below is based on the recommended default initialization of the MC68(EN)360 chip select logic.

Figure 4-1: VSBC-32(E) Memory Map

Address	Memory Device	MC68(EN)360
0x 00 xx xx xx	DRAM on DRAM/Flash piggyback	CS1
0x 04 xx xx xx	FLASH on DRAM/Flash piggyback	CS0
0x 07 00 0x xx	MC68(EN)360 internal RAM register	—
0x 09 xx xx xx	Flash/EPROM sockets[1]	CS3
0x 0A xx xx xx	SRAM	CS4
0x 0B F7 xx xx	CXC[2]	CS5
0x 0C xx xx xx	Real-time clock	CS6
0x 0D xx xx x1	VMEbus IRQ mask register	CS7+1
0x 0D xx xx x5	VMEbus control / status register	CS7+5
0x 0D xx xx x7	Board control / status register	CS7+7
0x 82 xx xx xx	VMEbus user-defined AM code	CS2
0x 83 xx xx xx	VMEbus user-defined AM code	CS2
0x 85 00 xx xx	VMEbus short I/O AM code	CS2
0x 87 xx xx xx	VMEbus standard AM code	CS2

1 *If the ROM sockets are selected as the default boot device, then the address 0x 09 xx xx xx, i.e. CS3 of the MC68[EN[360, is automatically selected as the base address for the flash on the memory piggyback.*

2 *See the "CXC" appendix of this manual for further addressing information.*



Note...

The above shown memory map is *PEP* default. All other addresses do not cause CS0..CS7 signals. Therefore access to them leads to bus errors (BERR).

Furthermore, in order to determine the base of the internal memory map of the MC68[EN]360 controller, the module base address register (MBAR) must be set. The location of this register is fixed in the address area Supervisor CPU Space at 3FF00H. For more information on the recommended MC68(EN)360 initialization sequence, please refer to the Software Installation section in this manual.

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4.2.2 Board Control/Status Register

Address: CS7 + 0x7

Format: Byte

Access: Read/write

Value after HW Reset: 0

***PEP* Default Address:** 0x 0D 00 00 07

Figure 4-2: CS7 + 0x7 Bitmap

7	6	5	4	3	2	1	0
WDG	*BERR2*	*BERR1*	*EN_WDG*	*TR_WDG*	*EN_BERR1*	*ACFAIL*	*LED_G*

Table 4-6: Register Description

Name	Register Value	Access	Description
WDG *bit 7*		Read/Write	Set by watchdog timer when timout has been reached. Used to differentiate between resets caused by the watchdog and resets caused by the reset button (power up resets can be identified within the MC68(EN)360).
BERR2 *bit 6*		Read/Write	Set by VMEbus error timer on timeout to identify bus errors caused by this timer. (See also VMEbus status/control register)
BERR1 *bit 5*		Read/Write	Set by on-board bus error timer on timeout to identify bus errors caused by this timer.
EN_WDG *bit 4*	1	Read/Write	Enables the watchdog timer. It can only be set once, and remains enabled until the next reset.
TR_WDG *bit 3*	1	Read/Write	Triggers the watchdog timer. Watchdog timeout = 512ms.
EN_BERR1 *bit 2*	1	Read/Write	Enables the on-board bus error timer. It also monitors all on-board I/O cycles, including the time from the VMEbus request to the VMEbus grant. Timeout = 8µs.
ACFAIL *bit 1*	1	Read/Write	VME ACFAIL signal latched when active in order to distinguish a level 7 NMI from an ABORT or ACFAIL.
LED_G *bit 0*	1	Read/Write	Enables the green ‘general purpose’ front panel LED.



Warning!

The correct functionality of your equipment may be jeopardized due to a loss of information, if bit 7 is written to. Therefore, the customer should not write any data to bit 7.

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4.2.3 VMEbus Control/Status Register

Address: CS7 + 0x5

Format: Byte

Access: Read/write

Value after HW Reset: See table

***PEP* Default Address:** 0x 0D 00 00 05

Figure 4-3: CS7 + 0x5 Bitmap

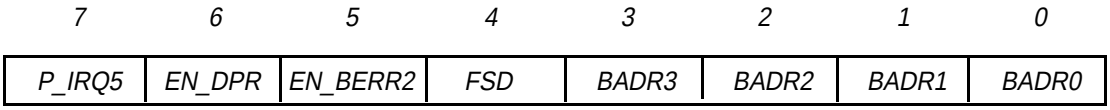


Table 4-7: Register Description

Name	Register Value	HW Reset Value		SW Reset Value (PEP)		Description
		Slot 1	Other	Slot 1	Other	
P_IRQ5 *bit 7*	1	0	0	0	0	Mailbox interrupt pending.
EN_DPR *bit 6*	1	0	0	Value stored in EEPROM		Dual-port SRAM (incl. mailbox interrupts) enabled for VMEbus requester. Base address established through bits BADR0..3.
EN_BERR2 *bit 5*	1	0	0	1	0	Enables the VMEbus error timer (all VMEbus cycles). Timeout = 128µs.
FSD *bit 4*	1	1	0	1	0	VMEbus “slot 1” detection flag of system controller..
BADR3..0 *bits 3..0*		0	0	Value stored in EEPROM		VMEbus address location of dual-ported SRAM. Equivalent to VMEbus address lines A23..A20, programmable from 0x 00..0x 0F in 1MB windows. Enabled by EN_DPR:. (See also following table.)

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Table 4-8: Board Base Addresses

BADR3..0	Board Base Address	BADR3..0	Board Base Address
0000	0x 00 00 00	1000	0x 80 00 00
0001	0x 10 00 00	1001	0x 90 00 00
0010	0x 20 00 00	1010	0x A0 00 00
0011	0x 30 00 00	1011	0x B0 00 00
0100	0x 40 00 00	1100	0x C0 00 00
0101	0x 50 00 00	1101	0x D0 00 00
0110	0x 60 00 00	1110	0x E0 00 00
0111	0x 70 00 00	1111	0x F0 00 00

4.2.4 VMEbus Interrupt Mask Register

Address: CS7 + 0x1

Format: Byte

Access: Read/write

Value after HW Reset: 0

Value after Inititalization of *PEP* Software: Value stored in EEPROM

***PEP* Default Address:** 0x 0D 00 00 01

Figure 4-4: CS7 + 0x1 Bitmap

7	6	5	4	3	2	1	0
EN_IRQ7	*EN_IRQ6*	*EN_IRQ5*	*EN_IRQ4*	*EN_IRQ3*	*EN_IRQ2*	*EN_IRQ1*	*SYSFAIL*

Table 4-9: Register Description

Name	Register Value	Description
EN_IRQx	1	Enable VMEbus interrupt requests where x = 1..7.
SYSFAIL	1	Enable VMEbus level-3 autovector interrupt SYSFAIL

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Appendix A

Memory Piggybacks

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A. Memory Piggybacks

A.1 General

The Memory Piggybacks described herein provide main memory capability for the storage of progam code and data either in DRAM or flash memory. Various configurations of DRAM and flash memory as indicated in the table below are available for a wide variety of PEP CPU boards. All configurations have 32-bit access and a maximum address range of 64 MB. In addition jumpers are available for providing write protection.

Table A-1: Memory Piggyback Types and Configurations

Type	Memory Configuration	
	DRAM	FLASH
DM600	4 MB	1 MB
		2 MB
		4 MB
DM601	16 MB	1 MB
		2 MB
		4 MB
DM602	1 MB	0 MB
		1 MB
		2 MB
DM603	32 MB	0 KB
		512 KB
		1 MB
		2 MB
		4 MB
DM604	8 MB	1 MB
		2 MB
		4 MB
DM605	64 MB	1 MB
		2 MB
		4 MB

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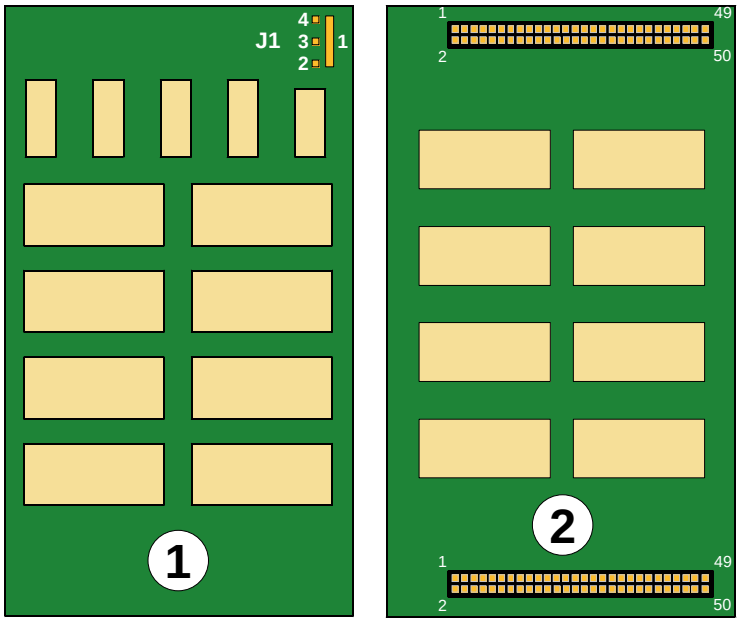
A.2 DM600

The DM600 is a memory piggyback fitted with:

- DRAM: 4 MB
- Flash Memory: 1, 2, or 4 MB

A.2.1Board Layout and Jumper Location

Figure A-1: DM600 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.2.2 Jumper Description and Flash Addresses

Table A-2: Jumper: J1 Settings and Flash Memory Address Ranges

Setting	Description	1MB Flash	2MB Flash	4MB Flash
Open	All flash EPROM's write protected			
1 - 2	*No Protection*			
1 - 3	Flash Bank 1: Write protected Flash Bank 1: Address Range	Upper 512 KB 0x04080000 - 0x04100000		Upper 2 MB 0x04020000 - 0x04400000
1 - 4	Flash Bank 0: Write protected Flash Bank 0: Address Range	Lower 512 KB 0x04000000 - 0x04080000	 0x04000000 - 0x04200000	Lower 2 MB 0x04000000 - 0x04200000

Default settings are in italics.

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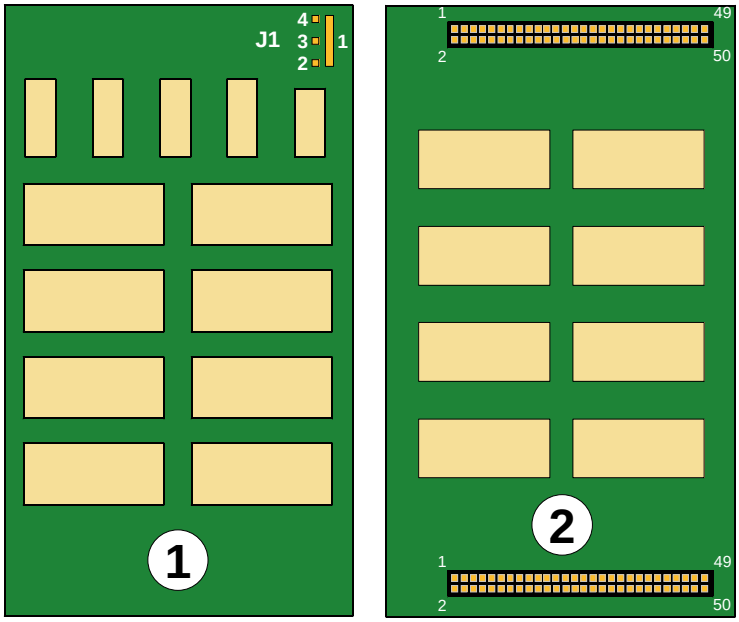
A.3 DM601

The DM601 is a memory piggyback fitted with:

- DRAM: 16 MB
- Flash Memory: 1, 2, or 4 MB

A.3.1Board Layout and Jumper Location

Figure A-2: DM601 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.3.2 Jumper Description and Flash Addresses

Table A-3: Jumper: J1 Settings and Flash Memory Address Ranges

Setting	Description	1MB Flash	2MB Flash	4MB Flash
Open	All flash EPROM's write protected			
1 - 2	*No Protection*			
1 - 3	Flash Bank 1: Write protected Flash Bank 1: Address Range	Upper 512 KB 0x04080000 - 0x04100000		Upper 2 MB 0x04020000 - 0x04400000
1 - 4	Flash Bank 0: Write protected Flash Bank 0: Address Range	Lower 512 KB 0x04000000 - 0x04080000	 0x04000000 - 0x04200000	Lower 2 MB 0x04000000 - 0x04200000

Default settings are in italics.

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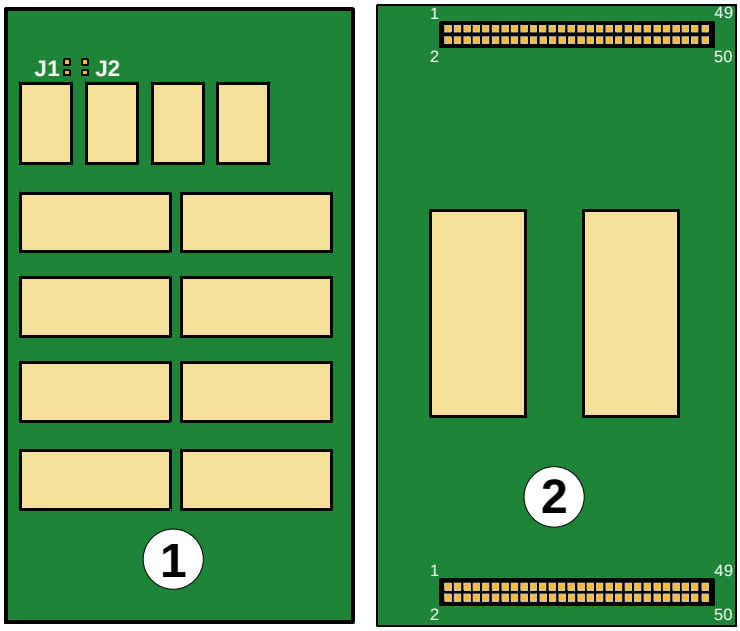
A.4 DM602

The DM602 is a memory piggyback fitted with:

- DRAM: 1 MB
- Flash Memory: 0, 1, or 2 MB

A.4.1Board Layout and Jumper Location

Figure A-3: DM602 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.4.2 Jumper Description and Flash Addresses

Table A-4: Jumpers: J1 and J2 Settings and Flash Memory Address Ranges

Setting		Description	1MB Flash	2MB Flash
J1	*Set*	*No Protection*		
	Open	Flash Bank 1: Write protected Flash Bank 1: Address Range	Upper 512 KB 0x04080000 - 0x04100000	
J2	*Set*	*No Protection (default)*		
	Open	Flash Bank 0: Write protected Flash Bank 0: Address Range	Lower 512 KB 0x04000000 - 0x04080000	0x04000000 - 0x04200000

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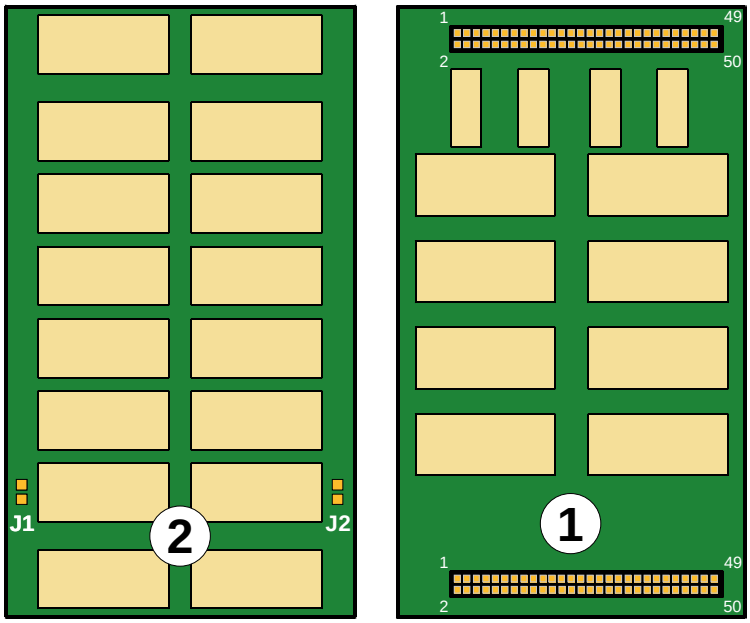
A.5 DM603

The DM603 is a memory piggyback fitted with:

- DRAM: 32 MB
- FLASH MEMORY:0, 0.5 (512 KB), 1, 2, or 4 MB

A.5.1 Board Layout and Jumper Location

Figure A-4: DM603 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.5.2 Jumper Description and Flash Addresses

Table A-5: Jumpers: J1 and J2 Settings and Flash Memory Address Ranges

Setting		Description	512KB or 1MB Flash	2MB Flash	4MB Flash
J1	*Set*	*No Protection*			
	Open	Flash Bank 0: Write protected	Lower 512 KB		Lower 2 MB
		Flash Bank 0: Address Range	0x04000000 - 0x04080000	0x04000000 - 0x04200000	0x04000000 - 0x04200000
J2	*Set*	*No Protection*			
	Open	Flash Bank 1: Write protected	Upper 512 KB (1MB only)		Upper 2 MB
		Flash Bank 1: Address Range	0x04080000 - 0x04100000		0x04020000 - 0x04400000

Default settings are in italics.

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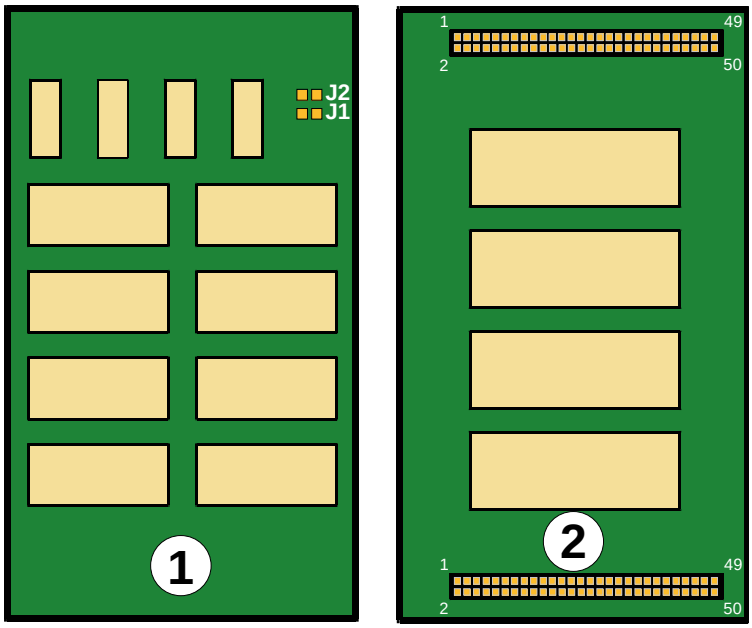
A.6 DM604

The DM604 is a memory piggyback fitted with:

- DRAM: 8 MB
- FLASH MEMORY:1or 4 MB

A.6.1 Board Layout and Jumper Location

Figure A-5: DM604 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.6.2 Jumper Description and Flash Addresses

Table A-6: Jumpers: J1 and J2 Settings and Flash Memory Address Ranges

Setting		Description	1MB Flash	4MB Flash
J1	*Set*	*No Protection*		
	Open	Flash Bank 0: Write protected	Lower 512 KB	Lower 2 MB
		Flash Bank 0: Address Range	0x04000000 - 0x04080000	0x04000000 - 0x04200000
J2	*Set*	*No Protection*		
	Open	Flash Bank 1: Write protected	Upper 512 KB (1MB only)	Upper 2 MB
		Flash Bank 1: Address Range	0x04080000 - 0x04100000	0x04020000 - 0x04400000

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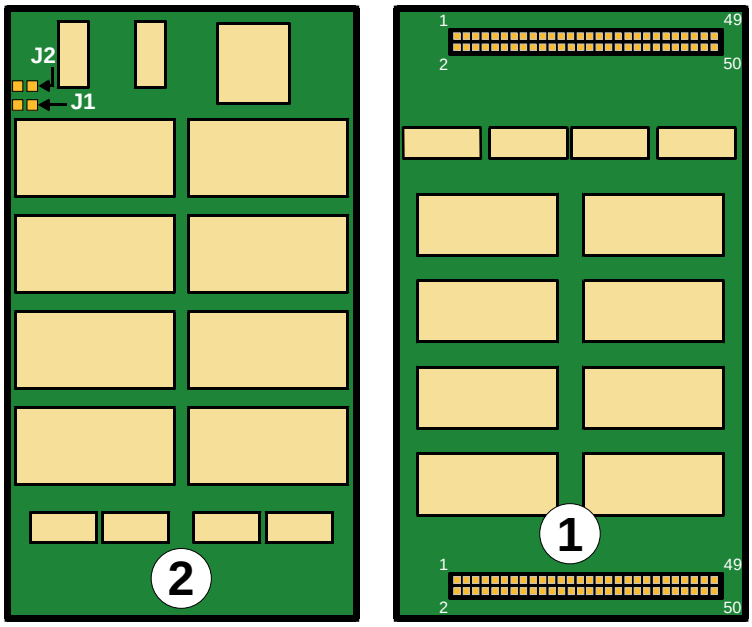
A.7 DM605

The DM605 is a memory piggyback fitted with:

- DRAM: 64 MB
- FLASH MEMORY:1or 4 MB

A.7.1 Board Layout and Jumper Location

Figure A-6: DM605 Memory Piggyback



Legend:

1. Flash Memory
2. DRAM

A.7.2 Jumper Description and Flash Addresses

Table A-7: Jumpers: J1 and J2 Settings and Flash Memory Address Ranges

Setting		Description	1MB Flash	4MB Flash
J1	*Set*	*No Protection*		
	Open	Flash Bank 0: Write protected	Lower 512 KB	Lower 2 MB
		Flash Bank 0: Address Range	0x04000000 - 0x04080000	0x04000000 - 0x04200000
J2	*Set*	*No Protection*		
	Open	Flash Bank 1: Write protected	Upper 512 KB (1MB only)	Upper 2 MB
		Flash Bank 1: Address Range	0x04080000 - 0x04100000	0x04020000 - 0x04400000

Default settings are in italics.

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Appendix B

Serial Interface Piggybacks

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B. Serial Interface Piggybacks

B.1 General

The serial interface (SI) piggybacks described herein adapt the multi-protocol serial channels of the 68EN360 controller chip to one of the following physical interfaces:

- 10Base2 (thin or cheapernet) Ethernet,
- 10Base5 (AUI) Ethernet,
- 10BaseT (twisted pair) Ethernet,
- RS-232 modem compatible,
- RS485 optoisolated (PROFIBUS),

and are available for a wide variety of PEP CPU boards.

Table B-1: SI Piggyback Types and Configurations

Type	Configuration	
	Standard	Connectors
SI-10B2	10Base2 (Ethernet: thin)	RG58 (Coaxial)
SI-10B5	10Base5 (AUI)	D-Sub (15-pin)
SI-10BT	10BaseT (Twisted-pair)	RJ45 (8-pin)
SI-PB232	RS-232 (Modem interface)	2 x RJ45 (8-pin)
SI-PB485-ISO	RS485 (Optoisolated, 2 wire half-duplex, PROFIBUS)	D-Sub (9-pin)

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B.2 SI-10B2

The SI-10B2 is a physical cheapernet (10Base2) interface to the 68EN360 Controller chip. It connects one of the range of PEP CPU boards to a 50 ohm coax cable via an RG58 BNC 'T' connector.

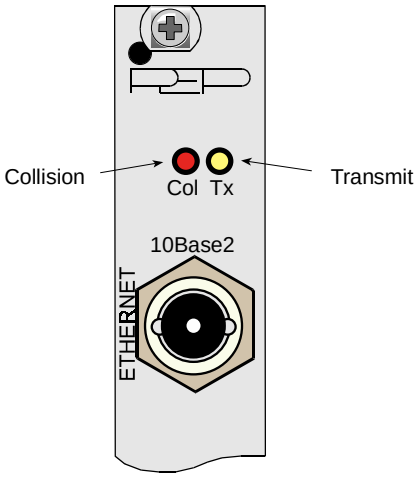
The SI6-10B2 has two LEDs fitted; a red LED indicates collision detection and a yellow LED for data transmission.

B.2.1 Specifications

On-board termination:	None (Cheapernet cable is terminated at both ends)
Max. Baudrate:	10Mbit/s according to Ethernet specification

B.2.2 Front Panel View

Figure B-1: SI-10B2 Serial Interface Piggyback



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B.3 SI-10B5

The SI-10B5 is a physical AUI interface to the 68EN360 Controller chip.

B.3.1 Specifications

On-board termination:	None
Max. Baudrate	10Mbit/s according toEthernet specification

B.3.2 Front Panel View and Pinout

Figure B-2: SI-10B5 Serial Interface Piggyback

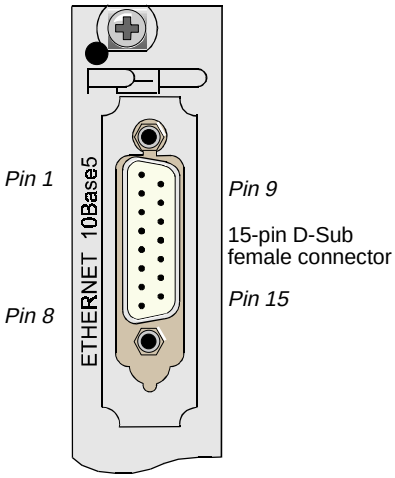


Table B-2: SI-10B5 Connector Pinout

Pin	Signal	Pin	Signal
1	Control IN circuit shield	9	Control IN circuit shield
2	Control IN circuit A	10	Data OUT circuit B
3	Data OUT circuit A	11	Data OUT circuit shield
4	Control IN circuit shield	12	Data IN circuit B
5	Data IN circuit A	13	+12V*
6	Voltage common	14	GND
7	N/C	15	N/C
8	N/C		

* *The SI-10B5 requires an external +12V from the base board. For further details please refer to the relevant base board manual*

N/C Not connected

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B.4 SI-10BT

The SI-10BT is a physical twisted pair (10BaseT) interface to the 68EN360 Controller chip. It connects one of the range of PEP CPU boards to an unshielded 100ohm twisted-pair cable via an RJ45 telephone jack.

The SI-10BT has two LEDs fitted: a red LED indicates collision detection and a yellow LED for data.

B.4.1 Specifications

On-board termination:	100ohm
Max. Baudrate:	10Mbit/s according to Ethernet specification

B.4.2 Front Panel View, Jumper Layout, and Pinouts

Figure B-3: SI-10BT Serial Interface Piggyback

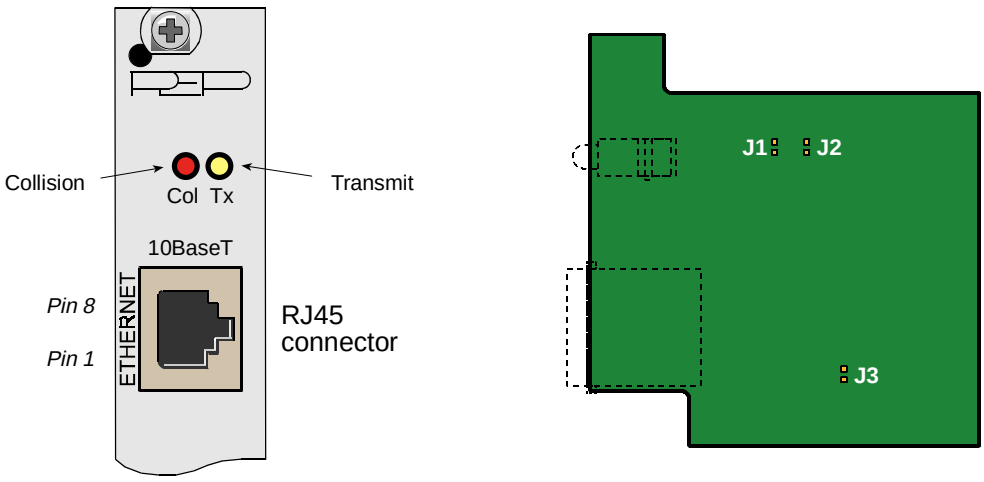


Table B-3: SI-10BT Connector Pinout

Pin	Signal
1	TD+
2	TD+
3	RD+
4	N/C
5	N/C
6	RD-
7	N/C
8	N/C

N/C *Not connected*

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4.2.1 SI-10BT Jumper Settings

Table B-4: Jumper J1 – Squelch Threshold

Setting	Descirption
Open	*Normal*
Set	4.5dB reduced threshold

Default settings are in italics.

Table B-5: Jumper J2 – Link Test

Setting	Descirption
Open	*Link Test enabled*
Set	Link Test disabled

Default settings are in italics.

Table B-6: Jumper J3 – Shielding

Setting	Descirption
Open	*Unshielded, 100 ohm termination*
Set	Shielded, 150ohm termination

Default settings are in italics.

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B.5 SI-PB232

The SI-PB232 provides two RS-232 serial interfaces to the 68EN360 Controller chip. It connects one of the range of PEP CPU boards via two RJ45 telephone jacks.

B.5.1 Front Panel View and Pinout

Figure B-4: SI-PB232 Serial Interface Piggyback

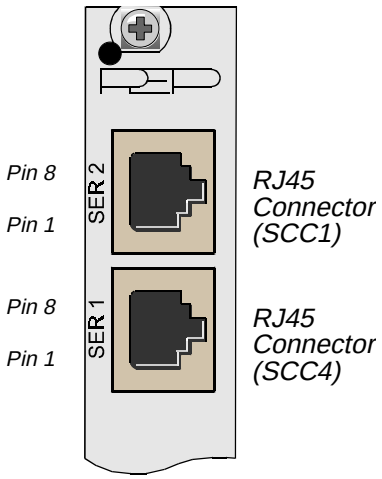


Table B-7: SI-PB232 Connectors SER1 and SER2 Pinouts

Pin	Signal
1	DSR
2	RTS
3	GND
4	TXD
5	RXD
6	DCD
7	CTS
8	DTR

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B.6 SI-PB485-ISO

The SI-PB485-ISO is an RS-485 optoisolated interface piggyback for 2-wire half-duplex (PROFIBUS) connection. It has one LED fitted indicating data transmission.

B.6.1 Specifications

On-board termination:	150ohm, jumper selectable
Isolation voltage	Optocoupler specified up to 2.5kV
Max. baudrate	1.5MBaud

B.6.2 Front Panel View, Jumper Layout, and Pinout

Figure B-5: SI-PB485-ISO Serial Interface Piggyback

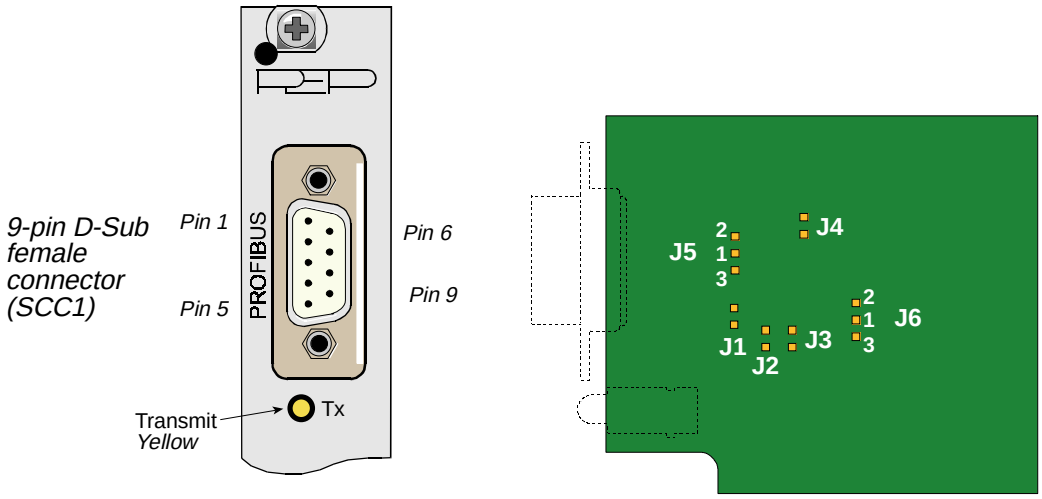


Table B-8: SI-PB485-ISO Connector Pinout

Pin	Signal	Description
1	N/C	—
2	N/C	—
3	RxD+/TxD+	Receive/Transmit Data plus
4	N/C	—
5	DGND	Data Ground (GND 5V)
6	VP	Voltage Plus (+5V)
7	N/C	—
8	RxD-/TxD-	Receive/Transmit minus
9	N/C	—

N/C Not connected

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B.6.3 SI-PB485-ISO Jumper Settings

Table B-9: Jumpers J1 and J2 – End-of-Line Termination

Setting	Description
Open	*No internal line termination*
Set	internal line termination

Default settings are in italics.

Table B-10: Jumpers J3 and J4 – Idle Setting

Setting	Description
Open	*No internal idle status*
Set	Internal idle status

Default settings are in italics.

Table B-11: Jumper J5 – Isolation Voltage Supply

Setting	Description
1 - 3	*Isolating VCC supplied internally*
1 - 2	Shielded, 150-ohm termination

Default settings are in italics.

Table B-12: Jumper J6 – Received Control

Setting	Description
1 - 3	*Receive permanently enabled*
1 - 2	Receive enabled

Default settings are in italics.

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Appendix C

CXC

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C. CXC

The Controller eXtension Connector (CXC) is the local interface. It contains a 16-bit data bus, seven address lines and eight decoded chip select lines. Each select line has 256 Bytes. In total, there are eight select signals.

C.1 CXC Address Ranges

The following tables provide address range information for both the CXC standard backplanes as well as the enhanced CXC backplanes (ECXC) for the CPU boards indicated.

Table C-1: CXC Address Range

Slot	Chip Select	[V]IUC VSBC-4	VM30	VSBC-32 IUC32	VM(6)42 VM(6)62	VSBC-860
BU2	CS0	0xF70000	0xC1F70000	0x0BF70000	0xCBF70000	0xB0000000
BU3	CS1	0xF70400	0xC1F70400	0x0BF70400	0xCBF70400	0xB1000000
BU4	CS2	0xF70800	0xC1F70800	0x0BF70800	0xCBF70800	0xB2000000
BU5	CS3	0xF70C00	0xC1F70C00	0x0BF70C00	0xCBF70C00	0xB3000000
BU6	CS4	0xF71000	0xC1F71000	0x0BF71000	0xCBF71000	0xB4000000
BU7	CS5	0xF71400	0xC1F71400	0x0BF71400	0xCBF71400	0xB5000000
BU8	CS6	0xF71800	0xC1F71800	0x0BF71800	0xCBF71800	0xB6000000
BU0**	CS7	0xF71C00	0xC1F71C00	0x0BF71C00	0xCBF71C00	0xB7000000

* *BU1 is the system slot*
** *On 5S, 8S, and 8ES for CXM-STAT1 only.*

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Table 1-2: Enhanced CXC Address Range

Slot	Chip Select	VSBC-860	VSBC-32 IUC32	VM642 VM662
BU2	CS0	0xB0000000	0x10000000	0x10000000
BU3	CS1	0xB1000000	0x11000000	0x11000000
BU4	CS2	0xB2000000	0x12000000	0x12000000
BU5	CS3	0xB3000000	0x13000000	0x13000000
BU6	CS4	0xB4000000	0x14000000	0x14000000
BU7	CS5	0xB5000000	0x15000000	0x15000000
BU8	CS6	0xB6000000	0x16000000	0x16000000
BU0*	CS7	0xB7000000	0x17000000	0x17000000

* *BU1 is the system slot*
** *On 5S, 8S, and 8ES for CXM-STAT1 only.*

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C.2 CXC Generic Pinouts

Table 1-3: CXC Connector Pinouts

Pin	Signals		
	Row A	Row B	Row C
1	IRQ_1	SER1_RCLK	User-defined
2	IRQ_2	SER1_TCLK	_DMA_ACK
3	IRQ_3	GND	_DMA_REQ
4	IRQ_4	SER1_TXD	User-defined
5	User-defined	SER1_RTS[1)]	SER3_TCLK
6	User-defined	GND	SER3_RCLK
7	VCC	SER3_RTS[1)]	VCC
8	User-defined	SER3_CD[1)]	SER3_TXD
9	User-defined	GND	SER3_RXD
10	User-defined	SER1_RXD	User-defined
11	SER2_DTR	User-defined	SER2_CD[1)]
12	SER3_DTR	GND	SER2_RTS[1)]
13	SER1_DTR	SER1_CTS[1)]	SER2_CTS[1)]
14	VCC	SER1_CD[1)]	VCC
15	_CS-CXC[1)]	GND	SER2_TCLK
16	_AS[1)]	SER3_CTS[1)]	SER2_RCLK
17	R/_W[1)]	_SYSR	SER2_TXD
18	_UDS[1)]	GND	SER2_RXD
19	_LDS[1)]	_EDTACK	VCC
20	VCC	CXC-CLK	_CS2[1)]
21	A1	GND	_CS3[1)]
22	A2	_CS0[1)]	_CS4[1)]
23	A3	_CS1[1)]	_CS5[1)]
24	A4	GND	_CS6[1)]
25	A5	A6	_CS7[1)]
26	VCC	A7	VCC
27	D0	GND	D10
28	D1	D6	D11
29	D2	D7	D12
30	D3	GND	D13
31	D4	D8	D14
32	D5	D9	D15

1) *Normally active low (by R/_W, only _W).*

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C.3 CPU Pinout Cross Reference

The table below shows a cross reference of the special CXC released by the MC68302 and the MC68EN360.

Table 1-4: Cross Reference of MC68302/MC68(EN)360 to CXC Signals

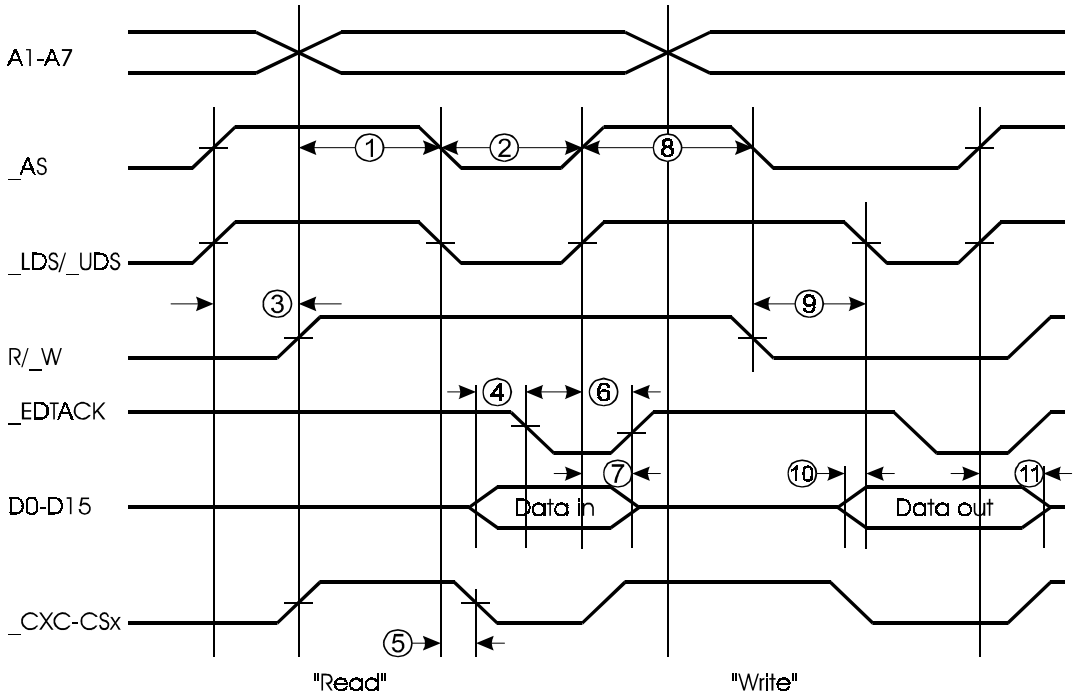
Pin	MC68302	MC68(EN)360	CXC Signals
A1	PB11	PC0/_RTS1/L1ST1	IRQ_1
A2	PB10	PC1/_RTS2/L1ST2	IRQ_2
A3	PB9	PC2/_RTS3/_L1RQB/L1ST3	IRQ_3
A4	PB8	PC3/_RTS4/_L1RQA/L1ST4	IRQ_4
A5	PB7/_WDOG	PB0/_SPISEL/_RRJCT1	User-defined
A6	PB6/_TOUT2	PB1/SPICLK/_RSTRT2	User-defined
A8	PB5/TIN2	PB2/SPIMOSI(SPITXD)/_RRJCT2	User-defined
A9	PB4/_TOUT1	PB3/SPIMISO(SPIRXD)/BRGO4	User-defined
A10	PB3/TIN1	PB8/_SMSYN1/_DREQ2	User-defined
A11	PB2/_IACK1	PB16/BRGO3/STRBO	SER2_DTR
A12	PB1/_IACK6	PB9/_SMSYN2/_DACK2	SER3_DTR
A13	PB0/_IACK7	PB17/_RSTRT1/STRBI	SER1_DTR
B1	RCLK1	PA8/CLK1/BRGO1/L1RCLKA/TIN1	SER1_RCLK
B2	TCLK1	PA10/CLK3/BRGO2/L1TCLKA/TIN2	SER1_TCLK
B4	TXD1	PA3/TXD2	SER1_TXD
B5	RTS1	PB13/_RTS2/L1ST2	SER1_RTS
B7	RTS3	PB15/_RTS4/_L1RQA/L1ST4	SER3_RTS
B8	CD3	PC11/_CD4/_L1RSYNCA	SER3_CD
B10	RXD1	PA2/RXD2	SER1_RXD
B11	BRG1	PB10/SMTXD2/L1CLKOB	User-defined
B13	CTS1	PC6/_CTS2	SER1_CTS
B14	CD1	PC7/_CD2/_TGATE2	SER1_CD
B16	CTS3	PC10/_CTS4/_L1TSYNCA/_SDACK1	SER3_CTS
C1	DONE	PB6/SMTXD1/_DONE1	User-defined
C2	DACK	PB5/BRGO2/_DACK1	DMA_ACK
C3	DREQ	PB4/BRGO1/_DREQ1	DMA_REQ
C4	BRG3	PB11/SMRXD2/L1CLKOA	User-defined
C5	TCLK3	PA14/CLK7/BRGO4/TIN4	SER3_TCLK
C6	RCLK3	PA15/CLK8/_TOUT4/L1TCLKB	SER3_RCLK
C8	TXD3	PA7/TXD4/L1RXDA	SER3_TXD
C9	RXD3	PA6/RXD4/L1TXDA	SER3_RXD
C10	BRG2	PB7/SMRXD1/_DONE2	User-defined
C11	CD2	PC9/_CD3/_L1RSYNCB	SER2_CD
C12	RTS2	PB14/_RTS3/_L1RQB/L1ST3	SER2_RTS
C13	CTS2	PC8/_CTS3/_L1TSYNCB/SDACK2	SER2_CTS
C15	TCLK2	PA12/CLK5/BRGO3/TIN3	SER2_TCLK
C16	RCLK2	PA13/CLK6/_TOUT3/L1RCLKB/BRGCLK2	SER2_RCLK
C17	TXD2	PA5/TXD3/L1RXDB	SER2_TXD
C18	RXD2	PA4/RXD3/L1TXDB	SER2_RXD

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C.4 Timing

Figure C-1: (E)CXC Signal Timing



Legend:

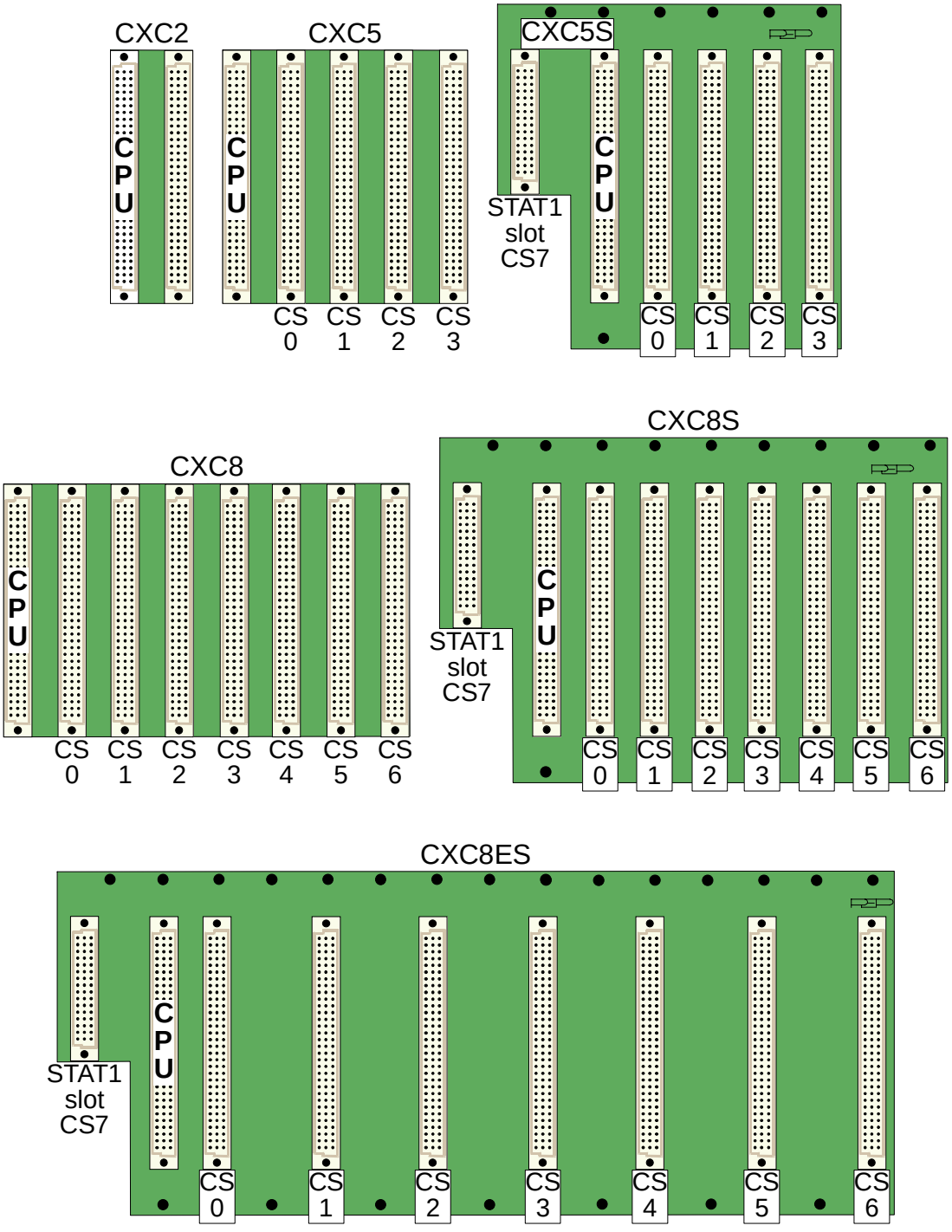
		Min.	Max.
1.	Address valid to_AS, _DS	10ns	-
2.	_AS asserted	80ns	-
3.	_AS negated to R/_W invalid	10ns	-
4.	Data-in valid to _EDTACK	0ns	-
5.	_CXC-CSx asserted to AS valid	-	25ns
6.	_EDTACK negated to AS negated	0ns	90ns
7.	Data-in hold time	0ns	50ns
8.	_AS negated	50ns	-
9.	_AS, R/_W asserted to _DS asserted	20ns	-
10.	Data-out valid to _DS asserted	15ns	-
11.	_AS, _DS negated to data-out invalid	0ns	-

A1-A7: address lines
_AS: address strobe
_LDS/_UDS: lower/upper data strobe
R/_W: read not write
_EDTACK: external data transfer acknowledge
_CXC-CSx: _CXC-CS0 to _CXC-CS7

Recommended: Assert _EDTACK with CSx and _UDS/_LDS and "data valid" during read cycles
Latch data with CSx and _UDS/_LDS during write cycles
Negate _EDTACK with _UDS/_LDS invalid

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C.5 CXC Backplanes



Note:

When using an 8TE board on the CXC5 and CXC8 backplane, one slot is lost between each board and the next.

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Appendix D

OS-9 Cabling

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D. OS-9 Cabling

This appendix outlines the connection definitions of OS-9 systems to various outside media.

D.1 OS-9 System – Terminal

D.1.1 Software (XON/XOFF) or No Handshake

Figure D-1: 15-Pin Connector on OS-9 Side

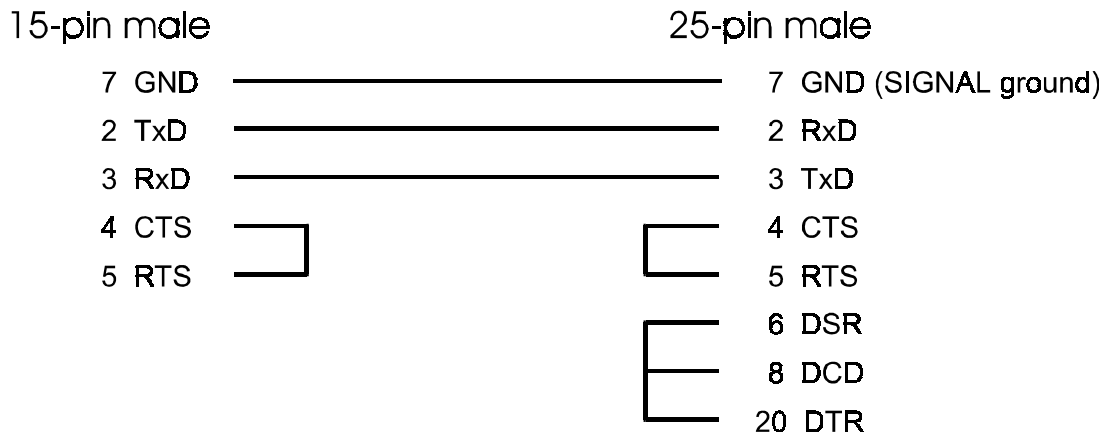
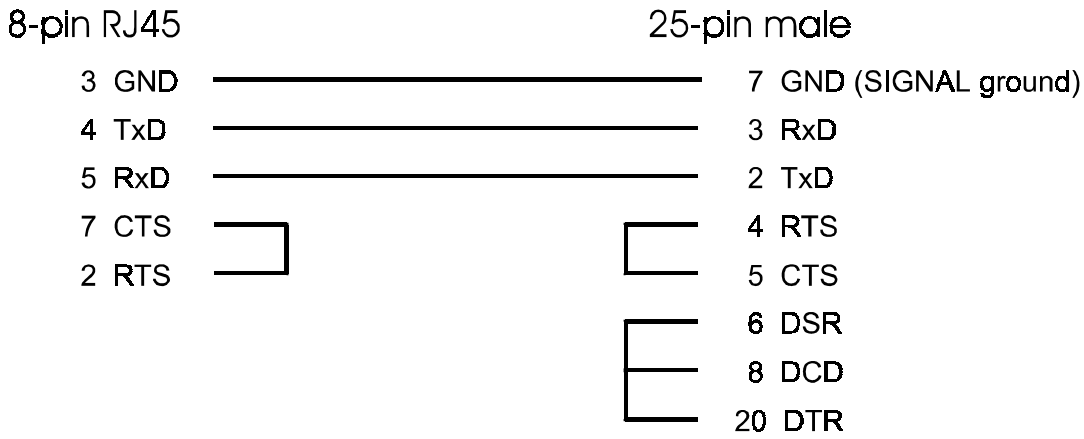
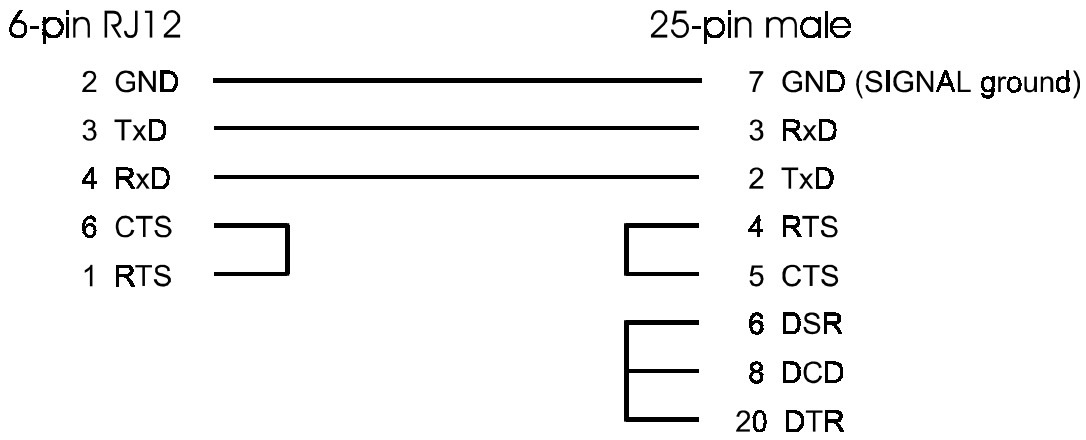


Figure D-2: 8-Pin RJ45 Connector on OS-9 Side (SMART I/O)



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Figure D-3: 6-Pin RJ12 Connector on OS-9 Side



D.1.2 Hardware Handshake (Set Terminal to CTS/DTR Handshake)

Figure D-4: 15-Pin Connector on OS-9 Side

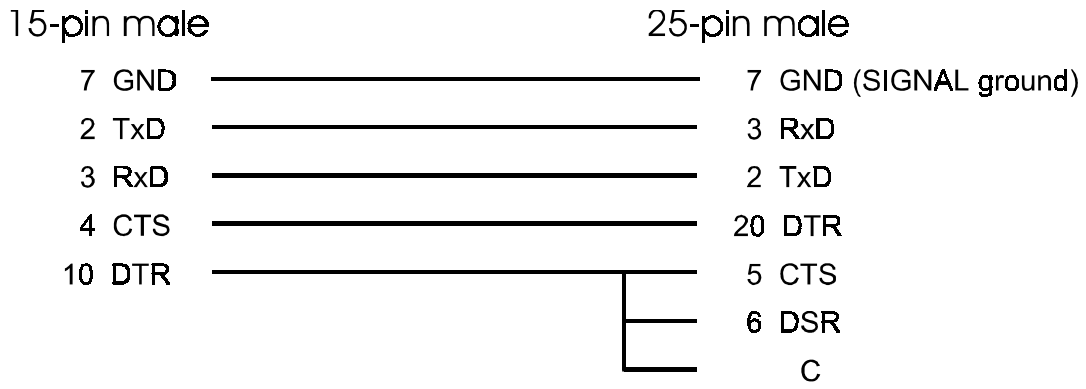
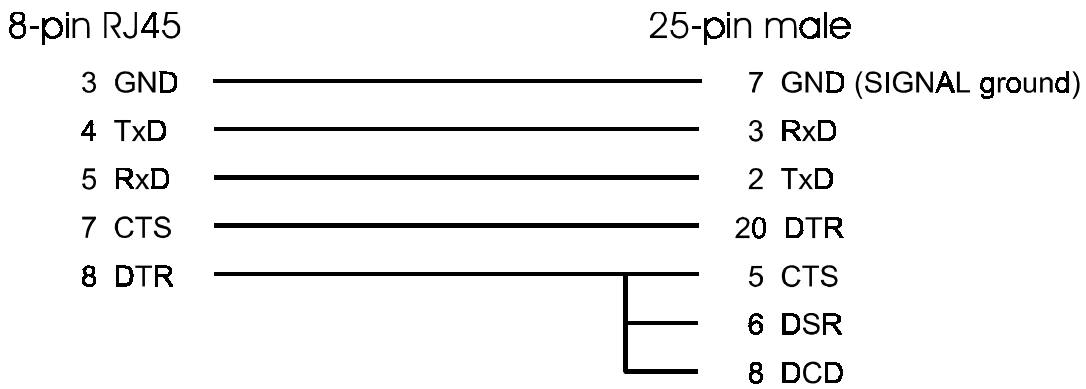


Figure D-5: 8-pin RJ45 Connector on OS-9 Side (SMART I/O)



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D.2 OS-9 System – PC

D.2.1 Software (XON/XOFF) or No Handshake

Figure D-6: 15-pin Connector on OS-9 Side, 25-pin Connector on PC Side

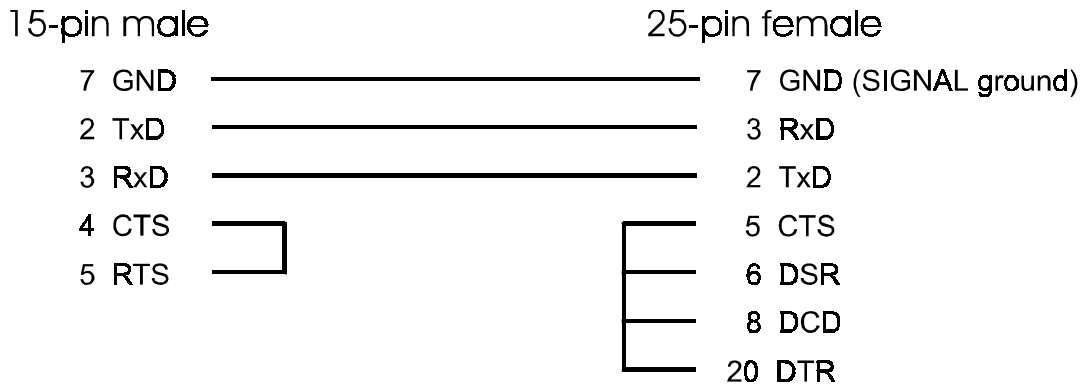
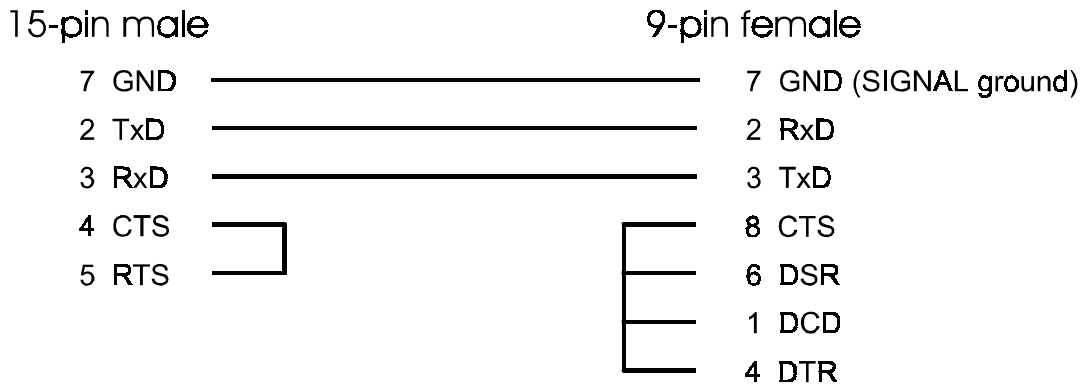


Figure D-7: 15-pin Connector on OS-9 Side, 9-pin Connector on PC Side



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Figure D-8: 8-pin RJ45 Connector on OS-9 Side (SMART I/O), 25-Pin Connector on PC Side

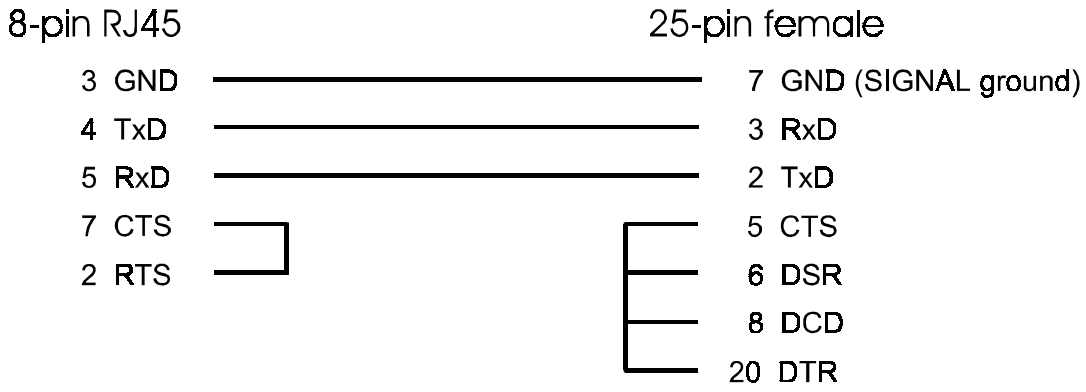


Figure D-9: 6-pin RJ12 Connector on OS-9 Side, 25-Pin Connector on PC Side

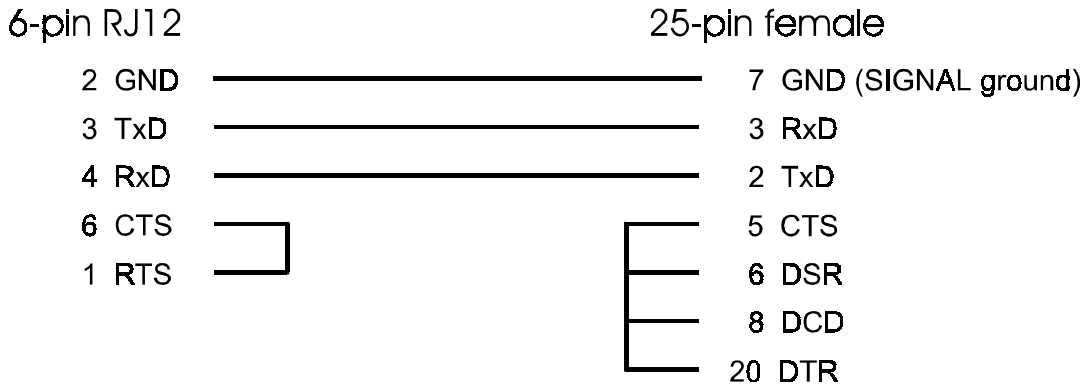
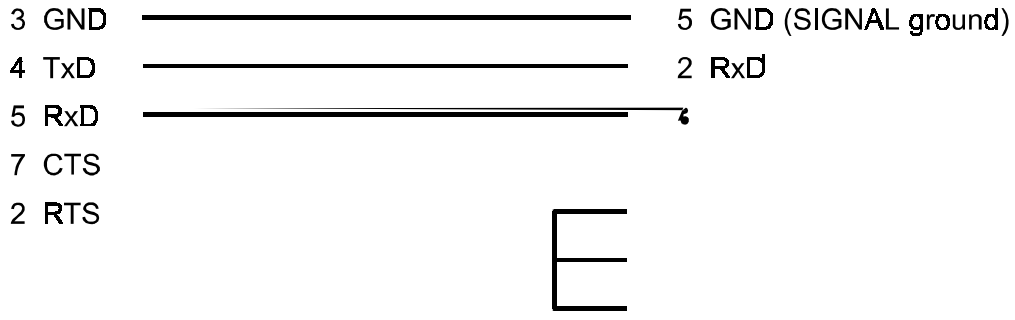


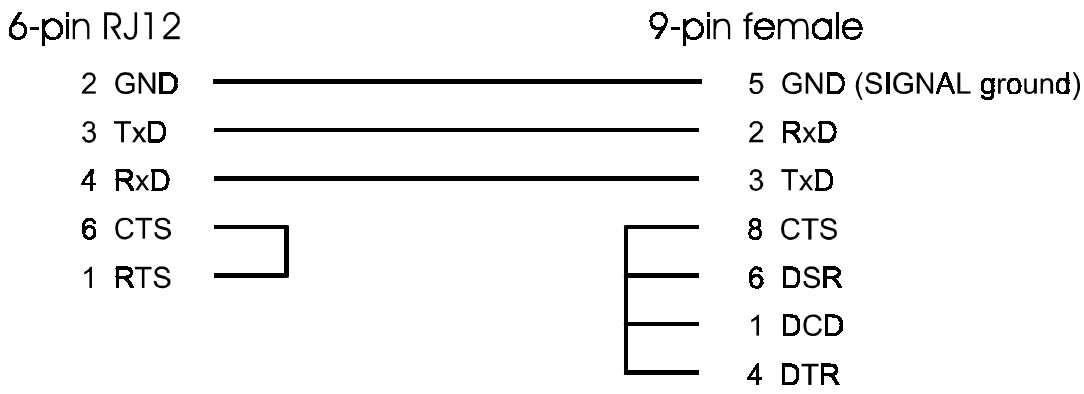
Figure D-10: 8-Pin RJ45 Connector on OS-9 Side (SMART I/O), 9-Pin Connector on PC Side



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Figure D-11: 6-pin RJ12 Connector on OS-9 Side, 9-pin Connedctor on PC Side



D.2.2 Hardware Handshake (Select RTS/CTS Handshake on the PC Side)

Figure D-12: 15-pin Connector on OS-9 Side, 25-pin Connector on PC Side

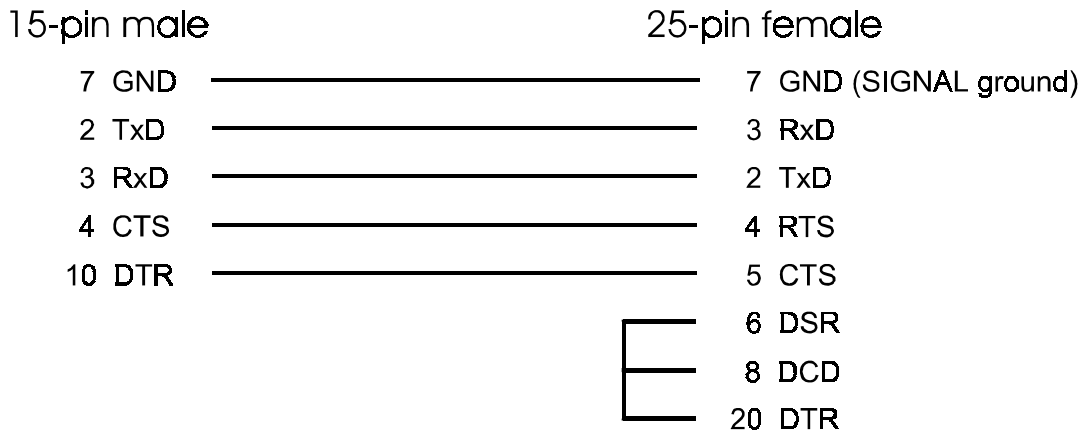
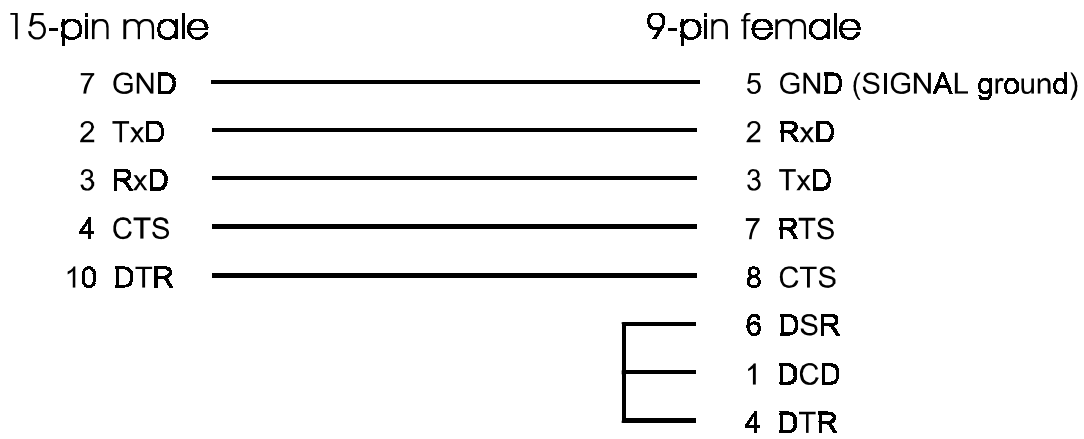


Figure D-13: 15-pin Connector on OS-9 Side, 9-pin Connector on PC Side



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Figure D-14: 8-pin RJ45 Connector on OS-9 Side (SMART I/O), 25-Pin Connector PC Side

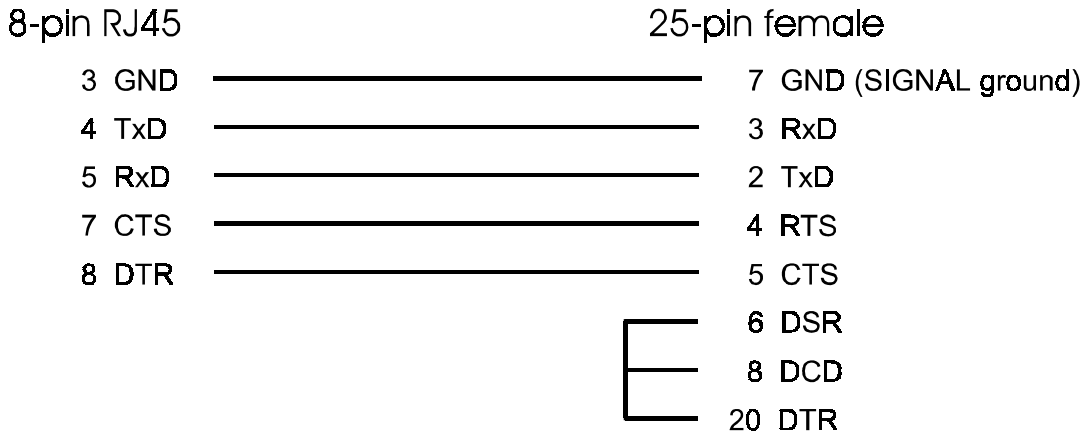
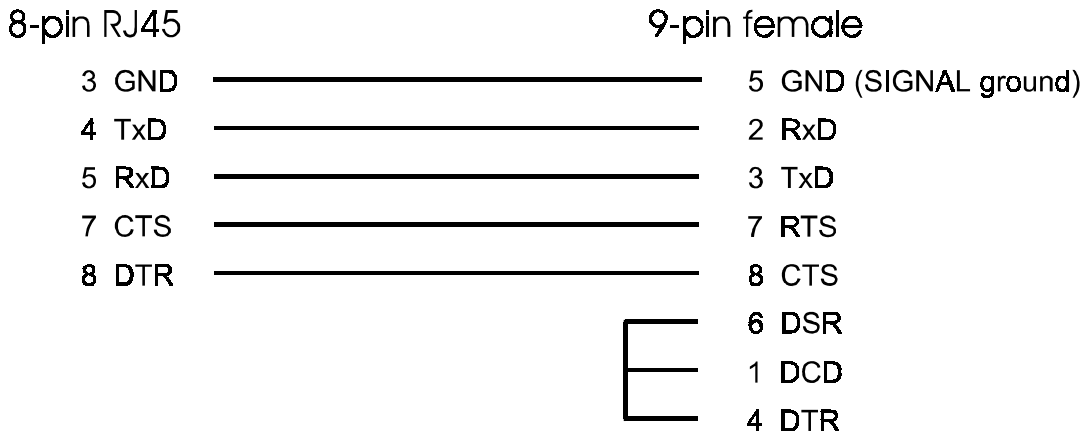


Figure D-15: 8-Pin Connector on OS-9 Side (SMART I/O), 9-Pin Connector on PC Side



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D.3 OS-9 System – Modem

Figure D-16: 15-pin Connector

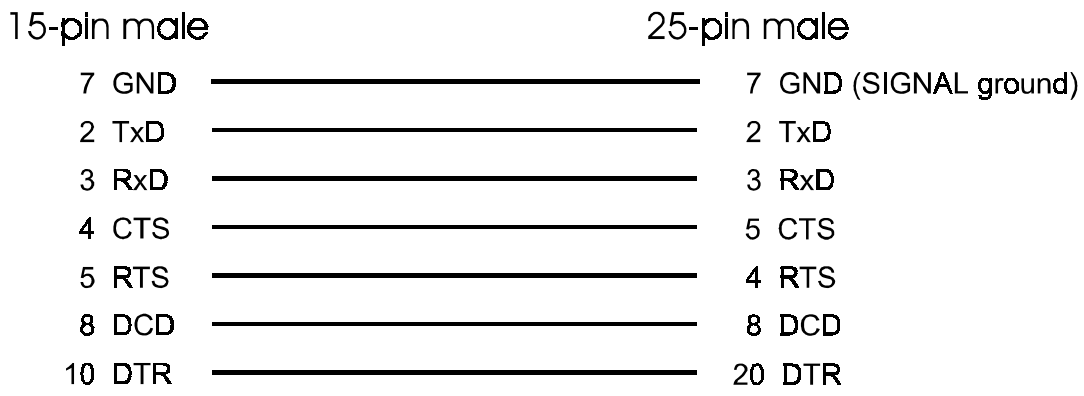
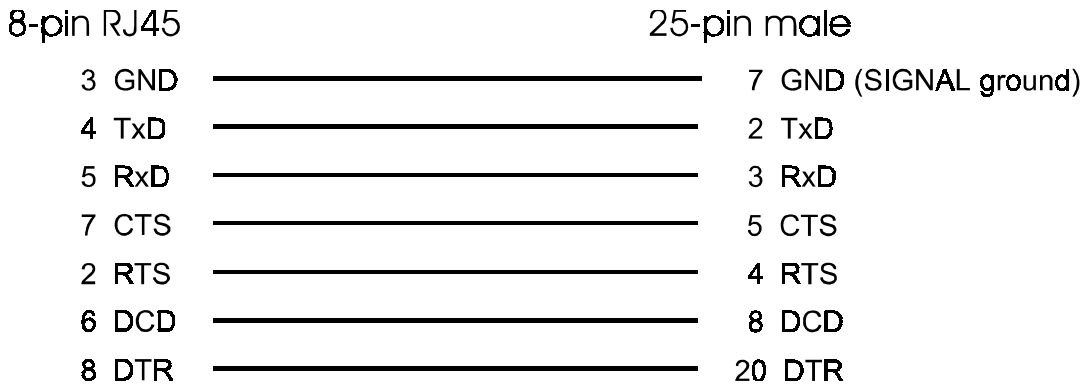


Figure D-17: 8-pin RJ45 Connector (SMART I/O)



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D.4 OS-9 System – OS-9 System

D.4.1 Software (XON/XOFF) or No Handshake

Figure D-18: 15-pin Connector

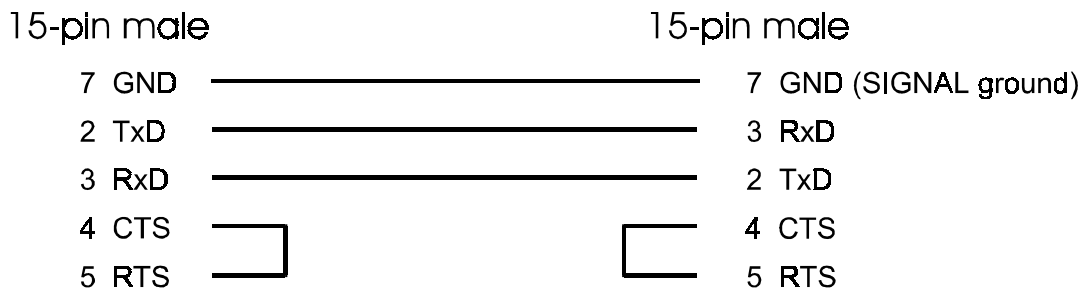


Figure D-19: 8-pin RJ45 Connector (SMART I/O)

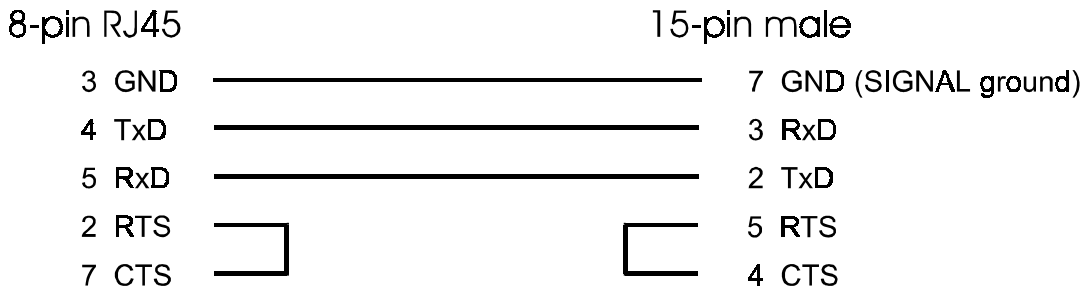
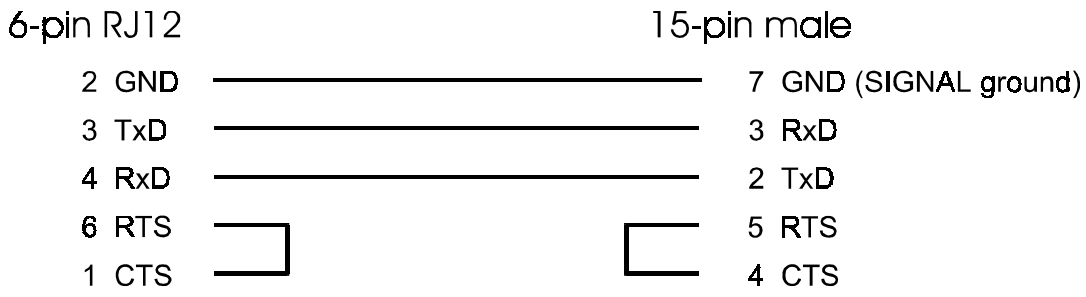


Figure D-20: 6-pin RJ12 Connector



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D.4.2 Hardware Handshake

Figure D-21: 15-pin Connector

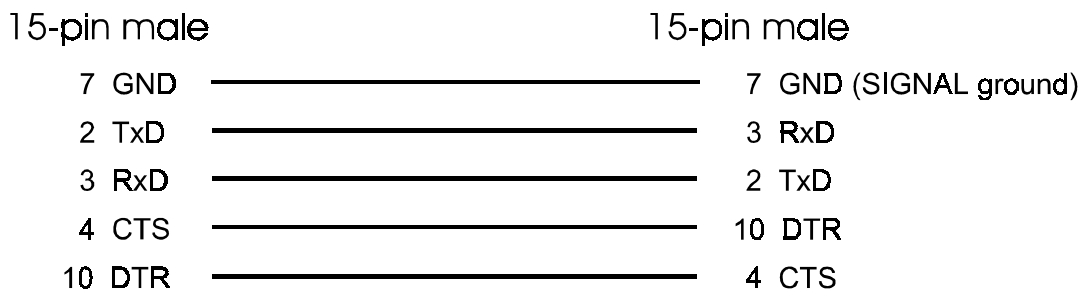
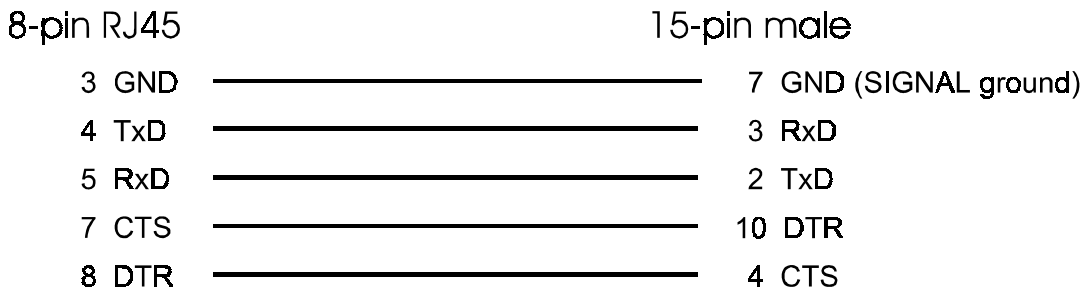


Figure D-22: 8-pin RJ45 Connector (SMART I/O)



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