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PB-DIN3

OPTOISOLATED DIGITAL INPUT

PIGGYBACK FOR VMOD-2 AND IMOD

ID: 03113 Index: 0300

USER'S MANUAL

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PRODUCT HISTORY:

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0300	TITLEPAGE UPDATED	SEPTEMBER 1997

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Observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. These can cause shorts and damage to the batteries or tracks on the board.

When installing piggybacks, switch off the power mains.

Furthermore, do not exceed the specified operational temperature ranges of the board version ordered. If batteries are present, their temperature restrictions must be taken into account.

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1. INTRODUCTION

1.1 Product Overview

The PB-DIN3 is a 20 channel optoisolated input piggyback, with 16 lines for logical level (24V DC) input and four status/interrupt inputs.

PB-DIN3 can be used either with the VMOD-2 (non-intelligent input/output module for the VMEbus), or with the IMOD.

1.2 Ordering Information

Name	Description	Order Number	
PB-DIN3	VMOD-2/IMOD piggyback with 20 digital optoisolated 24V DC input/output channels. Input filter	5230-33 3102	*Old* *New*

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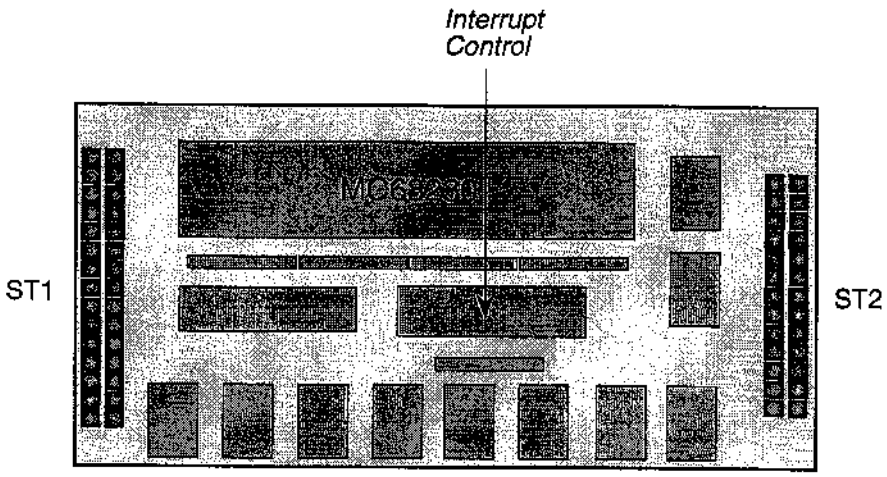
1.3 Specifications

Input channels	16 digital inputs plus 4 status/interrupt lines Common GND (2 groups of 8+2), optoisolated
Input voltage	24V DC typically
Input current	5mA at 24V typically
Switching level	<10V = low, >16V = high
Input filter	t_{rise}=20ms, t_{fall}=10ms
Isolation voltages	2500V RMS input to system 100V DC between inputs
Timer	24 bit
Timer clock	8 MHz
Identification byte	$F3
Address range	128 byte
DTACK generation	On-board
Power requirements	+5V DC (+/- 5%) 100mA typically
Temperature range Standard Extended Storage	 0...+70°C -40...+85°C -55 to +85°C
Operating humidity	0 to 95% (Non-condensing)
Piggyback dimensions	Width: 48mm Length: 100mm Depth: 12 mm
VMOD-2 interface	Two sets of twin row header pins providing all necessary communication paths and a mechanical mounting method.

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1.4 Board Overview

Component Side



1.5 Features

- Optoisolated input
- Input filter
- Software selectable channels; ports can work in a variety of different ways
- 24-bit programmable timer
- Interrupt request line. The interrupt vector is generated by piggybacks
- On-board DTACK generation

1.6 Advantages

The PB-DIN3 is designed to provide an easy to use interface for customer applications. The PB-DIN3 provides a cost-effective solution, quick and easy implementation as well as full compatibility with existing PEP products.

The piggyback can be used with the VMOD-2 or the IMOD carrier modules.

1.7 Related Publications

VMEbus Specifications Revision C1
Data Sheet for the MC68230 from Motorola

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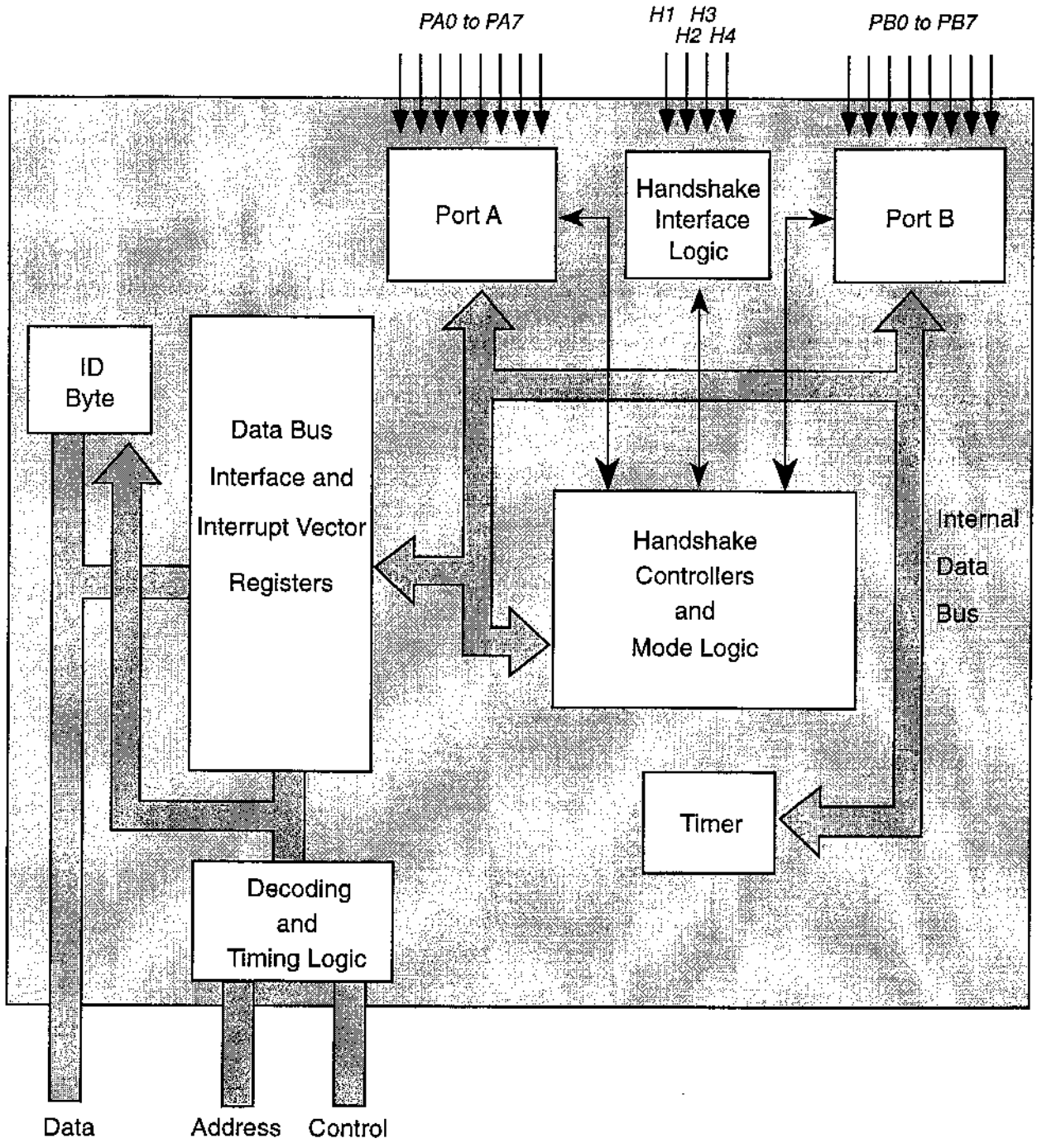
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2

2. FUNCTIONAL DESCRIPTION

This chapter describes the functionality of the main blocks of the PB-DIN3 piggyback.

Figure 2.0.0.1: PB-DIN3 Block Diagram



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2.1 The MC68230 Parallel Interface and Timer Chip (PI/T)

The MC68230 parallel interface and timer (PI/T) provides versatile double buffered interfaces and a system-oriented timer for MC68000 systems. The parallel interfaces operate either at 8 or 16 bits wide in unidirectional mode. An associated data direction register has to be set for input.

The PI/T timer contains a 24-bit counter and a 5-bit prescaler. The timer is clocked by the system clock (PI/T CLK pin) and the 5-bit prescaler may be used. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed time period. It can also be used for elapsed time measurement or as a device watchdog.

The main features of the PI/T include:

- MC68000 bus compatible
- Port Modes: Bit I/O
  Unidirectional 8 and 16 bit
- 24-bit programmable timing modes
- 5 seperate interrupt vectors
- Seperate port and timer interrupt service requests
- Registers are Read/Write and directly accessable

The PI/T consists of two logically independent sections: the ports and the timer. The port section consists of port A (PA0 to PA7), port B (PB0 to PB7) and four handshake pins (H1, H2, H3 and H4). The four programmable handshake pins, depending on the mode, can be used as interrupt generating inputs or status input pins.

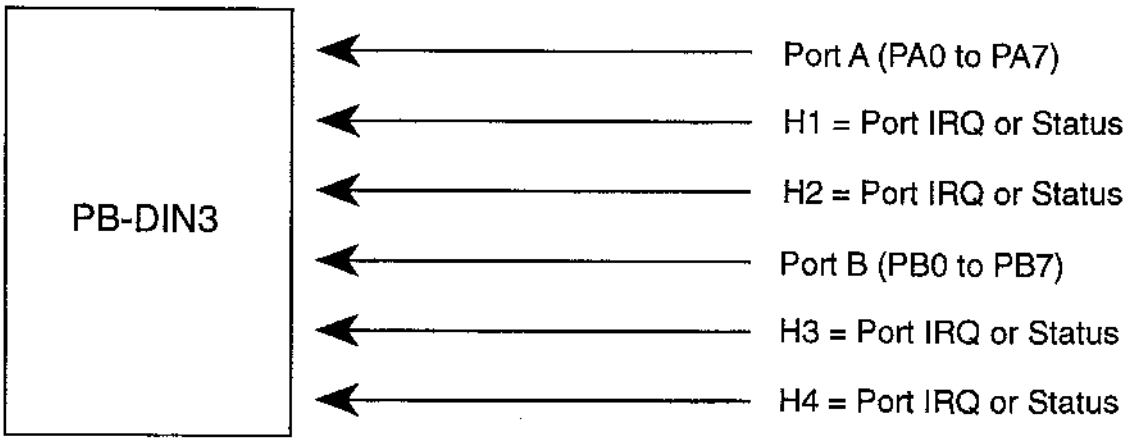
The timer consists of a 24-bit counter, optionally clocked by a 5-bit prescaler.

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2.2 The Input Ports

The two input ports each consist of eight unidirectional lines and two multifunction handshake lines. This is illustrated in the Figure below.

Figure 2.2.0.1: The PB-DIN3 Input Ports



Above all, the TTL input port enables the realisation of simple bit input of industrial applications such as switch operation or polling for the control of user-defined peripherals. Implementation of the individual bits is left completely up to the user.

The examples in chapter 4 illustrate the necessary initialisation procedures for the applications discussed above.

2.2.1 PI/T Port Modes

The PI/T can generally be used in 4 different port modes:

Mode 0:	Unidirectional 8-bit mode	
Mode 1:	Unidirectional 16-bit mode	
Mode 2:	*Bidirectional 8-bit mode*	*Not intended for the PB-DIN3*
Mode 3:	*Bidirectional 16-bit mode*	*Not intended for the PB-DIN3*

The PB-DIN3 is most suitable in mode 1. Mode 0 is also possible if different definitions for Port A and B are required (e.g. one non-latched input, one double buffered input).

2.2.2 The Handshake Pins H1, H2, H3 and H4

The four handshake pins are connected for use as inputs. The PI/T port mode control selects between interrupt generating or pure status input.

2.2.3 Input Line Specifications

- Each input line (PA0-7, PB0-7) has a low pass filter with a time constant of 10/20 ms;
- H1 - H4 have Schmidt triggers and option for lowpass;
- Input current at 24V is 5mA;
- High level (>16V) represents a "0" at the according PI/T port line;
- Low level (<10V) represents a "1" at the according port line.

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2.3 Timer Operation

The MC68230 timer can provide several facilities required by the MC68000 operating systems. It can generate periodic interrupts, or a single interrupt after a programmed time period. Also, it can be used for elapsed time measurement or as a device watchdog.

The PI/T timer contains a 24-bit synchronous down counter that is loaded from three 8-bit counter preload registers. The 24-bit counter may be clocked by the output of a 5-bit prescaler. If the prescaler is used, it may be clocked by the system clock (CLK pin). The counter signals the occurance of an event primarily through zero detection (a zero is detected when the counter of the 24-bit timer is equal to zero). This sets the Zero Detection Status (ZDS) bit in the timer status register. It may be checked by the processor or may be used to generate a timer interrupt. The ZDS bit can be reset by writing a one (1) to the timer status register in that bit position, independent of timer operation.

The general operation of the timer is flexible and easily programmable. The timer is fully configured and controlled by programming the 8-bit timer control register. It controls:

1) the choice between the port C operation and timer operation of three timer pins;
2) whether the counter is loaded from the counter preload register or rolls over when zero detect is reached;
3) the clock input;
4) whether the prescaler is used, and
5) whether the timer is enabled.

2.3.1 Run/Halt Definition

The overall operation of the timer is described in terms of the run or halt states. The control of the current state is determined by programming the timer control register.

When in the halt state, all of the following takes place:

1) The prior contents of the counter is not altered and is reliably readable via the count registers.
2) The prescaler is forced to $1F, whether or not it is used.
3) The ZDS status bit is forced to zero, regardless of the possible zero contents of the 24-bit counter.

The run state is characterized by:

1) The counter is clocked by the source programmed in the timer control register.
2) The counter is not readily readable.
3) The prescaler is allowed to decrement if programmed for use.
4) The ZDS status bit is set when the 24-bit counter changes from $000001 to $000000.

Note

The TIN (external timer input) cannot be used.

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2.4 Logic Interface

An important task performed by the logic interface is the generation of an ID byte. This built-in test feature allows an interrogation of the VMOD-2/IMOD, supplying an ID for each of the fitted piggybacks. If this is integrated into the application software, it can be used to check that any given tasks are valid for the fitted piggyback. Offsets $7F (for location A) and $FF (for location B), allow a software check of which piggybacks are fitted.

The PB-DIN3 has a "$F3" Byte.

Other ID Bytes are:

$EE	*PB-BIT*	*BITBUS communications controller*
$EF	*PB-DIO4*	*Digital I/O piggyback (high voltage)*
$F0	*PB-CNT*	*Counter piggyback*
$F1	*PB-DAC/2*	*D to A converter piggyback*
$EA	*PB-DAC3*	*D to A output piggyback*
$F2	*PB-DIO*	*Digital I/O piggyback*
$F3	*PB-DIN/3*	*Digital input piggyback*
$F4	*PB-ADC/2*	*A to D converter piggyback*
$EB	*PB-ADC3*	*A to D input piggyback*
$F5	*PB-CIO/2*	*Counter/I/O piggyback*
$F7	*PB-SIO4*	*Quad serial piggyback RS232*
$E7	*PB-SIO4A*	*Quad serial piggyback RS422/RS485*
$F8	*PB-DOUT*	*12 channel high voltage digital output*
$ED	*PB-DOUT2*	*16 channel high voltage digital output*
$F9	*PB-DIN2*	*Digital input piggyback*
$FB	*PB-DIO-2*	*Digital I/O piggyback*
$FC	*PB-REL*	*Relay piggyback*
$FD	*PB-DIO-3*	*Digital I/O piggyback*
$FE	*PB-STP*	*Stepper motor controller piggyback*

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3. CONFIGURATION

There are no jumpers on the PB-DIN3 that need to be configured.

3.1 VMOD-2/IMOD Jumper Configuration

In order for the PB-DIN3 to be put into use on either the VMOD-2 or IMOD boards, the IRQ and Base Address jumper settings on these boards must be correctly configured.

For more details on these jumper configurations, please refer to the VMOD-2 or IMOD user manuals.

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Note

For further information on programming the PB-DIN3 please refer to the *MC68230 Data Sheet.*

4.1.1 Port General Control Register ($01)

This register sets the operating mode of the PI/T and controls the handshake pins H1-H4 (port IRQ or input).

Register Description

Bits	Setting	Function		
7	0 0	Mode 0	Unidirectional 8-bit mode	
6	0 1	Mode 1	Unidirectional 16-bit mode	
	1 0	*Mode 2*	*Bidirectional 8-bit mode*	*Not intended for PB-DIN3*
	1 1	*Mode 3*	*Bidirectional 16-bit mode*	*Not intended for PB-DIN3*
5	0	H3 and H4 disabled		
	1	H3 and H4 enabled		
4	0	H1 and H2 disabled		
	1	H1 and H2 enabled		
3	x	H4		
2	x	H3	Bit = 1: Rising Edge active	
1	x	H2	Bit = 0: Falling Edge active	
0	x	H1		

Note

After a RESET, all bits are returned to 0. This puts the PI/T into an input device mode on all ports.

Port Mode Control Summary

Mode 0 - Unidirectional 8-bit mode

Port A

Submode 00 Pin Definable Double Buffered Input or Single Buffered Output
- H1 Latches input data.
- H2 Status/interrupt generating input, general purpose output, or operation with H1 in the interlocked or pulsed handshake mode.

Submode 01 Pin Definable Double Buffered Output or Nonlatched Input
- H1 Indicates data received by peripheral.
- H2 Status/interrupt generating input, general purpose output, or operating with H1 in the interlocked or pulsed handshake protocols.

Submode 1x Pin Definable Single Buffered Output or Nonlatched Input
- H1 Status/interrupt generating input.
- H2 Status/interrupt generating input or general purpose output.

Port B

H3 and H4 Identical to port A, H1 and H2

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Mode 1 - Unidirectional 16-bit mode

Port A	Most significant data byte or nonlatched input or single buffered output.
Submode XX	*Not Used*
H1	Status/interrupt generating input.
H2	Status/interrupt generating input or general purpose output.
Port B	Least significant data byte
Submode x0	Pin Definable Double Buffered Input or Single Buffered Output
H3	Latches input data.
H4	Status/interrupt generating input, general purpose output, or operation with H3 in the interlocked or pulsed handshake protocols.
Submode x1	Pin Definable Double Buffered Output or Nonlatched Input
H3	Indicates data received by peripheral.
H4	Status/interrupt generating input, general purpose output, or operation with H3 in the interlocked or pulsed handshake protocols.

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4.1.2 Port Service Request Register ($03)

This register controls the double function on some of the PI/T interrupt priorities.

Register Description

Bits 7 6 5 4 3 2 1 0	Function
0 0 0 1 1	Fixed when port EOC IRQs are used
	Interrupt Priority
0 0 0	H1 > H2 > H3 > H4 **Default**
0 0 1	H2 > H1 > H3 > H4
0 1 0	H1 > H2 > H4 > H3
0 1 1	H2 > H1 > H4 > H3
1 0 0	H3 > H4 > H1 > H2
1 0 1	H3 > H4 > H2 > H1
1 1 0	H4 > H3 > H1 > H2
1 1 1	H4 > H3 > H2 > H1

Note

After a reset all bits are returned to zero.

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4.1.3 Port A and B Data Direction Registers (Port A $05, Port B $07)

This register describes the bit in the ports A and B as either input or output.

Register Description

Bits 7 6 5 4 3 2 1 0	Function
	Each bit represents an input line.
0 0 0 0 0 0 0 0	On the PB-DIN3 all lines are set to inputs

Note

After a reset all bits are returned to zero.

4.1.4 Port Interrupt Vector Register ($0B)

This register contain the interrupt vector numbers of the VMOD-2 interrupt handler. The upper six bits are programmable, the lower two bits are self-modifying.

Register Description

Bits 7 6 5 4 3 2 1 0	Function
	Interrupt Vectors
1 1 1 1 0 0	Example: $F0 - $F3
0 0	H1 IRQ
0 1	H2 IRQ
1 0	H3 IRQ
1 1	H4 IRQ

Note

After a reset this register contains $0F.

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4.1.5 Port A and B Control Registers (Port A $0D, Port B $0F)

These registers control the functions of ports A and B, and contain enable flags for port IRQ inputs H3 and H4.

The definition on the register bit functions depends on the mode of operation. For more information, please refer to the *MC68230 Data Sheet.*

4.1.6 Port A and B Data Registers (Port A $11, Port B $13)

These registers hold the data for the PI/T ports A and B.

4.1.7 Port Status Register ($1B)

With the approprate edge on pins H1 through H4 of the PI/T, internal flip-flops are set in the port status register. These flip-flops are identified by status bits H1S through H4S. The flip-flops can be returned to their original state by writing a 1 to the status bit.

Register Description

Bits 7 6 5 4 3 2 1 0	Function
x x x x	Current levels at H1-H4 pins
x x x x	H4S, H3S, H2S, H1S status pins

Note

After a reset all bits are returned to zero.

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4.1.8 Timer Control Register ($21)

This register controls all timer operations.

Register Description

Bits 7 6 5 4 3 2 1 0	Function
0 1 x	*Timer Output (Tout) Control* The Tout pin is a square wave output in run state, and moves the counter once for the passage of all zeros. In halt state, the Tout pin is set low.
0	*Zero Detect Control* After passage of all zeros in the first clock cycle, the contents of the Counter Preload Register are placed in the counter and decrementation begins.
x	Any setting.
0 0	*Clock Control* The timer's internal 8-bit prescaler is enabled. The 8 MHz onboard clock decrements the prescaler and the prescaler decrements the counter from $00 to $1F.
0 1	The Tin pin serves as a timer enable input for the timer enable flag (active high). The internal clock is used and the prescaler is enabled.
1 0	The counter is timed with the falling edge on the Tin pin. The prescaler is enabled.
1 1	The counter is timed with the falling edge on the Tin pin. The prescaler is disabled.
0	*Timer Enable* Disabled. Timer in halt state.
1	Enabled. Timer in run state.

Note

After a reset all bits are returned to zero.

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4.1.9 Timer Interrupt Vector Register ($23)

This register contains the timer interrupt vector number. After reset, this register contains $0F.

4.1.10 Counter Preload Registers ($27 High, $29 Middle, $2B Low)

This group of three 8-bit registers contains the beginning timer value which is carried over to the timer count register after timer enable or zero detect impulse. After reset, all bits remain unaffected.

4.1.11 Timer Count Registers ($2F High, $31 Middle, $33 Low)

The current timer count is contained in this group of registers. After reset, all bits remain unaffected.

4.1.12 Timer Status Register ($35)

Bit 0 of this register contains information regarding zero detect status. This bit is set when the counter moves from $000001 to $000000 and is reset through a direct reset, or when the timer is placed in a halt state. After reset, all bits are returned to zero.

4.1.13 ID Register ($7F)

This register contains the ID byte, allowing automatic recognition of the piggyback fitted to the VMOD-2 or IMOD. This feature is particulary useful in a system with several piggybacks fitted. The ID byte is read using a byte read access. After reset, all bits remain unaffected.

PD-DIN3 ID byte = $F3

For more information on the ID byte, please see the ID Byte section in the Functional Description chapter.

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4.2 Address Map Overview

Register	Address Offset	Register Select Bits	Accessible	Affected by Reset	Affected by Read Cycle
Port General Control Register (PGCR)	$01	0 0 0 0 0	R/W	Yes	No
Port Service Request Register (PSRR)	$03	0 0 0 0 1	R/W	Yes	No
Port A Data Direction Register (PADDR)	$05	0 0 0 1 0	R/W	Yes	No
Port B Data Direction Register (PBDDR)	$07	0 0 0 1 1	R/W	Yes	No
Port Interrupt Vector Register (PIVR)	$0B	0 0 1 0 1	R/W	Yes	No
Port A Control Register (PACR)	$0D	0 0 1 1 0	R/W	Yes	No
Port B Control Register (PBCR)	$0F	0 0 1 1 1	R/W	Yes	No
Port A Data Register (PADR)	$11	0 1 0 0 0	R/W	No	* *
Port B Data Register (PBDR)	$13	0 1 0 0 1	R/W	No	* *
Port A Alternate Register (PAAR)	$15	0 1 0 1 0	R	No	No
Port B Alternate Register (PBAR)	$17	0 1 0 1 1	R	No	No
Port Status Register (PSR)	$1B	0 1 1 0 1	R/W*	Yes	No
Timer Control Register (TCR)	$21	1 0 0 0 0	R/W	Yes	No
Timer Interrupt Vector Register (TIVR)	$23	1 0 0 0 1	R/W	Yes	No
Counter Preload Register High (CPRH)	$27	1 0 0 1 1	R/W	No	No
Counter Preload Register Middle (CPRM)	$29	1 0 1 0 0	R/W	No	No
Counter Preload Register Low (CPRL)	$2B	1 0 1 0 1	R/W	No	No
Count Register High (CNTRH)	$2F	1 0 1 1 1	R	No	No
Count Register Middle (CNTRM)	$31	1 1 0 0 0	R	No	No
Count Register Low (CNTRL)	$33	1 1 0 0 1	R	No	No
Timer Status Register (TSR)	$35	1 1 0 1 0	R/W*	Yes	No

* A write to this register may perform a special status resetting operation

* * Mode dependent

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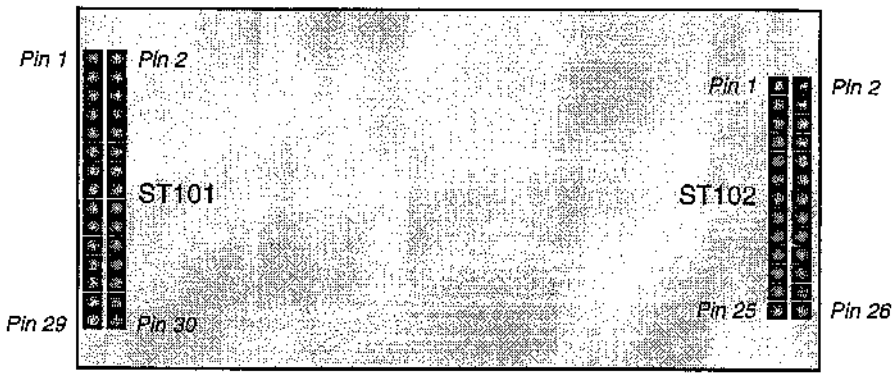


5. PINOUTS

The PB-DIN3 has two sets of connectors. ST101 is the rearmost row of 30 pins. At the front end of the piggyback there is ST102 with 26 pins.

5.1 Main Board

Figure 5.1.0.1: Board Connector Overview



5.1.1 ST101 Connector

The ST101 connector is fitted into the socket row BU1A or BU1B on the IMOD and VMOD-2 (depending if there is one or two piggybacks to be fitted) to the VMEbus interface logic.

Pin#	Signal	Pin#	Signal
1	GND	2	+5V (Vcc)
3	+12V	4	-12V
5	R/W	6	CLK
7	RESET	8	UDTACK*
9	INTA*	10	CS*
11	INT	12	N/C
13	ID7	14	IDS0*
15	ID6	16	IAS*
17	ID5	18	IA6
19	ID4	20	IA5
21	ID3	22	IA4
23	ID2	24	IA3
25	ID1	26	IA2
27	ID0	28	IA1
29	GND	30	+5V (Vcc)

* *Active Signal Low*

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5.1.2 ST102 Connector

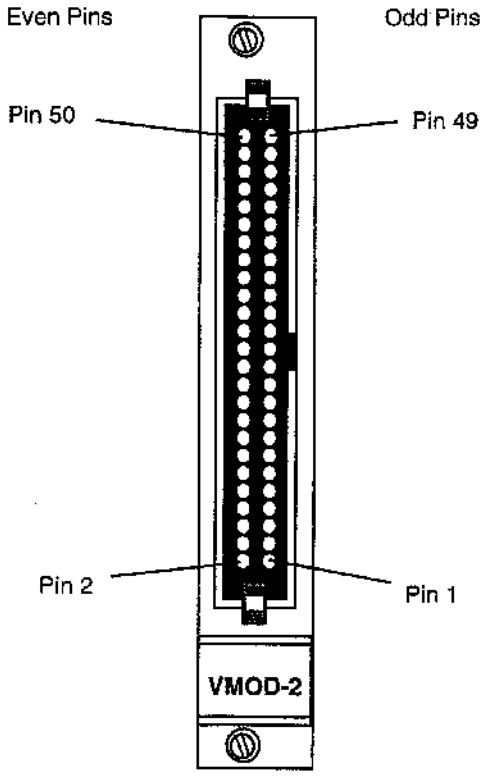
The ST102 connector is fitted into the socket row BU2A or BU2B on the IMOD and VMOD-2 (depending if there is one or two piggybacks to be fitted), directly to half of the 50-way VMOD-2 front panel connector, and ultimately to the user's external interfaces.

Pin#	Signal	Pin#	Signal
1	GNDA	2	GNDA
3	PA0	4	PB0
5	PA1	6	PB1
7	PA2	8	PB2
9	PA3	10	PB3
11	PA4	12	PB4
13	PA5	14	PB5
15	PA6	16	PB6
17	PA7	18	PB7
19	H1	20	H3
21	H2	22	H4
23	GND	24	GND
25	N/C	26	N/C

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5.2 VMOD-2/IMOD Front Panel

Figure 5.2.0.1: VMOD-2/IMOD Front Panel



Piggyback A

Pin #	Signal	Pin #	Signal
50	GNDA	49	N/C
48	PA0	47	PB0
46	PA1	45	PB1
44	PA2	43	PB2
42	PA3	41	PB3
40	PA4	39	PB4
38	PA5	37	PB5
36	PA6	35	PB6
34	PA7	33	PB7
32	H1	31	H3
30	H2	29	H4
28	GNDB	27	GNDB
26	Ext. Reset GND	25	Ext. Reset Vcc

Piggyback B

Pin #	Signal	Pin #	Signal
24	GNDA	23	N/C
22	PA0 19	21	PB0 18
20	PA1 17	19	PB1 16
18	PA2 15	17	PB2 14
16	PA3 13	15	PB3 12
14	PA4 11	13	PB4 10
12	PA5 9	11	PB5 8
10	PA6 7	9	PB6 6
8	PA7 5	7	PB7 4
6	H1 3	5	H3 2
4	H2 1	3	H4
2	GNDB	1	GNDB

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The relevant half of the VMOD-2 and IMOD front panel 50-way connector (pins 1..24 for lower position and pins 27..50 for upper) assumes the relationship of PB-ADC3 signals and its ST102.

An optional 50-way header behind the front panel connector has an identical pin-out to the front panel connector. It is provided for applications where the flat band cable is to be routed internally, or where an alternative front panel is to be fitted and used. In some cases, cables can be routed through the systems interior i.e. to the back panel (from this optional connector) and some from the external connector on the front panel. In doing so take care not to exceed the fan out ability of the piggyback's driver circuits.

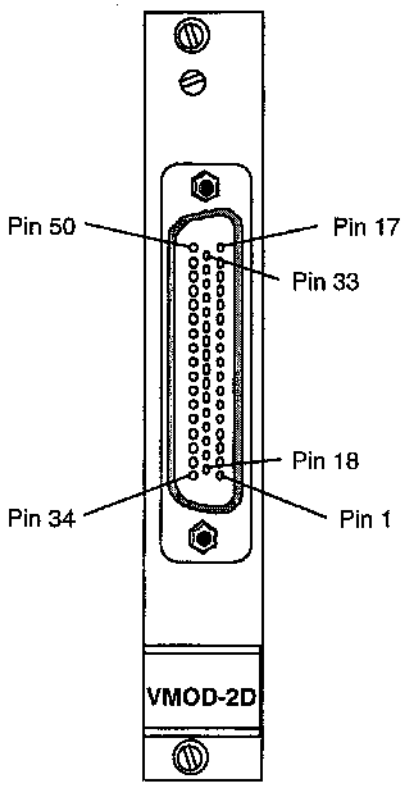
Note

With systems that have more than one of this type of connector , or which use several VMOD-2 or IMODs with various piggybacks, it is advisable to put a drop of paint on the back of the mating connector and on the front panel of the VMOD-2 or IMOD, for correct connection. The connector splits virtually in half (pins 1-24 and 27-50) for connection to the rear piggyback location.

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5.3 VMOD-2D Front Panel

Figure 5.3.0.1: VMOD-2D Front Panel



Piggyback A

Pin #	Signal	Pin #	Signal	Pin #	Signal
50	GNDA	33	PA0	17	N/C
49	PB0	32	PB1	16	PA1
48	PA2	31	PA3	15	PB2
47	PB3	30	PB4	14	PA4
46	PA5	29	PA6	13	PB5
45	PB6	28	PB7	12	PA7
44	H1	27	H2	11	H3
43	H4	26	GNDB	10	GNDB
42	Ext. Reset GND			9	Ext. Reset Vcc

Piggyback B

Pin #	Signal	Pin #	Signal	Pin #	Signal
		25	GNDA		
41	N/C	24	PB0	8	PA0
40	PA1	23	PA2	7	PB1
39	PB2	22	PB3	6	PA3
38	PA4	21	PA5	5	PB4
37	PB5	20	PB6	4	PA6
36	PA7	19	H1	3	PB7
35	H3	18	H4	2	H2
34	GNDB			1	GNDB

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5.4 VMOD-2 / VMOD-2D Pinout Relationship

Piggyback A

Signal	VMOD-2 Pin #	VMOD-2D Pin #	Signal	VMOD-2 Pin #	VMOD-2D Pin #
GNDA	50	50	N/C	49	17
PA0	48	33	PB0	47	49
PA1	46	16	PB1	45	32
PA2	44	48	PB2	43	15
PA3	42	31	PB3	41	47
PA4	40	14	PB4	39	30
PA5	38	46	PB5	37	13
PA6	36	29	PB6	35	45
PA7	34	12	PB7	33	28
H1	32	44	H3	31	11
H1	30	27	H4	29	43
GNDB	28	10	GNDB	27	26

Signal	VMOD-2 Pin #	VMOD-2D Pin #	Signal	VMOD-2 Pin #	VMOD-2D Pin #
Ext. Reset GND	26	42	Ext Reset Vcc	25	9

Piggyback B

Signal	VMOD-2 Pin #	VMOD-2D Pin #	Signal	VMOD-2 Pin #	VMOD-2D Pin #
GNDA	24	25	N/C	23	41
PA0	22	8	PB0	21	24
PA1	20	40	PB1	19	7
PA2	18	23	PB2	17	39
PA3	16	6	PB3	15	22
PA4	14	38	PB4	13	5
PA5	12	21	PB5	11	37
PA6	10	4	PB6	9	20
PA7	8	36	PB7	7	3
H1	6	19	H3	5	35
H2	4	2	H4	3	18
GNDB	2	34	GNDB	1	1

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6. INSTALLATION

6.1 VMEbus Connection

Caution!

Before installing or removing any VMEbus boards, always turn off the power to the bus and any external peripherals.

Inserting or removing modules, while the power is on, could result in damage to the VME module or peripherals interface.

Please refer to VMOD-2/IMOD user's manual for details on installing or removing.

Note

The VMEbus backplane uses automatic daisy-chaining (no BG/IACK jumpers), therefore does not need to be configured by the user.

For users with VBP backplanes, please refer to the *VBP Users Manual* for configuration information.

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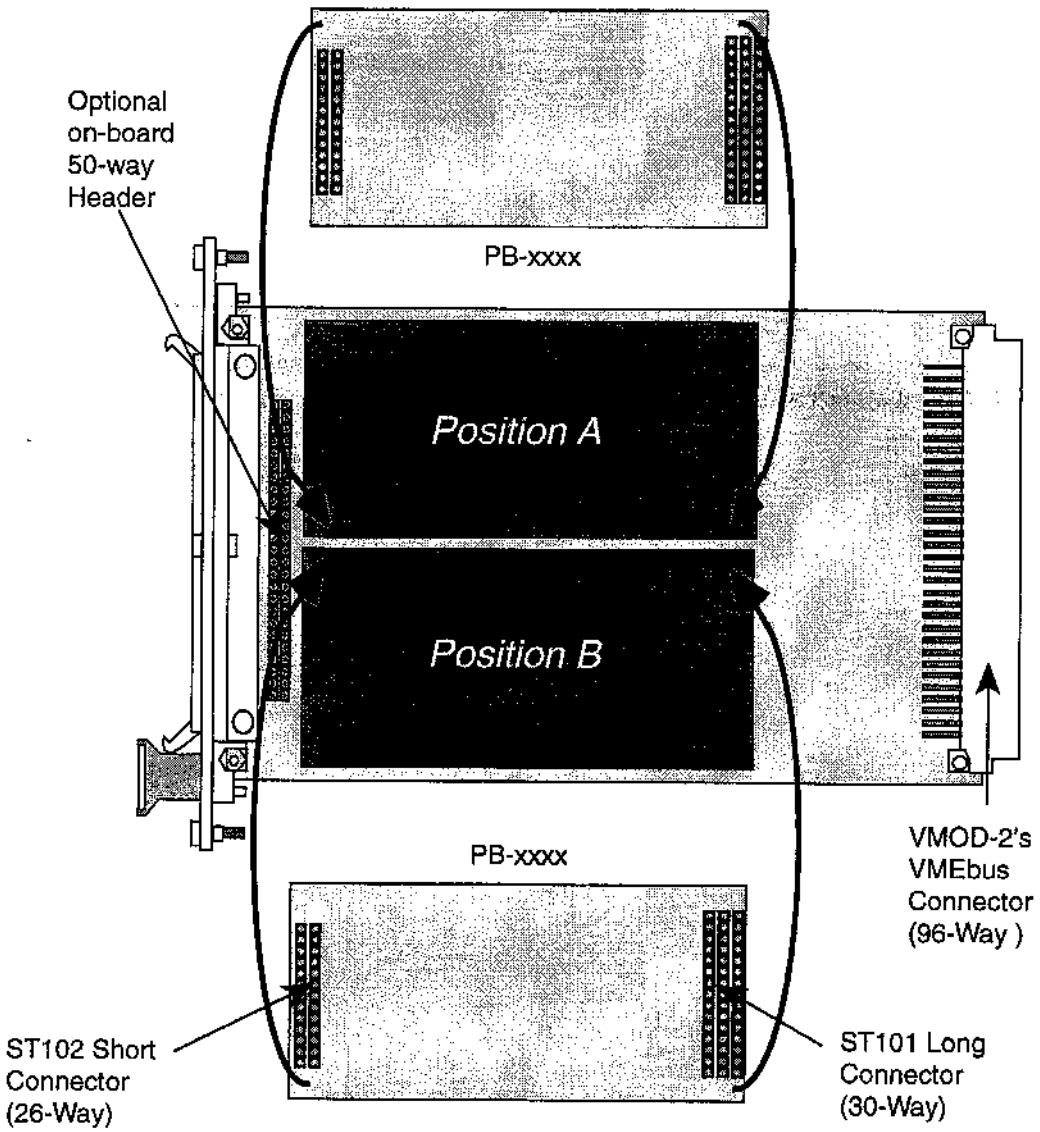
6.2 Installing the PB-DIN3

The PB-DIN3 may be plugged into any free piggyback position (A or B) on the VMOD-2 or IMOD. Please ensure the correct location before fitting.

Note

1. One connector on the PB-DIN3 has fewer pins than the other.
2. ST101 has two-rows which are to fit the front two-rows of the VMOD-2 amd IMOD three-row interface socket. Take care to ensure that the piggyback is in its correct position.

Figure 6.2.0.1: PB-DIN3 Installation Overview



Mechanical fastening and support is provided by the two interface connectors. In addition, the piggyback can be attached to the motherboard by screws and stand-off pillars at the front end of the piggyback, and at the corresponding location on the VMOD-2 and IMOD at the two holes provided for this purpose.

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6.3 General Notes for Using the System

Having designed a system, it is necessary to keep it in good working order. The three biggest risks to the system occur when:

- Connecting peripherals, disk-drives, printers, terminals and external power sources;
- Adding or changing modules, address settings and locations, etc;
- Becoming complacent and not referring to the manuals when altering or adding modules.

These risks can be reduced by:

- Checking the electrical compatibility of all devices to be connected;
- Ensuring that they are powered from the same mains supply branch (phase) and grounded to the same reference point;
- Shutting down all power before making or breaking any connections to modules or attachments to the system, including power to the peripherals;
- Observing sensible static protection procedures before handling any modules, piggybacks or memory IC's;
- Keeping all manuals available by the system and refer to them when required.

Some tips are:-

PEPCards are not over sensitive to static, but it is generally advisable to observe normal antistatic procedures.

When configuring the module, it should not be taken out of the original packing unless necessary. The clear packs can be opened and the jumpers set, piggybacks added, etc. without removing the card. This prevents inadvertent shorting of any on-board devices.

When inserting modules into a system, the power should be turned off and the mains lead not removed! The ground wire prevents the rack floating with dangerous static voltages, which could destroy circuits on the module being inserted.

The front panel of the module and the shell of the connector should be touched to any part of the rack before fitting. This discharges any static from the user.

Modules should not be pulled straight out of a rack and the back of the front panel checked to see if there are cables to unplug (such as the VSBC-1's 40-pin parallel on-board headers). Any leads should be disconnected from a module before unscrewing the front panel and removing from the rack. It should be ensured that, when fitted, these cables have enough play to allow the modules to be removed far enough to detach these cables. Modules should be put into the rack before connecting any front-panel connectors.

The "pulled" jumpers should be parked on to one of the pins they would normally bridge, so they can be quickly replaced.

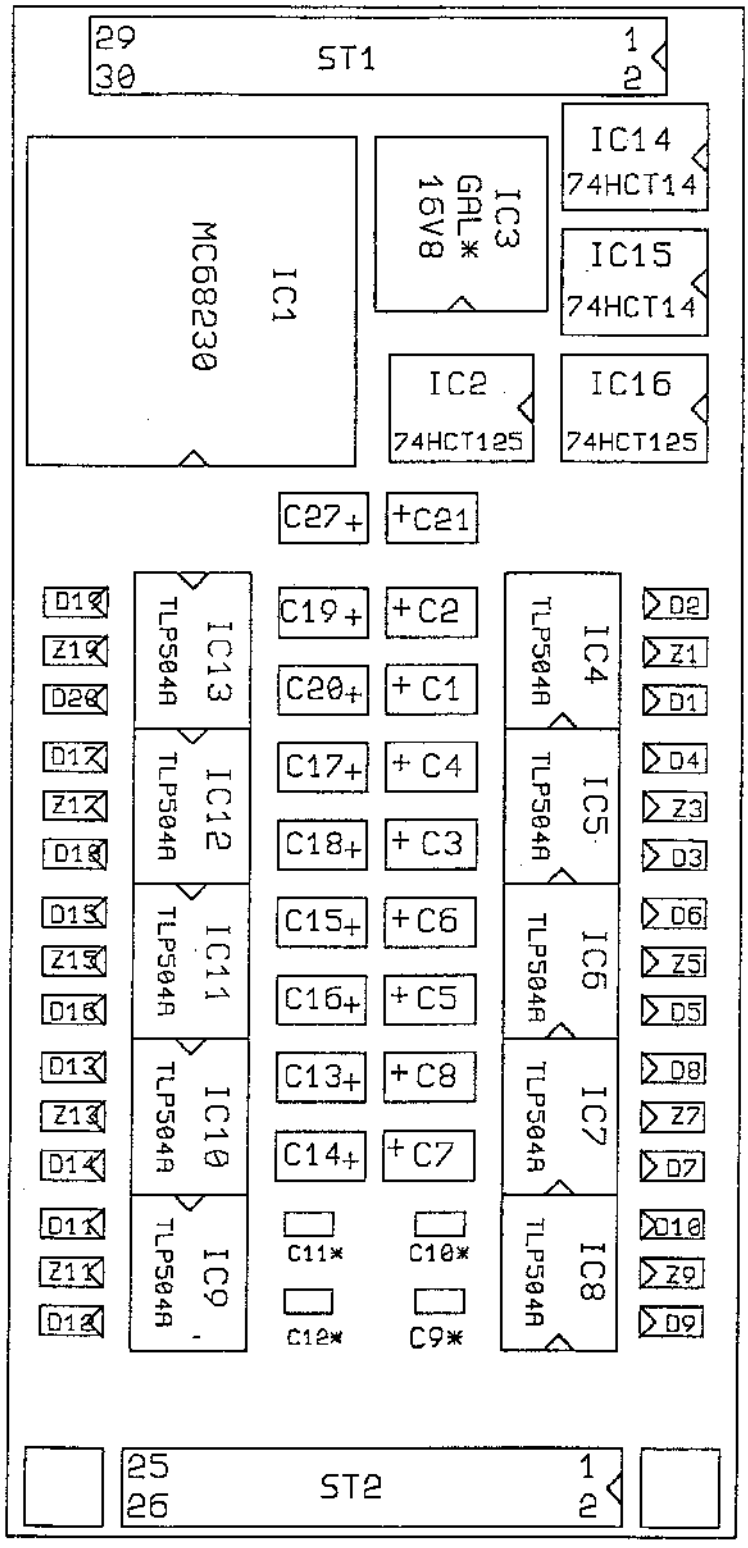
It should be remembered to check the mains input voltage selector switch before installing or using any PSU!

A record should be kept of settings and a copy forwarded with any board returned to PEP for failure analysis.

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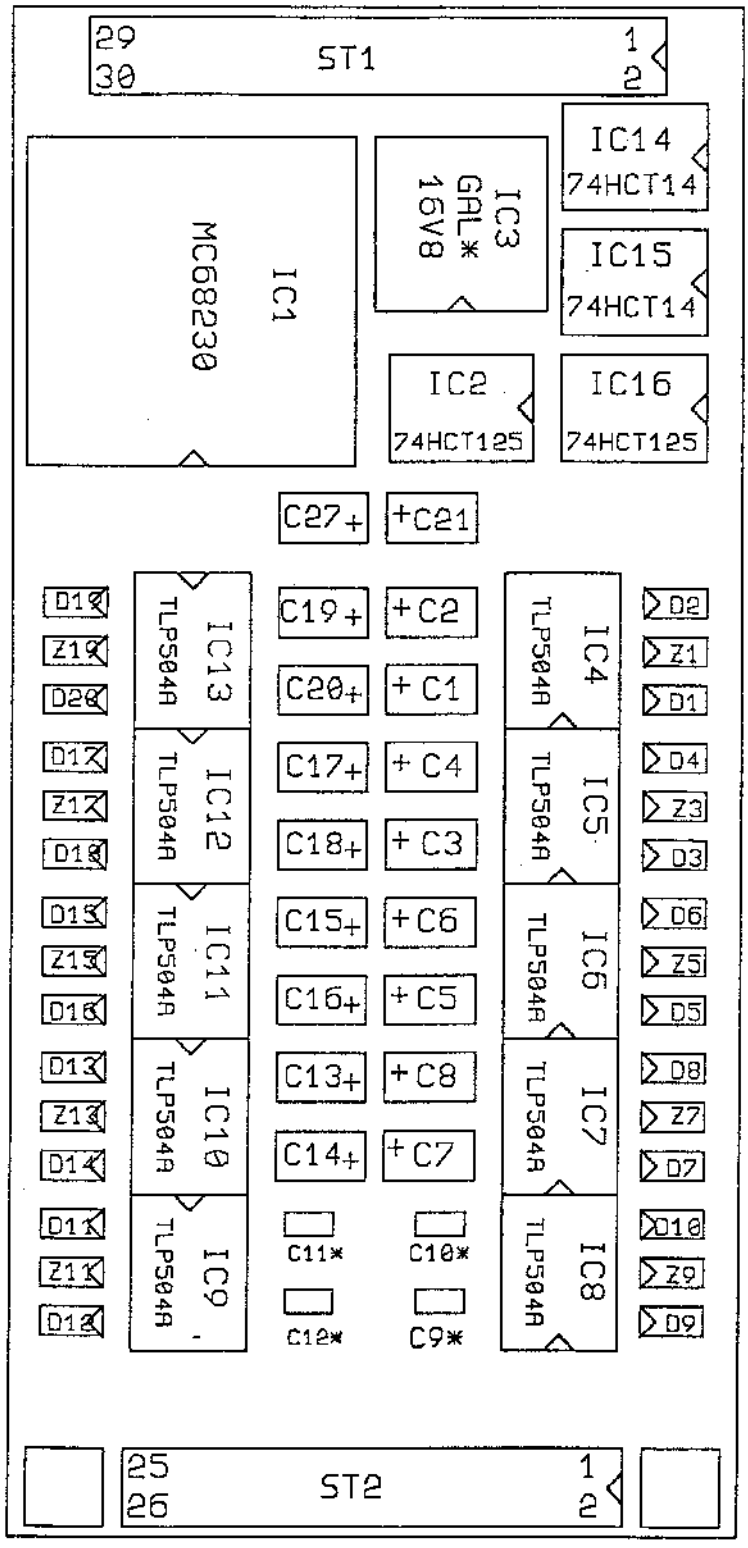


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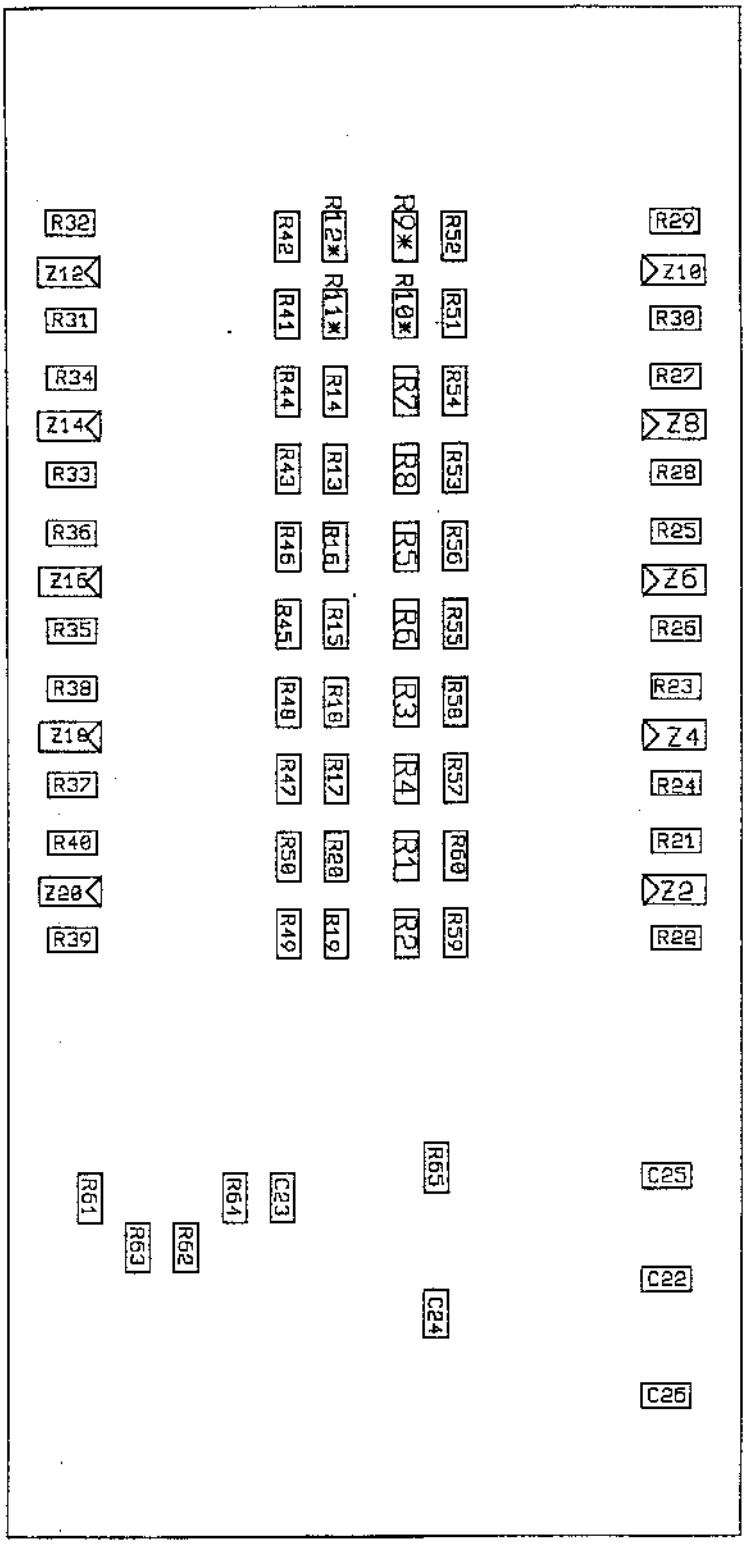


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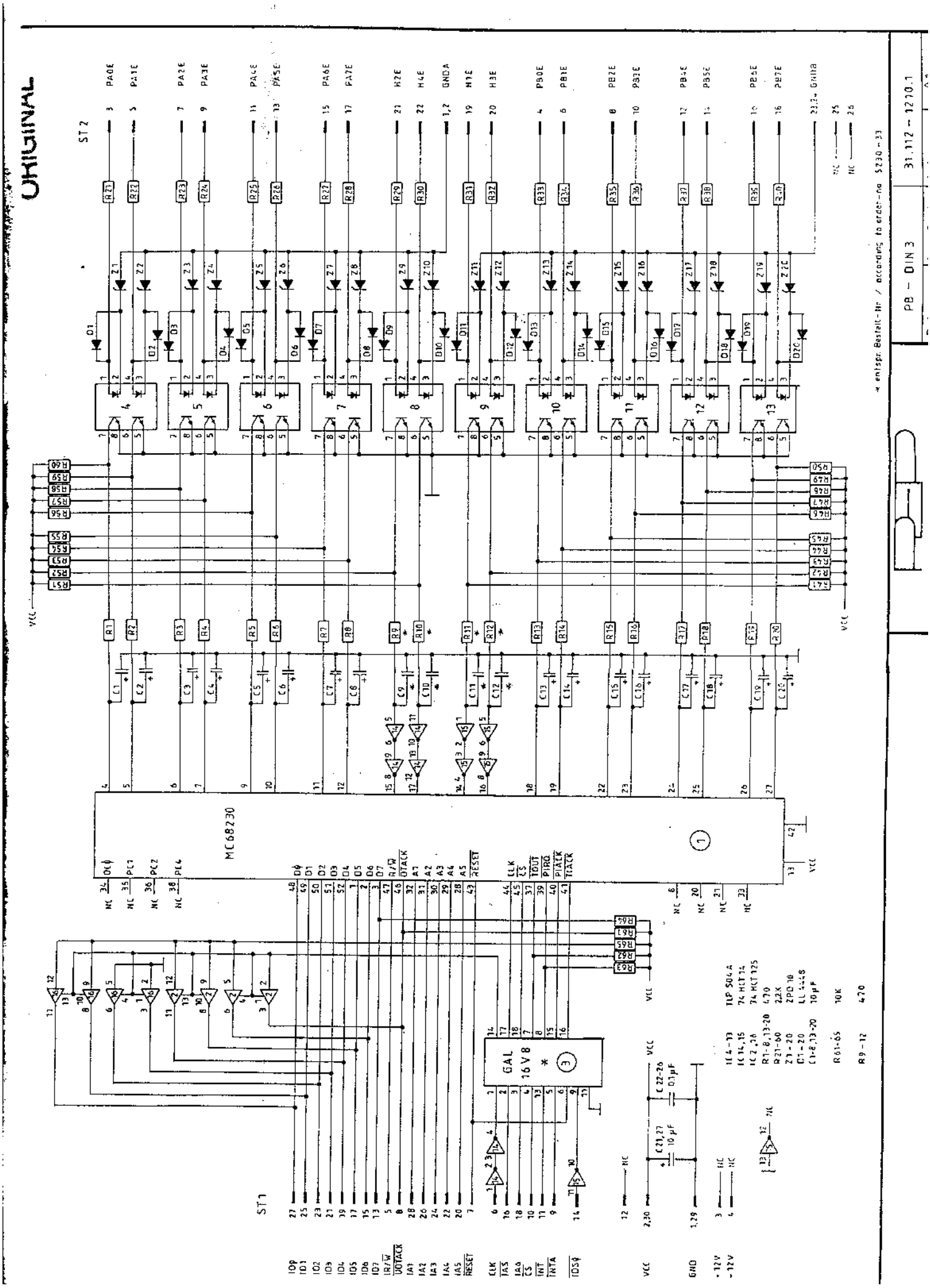


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