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kontron

VMEM-S2

8MB Static Memory / Feprom

for the VMEbus

Manual ID 02253, Rev. Index 0110
Nov 98

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Preface

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Revision History

Revision History			
Manual/Product Title:	**VMEM-S2**		
Manual ID Number:	**02253**		
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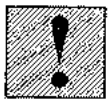
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- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or tracks on the board.

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- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please, follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the following page of this manual.

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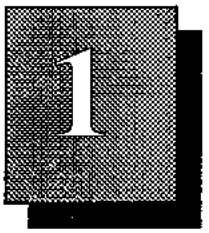
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1. INTRODUCTION

1.1 Product Overview

The VMEM-S2 is a static memory module with a capacity of up to 8MByte. The board has two memory banks, each with 32-pin sockets for 32-pin DIL ICs. It supports the new generation of memory chips such as the 1MBit (128K*8), 2MBit (256K*8) and 4MBit (512K*8). It can be configured with either of the following:

- static CMOS RAM (SRAM)
- ROM (EPROM, PROM)
- FLASH memory
- mixed RAM/ROM
- mixed RAM/FLASH
- mixed ROM/FLASH

Data retention is provided for by an on-board battery backup (lithium cell) and battery switchover circuitry. Each memory bank has separate battery backup selection, allowing the RAM to be buffered even in RAM/ROM configurations.

The VMEM-S2 supports the Intel™ type of FLASH memories and compatible devices. The board offers the capacity of programming and erasing FLASH memory, this being enabled and disabled by software with the status being displayed by LED on the front panel. Additionally the program and erase mode can be permanently disabled via a front panel switch.

1.2 Ordering Information

Name	Description	Order-Number
VMEM-S2	Static memory module without memory chips, on-board Lithium battery	5020-000
VMEM-S2	Same as above with 2MByte SRAM with 16(128K*8)	5020-102
VMEM-S2	Same as above with 8MByte SRAM with 16(512K*8)	5020-106
VMEM-S2	Same as above with 2MByte FLASH Eprom with 16(128K*8)	5020-202
VMEM-S2	Same as above with 1MByte SRAM with 8 128K*8 and 1MByte Flash Eprom with 8(128K*8)	5020-411

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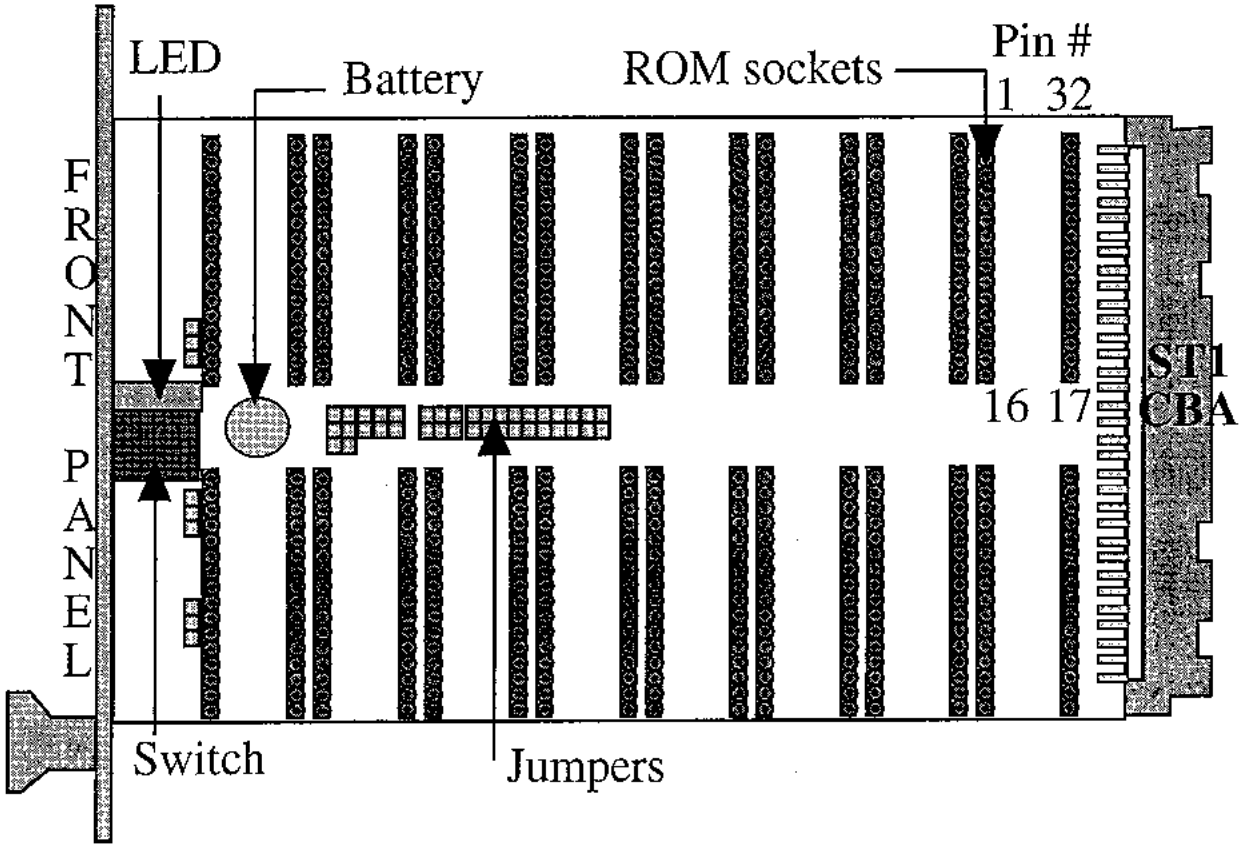
1.3 Specifications

Storage capacity	2MByte/4MByte/8MByte
Number of sockets	16x32-pin sockets
Devices supported	ROM 128K*8/256K*8/512K*8 RAM 128K*8/512K*8 FLASH 128K*8/256K*8/512K*8
Access time	selected by jumper, each memory bank separately <= 100ns <= 200ns
Address modifier	selected by jumper supervisory prog/data (3E/3D) supervisory/non-priv. prog/data (3E/3D/3A/39) user defined 1 (1F-18) user defined 2 (17-10) (supervisory/non-priv. short I/O (2D, 29) FLASH mode)
Battery backup (RAM)	jumper selectable via on-board Lithium cell or VMEbus 5V STDBY line
Power requirements	w/o memory chips typ. 220mA/5V
Temperature range	0 to +70°C operating -55 to +85°C storage
VMEbus interface	SLAVE (A24:D16)

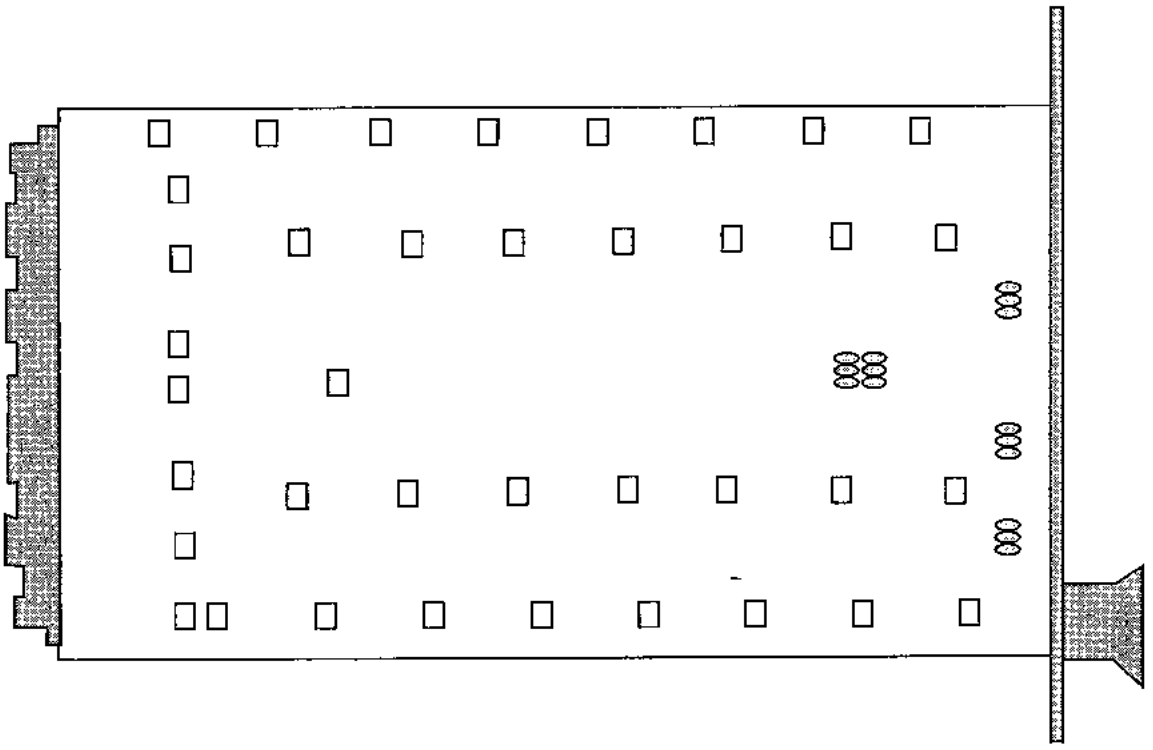
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1.4 Board Overview

Component side



Solder side



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1.5 Features

- Large memory support
- On-board battery backup
- Flash memory support
- RAM or ROM or mixed RAM/ROM

1.6 Typical Applications

1.7 Glossary of Terms

RAM	Random Access Memory
ROM	Read Only Memory
EPROM	Electrically Programmable Read Only Memory (can be erased by Ultra Violet light)
FLASH memory	a memory chip that is electronically programmable and erasable at chip or page level
EEPROM	Electrically Erasable Programmable Read Only Memory

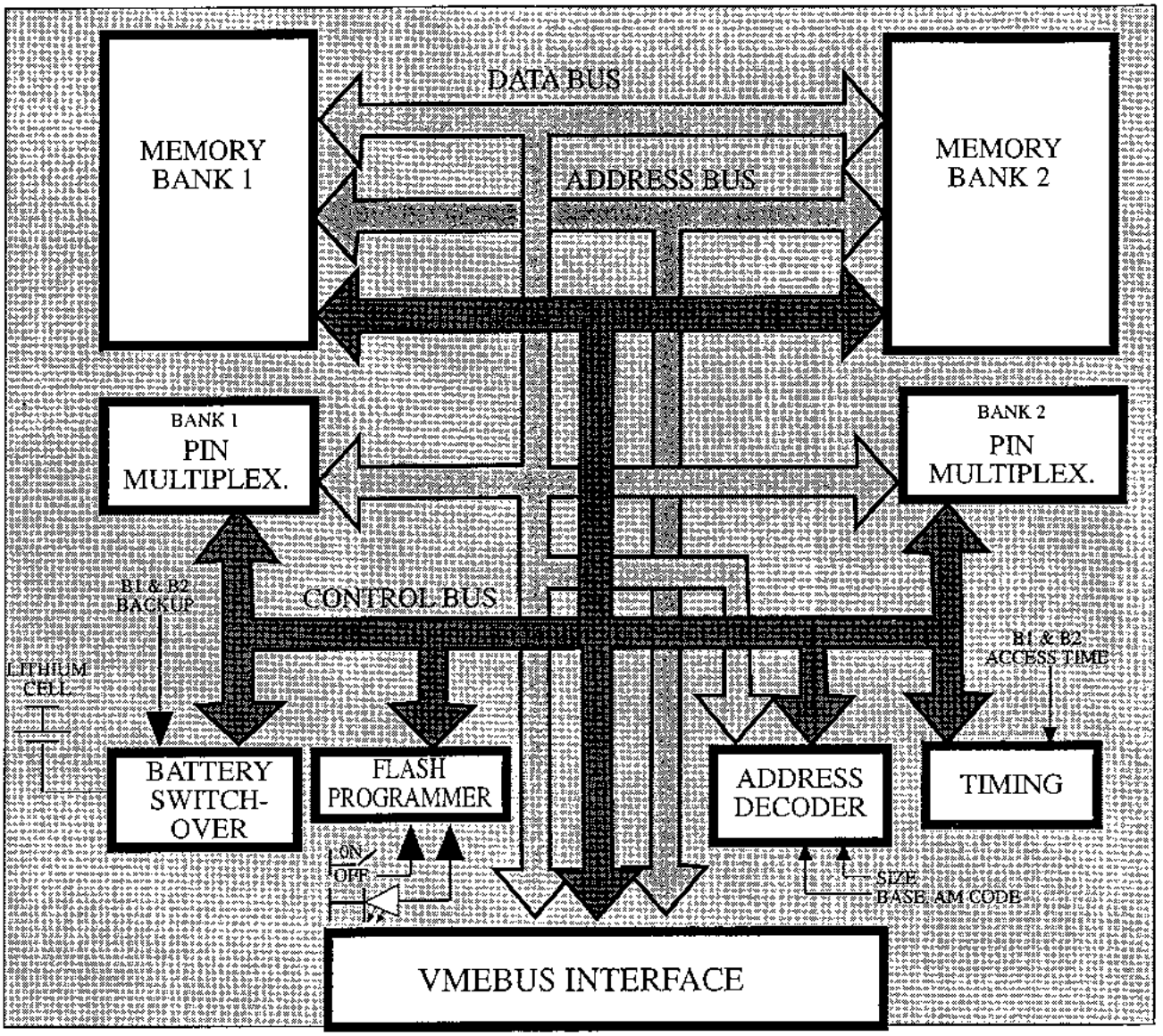
1.8 Related Publications

For more information please consult :

VMEbus Specifications C.1
AMD™ AM28F010-150 datasheet
INTEL™ P28F010-150 datasheet
CATALYST™ CAT28F010P-15 datasheet

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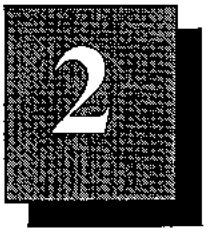
1.9 Block Diagram



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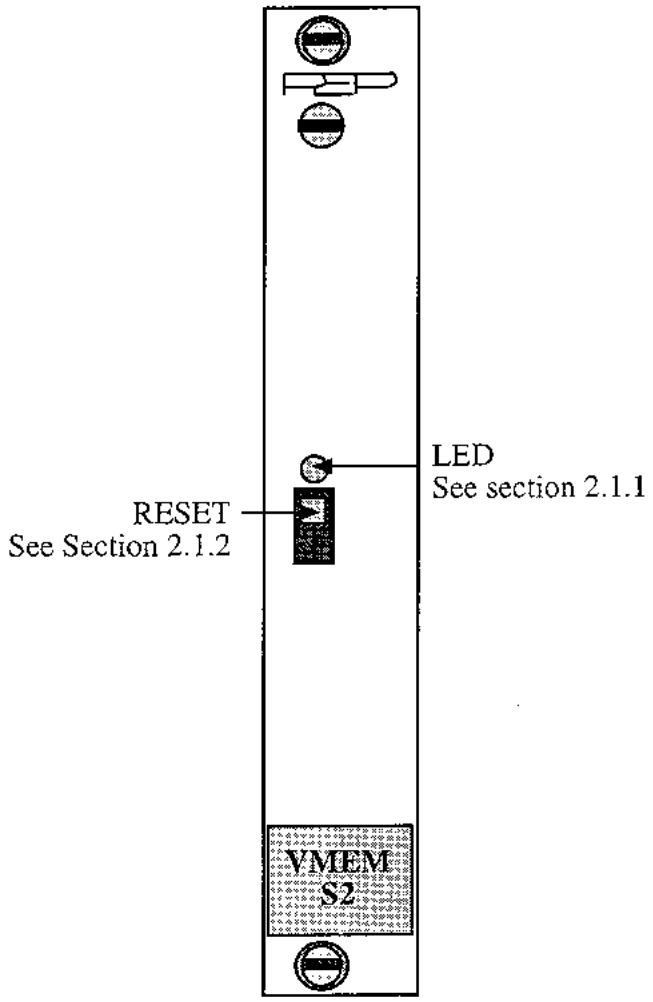
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2. FUNCTIONAL DESCRIPTION

Figure 2.0.0.1 Front Panel



2.1 Front Panel Functions

2.1.1 LED

This displays the status of VPP.

LED ON	VPP enabled or RAM write protection OFF
LED OFF	VPP disabled or RAM write protection is ON, default after a RESET

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2.1.2 RESET Front Panel Switch

This switch closes or opens the VPP path to the chips. The programming mode of the FLASH memories is either enabled or disabled. The priority is higher than that of the software controlled register. The switch can serve as a general overwrite protection for FLASH memories.

Switch UP	VPP disabled
Switch DOWN	VPP enabled

2.2 Memory Banks

The VMEM-S2 is divided into two memory banks.

Bank 1	IC32, 33, 34, 35, 40, 41, 42 and 43.
Bank 2	IC36, 37, 38, 39, 44, 45, 46 and 47.

These banks can be configured with either RAM or ROM as well as mixed RAM/ROM, building an address map with a volume of either 2, 4 or 8MByte.

2.2.1 Non-Mixed Configurations

Bank 1	Chip size	Bank 2	Chip size	Memory volume
(see 3.7)		(see 3.9)		
RAM	128K*8	RAM	128K*8	2 MByte
RAM	512K*8	RAM	512K*8	8 MByte
EPROM	128K*8	EPROM	128K*8	2 MByte
EPROM	256K*8	EPROM	256K*8	4 MByte
EPROM	512K*8	EPROM	512K*8	8 MByte
FEPROM	128K*8	FEPROM	128K*8	2 MByte
FEPROM	256K*8	FEPROM	256K*8	4 MByte
FEPROM	512K*8	FEPROM	512K*8	8 MByte

2.2.2 Mixed Configurations

In mixed configurations the location of RAM or ROM is not fixed and can be freely exchanged.

Bank 1	Chip size	Bank 2	Chip size	Memory volume
(see 3.7)		(see 3.9)		
RAM	128K*8	EPROM	128K*8	2 MByte
RAM	128K*8	FEPROM	128K*8	2 MByte
EPROM	128K*8	FEPROM	128K*8	2 MByte
RAM	512K*8	EPROM	512K*8	8 MByte
RAM	512K*8	EPROM	512K*8	8 MByte
EPROM	512K*8	FEPROM	512K*8	8 MByte
EPROM	256K*8	FEPROM	256K*8	4 MByte

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2.3 Addressing Memory

After the address modifier code, base address and address range has been set by jumper (see Chapter 3), the VMEM-S2 memory is contiguous starting with the corresponding VME address.

2.3.1 Base Address

The memory's base address (see Section 3.6) depends on the VMEM-S2 address range:

2MByte memory	base address selected in 8 steps in 2MByte steps;
4MByte memory	base address aelected in 4 steps in 4MByte steps;
8MByte memory	base address selected in 2 steps in 8MByte steps.

In addition to the memory base address there is a second base address for the on-board FLASH programming circuitry for controlling the program/erase mode. The address occupies 256Bytes within the VMEbus short I/O address range. It can be selected by jumper in 4KByte stages. (See Sections 2.4 and 3.3)

2.3.2 Address Modifier

One of the four 16MByte windows where the VMEM-S2 is located can be selected by jumper (see Section 3.4).
The four windows are:

1.	Supervisory program/data	(3E/3D)
2.	Supervisory/non-privileged program/data	(3E/3D/3A/39)
3.	User defined 1	(1F-18)
4.	User defined 2	(17-10)

2.4 Special Purposes Registers (SPR)

The VMEM-S2 has two special purpose registers with the following functions:

1. Switch FLASH programming voltage V_{PP} ON/OFF;
2. Switch RAM write protection ON/OFF;
3. Jumper readback for automatic setting verification.

The registers' base address can be selected in 4 steps by jumper. There are four different ranges (4KByte blocks) for these functions in the VME short I/O address range (see Section 3.3).

2.4.1 V_{PP} ON/OFF

The status of the V_{PP}_ON/OFF registers is displayed on the front panel LED (see 2.1.1). Jumper B0 must be set.

V_{PP}_ON base + $1	write only access byte only access data any setting during write switch-on time V_{PP} (12V) max. 20ms
V_{PP}_OFF base + $0	read/write access byte/word access data any setting during write switch-off time V_{PP} (12V) max. 20ms (jumper readback)

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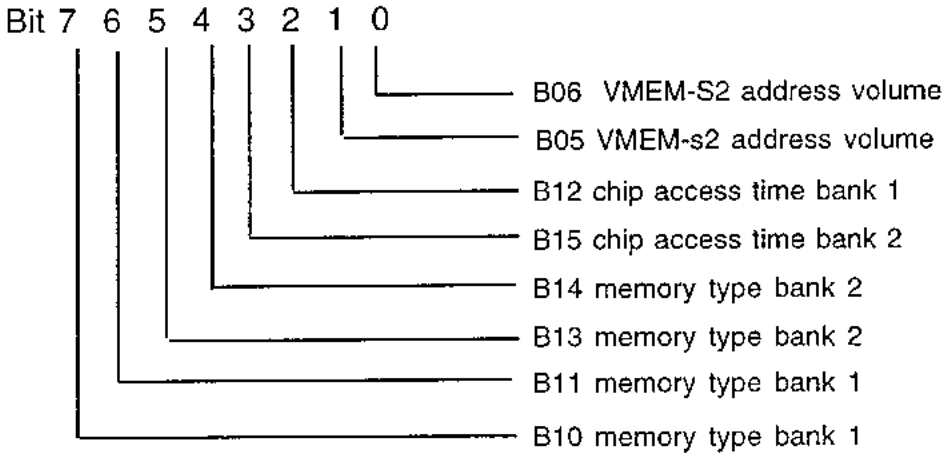
2.4.2 RAM Write Protection ON/OFF

The register has a double function when the VMEM-S2 is configured for RAM on **both** memory banks. The status of the V_{PP}_ON/OFF registers /RAM write protection is displayed on the front panel LED (see 2.1.1). Jumper B0 must be open. The RAM is default write protected after a RESET.

V_{PP}_ON register	base + $1 write only byte only data any setting during write switch-off RAM write protection, writing to the RAM alters the RAM contents
V_{PP}_OFF register	base + $0 read/write byte/word data any setting during write switch-on RAM write protection, writing to the RAM has no effect on RAM contents (jumper readback)

2.4.3 Reading Jumper Settings

Vital jumper settings can be read from the V_{PP}_OFF register irrespective if jumper B0 is set or open.



2.5 Access Times

The memory chips meet the JEDEC pinout specifications and have an access time of ≤200ns.

The VMEM-S2 has the facility for differing access times for the 2 memory banks. This optimises access times in mixed configurations. The times selected must be according to the chip suppliers' specifications. Times that can be selected are:

1. 100ns
2. 200ns

2.6 Jumper Readback

As an aid to the user, vital jumper settings can be read back. The settings, address volume, access times and chip types, can be read from the V_{PP}_OFF Register, depending on jumper settings. The jumpers effected are B5, B6, B10, B11, B12, B13, B14 and B15 (see Sections 2.4, 3.5 and 3.7 to 3.10).

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2.7 Software Write Protection for RAM

This feature can be selected by jumper. When selected, the RAM is write protected by default after a RESET. This can be altered by software via a control bit (see Section 3.2)

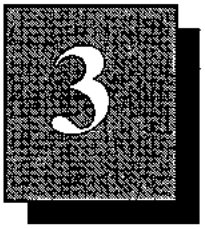
2.8 Battery Backup

Data retention with static RAM is available using the on-board Lithium battery or the VME +5V STDBY* line. Each memory bank can have separate data retention and, even in mixed RAM/ROM configurations, the RAM is buffered (see Sections 3.13 to 3.15).

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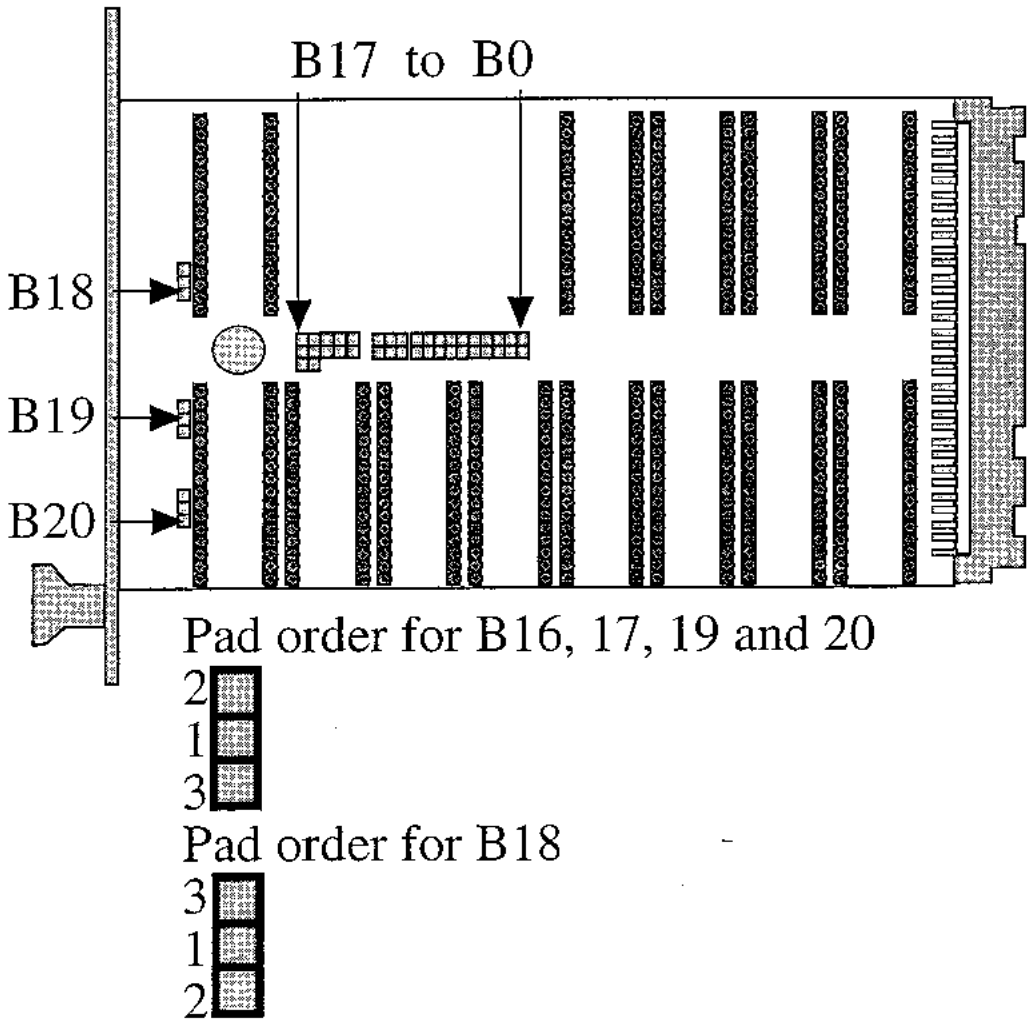
3. CONFIGURATION

The VMEM-S2 has all of its wire jumpers on the component side. There are 5 solder jumpers on the solder side of the board that double the functions of identically numbered wire jumpers on the component side. These are jumpers B16, B17, B18, B19 and B20. The solder jumpers are only to be used if their functions are to be permanently used, otherwise use the wire jumpers.

Note

Users should keep a highly visible reminder if the jumpers **B16, B17, B18, B19** and **B20** have been set by solder. Failure to do so could cause damage if, at a later date, the identically numbered wire jumpers are set to fulfill different functions.

Figure 3.0.0.1 Jumpers Component Side



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3.1 Default Jumper Settings

Below is listed the default jumper settings of the VMEM-S2, as supplied by order number.

Jumper	5020-000	5020-102	5020-106	5020-202	5020-411
B0	set	set	set	set	set
B1	set	set	set	set	set
B2	set	set	set	set	set
B3	set	set	set	set	set
B4	open	open	open	open	open
B5	set	set	open	set	set
B6	set	set	open	set	set
B7	set	set	set	set	set
B8	set	set	set	set	set
B9	set	set	set	set	set
B10	set	set	set	open	set
B11	set	set	set	open	set
B12	set	set	set	open	set
B13	set	set	set	open	open
B14	set	set	set	open	open
B15	set	set	set	open	open
B16	1-3	1-3	1-2	1-3	1-3
B17	1-3	1-3	1-2	1-3	1-3
B18	1-3	1-3	1-3	1-3	1-3
B19	1-3	1-3	1-3	1-3	1-3
B20	1-2	1-2	1-2	1-2	1-2

3.2 Jumper Overview

Jumper	Function	See Section
B0	RAM write protection	3.3
B1	Short I/O base address	3.4
B2	Short I/O base address	3.4
B3	Address modifier code	3.5
B4	Address modifier code	3.5
B5	VMEM-S2 address volume	3.6
B6	VMEM-S2 address volume	3.6
B7	Standard VMEbus base address	3.7
B8	Standard VMEbus base address	3.7
B9	Standard VMEbus base address	3.7
B10	Bank 1 memory type	3.8
B11	Bank 1 memory type	3.8
B12	Bank 1 access time	3.9
B13	Bank 2 memory type	3.10
B14	Bank 2 memory type	3.10
B15	Bank 2 access time	3.11
B16	Multiplexed pin 1 for bank 1	3.12
B17	Multiplexed pin 1 for bank 2	3.13
B18	Bank 1 battery backup	3.14
B19	Bank 2 battery backup	3.15
B20	Battery backup source	3.16

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3.3 RAM Write Protection

B0	RAM write protection
set	disabled
open	enabled

3.4 Short I/O Base Address

The short I/O base address is selected by jumper.

B1	B2	Base address
set	set	Short I/O base address + $0000
set	open	Short I/O base address + $1000
open	set	Short I/O base address + $2000
open	open	Short I/O base address + $3000

3.5 Address Modifier Code

B3	B4	AM code in standard VME address space
set	set	Standard supervisor program/data (3E, 3D)
set	open	Standard supervisor/user program/data (3E, 3D, 3A, 39)
open	set	User defined 1 (18-1F)
open	open	User defined 2 (10-17)

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3.6 VMEM-S2 Address Volume

B5	B6	VMEM-S2 address volume
set	set	2MByte
set	open	4MByte
open	set	reserved
open	open	8MByte

3.7 Standard VMEbus Base Address

The VMEbus address is selected by jumper.

B7	B8	B9	Base address in standard VME address space
set	set	set	VMEbus base address + $000000
set	set	open	VMEbus base address + $200000
set	open	set	VMEbus base address + $400000
set	open	open	VMEbus base address + $600000
open	set	set	VMEbus base address + $800000
open	set	open	VMEbus base address + $A00000
open	open	set	VMEbus base address + $C00000
open	oepn	open	VMEbus base address + $E00000

3.8 Bank 1 Memory Type

B10	B11	Memory type
set	set	RAM
set	open	reserved
open	set	EPROM
open	open	FLASH

3.9 Bank 1 Access Time

B12	Access time
set	100ns
open	200ns

3.10 Bank 2 Memory Type

B13	B14	Memory type
set	set	RAM
set	open	reserved
open	set	EPROM
open	open	FLASH

3.11 Bank 2 Access Time

B15	Access time
set	100ns
open	200ns

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Note

Jumpers B16 to B20 can either be set on the solder or component side of the board. If the configuration available from these jumpers is to be permanent then the solder jumpers can be used. Should this be done please make a highly visible note of the fact, as any later re-setting of the same jumpers on the component side (wire jumpers) can cause damage to the board. The location of the wire jumpers is displayed at the beginning of this chapter, the location of the solder jumpers is displayed in the figure at the end of this chapter.

3.12 Multiplexed Pin 1 for Bank 1

B16	Multiplexed pin 1
1-2	RAM with 512K*8 memory chip
1-3	any other configuration

3.13 Multiplexed Pin 1 for Bank 2

B17	Multiplexed pin 1
1-2	RAM with 512K*8 memory chip
1-3	any other configuration

3.14 Bank 1 Battery Backup

B18	Battery backup
1-2	enabled
1-3	disabled

3.15 Bank 2 Battery Backup

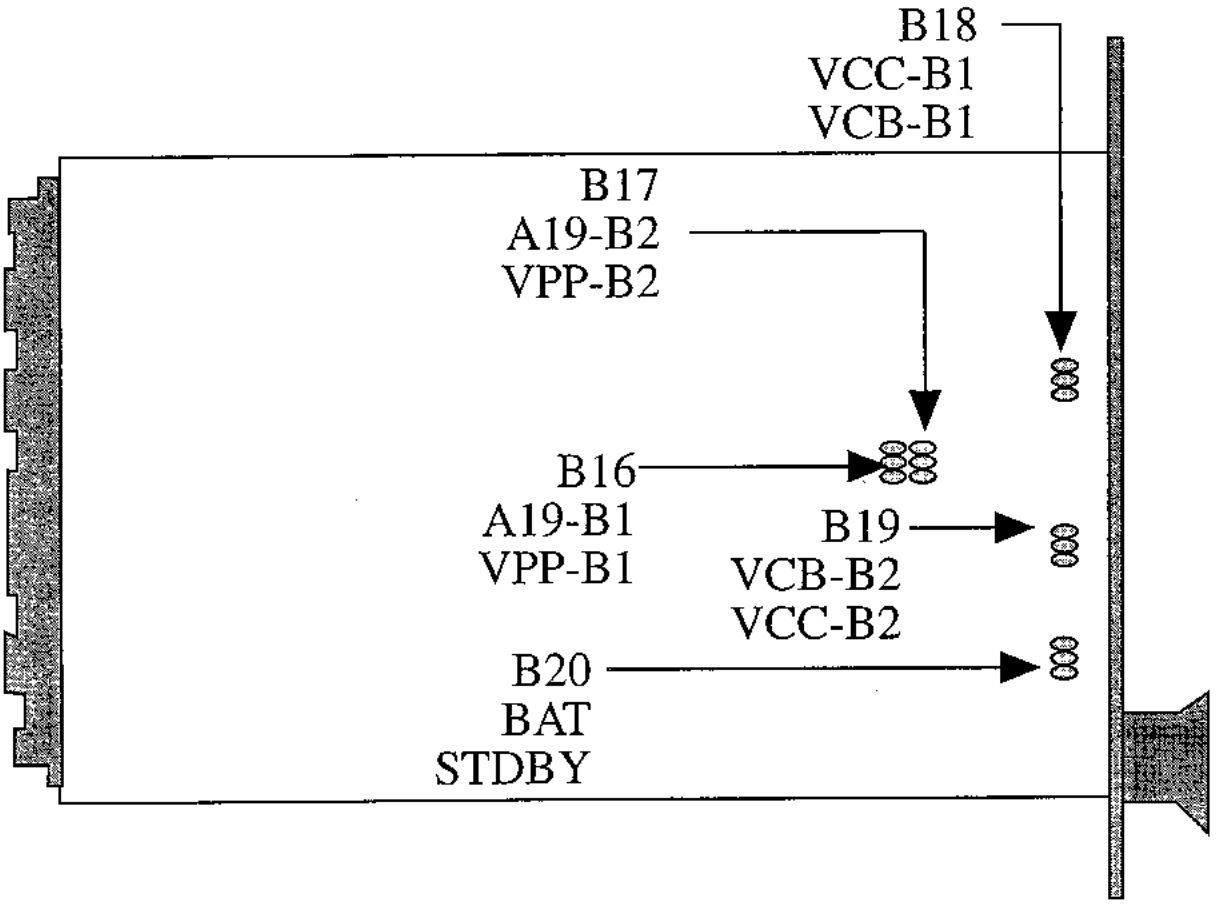
B19	Battery backup
1-2	enabled
1-3	disabled

3.16 Battery Backup Source

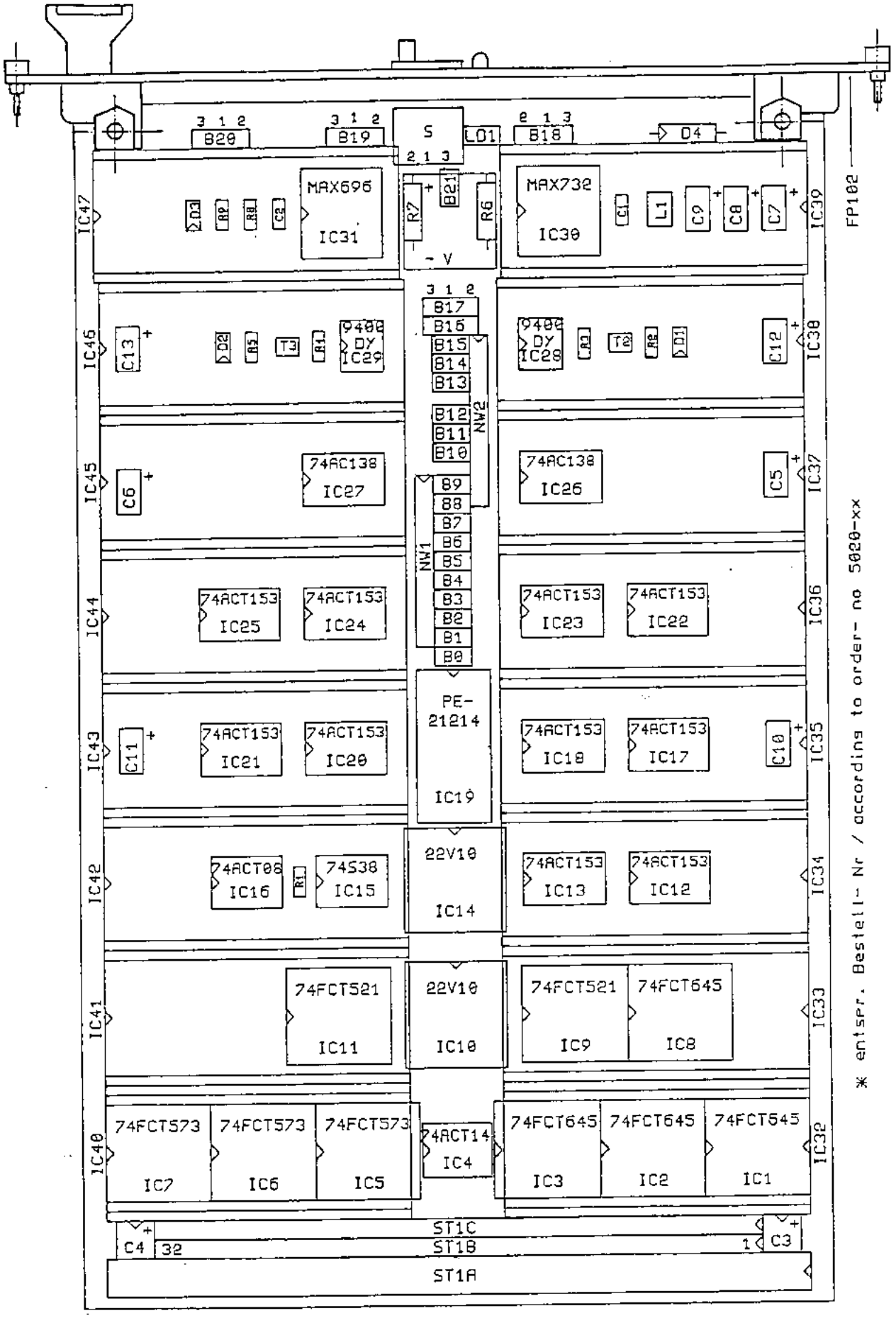
B20	Source
1-2	On-board Lithium cell
1-3	Via 5V StdBy line

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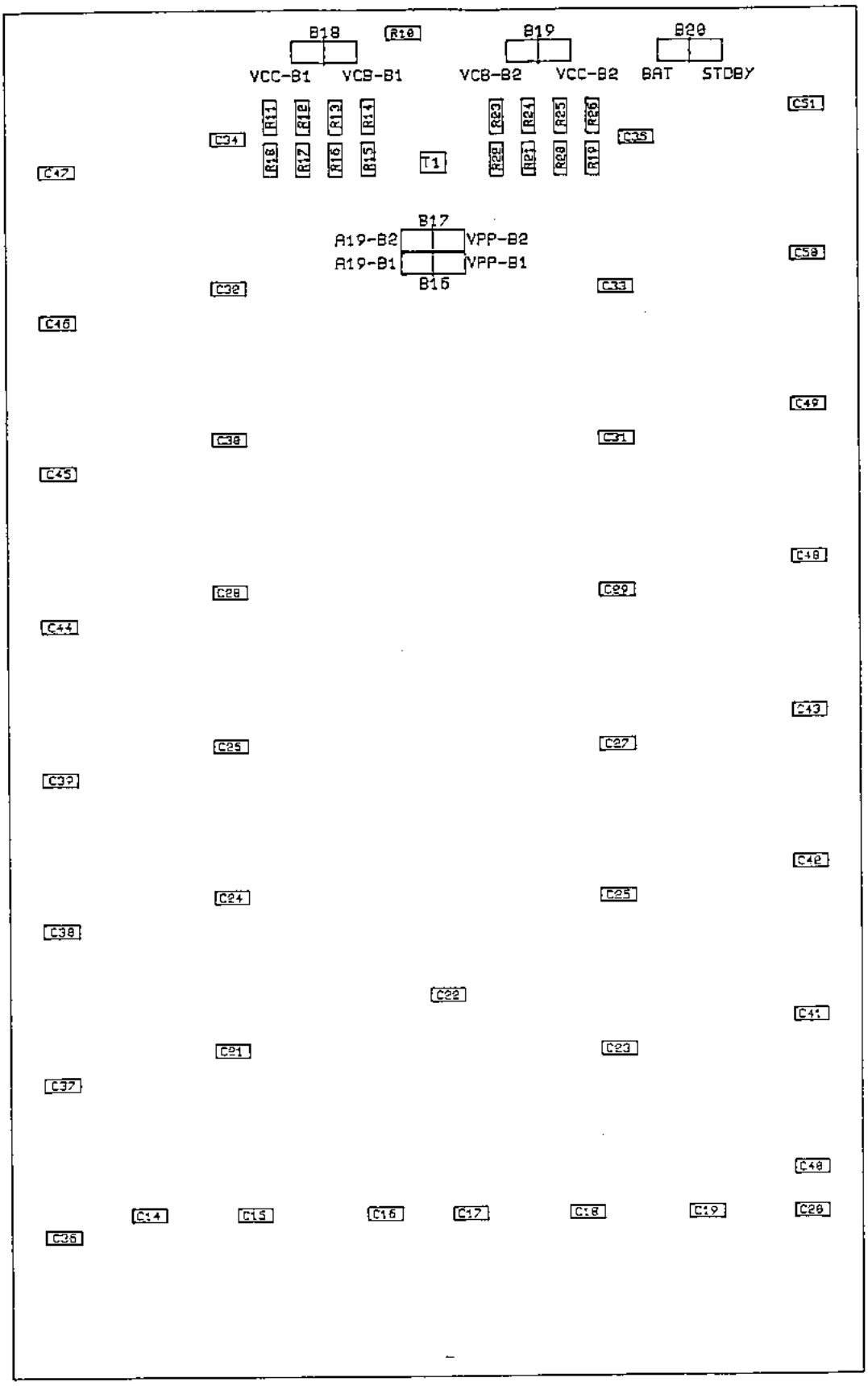
3.17 Solder Jumper Overview



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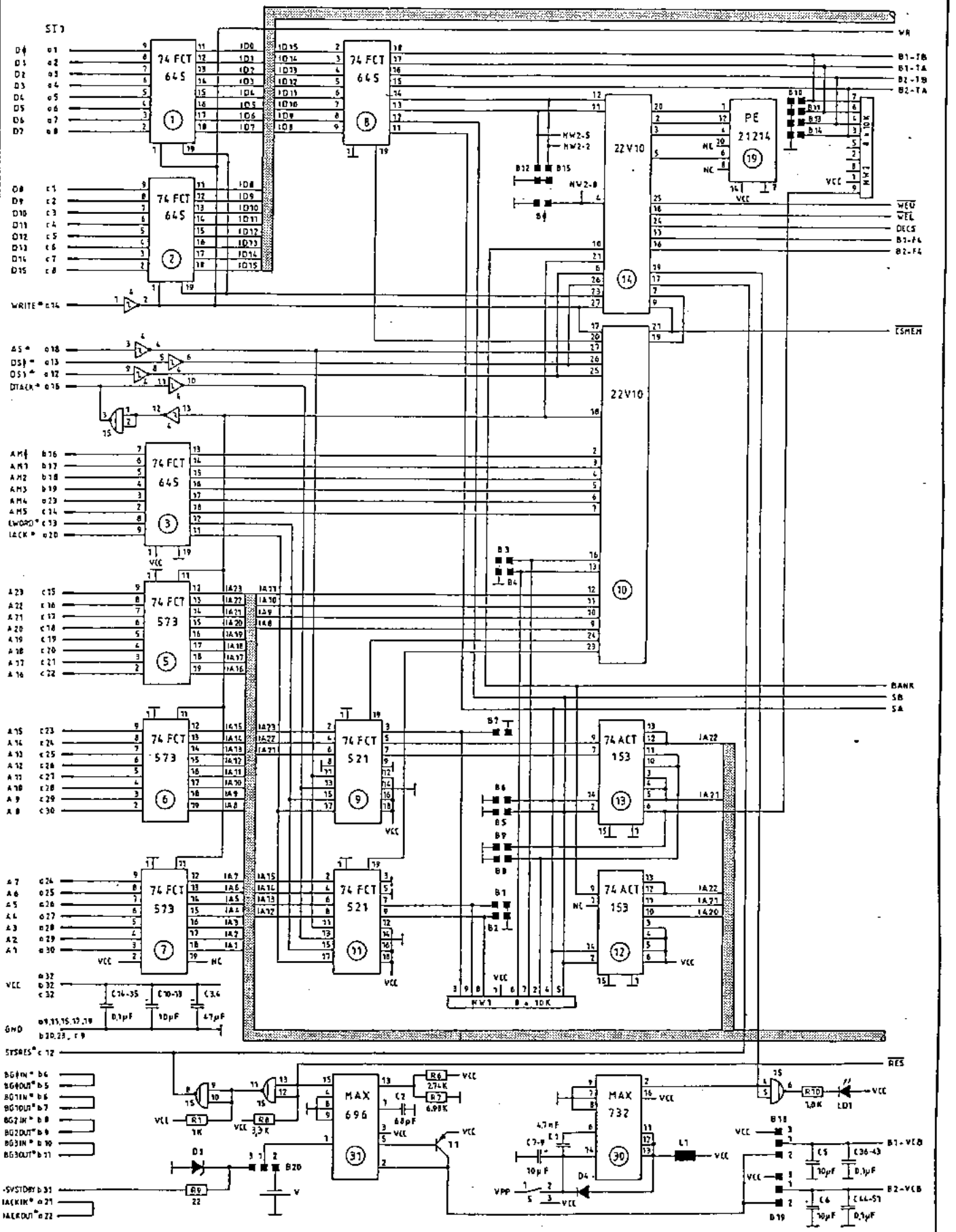


B-Seite / B-side



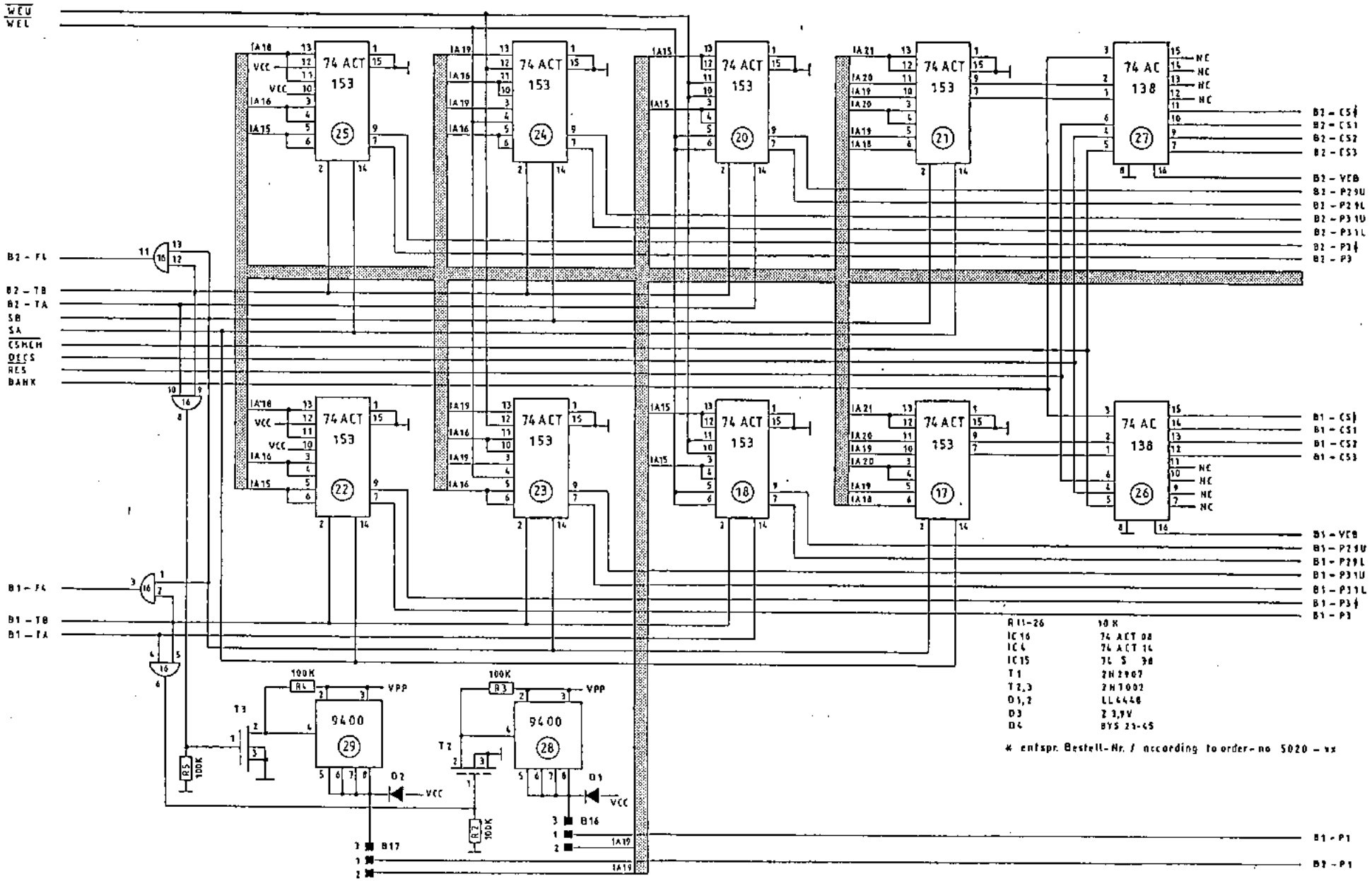
L-Seite / L-side

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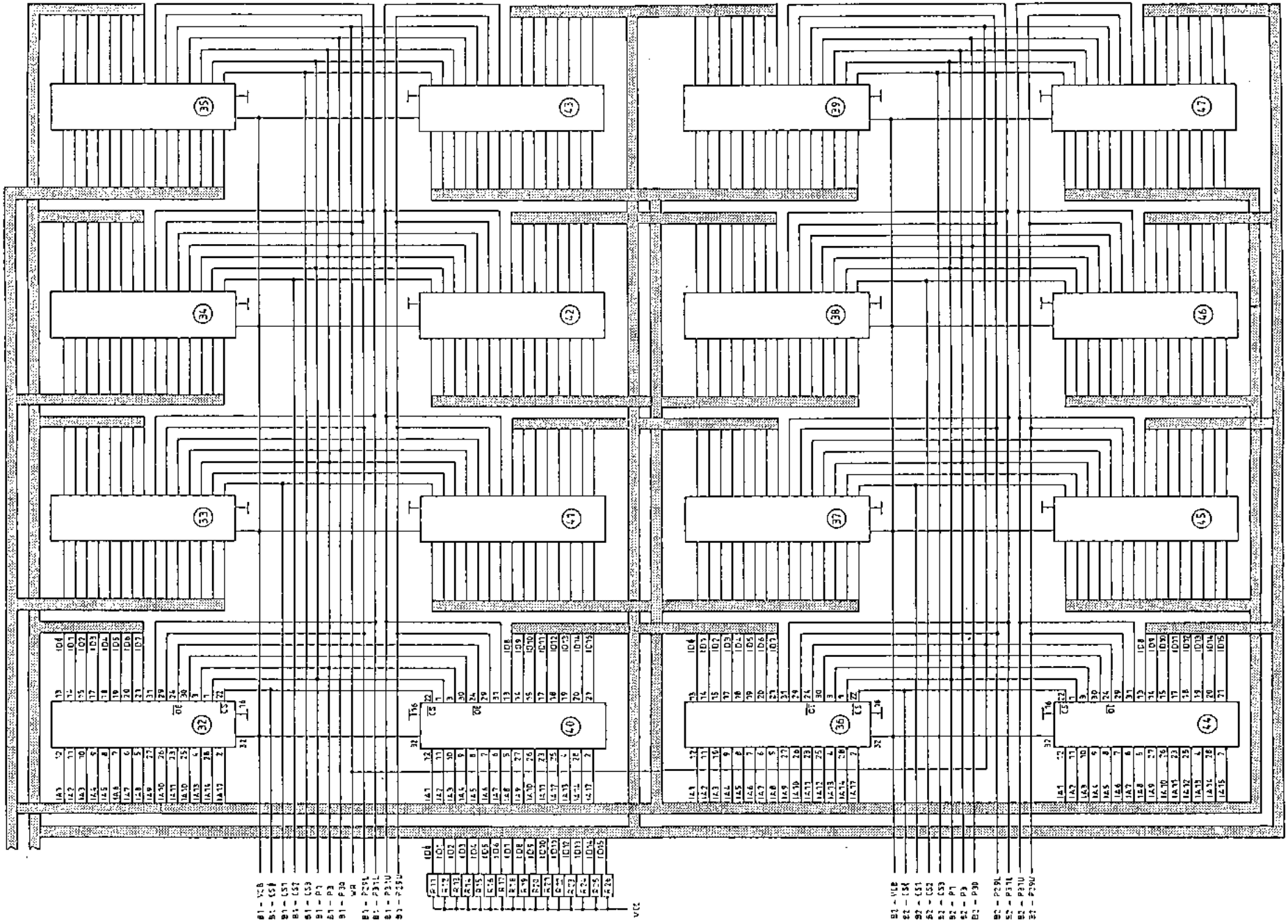
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R11–26	10 K
IC16	74 ACT 08
IC4	74 ACT 14
IC15	74 S 38
T1	2N2907
T2,3	2N1002
D1,2	LL4448
D3	Z 3,9V
D4	BYS 23-45

* entspr. Bestell-Nr. / according to order-no 5020 – xx



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Errata 1

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3. *Reference: Page 3 - 4, Chapter 3.9, Table ..... 1 - 4*
4. *Reference: Page 3 - 4, Chapter 3.11, Table ..... 1 - 4*

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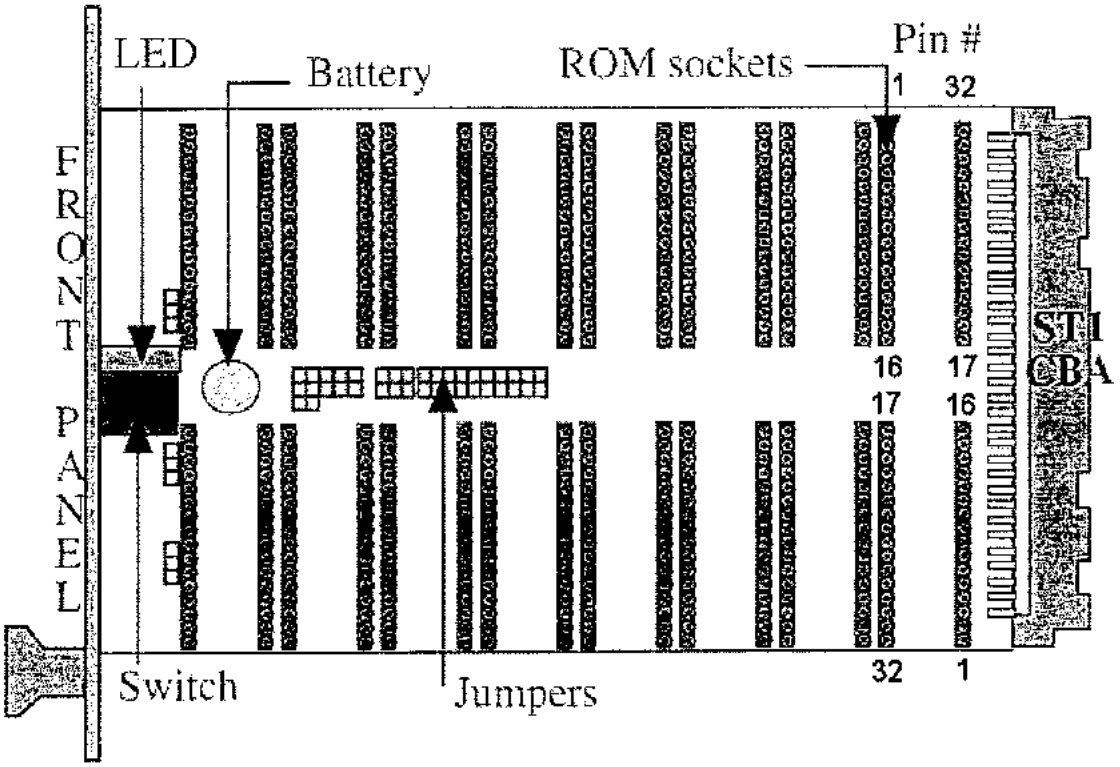
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1. Reference: Page 1 - 3, Chapter 1.4, Figure

The referenced information (figure indicating Board Overview – Component Side) is superseded by the following figure.

Component Side



2. Reference: Page 3 - 3, Chapter 3.5, Table

The referenced information (table in section "Address Modifier Code") is superseded by the following table.

B3	B4	AM CODE IN STANDARD VME ADDRESS SPACE
set	set	Standard supervisor program/data (3E, 3D)
set	open	Standard supervisor/user program/data (3E, 3D, 3A, 39)
open	set	User defined 1 (10 - 17)
open	open	User defined 2 (18 - 1F)

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3. Reference: Page 3 - 4, Chapter 3.9, Table

The referenced information (table) is superseded by the following table.

B12	ACCESS TIME
set	100ns
open	150ns

3. Reference: Page 3 - 4, Chapter 3.11, Table

The referenced information (table) is superseded by the following table.

B15	ACCESS TIME
set	100ns
open	150ns

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