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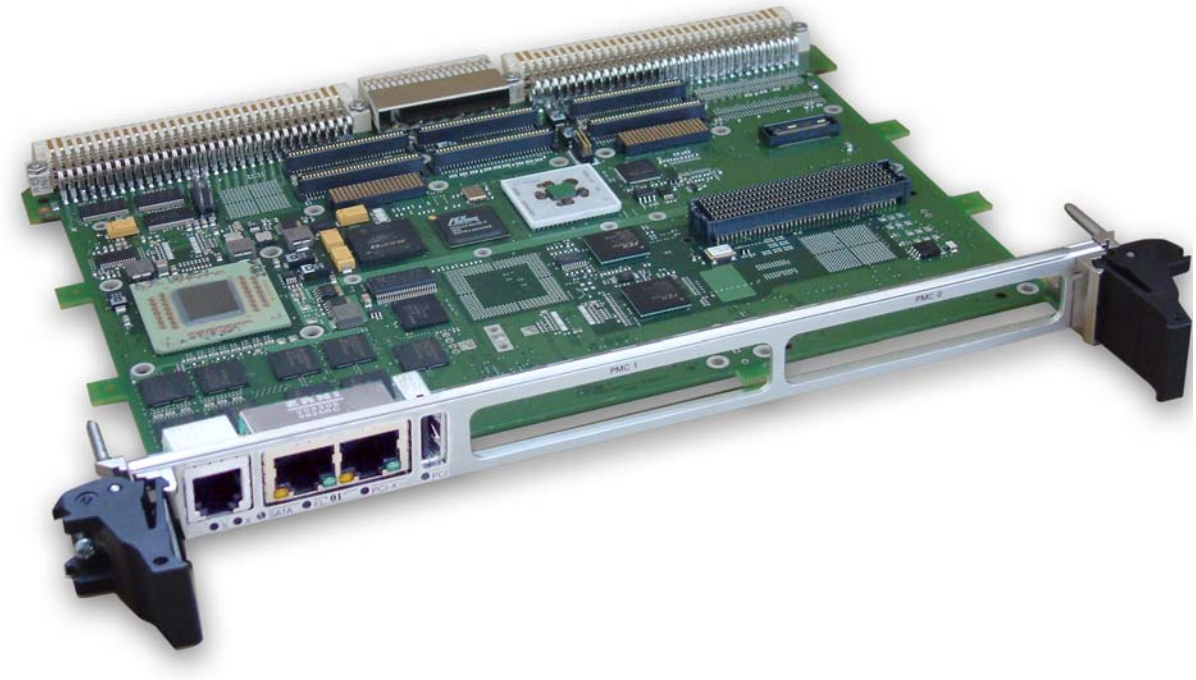
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» VM6250 «



6U VME PowerPC SBC
User's Guide

CA.DT.A65-2e - November 2010

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- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.



Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.



When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

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Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions



ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1 - Introduction

The VM6250 is built around Freescale's state-of-the-art MPC8640/8641 single or dual-core e600 processor.

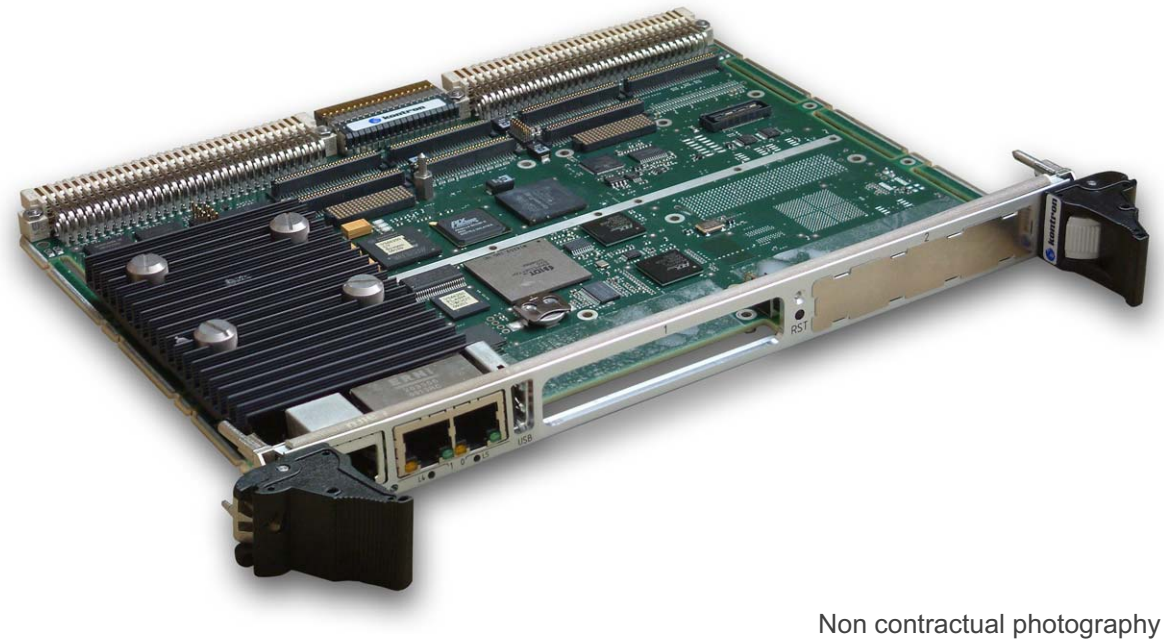
The VM6250 provides exceptional I/O capabilities onboard and outstanding flexibility by being the first 6U VME board to provide support for PMC, XMC and FMC mezzanine cards.

The VM6250's high performance, 2eSST, VME interface helps customers preserve their investment in legacy VME equipment.

The VM6250 was designed to be Kontron's next generation VME SBC providing substantial price and performance over previous generations of VME computers.

In this document, the term:

- VM6250 will be associated to 6U VME boards, air-cooled, air-cooled extended temperature and conduction-cooled versions:
  - VM6250-SA Air-cooled version
  - VM6250-WA Air-cooled extended temperature version
  - VM6250-RC Conduction-cooled version
- **VM6250-RTM** will be associated to the 6U VME Rear Transition Module (RTM)



Non contractual photography

Figure 1: VM6250-SA Overview

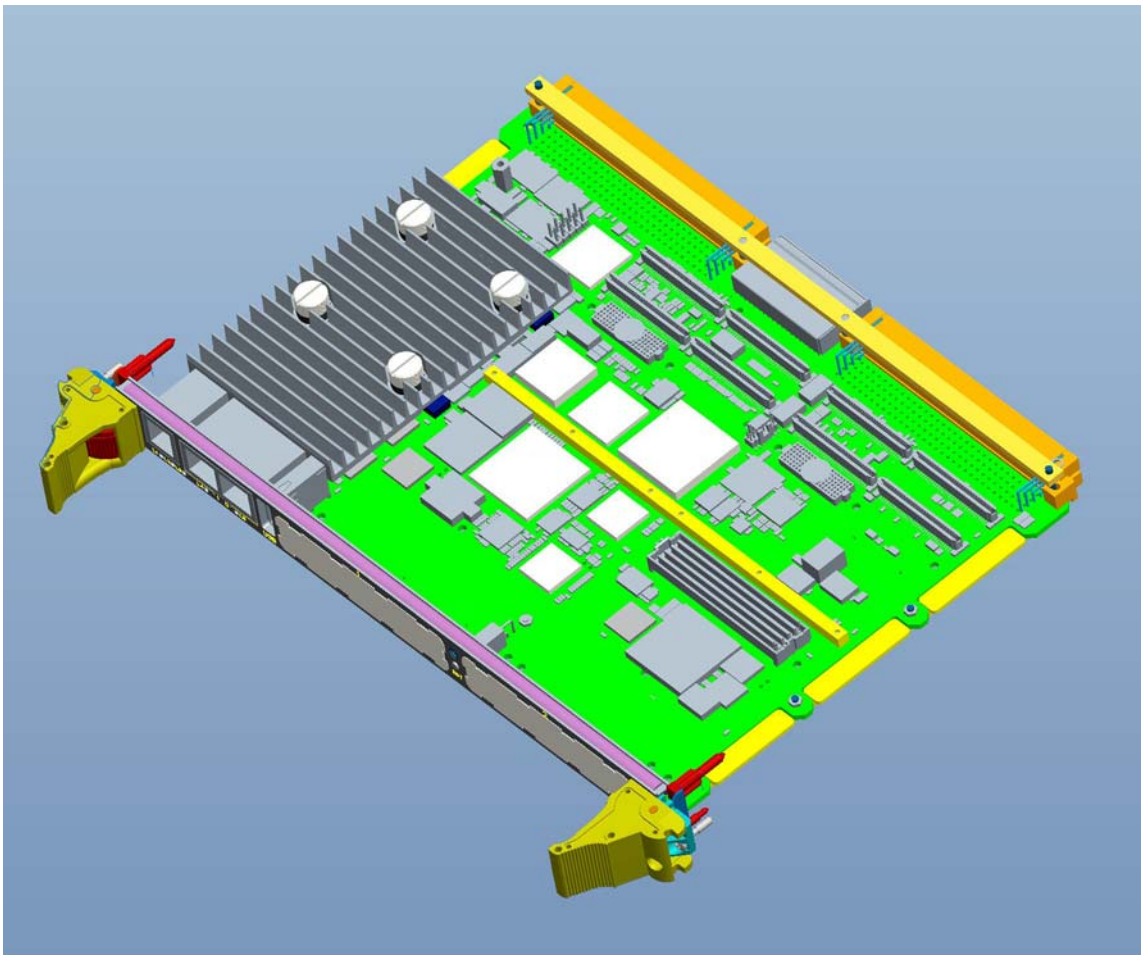


Figure 2: VM6250-WA Overview

1.1 Manual Overview

1.1.1 Objectives

This guide provides general information, hardware preparation and installation instructions, operating instructions and a functional description of the VM6250 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.7 “Related Publications" page 21).



As the standard policy for all the Kontron, hardware technical documentation reflects the most recent version of our products. The “Hardware Release Notes" (see section 1.7 “Related Publications" page 21) is to help to keep track of various evolutions that have happened during the early steps of the VM6250 ramp-up or later in its lifetime.



Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2 Audience

This guide is written to cover, as far as possible, the range of people who will handle or use the VM6250, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, systems, cabling, grounding and communications.

1.1.3 Scope

This guide describes all variants of the VM6250 series. It does not cover any PMC/XMC or FMC modules which are described in specific guides (see section 1.7 “Related Publications" page 21).

1.1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Functional Description
- Chapter 3 - Installation
- Chapter 4 - Programming Interface
- Chapter 5 - Power and Thermal Considerations
- Chapter 6 - VM6250-RTM Characteristics

1.2 Board Overview

1.2.1 Main Features

Powerful Freescale MPC864x PowerPC Architecture

The Freescale MPC864x processor features an AltiVec engine to perform 128-bit wide parallel processing instructions (SIMD), and a four channel DMA controller to accelerate data transfers.

In order to fit all the requirements with the best compromise between performance and dissipation, the VM6250 is available in several different configurations. It can be equipped with:

- a Freescale MPC8640 single processor at a frequency of 1 GHz
- a Freescale MPC8640D dual processor at frequencies of 1 GHz and 1.25 GHz
- a Freescale MPC8641D dual processor at a frequency of 1.33 GHz

Soldered DDR2 Memories with the Support of ECC

The MPC864x provides DDR2 memory controllers operating up to 533 MHz with 72-bit wide DDR2 SDRAM configured with 8 bits for Error-Correcting Code (ECC). The peak memory bandwidth is 4.3 GB/s.

Numerous Storage Interfaces

128 KB of Auto-store, Non-Volatile Random Access Memory allows backup of critical data when power is removed. Dual redundant 32 Mb NOR Flash are used to store firmware code and built-in tests, and two serial 256 Kb EEPROMs are dedicated to system and application date storage.

A USB 2.0 Flash drive slot is available onboard supporting low standard profile USB 2.0 Flash disk modules up to 8 GB.

Depending on the SATA Manufacturing Option, a SATA drive slot is available onboard supporting SATA HDD up to 120 GB.

The VM6250 is equipped with the ALMA2f VME controller supporting the VME64x and 2eSST protocols offering up to 320 MB/s peak throughput.

Backplane Switch

Two Gigabit Ethernet links are available on P0 connector. P0 Ethernet routing supports VITA 31.1 backplane networking.

In addition, one 4x PCI Express link is available on P0, which, optionally may be configured as one 4x Serial RapidIO link.

Extensive I/O Connectivity

The VM6250 provides up to four 10/100/1000BASE-T(X) Ethernet interfaces, two EIA-232 serial lines, three general purpose I/Os (GPIO), four USB 2.0 links, two SATA II interfaces and one 4x PCI-Express link.

Two onboard mezzanine sites support PCI, PCI-Express and FMC cards (VITA 57 FPGA I/O).

FMC Support, VITA 57

The VM6250 is one of the first high-performance 6U VME cards to support the new FPGA Mezzanine Card (FMC) standard defined by VITA 57.

Legacy Compatibility

The VM6250 has been designed to offer a legacy I/O compatibility with the Kontron's VMPC6x and PowerEngine7 boards to provide an easy path for technology insertion into existing systems.

Software

The VM6250 is delivered with PowerOn Built-in-Test and the OpenSource U-Boot firmware.

The VM6250 supports Wind River's VxWorks 6.6 Real Time Operating System Software and and Fedora 9 Linux distributions. Consult factory for other O/ support.

Designed to meet the Requirements of Harsh Environments

The VM6250 has been designed using the same PCB for both air and conduction-cooled boards. Build variants span a complete range of temperature, shock and vibration requirements as specified in the VITA 47 standards.

10-year Long Life Cycle

Investing in a new project is always a challenge and risky. Maximizing the lifetime of an application is therefore a critical issue when it comes to saving development investments.

The VM6250 has been designed with long life cycle components. Beyond the use of standard commercially available components, Kontron offers Longevity of Supply services which are designed to make the VM6250 available for then years or longer.

Carrier Board

The VM6250 supports the V2PMC2, a 6U VME PCI-X/PMC carrier card that holds up to two single-width or one double-width PCI-X/PMC modules.

Rear Transition Module

The VM6250 supports the VM6250-RTM, a 6U VME Rear Transition Module compliant to PMC I/O Module Standard VITA 36 - 199x Draft 0.1 July 19, 1999 (mechanical and PIM format).

1.2.2 I/O Interfaces

FUNCTION	DESCRIPTION
Ethernet	Broadcom BCM5466R low-power quad Gigabit Ethernet Transceiver: - Two 10/100/1000BASE-T(X) ports available on RJ-45 front panel connectors - Two 10/100/1000BASE-T(X) ports available on the rear P0 connector
USB	Four USB 2.0 channels - USB port 0 9-pin USB pin header, horizontal USB flash disk module - USB port 1 One USB port available on the VM6250 front panel - USB ports 2, 3 Two USB ports available on rear P0 connector
Serial ATA (SATA)	Depending on SATA Manufacturing option, - Two SATA II ports are available on rear P0 connector or - One SATA II port is available on rear P0 connector, and one SATA II port is available onboard.
Serial Ports	Two serial ports EIA-232 - COM1 EIA-232 (simplified) port on RJ-12 front panel connector or on the rear P2 connector - COM2 EIA-232 (simplified) port on RJ-12 front panel connector or on the rear P2 connector
GPIO	Three General Purpose I/O on rear P0 connector.
LED	Five status LEDs on front panel: L1, L2, L3, L4, L5
Reset	One reset button on front panel.

Table 1: I/O Interfaces

FUNCTION	VM6250		VM6250-RTM	
	Front Panel	Onboard	Front Panel	Onboard
Gigabit Ethernet	Y (x2)	-	Y (x2)	-
USB0	-	Y (9-pin)	-	-
USB1	Y	-	-	-
USB2	-	-	Y	-
SATA (P0 Manufacturing Option)	-	-	Y (x2)	-
SATA (onboard Manufacturing Option)	-	Y	Y	-
COM1 (EIA-232)	Y	-	-	Y (10-pin)
COM2 (EIA-232)	Y	-	-	Y (10-pin)
GPIO	-	-	-	Y (x3)
LED	Y (x5)	-	-	-
Reset Button	Y	-	-	-
PCI-Express	-	-	Y	-
SMB	-	-	-	Y

Table 2: Peripheral Connectivity

1.2.3 Ordering Information

Article	Order Number	Description
		Air-cooled version (1)
VM6250	VM6250-1SA24-10110	8640 1 GHz 1GB DDR2 SDRAM 128K NVRAM 2x PMC P0
VM6250	VM6250-2SA25-11110	8640D 1 GHz 2GB DDR2 SDRAM 128K NVRAM 2x PMC/XMC
VM6250	VM6250-2SA35-11110	8640D 1.25 GHz 2GB DDR2 SDRAM 128K NVRAM 2x PMC/XMC
VM6250	VM6250-2SA45-11110	8641D 1.33 GHz 2GB DDR2 SDRAM 128K NVRAM 2x PMC/XMC
		Air-cooled extended temperature version (1)
VM6250	VM6250-1WA24-10110	8640 1 GHz 1GB DDR2 SDRAM 128K NVRAM 2x PMC P0
VM6250	VM6250-2WA25-11110	8640D 1 GHz 2GB DDR2 SDRAM 128K NVRAM 2x PMC/XMC
VM6250	VM6250-2WA35-11110	8640D 1.25 GHz 2GB DDR2 SDRAM 128K NVRAM 2x PMC/XMC
		Conduction-cooled version (1)
VM6250	VM6250-1RC24-10110	8640 1 GHz 1GB DDR2 SDRAM 128K NVRAM 2x PMC
VM6250	VM6250-2RC25-11110	8640D 1 GHz 2GB DDR2 SDRAM 128K NVRAM 2x PMC/XMC
		Associated Product
RTM	PBV36-P0-VM6-00	6U VME Air-Cooled Rear Transition Module
Console Cable	KIT-RJ12DB9	Adaptation Cable RJ-12 <-> DB-9
PMCs Carrier	V2PMC2-SA	6U VME Air-Cooled Dual PMCs Carrier Card
PMCs Carrier	V2PMC2-RC	6U VME Conduction-Cooled Dual PMCs Carrier Card
USB Flash Disk	FDM-USB-*x*GB-L2-IV	USB Flash Disk Module (contact Kontron for the available capacity)
Kit Disk SATA	KIT-DISK25-SATA KIT-DISK18-SATA	Kit Disk SATA, compatible with SATA disk 2.5-inch Kit Disk SATA, compatible with SATA disk 1.8-inch (2)
EZ2-VM6250	EZ2-VM6250	Laboratory 6U VME Air-Cooled Development System

(1) Other features supported on demand. Please, contact, Kontron for availability.

(2) Please, contact, Kontron for availability.

Table 3: Order Code Table

1.2.3.1 FMC Manufacturing Option



Please, contact Kontron for availability.

1.2.3.2 SATA Manufacturing Option

Depending on the SATA manufacturing option:

SATA on P0: Two SATA II ports are available on rear P0 connector

or

SATA onboard: One SATA II port is available on rear P0 connector, and one SATA II port is available onboard.

This specific option is encoded in the order code, 2nd digit of the third part of the order code.

Article	Order Number	Description
		Air-cooled version
VM6250	VM6250-1SA24-13110	8640 1 GHz 1GB DDR2 SDRAM 128K NVRAM 1x PMC P0 SATA onboard
VM6250	VM6250-2SA25-13110	8640D 1 GHz 2GB DDR2 SDRAM 128K NVRAM 1x PMC/XMC SATA onboard
VM6250	VM6250-2SA35-13110	8640D 1.25 GHz 2GB DDR2 SDRAM 128K NVRAM 1x PMC/XMC SATA onboard
VM6250	VM6250-2SA45-13110	8641D 1.33 GHz 2GB DDR2 SDRAM 128K NVRAM 1x PMC/XMC SATA onboard
		Air-cooled extended temperature version
VM6250	VM6250-1WA24-13110	8640 1 GHz 1GB DDR2 SDRAM 128K NVRAM 1x PMC P0 SATA onboard
VM6250	VM6250-2WA25-13110	8640D 1 GHz 2GB DDR2 SDRAM 128K NVRAM 1x PMC/XMC SATA onboard
VM6250	VM6250-2WA35-13110	8640D 1.25 GHz 2GB DDR2 SDRAM 128K NVRAM 1x PMC/XMC SATA onboard

Table 4: Order Code Table (SATA onboard)

1.2.4 Block Diagram

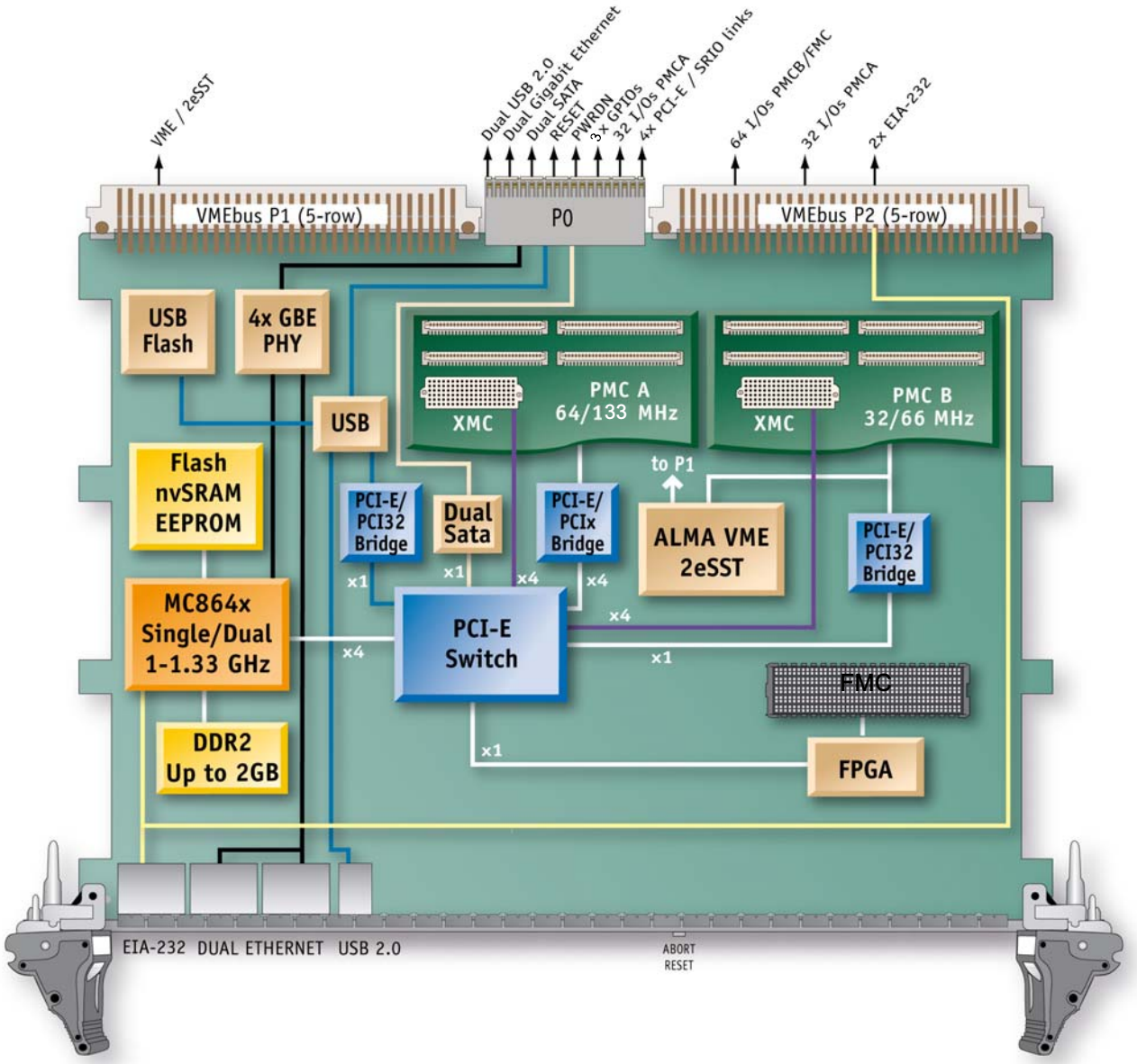


Figure 3: VM6250 Functional Block Diagram

1.2.5 Front Panel



Figure 4: Front Panel Connectors

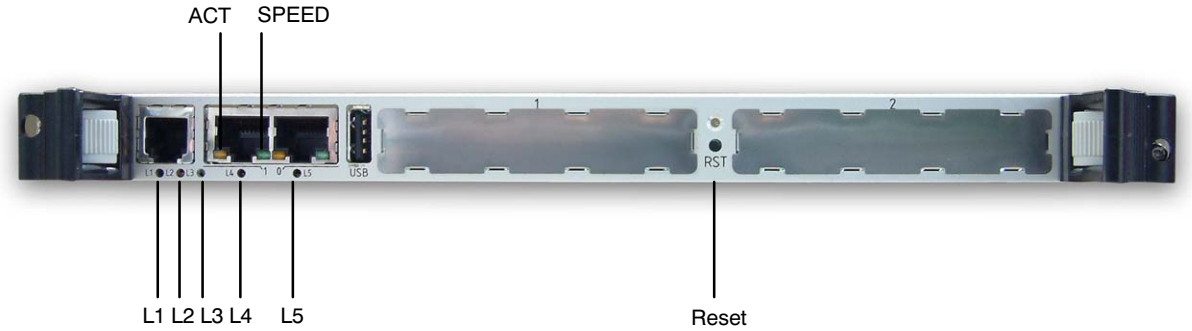


Figure 5: Reset Button and LEDs

Reset Button

Status LEDs Default Settings

L1	red/green	Reserved
L2	red	Reset is activated
	green	Activity on Rear LAN links
L3	red	MPC864x is in a checkstop state
	green	Activity on MPC864x Local Bus
L4	red	Board over-temperature alarm
	green	Activity on SATA link
L5	red	Factory mode is activated
	green	Activity on VME bus

Gigabit Ethernet LEDs

Status		SPEED LED green	ACT LED yellow
Ethernet link is not established		OFF	OFF
10/100 Mbps	Ethernet link establisehd	OFF	ON
	Ethernet Link Activity	OFF	BLINK
1000 Mbps	Ethernet link establisehd	ON	ON
	Ethernet Link Activity	ON	BLINK

Table 5: Ethernet LEDs Status Definition

1.2.6 Components Layout

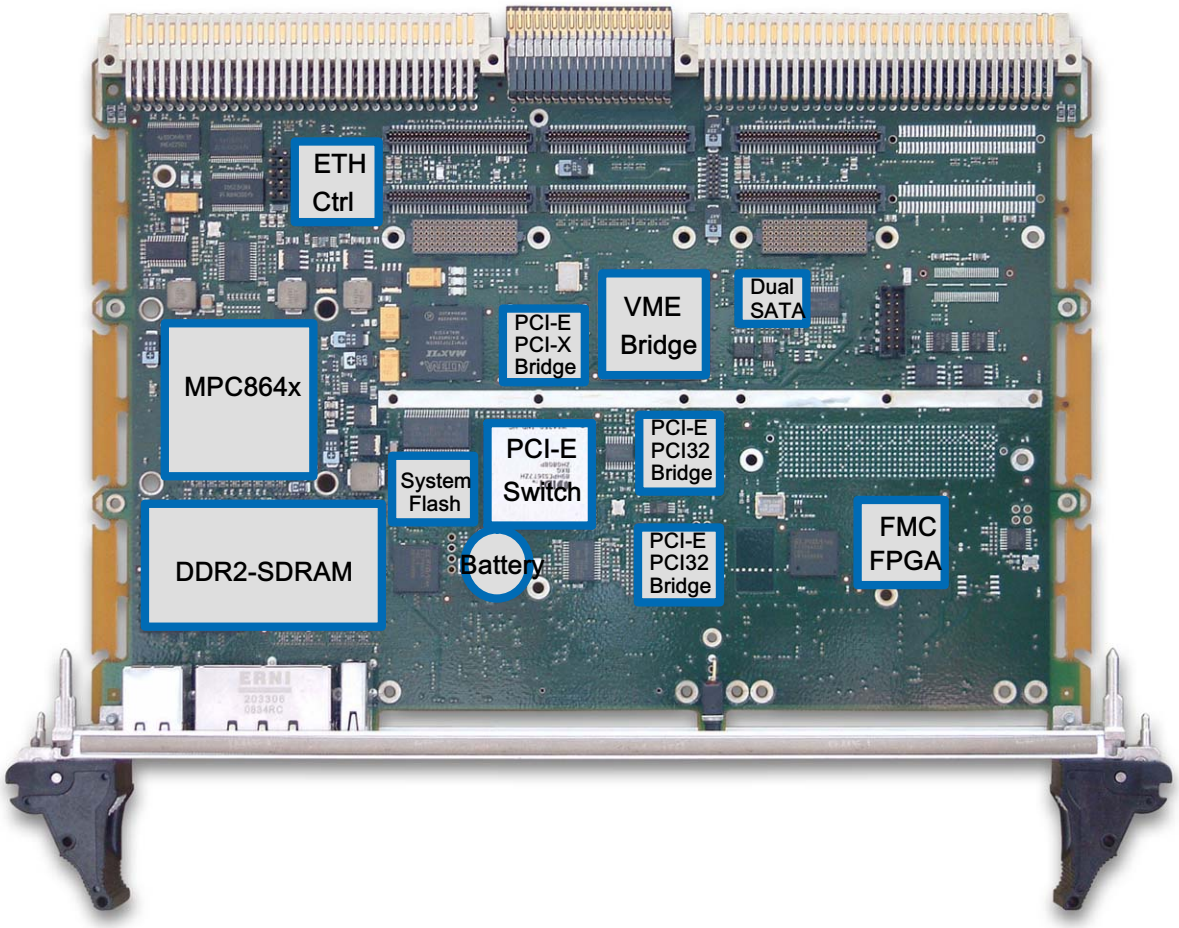


Figure 6: Components Layout (Top View)

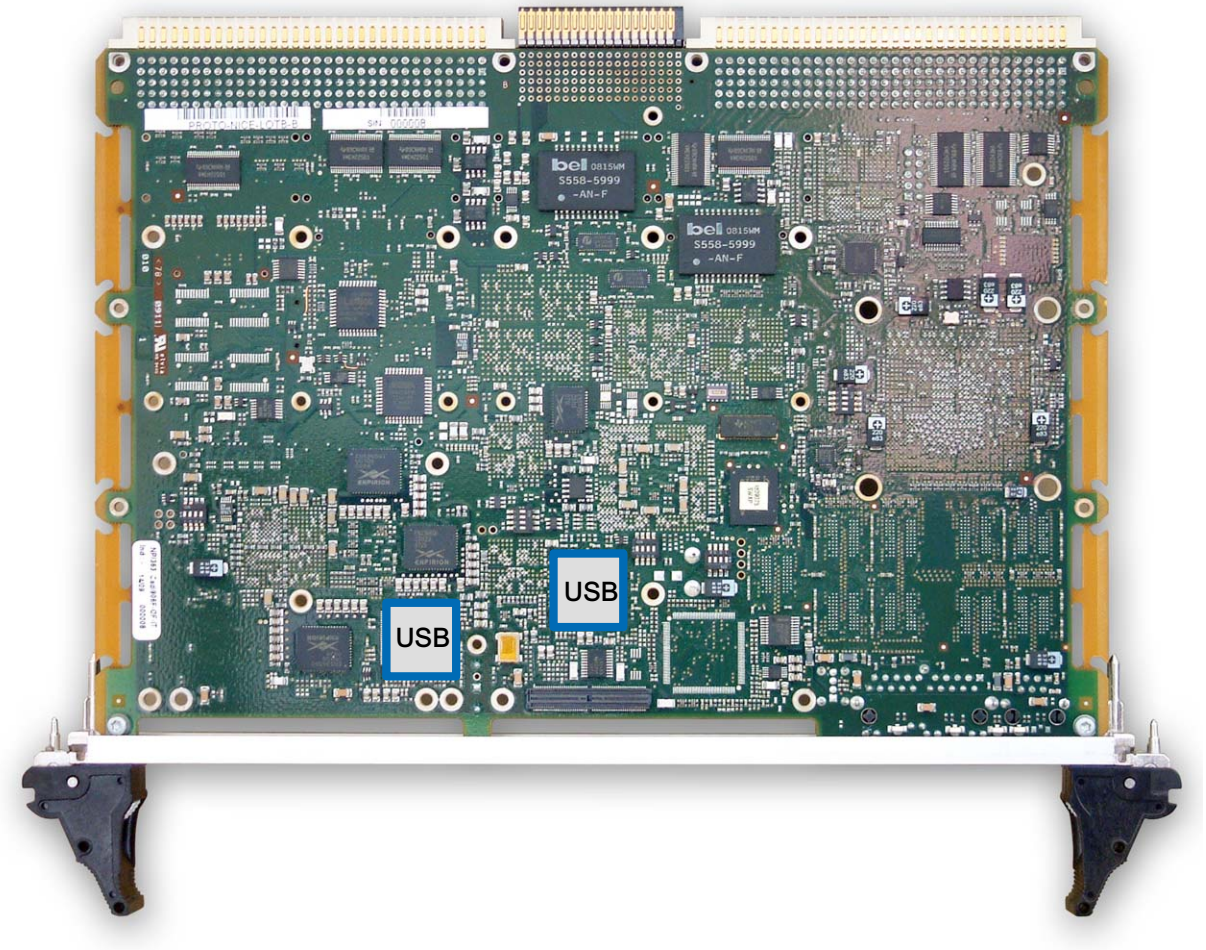


Figure 7: Components Layout (Bottom View)

1.2.7 VM6250-WA Specificities

This section sums up the main specificities of the VM6250-WA boards:

> Environmental Specifications, see also section 1.6 page 20.

WA Air-Cooled Extended Temperature	VITA 47 Conformal Coating	Yes
	Airflow	up to 3.0m/s (depending on the processor frequency)
	Temperature VITA 47-Class AC1 VITA 47-Class C1/C2	Cooling Method: Convection Operating: -20°C to +65°C Storage: -45°C to +85°C
	Vibration Sine (Operating) VITA 47-Class V1	2g / 20-500 Hz acceleration / frequency range
	Shock (Operating) VITA 47-Forced Air Cooled Class	20g / 11ms peak acceleration / shock duration half sine
	Altitude (Operating)	-1,640 to 33,000 ft
	Climatic Humidity	95% non-condensing
	Board Weight	~ 500 g

> Specific tighteners (x8) have been added on the PCB (see arrows in figure below):

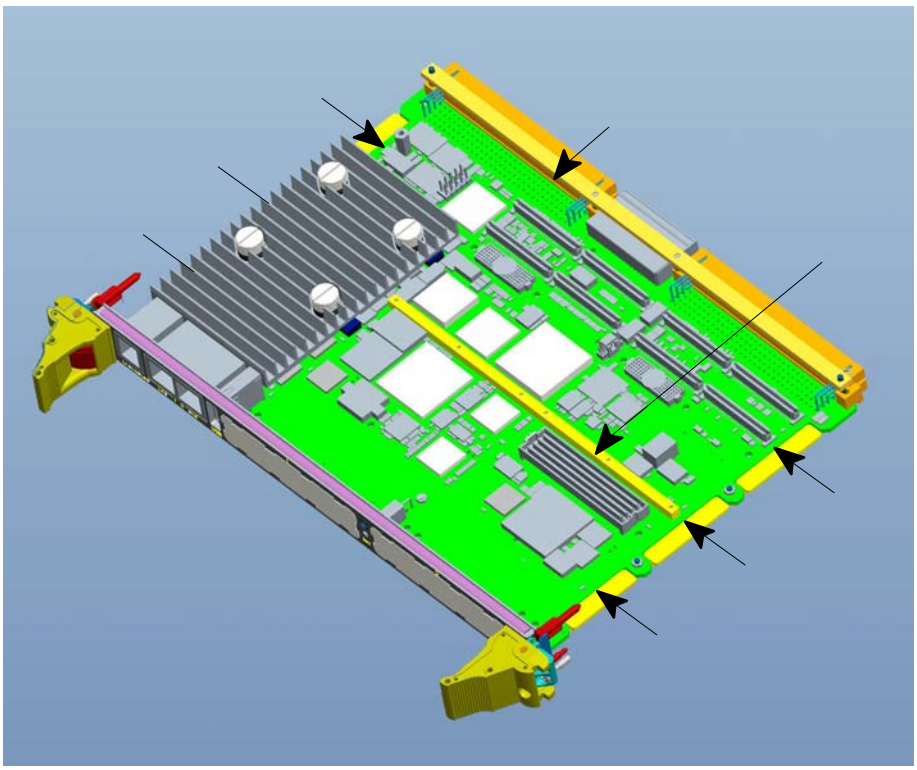


Figure 8: VM6250-WA - Location of the Tighteners

1.3 Technical Specification

	VM6250	SPECIFICATIONS
Processor and Memory	CPU	The VM6250 supports one of the following microprocessors: - Freescale MPC8640 Single-Core PowerPC, 1 GHz - Freescale MPC8640D Dual-Core PowerPC, 1 GHz or 1.25 GHz - Freescale MPC8641D Dual-Core PowerPC, 1.33 GHz
	Memory	System Memory: - 1 or 2 GB DDR2-533 SDRAM, wide, soldered - Error Checking and Correction (ECC) provided Cache structure: - 96 kB L1 on die full speed processor cache - 1 x 32 kB for instruction cache - 2 x 32 kB for data cache - 2 MB L2 on die full speed processor cache (1 MB by core) Firmware Boot Device: - 2 x 32 Mb soldered NOR flash for NetBootLoader or U-Boot firmware, redundant boot device NOVRAM: - 128 KB of Non-Volatile RandomAccess memory (Semtek) for autostore operation EEPROM: - two serial 256 Kb EEPROMs for systems and application data storage Nand Flash: - Socket for USB Nand Flash Module, Low Profile, 2.54 pitch connector, up to 8 MB
Interfaces	Rear I/O	The following interfaces are routed to the Rear P0 connector: - 2x USB 2.0 - 2x Gigabit Ethernet - Up to 2x SATA II depending on SATA Manufacturing option - 3x General Purpose Inputs and Outputs Signals (GPIOs) - x1/x4 PCI-Express links (if no RapidIO option) - x1/x4 Serial RapidIO links (multiplexed with PCI-Express) - 32 I/Os PMC#1 The following interfaces are routed to the Rear P2 connector: - 32 I/Os PMC#2 - 32 I/Os PMC#2 / FMC - 2x EIA-232
	Gigabit Ethernet	Four Gigabit Ethernet interfaces, based on the Broadcom BCM5466R Ethernet, low-power quad gigabit ethernet transceiver with Serdes and copper media interface. - Two ports available on the front panel, dual RJ-45 connector - Two ports routed to the Rear P0 connector - Automatic mode recognition - Automatic cabling configuration recognition Cabling requirement: Category 5, UTP, four-pair cabling
		Page 1 of 4

	VM6250	SPECIFICATIONS
Interfaces	USB	Four USB ports supporting UHCI and EHCI on VM6250: - One onboard to connect the optional Flash Disk Module - One USB 2.0 connectors on the front panel - Two USB 2.0 connectors on the Rear P0 connector
	Serial Lines	Two EIA-232 simplified serial lines - One on the front panel or on Rear P2 connector - One on rear P2 connector
	Mass Storage	SATA II: Dual Integrated Serial ATA Host Controller (Sil3132) Depending on SATA manufacturing option: - Two ports available on Rear P0 connector or - One port available on Rear P0 connector and one port onboard
	VME	ALMA2f VME controller (2eSST supported)
	FPGA Configurable I/Os	One optional FPGA (using one PMC/XMC slot) with VITA 57 connectivity for customized modules
Sockets	Front Panel Connectors	- SERIAL: one 6-pin RJ-11 connector - Ethernet: two RJ-45 connectors - USB: one 4-pin connector
	Onboard Connectors	- VME Connector P0, P1 and P2 - USB: onboard connector for Flash Disk Module - PMC#1 and XMC#1 connectors - PMC#2 and XMC#2 connectors - FMC connector (VITA 57, using one of the PMC/XMC slot) - JTAG/COP port for emulation probe connection - H8 serial line for test and debug
HW Monitoring	LEDS	System status: - L1, L2, L3, L4 and L5 Gigabit Ethernet status: - SPEED (green): Network Speed - ACT (yellow): Network/Link Activity
	Watchdog	Software configurable dual-stage Watchdog timer with programmable timeout from 125 ms to 256 s, generates IRQ or reset or IRQ/reset cascaded (EPLD implementation)
	RTC	Real Time Clock RV-8546-C2 from Micro-Crystal Switzerland
Software	U-Boot Firmware	Onboard 2 x 32 Mb NOR Flash Memory - Flash-write protection implemented under software control U-Boot features: - QuickBoot - QuietBoot - BootBlock - LAN boot capability for diskless systems (standard PXE) - Boot from USB floppy disk drive - Firmware parameters are saved in the EEPROM - Board serial number is saved within the EEPROM

	VM6250	SPECIFICATIONS
Software	Operating Systems	Operating systems supported: - Fedora 9 Linux - Wind River VxWorks 6.6 RTOS Please contact Kontron for further information concerning other operating systems.
General	Mechanical	6U, VME compliant form factor
	Power Supply	3.3V, 5V, +12V/-12V if required for mezzanine
	Power Consumption	Max. / Typ. MPC8640 1.00 GHz 33W / 27W MPC8640 1.25 GHz 43W / 35W MPC8640D 1.25 GHz 52W / 41W MPC8641D 1.33 GHz 61W / 45W
	Temperature Range	SA environmental class Operational: 0°C to +55°C (air flow: 1.2 to 2.4 m/s depending on processor frequency) Storage: -45°C to +85°C WA environmental class Operational: -20°C to +65°C (air flow: up to 3.0 m/s depending on processor frequency) Storage: -45°C to +85°C RC environmental class Operational: -40°C to +85°C Storage: -45°C to +100°C NOTE: When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the VM6250 (See “Battery" below).
	Climatic Humidity	SA environmental class 90% non-condensin WA environmental class 95% non-condensing RC environmental class 95% non-condensing
	Dimensions	233 mm x 160 mm
	Board Weight	SA environmental class: ~ 430g WA environmental class: ~ 500 g RC environmental class: ~ 700g

	VM6250	SPECIFICATIONS
General	MTBF	Refer to section 1.3.1 “MTBF Data" page 18
	Battery	3.0V battery for RTC with battery socket. Temperature ranges: Operational (load): -40°C to +85°C typical (refer to the battery manufacturer's specifications for exact range) Storage (no load): -55°C to +125°C typical (no discharge)
		Page 4 of 4

Table 6: VM6250 Main Specifications



For a detailed description of the VM6250-RTM (Rear Transition Module), refer to Chapter 6 “VM6250-RTM Characteristics" page 87.

1.3.1 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

VM6250-SA and VM6250-WA

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
VM6250-SA Order Code: VM6250-2SA25-11110 VM6250-WA Order Code: VM6250-2WA25-11110	216 191	161 565	31 071	39 119	34 192	8 505

Table 7: VM6250-SA and VM6250-WA MTBF Data

VM6250-RC

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
VM6250-RC Order Code: VM6250-2RC25-11110	329 216	241 625	48 204	63 832	53 360	11 976

Table 8: VM6250-RC MTBF Data

1.4 Software Support

Kontron is one of the few CompactPCI, VME and VPX vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, customers possessing a maintenance agreement with Kontron Modular Computers can be guaranteed hotline software support and are supplied with regular software updates. A dedicated web site is also provided for online updates and release downloads.

1.5 Standards

This Kontron product complies with the requirements of the following standards.

TYPE	ASPECT	DESCRIPTION
CE	EMC	EN55082 EN55022 Class A
Mechanical	Mechanical Dimensions	IEEE1101.10
Environmental	WEEE	Waste electrical and electronic equipment
	RoHS	Restriction of the use of certain hazardous substances in electrical and electronic equipment

1.6 Environmental Specifications

Version		
SA Standard Commercial	VITA 47 Conformal Coating	Optional
	Airflow	1.2m/s to 2.4/s (depending on the processor frequency)
	Temperature VITA 47-Class AC1 VITA 47-Class C1/C2	Cooling Method: Convection Operating: 0°C to +55°C Storage: -45°C to +85°C
	Vibration Sine (Operating) VITA 47-Class V1	2g / 20-500 Hz acceleration / frequency range
	Shock (Operating) VITA 47-Forced Air Cooled Class	20g / 11ms peak acceleration / shock duration half sine
	Altitude (Operating)	-1,640 to 15,000 ft
	Climatic Humidity	90% non-condensing
WA Air-Cooled Extended Temperature	VITA 47 Conformal Coating	Yes
	Airflow	up to 3.0m/s (depending on the processor frequency)
	Temperature VITA 47-Class AC1 VITA 47-Class C1/C2	Cooling Method: Convection Operating: -20°C to +65°C Storage: -45°C to +85°C
	Vibration Sine (Operating) VITA 47-Class V1	2g / 20-500 Hz acceleration / frequency range
	Shock (Operating) VITA 47-Forced Air Cooled Class	20g / 11ms peak acceleration / shock duration half sine
	Altitude (Operating)	-1,640 to 33,000 ft
	Climatic Humidity	95% non-condensing
RC Rugged Conduction Cooled	VITA Conformal Coating	Yes
	Temperature VITA 47-Class CC4 VITA 47-Class C1/C2	Cooling Method: Conduction Operating: -40°C to +85°C Storage: -45°C to +100°C
	Vibration Sine (Operating) VITA 47-Class V3	5g / 20-2000 Hz acceleration / frequency range
	Shock (Operating) VITA 47-Conduction Cooled Class	40g / 20ms peak acceleration / shock duration half sine
	Altitude (Operating)	-1,640 to 60,000 ft
	Climatic Humidity	95% non-condensing

Table 9: Environmental Specifications

1.7 Related Publications

The following publications contain information relating to this product:

PRODUCT / STANDARD	PUBLICATION
VM6250 Boards	VM6250 Hardware Release Notes CA.DT.A66 VM6250/RC User's Guide Supplement CA.DT.A75 VM6250 PBIT User's Guide SD.DT.F35 VM6250 U-Boot User Manual SD.DT.F36 VM6250 Release Notes Fedora9 SD.DT.F37 VM6250 VxWorks BSP User's Guide SD.DT.F44
CNET	MIL HDBK 217F, CNET RDF93 and CNET RDF2000 Reliability models
EN	EN55082 and EN55022 Class A Electromagnetic compatibility - Generic immunity standard - Industrial environment - Information technology equipment - Radio disturbances characteristics - Mimits and methods of measuremments
IEEE	IEEE Std 1101.2-1992 IEEE Standard for Machanical Core Specifications for Conduction Cooled Eurocards IEEE P1386-2001 Common Mezzanine Card Family CMC IEEE P1386.1-2001 Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)
Intel - Hewlett-Packard - NEC - Dell	IPMI v1.5 Intelligent Platform Management Interface Specification - Document Revision 1.1, february 20, 2002
Serial ATA	Serial ATA 1.0a Specification
VITA	VITA 1-1994 VME64 Specification VITA 1.1-199x VME64 Extension Draft Specification VITA 35-199x PMC-P4 Pin Out Mapping to VME-P0 and VME64x-P2 Draft Standard VITA 31.1-200x Gigabit Ethernet on VME64x Backplane Draft Standard VITA 20-2000x Conduction Cooled PCI mezzanine Card (CCPMC) VITA 38-2003 System Management on VME VITA 47 Environmental, Design and Construction, Safety, and Quality for Plug-In Units VITA 57 FPGA IO Mezzanine Standard
Underwriters Laboratories	UL94-V0 Standard Physical and environmental Mayers for PCI Mezzanine Cards (PMC)

Table 10: Related Publications

Chapter 2 - Functional Description

Refer to following sections for detailed information:

Section 2.1 page 23 **Processor and System Memory**

- Section 2.1.1 page 23 Processor
- Section 2.1.2 page 25 System Memory

Section 2.2 page 25 **PCI-Express Buses**

Section 2.3 page 26 **ALMA2f PCI to VME Bridge**

Section 2.4 page 29 **Storage**

- Section 2.4.1 page 29 Flash Memory
- Section 2.4.2 page 29 Serial EEPROMs
- Section 2.4.3 page 29 SPI EEPROM
- Section 2.4.4 page 29 NOVRAM
- Section 2.4.5 page 29 Dual Serial ATA

Section 2.5 page 30 **Peripherals**

- Section 2.5.1 page 30 Timer
- Section 2.5.2 page 30 Watchdog Timer
- Section 2.5.3 page 30 Power Monitor and Reset Generation

Section 2.6 page 30 **System FPGA**

Section 2.7 page 31 **Connectors Layout**

Section 2.8 page 2.8 **Board Interfaces**

- Section 2.8.1 page 33 Serial Interfaces
- Section 2.8.2 page 34 USB Interfaces
- Section 2.8.3 page 37 Gigabit Ethernet Interfaces
- Section 2.8.4 page 39 SATA Interfaces
- Section 2.8.5 page 40 VME Bus Interface - P0 Connector
- Section 2.8.6 page 42 VME Bus Interface - P1 Connector
- Section 2.8.7 page 46 VME Bus Interface - P2 Connector
- Section 2.8.8 page 48 PMC J11 and J21 Connectors
- Section 2.8.9 page 48 PMC J12 and J22 Connectors
- Section 2.8.10 page 49 PMC J13 and J23 Connectors
- Section 2.8.11 page 49 PMC J14 and J24 Connectors
- Section 2.8.12 page 50 PMC Signal Description
- Section 2.8.13 page 52 XMC J15 and J25 Connectors
- Section 2.8.14 page 53 XMC Signal Description
- Section 2.8.15 page 54 FMC Interface - P4 Connector

Section 2.9 page 55 **PMC Site**

2.1 Processor and Memory

2.1.1 Processor

The VM6250 is built around Freescale's state-of-the-art MPC8641 single or dual-core e600 processor.

Depending on the VM6250 board order code (refer to Table 3 “Order Code Table” page 7), following processor is used:

- Freescale MPC8640 single-core e600 processor @1.0 GHz
- Freescale MPC8640D dual-core e600 processor @1.25 GHz
- Freescale MPC8641D dual-core e600 processor @1.33 GHz



The MPC8640D processor features software, package and pin-for-pin compatibility with the MPC864D processor.
The MPC8640D is a lower power version of the high-performance MPC8641D dual-core processor

The MPC8641D processor includes two e600 cores each having 32 kB L1 instruction cache, 32 kB L1 data cache and 1 MB L2 cache. The processor further provides a DDR2 SDRAM memory controller, a local bus controller (LBC), a programmable interrupt controller (PIC), two I²C controllers, a four-channel DMA controller, and a dual universal asynchronous receiver/ transmitter (DUART). For high-speed interconnect, the MPC8641D provides two sets of multiplexed pins that support two interface standards: 1x/4x Serial RapidIO (with message unit) and 1x/2x/4x/8x/ PCI Express. Furthermore, four integrated 10 Mbit/s, 100 Mbit/s and 1 Gbit/s Ethernet controllers offer TCP offload and classification capabilities. The MPC8641D processor delivers optimized power-efficient computing and outstanding dual-core performance with low power consumption and high system integration.

The MPC8641D processor supports symmetric multiprocessing (SMP) and asymmetric multiprocessing (AMP). SMP allows a platform to run one operating system on both cores. AMP allows a platform to run multiple operating systems and applications on the two cores independently from each other, for example, one real-time optimized operating system is run on the first core while the other core manages non-real-time tasks.

To enhance the CPU performance, each core of the MPC8641D is suited with a 64-bit floatingpoint unit (FPU) and the powerful AltiVec vector processing unit.

The following list sets out some of the key features of the Freescale MPC8641D dual-core processor:

- Two e600 cores with the following characteristics:
  - 32-bit, high-performance, superscalar microprocessor
  - 64-bit floating-point unit (FPU)
  - AltiVec support
  - L1 cache: two separate 32 kB instruction and data caches
  - L2 cache: integrated 1 MB, eight-way set-associative unified instruction and data cache with ECC support
- MPX coherency module (MCM)
- DDR2 memory controller:
  - 64-bit memory controller (72-bit with ECC)
  - Support for up to 600 MHz DDR2 SDRAM
- Serial RapidIO interface:
  - Compliant with the RapidIO Interconnect Specification Revision 1.2
  - 1x and 4x LP-serial link interfaces
  - Transmission rates of 1.25, 2.5 and 3.125 Gbaud (data rates of 1.0, 2.0 and 2.5 Gbps) per lane

- PCI Express interface:
  - Compliant with the PCI Express Base Specification Revision 1.0a
  - Support for x1, x2 and x4 link widths
  - 2.5 Gbaud, 2.0 Gbps lane
- Four identical enhanced three-speed Ethernet controllers (eTSECs):
  - Each TSEC incorporates a media access control sublayer (MAC) that supports 10 Mbps, 100 Mbps and 1 Gbps networks
  - Compliant with IEEE 802.3, 802.3u, 802.3x, 802.3z, 802.3ac and 802.3ab
  - Support of full-duplex FIFO mode for high-efficiency ASIC connectivity
  - TCP/IP Offload
  - Header parsing
  - Quality of service support
  - VLAN insertion and deletion
  - MAC address recognition
- Programmable interrupt controller (PIC) with support for PCI Express message shared interrupts (MSI)
- Local bus controller (LBC)
- Integrated four-channel DMA controller
- Device performance monitor
- Dual I²C controllers
- Dual universal asynchronous receiver/transmitter (DUART):
  - Two 4-wire interfaces (SIN, SOUT, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC 16550D
- IEEE 1149.1-compliant, JTAG boundary scan

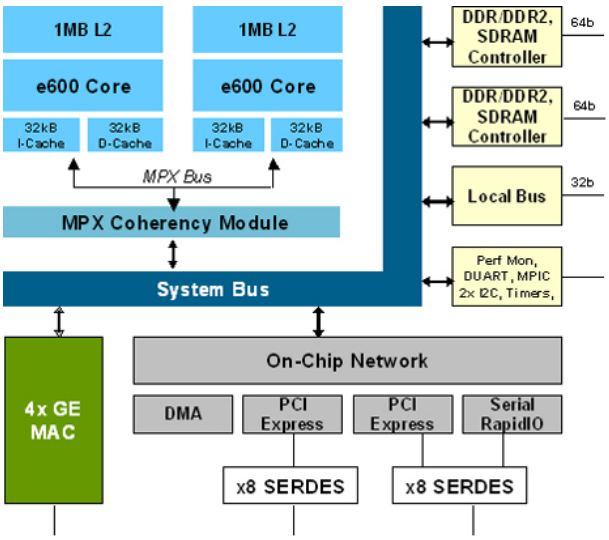


Figure 9: MPC8641D Block Diagram

2.1.2 Memory

The VM6250 supports a single-channel (72-bit), registered Double Data Rate (DDR2) memory with Error Checking and Correcting (ECC) running up to 600 MHz (PC3200). The available memory configuration can be either 1 GB or 2 GB. ECC is able to correct single-bit errors and detect multiple-bit errors.

2.2 PCI-Express Buses

The VM6250 provides two flexible high-speed interfaces each supporting eight lanes, fully compliant with PCI-Express (PCI-E) and Serial RapidIO (sRIO) standards.

In PCI-E mode of operation either a root complex or an endpoint configuration is possible.

The sRIO mode of operation is limited to four lanes which the speed of 1.25 or 2.5 or 3.125 Gbit/s is configurable.

PCI-E bus interface operates at 2.5 Gbps on each lane resulting in a peak bandwidth of 250 MB/s per lane (250 MB/s on receive way and 250 MB/s on transmit way). This bandwidth must be multiplied by the link width for 2x, 4x, 8x links. As an example, the bandwidth of a 4x PCI-E link is 1 GB/s (4x250 MB/s per way).

2.3 ALMA2f PCI to VME Bridge

The ALMA2f PCI to VME bridge is an ASIC/FPGA developed by Kontron. This component is a highly integrated single chip solution to interface the VME64 and the 64-bit PCI bus of the VM6250. Features include a system controller, a bus requester, a master interface, a slave interface, an interrupt handler, an interrupt generator and a 2-channel DMA controller.

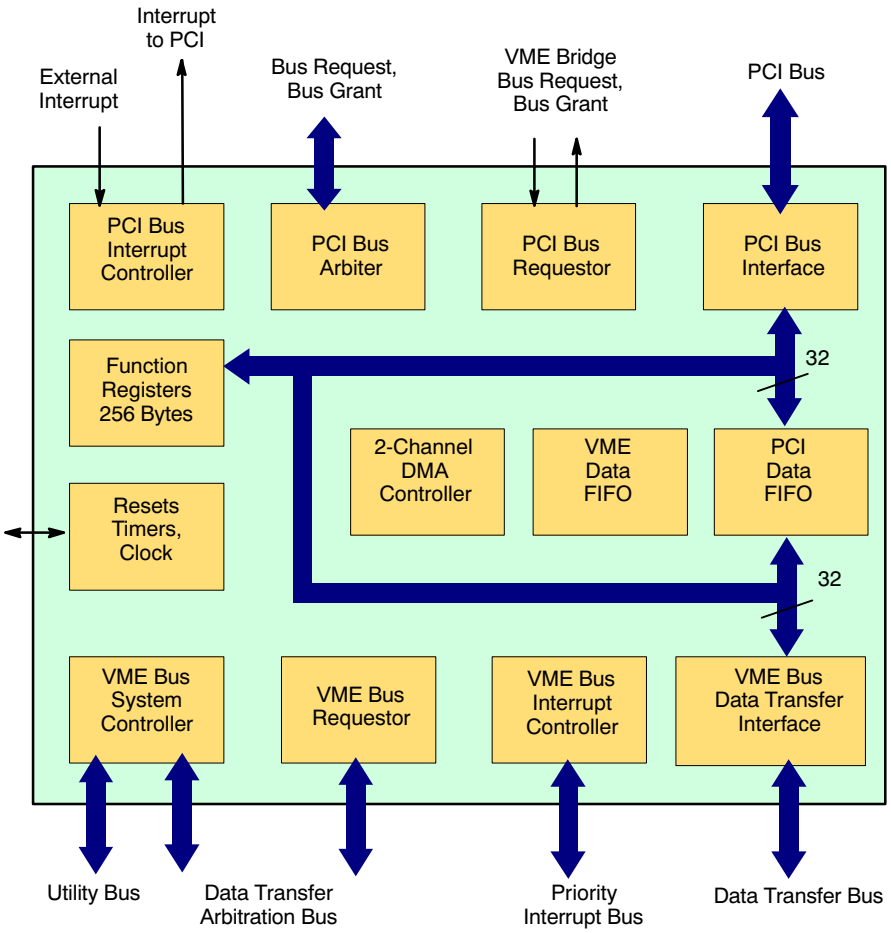


Figure 10: PCI to VME Bridge Block Diagram

ALMA2f main features are:

- Programmable 2eSST support:
  - A32/64 - D64 2eSST
- VME64 master/slave capability
- Full VME system controller and interrupt generator/handlet capacity
- 2eSST capability
- 2 KB data fifo
- Flexible address mapping
- Two DMA channels
- Hardware semaphores for multiprocessing
- ANSI/VITA 1 - 1994 VME64 compliant
- ANSI/VITA 1.1 - 1997 VME64 Extensions

2.3.1 VMEbus Master Access

The VME module provides D32, D16, D8 and UAT under A32, A24 or A16 addressing modes plus D64MBLT and D32BLT under A32 and A24 addressing modes. In addition, the newly introduced ALMA2f VME/PCI bridge features A64 addressing mode for D64BLT, D32BLT and single transfers. All Address Modifier (AM) combinations are supported.

The VME block mode, D64 or D32, can be automatically started from a PCI burst. The use of 2 KB internal FIFOs with programmable thresholds allows maximum speed in decoupled mode (Read-Ahead or Write-Posting). In the same way, since the PCI bus is much faster than the VME bus, even a suite of single PCI write transfers can be translated into VME D32BLT (BB2BLT mode). The ALMA2f VME/PCI bridge improves the MBLT64 transfers that were implemented in the ALMA_V64 VME/PCI bridge.

ALMA2f also introduces the 2eSST standard with data rate up to 180 MB/s peak for the master.

2eSST rate: ALMA2f enables SST160, SST267 and SST320 up to 320 MB/s peak. The 320MB/s VME 2eSST speed is not recommended with the VM6250 board. Depending on your backplane, 2eSST speed has to be adjust to 160 MB/s or 267 MB/s.



Rack Type: 5 rows backplane is mandatory for 2eSST functionality.
Rack Size: 6 slots recommended for now. As one of the key factors is the backplane tracks length, short backplanes are best suited for the 2eSST signals whatever the VME buffer technology.
Backplanes larger than 6 slots can also be used as long as the VME signals can meet the requirement described in rule 3.2 of VITA 1.5--200x.

2.3.2 VMEbus Slave Access

The VME slave interface supports the same addressing mode and data size as the VME master interface. Sixteen decoding channels are available for accessing the PCI bus from the VME bus (ALMA2f doubles the number of VME slave windows implemented in the earlier ALMA_V64). Each channel is independently configurable in the A64, A32, A24 or A16 address space. The 2eSST mode is supported only for the eight additional slave windows. These channels allow the user to program the PCI bus access parameters with a minimum granularity of 1MB.

2.3.3 VMEbus Arbitration

- **VME bus requester:**

  The VME/PCI bridge drives the bus requests on the four levels, BR0 to BR3 and the release of the bus can be managed with ROR (Release On Request), ROC (Release On Clear) or RNE (Release NEver) policy.

- **VME System Controller:**

  The VM6250 board is VME system controller when the board is fitted in slot 0 or if it is the first board of the bus grant daisy chain. The system controller mode is automatically detected (Auto System Controller).

- **VM6250 Identification on the VMEbus:**

  Each SBC in a rack or station must have an unique identification on the VME bus. This ID depends on the setting of the board into the VME rack and is used to calculate two VME base addresses to reach the PCI/VME bridge internal registers and the VM6250 SDRAM, respectively. The value of the VME BOARD ID, is stored in the serial access EEPROM.

2.3.4 DMA Channels

Two DMA channels are available to the user. The priority between channels is programmable and blocks may be interlaced or not. DMA completion can be signalled via an interrupt to the PCI bus.

2.3.5 Interrupt Management

The VME/PCI bridge Interrupt Controller can handle different interrupt sources:

- 7 VME interrupts (IRQ7*-IRQ1*),
- 8 mail box interrupts (they occur when a specific 8-bit register is addressed in write mode from the PCI or the VME),
- ACFAIL* and SYSFAIL* on VMEbus,
- internal exceptions (end of DMA, error acknowledges on PCI bus or VME bus, VMEbus arbitration timeout, ...).

All these interrupts can be masked and can drive either the INTA PCI bus interrupt which is the dedicated PCI interrupt pin, or any of the three programmable interrupt pins (INT1 to INT3).

2.4 Storage

2.4.1 Flash Memory

There are three Flash devices available as described below, two for the NetBootLoader and one for the NAND Flash Disk Controller.

2.4.1.1 NAND Flash

The VM6250 supports up to 8 GB of USB NAND Flash memory

2.4.1.2 Firmware Flash

The VM6250 provides two 32 Mb, redundant Firmware Flash (MirrorBit® NOR Flash) chips (for U-Boot firmware).

The fail-over mechanism for the Firmware recovery can be controlled via the SW2 DIP switch. If one Firmware Flash is corrupted, the second Firmware Flash can be enabled and boot the system again.

2.4.2 Serial EEPROMs

There are two 256-kbit onboard serial EEPROMs:

- One is used to store the Operating System boot parameters and user data and is connected to the I^2C controller.
- One is used to store system information (serial number, board configuration parameters, ...) and is connected to the FPGA.

2.4.3 SPI EEPROM

Serial EEPROM using the Serial Peripheral Interface (SPI) protocol.

2.4.4 NOVRAM

A 128 KB NOVRAM (NOnVolatile Random Access Memory) is implemented.

During standard operations, software applications read and write in the autostore NOVRAM just like in a standard SRAM.

Upon detection of a power loss, an autostore cycle is performed and all the 128 KB are automatically moved from the onchip SRAM to the onchip EEPROM using the energy stored in an onboard capacity.

At the next system power up, a recall cycle is performed to dump the EEPROM contents back to the SRAM.

The number of recall cycles is unlimited. The maximum of store cycles is 500 00, and the data retention period is 20 years at maximum temperature (+85°C).

A hardware jumper is provided to disable write cycles to this device.

2.4.5 Dual Serial ATA

Depending on the SATA manufacturing option, either:

- Two Serial ATA II (SATA II - 3 Gbps) ports are available on P0 connector.
- One Serial ATA II (SATA II - 3 Gbps) port is available on P0 connector, and one Serial ATA II port is available onboard.

Refer to section 2.8.5 “VME Bus Interface - P0 Connector” page 40 for more information on P0 pin assignment.

2.5 Peripherals

The following standard peripherals are available on the VM6250 board:

2.5.1 Timer

The VM6250 is equipped with the following timers:

- Real-Time Clock (RTC)

  The VM6250 is equipped with an onboard high-precision real-time clock RV-8564-C2. The RV-8564-C2 RTC is register-compatible with the PCF8564A RTC from Philips/NXP. Additionally, it provides a very tight frequency tolerance at low power consumption. The VM6250 does not include a 3 V lithium battery or a GoldCap power source for RTC backup. The RTC can be powered from the management power. However, if this power is switched off, the RTC will lose its data.

- Hardware delay timer for short reliable delay times

2.5.2 Watchdog Timer

The VM6250 provides a Watchdog Timer that is programmable for a timeout period ranging from 125 ms to 256 s in 12 steps. Failure to trigger the Watchdog Timer in time results in an interrupt or a system reset. In the dual-stage mode, a combination of both interrupt and reset is generated if the Watchdog is not serviced. A hardware status flag will be provided to determine if the Watchdog Timer generated the reset.

2.5.3 Power Monitor and Reset Generation

All onboard voltages on the VM6250 are supervised, which guarantees controlled power-up of the board. This is done by activating a stable power-up reset signals after the threshold voltages have been passed.

2.6 System FPGA

The following functions are implemented in the CPLD device:

- CPU reset configuration
- Board reset control
- Board registers
- LED control port
- Watchdog timer
- Delay timer
- Ethernet PHY configuration
- Serial hardware debug port
- I^2C master interface

2.7 Connectors Layout

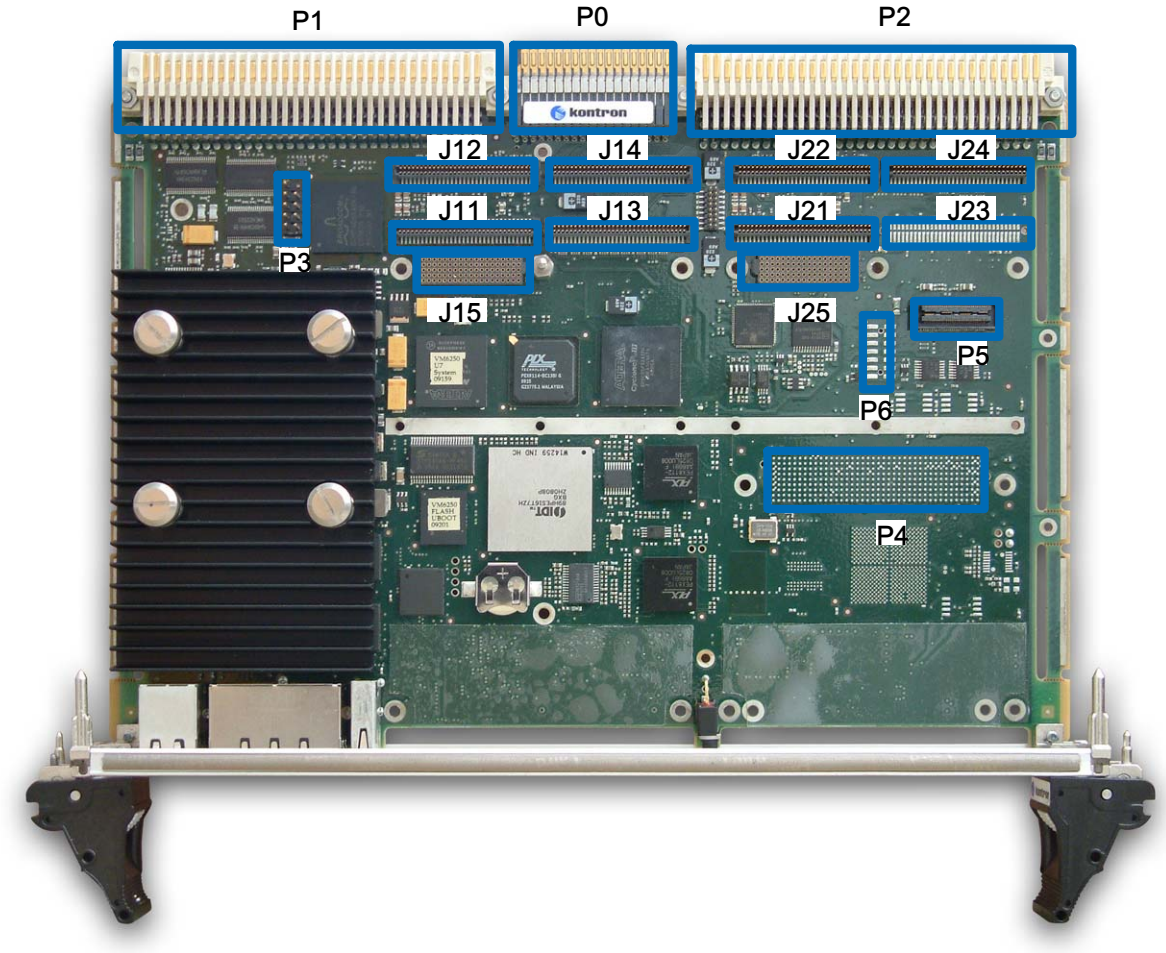


Figure 11: Connector Layout (Top View)

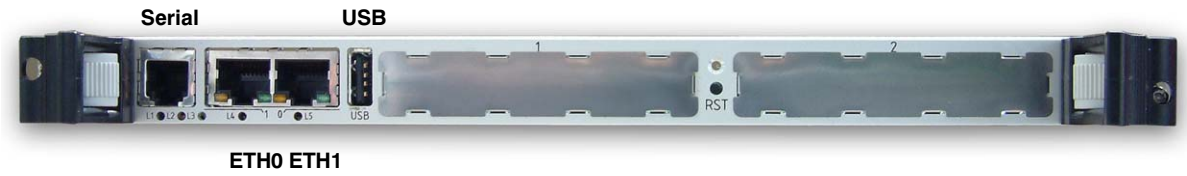


Figure 12: Front Panel Connector Layout

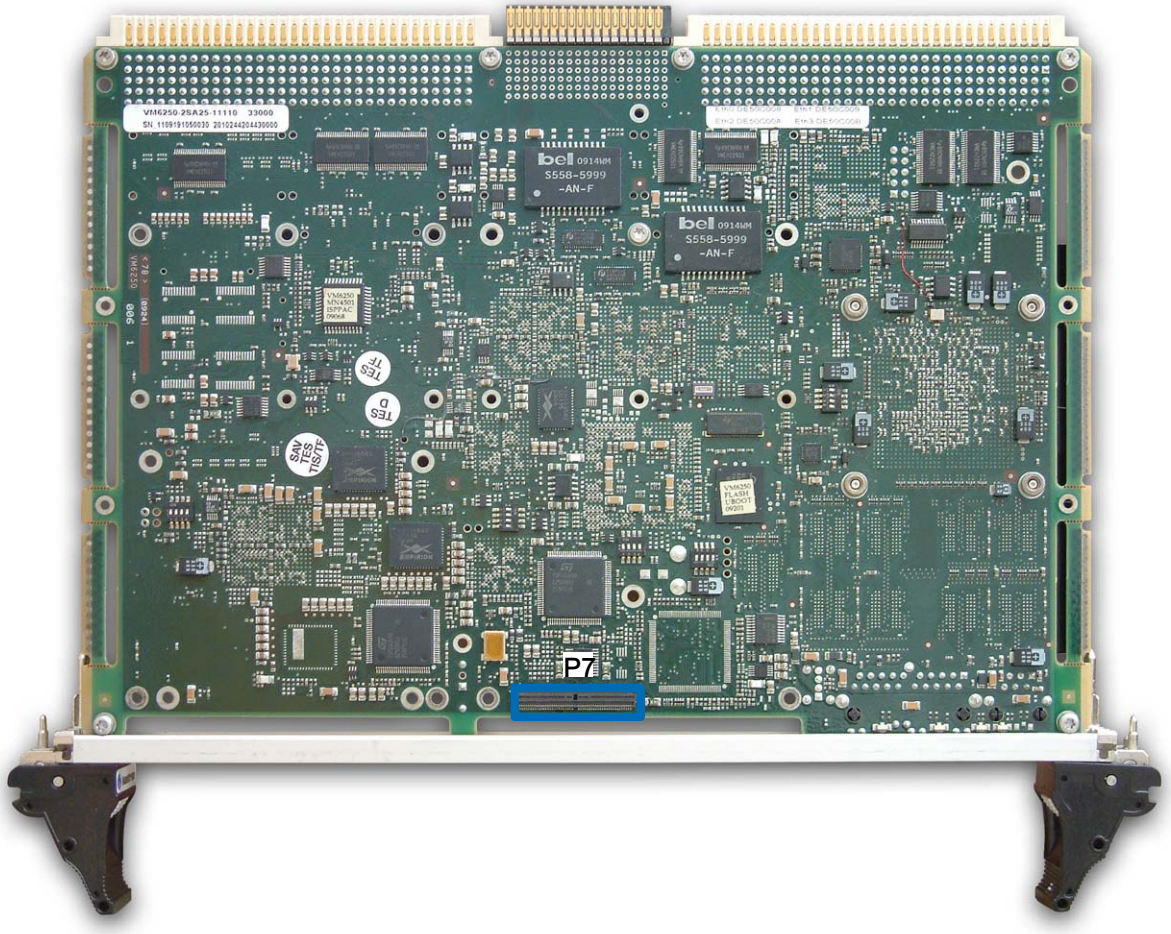


Figure 13: Connector Layout (Bottom View)

Refer to following sections for detailed information:

- Section 2.8.1 page 33 — Serial Interfaces
- Section 2.8.2 page 34 — USB Interfaces (P3 on pictures below)
- Section 2.8.3 page 37 — Gigabit Ethernet Interfaces (ETH0 ETH1 on pictures below)
- Section 2.8.4 page 39 — SATA Interfaces (P5 on pictures below)
- Section 2.8.5 page 40 — VME Bus Interfaces - P0 Connector
- Section 2.8.6 page 42 — VME Bus Interfaces - P1 Connector
- Section 2.8.7 page 46 — VME Bus Interfaces - P2 Connector
- Section 2.8.8 page 48 — PMC J11 and J21 Connector
- Section 2.8.9 page 48 — PMC J12 and J22 Connector
- Section 2.8.10 page 49 — PMC J13 and J23 Connector
- Section 2.8.11 page 49 — PMC J14 and J24 Connector
- Section 2.8.13 page 52 — XMC J15 and J25 Connector
- Section 2.8.15 page 54 — FMC Interface (P4 and P6 on pictures below)

2.8 Board Interfaces

2.8.1 Serial Interfaces

The VM6250 supports two serial EIA-232 simplified interfaces available:

- COM1: EIA-232 (simplified) port on RJ-12 front panel connector or on the rear P2 connector
- COM2: EIA-232 (simplified) port on RJ-12 front panel connector or on the rear P2 connector

Refer to section 2.8.7 “VME Bus Interface - P2 Connector” page 46 for more information on the serial lines pin assignment on P2 connector.

Serial Front Panel

Pin	Signal	Description
1	COM2 TXD	COM2 EIA-232 Transmit Data
2	Shell	Chassis Ground
3	COM1 TXD	COM1 EIA-232 Transmit Data
4	COM1 RXD	COM1 EIA-232 ReceiveData
5	GND	Ground
6	COM2 RXD	COM2 EIA-232 Receive Data

Table 11: Serial Connector Pinout

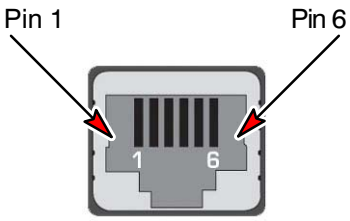


Figure 14: Serial Connector

Serial Cable Designation

Serial cable:

- RJ-14 (6-pin, 4-conductor): simplified EIA-232 on COM1
- RJ-12 (6-pin, 6-conductor): simplified EIA-232 on COM1 and COM2

- Use of a cable type RJ-12 (6-pin, 6-conductor), implies that COM1 and COM2 serial lines must be used from the Serial front panel. .
- Use of a cable type RJ-14 (6-pin, 4-conductor), lets COM2 serial line available on P2 connector.

A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

Kontron provides a specific connection kit Order Code: KIT-RJ12DB9.

It includes RJ-12 cable and a DB9 female adapter.



2.8.2 USB Interfaces

The VM6250 supports four USB 2.0 ports:

- one on the front panel
- one onboard to connect a flash disk module
- two on the rear P0 connector

On the USB 2.0 front panel port, USB cable with up to 1.8 meters in length can be used.

On the USB 2.0 Rear I/O ports, it is strongly recommended to use a cable below 1.8 meters in length for USB 2.0 devices.

The USB 2.0 ports are high-speed, full-speed, and low-speed capable. Hi-speed USB 2.0 allows data transfers of up to 480 Mb/s - 40 times faster than a full-speed USB (USB 1.1).

One USB peripheral may be connected to each port.

To connect more USB devices than there are available ports, an external hub is required.

Refer to section 2.8.5 “VME Bus Interface - P0 Connector” page 46 for more information on the serial lines pin assignment on P2 connector.

USB Front Panel

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	USB1_D-	Differential USB-	I/O
3	USB1_D+	Differential USB+	I/O
4	GND	GND	--

Table 12: USB Connector Pinout

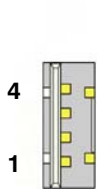


Figure 15: USB Connector



The VM6250 host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

USB onboard

The onboard USB device (P3 connector) is used to connect an USB flash disk module. The following figure and table provide pinout information for the onboard USB connector P3:

PIN	SIGNAL	FUNCTION	I/O
1	USB0_PWR	VCC	--
2	N.C.	Not Connected	--
3	USB0_D-	Differential USB-	I/O
4	N.C.	Not Connected	--
5	USB0_D+	Differential USB+	I/O
6	N.C.	Not Connected	--
7	GND	GND	--
8	N.C.	Not Connected	--
9	N.C.	Not Connected	--
10	N.C.	Not Connected	--

Table 13: USB onboard P3 Pinout

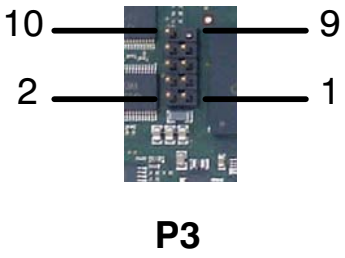


Figure 16: USB onboard Connector

The USB Flash module is fixed to the board, by using on one side the P3 connector, and on the other side, a standoff screwed to the VM6250 board and to the USB Flash module.

Order Code for the USB flash disk:

FDM-USB-*x*GB-L2-IV: industrial version with conformal coating (*x* GB)

Contact Kontron for available capacity.

> USB Flash Disk Layout

- Maximum space reserved for USB flash disk is 50 mm x 30 mm (LxW)
- The distance between connector and screw hole is 27.3 mm~27.9mm
- Maximum allowable connector height is 9.78 mm

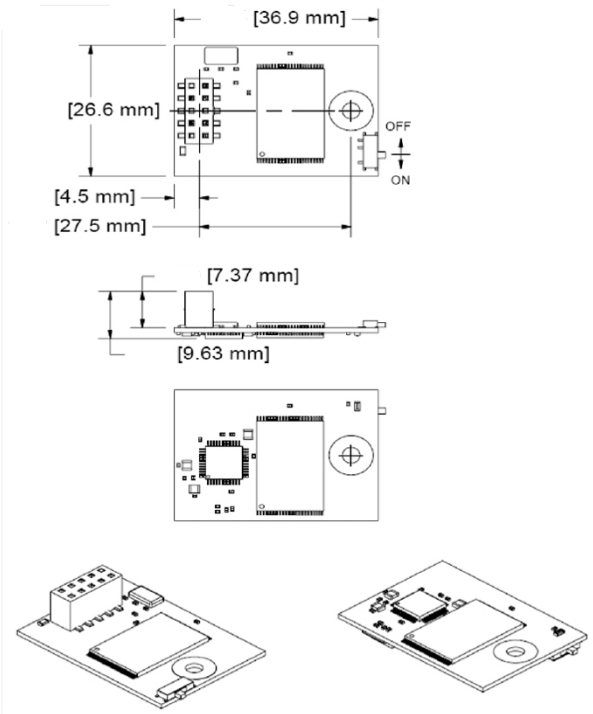


Figure 17: USB Flash Disk Overview

2.8.3 Gigabit Ethernet Interfaces

The Freescale MPC864x processor integrates four Triple-Speed Ethernet controllers which are associated on the VM6250 board with an external BCM5466R quad Gigabit Ethernet PHY.

The Ethernet channels 0 and 1 are routed to the front panel RJ-45 connectors, configured to be 1000BASE-T by default.

The Ethernet channels 2 and 3 are routed to the P0 connector.

Refer to section 2.8.5 “VME Bus Interface - P0 Connector” page 46 for more information on the gigabit ethernet pin assignment on P2 connector.

» Front Panel Gigabit Ethernet

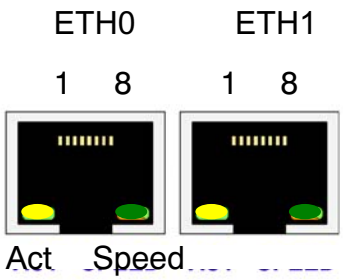


Figure 18: Dual Gigabit Ethernet Connector



The Ethernet transmission can operate effectively using a CAT5 cable with a maximum length of 100 m.

The Ethernet connectors are realized as RJ-45 connectors. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

2.8.3.1 ETH0 and ETH1 Pinouts

The ETH0 / ETH1 connectors supply the 10Base-T, 100Base-TX and 1000Base-T interfaces to the Ethernet controller.

PIN	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC-
6	I	TX-	I	RX-	I/O	BI_DB-
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD-

Table 14: Gigabit Ethernet Connectors ETH0 and ETH1 Pinout

2.8.3.2 Ethernet LED Status

» ACT (yellow)

This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

» SPEED (green)

STATUS		SPEED LED green	ACT LED yellow
Ethernet link is not established		OFF	OFF
10/100 Mbps	Ethernet link establisehd	OFF	ON
	Ethernet Link Activity	OFF	BLINK
1000 Mbps	Ethernet link establisehd	ON	ON
	Ethernet Link Activity	ON	BLINK

Table 15: Ethernet LEDs Status Definition

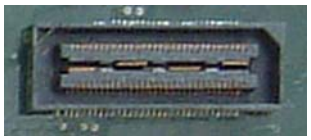
2.8.4 SATA Interface

This interface is available only on the boards featuring the **SATA onboard** manufacturing option. In such a configuration, only one SATA II port will be available on rear P0 connector.

The onboard SATA device (P5 connector) is used to connect a SATA HDD. The following table provides pinout information for the onboard SATA connector P5:

PIN	SIGNAL	FUNCTION	I/O
GND1 ... GND4	GND	Ground Signal	-
1	GND	Ground Signal	-
2 .. 6	N.C.	Not Connected	-
7	GND	Ground Signal	-
8 .. 12	N.C.	Not Connected	-
13	GND	Ground Signal	-
14	N.C.	Not Connected	-
15	SATA1 RX-	Differential Receive -	I
16	GND	Ground Signal	-
17	SATA1 RX+	Differential Receive +	I
18	+5V		-
19	GND	Ground Signal	-
20	+5V		-
21	SATA1 TX+	Differential Transmit +	O
22	+5V		-
23	SATA1 TX-	Differential Transmit -	O
24 .. 25	GND	Ground Signal	-
26	+3.3V		-
27	N.C.	Not Connected	-
28	+3.3V		-
29 .. 60	N.C.	Not Connected	-

Table 16: SATA onboard P5 Pinout



P5

Figure 19: SATA onboard Connector

2.8.5 VME Bus Interface - P0 Connector

2.8.5.1 P0 Connector Pin Assignment

Pin	P0 connector					
	Row a	Row b	Row c	Row d	Row e	Row f (2)
1	PMC1 IO 39 (1)	PMC1 IO 38 (1)	PMC1 IO 37 (1)	PMC1 IO 36 (1)	PMC1 IO 35 (1)	GND
2	ETH2 BI_DA+	ETH2 BI_DA-	GND	ETH2 BI_DC+	ETH2 BI_DC-	GND
3	ETH2 BI_DB+	ETH2 BI_DB-	GND	ETH2 BI_DD+	ETH2 BI_DD-	GND
4	ETH3 BI_DA+	ETH3 BI_DA-	GND	ETH3 BI_DC+	ETH3 BI_DC-	GND
5	ETH3 BI_DB+	ETH3 BI_DB-	GND	ETH3 BI_DD+	ETH3 BI_DD-	GND
6	RST_BP#	USB3 PWR	ISP_PAC_RST #	Reserved	USB2 PWR	GND
7	USB3 DA+	USB3 DA-	GND	USB2 DA+	USB2 DA-	GND
8	SATA0 TX+	SATA0 TX-	GND	SATA0 RX+	SATA0 RX-	GND
9	SATA1 TX+ (3)	SATA1 TX- (3)	GND	SATA1 RX+ (3)	SATA1 RX- (3)	GND
10	PMC1 IO 34 (1)	PMC1 IO 33 (1)	GPIO1	GPIO2	GPIO3	GND
11	PMC1 IO 58	PMC1 IO 60	PMC1 IO 46	PMC1 IO 48	PMC1 IO 50	GND
12	PMC1 IO 62	PMC1 IO 64	PMC1 IO 45	PMC1 IO 52	PMC1 IO 54	GND
13	PMC1 IO 61	PMC1 IO 63	PMC1 IO 56	PMC1 IO 51	PMC1 IO 53	GND
14	PMC1 IO 57	PMC1 IO 59	PMC1 IO 55	PMC1 IO 47	PMC1 IO 49	GND
15	PEX RXL0+	PEX RXL0-	GND	PEX TXL0+	PEX TXL0-	GND
16	PEX RXL1+	PEX RXL1-	GND	PEX TXL1+	PEX TXL1-	GND
17	PEX RXL2+	PEX RXL2-	GND	PEX TXL2+	PEX TXL2-	GND
18	PEX RXL3+	PEX RXL3-	GND	PEX TXL3+	PEX TXL3-	GND
19	PMC1 IO 44 (1)	PMC1 IO 43 (1)	PMC1 IO 42 (1)	PMC1 IO 41 (1)	PMC1 IO 40 (1)	GND

(1) In the column 1, 10 and 19, they may be signals or Not Connected (N.C.). The default is the signals listed. The N.C. option is made available by removing three, 0-ohm resistor packs. Please contact Kontron for more information on this topic.

(2) The **f** row is the metal shielded on the outside P0 connector.

(3) These signals are Not Connected (N.C.) for boards featuring the **onboard SATA** manufacturing option. In such configurations, the 2nd SATA device is available onboard.

Table 17: P0 Connector Pin Assignment

2.8.5.2 P0 Signal Description

Mnemonic	Legend	Signal Description
ETH*x* BI_DA+/-		Ethernet *x*: First pair of Transmit/Receive data.
ETH*x* BI_DB+/-		Ethernet *x*: Second pair of Transmit/Receive data.
ETH*x* BI_DC+/-		Ethernet *x*: Third pair of Transmit/Receive data.
ETH*x* BI_DD+/-		Ethernet *x*: Fourth pair of Transmit/Receive data.
GND		Ground
GPIO*x*		General Purpose I/O *x*
ISP_PAC_RST		Power Supply Reset Signal
PEX RXL*y*+/-		x4 PCI Express (or Serial Rapid IO) Link - Receive+/- Lane *y*
PEX TXL*y*+/-		x4 PCI Express (or Serial Rapid IO) Link - Transmit+/- Lane *y*
PMC1 IO *yy*		PMC Site #1 I/0 signal *yy*
Reserved		Reserved (do not use)
RST_BP		Board Reset Signal
SATA*x* RX+/RX-		Serial ATA *x* Receive +/-
SATA*x* TX+/TX-		Serial ATA *x* Transmit +/-
USB*x* DA+/-		Differential Data Pair of USB Line *x*
USB*x* PWR		USB Line *x*

Table 18: P0 Signal Description

2.8.6 VME Bus Interface - P1 Connector

2.8.6.1 P1 and P2 Row B (VMEbus) Connector Pin Assignment

Pin	P1					P2
	Row z	Row a	Row b	Row c	Row d	Row b
1	N.C.	D00	BBSY*	D08	+5V	+5V
2	GND	D01	BCLR*	D09	GND	GND
3	N.C.	D02	ACFAIL*	D10	N.C.	RETRY*
4	GND	D03	BG0IN*	D11	N.C.	A24
5	N.C.	D04	BG0OUT*	D12	N.C.	A25
6	GND	D05	BG1IN*	D13	N.C.	A26
7	N.C.	D06	BG1OUT*	D14	N.C.	A27
8	GND	D07	BG2IN*	D15	N.C.	A28
9	N.C.	GND	BG2OUT*	GND	GAP* (1)	A29
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0* (1)	A30
11	N.C.	GND	BG3OUT*	BERR*	GA1* (1)	A31
12	GND	DS1*	BR0*	SYSRESET*	+3.3V	GND
13	N.C.	DS0*	BR1*	LWORD*	GA2* (1)	+5V
14	GND	WRITE*	BR2*	AM5	+3.3V	D16
15	N.C.	GND	BR3*	A23	GA3* (1)	D17
16	GND	DTACK*	AM0	A22	+3.3V	D18
17	N.C.	GND	AM1	A21	GA4* (1)	D19
18	GND	AS*	AM2	A20	+3.3V	D20
19	N.C.	GND	AM3	A19	SMB_SCL	D21
20	GND	IACK*	GND	A18	+3.3V	D22
21	N.C.	IACKIN*	IPMB_SCL	A17	SMB_SDA	D23
22	GND	IACKOUT*	IPMB_SDA	A16	+3.3V	GND
23	N.C.	AM4	GND	A15	SMB_ALERT	D24
24	GND	A07	IRQ7*	A14	+3.3V	D25
25	N.C.	A06	IRQ6*	A13	N.C.	D26
26	GND	A05	IRQ5*	A12	+3.3V	D27
27	N.C.	A04	IRQ4*	A11	N.C.	D28
28	GND	A03	IRQ3*	A10	+3.3V	D29
29	N.C.	A02	IRQ2*	A09	N.C.	D30
30	GND	A01	IRQ1*	A08	+3.3V	D31
31	N.C.	-12V	+5V_STAND BY	+12V	GND	GND
32	GND	+5V	+5V	+5V	+5V	+5V

* VME signals active when low.

(1) Geographical address pins, refer to section 2.8.6.2 page 43 for more information.

Table 19: P1 and P2 (Row B) Connector Pin Assignment



Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, ***toxic fumes*** may be produced due to the destruction of components. Only use the VM6250 in VME IEEE1014x or VME64 backplanes that supply power on both P1 and P2 connectors. Failure to observe this warning may result in damage to the board.

2.8.6.2 Geographical Address Pin Assignment

The 6 geographical address pins (GA0*, GA1*, GA2*, GA3*, GA4* and GAP*) shall be tied to ground or left open (floating) on the backplane J1 connector as defined in the table below.

Slot Number	GAP* Pin	GA4* Pin	GA3* Pin	GA2* Pin	GA1* Pin	GA0* Pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

The device that samples the levels of the geographical address pins will read the inverted value of the slot number into which the board is plugged. When the board is powered on without being plugged into a VME/VME64 backplane the slot number will be zero with a parity error (GAP* open).

2.8.6.3 VMEbus Signal Description

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector.

Mnemonic	Signal Description
A01 to A15	**Address Bus (bits 1 to 15)**. Address lines that are used to broadcast a short, standard or extended address.
A16 to A23	**Address Bus (bits 16 to 23)**. Address lines that are used in conjunction with A01-A15 to broadcast a standard or extended address.
A24 to A31	**Address Bus (bits 24 to 31)**. Address lines that are used in conjunction with A01-A23 to broadcast an extended address.
ACFAIL*	**AC Failure**. This signal indicates when the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met.
AM0 to AM5	**Address Modifier (bits 0 to 5)**. These signals are used to broadcast information such as the address size, cycle type, master identification or any combination of these.
AS*	**Address Strobe**. This signal indicates when a valid address has been placed on the address bus.
BBSY*	**Bus Busy**. This signal is driven low by the requester associated with the current bus master to indicate that its master is using the bus.
BCLR*	**Bus Clear**. This signal is generated by an arbiter to indicate that there is a higher priority request for the bus than the one being processed. This signal requests the current master to release the bus.
BERR*	**Bus Error**. This signal is generated by a slave or bus timer to tell the master that the data transfer was not completed.
BG0IN* to BG3IN*	**Bus Grant (0 to 3) In**. These signals are generated by the arbiter to tell the board receiving it that if it is requesting the bus on that level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BGxIN*/BGxOUT* signals form the bus grant daisy chain, i.e. the BGxOUT* of one board forms the BGxIN* of the next board in the daisy chain.
BG0OUT* to BG3OUT*	**Bus Grant (0 to 3) Out**. These signals are generated by requesters to tell the next board in the daisy chain that if it is requesting the bus on that level, then it may use the bus. Otherwise the board should pass the signal down the daisy chain.
BR0* to BR3*	**Bus Request (0 to 3)**. A low level, generated by a requester, on one of these lines, shows that some master needs to use the bus.
D00 to D31	**Data Bus (0 to 31)**. These signals are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers.
DS0*, DS1*	**Data Strobe 0, 1**. These signals are used with LWORD* and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows that data has been accepted from the data bus.
DTACK*	**Data Transfer Acknowledge**. This signal is generated by a slave. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle.

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Mnemonic	Signal Description
GA0* to GA4* and GAP*	Geographical address pins (refer to the table in section 2.8.6.2). These pins indicate to the VME board which one of the backplane slot it currently uses (0 to 21).
GND	The DC voltage reference for the system.
IACK*	**Interrupt Acknowledge**. This signal is used by the interrupt handler to acknowledge an interrupt request. It is routed to the IACKIN* pin of slot 1, where it is monitored by the IACK daisy chain driver.
IACKIN*	**Interrupt Acknowledge In**. This signal tells the board receiving it that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN*/IACKOUT* form the interrupt acknowledge daisy chain.
IACKOUT*	**Interrupt Acknowledge Out**. This signal is sent by a board to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress.
IPMB_SCL	**Intelligent Platform Management Bus** - Clock I2C
IPMB_SDA	**Intelligent Platform Management Bus** - Data I2C
IRQ1* to IRQ7*	**Interrupt Request (1 to 7)**. These signals are driven low by interrupters to request an interrupt on the corresponding level.
LWORD*	**Longword**. This signal is used with DS0*, DS1* and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer.
N.C.	This pin is not connected.
SMB_ALERT*	**System Management Bus** - Alert
SMB_SCL	**System Management Bus** - Serial clock line from the SMBus master to SMBus slave devices.
SMB_SDA	**System Management Bus** - Bi-directional serial data line between the SMBus master and the SMBus slave device.
SYSCLK	**System Clock**. This signal provides a constant 16 MHz clock signal that is independent of any other bus timing.
SYSFAIL*	**System Fail**. This signal shows that a failure has occurred in the system. It can be generated by any board in the system. It is also asserted after a reset and released when the board reset self-tests are passed successfully.
SYSRESET*	**System Reset**. When this signal is low, it causes the system to be reset.
WRITE*	**Write**. This signal is generated by a master to show whether the data transfer cycle is a read or a write.
+3.3V	+3.3 Volts DC power.
+5V	+5 Volts DC power
+12V	+12 Volts DC power.
-12V	-12 Volts DC power.

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Table 20: VME Signal Description

2.8.7 VME Bus Interface - P2 Connector

2.8.7.1 P2 Connector Pin Assignment

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector. Refer to section 2.8.6.1 page 42 for a detailed description of the row b of the P2 connector.

Pin	Row z	Row a	Row c	Row d
1	PMC1 IO 02	PMC2 IO 02	PMC2 IO 01	PMC1 IO 01
2	GND	PMC2 IO 04	PMC2 IO 03	PMC1 IO 03
3	PMC1 IO 05	PMC2 IO 06	PMC2 IO 05	PMC1 IO 04
4	GND	PMC2 IO 08	PMC2 IO 07	PMC1 IO 06
5	PMC1 IO 08	PMC2 IO 10	PMC2 IO 09	PMC1 IO 07
6	GND	PMC2 IO 12	PMC2 IO 11	PMC1 IO 09
7	PMC1 IO 11	PMC2 IO 14	PMC2 IO 13	PMC1 IO10
8	GND	PMC2 IO 16	PMC2 IO 15	PMC1 IO12
9	PMC1 IO 14	PMC2 IO 18	PMC2 IO 17	PMC1 IO 13
10	GND	PMC2 IO 20	PMC2 IO 19	PMC1 IO 15
11	PMC1 IO 17	PMC2 IO 22	PMC2 IO 21	PMC1 IO 16
12	GND	PMC2 IO 24	PMC2 IO 23	PMC1 IO 18
13	PMC1 IO 20	PMC2 IO 26	PMC2 IO 25	PMC1 IO 19
14	GND	PMC2 IO 28	PMC2 IO 27	PMC1 IO 21
15	PMC1 IO 23	PMC2 IO 30	PMC2 IO 29	PMC1 IO 22
16	GND	PMC2 IO 32	PMC2 IO 31	PMC1 IO 24
17	PMC1 IO 26	PMC2 IO 34	PMC2 IO 33	PMC1 IO 25
18	GND	PMC2 IO 36	PMC2 IO 35	PMC1 IO 27
19	PMC1 IO 29	PMC2 IO 38	PMC2 IO 37	PMC1 IO 28
20	GND	PMC2 IO 40	PMC2 IO 39	PMC1 IO 30
21	PMC1 IO 32	PMC2 IO 42	PMC2 IO 41	PMC1 IO 31
22	GND	PMC2 IO 44	PMC2 IO 43	S0_TX
23	S1_TX	PMC2 IO 46	PMC2 IO 45	S0_RX
24	GND	PMC2 IO 48	PMC2 IO 47	S0-RTS
25	S1_RX	PMC2 IO 50	PMC2 IO 49	S0_CTS
26	GND	PMC2 IO 52	PMC2 IO 51	RFU
27	S1-RTS	PMC2 IO 54	PMC2 IO 53	RFU
28	GND	PMC2 IO 56	PMC2 IO 55	RFU
29	S1-CTS	PMC2 IO 58	PMC2 IO 57	RFU
30	GND	PMC2 IO 60	PMC2 IO 59	RFU
31	RFU	PMC2 IO 62	PMC2 IO 61	GND
32	GND	PMC2 IO 64	PMC2 IO 63	+5V

* Signals active when low.

Table 21: P2 Connector Pin Assignment

2.8.7.2 P2 Signal Description

The VME signals (row b) are described in section 2.8.6.3.

Mnemonic	Legend	Signal Description
GND		Ground
PMC *x* IO yy		PMC Site *x* I/O signal *yy*
RFU		Reserved for Future Use (serial lines)
S*x*_CTS		Channel EIA-232 *x* - Clear-To-Send
S*x*_RTS		Channel EIA-232 *x* - Ready-To-Send
S*x*_RX		Channel EIA-232 *x* - Receive Data
S*x*_TX		Channel EIA-232 *x* - TransmitData
+5V		+5 Volts DC power

Table 22: P2 Signal Description

2.8.8 PMC J11 and J21 Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	N.C.	17	REQ#	33	FRAME#	49	AD[09]
2	-12V	18	+5V	34	GND	50	+5V
3	GNG	19	V(I/0) (1)	35	GND	51	GND
4	INTA#	20	AD[31]	36	IRDY#	52	C/BE0#
5	INTB#	21	AD[28]	37	DEVSEL#	53	AD[06]
6	INTC#	22	AD[27]	38	.+5V	54	AD[05]
7	BUSMODE1#	23	AD[25]	39	PCIXCAP	55	AD[04]
8	+5V	24	GND	40	LOCK#	56	GND
9	INTD#	25	GND	41	SDONE#	57	V(I/O) (1)
10	N.C.	26	C/BE3#	42	SBO#	58	AD[03]
11	GND	27	AD[22]	43	PAR	59	AD[02]
12	+3.3V_SUS	28	AD[21]	44	GND	60	AD[01]
13	CLK	29	AD[19]	45	V(I/O) (1)	61	AD[00]
14	GND	30	+5V	46	AD[15]	62	+5V
15	GND	31	V(I/0) (1)	47	AD[12]	63	GND
16	GNT#	32	AD[17]	48	AD[11]	64	REQ64#

(1) V(I/O) is 3.3V only. Neither PMC site provides a 3.3V keying pin

PCI signals active when low.

Table 23: PMC J11 and J21 Conne4ctor Pin Assignment

2.8.9 PMC J12 and J22 Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+12V	17	N.C.	33	GND	49	AD[08]
2	N.C.	18	GND	34	IDSEL B (1)	50	+3.3V
3	Pulled to +3.3V via 10K	19	AD[30]	35	TRDY#	51	AD[07]
4	Pulled to +3.3V via 10K	20	AD[29]	36	+3.3V	52	REQ B# (1)
5	Pulled to +3.3V via 10K	21	GND	37	GND	53	+3.3V
6	Ground	22	AD[26]	38	STOP#	54	GNT B# (1)
7	GND	23	AD[24]	39	PERR#	55	PMC-RSVD
8	N.C.	24	+3.3V	40	GND	56	GND
9	N.C.	25	IDSEL	41	+3.3V	57	PMC-RSVD
10	N.C.	26	AD[23]	42	SERR#	58	EREADY
11	Pulled to +3.3V via 2.7K	27	+3.3V	43	C/BE1#	59	GND
12	+3.3V	28	AD[20]	44	GND	60	N.C.
13	RST#	29	AD[18]	45	AD[14]	61	ACK64#
14	GND	30	GND	46	AD[13]	62	+3.3V
15	+3.3V	31	AD[16]	47	M66EN	63	GND
16	GND	32	C/BE2#	48	AD[10]	64	N.C.

(1) IDSEL B, REQ B# and GNT B# are provided for use by dual-function PMC modules or processor-PMC modules

PCI signals active when low.

Table 24: PMC J12 and J22 Connector Pin Assignment

2.8.10 PMC J13 and J23 Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	N.C.	17	AD[59]	33	GND	49	AD[37]
2	GND	18	AD[58]	34	AD[48]	50	GND
3	GND	19	AD[57]	35	AD[47]	51	GND
4	C/BE7#	20	GND	36	AD[46]	52	AD[36]
5	C/BE6#	21	V(I/O)	37	AD[45]	53	AD[35]
6	C/BE5#	22	AD[56]	38	GND	54	AD[34]
7	C/BE4#	23	AD[55]	39	V(I/O)	55	AD[33]
8	GND	24	AD[54]	40	AD[44]	56	GND
9	V(I/O)	25	AD[53]	41	AD[43]	57	V(I/O)
10	PAR64	26	GND	42	AD[42]	58	AD[32]
11	AD[63]	27	GND	43	AD[41]	59	N.C.
12	AD[62]	28	AD[52]	44	GND	60	N.C.
13	AD[61]	29	AD[51]	45	GND	61	N.C.
14	GND	30	AD[50]	46	AD[40]	62	GND
15	GND	31	AD[49]	47	AD[39]	63	GND
16	AD[60]	32	GND	48	AD[38]	64	N.C.

PCI signals active when low.

Table 25: PMC J13 and J23 Connector Pin Assignment

2.8.11 PMC J14 and J24 Connector Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	PMC IO 01	17	PMC IO 17	33	PMC IO 31	49	PMC IO 49
2	PMC IO 02	18	PMC IO 18	34	PMC IO 34	50	PMC IO 50
3	PMC IO 03	19	PMC IO 19	35	PMC IO 35	51	PMC IO 51
4	PMC IO 04	20	PMC IO 20	36	PMC IO 36	52	PMC IO 52
5	PMC IO 05	21	PMC IO 21	37	PMC IO 37	53	PMC IO 53
6	PMC IO 06	22	PMC IO 22	38	PMC IO 38	54	PMC IO 54
7	PMC IO 07	23	PMC IO 23	39	PMC IO 39	55	PMC IO 55
8	PMC IO 08	24	PMC IO 24	40	PMC IO 40	56	PMC IO 56
9	PMC IO 09	25	PMC IO 25	41	PMC IO 41	57	PMC IO 57
10	PMC IO 10	26	PMC IO 26	42	PMC IO 42	58	PMC IO 58
11	PMC IO 11	27	PMC IO 27	43	PMC IO 43	59	PMC IO 59
12	PMC IO 12	28	PMC IO 28	44	PMC IO 44	60	PMC IO 60
13	PMC IO 13	29	PMC IO 29	45	PMC IO 45	61	PMC IO 61
14	PMC IO 14	30	PMC IO 30	46	PMC IO 46	62	PMC IO 62
15	PMC IO 15	31	PMC IO 31	47	PMC IO 47	63	PMC IO 63
16	PMC IO 16	32	PMC IO 32	48	PMC IO 48	64	PMC IO 64

Table 26: PMC J14 and J24 Connector Pin Assignment

2.8.12 PMC Signal Description

Mnemonic	Signal Description
AD[00] to AD[63]	Address/Data bits. Multiplexed address and data bus. AD32 to AD63 are specifics to 64-bit bus extension.
ACK64#	Acknowledge 64-bit Transfer. Driven low by the device to indicate that the target is willing to transfer data using 64 bits.
BUSMODE1#	Bus Mode 1. Driven low by a PMC module to indicate that it supports the current bus mode
C/BE0# to C/BE7#	Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus. C/BE4# to C/BE7# are specifics to 64-bit bus extension.
CLK	Clock. Except RST*, the 64-bit PCI bus signals are synchronous to 33 or 66 MHz clock.
DEVSEL#	Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access.
FRAME#	FRAME. Driven low by the current master to signal the start and duration of an access.
EREADY	EREADY. Output of non-monarch PPMCs that indicates it has completed its onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles. Input to the monarch PPMC that indicates all non-monarch PPMCs have completed their onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles.
GNT#	Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent. GNT B# is provided for use by dual-function PMC modules or processor-PMC modules.
IDSEL	Initialization Device Select. Device chip select during configuration cycles. IDSEL B is provided for use by dual-function PMC modules or processor-PMC modules.
INTA# to INTD#	Interrupt lines. Level-sensitive, active-low interrupt requests.
IRDY#	Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase.
LOCK#	LOCK. Driven low to indicate an atomic operation that may require multiple transactions to complete.
M66EN	66 MHZ Enable. Indicates to a device if the bus segment is operating at 66 or 33 MHz. If it is high then the bus speed is 66 MHz and if it is low then the bus speed is 33 MHz.
N.C.	This pin is not connected.
PAR	Parity. Parity protection bit for AD0 to AD31 and C/BE0# to C/BE3#.
PAR64	Parity Upper DWORD. Parity protection bit for AD32 to AD63 and C/BE4# to C/BE7#.
PERR#	Parity Error. Driven low by a PCI agent to signal a parity error.
PMC IO 01 to PMC IO 64	64-bit PCI bus PMC 64 signals. Used to transmit I/O signals from PCI 64 PMC connector (J14) to P2 connector.
PMC-RSVD	Reserved. Do not connect this pin.
REQ#	Request. Driven low by a PCI agent to request ownership of the PCI bus. REQ B# is provided for use by dual-function PMC modules or processor-PMC modules.

Mnemonic	Signal Description
REQ64#	Request 64-bit Transfer. Driven low by the current bus master, indicates that it desires to transfer data using 64 bits.
RST#	Reset. Driven low to reset the PCI bus.
SBO#	Snoop Backoff. Indicates a hit of a modified line asserted.
SDONE#	Snoop Done. Indicates the status of the snoop for the current access.
SERR#	System Error. Driven low by a PCI agent to signal a system error.
STOP#	STOP. Driven low by a PCI target to signal a disconnect or target-abort.
TRDY#	Target Ready. Driven low by the current target to signal its ability to complete the current data phase.
V(I/O)	Power supply delivered by the board. On the PCI 64 PMC slots, +3.3 Volts power is supplied. +5 Volts signaling PMCs are not supported. Contact Kontron for more information.
+3.3V	+3.3 Volts DC power
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power

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Table 27: PMC Signal Description

2.8.13 XMC J15 and 25 Connector Pin Assignments

Two XMC sites are provided to allow the installation of VITA 42.3, PCI-Express mezzanine cards. The signals assignments are as shown in the following table. The encoding for GA[2:0] should not conflict with other SMbus/IPMI devices.

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR (1)
4	GND	GND	TCK	GND	GND	MRSTO#
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR (1)
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	N.C.	RFU	RFU	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	MBIST#	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	N.C.	PER0p5	PER0n5	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	N.C.	PER0p7	PER0n7	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK-0	N.C.	N.C.	N.C.	N.C.

(1) VPWR is connected to +12V via a 0 ohm resistor.
The 5V option is available, please contact Kontron for more information on this topic.

Signals active when low.

Table 28: XMC J15 and J25 Connector Pin Assignments

2.8.14 XMC Signal Decription

Mnemonic	Legend	Signal Description
GA[0..2]		I2C channel select. These signals allow a carrier to address a specific XMC slot on an IPMI I2C bus shared by multiple XMCs.
GND		Ground
MBIST		XMC Built In Self Test. This signal allows the carrier to determine whether an XMC has completed its built-in self test.
MPRESENT		Module present. This signal allows the carrier to determine whether an XMC is present.
MRSTI		XMC Reset In. When this signal is asserted low by the carrier, the mezzanine card shall initialize itself into a known state.
MRSTO		XMC Reset Out. As input to the carrier, this optional signal provides an input to the carrier's reset logic in order to support a reset button or other reset source on the XMC.
MSCL		IPMI I2C serial clock.
MSDA		IPMI I2C serial data.
NVMRO		XMC Write Prohibit. When this signal is asserted high, the XMC shall disable writes to non-volatile memory on the XMC.
N.C.		Not Connected. Do not Used
PET0p/n[0..7]		Link 0 Differential Transmit. These signals are used by the XMC to receive high-speed protocol-specific data TO the carrier over the PCI Express interface.
PER0p/n[0..7]		Link 0 Differential Receive. These signals are used by the XMC to receive high-speed protocol-specific data FROM the carrier over the PCI Express interface.
REFCLK+/-0		Differential reference clock for Link 0 PCI Express interface.
RFU		Reserved for Future Use
TCK		JTAG Clock.
TDI		JTAG Data In
TDO		JTAG Data Out
TMS		JTAG Mode Select
TRST		JTAG Reset.
VPWR		Power pins. These signals carry either 12V or 5V power from the carrier to the XMC.
3.3V		
3.3V AUX		
+/-12V		

Table 29: XMC Signal Description

2.8.15 FMC Interface - P4 and P6 Connectors

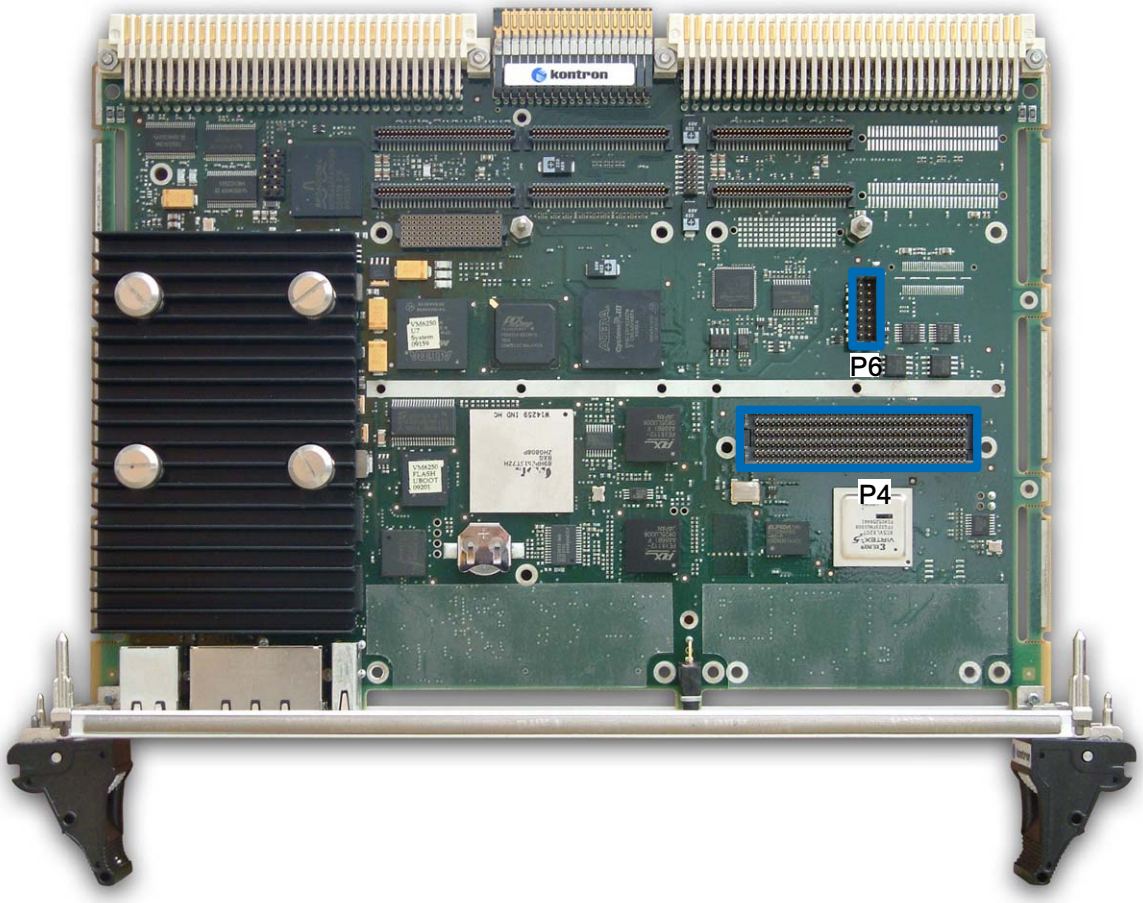


Figure 20: FMC Connectors Layout (Top View)

Please, contact Kontron for availability.

2.9 PMC Site

The VM6250 provides two XMC/PMC sites:

- The PCI-X 64 XMC/PMC site 1, 64-bit wide, operates at 133 MHz (refer to Table 30 for more information about the PCI 64 PMC Site 1 configuration).
- The PCI 32 XMC/PMC site 2, 32-bit wide, operates at 66 MHz (refer to Table 31 for more information about the PCI 32 XMC/PMC Site 2 configuration).

Kontron products include standard XMCs/PMCs such as Graphics XMC (XMC-G72), Ethernet XMC (XMC-ETH2). Refer to the Release Notes associated with your operating system for more information about the supported PMCs.

For EMC protection reasons, when not used, the PMC slots are fitted with a blanking plate.



Figure 21: PMC Site Locations

2.9.1 PCI-X 64 XMC/PMC Site 1



Electrostatic Discharge (ESD) can damage components. To avoid ESD damage, the board should be kept in its protective antistatic packaging until it is ready to be installed. During installation make sure to wear an antistatic wrist strap to discharge static electricity.

PMC Site 1 can alternately be used as an XMC site with a x4 PCI-Express link to the MPC864x processor. A XMC card installed in this location uses its P5 (J15 on the VM6250) for the Express Link. The installed XMC should provide either front panel I/O or utilize a P4 (J14 on the VM6250) for I/O.

The following table sums up all information concerning the PCI 64 PMC Site 1. It gives information needed for software and hardware configuration.

FUNCTION	VALUE	DESCRIPTION
PMC Connectors	J11	Connects the signals for the 64-bit PCI bus.
	J12	Connects the signals for the 64-bit PCI bus.
	J13	Connects the signals for the 64-bit PCI bus.
	J14	Connects the User Defines I/O signals.
XMC Connectors	J15	Connects the signals for the switched communications.
V(I/O) Voltage Level	+3.3V	The signaling voltage of the 64-bit PCI bus is +3.3V. It is not +5V tolerant. The user must check that its PMC type is compatible with this signaling voltage (refer to section 2.9.3 page 58).
PCI Bus Mode	64 Bits	The PCI bus is in 64-bit mode.
PCI Bus Rate	133 MHz	The PCI bus can run at 133 MHz (refer to the Hardware Release Notes for possible restrictions).
PCI Interrupts	INTA INTB INTC INTD	Connected to the Interrupt Controller.
Bus Number	6	64-bit PCI bus corresponds to PCI bus number 0.
Device Number	4	PMC Site 1 is device number 1 on the 64-bit PCI bus.
REQ/GNT IDSEL	0 AD[20]	for single function PMC's
Alternate REQ/GNT Alternate IDSEL	2 AD[24]	for dual function PMC's

Table 30: PCI 64 XMC/PMC Site 1 Information

2.9.2 PCI 32 XMC/PMC Site 2



Electrostatic Discharge (ESD) can damage components. To avoid ESD damage, the board should be kept in its protective antistatic packaging until it is ready to be installed. During installation make sure to wear an antistatic wrist strap to discharge static electricity.

PMC Site 2 can alternately be used as an XMC site with a x4 PCI-Express link to the MPC8641x processor. A XMC card installed in this location uses its P5 (J25 on the VM6250) for the Express Link. The installed XMC should provide either front panel I/O or utilize a P4 (J24 on the VM6250) for I/O.

The following table sums up all information concerning the PCI 32 XMC/PMC Site 2. It gives information needed for software and hardware configuration.

FUNCTION	VALUE	DESCRIPTION
PMC Connectors	J21	Connects the signals for the 64-bit PCI bus.
	J22	Connects the signals for the 64-bit PCI bus.
	J23	Connects the signals for the 64-bit PCI bus.
	J24	Connects the User Defines I/O signals.
XMC Connectors	J25	Connects the signals for the switched communications.
V(I/O) Voltage Level	+3.3V	The signaling voltage of the 64-bit PCI bus is +3.3V. It is not +5V tolerant. The user must check that its PMC type is compatible with this signaling voltage (refer to section 2.9.3 page 58).
PCI Bus Mode	32 Bits	The PCI bus is in 32-bit mode.
PCI Bus Rate	66 MHz	The PCI bus can run at 66 MHz (refer to the Hardware Release Notes for possible restrictions).
PCI Interrupts	INTA INTB INTC INTD	Connected to the Interrupt Controller.
Bus Number	6	64-bit PCI bus corresponds to PCI bus number 0.
Device Number	5	XMC/PMC Site 2 is device number 1 on the 64-bit PCI bus.
REQ/GNT IDSEL	1 AD[21]	for single function PMC's
Alternate REQ/GNT Alternate IDSEL	3 AD[25]	for dual function PMC's

Table 31: PCI 64 XMC/PMC Site 2 Information

2.9.3 Signaling Voltage Keying Pin

The PCI bus of the VM6250 and the PMC plugged on the PCI slot have to operate on the same signaling level.

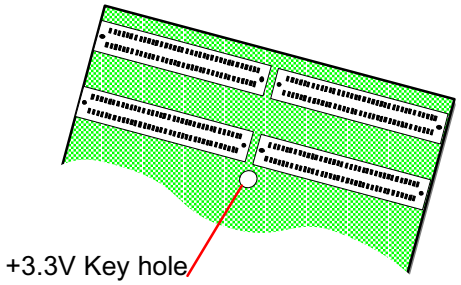
The VM6250 sets the signaling level for the PCI busses to +3.3V (i.e. V(I/O)=+3.3V). The V(I/O) pins of the PCI PMC are connected to +3.3V.

The distinction between PMC types is the signaling level they use, not the power rails they connect to, nor the component technology they contain.

On the VM6250 PCI PMC slots, only two PMC types must be intalled:

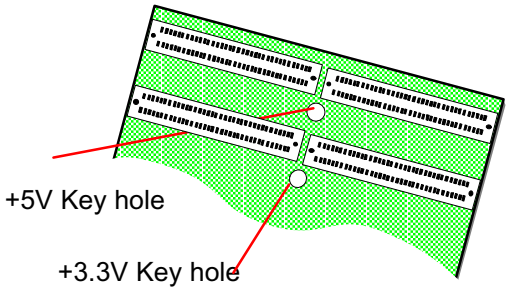
> +3.3V PMC

It is designed to work only in a +3.3V signaling level and will only have a keying hole.

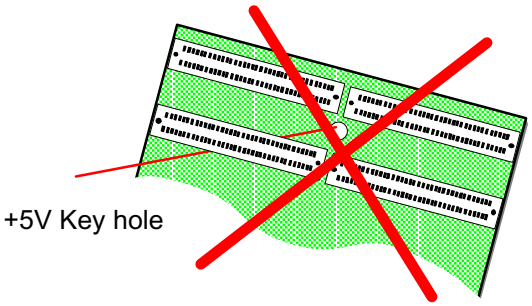


> Universal PMC

It supports both voltages (+5V and +3.3V). This PMC is capable of detecting the signaling level in use and adapting itself to that environment. It has two keying holes (+5V and +3.3.V) and can, therefore, be plugged into either signaling level.



As no PMC voltage selection key is provided on the board, make sure not to insert a +5V PMC on the board. Failture to observe this restriction may result in damage to the PMC or the VM6250.



Chapter 3 - Installation

The VM6250 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VM6250. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.



Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

3.2 Board Identification

The VM6250-SA boards are identified by labels fitted to the bottom side.

A "Board Idenditification" label and associated 2D barcode.

- Order Code . . . . . Top, left location
- E.C. Level . . . . . Top, right location
- Serial Number . . . . . Bottom, left location
- Variant . . . . . Bottom, right location

B "Ethernet Number" label for ETH0, ETH1, ETH2 and ETH3 interfaces and associated 2D barcode (address interfaces are in hexadecimal format).

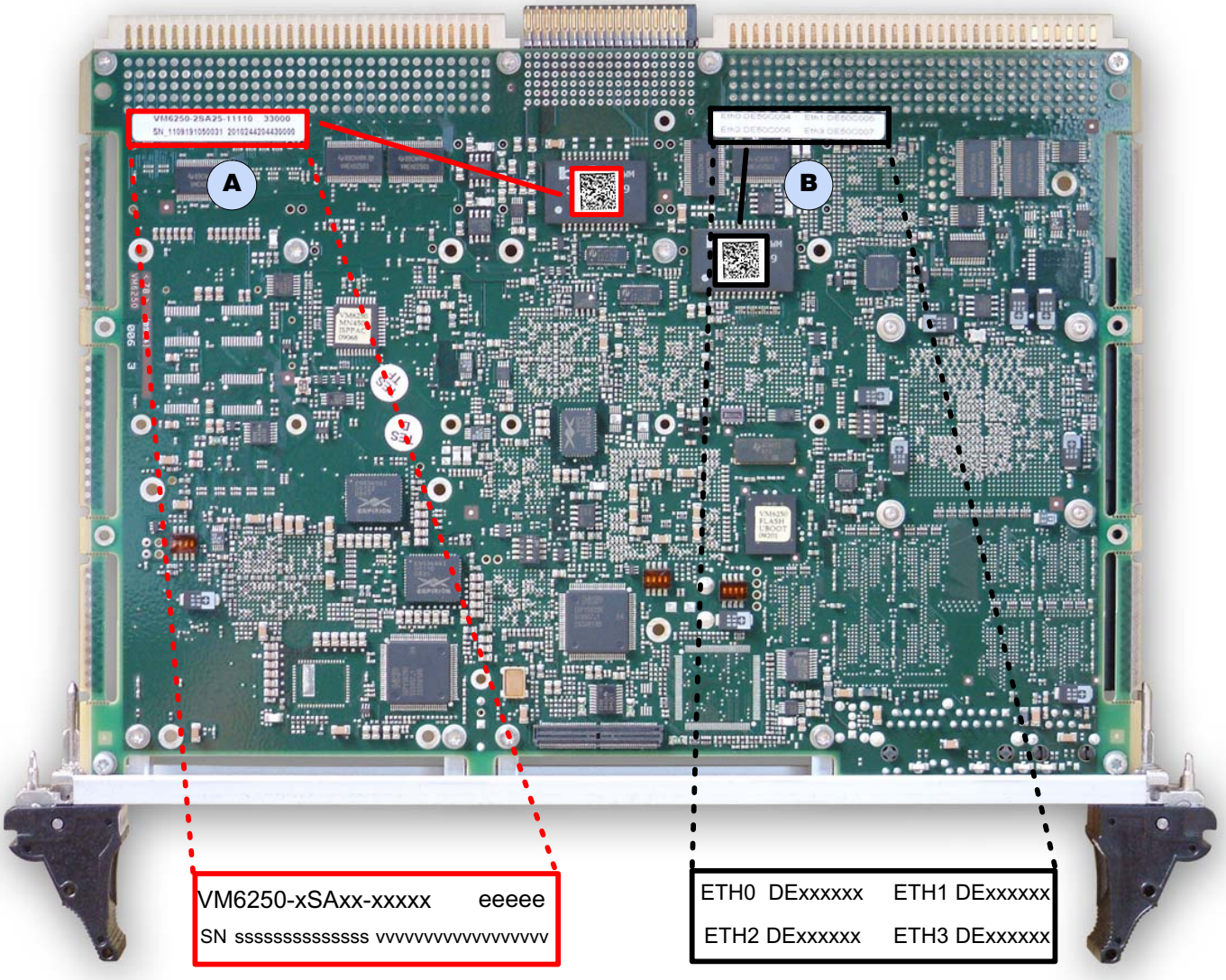


Figure 22: Board Identification (Bottom View)

3.3 Board Configuration

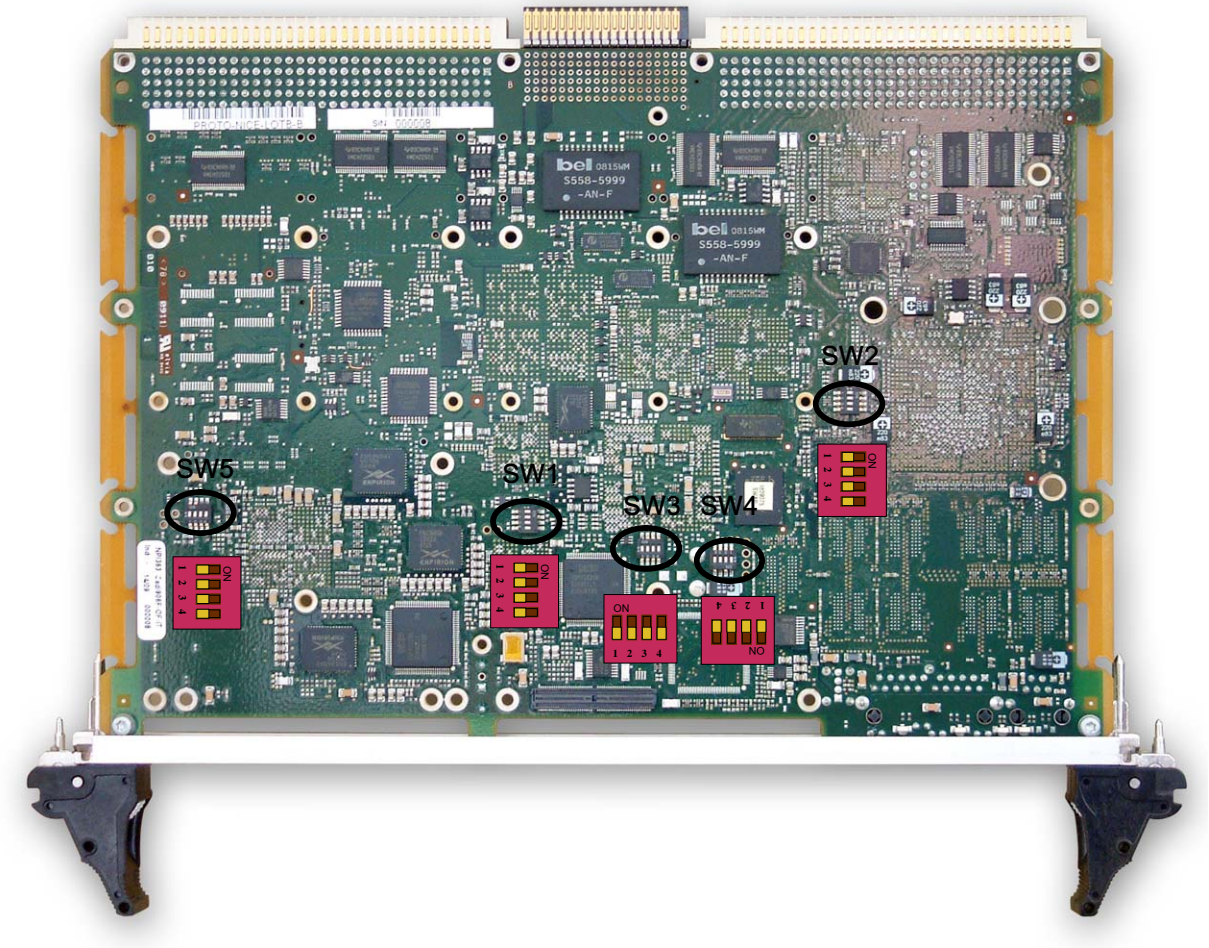


Figure 23: Board Configuration

Four 4-bit DIP switches are available on the VM6250: SW1, SW2, SW3, SW4 and SW5.

3.3.1 DIP Switch SW1 Description

DIP Switch SW1	Function	Description
1 .. 4	Reserved	Reserved

3.3.2 DIP Switch SW2 Description

DIP Switch SW2	Function	Description
1	Reserved	Reserved
2	Boot Flash Selection	ON (0) Boot from Flash 1 OFF (1) Boot from Flash 0
3	Reserved	Reserved
4	Reserved	Reserved

3.3.3 DIP Switch SW3 Description

DIP Switch SW3	Function	Description
1 .. 4	Reserved	Reserved

3.3.4 DIP Switch SW4 Description

DIP Switch SW4	Function	Description
1	Boot Flash 0 WP#	ON (0) Boot Flash 0 Write Protected OFF (1) Boot Flash 0 Write Enabled
2	Boot Flash 1 WP#	ON (0) Boot Flash 1 Write Protected OFF (1) Boot Flash 1 Write Enabled
2 .. 4	Reserved	Reserved

3.3.5 DIP Switch SW5 Description

DIP Switch SW5	Function	Description
1 .. 4	Reserved	Reserved

3.4 Package Content

The VM6250 is packaged with several components. The packing contents of the VM6250 Series may vary depending on customer requests.

- **CPU Module**
  - Order Code: VM6250-*xxxxxxxxxx*
    - Processor specifications differ depending on Order Code
    - Heat sink assembled on the board
    - Battery assembled on the board
  - Serial adaptation cable RJ-12 <-> DB-9 (Order Code: KIT-RJ12DB9)
  - CD-ROM Technical Documentation
- **PMCs Carrier**
  - Order Code: V2PMC2-*xx*
- **Rear Transition Module**
  - Order Code: PBV36-P0-VM6-00
- **USB Flash Disk Module**
  - Order Code: FDM-USB-*x*GB-L2-IV

3.5 Initial Installation Procedure

The following procedures are applicable only for the initial installation of the VM6250 in a system.

To perform an initial installation of the VM6250 in a system proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed.

   
   Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VM6250 refer to Chapter 4. For the installation of VM6250 specific peripheral devices and Rear I/O devices refer to the appropriate sections in Chapter 3.

   
   Care must be taken when applying the procedures below to ensure that neither the VM6250 nor other system boards are physically damaged by the application of these procedures.

3. To install the VM6250 perform the following:

   1. Ensure that no power is applied to the system before proceeding.

      
      When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
   3. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
   4. Fasten the two front panel retaining screws.
   5. Connect all external interfacing cables to the board as required.
   6. Ensure that the board and all required interfacing cables are properly secured.

The VM6250 is now ready for operation. For operation of the VM6250, refer to appropriate VM6250 specific software, application, and system documentation.

3.6 Standard Removal Procedure

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

   
   Care must be taken when applying the procedures below to ensure that neither the VM6250 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the two front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

   
   Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

3.7 Installation of Peripheral Devices

The VM6250 is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following chapters provide information regarding installation aspects and not detailed procedures.

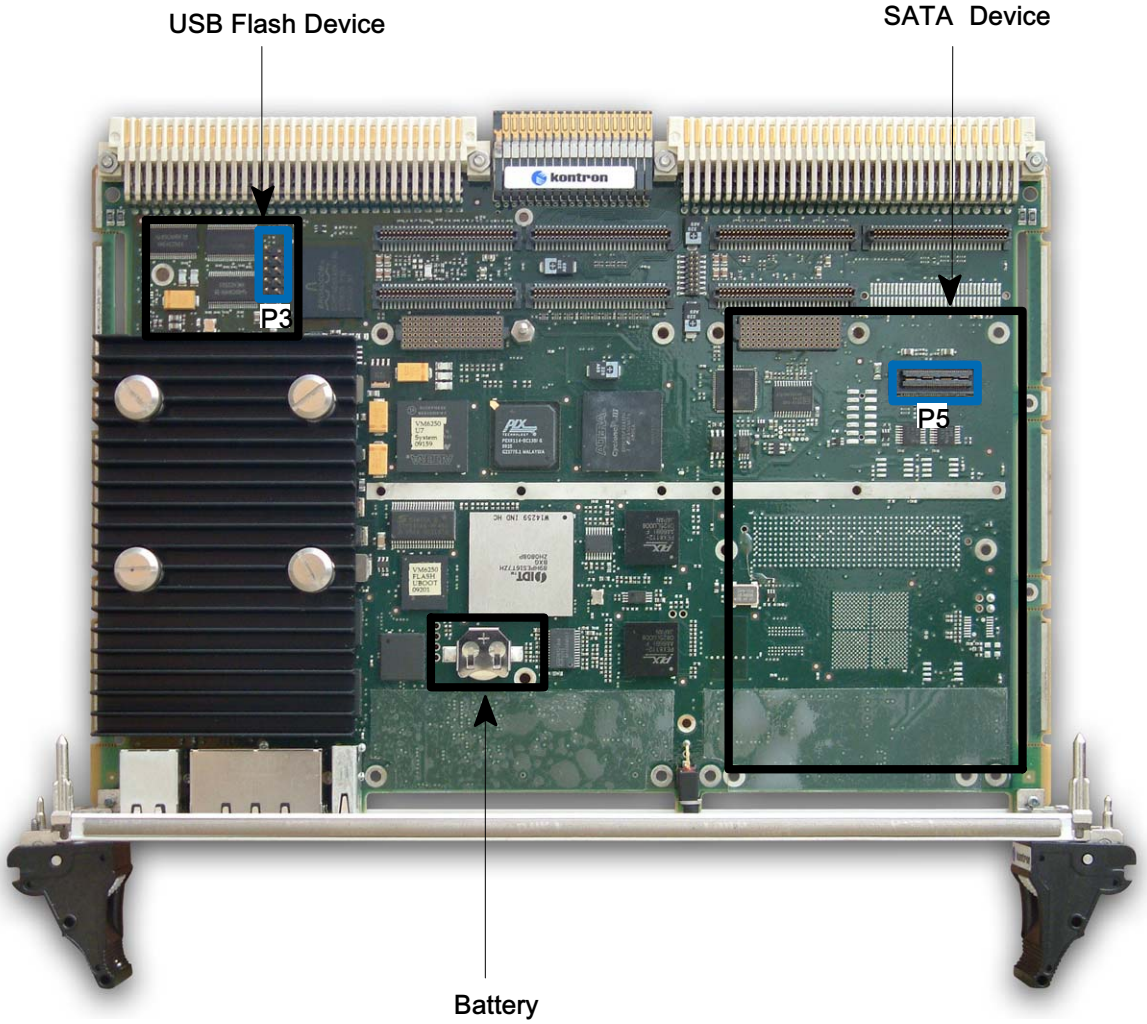


Figure 24: Onboard Devices

3.7.1 USB Device Installation

The VM6250 supports all USB plug and play computer peripherals.

Note All USB devices may be connected or removed while the host or other peripherals are powered up.

USB Flash Disk Installation



The USB Flash module is fixed to the board, by using:

- on one side the P3 connector,
- on the other side, a standoff screwed to the VM6250 board and to the USB Flash module.

Figure 25: USB Flash Disk Bottom View

3.7.2 Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

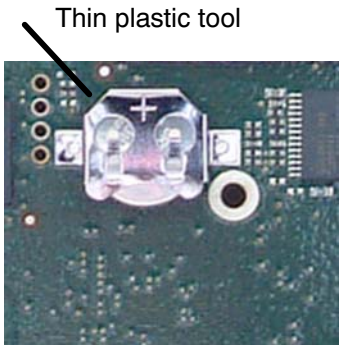


Figure 26: Battery Location

To replace the battery, proceed as follows:

> Turn off power.

> Use a thin plastic tool to push the battery outside the safety cache. Push from the right or left top side of the safety cache.

> Remove the battery.

> Place the new battery in the socket.

> Make sure that you insert the battery the right way round. The plus pole must be on the top!

Note Care must be taken to ensure that the battery is correctly replaced.
The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

3.7.3 Serial ATA Extension Module

A Serial ATA Extension Module with up to 120 GB SATA HDD may be connected to the VM6250 via the onboard connector P5.

- This module must be installed only on the VM6250 boards that support the SATA onboard manufacturing option.
- The SATA onboard manufacturing option is not available on VM6250-RC boards.

If not already done, the SATA extension module must be physically installed on the VM6250 prior to installation of the VM6250 in a system.

During installation it is necessary to ensure that the SATA Flash module is properly seated in the onboard connector P5, i.e. the pins are aligned correctly and not bent.



Figure 27: SATA Extension Module: Front and Bottom Viewes

The SATA extension module (order code: KIT-DISK25-SATA or KIT-DISK18-SATA) is made up of:

- 1 plate fitted with SATA connectors
- 4x screws CZX-M3X5-INOX
- 4x screws CZX-M2.5X5-INOX

Installation process (if not already done):

1. Insert the SATA disk in the SATA connector. Example of SATA disk validated:
   - Manufacturer: Western Digital
   - Part No: SSD-D0015SI-5000
2. Fix the SATA disk to the plate using the four screws CZX-M3X5-INOX. Use medium strengh threadlocker (recommended torque of 0.4 Nm).
3. Plug the kit (plate and disk) on the VM6250 board, SATA connector (P5)
4. Fix the kit to the VM6250 board using the four screws CZX-M2.5X5-INOX. Use medium strengh threadlocker (recommended torque of 0.3 Nm).

3.7.4 PMC Installation

PMC modules are delivered with a full kit of parts for mounting them, and the user guide for the module normally contains instructions on how to fit the module.

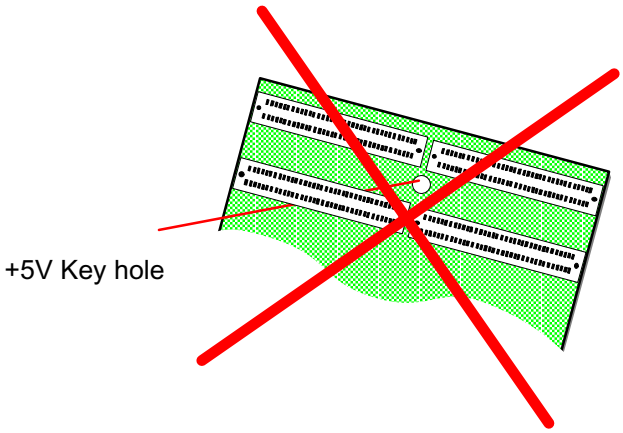
The installation of the PMC on the VM6250 conforms to the IEEE P1386.1 standard.

To install the XMC/PMC module, refer to Figure 28 to Figure 32 and follow the steps below:

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the VM6250 board or the XMC/PMC.
If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

1. Place carefully the VM6250 with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Remove the blanking plate from the appropriate XMC/PMC slot of the VM6250.
3. Check that the standoffs are attached to the XMC/PMC.
4. Install the XMC/PMC, component-side down, aligning the PCI connectors with their mating connectors on the VM6250 and the XMC connector if available. Press them together so that the friction from the pins holds them together. Insert the standoff plug mounted on the VM6250 into the keyhole. The module's bezel will fill the slot and provide a connection to the module.

   As no PMC voltage selection key is provided on the board, make sure not to insert a +5V PMC on the board. Failture to observe this restriction may result in damage to the PMC or the VM6250.
   Refer to section 2.9.3 “Signaling Voltage Keying Pin" page 58 for more information on this topic.



5. Screw the XMC/PMC in place using the 4 mounting points, on the bottom side of the VM6250 . You need a Phillips screwdriver for this stage.
6. The XMC/PMC attachment is now complete.
7. Insert the VM6250 into the chassis making sure it is plugged into the backplane.

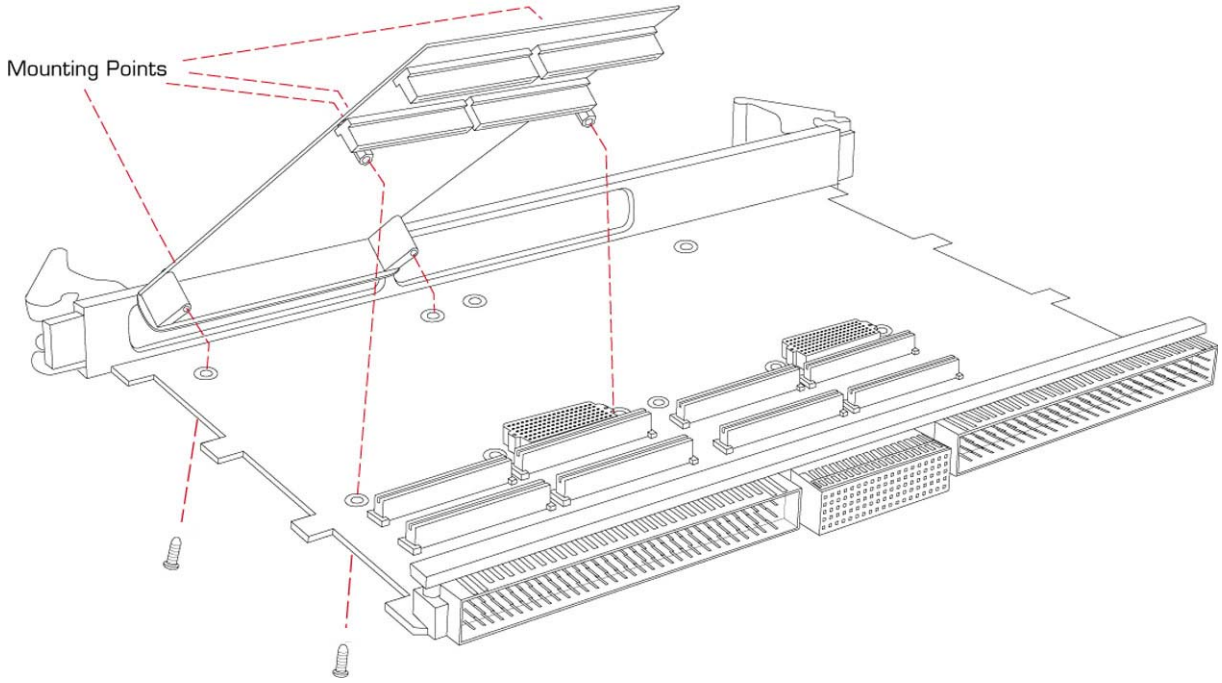


Figure 28: PMC Installation on PMC Site 1

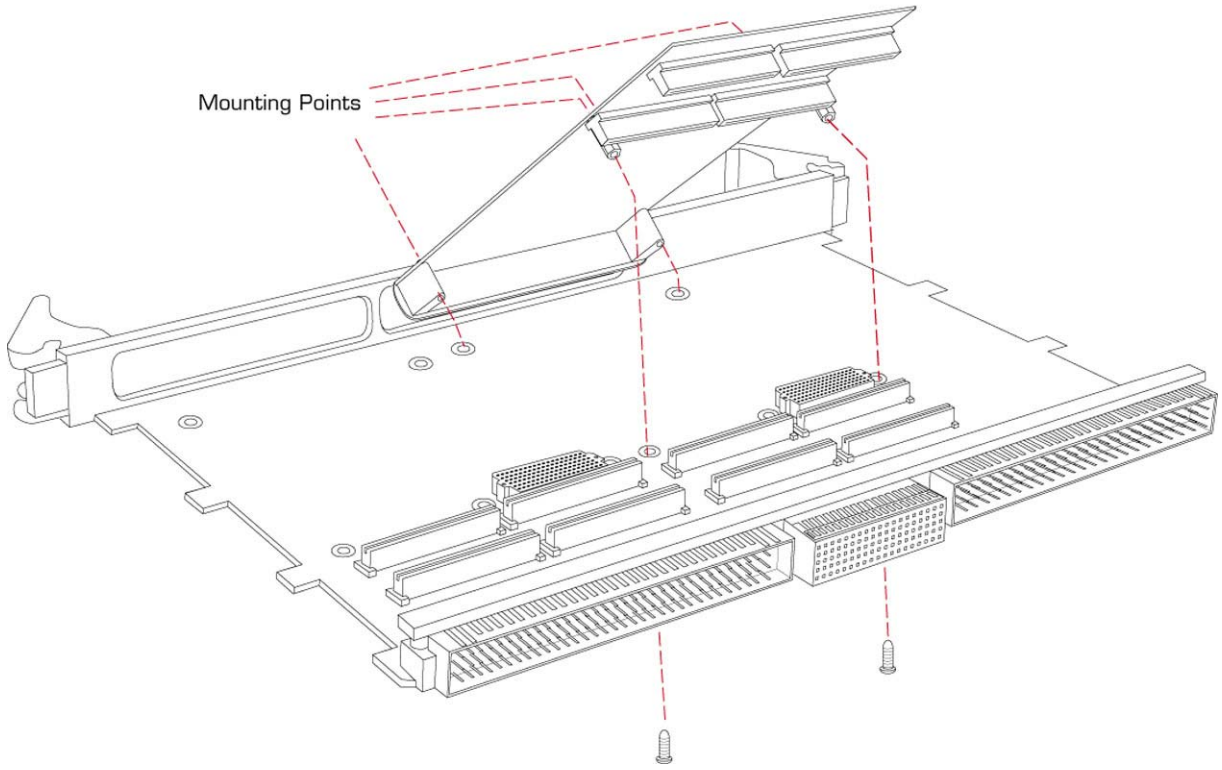


Figure 29: PMC Installation on PMC Site 2

3.7.5 XMC Installation

The XMC board standard is based on the PMC mechanical definition, and occupies the same board area.

The XMC board add one new connector to the connectors already on a PMC. The new connectors support high-speed differential signals for fabric communications.

Figure 30 shows a XMC fitted only with the XMC connector.

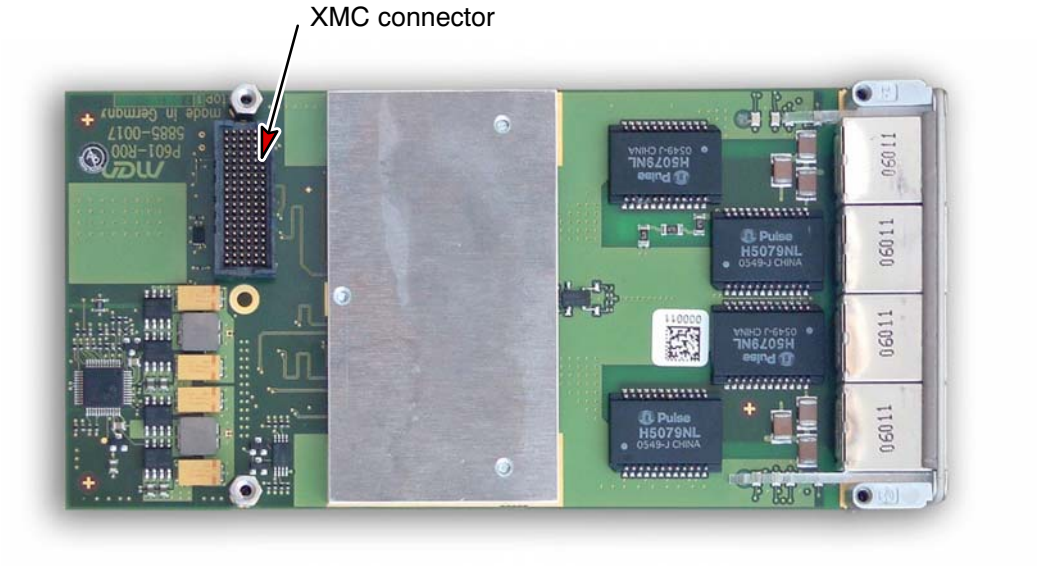


Figure 30: Example of XMC Board

Figure 31 shows a XMC installation on the PMC Site 1.

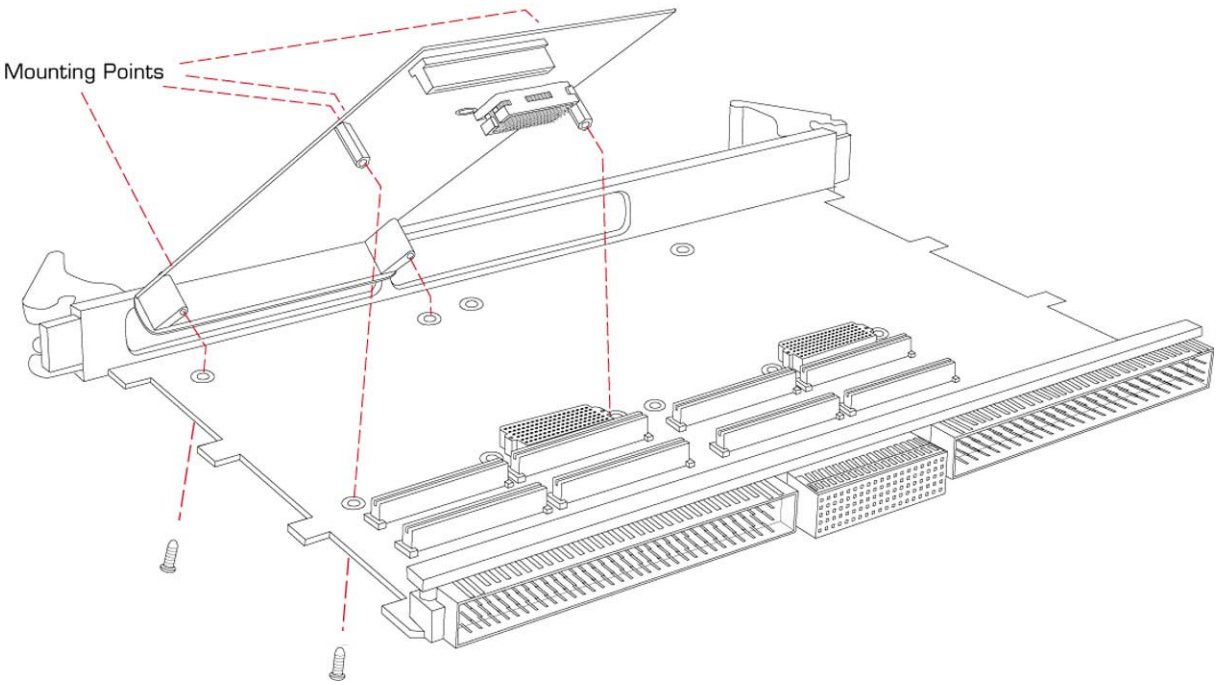


Figure 31: XMC Installation on PMC Site 1

Figure 32 shows a XMC installation on the PMC Site 2.

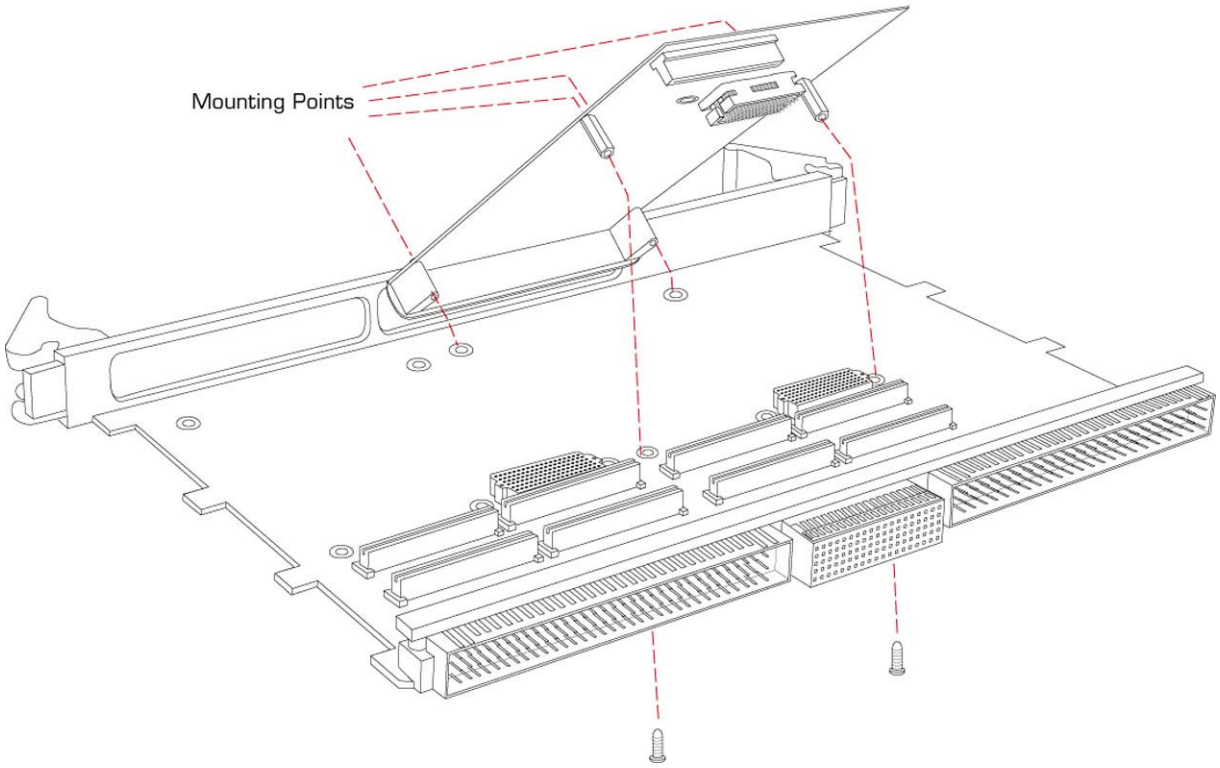
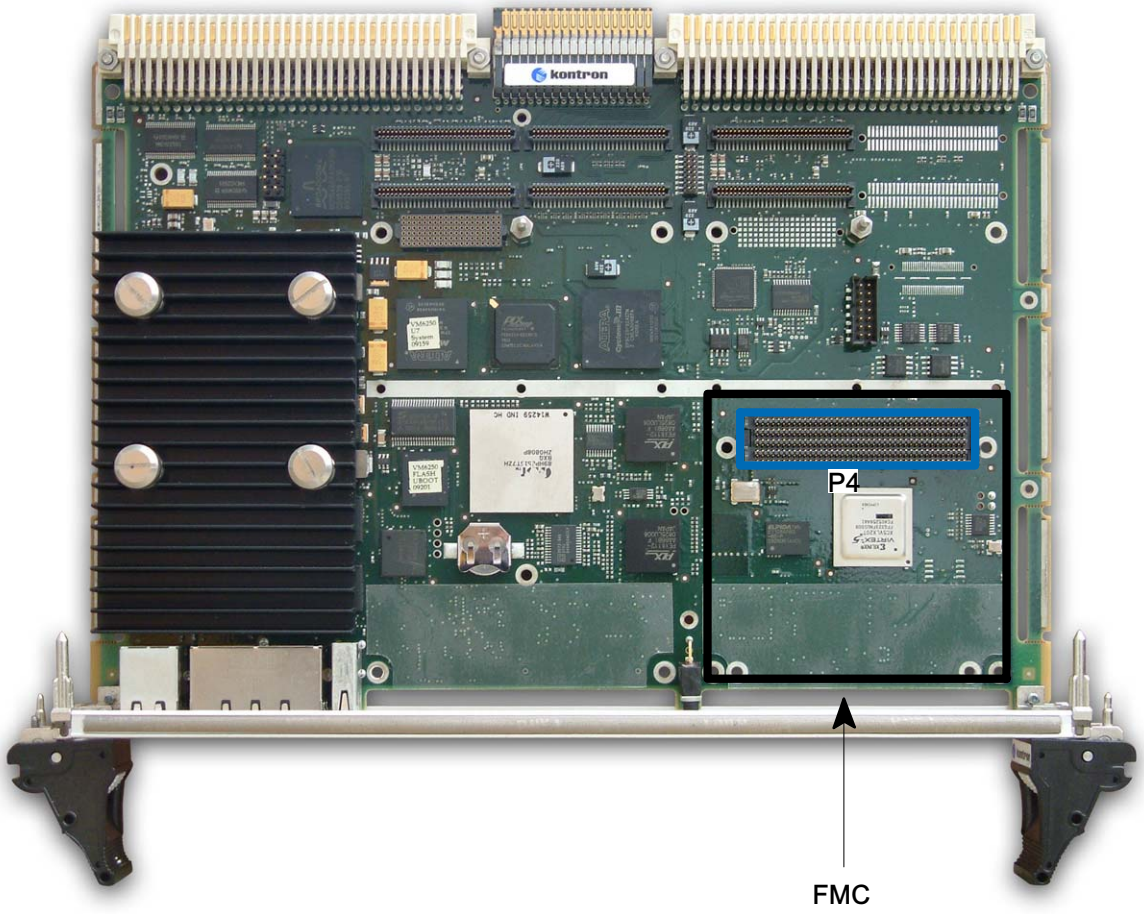


Figure 32: XMC Installation on PMC Site 2

3.7.6 FMC Installation



Please, contact Kontron for availability.

3.8 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation:

- VM6250 Release Notes Fedora9 . . . . . SD.DT.F37
- VM6250 VxWorks BSP User's Guide SD.DT.F44

Chapter 4 - Programming Interface

4.1 Interrupt Routing

The Freescale MPC8641x processor has twelve dedicated interrupt inputs. These interrupts will be used on the VM6250 board according to the following table:

Pin	Description
IRQ0	Reserved - PCIe1 INTA
IRQ1	Reserved - PCIe1 INTB
IRQ2	Reserved - PCIe1 INTC
IRQ3	Reserved - PCIe1 INTD
IRQ4	Reserved - PCIe2 INTA
IRQ5	Reserved - PCIe2 INTB
IRQ6	Reserved - PCIe2 INTC
IRQ7	Reserved - PCIe2 INTD
IRQ8	Watchdog Timer
IRQ9	Thermal Alert
IRQ10	GPIO Interrupt
IRQ11	Ethernet PHY Channel 1..4 IRQ Shared

Table 32: CPU Interrupts

Device	CPU IRQ0 / INTA	CPU IRQ1 / INTB	CPU IRQ2 / INTC	CPU IRQ3 / INTD
USB FP/FLASH	INTA	-	-	-
USB P0	-	-	-	INTA
SATA	INTD	INTA	INTB	INTC
XMC 2 / FPGA I/O	INTC	INTD	INTA	INTB
PMC 2	INTB	INTC	INTD	INTA
ALMA2f	INTC	INTD	INTA	INTB
XMC 1 / PMC 1	INTB	INTC	INTD	INTA

4.2 Chip Select Lines Usage

Chip Select	Description
CS0 (1)	Flash Boot 1
CS1 (1)	Flash Boot 2
CS2	Not Used
CS33	System CPLD Registers
CS4	NVSRAM Memory
CS5	Not Used

(1) CS0, CS1 and CS2 device selection can change depending on DIP sitches configuration.

Table 33: Chip Select

Chapter 5 - Power and Thermal Considerations

5.1 Power Considerations

5.1.1 System Power

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VM6250 system environment.

5.1.1.1 VM6250 Baseboard

The VM6250 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the VM6250 should be carefully tested to ensure compliance with these ratings.

Supply Voltage	Maximum Permitted Voltage
+3.3VDC	+3.6V
+5VDC	+6V
+12V/-12VDC (1)	+14V/-14V

(1) if required for mezzanine.

Table 34: Maximum Input Power



The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with these figures may result in damage to your board.

The following table specifies the range of the different input power voltages within the board is functional. The VM6250 is not guaranteed to function if the board is not operating within the prescribed limits.

Input Supply Voltage	Absolute Range
+3.3V	3.25V min. to 3.45V max.
+5V	4.875V min to 5.25V max.
+12V (1)	11.64V min. to 12.6V max.
-12V (1)	-12.6V min. to -11.64V max.

(1) if required for mezzanine.

Table 35: DC Operational Input Voltage Ranges

5.1.1.2 Backplane

Backplanes to be used with the VM6250 must be adequately specified. The backplane must provide optimal power distribution for the +3.3V, +5V and +12V power inputs. It is recommended to use only backplanes which have at least two power planes for the +3.3V and +5V voltages.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use Positronic or M-type connector backplanes and power supplies where possible.

5.1.1.3 Power Supply Units

Power supplies for the VM6250 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the VM6250 has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

» Start-Up Requirements

Power supplies must comply with the following guidelines, in order to be used with the VM6250.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0V to nominal Vout.

» Power-UP Sequence

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation.

The time from +5 VDC until the output reaches its minimum in regulation level and from +3.3 VDC until the output reaches its minimum in regulation level must be < 20 ms.

Tolerance

The following table provides information regarding the required characteristics for each board input voltage.

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (P-P)	REMARKS
5V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
3.3V	+3.3 VDC	+5%/-3%	50 mV	Main voltage
+12V	+12 VDC	+5%/-5%	240 mV	Required
-12V	-12 VDC	+5%/-5%	240 mV	Not Required
V I/O (PCI) singalling voltage	+3.3 VDC or +5 VDC	+5%/-3%	50 mV	Depends on board version
GND	Ground, not directly connected to potential earth (PE)			

Table 36: Input Voltage Characteristics

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.



If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the VM6250 baseboard and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and power specifications for the VM6250 board and the VM6250 accessories. The values were measured using an 8-slot passive VME backplane with two power supplies: one for the CPU, and the other for the hard disk.

5.1.2.1 Real Applications

The following tables indicate the power consumption using real applications with soldered DDR2 SDRAM.

The Power Consumption was measured using U-Boot or Linux IDLE Mode.

POWER	VM6250-1SA2410110	VM6250-2SA2511110	VM6250-2SA3511110	VM6250-2SA4511110
Typical	(2.4A x 5V) + (4.7A x 3.3V) = **27W**	(3.5A x 5V) + (5.1A x 3.3V) = **35W**	(4.7A x 5V) + (5.1A x 3.3V) =**41W**	(5.6A x 5V) + (5.2A x 3.3V) =**45W**

Table 37: Power Consumption: U-Boot or Linux IDLE Mode

The Power Consumption was measured using Linux with 100% processor load.

POWER	VM6250-1SA2410110	VM6250-2SA2511110	VM6250-2SA3511110	VM6250-2SA4511110
Maximal	(3.0A x 5V) + (5.3A x 3.3V) = **33W**	(4.8A x 5V) + (5.7A x 3.3V) =**43W**	(6.7A x 5V) + (5.6A x 3.3V) =**52W**	(8.3A x 5V) + (5.7A x 3.3V) =**61W**

Table 38: Power Consumption: Linux 100% Processor Load

5.2 Thermal Considerations

The following sections provide system integrators with the necessary information to satisfy the thermal and airflow requirements when implementing VM6250 applications.

5.2.1 Thermal Monitoring

To ensure optimal and long-term reliability of the VM6250, all onboard components must remain within the maximum temperature specifications. The most critical components on the VM6250 are the processor and the memory. Operating the VM6250 above the maximum operating limits will result in permanent damage to the board. To ensure functionality at the maximum temperature, the Module Management Controller supports several temperature monitoring and control features.

The VM6250 includes four temperature sensors that are accessible via the Module Management Controller. They are distributed over the complete board to measure the onboard temperature values?

5.2.1.1 Placement of the Temperature Sensors

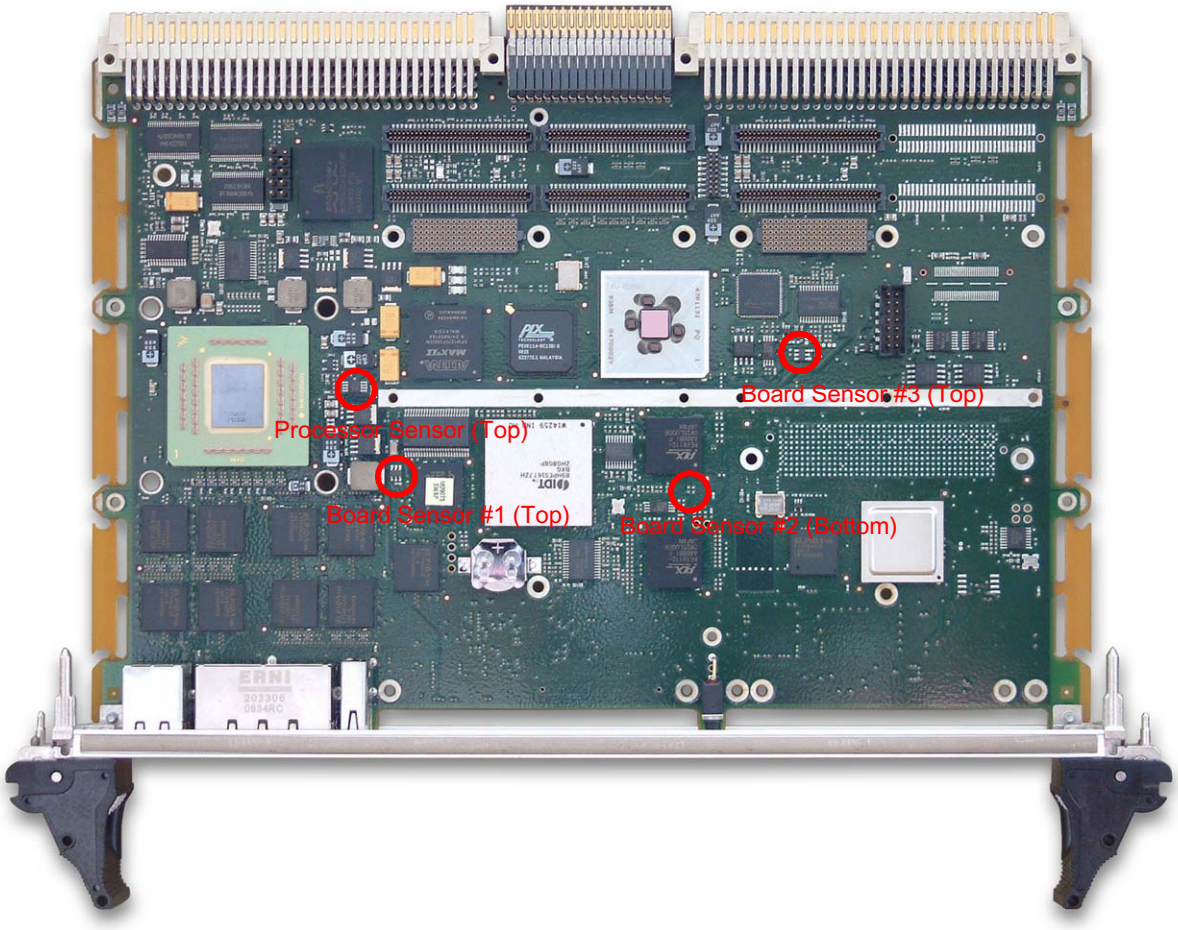


Figure 33: Board Temperature Sensor Placement (Top View)

Board Thermal Monitoring

The VM6250 includes three board temperature sensors distributed over the complete board to measure the board temperature (see Figure 33 page 81). Board Sensor #1, #2 and #3, respectively with I2C addresses 0x4A, 0x48 and 0x49. Board Sensor #1 and #3 are located on the top side of the board, and Board Sensor #2 on the bottom side of the board.

Key Features:

- Local temperature accuracy: +/- 2°C
- Operating temperature: -40°C / 150°C

Processor Thermal Monitoring

The Freescale MPC864x processor includes one die temperature sensor (Processor Sensor), as illustrated in Figure 33 page 81.

Processor Sensor, with I2C address 0x2B is loacated on the top side of the board.

Via the Processor Sensor, the Module Management Controller can measure the processor die temperature.

Key Features:

- Local temperature accuracy: +/- 3°C
- Remote temperature accuracy: +/- 0.75°C
- Operating temperature: 0°C / 125°C

This sensor is dedicated to junction processor temperature and checks only maximal Tj temperature.

5.3 CPU Internal Thermal Regulation

The Instruction Cache Throttling mechanism allows for the reduction of the CPU's power consumption and thus the CPU's temperature. This mechanism requires a dedicated software such as a thermal application or an OS daemon. For further information about the Instruction Cache Throttling, refer to the MPC8640/MPC8640D or MPC8641D Integrated Host Processor Family Reference Manual.

5.4 External Thermal Regulation

The external thermal regulation of the VM6250 is realized using a dedicated heat sink in conjunction with a system chassis that provides thermal supervision, controlled system airflow and thermal protection, such as increased airflow, reduced ambient air temperature, or power removal.

The heat sink provided on the VM6250 has been specifically designed to ensure the best possible basis for operational stability and long-term reliability. The physical size, shape and construction of the heat sink ensures the lowest possible thermal resistance.

5.4.1 Air Flow Direction

» Air Flow from PMC Slots to CPU Area

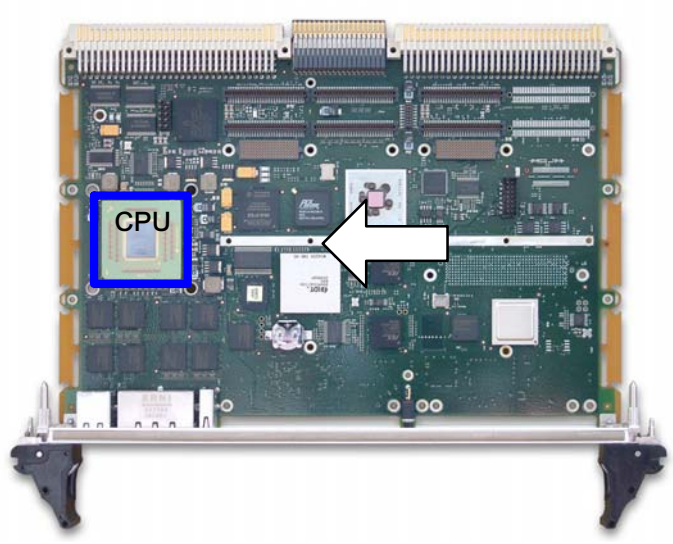


Figure 34: Air Flow fromPMC Slots to CPU Area

» Air Flow from CPU Area to PMC Slots

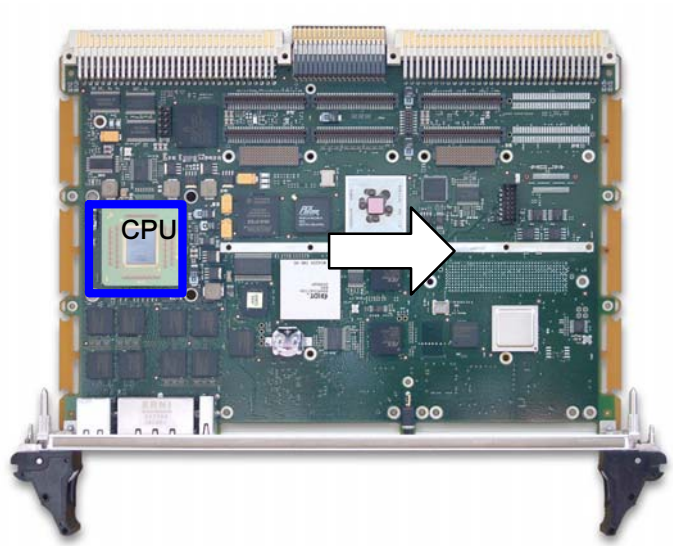


Figure 35: Air Flow fromCPU Area to PMC Slots

5.4.2 Thermal Functional Point

Following tables sum up air flow and air speed conditions for several VM6250 processor version. These measures are made for a CPU junction temperature (Tj) of 105°C, an ambient temperature of 55°C for SA baords, 65°C for WA boards.

Air-cooled (SA) Boards

Order Code	PCM Sites	Air Speed Tj 105°C (m/s)	Air Flow Tj 105°C (m3/s)	Air Flow Tj 105°C (cfm)
VM6250-1SA24-10110	No PMCs No SATA HDD	1.2	0.0061	12.9
VM6250-2SA25-11110		1.3	0.0066	14.0
VM6250-2SA35-11110		1.7	0.0086	18.2
VM6250-2SA45-11110		2.0	0.0101	21.5
VM6250-1SA24-10110	Two PMCs Gigabit Ethernet	1.3	0.0066	14.0
VM6250-2SA25-11110		1.5	0.0076	16.1
VM6250-2SA45-11110		2.4	0.0120	25.6

Table 39: Air Speed and Air Flow Measurements for SA Boards

Air-cooled Extended Temperature (WA) Boards

Order Code	PCM Sites	Air Speed Tj 105°C (m/s)	Air Flow Tj 105°C (m3/s)	Air Flow Tj 105°C (cfm)
VM6250-1WA24-10110	No PMCs No SATA HDD	2.0	0.0101	21.5
VM6250-2WA25-11110		2.1	0.0105	22.4
VM6250-2WA35-11110		2.5	0.0125	26.7
VM6250-1WA24-10110	Two PMCs Gigabit Ethernet	2.2	0.0110	23.5
VM6250-2WA25-11110		2.3	0.0116	24.6
VM6250-2WA35-11110		3.0	0.0151	32.2

Table 40: Air Speed and Air Flow Measurements for WA Boards

Following curve shows maximum acceptable temperature for the junction temperature of the processor in following configuration:

VM6250	VM6250-2SA25-11110	8640D	1 GHz	2GB DDR2 SDRAM 128K NVRAM	2x PMC/XMC
VM6250	VM6250-2WA25-11110	8640D	1 GHz	2GB DDR2 SDRAM 128K NVRAM	2x PMC/XMC

with no PMC fitted on the PMC slots.

For instance,

- at 55°C, minimum air flow needed to cool enough the processor die is about 1.3 m/s.
- at 65°C, minimum air flow needed to cool enough the processor die is about 2.1 m/s.

Note Measurements have been made with the two air flow direction (from PMC slots to CPU area and from CPU area to PMC slots).

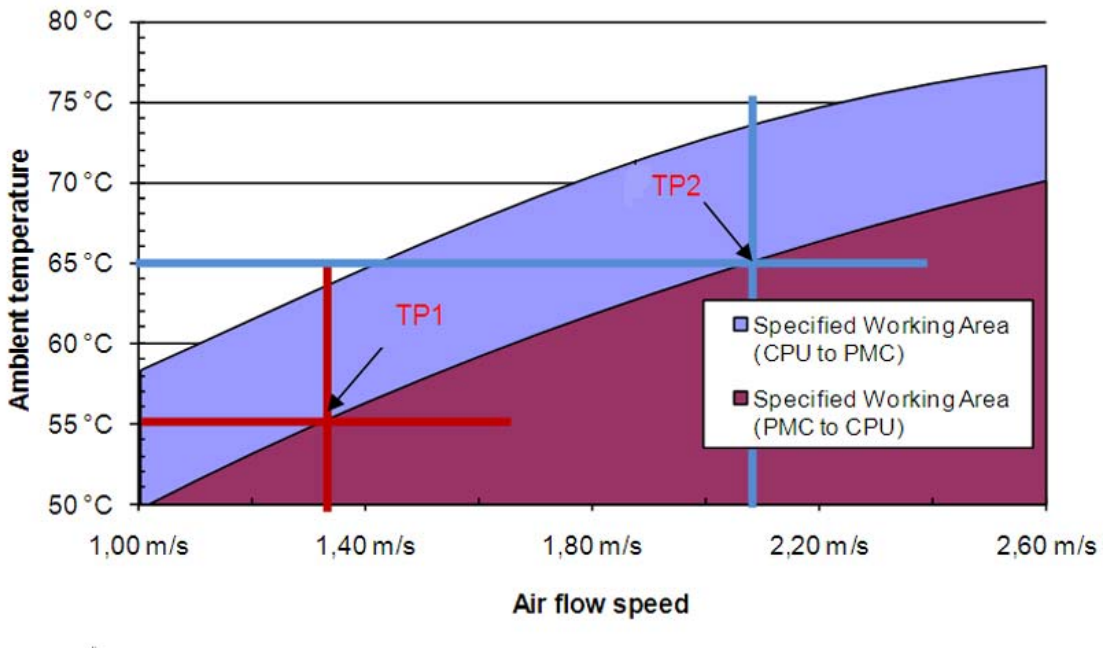


Figure 36: VM6250-SA/WA Thermal Performance: No PMC fitted

Following curve shows maximum acceptable temperature for the junction temperature of the processor in following configuration:

VM6250	VM6250-2SA25-11110	8640D	1 GHz	2GB DDR2 SDRAM 128K NVRAM	2x PMC/XMC
VM6250	VM6250-2WA25-11110	8640D	1 GHz	2GB DDR2 SDRAM 128K NVRAM	2x PMC/XMC

with one PMC fitted on each PMC slot.

For instance,

- at 55°C, minimum air flow needed to cool enough the processor die is about 1.5 m/s.
- at 65°C, minimum air flow needed to cool enough the processor die is about 2.3 m/s.

Note Measurements have been made with the two air flow direction (from PMC slots to CPU area and from CPU area to PMC slots).

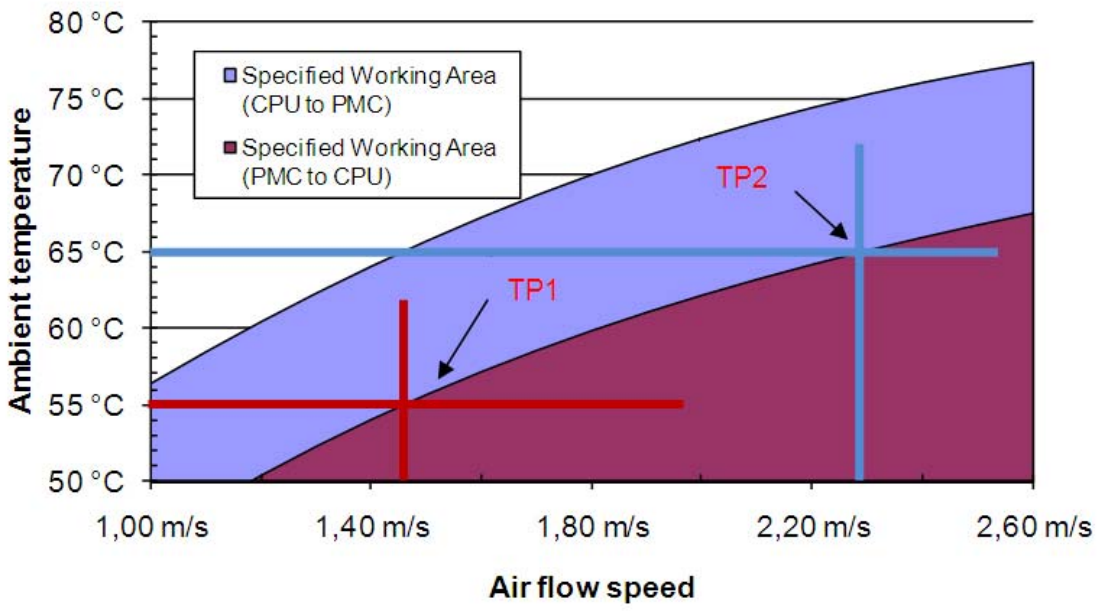


Figure 37: VM6250-SA/WA Thermal Performance: PMCs fitted

Chapter 6 - VM6250-RTM Characteristics

The VM6250-RTM (Order Code: PBV36-P0-VM6-00 rear transition module is compliant to PMC I/O Module Standard VITA 36 - 199x Draft 0.1 July 19, 1999 (mechanical and PIM format).

The main functionalities of the VM6250-RTM rear transition module are:

- Two 10/100/1000BASE-TX Ethernet interface, H1 and H2 connectors on Figure 38
- One USB connector, H4 on Figure 38
- One SMB connector, H5 on Figure 38
- Two Serial lines ports available on two HE10 connectors (H7, H8 on Figure 38)
- Three GPIOs signals available through an HE10 connector, H9 connector on Figure 38
- Two Serial ATA connectors, H10 and H11 connector on Figure 38
- One PCI Express connector, H12 connector on Figure 38
- PMC Site 1[64:1] I/O routed to J14[32:1] connector from RP2 connector
- PMC Site 2[64:1] I/O routed to J24[32:1] connector from RP2 connector (only on PBV36-P0-VM6-00 Rev. C)

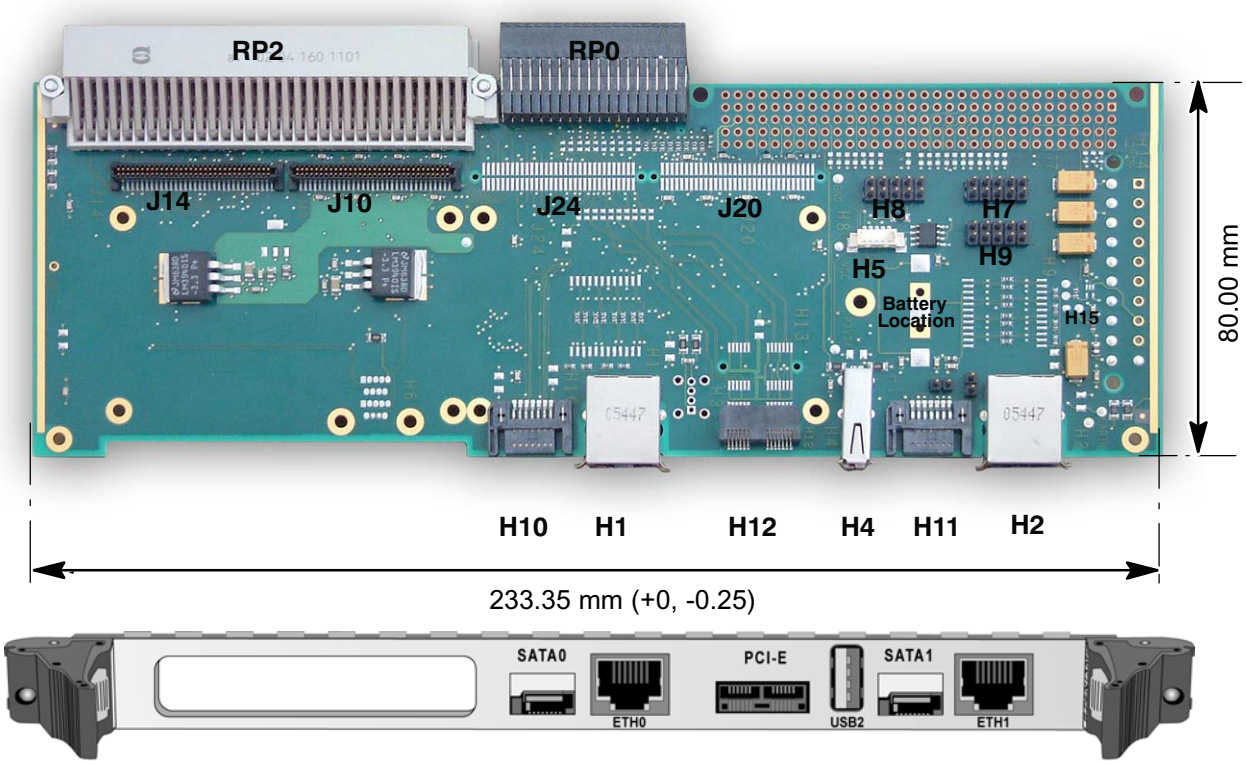


Figure 38: PBV36-P0-VM6-00 Module Overview

6.1 Installation of the Rear Transition Module

The VM6250-RTM module is designed to be used with a VME64 extensions backplane. Each slot in the backplane contains two 160-pin connectors and one connector with 95 user-defined pins. The top connector in each slot is designed J1, the middle connector is J0 and the bottom connector is J2.

The VM6250 rear transition module plugs into the J0, J1 and J2 connectors, on the back side of the VMEbus backplane, in the same slot as the VM6250 board (see Figure 39).

To install the rear transition module:

1. Make sure the system and peripheral equipment power are off.
2. Install the cables into the appropriate connectors on the transition module (see section 6.2 page 89).
3. Line-up the RP0 and RP2 connectors (also named P0 and P2 in this chapter) on the rear transition module with the J0 and J2 connectors on the backplane.
4. Press the outer edge of the transition module until the board is firmly seated in the connector.
5. Connect any additional cables.
6. Turn on system power.

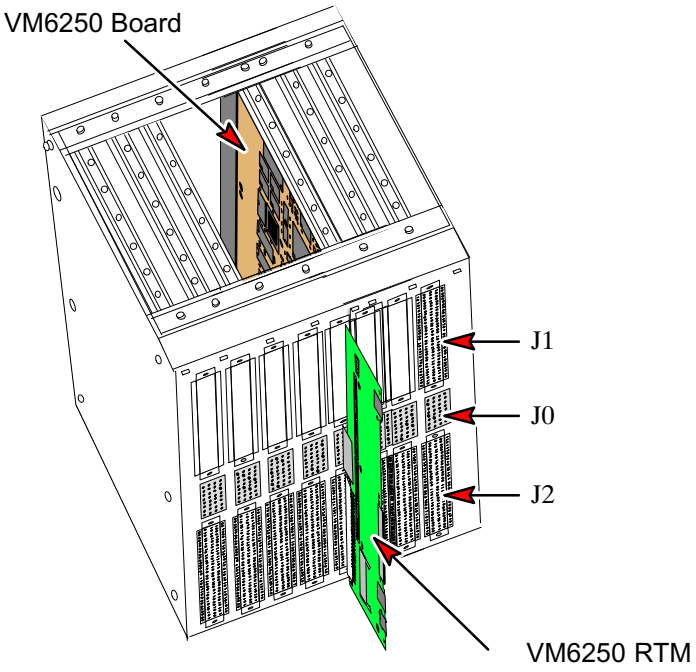


Figure 39: Installing the VM6250-RTM

6.2 Connectors

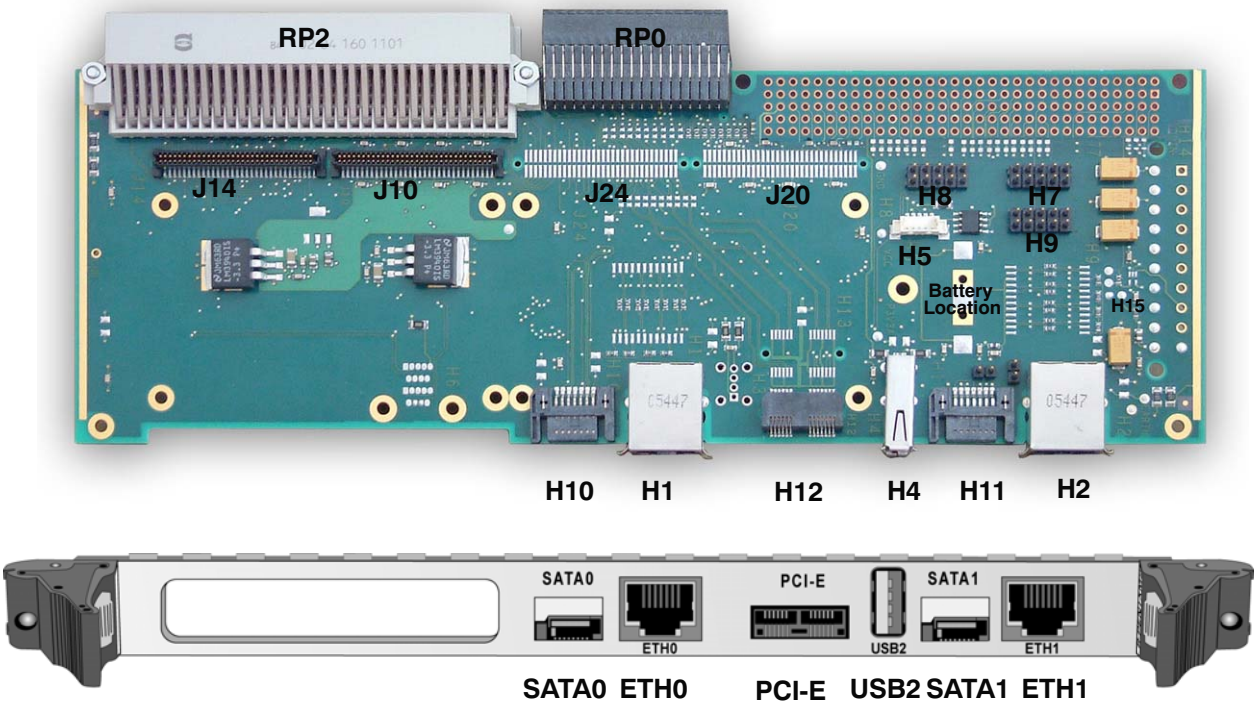


Figure 40: VM6250-RTM Connectors Location

6.2.1 RP0 Connector Pin Assignment

The RP0 connector has the same pin assignment as the P0 connector of the VM6250 board.

Refer to the “VME Bus Interface - P0 Connector" in section 2.8.5 page 40 for a complete information about the pin assignments of the RP0 connector.

6.2.2 RP2 Connector Pin Assignment

The RP2 connector has the same pin assignment as the P2 connector of the VM6250 board.

Refer to the “VME Bus Interface - P2 Connector" in section 2.8.7 page 46 for a complete information about the pin assignments of the RP2 connector.

6.2.3 H1 (ETHERNET 0) & H2 (ETHERNET 1) - Gigabit ETHERNET Connector

Routed from P0 to **H1** and **H2**, RJ-45 connectors (AMP - Part Number 106066-2).

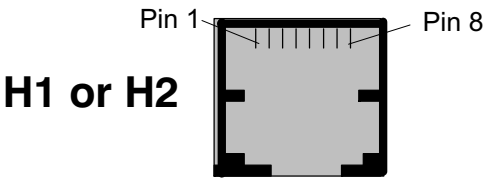
Available through the **ETH0** and **ETH1** RTM front panel connectors.

Connector Pin Assignment

Pin	Signal	Pin	Signal
1	BI_DA+	2	BI_DA-
3	BI_DB+	4	BI_DC+ (*)
5	BI_DC- (*)	6	BI_DB-
7	BI_DD+ (*)	8	BI_DD- (*)
9	Chassis Ground		

(*) : In 10BASE-T or 100BASE-T these signals are not used.

Type of Connector



Signal Description

Mnemonic	Signal Description
BI_DA+/-	In 1000BASE-T: First pair of Transmit/receive data In 10BASE-T/100BASE-TX: Pair of Transmit data
BI_DB+/-	In 1000BASE-T: Second pair of Transmit/receive data In 10BASE-T/100BASE-TX: Pair of Receive data
BI_DC+/-	In 1000BASE-T: Third pair of Transmit/receive data In 10BASE-T/100BASE-TX: Unused.
BI_DD+/-	In 1000BASE-T: Fourth pair of Transmit/receive data In 10BASE-T/100BASE-TX: Unused.

6.2.4 H4 (USB1) - USB Connector

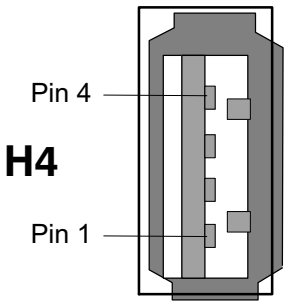
Routed from P0 to **H4**, a vertical USB connector.

Available through the **USB** RTM front panel connectors.

Connector Pin Assignment

Pin	Signal
1	+5 V Fused
2	USB1 DATA-
3	USB1 DATA+
4	GND
CASE	M GND

Type of Connector



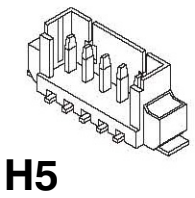
6.2.5 H5 - SMB Connector

Routed from P1 to **H5** (`MOLEX` - Part Number `53398-0590`)

Connector Pin Assignment

Pin	Signal
1	SMB_SCL
2	GND
3	SMB_SDA
4	N.C.
5	SMB_ALERT#

Type of Connector



Signal Description

Mnemonic	Signal Description
GND	Ground
N.C.	Not Connected
SMB_ALERT	System Management Bus - Alert
SMB_SCL	System Management Bus - Serial clock line from the SMBus master to SMBus slave devices.
SMB_SDA	System Management Bus - Bi-directional serial data line between the SMBus master and the SMBus slave device.

6.2.6 H7 (S0/COM1) & H8 (S1/COM2) - SERIAL Connector

Routed from P2 to **H7** and **H8**; individual 10-pin HE10 connectors



A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

H7 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	N.C.	2	S0_RX
3	S0_TX	4	N.C.
5	GND	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.

H8 Connector Pin Assignment

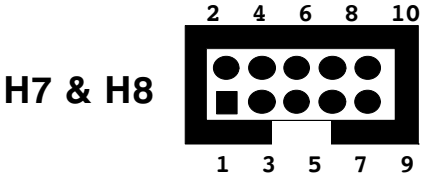
Pin	Signal	Pin	Signal
1	N.C.	2	S1_RX
3	S1_TX	4	N.C.
5	GND	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.

Signal Description

Mnemonic	Signal Description
GND	Ground
N.C.	Not Connected
S*x*_RX	Channel EIA-232 *x* Receive Data
S*x*_TX	Channel EIA-232 *x* Transmit Data

Type of Connector

Right angle HE10 10-pin connector, male, with board lock.



The H7 and H8 connectors can be connected via a NULL MODEM adapter on a VT100 console.

6.2.7 H9 - GPIOs and MISC Signals

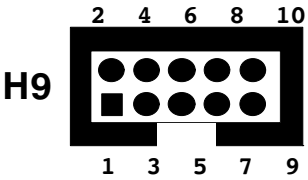
Routed from P0 to **H9**; individual 10 pins HE10 connector.

Connector Pin Assignment

Pin	Signal	Pin	Signal
1	6300 ESB GPIO41	2	N.C.
3	6300 ESB GPIO42	4	N.C.
5	6300 ESB GPIO43	6	N.C.
7	N.C.	8	GND
9	RESET#	10	GND

Type of Connector

Right angle HE10 10-pin connector, male, with board lock.



Signal Meaning

Mnemonic	Signal Description
6300 ESB GPIO*xx*	GPIO *xx* from 6300 ESB
GND	Ground
N.C.	Not Connected
RESET#	

6.2.8 H10 (SATA0) and H11 (SATA1) - Serial ATA Connector

Routed from P0 to **H10** and **H11**; SATA connector, right angle version with metal latch (MOLEX - Part Number 47080-4001)

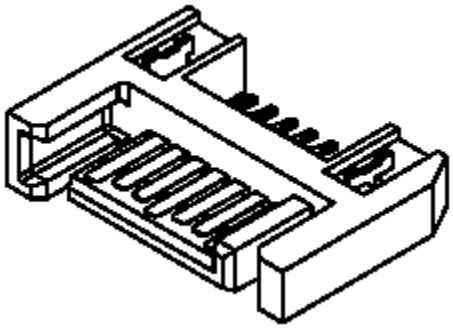
Available through the **SATA0** and **SATA1** RTM front panel connectors.

Note Depending on the SATA manufacturing option of the associated VM6250 board:
- Two SATA devices are available through the **SATA0** and **SATA1** RTM front panel connectors: SATA on P0 manufacturing option.
- Only one SATA device is available through the **SATA0** RTM front panel connectors: SATA onboard manufacturing option.

Connector Pin Assignment

Pin	Signal	Pin	Signal
1	GND	2	SATA*x* TX+
3	SATA*x* TX-	4	GND
5	SATA*x* RX-	6	SATA*x* RX+
7	GND		

Type of Connector



Signal Description

Mnemonic	Signal Description
GND	Ground
SATA*x* RX+/RX-	Serial ATA *x* Receive +/-
SATA*x* TX+/TX-	Serial ATA *x* Transmit +/-

6.2.9 H12 - PCI Express Connector

Routed from P0 connector to **H12**, a 26-pin right angle connector (SAMTEC - Order Code MEC8-RA)

Available through the **PCI-E** RTM front panel connectors.

Connector Pin Assignment

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PEX RXL0+	4	PEX TXL0+
5	PEX RXL0-	6	PEX TXL0-
7	GND	8	GND
9	PEX RX1L+	10	PEX TXL1+
11	PEX RXL1-	12	PEX TXL1-
13	GND	14	GND
15	PEX RXL2+	16	PEX TXL2+
17	PEX RXL2-	18	PEX TXL2-
19	GND	20	GND
21	PEX RXL3+	22	PEX TXL3+
23	PEX RXL3-	24	PEX TXL3-
25	GND	26	GND

Type of Connector



Signal Meaning

Mnemonic	Signal Description
PEX RXL[0..3]+/-	x4 PCI Express Link - Differential Receive Lane [0..3]
PEX TXL[0..3]+/-	x4 PCI Express Link - Differential Transmit Lane [0..3]
GND	Ground

6.2.10 7PCI 64 PIM Site 1 Connector

J14 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	PMC64 IO 01	2	PMC64 IO 02
...	...	...	...
63	PMC64 IO 63	64	PMC64 IO 64

Signal Description

Mnemonic	Signal Description
PMC64 IO *xx*	I/O 01 through 64 of the motherboard PMC: J14[01 ... 64] for PMC Site 1
N.C.	Not Connected

Known Limitations

- 4.8 mm high components have been placed under PIM site 1. This trangresses the VITA 36 standard which specifies 2.5 mm. Some PIMs may not fit in this site.

J10 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	N.C.	4	N.C
5	+5V	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	+3.3V
11	N.C.	12	N.C.
13	GND	14	N.C.
15	N.C.	16	N.C.
17	N.C.	18	GND
19	N.C.	20	N.C.
21	+5V	22	N.C.
23	N.C.	24	N.C.
25	N.C.	26	+3.3V
27	N.C.	28	N.C.
29	GND	30	N.C.
31	N.C.	32	N.C.
33	N.C.	34	GND
35	N.C.	36	N.C
37	+5V	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	+3.3V
43	N.C.	44	N.C.
45	GND	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	GND
51	N.C.	52	N.C.
53	+5V	54	N.C.
55	N.C.	56	N.C.
57	N.C.	58	+3.3V
59	N.C.	60	N.C.
61	N.C.	62	N.C.
63	N.C.	64	N.C.

6.2.11 PCI 64 PIM Site 2 Connector



Up to PBV36-P0-VM6-00 Rev. C, the pinout of J20 and J24 connectors is reserved. If available, do not try to use these connectors.



From PBV36-P0-VM6-00 Rev. C, the pinout of the J20 and J24 connectors is available. See sections J24 and J20 Connector Pin Assignment below.



Installation of a PIM on the Site 2 of a PBV36-P0-VM6-00 Rev C. requires specific adjustments:
- removing H10 (SATA0), H1 (ETH0) and H12 (PCI-E) connector on the RTM,
- usage of a RTM specific front panel.

Contact your Kontron representative for more information on this topic.

J24 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	PMC64 IO 01	2	PMC64 IO 02
...	...	...	...
63	PMC64 IO 63	64	PMC64 IO 64

Signal Description

Mnemonic	Signal Description
PMC64 IO *xx*	I/O 01 through 64 of the motherboard PMC: J24[01 ... 64] for PMC Site 2
N.C.	Not Connected

Known Limitations

- The RTM does not include the 3 mm recess at the rear card edge on the area of PIM Site as required by VITA 36 standard. This may require removal or loosening of the rear panel in order to remove and install a PIM at Site 2.

J20 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	N.C.	4	N.C
5	+5V	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	+3.3V
11	N.C.	12	N.C.
13	GND	14	N.C.
15	N.C.	16	N.C.
17	N.C.	18	GND
19	N.C.	20	N.C.
21	+5V	22	N.C.
23	N.C.	24	N.C.
25	N.C.	26	+3.3V
27	N.C.	28	N.C.
29	GND	30	N.C.
31	N.C.	32	N.C.
33	N.C.	34	GND
35	N.C.	36	N.C
37	+5V	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	+3.3V
43	N.C.	44	N.C.
45	GND	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	GND
51	N.C.	52	N.C.
53	+5V	54	N.C.
55	N.C.	56	N.C.
57	N.C.	58	+3.3V
59	N.C.	60	N.C.
61	N.C.	62	N.C.
63	N.C.	64	N.C.

6.2.12 Reset

The front panel reset toggle switch can be set to the RESET position to generate an hard reset.

6.2.13 Mechanical Ground

One HE10 2-pin connector is placed on the board to allow to hard connect electrical (GND) and mechanical (EARTH) grounds.

While adding a jumper on connector, both ground signals are tighten together.

» H15 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	EARTH	2	GND

» Signal Meaning

Mnemonic	Signal Description
EARTH	Electrical Ground
GND	Mechanical Ground

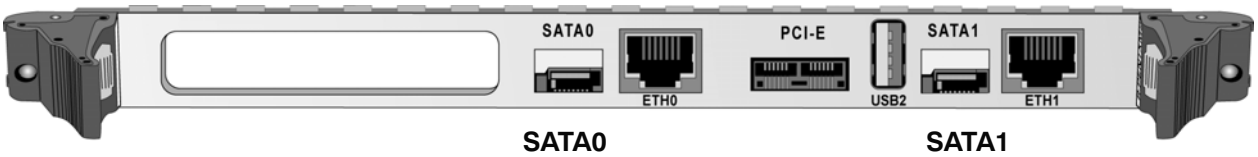
A metalized mechanical hole (3mm diameter) is located on the board to allow to fix an electrical pod in order to bring the mechanical ground from the chassis.

6.2.14 Power Supplies

- Two 800 mAmp voltage regulators are used on the board to provide 3.3V power supply to each PIM site.
- A standard lithium battery to supply CPU board's RTC is also available.

6.3 Cables

6.3.1 SATA Cable



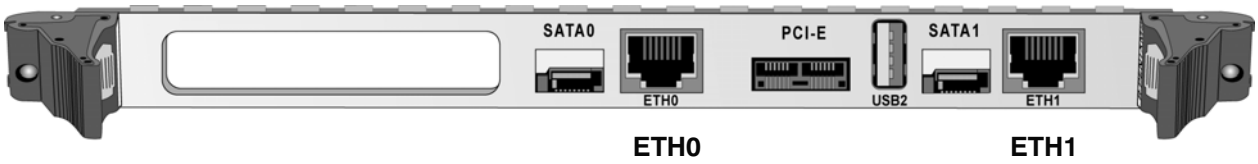
Recommended SATA II cable for data rate up to 3 Gbps:

- Manufacturer: MOLEX
- Part No: 88762-5410.



Figure 41: Serial ATA Cable

6.3.2 Ethernet Cable



Gigabit Ethernet standard cable:
1000BASE-T requires category 5e, 5+ or 6 copper cable, with a maximal length of 100m for an UTP or FTP cable, and 150m for a STP or FSTP cable.

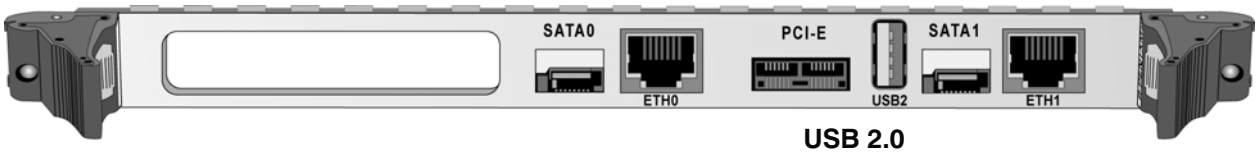


Figure 42: Gigabit Ethernet Cable

6.3.3 PCI-Express Cable

Please contact your Kontron representative for more information on this topic.

6.3.4 USB 2.0 Cable



USB 2.0

USB 2.0 standard cable



USB series “A" plug and receptacle

Figure 43: USB 2.0 Cable

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