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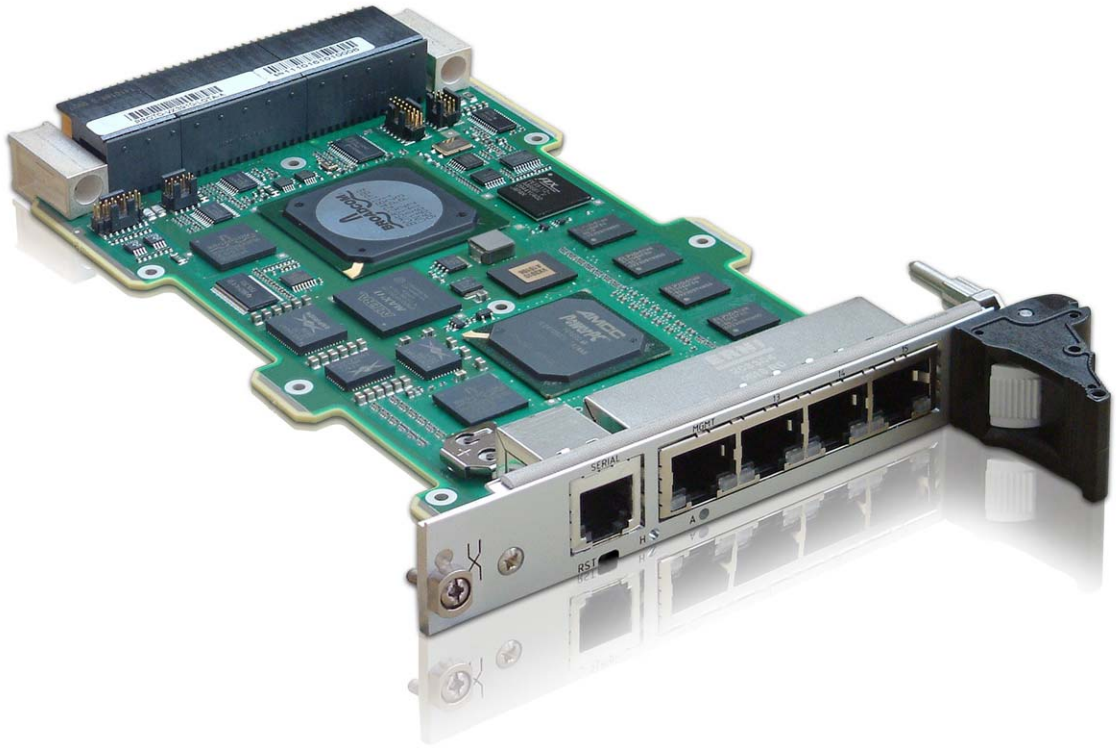
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» VX3910 «



High-performance OpenVPX Switch
User's Guide

CA.DT.A81-3e - June 2014

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Revision History

Publication Title:	VX3910 User's Guide	
Doc. ID:	CA.DT.A81-3e	
Rev.	Brief Description of Changes	Date of Issue
3e	Update of: - Order Codes - Figure 6: Functional Block Diagram - Figure 7: BCM56224B Block Diagram - Table 8: BCM56224B Port Mapping - Section 3.5.3.2: P1 connector New section: 4.5 - Firmware Evolution	06-2014
2e	Weight and MTBF information added (sub-section 1.3.3 and 1.3.10). Section RC Characteristics added.	03-2011
1e	Updates after review	10-2010
0e	Initial Issue	09-2010

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- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

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Conventions

This guide uses several types of notice: Note, Caution, ESD.



Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.



When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

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Special Handling and Unpacking Instructions



ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction.

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Chapter 1 - Introduction

1.1 Product Overview

The VX3910 is a Standard Fabric 3U OpenVPX Gigabit Ethernet Switch with 24 channels providing Layer 2 and Layer 3 switching/routing functions in a 3U VPX compliant form factor.

The product features 24 x 1000BASE-BX ports to the VPX backplane plus 3 x 1 GbE front panel Interfaces.

1.1.1 VX3910 Features

The board is composed of the following building blocks:

- Ethernet Infrastructure
- Unit Computer and Memory
- Glue Logic
- JTAG

Ethernet Infrastructure

- Gigabit Ethernet Multilayer Switch:
  - Broadcom StrataXGS® BCM56224B
  - 28 ports 1 GbE
  - 16K Layer2 Table, 2K Filter Processor memory, 1K Layer2 Multicast Tables
  - 4K Layer3 Table entries
  - 32-bit/66 MHz PCI management interface
- Front 10/100/1000BASE-T uplinks

Unit Computer and Memory

- PowerPC IBM PPC405EX 600 MHz
- Used for switch provisioning and diagnostics
- 512 MB DDR2 RAM 200 MHz
- 64 MB NOR Flash
- 1 GB NAND Flash
- Real Time Clock
- Temperature Sensor

Power Supply

- The VPX backplane connector supports the following main supplies: 5.0V.
- In addition, auxiliary voltages 3.3V is supported.

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Miscellaneous

- Management connection to Unit Computer via EIA-232 front RJ11
- Management connection to Unit Computer using front 10/100/1000BASE-T management port
- Management connection to Unit Computer via EIA-232 at P2
- FRU data storage (serial ID) in Unit Computer NOR Flash
- Board support package includes WindRiver Linux, device drivers, protocol stacks bootloader and power-on self-tests
- Standard Air (SA) and Rugged Conduction-Cooled (RC) builds

1.1.2 General Compliances

The board is compatible to the following standards:

- IEEE 802.3, 2000
- IEEE 802.3ae, 2002
- VITA 46.0 VPX Base Specification
- ANSI/VITA 65-2010 OpenVPX System Specification

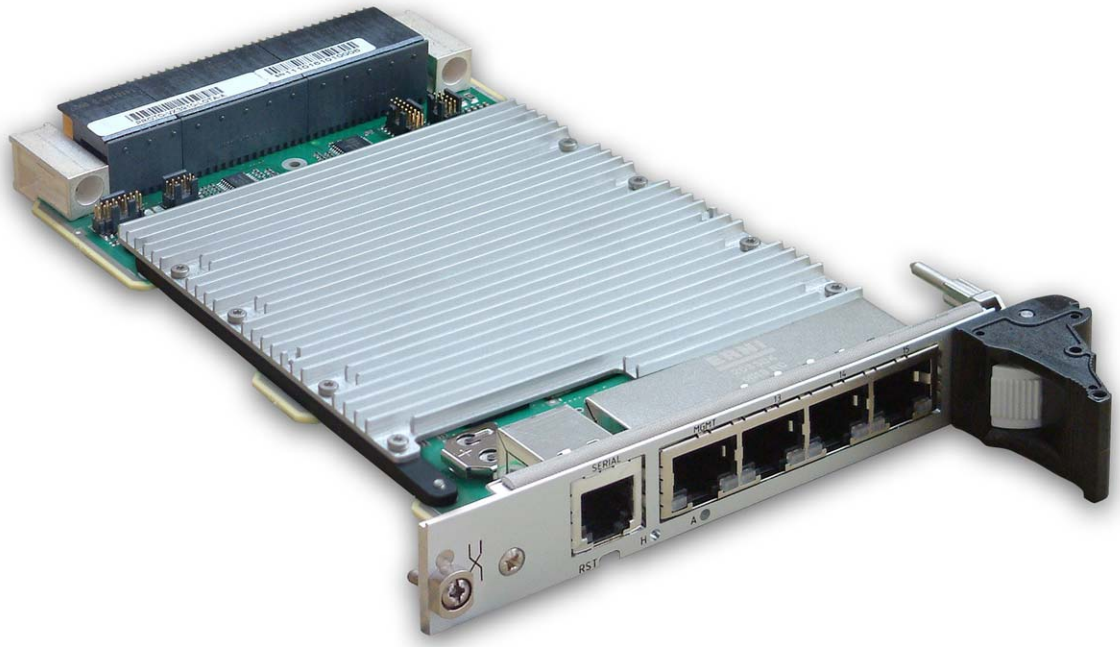


Figure 1: VX3910-SA Overview

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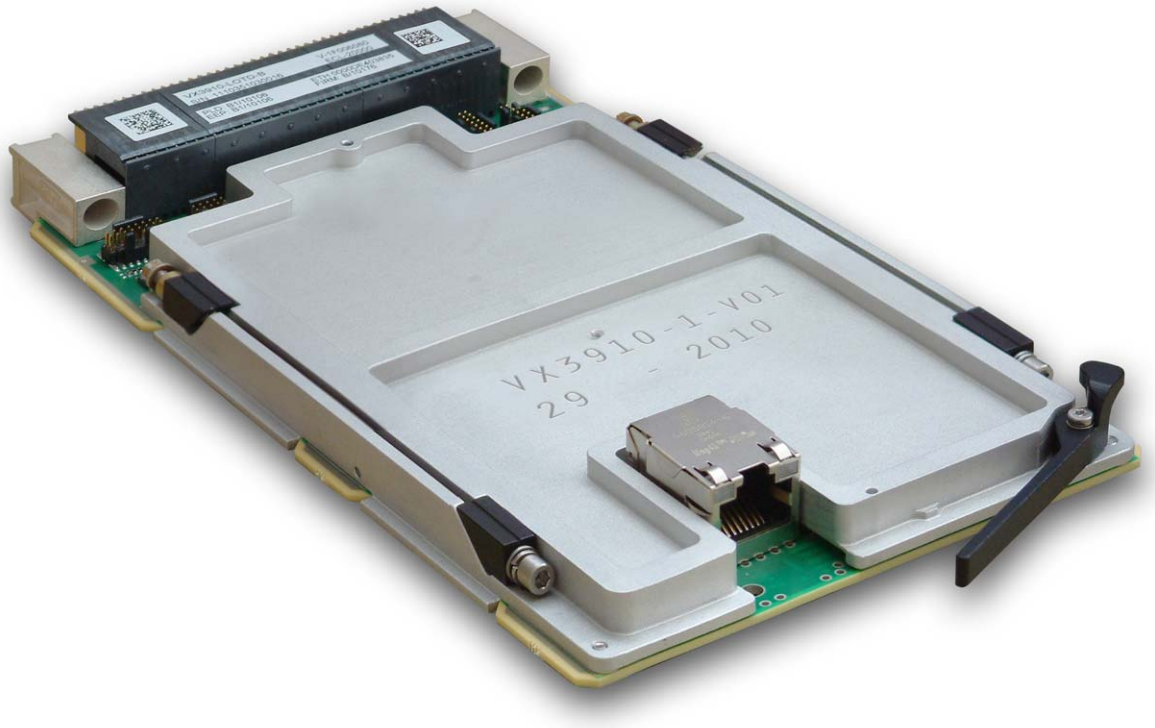


Figure 2: VX3910-RC Overview

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1.2 Ordering Information

Manufacturing Options

- Rear Panel Interfaces: Option 1: 24x 1000BASE-BX
  Option 2: 22x 1000BASE-BX + 1x 1000BASE-T
- Front Panel Size 0.8 inch
  1 inch
- Ruggedization Levels: Standard Air-Cooled (SA)
  Rugged Conduction-Cooled (RC)

Order Code Available

Order Code		Description
SA - Standard Commercial		
VX3910-SA	VX3910-SA-B0200	3U VPX Ethernet Switch Rear Panel Interfaces: 22x 1000BASE-BX + 1x 1000BASE-T Front Panel Interfaces: 3x 1000BASE-T Front Panel size: 0.8 inch Standard Air-Cooled build
VX3910-SA	VX3910-SA-B1200	3U VPX Ethernet Switch Rear Panel Interfaces: 22x 1000BASE-BX + 1x 1000BASE-T Front Panel Interfaces: 3x 1000BASE-T Front Panel size: 1 inch Standard Air-Cooled build
VX3910-SA	VX3910-SA-B0400	3U VPX/OpenVPX Ethernet Switch Compliant wiht slot profile: SLT3-SWH-2F24U Rear Panel Interfaces: 24x 1000BASE-BX Front Panel Interfaces: 3x 1000BASE-T Front Panel size: 0.8 inch Standard Air-Cooled build
VX3910-SA	VX3910-SA-B1400	3U VPX/OpenVPX Ethernet Switch Compliant wiht slot profile: SLT3-SWH-2F24U Rear Panel Interfaces: 24x 1000BASE-BX Front Panel Interfaces: 3x 1000BASE-T Front Panel size: 1 inch Standard Air-Cooled build
RC - Rugged Conduction-Cooled		
VX3910-RC	VX3910-RC-BN200	3U VPX Ethernet Switch Rear Panel Interfaces: 22x 1000BASE-BX + 1x 1000BASE-T Rugged Conduction-Cooled build
VX3910-RC	VX3910-RC-BN400	3U VPX/Open VPX Ethernet Switch Compliant wiht slot profile: SLT3-SWH-2F24U Rear Panel Interfaces: 24x 1000BASE-BX Rugged Conduction-Cooled build

Table 1: Ordering Information

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1.3 Technical Specification

1.3.1 Power

Supply voltages are:

> 5 Volts

Power consumption of the VX3910:

> Idle (no links): 15W
> Typical: 20W
> Maximum (full traffic/load): 25W

1.3.2 Mechanics

> 3U VPX board occupying 1 slot (4 HP)
> 100 mm (H) x 160 mm (D)
> The SA board uses standard VPX front panel (0.8 inch or 1 inch depending on manufacturing option) and handles.

1.3.3 Weight

> Standard Air, without heatsink: 189g
> Standard Air, with heatsink: 252g
> Rugged Conduction-Cooled: 324g

1.3.4 Environmental Specifications

ENVIRONMENTAL SPECIFICATIONS		
	SA - Standard Commercial	RC - Rugged Conduction-Cooled
Conformal Coating	Optional	Standard
Airflow	1 m/s (4 CFM)	N.A.
Temperature	VITA 47-Class AC1	VITA 47-Class CC4
Cooling Method	Convection	Conduction
Operating	0°C to +55°C	-40°C to +85°C
Storage	-45°C to +85°C	-45°C to +100°C
Vibration Sine (Operating)	2g / 20-500 Hz acceleration / frequency range	5g / 22-2,000 Hz acceleration / frequency range
Random	VITA 47-Class V1	VITA 47-Class V3
Shock (Operating)	20g / 11 ms peak accel. / shock duration half sine	40g / 20 ms peak accel. / shock duration half sine
Altitude (Operating)	-1,640 to 15,000 ft	-1,640 to 60,000 ft
Relative Humidity	90% non-condensing	95% non-condensing

Table 2: Environmental Specifications

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1.3.5 Safety

The board is designed to meet the following requirements:

- UL 60950, 3rd edition (US and Canada)
- EN 60950 (Europe)
- LVD 73/23/EEC (Europe)
- Denan Law (Japan Safety)

The board is designed to meet the following flammability requirement (as specified in telcordia GR-63-CORE):

- UL 94V-0/1 with Oxygen index of 28% or greater material

1.3.6 Electromagnetic Compatibility

The board is designed to meet or exceed class B limit of the following specifications/requirements (assuming an adequate system/chassis):

- FCC 47 CFR Part 15, Subpart B (USA)
- EMC Directive 89/336/EEC (Europe)
- EN55022 (Europe)
- EN55024 (Europe)
- EN61000-6-3 (Europe)
- EN61000-6-2 (Europe)
- CISPR22
- VCCI (Voluntary Japan Electromagnetic Compatibility requirement)
- EN 300 386, Electro-Magnetic Compatibility (EMC) Requirements for Public Telecommunication Network Equipment: Electromagnetic Compatibility (EMC) Requirements

1.3.7 WEEE

Compliant to:

- Directive 2002/96/EC: Waste electrical and electronic equipment

1.3.8 RoHS

Compliant to:

- Directive 2002/95/EC: Restriction of the use of certain hazardous substances in electrical and electronic equipment

1.3.9 Lead-free

The product has to be completely lead-free concerning the production process and the components used.

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1.3.10 Reliability / MTBF

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign GB
- Air Inhabited Cargo AIC
- Naval Sheltered NS
- Air Rotary Wing ARW

VX3910-SA-B0200

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
Order Code: VX3910-SA-B0200	273 676	202 682	45 126	52 955	45 446	12 945

Table 3: VX3910-SA MTBF Data

VX3910-RC-BN200

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
Order Code: VX3910-BN200	408 342	291 954	65 271	80 800	66 247	16 014

Table 4: VX3910-RC MTBF Data

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1.4 Software Support

The following table contains information related to software supported by the VX3910.

VX3910	SPECIFICATIONS
General	- Reliable field upgrades for all software components - Dual boot images with roll-back capability - Management via SNMP and Command Line Interface - System access via TELNET, SSH and serial line
Ethernet/Bridging	- Static link aggregation (IEEE 802.3ad) - Classic and rapid spanning tree algorithms (IEEE 802.1D, IEEE802.1w) - Multiple Spanning Tree (IEEE 802.S) - Quality Of Service on all ports (IEEE 802.1p) - Full Duplex operation and flow control on all ports (IEEE 802.3x) - Static MAC filtering - Port Authentication (IEEE 802.1X) - Auto negociation of speeds and operational mode on all external copper GE interfaces as well as on all base fabric interfaces - Layer 2 multicast services using GARP/GMRP (IEEE 802.1p) - VLAN support including VLAN tagging (IEEE 802.3ac), dynamic VLAN registration with GARP/GVRP (IEEE 802.31Q) and Protocol based VLANs (IEEE 802.1v) - Double VLAN tagging - Port Mirroring
QoS	- CoS (Class of Service) - DifffServ (Differentiated Services) - ACL (Access Control List)
Applications	- SNTP client for retrieving accurate time and date information - DHCP server - Onboard event management - Test and trace facilities - POST (power on self tests) diagnostics - Standards based SNMP implementation supporting SNMP v1, v2 and v3 for monitoring and management purposes - Persistent storage of configuration across restarts - Support for retrieving and installing multiple configurations
Supported MIBs	- For a list of supported MIBs, see Chapter 4.2

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VX3910	SPECIFICATIONS
Bootloader	- U-Boot Version 1.3.4 - POST - Multi-image support - Reliable field upgradable - H/W protected - KCS interface to PM - Serial console support
Operating System	- Wind River PNE 2.0

Table 5: VX3910 Software Specification

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Chapter 2 - Installation

The VX3910 has been designed for easy installation. However, the following standard precautions, installations procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VX3910. Kontron assumes no responsibility for any damage resulting from



Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.



Be careful when inserting or removing the VX3910. The SFP cages have sharp edges which might lead to injuries.



ESD Equipment!
This VPX board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:
- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Don't touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.
- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.

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2.2 VX3910 Identification

The VX3910 boards are identified by labels fitted to the top side.

A "Order Code, Variant, Serial Number and E.C. Level" labels (Versions Text and 2D available).

B "PLD, Ethernet Address, EEP and Firmware" labels (Versions Text and 2D available).



Figure 3: VX3910 Identification (Top Side)

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2.3 VX3910 Configuration

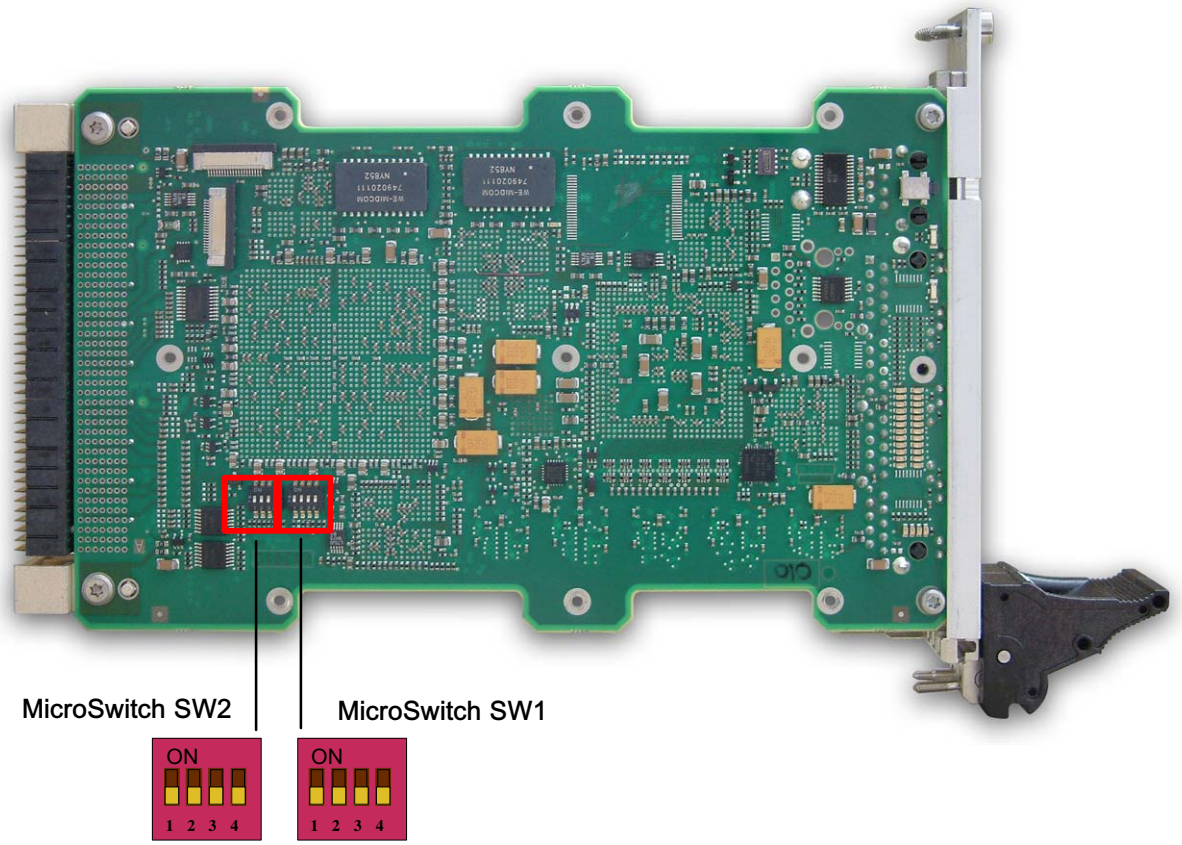


Figure 4: Microswitches Location

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2.3.1 Microswitch SW1 Description

Function	Description
1 - ETH15_LAN_SWITCH	ETH15 location **on**: rear panel **off**: front panel (**default**)
2 - Reserved	
3 - CC_SEL	**PCIe Common Clock Selection** **on**: Internal reference clock or P1 reference clock **off**: Internal reference clock or P0 reference clock (**default**)
4 - Maskablereset#	**Maskablereset# propagation** **on**: Maskablereset propagated to CPLD **off**: Maskablereset not propagated to CPLD (**default**)

Table 6: Microswitch SW1 Description

2.3.2 Microswitch SW2 Description

Function	Description
1 - P0_SEL	**PCIe VPX Common Clock Reference #1** **on**: P0 Clock **off**: Internal Clock (**default**)
2 - P1_SEL	**PCIe VPX Common Clock Reference #2** **on**: P1 Clock as Common Clock Reference **off**: P1 as output PCIe VPX Common Clock (**default**)
3 - CLK_EN0	**P1 PCIe VPX Clock[3..0] Generation** **on**: Enable **off**: Disable (**default**)
4 - CLK_EN1	**P1 PCIe VPX Clock[7..4] Generation** **on**: Enable **off**: Disable (**default**)

Table 7: Microswitch SW2 Description

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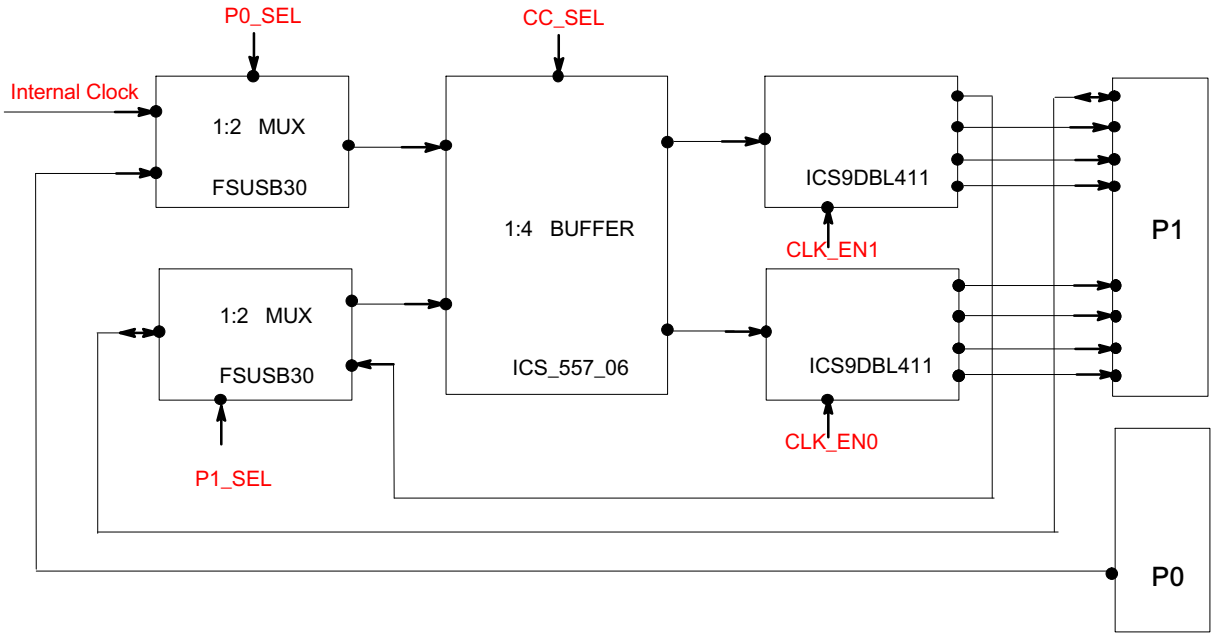


Figure 5: VPX Clock Diagram

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2.4 VX3910 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX3910 in a system. Procedures for standard removal operations are found in section 2.5 Standard Removal Procedures

To perform an initial installation of the VX3910 in a system proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1 Safety Requirements are observed.

   
   Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX3910 refer to the CLI Reference Manual.

   
   Care must be taken when applying the procedures below to ensure that neither the VX3910 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX3910 perform the following:
   - > Ensure that no power is applied to the system before proceeding.
   - > Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

     
     DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   - > Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
   - > Fasten the front panel retaining screws.
   - > Connect all external interfacing cables to the board as required.
   - > Ensure that the board and all required interfacing cables are properly secured.
4. The VX3910 is now ready for operation.

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2.5 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1 Safety Requirements are observed.

   
   Care must be taken when applying the procedures below to ensure that neither the VX3910 nor other system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.

   
   Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Dispose of the board as required.

2.6 Software Installation

The VX3910 comes as a pre-installed system with all necessary OS, filesystem, drivers and applications factory-installed with default configurations.

Updating the Software with new operating system or applications or new versions is provided by a dedicated update mechanism, which is described in Chapter 4 page 43.

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2.7 Quick-Start

This section gives instructions for (initially) accessing the CLI (Command Line Interface) of the VX3910 using either in-band access via the ethernet fabric or the out-of-band management interfaces (serial port or Fast Ethernet) accessible from the front plate serial connector or via an appropriate RIO module. The CLI is required for configuring the GbE switch.

2.7.1 Out-of-Band CLI Access

The CLI can be accessed via serial port (using the front plate connector and provided adapter or an appropriate RIO module) or Fast Ethernet (via the front plate RJ45 connector).

2.7.1.1 Serial Port

The serial port is ready to use offhand without further configuration.

Port settings are:

- 115200 bps (serial speed might be different for customized board variants)
- 8 bit, no parity, 1 stop bit (8N1)
- no flow control

2.7.1.2 Fast Ethernet Serviceport

The Gigabit Ethernet serviceport on the VX3910 front plate has no IP address set by default, it is necessary to assign an IP address statically or enable dhcp on the serviceport. Because the required configuration steps are done in the CLI, an initial access using the serial port is required.

The procedure for assigning an IP address to the serviceport is described in the following. User input is printed in bold letters.

1. Connect to serial port on the front plate (using the Kontron DB9 adapter cable) or RIO module (using a RJ45 straight cable).
2. Ensure that the board is powered up.
3. Log in as admin and enter privileged mode by typing 'enable' (no passwords required by default).

```
User:admin
Password:
(Ethernet Fabric) >enable
Password:


(Ethernet Fabric) #
```

4. Set IP address and netmask. (see below for an example IP address setting)

```
(Ethernet Fabric) #serviceport ip 192.168.50.107 255.255.255.0
```

The GbE management interface is available from now on.

Alternatively, DHCP can be set for the serviceport

```
(Ethernet Fabric) #serviceport protocol dhcp
```

An IP address will be assigned to the serviceport by a DHCP server.

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5. Save configuration using the ‘write mem’ command and confirm with ’y’’

```
(Ethernet Fabric) #write mem


This operation may take a few minutes.
Management interfaces will not be available during this time.


Are you sure you want to save? (y/n) y


Config file ´current/startup-config´ created successfully.


Configuration Saved!


(Ethernet Fabric) #
```

To access the CLI via Fast Ethernet serviceport, open a telnet connection to the configured IP address, port 23.

2.7.2 In-Band CLI-Access

The GbE switch network port (in-band management access) on the VX3910 has no IP address set by default, it is necessary to assign an IP address either statically or by using DHCP to the network port. Because the required configuration steps are done in the CLI, an initial access using the serial port is required.

The procedure for assigning an IP address to the network port is described in the following. User input is printed in bold letters.

1. Connect to serial port on the front plate (using the Kontron DB9 adapter cable) or RIO module (using a RJ45 straight cable).
2. Ensure that the board is powered up.
3. Log in as admin and enter privileged mode by typing ’enable’ (no passwords required by default).

```
User:admin
Password:
(Ethernet Fabric) >enable
Password:


(Ethernet Fabric) #
```

4. Set IP address, netmask and default gateway. (see below for an example IP address setting)

```
(Ethernet Fabric) #network parms 192.168.50.107 255.255.255.0 192.168.50.254
```

The GbE management interface is available from now on.

Alternatively, DHCP can be set for the network port

```
(Ethernet Fabric) #network protocol dhcp
```

An IP address will be given to the network port by a DHCP server.

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5. Save configuration using the ‘write mem’ command and confirm with ’y’’

```
(Ethernet Fabric) #write mem

This operation may take a few minutes.
Management interfaces will not be available during this time.

Are you sure you want to save? (y/n) y

Config file ´current/startup-config´ created successfully.

Configuration Saved!

(Ethernet Fabric) #
```

To access the CLI via Fast Ethernet networkport, open a telnet connection to the configured IP address, port 23.

It might make sense to separate the management network from the data path by setting appropriate VLANs

For additional information on the system configuration, refer to the VX3910 CLI Reference Manual.

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Chapter 3 - Functional Description

The board is composed of the following building blocks:

- Ethernet Infrastructure
- Unit Computer and Memory
- Glue Logic
- JTAG

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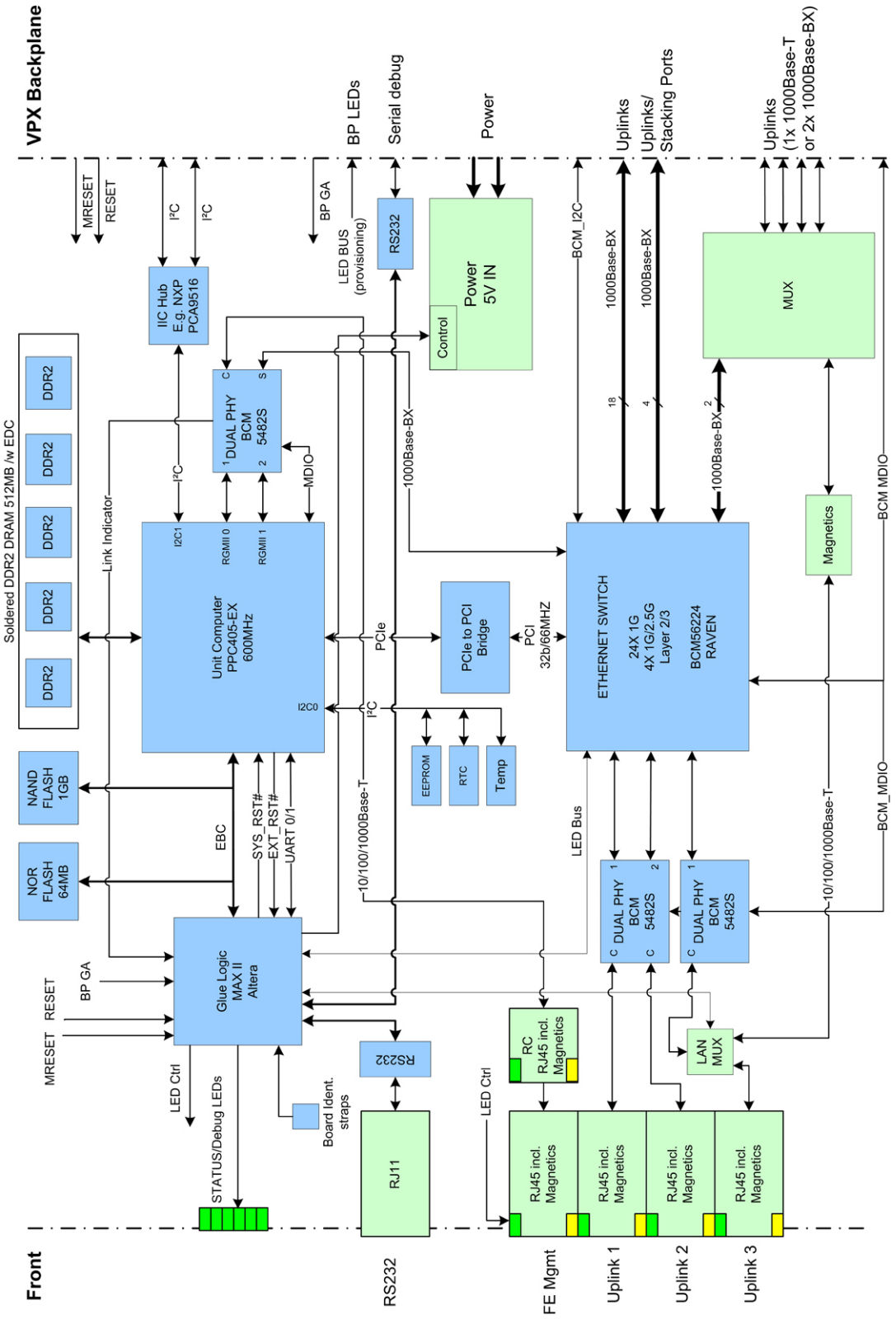


Figure 6: Functional Block Diagram VX3910

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3.1 Ethernet Infrastructure

3.1.1 Gigabit Ethernet Multilayer Switch Device

The Gigabit Ethernet Multilayer Switch device is a Broadcom BCM56224B. The BCM56224B is a highly integrated and cost-effective multilayer Ethernet switch from the Broadcom StrataXGS® product line. It is a single-chip solution with a high-performance 32-bit MIPS CPU and 28 GbE ports.

Common Features:

- 24 ports 1 GbE
- 16K Layer 2 Tables, 2K Filter Processor memory, 1K Layer 2 Multicast Tables.
- 4K Layer3 Table entries
- 32-bit/66 MHz PCI management interface
- LED-Bus
- JTAG
- 1152-pin BGA

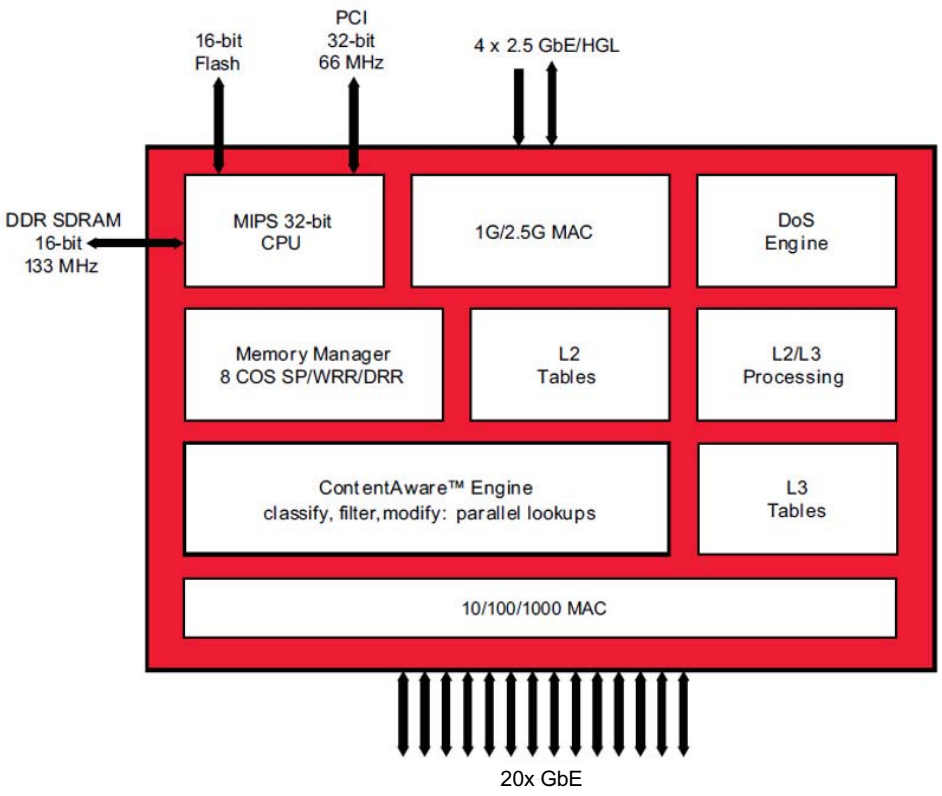


Figure 7: BCM56224B Block Diagram

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CLI	BCM Port	Option1: 24x 1000BASE-BX	Option 2: 22x 1000BASE-BX + 1x 1000BASE-T	Interface	Speed Settings
0/1	CH1	Bakplane P2 wafer 14	Bakplane P2 wafer 14	1000BASE-BX	1000 Mbps
0/2	CH2	Bakplane P2 wafer 13	Bakplane P2 wafer 13	1000BASE-BX	1000 Mbps
0/3	CH3	Bakplane P2 wafer 12	Bakplane P2 wafer 12	1000BASE-BX	1000 Mbps
0/4	CH4	Bakplane P2 wafer 11	Bakplane P2 wafer 11	1000BASE-BX	1000 Mbps
0/5	CH5	Bakplane P2 wafer 10	Bakplane P2 wafer 10	1000BASE-BX	1000 Mbps
0/6	CH6	Bakplane P2 wafer 9	Bakplane P2 wafer 9	1000BASE-BX	1000 Mbps
0/7	CH7	Bakplane P2 wafer 8	Bakplane P2 wafer 8	1000BASE-BX	1000 Mbps
0/8	CH8	Bakplane P2 wafer 7	Bakplane P2 wafer 7	1000BASE-BX	1000 Mbps
0/9	CH9	Bakplane P2 wafer 6	Bakplane P2 wafer 6	1000BASE-BX	1000 Mbps
0/10	CH10	Bakplane P2 wafer 5	Bakplane P2 wafer 5	1000BASE-BX	1000 Mbps
0/11	CH11	Bakplane P2 wafer 4	Bakplane P2 wafer 4	1000BASE-BX	1000 Mbps
0/12	CH12	Bakplane P2 wafer 3	Bakplane P2 wafer 3	1000BASE-BX	1000 Mbps
0/13	CH13	Front panel RJ-45 Port 13	Front panel RJ-45 Port 13	1000BASE-T	10/100/1000 Mbps
0/14	CH14	Front panel RJ-45 port 14	Front panel RJ-45 port 14	1000BASE-T	10/100/1000 Mbps
0/15	CH15	Front panel RJ-45 Port 15	Front panel RJ-45 Port 15 or Backpake P2 wafers 15 and 16 (2)	1000BASE-T	10/100/1000 Mbps
0/16	CH16	Bakplane P2 wafer 2	Bakplane P2 wafer 2	1000BASE-BX	1000 Mbps
0/17	CH17	Bakplane P2 wafer 1	Bakplane P2 wafer 1	1000BASE-BX	1000 Mbps
0/18	CH18	Bakplane P1 wafer 16	Bakplane P1 wafer 16	1000BASE-BX	1000 Mbps
0/19	CH19	Bakplane P1 wafer 15	Bakplane P1 wafer 15	1000BASE-BX	1000 Mbps
0/20	CH20	Bakplane P1 wafer 14	Bakplane P1 wafer 14	1000BASE-BX	1000 Mbps
0/21	CH21	Bakplane P1 wafer 13	Bakplane P1 wafer 13	1000BASE-BX	1000 Mbps
0/22	CH22	Bakplane P2 wafer 15	-	1000BASE-BX	1000 Mbps
0/23	CH23	Bakplane P2 wafer 16	-	1000BASE-BX	1000 Mbps
0/24	CH0 (1)	Unit Computer Link	Unit Computer Link	1000BASE-BX	1000 Mbps
0/25	UCH0 (3)	Bakplane P1 wafer 12	Bakplane P1 wafer 12	1000BASE-BX	1000 Mbps
0/26	UCH1 (3)	Bakplane P1 wafer 11	Bakplane P1 wafer 11	1000BASE-BX	1000 Mbps
0/27	UCH2 (3)	Bakplane P1 wafer 10	Bakplane P1 wafer 10	1000BASE-BX	1000 Mbps
0/28	UCH3 (3)	Bakplane P1 wafer 9	Bakplane P1 wafer 9	1000BASE-BX	1000 Mbps

(1) CH0 is the internal link between the CPU and the switch

(2) Depending on the SW1_1 microswitch configuration
(refer to section 2.2 “VX3910 Configuration” page 11)

(3) UCH3 ... UCH0 are the four ports for 1 Gigabit Ethernet (GbE) uplink/stacking

Table 8: BCM56224B Port Mapping

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3.1.1.1 PCI

The switch uses the 32-bit/66 MHz PCI management interface and it is the device0 (IDSEL is connected to AD16 at the PCI Bridge).

3.1.1.2 Management Data Input/Output (MDIO)

The MDIO interface is connected to two BCM5482S, dual-port 10/100/1000BASE-T gigabit ethernet transceivers.

3.1.1.3 JTAG

The JTAG Interface is connected to the JTAG chain on the VX3910. JTDI is connected to the TDO from the preceding device (PCIe to PCI Bridge) in the JTAG chain and JTDO is connected to the following device (BCM5482S) in the JTAG chain. The signals JTMS, JTCK and JTRST are connected to all JTAG chain devices. TRST is pulled low to keep the TAP controller in the switch in reset during normal operation. JTCE is pulled low during normal operation.

3.1.1.4 LED bus

The LED bus is connected to the CPLD. The CPLD controls the front LEDs at the VX3910 front panel.

3.1.2 10/100/1000BASE-T Gigabit Ethernet Interfaces

The VX3910 supports up to 3 10/100/1000Base-T interfaces. The table below shows the possible configurations depending on the board order code and configuration.

Order Code	Port 1	Port 2	Port 3
VX3910-SA-B*x*200 SW1_1 set to: **off**: front panel	Front Panel, port 13	Front Panel, port 14	Front Panel, port 15
VX3910-SA-B*x*200 SW1_1 set to: **on**: rear panel	Front Panel, port 13	Front Panel, port 14	Rear P2
VX3910-SA-B*x*400	Front Panel, port 13	Front Panel, port 14	Front Panel, port 15
VX3910-RC-BN200	Unused	Unused	Rear P2
VX3910-RC-BN400	Unused	Unused	Unused

Table 9: Uplink Options

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3.1.3 PCIe to PCI Bridge

The PLX PEX 8112 bridges the PCIE signals from the PPC405EX to the PCI interface of the BCM56224B.

Common features:

- Single Lane PCIe-to-PCI transparent forward bridge
- PCIe 1 lane 2.5 Gbps Gen 1
- PCI 32-bit/66 MHz
- 144-pin BGA

The PEX 8112 is able to connect up to four PCI devices. On the VX3910 only the BCM56224B switch is connected as device 0 on the PCI bus.

BCM56224B	PEX 8112
MPI_IDSEL	PCI_AD16
MPI_GNT#	PCI_GNT0#
MPI_REQ#	PCI_REQ0#
MPI_CLK#	PCI_CLKOUT0#
MPI_INTA#	PCI_INTA#

Table 10: PCIe MPI Signals

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3.2 Unit Computer and Memory

The Unit Computer controls the Ethernet infrastructure and hosts the management application. It is a PowerPC PPC405EX with the following features:

- 600 MHz core frequency
- PCIe management connection to Ethernet Switch
- GbE connections to front management port and Ethernet Switch

The Unit Computer is equipped with the following peripherals:

- 512 MB DDR2 Memory with 400 MHz data rate and ECC
- 64 MB NOR Flash memory for two Firmware images
- 1024 MB NAND Flash for high volume storage (TFTP Server applications) with high frequency read
- Real Time Clock with integrated oscillator, powered by a capacitor with up to two weeks of back up power
- CONFIG EEPROM holding the configuration data

IPMI Support

The PPC405EX I2C #1 connects to NXP PCA9546A 4-channel I2C-bus switch.

- NXP PCA9546A I2C address is set to 0b1110001 (7-bit address)
- Channel SD0 connects to VPX
- Channel SD1 connects to VPX
- Channel SD2 and Channel SD3 are not used

Ethernet Ports

The Unit Computer has two ethernet ports: Management Interface and Switch Uplink.

- Port 1 operates in 10/100/1000BASE-T mode and connects to front RJ45 with integrated magnetics in both SA and RC classes.
- Port 2 operates in 1000BASE-BX mode and connects to local Switch Device.

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Real Time Clock

The Micro Crystal Switzerland RV-8564-C2 connects the PPC405EX I2C #0 interface.

- RTC with integrated oscillator
- 32.768 KHz Clock Output +/- 20ppm (~10.5 min/year)
- 100 KHz I2C interface, address read A2h, address write A3h
- Battery back-up for up to 10 years

Note Not available on VX3910-RC boards.

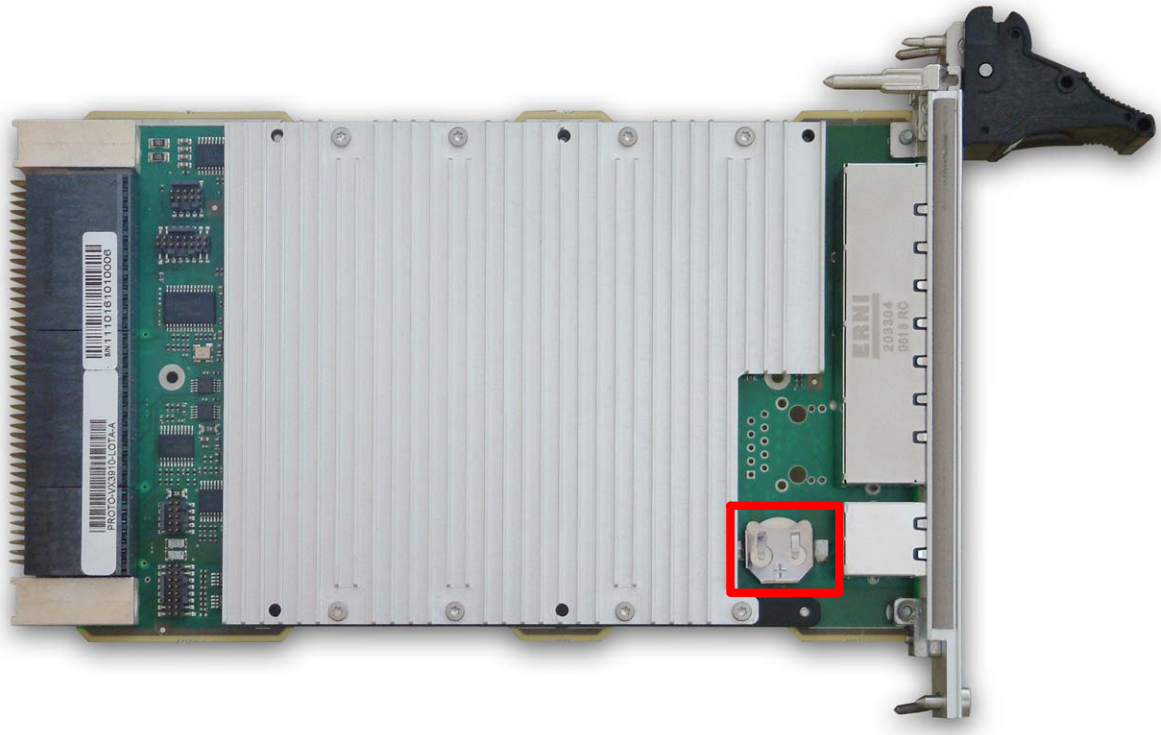


Figure 8: Location of battery on VX3910-RC boards

Temperature Sensors

The National Semiconductor LM73 connects to PPC405EX I2C #0

- Accuracy is better +/- 2°C
- I2C Sensor measures inlet air
- Alert# signal is connected to CPLD

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3.3 Glue Logic

The VX3910 glue logic is an Altera CPLD EPM2210F256 with the following functions:

- Power control
  - Monitor Power Good Signals
- Reset control
  - Reset distribution
  - Reset inputs
- PPC405EX interface
  - 100 MHZ
  - 8-bit data
  - 256 bytes (8-bit address) register space
- LED control
- BCM 56526 LED Bus Controller Interface
  - BCM56224B has the same interface.
- NOR Flash Control
  - 512 Mbit/1024 Mbit/2048 Mbit device support
- Memory Write Protection
  - Requires specific VPX-Backplane pin NVMRO (shall condition writes to ALL types of non volatile memories)
- Miscellaneous
  - System Global Address: SA[4:0] VPX Geographical address shall be used (readable by 405ex), these are 6 pins, GA 0..4 + GA parity
  - Board Variant: BRD_VAR[2:0]
  - Board Revision: BRD_REV[2:0]

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3.4 Write Protection Feature

The backplane signal NVMRO defines the protection:

- If NVMRO is set to High, all non volatile memory is read only, write protected.
- If NVMRO is set to Low, all non volatile memory is not write protected.

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3.5 Board Interfaces

3.5.1 Front Panel Status LEDs and Reset Button

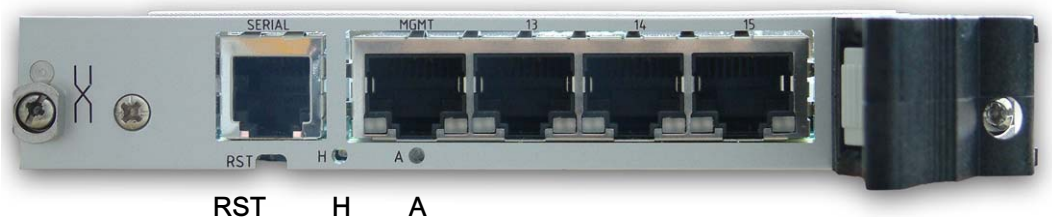


Figure 9: Front Panel of the VX3910-SA

Status LEDs

> H

Green LED, Healthy, ON = Switch operational
Red LED, Fault, ON = Switch fault

> A

Green LED, Reserved

Reset Button

> RST

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3.5.2 Front Panel Ports

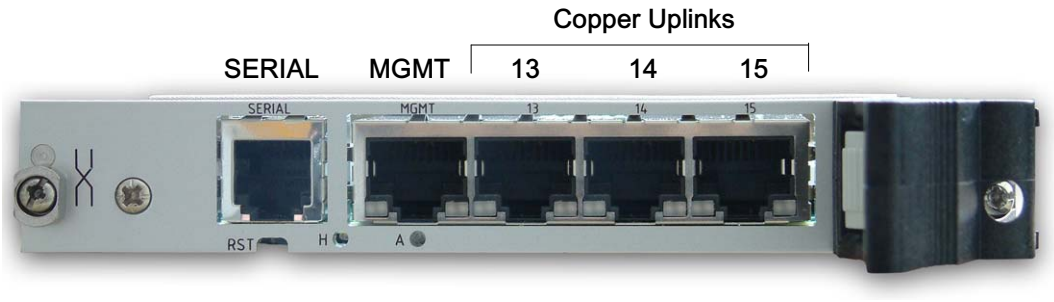


Figure 10: Front Panel Ports of the VX3910-SA

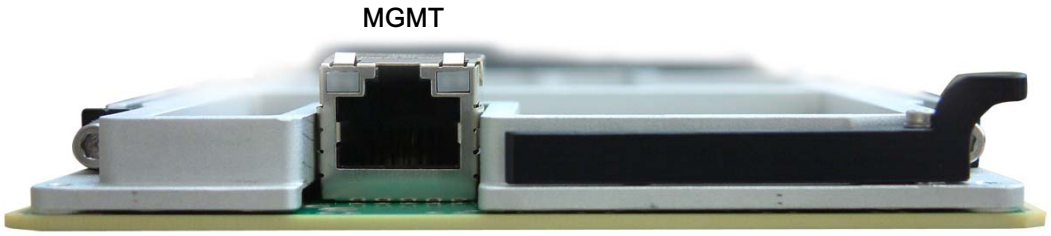


Figure 11: Front Panel Ports of the VX3910-RC

> SERIAL
1x RJ11 for Management (RJ11 connector), see section 3.5.2.1 “Serial Interface” page 32.

> MGMT
1x 10/100/1000BASE-T for management (RJ45 connector), see section 3.5.2.2 “Gigabit Ethernet Management Interface” page 33.

> 13 - 14 - 15
3x 10/100/1000BASE-T for GbE front panel Interfaces (RJ45 connectors), see section 3.5.2.3 “Copper Uplinks” page 34.

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3.5.2.1 Serial Interface

PIN	SIGNAL
1	RTS
2	Shell
3	TXD
4	RXD
5	GND
6	CTS

Table 11: Serial Connector Pin Assignment

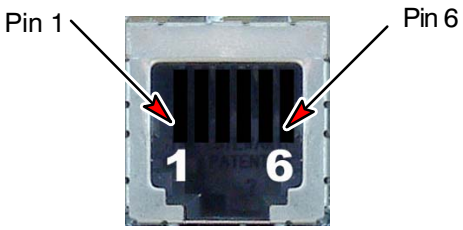


Figure 12: Serial Connector

MNEMONIC	DESCRIPTION
CTS	EIA-232 Clear-To-Send
RTS	EIA-232 Ready-To-Send
RXD	EIA-232Receive Data
TXD	EIA-232 Transmit Data
GND	Ground
Shell	Chassis Ground

Table 12: Serial Connector Signal Description

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3.5.2.2 Gigabit Ethernet Management Interface

The Ethernet transmission can operate effectively using a CAT5 cable with a maximum length of 100 m.

The Gigabit Ethernet MAC of the PPC405EX is used as a management interface. A Gigabit Ethernet PHY transceiver and a RJ45 connector with integrated magnetics and two LED's, located on the front panel, are used to complete the network interface.

The default setting of the PHY is to operate in auto-negociation enabled mode, 10/100/1000, Full or Half duplex. The LEDs indicate Link/Activity (LED: Green) and Speed (LED: Green/Amber).

The standard RJ45 connector has the following pin assignment:

PIN	1000BASE-T	
	I/O	SIGNAL
1	I/O	BI_DA+
2	I/O	BI_DA-
3	I/O	BI_DB+
4	I/O	BI_DC+
5	I/O	BI_DC-
6	I/O	BI_DB-
7	I/O	BI_DD+
8	I/O	BI_DD-

Table 13: Gbe Management Connector Pin Assignment

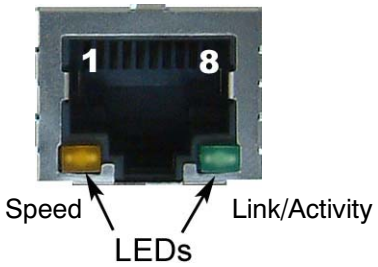


Figure 13: Gbe Management Connector

Gigabit Ethernet LEDs Signification

Speed LED	STATUS
OFF	Port did not perform linkup
ON	Port performed linkup but no activity
BLINKING	Port performed linkup and there is activity

Speed LED	STATUS
OFF	10BASE-T
ON (Amber)	100BASE-TX
ON (Green)	1000BASE-T

Table 14: Gigabit Ethernet LEDs Signification

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3.5.2.3 Copper Uplinks

The Ethernet transmission can operate effectively using a CAT5 cable with a maximum length of 100 m.

The VX3910-SA supports four 10/100/1000BASE-T RJ45 fabric switch uplinks to the front panel. The switch is connected to the RJ45 connectors with integrated magnetics and status LEDs on the front panel via external PHYs.

The RJ45 connectors have the following pin assignment (MID-X hub mode).

PIN	1000BASE-T	
	I/O	SIGNAL
1	I/O	BI_DA+
2	I/O	BI_DA-
3	I/O	BI_DB+
4	I/O	BI_DC+
5	I/O	BI_DC-
6	I/O	BI_DB-
7	I/O	BI_DD+
8	I/O	BI_DD-

Table 15: Cooper Uplinks Connector Pin Assignment

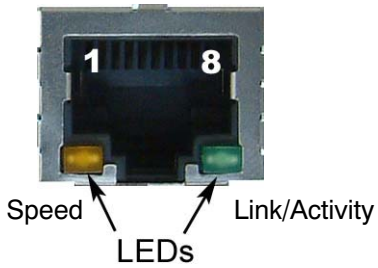


Figure 14: Copper Uplinks Connector

Copper Uplink LEDs Signification

Link Activity Green LED	STATUS
OFF	Port did not perform linkup
ON	Port performed linkup but no activity
BLINKING	Port performed linkup and there is activity

Speed Green/Yellow LED	STATUS
OFF	100BASE-TX
ON	1000BASE-T

Table 16: Copper Uplink LEDs Signification

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3.5.3 Backplane Connectors

The complete 3U VPX connector configuration comprises three connectors named P0 to P2.

- P0: 8-wafer 7-row connector.
- P1 to P2: 16-wafer 7-row differential connectors.

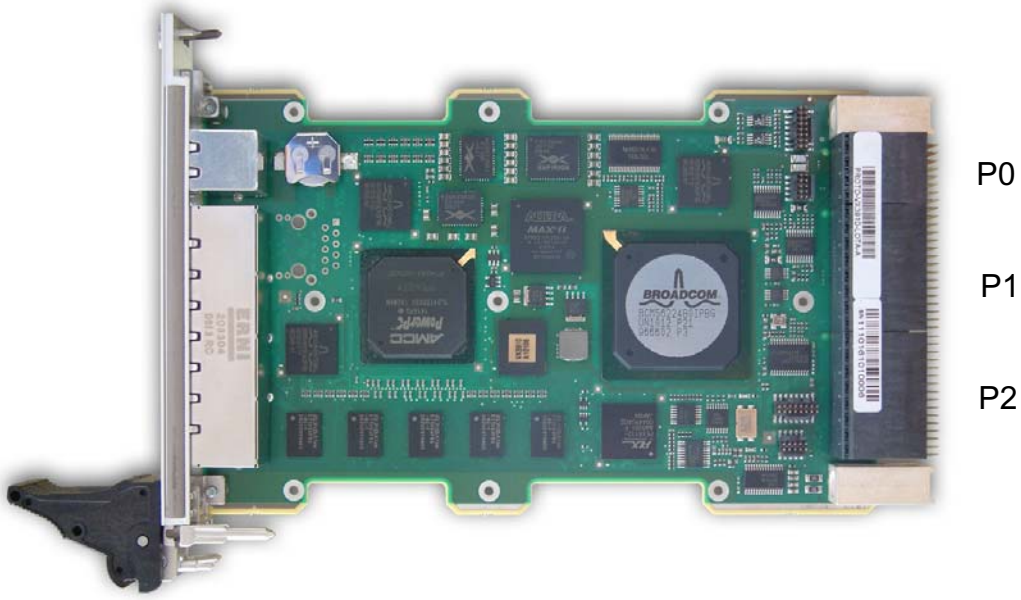


Figure 15: Backplane Connectors

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3.5.3.1 P0 Connector

P0 Wafer Assignment

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	NC (+12V)	NC (+12V)	NC (+12V)	NC	NC (+3V3)	NC (+3V3)	NC (+3V3)
2	NC (+12V)	NC (+12V)	NC (+12V)	NC	NC (+3V3)	NC (+3V3)	NC (+3V3)
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	SMB1 CLK	SMB1 DAT	GND	NC (-12V_AUX)	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	SMB0 CLK	SMB0 DAT
6	GA3*	GA2*	GND	NC (-12V_AUX)	GND	GA1*	GA0*
7	(TCK)	GND	PCIe_CLK- (TDO)	PCIe_CLK+ (TDI)	GND	(TMS)	(TRST*)
8	GND	NC	NC	GND	NC	NC	GND
CASE	GND						

* signal active when low

Table 17: VPX Connector P0 Wafer Assignment

P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+5V	+5 Volts DC power (VS3 VPX supply)
GA*i*	Geographical Address Pin
GAP	Geographical Address Parity
GND	Ground
NC	Not Connected
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated. This allows systems with security sensitivity the ability to run classified or sensitive data without the concern that the data will be kept over power cycles.
PCIe_CLK+/-	100 MHz PCIe Common Clock Input
SMB0	System Management Bus 0
SMB1	System Management Bus 1
SYSRESET*	System Reset. Input and open collector output.

Table 18: VPX Connector P0 Signal Definition

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3.5.3.2 P1 Connector

» P1 Wafer Assignment

Depending on the manufacturing option **Rear Panel Interfaces** (**Option 1** or **Option 2**), the P1 wafer assigment differs.

Table 19 page 37 details the P1 wafer assignment for Rear Panel Interfaces - Option 1:
24x 1000BASE-BX

Table 20 page 38 details the P1 wafer assignment for Rear Panel Interfaces - Option 2:
22x 1000BASE-BX + 1x 1000BASE-T

> **Option 1:** 24x 1000BASE-BX

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.
2	GND	N.C.	N.C.	GND	N.C.	N.C.	GND
3	VBAT	GND	N.C.	N.C.	GND	N.C.	N.C.
4	GND	N.C.	N.C.	GND	N.C.	N.C.	GND
5	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.
6	GND	N.C.	N.C.	GND	N.C.	N.C.	GND
7	Reserved	GND	N.C.	N.C.	GND	N.C.	N.C.
8	GND	N.C.	N.C.	GND	N.C.	N.C.	GND
9	BSC_SCL	GND	ETH-STK3 TX-	ETH-STK3 TX+	GND	ETH-STK3 RX-	ETH-STK3 RX+
10	GND	ETH-STK2 TX-	ETH-STK2 TX+	GND	ETH-STK2 RX-	ETH-STK2 RX+	GND
11	BSC_SDA	GND	ETH-STK1 TX-	ETH-STK1 TX+	GND	ETH-STK1 RX-	ETH-STK1 RX+
12	GND	ETH-STK0 TX-	ETH-STK0 TX+	GND	ETH-STK0 RX-	ETH-STK0 RX+	GND
13	MAG_PWR_ P1V8	GND	ETH-SW21 TX-	ETH-SW21 TX+	GND	ETH-SW21 RX-	ETH-SW21 RX+
14	GND	ETH-SW20 TX-	ETH-SW20 TX+	GND	ETH-SW20 RX-	ETH-SW20 RX+	GND
15	Maskable Reset (1)	GND	ETH-SW19 TX-	ETH-SW19 TX+	GND	ETH-SW19 RX-	ETH-SW19 RX+
16	GND	ETH-SW18 TX-	ETH-SW18 TX+	GND	ETH-SW18 RX-	ETH-SW18 RX+	GND
CASE	GND						

(1) Signal active when low

Table 19: VPX Connector P1 Wafer Assignment (Option 1)

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> Option 2: 22x 1000BASE-BX + 1x 1000BASE-T

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.
2	GND	N.C.	N.C.	GND	N.C.	N.C.	GND
3	VBAT	GND	N.C.	N.C.	GND	N.C.	N.C.
4	GND	N.C.	N.C.	GND	N.C.	N.C.	GND
5	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.
6	GND	N.C.	N.C.	GND	N.C.	N.C.	GND
7	Reserved	GND	N.C.	N.C.	GND	N.C.	N.C.
8	GND	N.C.	N.C.	GND	N.C.	N.C.	GND
9	BSC_SCL	GND	ETH-STK3 TX-	ETH-STK3 TX+	GND	ETH-STK3 RX-	ETH-STK3 RX+
10	GND	ETH-STK2 TX-	ETH-STK2 TX+	GND	ETH-STK2 RX-	ETH-STK2 RX+	GND
11	BSC_SDA	GND	ETH-STK1 TX-	ETH-STK1 TX+	GND	ETH-STK1 RX-	ETH-STK1 RX+
12	GND	ETH-STK0 TX-	ETH-STK0 TX+	GND	ETH-STK0 RX-	ETH-STK0 RX+	GND
13	MAG_PWR_ P1V8	GND	ETH-SW21 TX-	ETH-SW21 TX+	GND	ETH-SW21 RX-	ETH-SW21 RX+
14	GND	ETH-SW20 TX-	ETH-SW20 TX+	GND	ETH-SW20 RX-	ETH-SW20 RX+	GND
15	Maskable Reset (1)	GND	ETH-SW19 TX-	ETH-SW19 TX+	GND	ETH-SW19 RX-	ETH-SW19 RX+
16	GND	ETH-SW18 TX-	ETH-SW18 TX+	GND	ETH-SW18 RX-	ETH-SW18 RX+	GND
CASE	GND						

(1) Signal active when low

Table 20: VPX Connector P1 Wafer Assignment (Option 2)

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P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
ETH-STK*xx* TX+/-	Ethernet 1000BASE-BX Link *xx* Transmit +/- 4 additional GbE stacking ports
ETH-STK*xx* RX+/-	Ethernet 1000BASE-BX Link *xx* Receive +/- 4 additional GbE stacking ports
ETH-SW*xx* TX+/-	Ethernet 1000BASE-BX Link *xx* Transmit +/-
ETH-SW*xx* RX+/-	Ethernet 1000BASE-BX Link *xx* Receive +/-
ETH-SW*xx* DA+/-	Ethernet 1000BASE-T Link *xx:* First pair of transmit/receive data
ETH-SW*xx* DB+/-	Ethernet 1000BASE-T Link *xx:* Second pair of transmit/receive data
ETH-SW*xx* DC+/-	Ethernet 1000BASE-T Link *xx:* Thrid pair of transmit/receive data
ETH-SW*xx* DD+/-	Ethernet 1000BASE-T Link *xx:* Fourth pair of transmit/receive data
MaskableReset*	Optional reset input for this module. May be left unconnected if not used.
NC	Not Connected
GND	Ground
Reserved	Reserved. Do not connect.

Table 21: VPX Connector P1 Signal Definition

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3.5.3.3 P2 Connector

» P2 Wafer Assignment

Depending on the manufacturing option **Rear Panel Interfaces** (**Option 1** or **Option 2**), the P2 wafer assigment differs.

Table 22 page 40 details the P2 wafer assignment for Rear Panel Interfaces - Option 1:
24x 1000BASE-BX

Table 23 page 41 details the P2 wafer assignment for Rear Panel Interfaces - Option 2:
22x 1000BASE-BX + 1x 1000BASE-T

> **Option 1:** 24x 1000BASE-BX

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM1 RTS	GND	ETH-SW17 TX-	ETH-SW17 TX+	GND	ETH-SW17 RX-	ETH-SW17 RX+
2	GND	ETH-SW16 TX-	ETH-SW16 TX+	GND	ETH-SW16 RX-	ETH-SW16 RX+	GND
3	COM1 TXD	GND	ETH-SW12 TX-	ETH-SW12 TX+	GND	ETH-SW12 RX-	ETH-SW12 RX+
4	GND	ETH-SW11 TX-	ETH-SW11 TX+	GND	ETH-SW11 RX-	ETH-SW11 RX+	GND
5	COM1 CTS	GND	ETH-SW10 TX-	ETH-SW10 TX+	GND	ETH-SW10 RX-	ETH-SW10 RX+
6	GND	ETH-SW9 TX-	ETH-SW9 TX+	GND	ETH-SW9 RX-	ETH-SW9 RX+	GND
7	COM1 RXD	GND	ETH-SW8 TX-	ETH-SW8 TX+	GND	ETH-SW8 RX-	ETH-SW8 RX+
8	GND	ETH-SW7 TX-	ETH-SW7 TX+	GND	ETH-SW7 RX-	ETH-SW7 RX+	GND
9	MDC	GND	ETH-SW6 TX-	ETH-SW6 TX+	GND	ETH-SW6 RX-	ETH-SW6 RX+
10	GND	ETH-SW5 TX-	ETH-SW5 TX+	GND	ETH-SW5 RX-	ETH-SW5 RX+	GND
11	MDIO	GND	ETH-SW4 TX-	ETH-SW4 TX+	GND	ETH-SW4 RX-	ETH-SW4 RX+
12	GND	ETH-SW3 TX-	ETH-SW3 TX+	GND	ETH-SW3 RX-	ETH-SW3 RX+	GND
13	LED_DATA	GND	ETH-SW2 TX-	ETH-SW2 TX+	GND	ETH-SW2 RX-	ETH-SW2 RX+
14	GND	ETH-SW1 TX-	ETH-SW1 TX+	GND	ETH-SW1 RX-	ETH-SW1 RX+	GND
15	LED_CLK	GND	ETH-SW22 TX-	ETH-SW22 TX+	GND	ETH-SW22 RX-	ETH-SW22 RX+
16	GND	ETH-SW23 TX-	ETH-SW23 TX+	GND	ETH-SW23 RX-	ETH-SW23 RX+	GND
CASE	GND						

Table 22: VPX Connector P2 Wafer Assignment (Option 1)

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> Option 2: 22x 1000BASE-BX + 1x 1000BASE-T

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM1 RTS	GND	ETH-SW17 TX-	ETH-SW17 TX+	GND	ETH-SW17 RX-	ETH-SW17 RX+
2	GND	ETH-SW16 TX-	ETH-SW16 TX+	GND	ETH-SW16 RX-	ETH-SW16 RX+	GND
3	COM1 TXD	GND	ETH-SW12 TX-	ETH-SW12 TX+	GND	ETH-SW12 RX-	ETH-SW12 RX+
4	GND	ETH-SW11 TX-	ETH-SW11 TX+	GND	ETH-SW11 RX-	ETH-SW11 RX+	GND
5	COM1 CTS	GND	ETH-SW10 TX-	ETH-SW10 TX+	GND	ETH-SW10 RX-	ETH-SW10 RX+
6	GND	ETH-SW9 TX-	ETH-SW9 TX+	GND	ETH-SW9 RX-	ETH-SW9 RX+	GND
7	COM1 RXD	GND	ETH-SW8 TX-	ETH-SW8 TX+	GND	ETH-SW8 RX-	ETH-SW8 RX+
8	GND	ETH-SW7 TX-	ETH-SW7 TX+	GND	ETH-SW7 RX-	ETH-SW7 RX+	GND
9	MDC	GND	ETH-SW6 TX-	ETH-SW6 TX+	GND	ETH-SW6 RX-	ETH-SW6 RX+
10	GND	ETH-SW5 TX-	ETH-SW5 TX+	GND	ETH-SW5 RX-	ETH-SW5 RX+	GND
11	MDIO	GND	ETH-SW4 TX-	ETH-SW4 TX+	GND	ETH-SW4 RX-	ETH-SW4 RX+
12	GND	ETH-SW3 TX-	ETH-SW3 TX+	GND	ETH-SW3 RX-	ETH-SW3 RX+	GND
13	LED_DATA	GND	ETH-SW2 TX-	ETH-SW2 TX+	GND	ETH-SW2 RX-	ETH-SW2 RX+
14	GND	ETH-SW1 TX-	ETH-SW1 TX+	GND	ETH-SW1 RX-	ETH-SW1 RX+	GND
15	LED_CLK	GND	ETH-SW15 DB-	ETH-SW15 DB+	GND	ETH-SW15 DA-	ETH-SW15 DA+
16	GND	ETH-SW15 DD-	ETH-SW15 DD+	GND	ETH-SW15 DC-	ETH-SW15 DC+	GND
CASE	GND						

Table 23: VPX Connector P2 Wafer Assignment (Option 2)

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P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
COM1 TXD/RXD	EIA-232 Transmit/Receive Data
COM1 CTS	EIA-232 Clear To Send
COM1 RTS	EIA-232 Ready To Send
ETH-SW*xx* TX+/-	Ethernet 1000BASE-BX Link *xx* Transmit +/-
ETH-SW*xx* RX+/-	Ethernet 1000BASE-BX Link *xx* Receive +/-
ETH-SW*xx* DA+/-	Ethernet 1000BASE-T Link *xx:* First pair of transmit/receive data
ETH-SW*xx* DB+/-	Ethernet 1000BASE-T Link *xx:* Second pair of transmit/receive data
ETH-SW*xx* DC+/-	Ethernet 1000BASE-T Link *xx:* Thrid pair of transmit/receive data
ETH-SW*xx* DD+/-	Ethernet 1000BASE-T Link *xx:* Fourth pair of transmit/receive data
LED_CLK	
LED_DATA	
MDC	
MDIO	

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Chapter 4 - Software Description

4.1 Supported RFCs

The Software supports the following standards and RFCs (Request for Comments).

4.1.1 Management

> RFC 826 - ARP
> RFC 854 - Telnet
> RFC 855 - Telnet Option
> RFC 1155 - SMI v1
> RFC 1157 - SNMP
> RFC 1212 - Concise MIB Definitions
> RFC 1901 - Community based SNMP v2
> RFC 2246 - The TLS Protocol, Version 1.0
> RFC 2271 - SNMP Framework MIB
> RFC 2295 - Transparent Content Negotiation
> RFC 2296 - Remote Variant Selection; RSVA/1.0 State Management "cookies"
> RFC 2346 - AES Ciphersuites for Transport Layer Security
> RFC 2576 - Coexistence between SNMP v1,v2 & v3
> RFC 2578 - SMI v2
> RFC 2579 - Textual Conventions for SMI v2
> RFC 2580 - Conformance statements for SMI v2
> RFC 3410 - Introduction and Applicability Statements for Internet Standard Management Framework
> RFC 3411 - An Architecture for Describing SNMP Management Frameworks
> RFC 3412 - Message Processing and Dispatching (December 2002)
> RFC 3413 - SNMP Applications (December 2002)
> • RFC 3414 - User-based Security Model (December 2002)
> RFC 3415 - View-based Access Control Model (December 2002)
> RFC 3416 - Version 2 of SNMP Protocol Operations (December 2002)
> RFC 3417 - Transport Mappings (December 2002)
> RFC 3418 - MIB for the Simple Network Management Protocol.
> RFC 3635 - Definition of Managed Objects for Ethernet-like Interface Types
> SSL 3.0 and TLS 1.0
  - RFC 2246—The TLS protocol, version 1.0
  - RFC 2346—AES cipher suites for Transport layer security
  - RFC 2818—HTTP over TLS
> SSH 1.5 and 2.0
  - RFC 4253—SSH transport layer protocol

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- RFC 4252—SSH authentication protocol
- RFC 4254—SSH connection protocol
- RFC 4251—SSH protocol architecture
- RFC 4716—SECSH public key file format
- RFC 4419—Diffie-Hellman group exchange for the SSH transport layer protocol

> Configurable Management VLAN ID
> Industry Standard CLI
> HTML 4.0 specification, December 1997
> Java® Plug-in and Java Script™ 1.3

4.1.2 Switching

> IEEE 802.1AB—Link level discovery protocol
> IEEE 802.1D—Spanning tree
> IEEE 802.1p—Ethernet priority with user provisioning and mapping
> IEEE 802.1Q—Virtual LANs w/ port-based VLANs
> IEEE 802.1S—Multiple spanning tree compatibility
> IEEE 802.1v—Protocol-based VLANs
> IEEE 802.1W—Rapid spanning tree
> iEEE 802.1AB—LLDP
> IEEE 802.1X—Port-based authentication
> IEEE 802.3—10BASE-T
> IEEE 802.3u—100BASE-T
> IEEE 802.3ab—1000BASE-T
> IEEE 802.3ac—VLAN tagging
> IEEE 802.3ad—Link aggregation
> IEEE 802.3ae—10 GbE
> IEEE 802.3x—Flow control
> ANSI/TIA-1057—LLDP-MED
> GARP—Generic Attribute Registration Protocol: clause 12, 802.1D-2004
> GMRP—Dynamic L2 multicast registration: clause 10, 802.1D-2004
> GVRP—Dynamic VLAN registration: clause 11.2, 802.1Q-2003
> RFC 4541—IGMP snooping and MLD snooping
> Broadcast storm recovery
> Double VLAN/vMAN tagging
> DHCP SnoopingDynamic ARP inspection
> Independent VLAN Learning (IVL) support
> IPv6 classification APIs
> Jumbo Ethernet frames
> Port mirroring
> Static MAC filtering

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- IGMP and MLD snooping querier
- Port MAC locking
- MAC-based VLANs
- IP source guard
- IP subnet-based VLANs
- Voice VLANs
- Protected ports
- Event and error logging facility
- Runtime and configuration download capability
- PING utility
- RFC 768—UDP
- RFC 783—TFTP
- RFC 791—IP
- RFC 792—ICMP
- RFC 793—TCP
- RFC 826 — ARP
- RFC 951—BootP
- RFC 1321—Message digest algorithm
- RFC 1534—Interop. between BootP and DHCP
- RFC 2030—Simple Network Time Protocol (SNTP) V4 for IPv4, IPv6, and OSI
- RFC 2131—DHCP Client/Server
- RFC 2132—DHCP options and BootP vendor ext.
- RFC 2865—RADIUS client
- RFC 2866—RADIUS accounting
- RFC 2868—RADIUS attributes for tunnel protocol support
- RFC 2869—RADIUS extensions
- RFC 28869bis — RADIUS support for Extensible Authentication Protocol (EAP)
- RFC 3164—The BSD syslog protocol
- RFC 3580—802.1X RADIUS usage guidelines

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4.1.3 QoS

DiffServ

- RFC 2474—Definition of the differentiated services field (DS Field) in the IPv4 and IPv6 headers
- RFC 2475—An architecture for differentiated services
- RFC 2597—Assured forwarding PHB group
- RFC 3246—An expedited forwarding PHB (Per-Hop Behavior)
- RFC 3260—New terminology and clarifications for DiffServ

Access Control Lists (ACL)

- Permit/deny actions for inbound or outbound IP traffic classification based on:
  - Type of service (ToS) or differentiated services (DS) DSCP field
  - Source IP address
  - Destination IP address
  - TCP/UDP source port
  - TCP/UDP destination port
  - IPv6 flow label
  - IP protocol number
- Permit/deny actions for inbound or outbound Layer 2 traffic classification based on:
  - Source MAC address
  - Destination MAC address
  - EtherType
  - VLAN identifier value or range (outer and/or inner VLAN tag)
  - 802.1p user priority (outer and/or inner VLAN tag)
- Optional rule attributes:
  - Assign matching traffic flow to a specific queue
  - Redirect or mirror (flow-based mirroring) matching traffic flow to a specific port
  - Generate trap log entries containing rule hit counts

Class of Service (CoS)

- Direct user configuration of the following:
  - IP DSCP to traffic class mapping
  - IP precedence to traffic class mapping
  - Interface trust mode: 802.1p, IP Precedence, IP DSCP, or untrusted
  - Interface traffic shaping rate
  - Minimum and maximum bandwidth per queue
  - Strict priority versus weighted (WRR/WDRR/WFQ) scheduling per queue
  - Tail drop versus Weighted Random Early Detection (WRED) queue depth management

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4.2 Supported MIBs

The Software supports the following MIBs (Management Information Bases)

4.2.1 Enterprise MIB

> Support for all managed objects not contained in standards based MIBs.

4.2.2 Switching Package MIBs

> RFC 1213 - MIB-II
> RFC 1493 - Bridge MIB: Definitions of Managed Objects for Bridges (dot1d)
> RFC 1643 – Definitions of managed objects for the Ethernet-like interface types
> RFC 2233 - The Interfaces Group MIB using SMI v2
> RFC 2618 - RADIUS Authentication Client MIB
> RFC 2620 - RADIUS Accounting MIB
> RFC 2674 - VLAN & Ethernet Priority MIB: The Bridge MIB Extension module for managing Priority and Multicast Filtering, defined by IEEE 802.1D-1998.
> RFC 2674 - Q-BRIDGE-MIB: The VLAN Bridge MIB module for managing Virtual Bridged Local Area Networks
> RFC 2737 – Entity MIB version 2
> RFC 2819 - RMON Groups 1,2,3 & 9
> RFC 2863 – Interfaces Group MIB
> RFC 3291 - Textual Conventions for Internet Network Addresses
> RFC 3635 - Etherlike-MIB: Definitions of Managed Objects for the Ethernet-like Interface Types
> IANA-ifType-MIB
> IEEE 802.1X MIB (IEEE8021-PAE-MIB)
> IEEE 802.3AD MIB (IEEE8021-AD-MIB)

4.2.3 QoS Package MIBs

> RFC 3289 - DIFFSERV-MIB: Management Information Base for the Differentiated Services Architecture
> RFC 3289 - DIFFSERV-DCSP-TC MIB: Management Information Base for the Textual Conventions used in DIFFSERV-MIB

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4.2.4 SNMP (Simple Network Management Protocol) MIBs

- RFC 1907 - SNMPv2-MIB: The MIB module for SNMPv2 entities
- SNMP-COMMUNITY-MIB: This MIB module defines objects to help support coexistence between SNMPv1, SNMPv2 and SNMPv3.
- SNMP-FRAMEWORK-MIB: The SNMP Management Architecture MIB
- SNMP-MPD-MIB: The MIB for Message Processing and Dispatching
- SNMP-NOTIFICATION-MIB: The Notification MIB Module
- SNMP-TARGET-MIB: The Target MIB Module
- SNMP-USER-BASED-SM-MIB: The management information definitions for the SNMP User-based Security Model.
- SNMP-VIEW-BASED-ACM-MIB: The management information definitions for the View-based Access Control Model for SNMP.

4.2.5 Kontron Private MIBs

For the VX3910, Kontron provides several MIBs in addition to the Standard MIBs (see “Supported MIBs” on page 47) that allows to use SNMP for configuration of :

- extended Ethernet features
- SGA/GA
- extended management features

Kontron specific MIBs start with a “kex_”. Here‘s a list of MIBs provided (in this example for release GA 2.0) including its content:

- **kex_config**
  - SNMP engine ID
  - Set Hardware Date and Time
  - Set BSP startup services
  - Handle arbitrary config. files
  - ACL Trap Sleep Time
  - Delete Configuration File
- **kex_mgmt**
  - Protection Port Groups
  - Advertise Speed
  - Update/Startup status
  - VLAN multicast flooding
  - Port multicast flooding
  - LAG unicast enhanced hashing
  - Send IGMP reports
  - CPU load
  - Port learning
  - Fast Reload
  - Memory Usage
  - L2 port bridge

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- kex_oem
  - Customer specific information
    - OEM serial number
    - OEM hardware part number
    - OEM software part number
    - OEM software configuration
- kex_version
  - Support FPGA version of board
  - Support SGA address
  - Support PCB version of board

To use the MIBs, you must import the MIBs into the MIB browser. The MIBs are provided on demand for current releases.

SNMP can also be used for updating System Software and PLD.

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4.3 Bootloader

On the VX3910 VPX Ethernet Switch board, the bootloader U-Boot (universal bootloader) is used. The bootloader initializes the main components of the board like Unit Computer, DDR2 RAM, serial lines etc. for operation and performs a power on self test (POST). After these steps have been finished, kernel and application are started from flash.

4.3.1 Power On Self Test

4.3.1.1 Test Routines

Upon power on or system reset, the bootloader performs the following power on self tests (POST):

Test	Description
Serial	Onboard Unit Computer serial controller loopback test
I2C	Check for presence of onboard I2C devices
PCI Express	Check for PCI Express switch device presence
Serviceport	Onboard PPC405EX ethernet internal loopback test
DDR RAM data line	Data line test. Checks for stucked or shortened data lines
DDR RAM address line	Adress line test. Checks for stucked or shortened address lines
DDR RAM memory cells	Checkerboard standard test algorithm
Bootloader environment	Check for valid bootloader environment (CRC correct or both CRCs are 0xFFFFFFFF == not initialized)
VPD area	Check for valid VPD area (CRC is valid)

Table 24: POST Tests

In the case that a POST fails, a POST error code is written into the postcode register of the onboard CPLD. The boot process is not stopped as there are good chances that the board can finish startup sequence successfully. The postcode register is also accessible by the PM which can report error codes to a separate management instance.

The following table shows the POST code values written into the CPLDs postcode register in case of a POST error.

Device	Test
0X00	All POST were successful
0X01	Serial POST failed
0X02	I2C POST failed
0X04	PCIe POST failed
0X08	Ethernet POST failed
0X10	Environment POST failed
0X20	VPD POST failed
0X40	Memory data/address line POST failed
0X80	Memory device cells POST failed

Table 25: POST Routines and Error Codes

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4.3.2 Bootloader Shell Options

The boot process can be interrupted by entering the bootstopkey phrase “stop”. This will open a bootloader shell session.

Entering “?” provides a list of possible built-in commands, “printenv” provides a list of current environment settings. The bootloader shell can be used to customize boot options and system startup by changing some of its environment variables. A list of available environment variables and its description can be seen in the table below.

Name	Type	Description
bootargs	Var	Default kernel arguments. (mem=504M root=/dev/ram0 quiet)
bootcmd	Script	This variable defines a command string that is automatically executed when the initial countdown is not interrupted. This command is only executed when the variable bootdelay is also defined!
bootcmdflash	Script	contains the standard startup script for loading OS image from flash partition command. This will load the Linux kernel and start it with a CRAMFS (TBC, maybe INITRD) type root f ile system.
bootcmdnet	Script	contains the standard startup script for loading OS image from network
bootcmdprd	Script	contains the standard startup script for use during board production
bootcmdrecover	Script	contains standard startup script for board f irmware recovery in boot firmware
bootdelay	Var	After reset, U-Boot will wait this number of seconds before it executes the contents of the bootcmd variable. During this time a countdown is printed, which can be interrupted by pressing any key. Set this variable to 0 boots without delay. Be careful: depending on the contents of your bootcmd variable, this can prevent you from entering interactive commands again forever! Set this variable to -1 to disable autoboot. default: 3 for boot monitor, 10 for boot write-protected boot firmware.
bootsource	Var	When the standard boot sequence is used, contains the boot source, either flash, net, prd to select the respective boot sequence to activate. It is only used when bootcmd contains the default startup script, which may be overridden by the user. default: flash
bootstopkey	Var	Defines the key phrase that the user needs to type to drop into the bootloader command line interface during startup. not set – use string “stop” as bootstop key phrase (default) <any> - use string <any> as bootstop key phrase
clear_config	Script	Erase config partition to restore factory defaults for Linux BSP set
clear_env	Script	Command script (use with “run clear_env”) that erases the U-Boot environment for the active image
disable_rollback	Var	0 – rollback when CRC check of kernel or rootfs fails (default) 1 – do not rollback
ethact	Var	Default network interface used by network commands (bootp, tftpboot et al) default: ppc_4xx_eth0

Table 26: Bootloader Shell Options

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Name	Type	Description
ethaddr	Auto	contains the default base MAC address of the board. If this is not set, the MAC address from VPD is used.
flash_update	Script	Command script to flash a Linux kernel and rootfs image transferred with tftpboot to the active Linux kernel and rootfs partition
loadaddr	Var	Default load address for network transfers. This is used as a temporary storage for netbooting and firmware updates. default: 0x20000000
memtest	Var	Controls POST memory test execution: 0: only data and address line test is executed 1: fast memory test with checkerboard pattern (tests 4MB of memory divided on dif ferent 128kB memory chunks) 2: full memory test with checkerboard pattern If not set, the fast memory test is performed
postresult	Auto	Stores the POST result 0 – no POST error occurred 1 – a POST error occurred
recover_flash	Script	Command script that is executed when the onboard flash is corrupted
reset_unknown	Var	0 – do not cold reset when unknown reset type is detected 1 – enable cold reset when unknown reset type is detected (default)
ignore_posterr	Var	0 – ignore POST errors (default) 1 – Start CLI on POST errors
uboot_flash_update	Script	Command script to flash a U-Boot binary image transferred with tf tpboot to the active image bootloader
watchdogboot	Var	0 – disable boot monitor watchdog 5...n – timeout in seconds before boot monitor watchdog f ires default: 45 Note: This is the pBMWD watchdog.
watchdogos	Var	0 – disable OS load watchdog 15..dis.n – timeout in seconds before load OS watchdog f ires default: 45 Note: This is the pOSWD watchdog.

Table 27: Bootloader Shell Options (continued)

There are three different types of bootloader environment variables:

- Script: The variable is a set of consecutive (more simple) bootloader commands to perform a specific task. A command script is invoked using the ‘run <script>’ syntax. E.g. the ‘run clear_env’ command would erase the bootloader environment sectors causing the bootloader to use its default environment upon next restart.
- Var: The variable controls a specific behaviour of the bootloader startup sequence. E.g. the ‘bootdelay’ variable controls the time u-boot waits before execution of the bootcmd which normally loads and starts the linux kernel.
- Auto: The variable is automatically set during bootloader startup sequence. E.g. the ‘postresult’ variable stores the result of the POST.

It is possible to modify envionment variables and start the pre-defined scripts form the bootloader shell. It is strongly discouraged to modify the pre-defined script variables. However, definition and execution of user-defined script variables can be done.

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Meddling with the bootloader environment variables can affect significantly the startup sequence of the board and may cause the system to be un-bootable.

Modification of bootloader environment variables is done using the ‘setenv’ and ‘saveenv’ bootloader CLI commands. In the following example, the new environment script variable ‘bootcmdmyscript’ is defined. After that, the ‘bootsource’ is set to <myscript> causing the bootloader to execute <bootcmdmyscript> upon next restart. In addition, bootdelay is increased to 10. Finally, all changes are stored into flash environment sector.

```
=> setenv bootcmdmyscript ´bootp; tftpboot ${loadaddr} myimg.multi; bootm ${loadaddr}´
=> setenv bootsource myscript
=> setenv bootdelay 10
=> saveenv
```

Environment changes are stored in one of the redundant bootloader environment sectors. In case of failure (e.g. power loss), the settings of the redundant sector are still available. However, the fabric default setting is running with environment sectors erased. In this case the following startup message is displayed:

```
ENV: Using default environment
```

Any changes of the environment can be cleared using the ‘clear_env’ script (provided that ‘clear_env’ itself was not changed):

```
=> run clear_env
```


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4.4 Firmware Administration

A running VX3910 system requires – after the bootloader has passed control to the kernel – the kernel itself, the root file system (initrd) and the FASTPATH switching application. These software components make up the VX3910 firmware.

The board supports two permanent storage devices, one is an on-board integrated 64 MB NOR flash that is also used as the power-up boot source and contains bootloader as well as operating system and application data. The other is an onboard NAND flash device with 1GB in size that can be used to hold image data if the board is operated as a TFTP server for CPU blades in a system.

The onboard NOR flash is logically divided into two banks, where the first bank is used during normal system operation. The second bank contains an exact copy of the first bank and can be used to restore normal system operation in case the first bank contains an invalid boot image. The first bank involves flash partitions mtd0-4 whereas the second bank is stored in partition mtd5. Partition mtd6 holds the bootloader boot firmware which is stored in one single write-protected flash sector. The partition scheme of the flash is shown below:

Physical Address	Offset in Flash	Size	Linux Partition	Designation	Description
0xFC000000	0x0000000	512 KB	mtd0	u-boot	Secondary bootloader based on U-Boot
0xFC080000	0x0080000	128 KB	mtd1	vpd	Vital Product Data
		128 KB		inv	Inventar Data
0xFC0C0000	0x00C0000	128 KB	mtd2	env	Redundant bootloader environment (each 128 KB)
0xFC0E0000	0x00E0000	128 KB			
0xFC100000	0x0100000	26112 KB	mtd3	kernel	Linux system (kernel and initrd multi image)
0xFDA80000	0x1A80000	5376 KB	mtd4	config	Read/Write Configuration data
0xFDFC0000	0x1FC0000	32512 KB	mtd5	backup	Contains backup image. Verbatimcopy of mtd0-4
0xFFF80000	0x3F80000	512 KB	mtd6	boot-fw	Write protected boot firmware based on U-Boot

Table 28: Onboard NOR FLASH Partition Scheme (64MB)



The board does support OS images up to 25.5 MB size.



Note that only flash partition mtd4 is using the JFFS2 file system for storage.
All other flash partitions are not formatted and accessible from linux only as raw devices.



The U-Boot boot loader uses one flash sector for storing its environment variables. These can be saved and manipulated from the u-boot CLI and using linux tools. To enable atomic updates of the environment variables, U-Boot uses redundant environment sectors; in case of a failure in completely writing the current sector (e.g. due to loss of power or reset during writes), it will automatically use the redundant environment. Therefore each boot monitor uses two flash sectors (partition mtd2) for storing its environment and redundant copy.

A complete software release for the VX3910 consists of three files:

> vx3910-update-<release>.pkg

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> vx3910-8727-firmware.<release>.tar

In the following, the CLI commands to setup and copy FW images and the CLI commands necessary to perform firmware upgrades are described.

The CLI commands described below are executed in the privileged mode of the CLI hierarchy, which is entered by executing the 'enable' command. Please refer to the "VX3910 CLI Reference Manual" for more information regarding the CLI commands and the way to use them.

4.4.1 Updating Firmware

The firmware - including bootloader - image is updated using the CLI. The following precautions are met to ensure a reliable and failsafe update procedure:

> Two independent system partitions, containing system 1 and system 2 firmware. The active system is always system 1. System 1 is stored in flash mtd partitions mtd0-4, system 2 is a verbatim copy of system 1 and is stored in flash partition mtd5 as a whole. This allows flash recovery from the redundant system in case that update fails due to power loss or similar errors.

The system update package(vx3910-update-<release>.pkg) contains an image of bootloader, kernel, root filesystem and config partition as well as a MD5 checksum file for consistency check.

When performing a firmware update, the software package is loaded from a remote TFTP server. A software update of the VX3910 VPX Switch is done by performing the following steps:

1. Prepare network access of the board
2. Log in to the privileged exec mode of the CLI of the board
3. Copy system image into the system 1 of the flash memory.

```
(Ethernet Fabric) # copy tftp://192.168.50.154/VX3910-update-GA-2.00.pkg image1
(Ethernet Fabric) #
```

4. Check availability of valid boot image in image1 using the command 'show bootvar'

```
(Ethernet Fabric) # show bootvar
Image Descriptions
       image1 : Product ID : 1900
              Product Variant : 0
              U-Boot Release : GA 2.00
              Manufacturer ID : 15000
              Build-Date : 20100520030324
       image2 : Product ID : 1900
              Product Variant : 0
              U-Boot Release : BETA 1.00
              Manufacturer ID : 15000
              Build-Date : 20100119185922

Images currently available on Flash

active (image1) backup (image2)
------------------  --------------------
GA 2.00             BETA 1.00

Restart the board

(Ethernet Fabric) # reload
```


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5. In case of problems with booting the system, last working image2 will automatically be copied to image1. This procedure restores normal system behaviour. Configuration settings made with image1 are lost and shoud be saved by copying image1 to image 2 before.
6. It is recommended to copy image 1 to image 2 to have a fully redundant system

```
(Ethernet Fabric) # copy image1 image2
Copying image1 to image2
(Ethernet Fabric) #
```

The image will be copied including the configuration settings currently stored for image 1

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4.5 Firmware Evolutions

4.5.1 GA2.01 New Features

- Support for L3 routing has been added to the switch management application.
- Temperature monitoring support has been added to the switch management application.

4.5.2 GA2.03 New Features

- Support of the Marvel Alaska® 88E1340 quad transceiver, allowing the conversion of twenty 1000BASE-BX uplink ports to twenty 10/100/1000BASE-T uplink ports on a custom RTM or backplane that implements those transceivers.
- Experimental support for 1000BASE-X without CL37 auto-negotiation.

4.5.2.1 Marvel Alaska® 88E1340 support

The Fastpath application has been enhanced to support a custom RTM or backplane that implements 20 10/100/1000BASE-T ports by Marvel Alaska® 88E1340 Phy devices.

New command line interface commands have been added to activate this special configuration.

Format	set board port-map [default|custom-rtm-1]
	show boardinfo port-map
Mode	Priviledged EXEC
	User EXEC

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Default port-map

The original port map "default" has been implemented like the following table:

CLI	BCM Port	PHY Address	Interface	Speed Settings
0/1	CH1	-	1000BASE-BX	1000 Mbps
0/2	CH2	-	1000BASE-BX	1000 Mbps
0/3	CH3	-	1000BASE-BX	1000 Mbps
0/4	CH4	-	1000BASE-BX	1000 Mbps
0/5	CH5	-	1000BASE-BX	1000 Mbps
0/6	CH6	-	1000BASE-BX	1000 Mbps
0/7	CH7	-	1000BASE-BX	1000 Mbps
0/8	CH8	-	1000BASE-BX	1000 Mbps
0/9	CH9	-	1000BASE-BX	1000 Mbps
0/10	CH10	-	1000BASE-BX	1000 Mbps
0/11	CH11	-	1000BASE-BX	1000 Mbps
0/12	CH12	-	1000BASE-BX	1000 Mbps
0/13	CH13 (2)	14	1000BASE-T	10/100/1000 Mbps
0/14	CH14 (2)	15	1000BASE-T	10/100/1000 Mbps
0/15	CH15 (2)	16	1000BASE-T	10/100/1000 Mbps
0/16	CH16	-	1000BASE-BX	1000 Mbps
0/17	CH17	-	1000BASE-BX	1000 Mbps
0/18	CH18	-	1000BASE-BX	1000 Mbps
0/19	CH19	-	1000BASE-BX	1000 Mbps
0/20	CH20	-	1000BASE-BX	1000 Mbps
0/21	CH21	-	1000BASE-BX	1000 Mbps
0/22	CH22	-	1000BASE-BX	1000 Mbps
0/23	CH23	-	1000BASE-BX	1000 Mbps
0/24	CH0 (1)	-	1000BASE-BX	1000 Mbps
0/25	UCH0 (3)	-	1000BASE-BX	1000 Mbps
0/26	UCH1 (3)	-	1000BASE-BX	1000 Mbps
0/27	UCH2 (3)	-	1000BASE-BX	1000 Mbps
0/28	UCH3 (3)	-	1000BASE-BX	1000 Mbps

(1) CH0 is the internal link between the CPU and the switch

(2) CH13, CH14 and CH15 are front panel uplinks for SA versions

(3) UCH3 ... UCH0 are the four ports for 1 Gigabit Ethernet (GbE) uplink/stacking

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Custom port-map

The new port map "custom-rtm-1" has been implemented like the following table:

CLI	BCM Port	PHY Address	Interface	Speed Settings
0/1	CH1	10	1000BASE-T	10/100/1000 Mbps
0/2	CH2	11	1000BASE-T	10/100/1000 Mbps
0/3	CH3	20	1000BASE-T	10/100/1000 Mbps
0/4	CH4	21	1000BASE-T	10/100/1000 Mbps
0/5	CH5	22	1000BASE-T	10/100/1000 Mbps
0/6	CH6	23	1000BASE-T	10/100/1000 Mbps
0/7	CH7	27	1000BASE-T	10/100/1000 Mbps
0/8	CH8	26	1000BASE-T	10/100/1000 Mbps
0/9	CH9	25	1000BASE-T	10/100/1000 Mbps
0/10	CH10	24	1000BASE-T	10/100/1000 Mbps
0/11	CH11	31	1000BASE-T	10/100/1000 Mbps
0/12	CH12	30	1000BASE-T	10/100/1000 Mbps
0/13	CH13 (2)	14	1000BASE-T	10/100/1000 Mbps
0/14	CH14 (2)	15	1000BASE-T	10/100/1000 Mbps
0/15	CH15 (2)	16	1000BASE-T	10/100/1000 Mbps
0/16	CH16	29	1000BASE-T	10/100/1000 Mbps
0/17	CH17	28	1000BASE-T	10/100/1000 Mbps
0/18	CH18	4	1000BASE-T	10/100/1000 Mbps
0/19	CH19	5	1000BASE-T	10/100/1000 Mbps
0/20	CH20	6	1000BASE-T	10/100/1000 Mbps
0/21	CH21	7	1000BASE-T	10/100/1000 Mbps
0/22	CH22	9	1000BASE-T	10/100/1000 Mbps
0/23	CH23	8	1000BASE-T	10/100/1000 Mbps
0/24	CH0 (1)	-	1000BASE-BX	1000 Mbps
0/25	UCH0 (3)	-	1000BASE-BX	1000 Mbps
0/26	UCH1 (3)	-	1000BASE-BX	1000 Mbps
0/27	UCH2 (3)	-	1000BASE-BX	1000 Mbps
0/28	UCH3 (3)	-	1000BASE-BX	1000 Mbps

(1) CH0 is the internal link between the CPU and the switch

(2) CH13, CH14 and CH15 are front panel uplinks for SA versions

(3) UCH3 ... UCH0 are the four ports for 1 Gigabit Ethernet (GbE) uplink/stacking

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Chapter 5 - VX3910-RC Characteristics

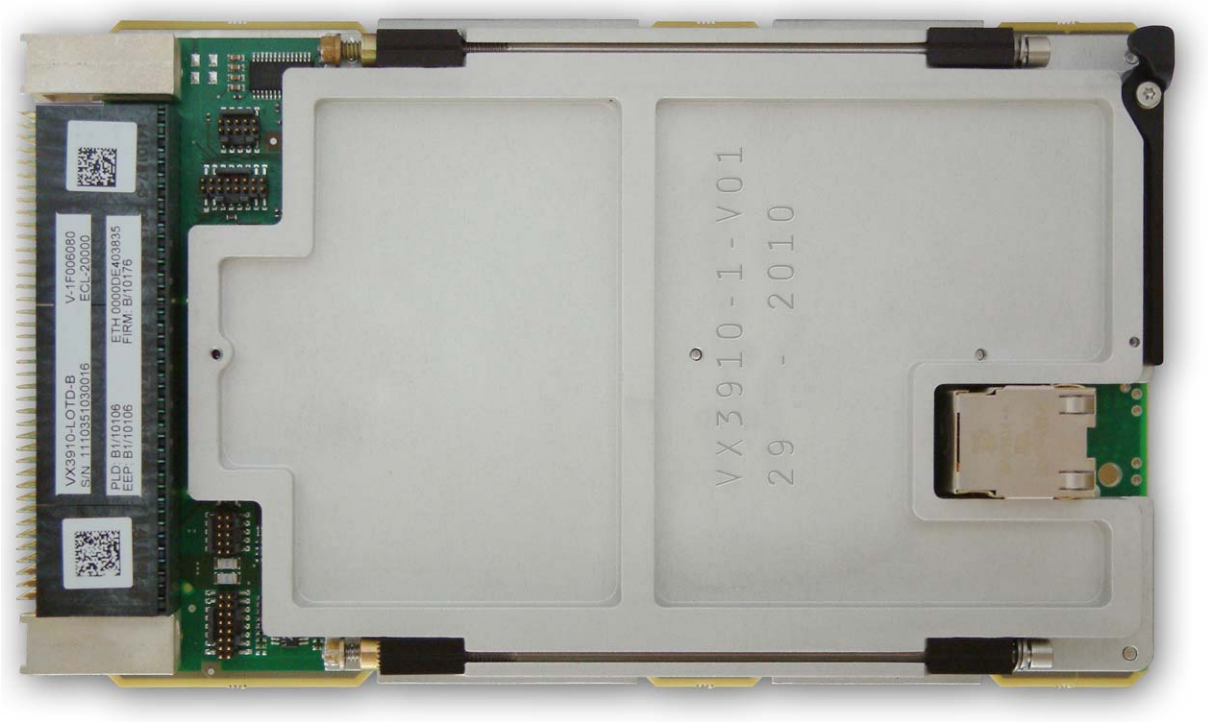


Figure 16: VX3910-RC Overview

Available order codes are listed in table below:

Article	Order Code	Description
		3U VPX Rugged Conduction-Cooled Build SBC
VX3910-RC	VX3910-RC-BN200	3U VPX Ethernet Switch Rear Panel Interfaces: 22x 1000BASE-BX + 1x 1000BASE-T
VX3910-RC	VX3910-RC-BN400	3U VPX/Open VPX Ethernet Switch Compliant wiht slot profile: SLT3-SWH-2F24U Rear Panel Interfaces: 24x 1000BASE-BX

Table 29: VX3910-RC Order Code

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5.1 VX3910-RC Specificities

FUNCTION	DESCRIPTION	SEE ALSO
Battery	No battery available onboard	
Board Identification	Specific ruggedizer identification	**Section 5.2 page 62**
Environmental Specifications	Environmental specifications depend on environmental class	**Section 5.3 page 63** Section 1.3.4 page 5
MTBF	MTBF depends on the environmental class	**Section 5.4 page 63** Section1.3.10 page 7
Peripheral Connectivity	Gigabit Ethernet Management Interface	**Section 5.5 page 64**

Table 30: VX3910-RC Specificities

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5.2 Board Identification

The VX3910-RC boards are identified by labels fitted on top and bottom sides.

These labels are at the same location and have the same meaning as the VX3910-SA boards (refer to section 2.2 “VX3910 Identification” page 11).

In addition, the ruggedizer is identified by:

- AA “Ruggedizer Identification” (printed on the ruggedizer)
- AB “Ruggedizzer dated from” (printed on the ruggedizer)
- AC “Ruggedizer Engineering Change Level” (E.C. Level) label

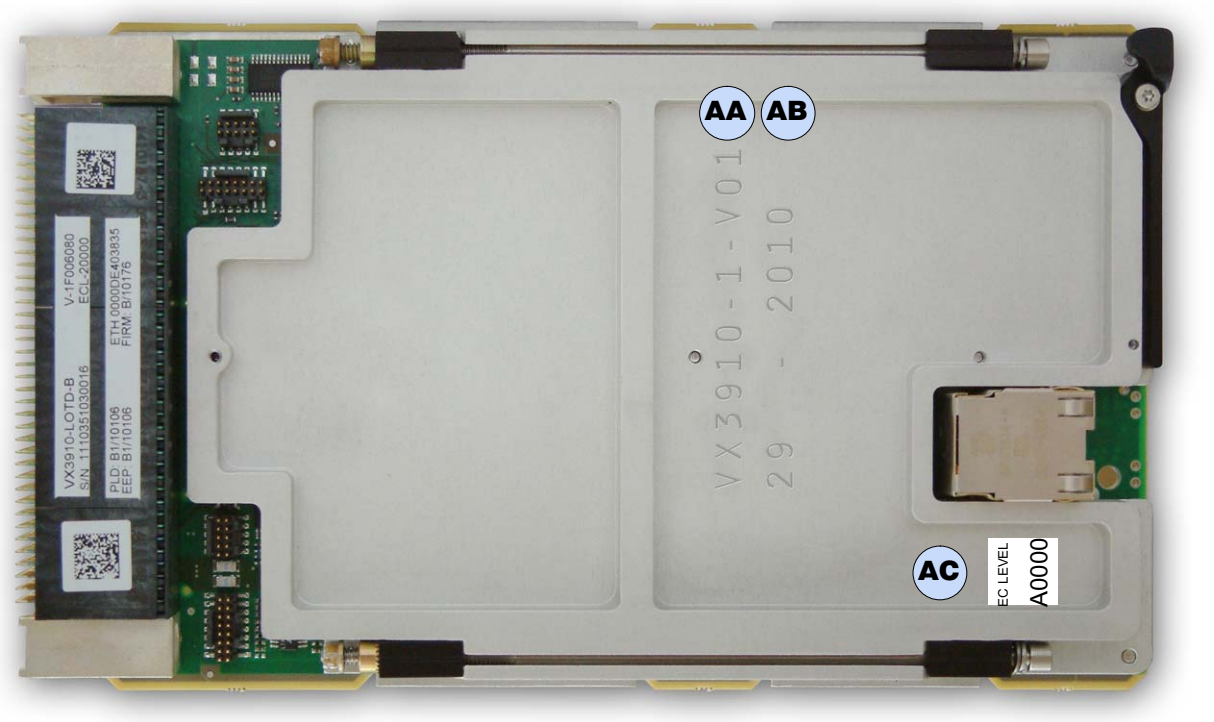


Figure 17: VX3910-RC Identification (Top Side)

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5.3 Environmental Specifications

ENVIRONMENTAL SPECIFICATIONS	
	RC - Rugged Conduction-Cooled
Conformal Coating	Standard
Airflow	N.A.
Temperature	VITA 47-Class CC4
Cooling Method	Conduction
Operating	-40°C to +85°C
Storage	-45°C to +85°C
Vibration Sine (Operating)	5g / 22-2,000 Hz acceleration / frequency range
Random	VITA 47-Class V3
Shock (Operating)	40g / 11ms peak accel. / shock duration half sine
Altitude (Operating)	-1,640 to 50,000 ft
Relative Humidity	95% non-condensing

Table 31: Environmental Specifications

5.4 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

VX3910-RC-BN200

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
VX3910/RC Order Code: VX3910-RC-BN200	408 342	291 954	65 271	80 800	66 247	16 014

Table 32: VX3910-RC-2N200 MTBF Data

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5.5 Peripheral Connectivity

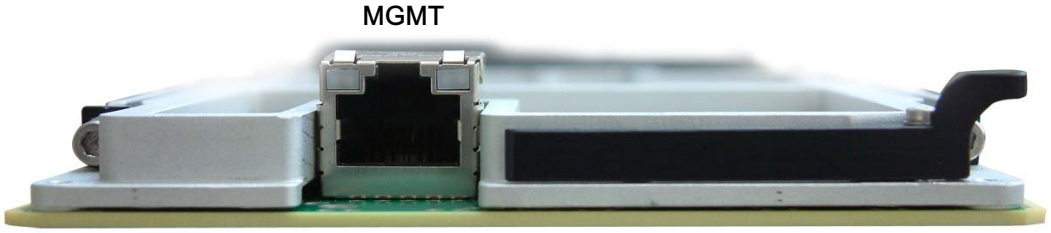


Figure 18: Front Panel Ports of the VX3910-RC

> MGMT
1x 10/100/1000BASE-T for management (RJ45 connector), see section 3.5.2.2 “Gigabit Ethernet Management Interface” page 33.

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MAILING ADDRESS
Kontron Modular Computers S.A.S.
150 rue Marcelin Berthelot - BP 244
ZI TOULON EST
83078 TOULON CEDEX - France

TELEPHONE AND E-MAIL
+33 (0) 4 98 16 34 00
Sales: Order-ATD-Toulon@Kontron.com
Support: GSS-ATD-Toulon@Kontron.com

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