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1, 2, or 4-channel, 60 Ms/s Transient Recorder

Analog recording to 60 Ms/s with 10-bit resolution

V440

Features

- 1, 2, or 4 input channels
- 60 megasample per second, 10-bit operation
- 64 ksample memory per channel
- Internal or external clock
- Pedestal-subtraction DACs
- Programmable pre- and post-trigger sample sizes
- Multi-hit capability
- Internal, external, or programmable threshold-based triggering
- Power-up self-test capability

Typical Applications

- High Energy Physics Experiments
- Electrical discharge studies

General Description

The V440 is a single-width, C-size, register-based, VXIbus module that contains one, two, or four transient digitizer channels. The module digitizes incoming analog signals at a maximum rate of 60 Msamples per second, with 10-bit resolution. A bipolar pedestal-subtraction signal, controlled by a 12-bit DAC, is available on each channel. The digitizing rate is controlled by an on-board, crystal-controlled clock, an externally supplied ECL clock applied to a front-panel connector, the VXIbus 10 MHz ECL clock, or one of the ECL trigger lines present on the VXIbus P2 connector. The selected clock source is common to all channels. This clock may also be routed to the ECL trigger lines to synchronize other V440s.

Digitized samples are stored in on-board memory. Each channel includes a 64 ksample memory which (in the 4-channel option) is accessible from VXIbus as a 512 kbyte block of global memory. The module has two operating modes: single-shot and multi-hit. In single-shot mode, memory is divided into pre-trigger and post-trigger segments. Digitizing is initiated by software command. Once a trigger signal is received, recording continues until each channel's post-trigger memory segment has been filled. The size of each memory segment is controlled by a programmable, 16-bit, post-trigger counter. This allows the number of post-trigger samples for all channels to vary between 0 and 100%.

In multi-hit mode, all samples are treated as post-trigger values and digitizing is held off until the receipt of the trigger signal. In this case, the post-trigger counter is used to hold the number of samples to be recorded for each "hit." Digitizing is halted once the entire 64 ksample memory has been filled.

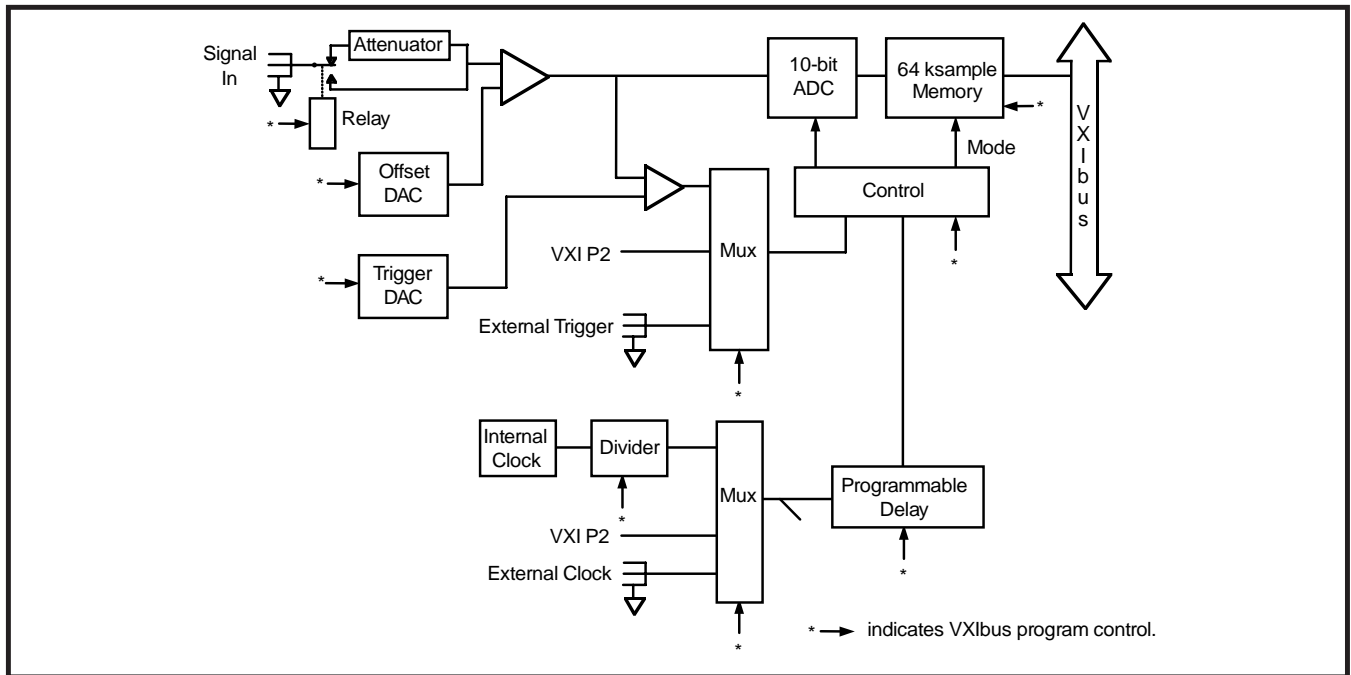
The trigger source is the logical OR of a software command, the receipt of an external TTL signal, any of the eight TTL VXIbus trigger lines, or any input signal exceeding a predetermined threshold level. The V440 must be "armed" before it will respond to any of the non-software triggers. The choice of which VXIbus triggers are used is determined by software command. The threshold level is established by an on-board digital-to-analog converter circuit. This circuit is programmable and has a resolution of eight bits. A programmable 8-bit delay counter in each channel can be used to delay the acceptance of the trigger signal. The delay count is decremented with each tick of the sample clock.

An interrupt is asserted at the completion of the digitizing sequence. The priority level at which it is asserted is programmable from VXIbus. The memory is mapped such that the first pre-trigger sample, or the first sample recorded in multi-hit mode, is read from the first memory address. That is, regardless of where in physical memory the first sample resides, it is read from logical address zero.

The V440 supports both static and dynamic configuration. It may be accessed using A32/A24/A16, D32/D16 data transfers.



V440 Block Diagram



Item	Specifications
Number of Input Channels	1, 2 or 4
Analog Signal Input Type	Single-ended
Analog Input Range, Input Impedance	± 10 V, 10 k Ω ; or ± 1.75 V, 50 Ω programmable
Large Signal Analog Bandwidth (-3 dB) ± 1.75 V input range	70 MHz, minimum; 100 MHz, typical
Resolution	10 bits
DC Accuracy	
Differential nonlinearity	0.75 LSB, typical; 1.25 LSB, maximum
Integral nonlinearity	1.0 LSB, typical; 2.0 LSB, maximum
No missing codes	Guaranteed
Dynamic Performance (40 MHz sample rate)	
Transient response	10 ns
Overvoltage recovery time	minimum typical
Effective number of bits:	
$f_{in} = 2.3$ MHz	8.4 bits 8.8 bits
$f_{in} = 10.3$ MHz	7.8 bits 8.2 bits
$f_{in} = 15.3$ MHz	7.3 bits 7.8 bits
Pedestal Subtraction DACs	
Resolution	12 bits
Maximum value	\pm Full-scale input range
Recording Modes	Single-shot and multi-hit
Memory Size	64 ksamples per channel (256 ksamples total)
Post-trigger Sample Size	Variable from 0 to 65,535
Connector Type	
-NAy1 Option	Coaxial, BNC type
-WAy1 Option	Coaxial, SMB type

V440 (continued)

Clock	
Internal source	On-board, crystal-controlled
Frequency choices	3.75, 7.5, 15, 30, and 60 MHz
External source	ECL signal to 60 MHz
Duty cycle	45 to 55%
Backplane sources	10 MHz ECL clock or ECL trigger line on P2 connector
External Trigger	
Source	Negative-going TTL signal
Minimum pulse width	20 ns
Threshold DAC	
Resolution	8 bits
Maximum value	±2.0 V
Power Requirements (4 channel options)	
+5 V	8.5 A
-5.2 V	1.5 A
+24 V	40 mA
-24 V	40 mA
-2 V	300 mA
Environmental and Mechanical	
Temperature range	
Operational	0°C to 50°C
Storage	-25°C to +75°C
Relative humidity	0 to 85%, non-condensing to 40°C
Cooling requirements	10 CFM
Dimensions	340 mm x 233.35 mm x 30.48 mm (C-size VXIbus)
Front-panel potential	Chassis ground

Ordering Information

Model V440-NA11 1-channel, 60 MHz Transient Digitizer, BNC Connectors
Model V440-NA21 2-channel, 60 MHz Transient Digitizer, BNC Connectors
Model V440-NA41 4-channel, 60 MHz Transient Digitizer, BNC Connectors
Model V440-WA11 1-channel, 60 MHz Transient Digitizer, SMB Connectors
Model V440-WA21 2-channel, 60 MHz Transient Digitizer, SMB Connectors
Model V440-WA41 4-channel, 60 MHz Transient Digitizer, SMB Connectors

Related Products

5919-Z1A Connector—SMB Female



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