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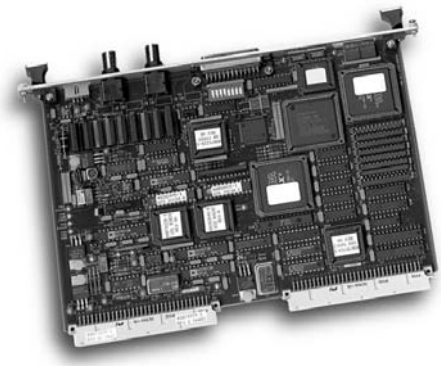
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Bit Synchronizer

BSU532/BSV533



- **Reconstructs a degraded serial PCM signal and creates a clock at bit rates up to 20 Mbps**
- **Converts any IRIG (or Miller-squared) code to any of the input codes (use with IRIG formats: NRZ-L/M/S, BiΦ-L/M/S, DBiΦ-M/S, DM-M/S, RZ, RNRZ-L, or non-IRIG formats: M2-M/S)**
- **Processes or reprocesses data through Randomizer/ Derandomizer (Randomizer ensures 50% transition density with use of external tape recorder; Derandomizer reproduces original stream)**
- **Utilizes a unique digital design to enhance reliability, eliminating recalibration**

The Bit Synchronizer is a 6U VME module, available in two models (BSU532 and BSV533), which creates a clock synchronized to an incoming PCM data steam and makes bit decisions on that stream at data rates up to 20 Mbps. It converts the input data code to NRZ-L and one other operator-selected IRIG format. The module conditions the signal through analog and digital filtering techniques that implement automatic gain, offset, frequency (tracking), and phase control.

Both Bit Sync modules use a unique digital approach to making bit decisions, increasing performance over traditional analog bit syncs and eliminating recalibration. The input can be selected from one of four single-ended inputs or from one RS-422 input. Input impedance of 10 kΩ or 75 Ω can be selected. Each input can be individually terminated so that non-selected inputs are not left unterminated.

The principal difference between the two models is the BSV533's Viterbi decoder, which decodes convolutionally encoded signals to provide an improved level of bit error rate performance.

The BSV533's Viterbi Forward Error Correction (FEC) decoder and convolutional encoder decodes rate 1/2 (or 1/3) constraint length K=7 encoded data with 8 combinations of connection vector swapping and alternate symbol inversion; and provides BER improvement of 5.2 dB @ 10^{-5} (5.5 dB @ 10^{-5}).

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BSU532/BSV533 Specifications

Inputs

IRIG Code Formats	NRZ-L/M/S, BiΦ-L/M/S, DBiΦ-M/S, DM-M/S, RZ, RNRZ-L, and M2-M/S
Bit Rate	NRZ codes: 10 bps to 20 Mbps; other codes: 10 bps to 10 Mbps
PCM Data Single-Ended	BNC (2), DB-25 (2)
RS-422	DB-25
AC Offset	Up to 100% of signal amplitude at frequencies up to 0.1% of bit rate
DC Offset	± 20V @ HIGH impedance ± 8V @ LOW impedance
Usable Input Range	0.25 to 20V peak-to-peak
Impedance	Single-ended: 10 kΩ, < 50 pf, nominal, or 75 Ω; RS-422: 120 Ω side to side

Outputs

External Connectors (TTL or RS-422 on DB-25):

NRZ-L	Data in NRZ-L form
Clock	NRZ-L data clock, 0°, 90°, 180°, 270°
Tape	Analog tape output in any of above IRIG code formats as selected by operator
Convolutional Encoder	Rate 1/2 or 1/3, K=7 data

Functions

Bit Decision and Synchronization	Output to PCM decommutator or out rear panel for system diagnostics
IRIG Code Conversion	Output to analog tape or other external equipment through rear panel connector
Detector Type	Integrate/Dump or Filter/Sample
Tuning Resolution	0.1%
Track Range	0.1% to 15.0% adjustable in 0.1% increments
Capture Range	± (1/2 track range + 1/4 loop bandwidth setting)
Loop Bandwidth	Selectable: 0.1, 0.3, 1, 2, 3%
Bit Error Rate	Within 1.0 dB of theoretical, up to 5 Mbps; within 1.5 dB from 5 to 10 Mbps; within 2.0 dB from 10 to 20 Mbps
Viterbi BER Improvement	5.2 dB @ 10^{-5} BER, K=7 rate 1/2 5.2 dB @ 10^{-5} BER, K=7 rate 1/3
Acquisition Time	Within 10 data transitions, NRZ-L, SNR ³ 15 dB
Minimum Transition Density	3.12% with input 8 dB SNR
Sync Threshold	Minimum SNR for sync acquisition is 0 dB for transition density ≥ 50%
Randomizer	Forward sequence = 2^{15}-1
Derandomizer	Forward or reverse sequence = 2^n-1, where n = 11, 15, 17, 20

Flywheeling with Continuous 1's or 0's:

NRZ Codes	Sync is maintained through strings as long as 512 bits once every 2,047 bits
Other Codes	Indefinite after sync is achieved
Conditions	SNR ≥ 9 dB; LBW = 0.1%, track range = 0.5%; no jitter, AM, or baseline perturbations (the difference between the programmed bit rate and input frequency is ≤ 0.1%)

Flywheeling with Data Dropouts:

NRZ Codes	Sync is maintained through dropouts as long as 512 bits once every 2,047 bits
Other Codes	Sync is maintained through dropouts as long as 128 bits once every 2,047 bits
Conditions	SNR ≥ 12 dB; LBW = 0.1%, track range = 0.5%; no jitter, AM, or baseline perturbations (the difference between the programmed bit rate and input frequency is ≤ 0.1%)
Soft Bit Mode	Normal or invert

General Requirements

System Chassis	1 6U or 9U slot
MUXbus II Arbiter Positions	None required
Rear Panel	1 slot
Connector Type	2 BNC, DB-25
Maximum per System	Virtually unlimited
Maximum per Chassis	16
Power	5V @ 2 A, typical
Environment	See Base System Chassisdata sheet
Module Size	233mm (6U) x 160mm
Diagnostic Display	6 status LEDs: BDOK, DACK, VITLOCK, BSLK, SIG, LOWZ

Program Setup

Keyboard and Mouse	Fill-in-the-blank OSF/Motif™ displays with list-pick selections
ASCII Text File	User-created description

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Printed in USA / ML294 Rev. D
Cleared for Public Domain Release by Directorate for Freedom of Information and Security Review (DFOISR), dated 6/24/04, reference number 04-S-1758.
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