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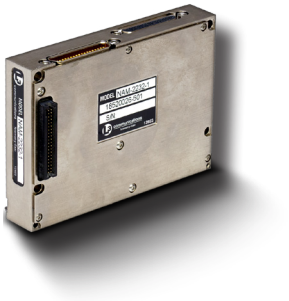
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NAM-2232
NETDAS 32-CHANNEL, DIFFERENTIAL ANALOG SIGNAL CONDITIONER MODULE



OVERVIEW

L3 Telemetry & RF Products (L3 T&RF) NAM-2232 is a signal conditioning module that monitors up to 32 differential analog inputs, generating converted digital output in 32 unique words. The module design utilizes specialized Digital Signal Processing (DSP) filtering concepts that provide performance similar to traditional analog-based implementations, while requiring significantly fewer electronic components. The end result is greater channel density, at a lower cost per channel, with greater functionality.



Each channel provides an input multiplexer used to select its signal source between the external sensor and system ground to support Zero Calibration (Z-CAL). The multiplexer's output is fed to a programmable gain stage supporting a total gain between 0.25 and 16. The amplified signal is then passed through an anti-aliasing filter, followed by a 16-bit Analog-to-Digital Converter (ADC) operating at a rate of 781.250 ksps and feeding the DSP filter. To minimize distortion induced by frame sampling, the ADC rate is up-sampled from 781.250 kHz to 50 MHz.

The NAM-2232 features a single constant voltage excitation source that provides ± 6 V at a maximum of 160 mA. Each channel provides a number of calibration and balance features to facilitate programming and checkout — Z-CAL, Numerical Calibration (N-CAL), transducer offset, amplifier offset and manual offset.

The NAM-2232 allows the user to enable simultaneous sample and hold, which provides phase correlation between all similarly configured analog channels within the entire Data Acquisition Unit (DAU), or within a complete synchronized NetDAS™ system.

All features of the NAM-2232 are supported by L-3's Vista TEC™ software, which includes an operational checkout feature that provides automated testing of all channels to compare data received and against user-specified targets.

FEATURES

- 32 channels of differential analog signal conditioning
- Each channel supports inputs up to 40 V_{p-p}
- Includes one constant voltage excitation source that provides ± 6 V at a maximum of 160 mA
- Each channel has independent and user- selectable gain and offset settings
- Provides Z-CAL, N-CAL, tranducer offset, amplifier offset and manual offset functions
- Supports simultaneous sample and hold function on a per-channel basis
- Fully programmable by L-3's Vista TEC software

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SPECIFICATIONS

INPUT

	Gain of Entire Channel	Input Pins Maximum
Differential Input Voltage (Definition: In_P – In_N)	0.25 1 16	40 V_{p-p} 10 V_{p-p} 0.625 V_{p-p}
Maximum Offset Voltage	± 50 % times input differential voltage	
Maximum Single-Ended Input Applied to In_P or In_N	± 40 V	
Differential Input Impedance	> 1 MΩ	
Single-Ended Input Impedance	> 1 MΩ for Vin < 15 V	
Over-Voltage Protection	± 50 V with latch-up protection	

GAIN

Range	0.25 to 16
Accuracy	± 0.5 % of Full Scale (FS)
Stability	± 0.75 % of selected value, including effects of excitation drift
Linearity	± 0.1 % Best Straight Line (BSL)

OFFSET

Channel Offset Stability	± 0.5 % FS
Reference to Output (RTO) Offset Capability	± 50 % of FS range (offset performed in FPGA before filtering)

DIGITAL FILTER

Programmable 3 dB Cutoff Frequency (FC)	FC = 10 Hz to 5 kHz
Full Passband (FPB) Defined	FPB = 0.72 x FC
Inter-Channel Correlation	± 2 degrees from DC to FPB (for channels configured with the same FC)
Stopband	> 4 x FC (corresponding to Nyquist when sampling at 8 x FC) @ 60 dB minimum
Amplitude Response	Flat within ± 0.5 % from DC to FPB Attenuation at FC: -3 ± ½ dB
Filter Type	8-pole, low-pass Butterworth Infinite Impulse Response (IIR) filter
Output Rate	50 Msps
ADC Sample Rate	50 MHz / 64 = 781.250 ksps

CONSTANT VOLTAGE EXCITATION

Excitation	One positive regulator, one negative regulator	
Programmability	Non-programmable, permanently enabled	
Voltage Output	± 6 V	
Accuracy	± 0.5 %	
Full Load	± 15 V excitation supply ± 7 V excitation supply	20 mA 160 mA

OUTPUT

16-bit Conversion	The channel output is converted to a 16-bit word either, straight binary or 2s complement Note: Full-scale signal is converted into 15 bits with remaining bit used to accommodate offset
Output Word Size	Supports common word size or extended read mode

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