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MMI-4310/MMI-4311

QUAD VMEbus AUDIO BOARD

INSTALLATION AND HARDWARE REFERENCE MANUAL

Release 2.0

April 1999

Part Number 880-3190-001

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Visicom Quad Audio Board User's Manual

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1. Installation

1.1 Scope

This section provides information necessary for the installation of the MMI-4310 and MMI-4311 digital audio boards into a host VMEBus system.

1.2 Installation and Switch Settings

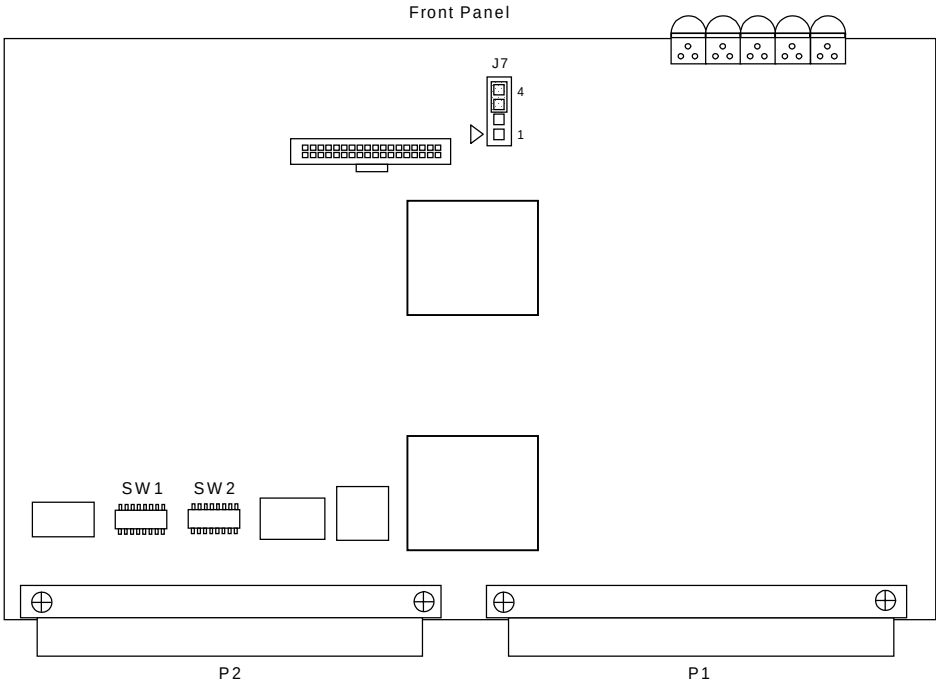


Figure 1.1 Mainboard Switch Locations

1.3 MMI-430 Mainboard DIP Switch Settings

The MMI-430 contains 2 DIP Switches SW1 and SW2 which configure the board's base address and interrupt level in a VME system. Figure 1.2 shows the factory default settings as they appear on the board. As indicated, flipping a switch to the left (on) sets that bit to a zero. Flipping it to the right (off) sets it to a one.

Jumper J7 is only used for compatibility with the (discontinued) MMI-4211-M1 model. For normal operation the jumper should be set to connect pins 3 and 4.

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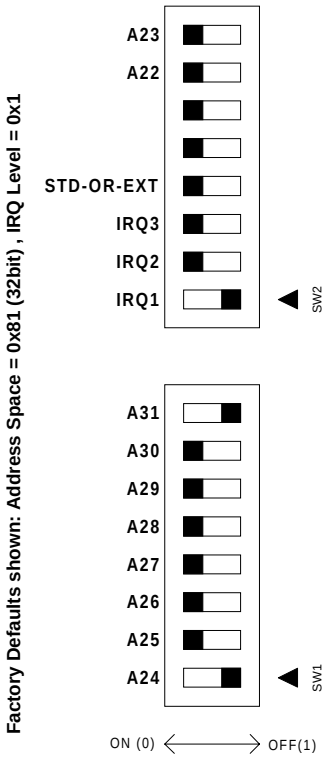


Figure 1.2 MMI-430 Mainboard Address and Interrupt Level Switches

1.4 Setting the VME Address

Refer to The STD-OR-EXT and A31-A22 switches are used to set the base address for the MMI-430. The STD-OR-EXT switch is used to configure the board for Standard (24 bit) or Extended (32 bit) VME addresses with STD being a 1 (off) and EXT being a 0 (on). In Standard addressing, the 43xx board may be set to addresses 0x400000, 0x800000, or 0xC00000. In Extended addressing the board may be addressed on 4MB boundaries within the range of 0x400000 to 0xFFC00000 (1024 possible addresses). The factory default setting is 0x81000000, extended addressing. If STD mode is selected, switches A31-A24 are ignored. 0x0 is a valid address setting but is not recommended, however, because that 4MB range is typically used for other VMEbus system purposes.

1.5 Setting the VME Interrupt Level

The VME IRQ bits are used to set the VME interrupt level to be used by the MMI-430, with VME-IRQ1 representing the least significant bit of the interrupt level. The desired interrupt level can be selected as shown in Table 1.

Table 1. Interrupt Level Chart

IRQ Level	IRQ3	IRQ2	IRQ1
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

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1.6 Switch Settings for DB-310 (MMI-4310)

The DB-310 daughterboard provides DIP-switch-programmable setting of input and output coupling and impedance.

Odd-numbered switches (SW1, SW3, SW5, SW7) select output impedance when transformer coupling is selected. When DIRECT is selected, the output connection is tied directly to the output of the corresponding channel (A, B, C, or D). In DIRECT mode, the output impedance is nominally 16Ω. The even-numbered switches (SW2, SW4, SW6, SW8) select ether input impedance, when transformer coupling is selected, or DIRECT coupling. Figure 1.3 shows the settings vs. modes for input and output. Moving the switch towards the front panel selects the ON position.

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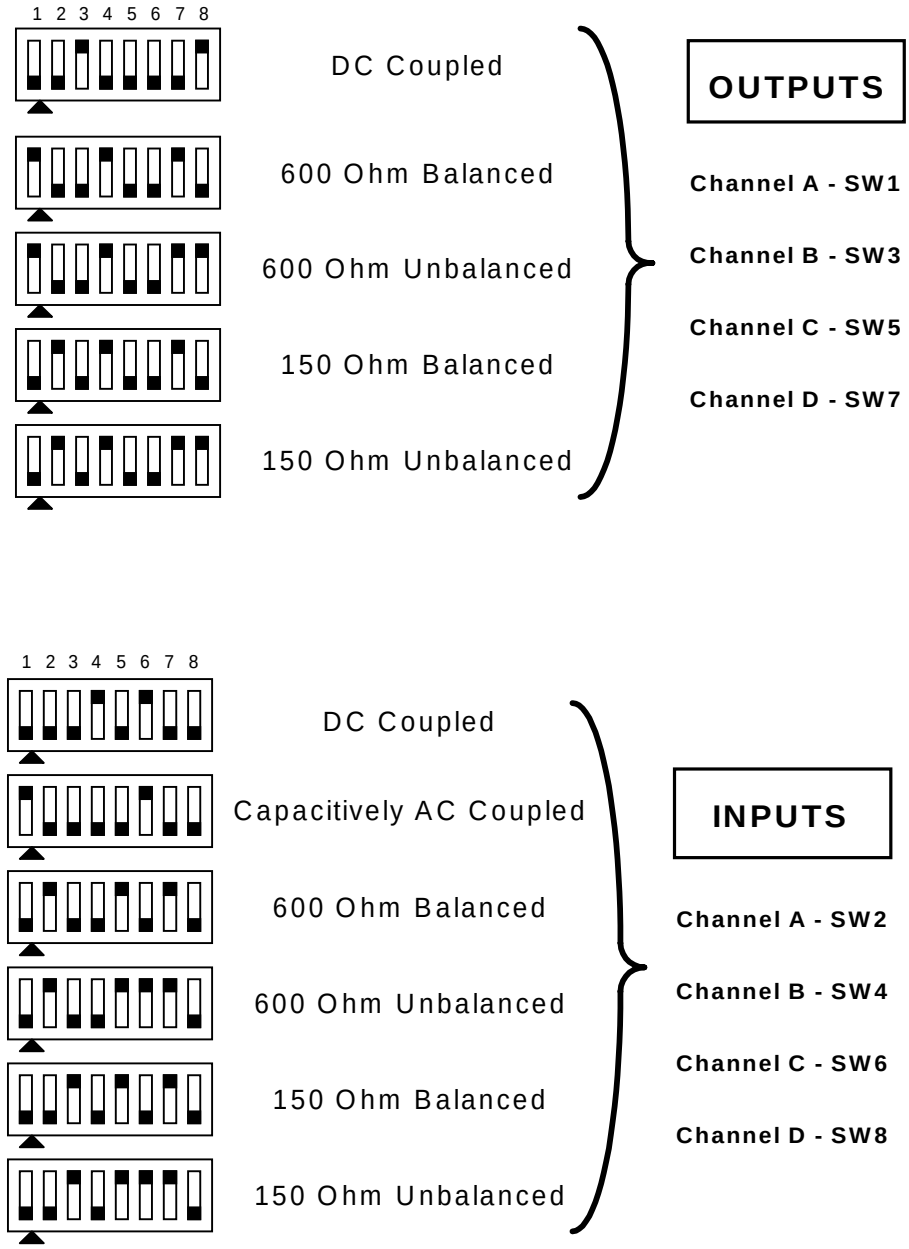


Figure 1.3 DB-310 (MMI-4310) Daughterboard Switch Settings

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1.7 MMI-4310 Audio I/O Connector

All audio input and output connections for the MMI-4310 are made via an AMP p/n 87813-7 20-pin rectangular connector. The mating connector is an AMP p/n 226305-1, which is a flat coaxial ribbon cable connector. The pinout for this connector is shown in Figure 1.4. This connector is shown in the vertical position as viewed from the front panel.

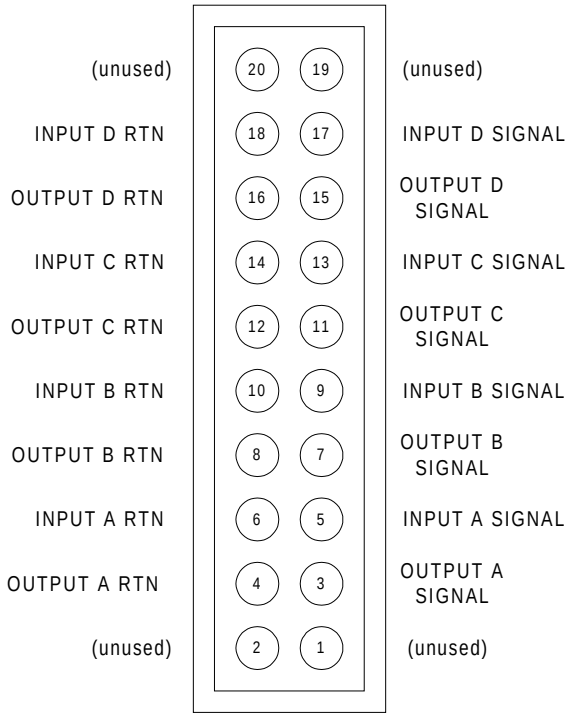


Figure 1.4 MMI-4310 Audio I/O Connector Pinout

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2. General Information

2.1 Features

- Four Digital Audio Channels
- Digital Recording and Playback (each channel)
- High-Fidelity (CD/DAT) Quality Audio
- Analog Interface

  16-bit Delta-Sigma A/D converters
  16-bit Delta-Sigma D/A Converters
  Line Level Inputs and Outputs
  Separate Mic. & Line Inputs (MMI-4311)

- Software Controlled Sample Frequencies (independent per channel)
- Continuously Programmable Sample rates from 6KHz to 48KHz
- Software Controlled Input and Output Levels
- Supported by VisiCom's DiSPATCH Firmware Package
- Programmable Output Mixing

2.2 MMI-4310 Description

The MMI-4310 is the combination of a MMI-430 mainboard and a DB-310 daughterboard. The DB-310 daughterboard provides 4 transformer-coupled inputs and 4 transformer-coupled line-level outputs. Onboard DIP switches allow setting input and output impedance. The inputs can be individually set for DC-coupling, AC (capacitor)-coupling, 600Ω transformer-coupling or 150Ω transformer-coupling. The **DiSPATCH** software maps the input and output gain settings to emulate a MMI-4210 board.

2.3 MMI-4311 Description

The MMI-4311 is the combination of a MMI-430 mainboard and a DB-311 daughterboard. The DB-311 daughter board provides 4 stereo 3.5mm phone jacks for microphone inputs, 4 stereo 3.5mm phone jacks for line-level inputs, and 4 stereo 3.5mm phone jacks for line-level outputs.

Left and Right channel microphone preamp and left and right output amplifier gains for a given I/O module are set simultaneously via the **mmi-test amplify** or **DiSPATCH mmi_amplify** command. CODEC input signal sensitivity and output signal level (volume) for each I/O channel can be independently adjusted via software control.

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2.4 MMI-4310/4311 Common Features

The MMI-430 mainboard comprises four identical I/O modules - one per DSP - each of which provides the circuits to convert between analog and digital signals and to amplify the analog signals. It also provides switching circuits for routing the output signals from each of the four D/A converters to analog mixers, and a power conditioning circuit for the analog circuitry.

Each I/O module channel of the MMI-430 connects to the SSI and SCI ports of its the corresponding Motorola DSP56002 DSP and provides, a 16-bit stereo Delta-Sigma A/D and a 16-bit stereo D/A converters to provide high quality, digital recording and playback. For the MMI-4310, only the left channel of each I/O module is used.

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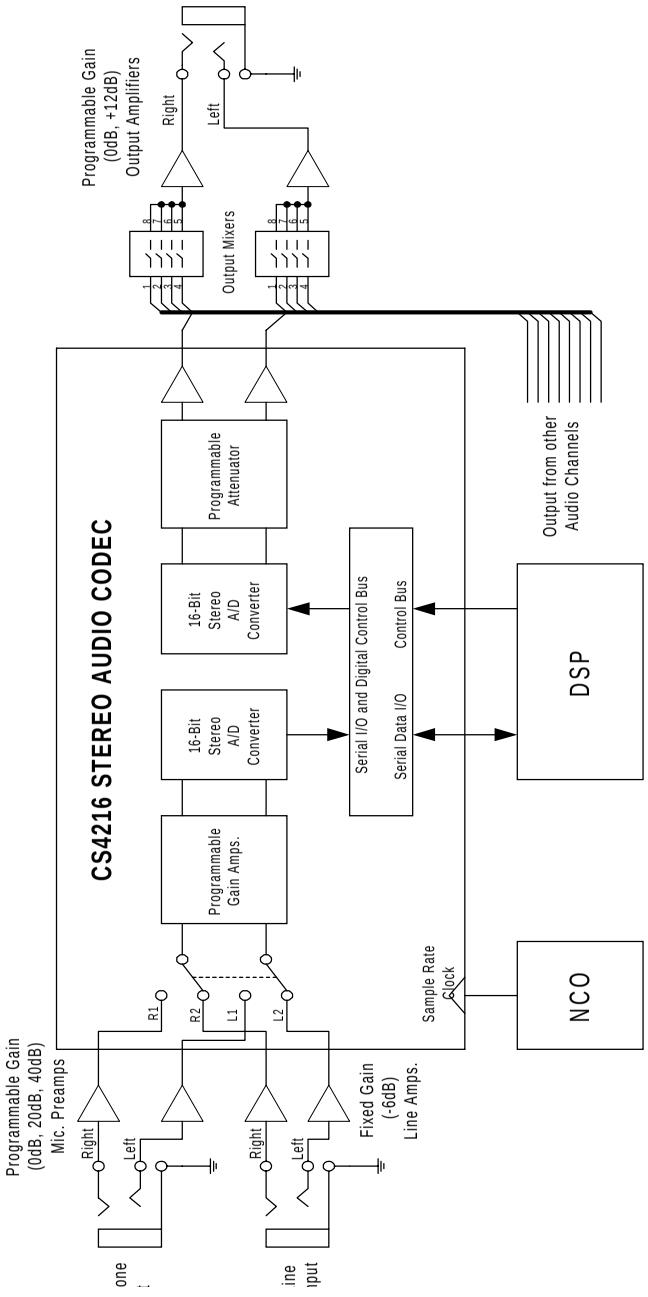


Figure 2.1 Audio Block Diagram (MMI-4311 shown)

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Figure 2.1 shows the main elements of an audio I/O channel. The interface for the MMI-4311 is shown for the sake of simplicity. The DB-311 daughterboard (MMI-4311) provides 3.5mm stereo phone jacks for input and output as shown in Figure 5. The DB-310 daughterboard (MMI-4310) provides the capability of inserting isolation transformers between inputs and/or outputs, but only the left channel microphone input and left channel output is used on each CODEC. The DB-310 physical connection to the outside world is via a single rectangular 20-pin connector instead of individual phone jacks. Otherwise, the interface is the same as shown in Figure 2.1.

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3. INPUT SECTION

For the MMI-4311 there are separate stereo inputs for microphone and line for each channel. The line inputs go through fixed gain buffers. These buffers attenuate line-level inputs (-6dB) to allow up to 2Vrms input signals without clipping. The microphone preamplifers provide software-controlled (using the **mmi-test amplify** or DiSPATCH **mmi_amplify** command) gain settings of 0dB, 20dB or 40dB. The MMI-4310 only uses the left channel microphone inputs of each input section.

The CS4216 Stereo CODEC input section provides switching between mic. and line inputs and 0 to 22.5dB of gain. The DiSPATCH INPUT_GAIN command sets the CODEC input gain for one of 16 possible gain settings. The A/D converter is a stereo 16-bit Delta-Sigma type.

3.1 MMI-4311 INPUT GAIN SETTINGS

Table 2 shows the correlation to the value programmed in the **input_gain** command and the gain that the CODEC's Programmable Gain Amps are set to for the MMI-4311. Add this value to the microphone preamp or line input buffer's gain to determine the overall input gain. Thus, for Mic. preamp gain = 20dB, CODEC input gain = 10.5dB, the net gain would then be 30.5dB.

The DSP for that channel controls the selection between line and mic. (MMI-4311), mic. input gain setting, the CS4216's input gain setting, and programs the NCO to set the sampling frequency. Digitized audio data is sent serially from the CODEC to the DSP via the SSI port.

Table 2. MME-4311 CODEC Gain vs. INPUT_GAIN setting

INPUT_GAIN Setting	CODEC Input Gain
0 - 15	0dB
16 - 31	1.5dB
32 - 47	3.0dB
48 - 63	4.5dB
64 - 79	6.0dB
80 - 95	7.5dB
96 - 111	9.0dB
112 - 127	10.5dB
128 - 143	12.0dB
144 - 159	13.5dB
160 – 175	15.0dB

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176 - 191	16.5dB
192 - 207	18.0dB
208 - 223	19.5dB
224 - 239	21.0dB
240 - 255	22.5dB

3.2 MMI-4310 INPUT GAIN SETTINGS

The MMI-4310 has been designed to emulate the operation of the MMI-4210 board. In the MMI-4210, the input gain setting was performed with a digital potentiometer in the feedback loop of an opamp. A logarithmic adjustment circuit provided a gain adjustment for a range of 1 to 1000. The HSP software provided for the MMI-4310 automatically determines the input gain setting that would normally be set using the **amplify** command, (the 0dB, 20dB and 40dB settings) and maps the appropriate gain setting to be sent to the CODEC, resulting in the gains shown in Table 3. Table 3 shows the correlation to the value programmed in the **input_gain** command and the net gain from input connection to the input of the A/D converter.

The HSP software for the MMI-4310 sets the CODECs for mic. input. The DSP for any given channel controls the CS4216's input gain setting, and programs the NCO to set the sampling frequency. Digitized audio data is sent serially from the CODEC to the DSP via the SSI port.

Table 3. MMI-4310 Net Gain vs. INPUT_GAIN setting

INPUT_GAIN Setting	Net Input Gain
0 – 6	0dB
7 – 12	1.5dB
13 – 18	3.0dB
19 – 24	4.5dB
25 – 30	6.0dB
31 – 36	7.5dB
37 – 42	9.0dB
43 – 48	10.5dB
49 – 54	12.0dB
55 – 60	13.5dB
61 – 67	15.0dB
68 – 73	16.5dB

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74 – 79	18.0dB
80 – 81	19.5dB
82 – 87	20.0dB
88 – 93	21.5dB
94 - 99	23.0dB
100 - 105	24.5dB
106 - 111	26.0dB
112 - 117	27.5dB
118 - 124	29.0dB
125 - 130	30.5dB
131 - 136	32.0dB
137 - 142	33.5dB
143 - 148	35.0dB
149 - 154	36.5dB
155 - 160	38.0dB
161 - 162	39.5dB
163 - 168	40.0dB
169 – 174	41.5dB
175 - 180	43.0dB
181 - 187	44.5dB
188 - 193	46.0dB
194 - 199	47.5dB
200 - 205	49.0dB
206 - 211	50.5dB
212 - 217	52.0dB
218 - 223	53.5dB
224 - 229	55.0dB
230 - 235	56.5dB
236 - 241	58.0dB
242 - 248	59.5dB
249 - 254	61.0dB
255	62.5dB

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4. OUTPUT SECTION

Digitized audio data is sent serially from the DSP to the CS4216 CODEC via the SSI Port. The digititized audio stream is converted back to left and right analog audio by the stereo 16-bit Delta-Sigma Digital-to-Analog converters. The CODEC's software controlled attenuator provides 0 to -46.5dB of attenuation in 1.5dB increments.

4.1 MMI-4311 OUTPUT GAIN SETTINGS

Table 4 shows the correlation between the value specified in the **output_gain** command and the resulting output attenuation for the MMI-4311. Minimum **output_gain** setting corresponds to maximum CODEC output attenuation (46.5dB). Maximum **output_gain** setting (255) corresponds to minimum CODEC output attenuation (0dB). As, with the input gains, this value is added to the output amplifier gain to determine the net output gain. The output amplifier gain can be selected to be either 0dB or 12dB via the **mmi-test amplify** or DiSPATCH **mmi_amplify** command. For example, for an output attenuation of –39.0dB and an output amplifier setting of 12dB, the net gain would be –27.0dB from the DAC output to the MMI-4311 output jack.

Table 4. MMI-4311 CODEC Output Gain vs. OUTPUT_GAIN setting

OUTPUT_GAIN Setting	CODEC Output Gain
0 - 7	-46.5dB
8 - 15	-45.0dB
16 - 23	-43.5dB
24 - 31	-42.0dB
32 - 39	-40.5dB
40 - 47	-39.0dB
48 - 55	-37.5dB
56 - 63	-36.0dB
64 - 71	-34.5dB
72 - 79	-33.0dB
80 - 87	-31.5dB
88 - 95	-30.0dB
96 - 103	-28.5dB
104 - 111	-27.0dB
112 - 119	-25.5dB
120 -127	-24.0dB
128 - 135	-22.5dB

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136 - 143	-21.0dB
144 - 151	-19.5dB
152 - 159	-18.0dB
160 - 167	-16.5dB
168 - 175	-15.0dB
176 - 183	-13.5dB
184 - 191	-12.0dB
192 - 199	-10.5dB
200 - 207	-9.0dB
208 - 215	-7.5dB
216 - 223	-6.0dB
224 - 231	-4.5dB
232 - 239	-3.0dB
240 - 247	-1.5dB
248 - 255	0.0dB

The left and right outputs of each CODEC are routed to the corresponding mixer inputs for all four output stereo output channels. The mmi-test **route** or DiSPATCH **route_output** command selects which CODEC outputs are routed to which output amplifiers. Thus any channel's stereo output can be routed to any combination of the four stereo outputs (Output A, Output B, Output C, Output D). The stereo output amplifiers provide software selectable gain of either 0dB or 12dB and can drive 600Ω loads. The **mmi-test amplify** or DiSPATCH **mmi_amplify** command is used to select this gain setting for the output amplifiers. The output amplifer gain stage is after the routing mixers. This allows the same output signal to be routed to different output channels with two possible separate gains, if so desired.

4.2 MMI-4310 OUTPUT GAIN SETTINGS

For the MMI-4310, only the left channel of each output is used and any channel's output may be routed to any combination of monophonic outputs A,B,C and/or D.

The HSP driver software for the MMI-4310 automatically sets the output amplifier gain to +12dB. The MMI-4210 used a digital potentiometer in the feedback loop of an inverting opamp circuit. The gain adjustment for the MMI-4210 was therefore linear. Since the MMI-430's CODECs have a logarithmic attenuation adjustment, the HSP must re-map the value specifed in the **output_gain** command to emulate this linear gain setting. Table 5 shows the correlation between the value specified in the **output_gain** command and the net output gain from the DAC output to the output connector for the MMI-4310.

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Table 5. MMI-4310 Net Output Gain vs. OUTPUT_GAIN setting

OUTPUT_GAIN Setting	Net Output Gain
0 - 1	-34.5dB
2	-27.0dB
3	-24.0dB
4	-22.5dB
5	-21.0dB
6	-19.5dB
7	-18.0dB
8 - 9	-16.5dB
10 - 11	-15.0dB
12 - 13	-13.5dB
14 - 16	-12.0dB
17 - 20	-10.5dB
21 - 23	-9.0dB
24 - 28	-7.5dB
29 - 34	-6.0dB
35 - 40	-4.5dB
41 - 48	-3.0dB
49 - 58	-1.5dB
59 - 69	0.0dB
70 - 82	1.5dB
83 - 98	3.0dB
99 - 117	4.5dB
118 - 140	6.0dB
141 - 167	7.5dB
168 - 198	9.0dB
199 - 237	10.5dB
238 - 255	12.0dB
216 - 223	-6.0dB
224 - 231	-4.5dB
232 - 239	-3.0dB

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240 - 247	-1.5dB
248 - 255	0.0dB

The CS4216's output attenuator, the mixer channel selection and the output amplifier's gain is controlled by its respective DSP.

4.3 Digital Block Diagram

Figure 4.2 shows only the blocks for Channel A and the common board resources (VMEbus I/O and DRAM).

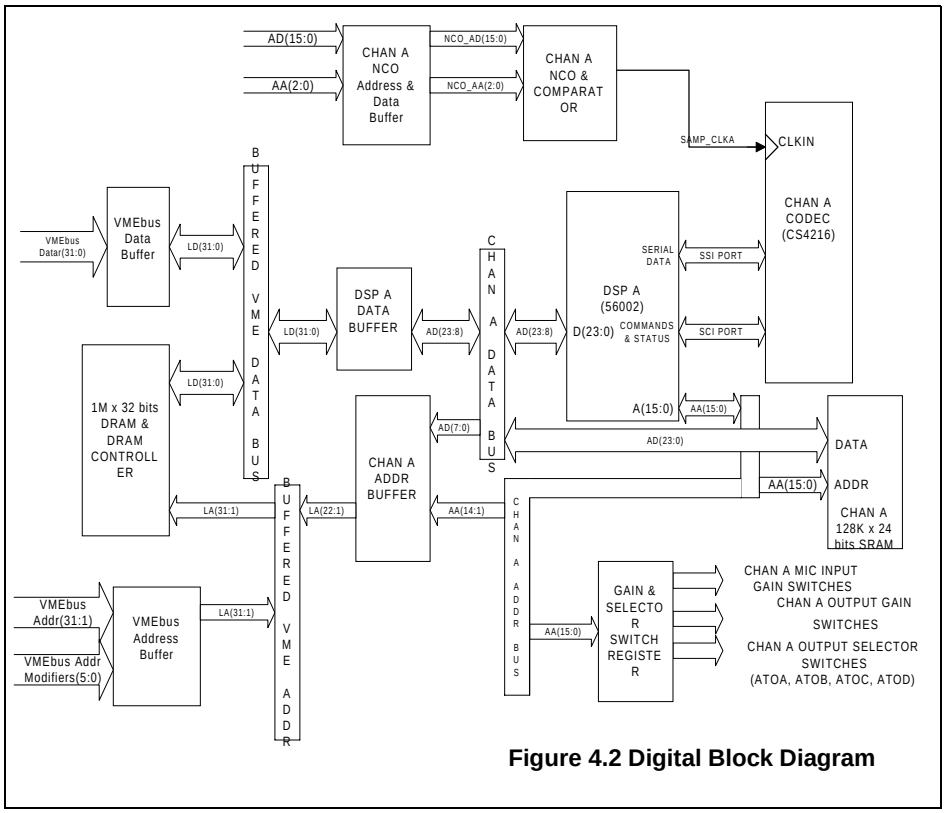


Figure 4.2 Digital Block Diagram

The VMEbus ADDRESS and DATA BUFFERS provide the interface between the onboard resources and the VMEbus. All data, status and DSP programming is accessed via the 1M x 32 bit Dynamic Random Access Memory (DRAM). DSP programs are loaded from VMEbus into DRAM. The appropriate DSP56002 chip(s) must then read DRAM and load the program intended for them into their private Static Random Access Memory (SRAM). Digital audio data is passed back and forth from/to the CS4216 Coder/Decoders (CODEC) via the SSI and SCI ports of each DSP chip. There is no mechanism to write directly from the VMEbus to each DSP's private address and data busses. Data must flow through DRAM.

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Each channel has a NUMERICALLY CONTROLLED OSCILLATOR (NCO) which provides the master clock from which the actual input and output sample rate clocks are derived. Its frequency can be programmed in very small steps to produce sample rates ranging from 6KHz to 48KHz in approximately 1Hz increments. The 56002 DSP chip programs the output frequency for the NCO. The output of the NCO is a sinewave, so a comparator circuit is used to convert the sinewave into a squarewave signal.

Each channel has its own 16-bit stereo CODEC. The CODECs contain 16-bit A/D and D/A converters and control logic. Digital data from the A/D converter and digital data to be played through the D/A is routed through the SSI serial port of each DSP to its corresponding CODEC. The CODECs use the SCI ports to accept commands and to report status information to their corresponding DSP chip.

A BUS ARBITER (not shown) controls which DSPs have access to the local bus (the buffered VMEbus address and data busses) at any given time. Arbitration is handled in a round-robin fashion to provide the fairest bus allocation when two or more DSPs are requesting use of the bus.

Each DSP has its own private bank of 128k x 24-bit SRAM that contains its program and data. Each memory bank is subdivided into 64k of Program Memory, 32k of X Memory and 32k of Y Memory. From the view of the DSP program, its program memory is accessed from 0x0000-0xFFFF, its X memory is accessed from 0x0000-0x7FFF and its Y memory is accessed from 0x0000-0x7FFF.

Each DSP must fetch its program from, and read and write data from/to the onboard 1M x 32 bit DRAM. The onboard DRAM/DSP interfaces are the only means by which digital audio data is transferred to and from the VMEbus. The VMEbus has no direct link to the DSP's private SRAM memories. Each DSP accesses locations 0x8000-0xBFFF to read and write from DRAM. Each DSP channel has an 8-bit page register that allows it to select which of 256 "pages" within the 4MB DRAM space it will access. The page number is written from the lower 8 bits of the DSP's data bus (xD(0..7)) to DRAM address bits LA(15..22). Thus there are 256 "pages" with 16,384 locations per page that any DSP may address.

From the DSP program's viewpoint, the input and output amplifier gain settings, output routing switches, NCO registers, channel LED and page select register are memory locations in the range of 0xC000-0xC017. These register functions are set "on" by writing to them and set "off" by reading from them. Table IV lists the memory map as each DSP's program "sees" it.

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Table 6. Memory Map from the DSP's Viewpoint

Addr. (from DSP View)	Channel A	Channel B	Channel C	Channel D	Function
0xC000	LEDA	LEDB	LEDC	LEDD	Channel LED
0xC001	APSR	BPSR	CPSR	DPSR	Page Select Register
0xC002	ATOA	BTOA	CTOA	DTOA	Output Routing
0xC003	ATOB	BTOB	CTOB	DTOB	Output Routing
0xC004	ATOC	BTOC	CTOC	DTOC	Output Routing
0xC005	ATOD	BTOD	CTOD	DTOD	Output Routing
0xC006	AIN_GAIN0	BIN_GAIN0	CIN_GAIN0	DIN_GAIN0	Mic. Input Gain
0xC007	AIN_GAIN20	BIN_GAIN20	CIN_GAIN20	DIN_GAIN20	Mic. Input Gain
0xC008	AIN_GAIN40	BIN_GAIN40	CIN_GAIN40	DIN_GAIN40	Mic. Input Gain
0xC009	AOUT_GAIN12	BOUT_GAIN12	COUT_GAIN12	DOUT_GAIN12	Output Amp Gain
0xC010	A NCO REG 0	B NCO REG 0	C NCO REG 0	D NCO REG 0	NCO Reg 0 Enable
0xC011	A NCO REG 1	B NCO REG 1	C NCO REG 1	D NCO REG 1	NCO Reg 1 Enable
0xC012	A NCO REG 2	B NCO REG 2	C NCO REG 2	D NCO REG 2	NCO Reg 2 Enable
0xC013	A NCO REG 3	B NCO REG 3	C NCO REG 3	D NCO REG 3	NCO Reg 3 Enable
0xC014	A NCO REG 4	B NCO REG 4	C NCO REG 4	D NCO REG 4	NCO Reg 4 Enable
0xC015	A NCO REG 5	B NCO REG 5	C NCO REG 5	D NCO REG 5	NCO Reg 5 Enable
0xC016	A NCO REG 6	B NCO REG 6	C NCO REG 6	D NCO REG 6	NCO Reg 6 Enable
0xC017	A NCO REG 7	B NCO REG 7	C NCO REG 7	D NCO REG 7	NCO Reg 7 Enable

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5. Programming Information

5.1 General

The CS4216 Audio CODEC provides input selection (mic/line), input gain setting, and output attenuation setting amplifiers as shown in the following diagrams:

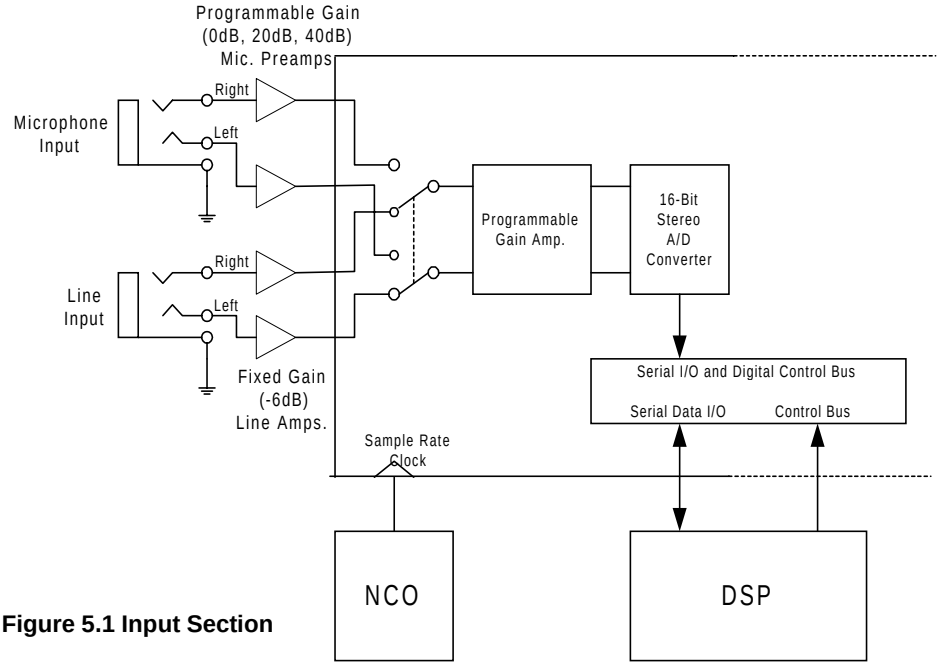


Figure 5.1 Input Section

The microphone amplifier outputs are connected to the CODEC's input 1 (left and right). The microphone amplifier provides three software programmable gains: 1 (0dB), 10 (20dB) and 100 (40dB). So when the CODEC's input gain is set to 22.5dB and the microphone amplifier's gain is set to 0dB, a 75mVrms signal at the line input will produce a full scale digital signal at the output of the A/D converter. For a mic. input amplifier gain of 20dB and a CODEC input gain of 22.5dB, a 7.5mVrms siginal will produce full scale output and for a mic. input amplifier gain setting of 40dB and a CODEC input gain of 22.5, a 0.75mVrms signal will produce full scale output. The 0dB, 12dB and 20dB gain settings affect both left and right channels simultaneously. The input attenuator gains internal to the CS4216 CODECs may be programmed independently for left and right channels. The 0dB, 12dB and 20dB gain settings may be thought of as a "coarse" adjustment or a "range" setting, while the internal programmable gain settings may be thought of as "fine" adjustments.

The line input amplifier outputs are connected to the CODEC's input 2 (left and right). The line input amplifier provides a fixed gain of 0.5 (-6dB). So when the programmable gain

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amplifier is set to 0dB, a 2Vrms signal at the line input will produce a full scale digital signal at the output of the A/D converter.

Selection of mic. or line inputs is made inside the CODEC under control of that channel's DSP.

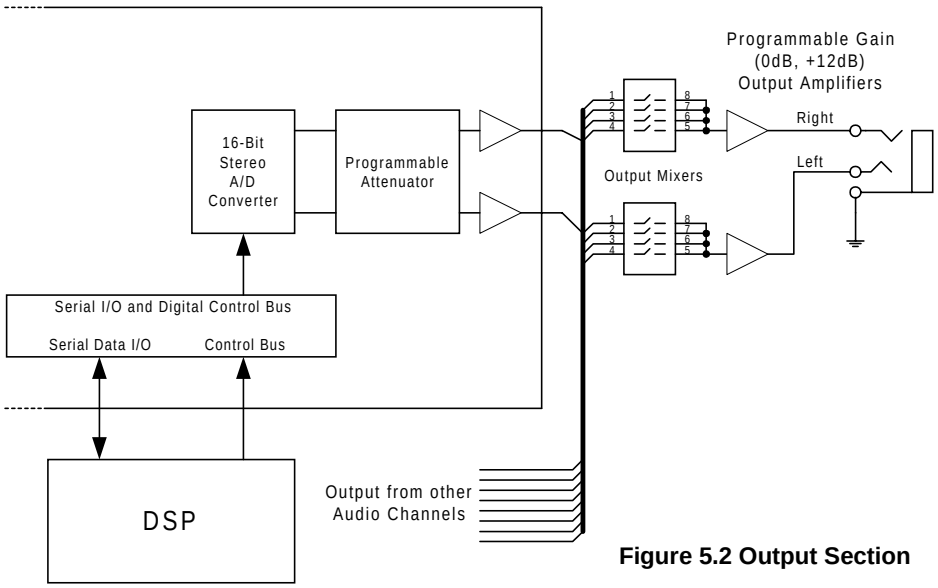


Figure 5.2 Output Section

The CODEC's output signals are connected via the mixing circuits to the line output amplifier. The line output amplifier provides a software selectable gain of 1 (0dB) or 4 (12dB). As with the input amplifiers, the 0dB and 12dB settings affect both left and right channels simultaneously. Output attenuation is independently programmable internal to the CS4216 CODEC for left and right channels. When the programmable attenuator is set to 0dB and the output amplifier gain is set to +12dB, a full scale digital signal at the input to the D/A converter will produce a 4Vrms signal at the unterminated line output. This is sufficient to drive high impedance headphones (>300Ω) with a loud signal. The line output impedance is 16Ω. If the input impedance of the device being driven is 600Ω or greater, setting the output buffer amp gain to -6dB will produce a standard CD line level (2Vrms) signal.

Figure 5.3 shows the configuration of the output mixer circuits. For the sake of simplicity, only two output channels are shown, and only half of each of those. For the MMI-4311, there are eight such mixer circuits (two for each stereo output channel). For the MMI-4310, only the left channel mixer circuits are used. The switches shown are analog switches that are controlled by each channel's DSP. The buffered outputs of any combination of CODECs may be connected to any of the four output channel amplifiers.

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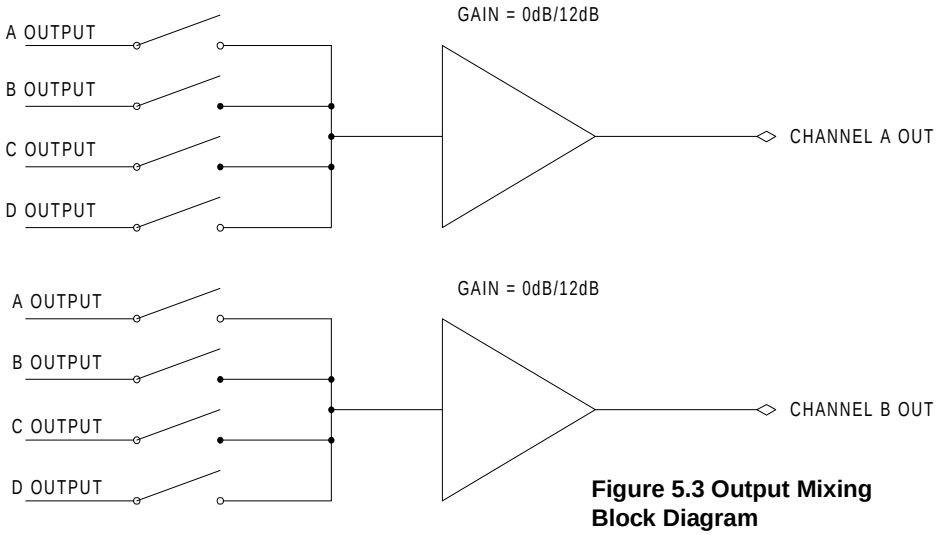


Figure 5.3 Output Mixing Block Diagram

5.2 MMI-430 Memory Map

Table 7 shows the register locations within the MMI-430's memory space. The address shown is the offset from the VMEbus base address set by the address DIP switches. This table shows the map as the host processor sees it.

Table 7. MMI-430 Memory Map

Address Space	Function	Address
General Shared DRAM	Byte-Addressable DRAM address space	0x000000 to 0x3FFDFF
43XX ID Registers	Read-Only "0" for 43XX (Read/Write for 42XX)	0x3FFE03
	Read-Only "0" for 43XX (Read/Write for 42XX)	0x3FFE07
	Read-Only "0" for 43XX (Read/Write for 42XX)	0x3FFE0B
	Read-Only "0" for 43XX (Read/Write for 42XX)	0x3FFE0F
DSP Reset Registers	DSP A Reset Register	0x3FFE13
	DSP B Reset Register	0x3FFE17
	DSP C Reset Register	0x3FFE1B

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	DSP D Reset Register	0x3FFE1F
GP LED	Front Panel General Purpose LED	0x3FFE43
DSP A Host Port I/O Space	Interrupt Control Register (ICR)	0x3FFE83
	Command Vector Register	0x3FFE87
	Interrupt Status Register (ISR)	0x3FFE8B
	Interrupt Vector Register (IVR)	0x3FFE8F
	Null Register	0x3FFE93
	Transmit/Receive High Byte	0x3FFE97
	Transmit/Receive Middle Byte	0x3FFE9B
	Transmit/Receive Low Byte	0x3FFE9F
DSP B Host Port I/O Space	Interrupt Control Register (ICR)	0x3FFEC3
	Command Vector Register	0x3FFEC7
	Interrupt Status Register (ISR)	0x3FFECB
	Interrupt Vector Register (IVR)	0x3FFECF
	Null Register	0x3FFED3
	Transmit/Receive High Byte	0x3FFED7
	Transmit/Receive Middle Byte	0x3FFEDB
	Transmit/Receive Low Byte	0x3FFEDF
DSP C Host Port I/O Space	Interrupt Control Register (ICR)	0x3FFF03
	Command Vector Register	0x3FFF07
	Interrupt Status Register (ISR)	0x3FFF0B
	Interrupt Vector Register (IVR)	0x3FFF0F
	Null Register	0x3FFF13
	Transmit/Receive High Byte	0x3FFF17
	Transmit/Receive Middle Byte	0x3FFF1B
	Transmit/Receive Low Byte	0x3FFF1F
DSP D Host Port I/O Space	Interrupt Control Register (ICR)	0x3FFF43
	Command Vector Register	0x3FFF47
	Interrupt Status Register (ISR)	0x3FFF4B
	Interrupt Vector Register (IVR)	0x3FFF4F
	Null Register	0x3FFF53

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	Transmit/Receive High Byte	0x3FFF57
	Transmit/Receive Middle Byte	0x3FFF5B
	Transmit/Receive Low Byte	0x3FFF5F

5.3 Communicating Via the DSP's Serial Ports

5.3.1 CS4216 CODEC SSI & SCI PORTS

The CS4216 stereo CODECS are connected to their corresponding DSP 56002s via each DSP's two serial ports (SSI and SCI), The SSI port is used for audio data only, and the SCI port is used for control and status only. The CS4216 CODEC is configured for its Serial Mode 4. In this mode, all control data is handled via the SCI port and all audio data is passed through the SSI port.

The output data from the A/D converter is sent out over the SDOUT pin of the SSI port. The input data to the D/A converter is received through the SDIN pin of the SSI port. Bits 0-15 of the SDOUT pin contain the 16-bit left-channel output data word. Bits 16-32 contain the 16-bit right-channel data word. Similarly for the SDIN pin, bits 0-15 contain the 16-bit left channel data word and bits 16-32 contain the 16-bit right-channel data word to be played through the D/A converter. Both input and output data words are transmitted MSB first (bit 0 = left MSB, bit 16 = right MSB).

Input and output gain settings, mic/line input switching and output muting commands are transmitted to the CODECs via the CDIN pin of the SCI port. Bits 0, and 24-31 are all zeroes. Bits 3-7 contain the left output attenuation setting. Bit 3 is the left channel MSB. Bits 8-12 contain the right output attenuation setting. Bit 8 is the right channel MSB. Bit 13 is the Mute bit. If it is set to a one, the left and right outputs are muted. Bit 14 is the mic/line control for the left channel (0 = left mic, 1 = left line). Bit 15 is the mic/line control for the right channel (0 = right mic, 1 = right line) Bits 16-19 contain the left channel input gain setting. Bit 16 is the left channel MSB. Bits 20-23 contain the right channel input gain setting. Bit 20 is the right channel MSB.

CODEC status information is send out through the CDOUT pin of the SCI port. Bits 9 and 29 contain the ADV status bit (0 = invalid left A/D data, 1 = valid left A/D data). Bits 10 and 26 contain the LCL status bit (0 = left channel normal, 1 = left channel is clipping). Bits 11 and 27 contain the RCL status bit (0 = right channel normal, 1 = right channel is clipping). Bits 14-15 and 24-25 contain the ERR status bits (00 = normal, no errors; 01 = input subframe error, control data will be ignored; 10 = sync pulse is incorrect, outputs will be muted; 11 = SCLK is outside the allowable range).

5.3.2 DSP 56002 PORT C (SSI/SCI) SETUP

Port C is a triple-function, 9-pin I/O port on the DSP 56002. Operation of Port C is controlled by three memory-mapped registers – Port C Control Register (PCC), Port C Data Direction Register (PCDDR) and Port C Data Register (PCD). The DSP's Port C Registers must be set up as follows to operate properly as a SSI Port and a SCI Port:

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5.3.3 Port C Control Register (PCC)

23		9	8	7	6	5	4	3	2	1	0
Reserved		CC8 STD	CC7 SRD	CC6 SCK	CC5 SC2	CC4 SC1	CC3 SC0	CC2 CLK	CC1 TXD	CC0 RXD	CC8 STD
0		1	1	1	1	0	0	1	1	1	1
		SSI port							SCI Port		

1 = Serial Interface

0 = Parallel I/O

5.3.4 Port C Data Direction Register (PCDDR)

23		9	8	7	6	5	4	3	2	1	0
Reserved			CC8	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
0			X	X	X	X	1	1	X	X	X

1 = Output

0 = Input

X = don’t care

5.4 SCI Port

In the MMI-430, the SCI port of each DSP only controls the corresponding CS4216 CODEC. The SCI port should be configured in mode 0 (8-bit synchronous data (shift register) mode).

5.5 SSI Port Setup

The SSI port may be viewed as two control registers (CRA, CRB), one status register (SSISR), one transmit register (TX), one receive register (RX) and a special-purpose time slot register (TSR). The DSP 56002's SSI port must be set up as follows:

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5.5.1 SSI Control Register A (CRA)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSR	WL1	WL0	DC4	DC3	DC2	DC1	DC0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0
X	1	0	0	0	0	0	1	-- Don't Care --							

WL1/0: Word Length: 16-bits

DC4-0: Two Words per Frame

5.5.2 SSI Control Register B (CRB)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RIE	TIE	RE	TE	MOD	GCK	SYN	FS1	FS0	SFD	SKD	SD2	SD1	SD0	OF1	OF0
		1	1	1	0	1	1	0	0	0	0	X	X	Don't Care	

SKD: Serial Clock Direction = Input

SD2: Frame Sync Direction = Input

SFD: Shift Direction = MSB First

FS1/0: Frame Sync Length = both 1-bit

SYN: Synchronous Tx & Rx

GCK: Continuous Clock

MOD: Network Mode

TE: Transmitter Enabled

RE: Receiver Enabled

In network mode, the SSI will receive an interrupt for each left and each right sample. The first sample in the frame is the left word and the frame sync bits in the SSI Status Register (TFS and RFS) will be set during the left time slot.

5.6 Reset Mode

When RESET is selected, all of the CODECs and DSPs are reset, all mixer analog switches are opened and all LEDs are turned off.

5.7 Output Signal Mixing

When the MMI-430 board first powers up, none of the output switches are closed. When any DSP is booted up, it is connected to all 4 outputs. The mmi-test route or DiSPATCH route_output command can be used to establish the desired mixer connections.

5.8 CODEC Control Port Mode

When a CODEC is selected, the SCI port of the corresponding DSP is connected to the CODEC's control port. The CODEC control port is a read/write 16-bit shift register configured as shown on page 21 of the CS4216 data sheet (figure 13).

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Note: There is no separate select mechanism for shifting in and shifting out the CODEC control port data. Therefore, in order to shift data out to be read, data must also be shifted in at the same time.

5.9 Numerically Controlled Oscillator (NCO) Operation

The numerically controlled oscillators are Analog Devices AD9830s. They create an extremely accurate sinewave output by making use of the linear nature of the change of phase angle for sinusoidal waveforms. The change in phase angle and the reference clock period determine the frequency by the following formula:

$$f = \Delta(\text{phase}) \times f(\text{ref. clock}) / 2\pi$$

The Δ(phase) value is entered as two 16 bit words. These are entered into the 32 bit FREQ0 register of the NCO. The NCO makes use of an internal sine lookup table and a 10-bit DAC to generate the necessary sinusoidal waveform from the given phase value. A filter and comparator stage after the NCO converts the sinusoidal waveform into a squarewave for use as the master clock for the corresponding CODEC. The CS4216 CODECs are set to divide their master clock frequencies by 256 to obtain the sample rate. The sample rate is determined by the following formula:

$$SR = [\ NCO \times 25{,}000{,}000\ ] / [\ 2{,}147{,}483{,}648 \times 256\ ]$$

Where NCO = The 32 bit phase value

Each NCO is connected to its corresponding DSP's private 16-bit data bus. Thus the only means of programming the NCOs is via the DSP chips. The DiSPATCH SET_SRATE command can be used to set the correct sample clock frequency.

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6. Performance Specifications

6.1 General

A/D CONVERTER	16-bits Delta-Sigma
I/P LEVEL CONTROL	Software controlled input gain in three ranges: 0 to 22.5dB in 1.5dB steps 20dB to 42.5dB in 1.5dB steps 40 to 62.5dB in 1.5dB steps
D/A CONVERTER	16-bits Delta-Sigma, 64x oversampling
O/P VOLUME CONTROL	Software controlled output gain/attenuation: Two ranges -46.5dB to 0dB in 1.5dB steps –34.5dB to +12dB in 1.5dB steps
DRAM	1M x 32bits VMEbus
SRAM	64k x 24bits Program Memory (for each DSP) 32k x 24Bits X Memory (for each DSP) 32k x 24bits Y Memory (for each DSP)

6.2 Line Level Inputs

INPUT IMPEDANCE	20KΩ nominal
AMPLITUDE	0.15Vrms to 2Vrms (full scale)
FREQUENCY RESPONSE	+0.2dB/-0.5dB, 20 to 20KHz
THD+NOISE	<0.02% @ 1KHz, <0.05% 20 to 20KHz

6.3 Microphone Input

TYPE	Single ended
INPUT IMPEDANCE	47KΩ nominal
AMPLITUDE	6mVrms to 78mVrms (full scale)

6.4 Line Level Outputs

OUTPUT IMPEDANCE	16Ω nominal
AMPLITUDE	200mVrms to 4Vrms into 600Ω (full scale)
FREQUENCY RESPONSE	+0.2dB/-0.5dB, 20 to 20KHz
THD+NOISE	<0.03% @ 1KHz, <0.05% 20 to 20KHz

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6.5 Power, Dimensions and Environmental

+5VDC	2.25A (max.) (11.25W)
+12VDC	67mA (max.) (804mW)
-12VDC	67mA (max.) (804mW)
BOARD SIZE	Standard 6U – 9.187” x 6.299” x 0.800”
WEIGHT	13 oz. (0.369 kg)
STORAGE TEMPERATURE	-20 to +125 degrees C
OPERATING TEMPERATURE	0 to +70 degrees C
RELATIVE HUMIDITY	0 to 95% non-condensing

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Appendix A. Related Documents

A.1. VisiCom Publications

- DiSPATCH User's Manual

  VisiCom Part Number 880-3095-001

A.2. Other Publications

DSP56000/DSP56002 Digital Signal Processor User's Manual, DSP56000UM/AD REV 2 Available from: Motorola Literature Distribution P.O. Box 20912 Phoenix, Arizona 85036
CS4216 Stereo Audio CODEC Data Sheet Publication Number: DS83PP5 January 1993 Available from :Crystal Semiconductor Corporation P.O. Box 17847 4210 S. Industrial Dr. Austin, Texas 78744 Tel: (512) 445-7222 Fax: (512) 445-7581
Detailed information on the AD9830 Numerically Controlled Oscillator can be found on the Analog Devices website: http://www.analog.com Further information can be obtained from : Analog Devices, Inc. One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106

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