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ADM-3
DUMB TERMINAL
MAINTENANCE MANUAL

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SECTION 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual contains a general description, installation and operating instructions, theory of operation, and maintenance information for the Lear Siegler ADM-3 Interactive Display Terminal.

Additional information is contained in the ADM-3 Operator's Handbook. The maintenance technician should be thoroughly familiar with material in the Operator's Handbook before attempting to troubleshoot or repair the ADM-3.

1.2 ADM-3 CAPABILITIES

The ADM-3 has the following general capabilities:

a. Receives USASCII-coded data from a remote computer and displays it on a CRT screen displaying up to 960 characters (1920 characters, optional).

b. Permits the operator, using a keyboard, to compose a message, visible on the screen as it is transmitted to the remote computer or other device.

c. Through an extension port, permits interfacing with a hard-copy printer, magnetic tape recorder, or other terminals.

d. Provides for full-duplex or half-duplex communications, through either an RS-232C or current-loop interface.

e. Permits 202 communications line turnaround by means of either EOT or ETX code-turnaround (in which the controlling device transmits a turnaround code to give control to the device at the other end of the line), or secondary-channel turnaround (in which a secondary channel selection establishes control of a device for data transmission through the primary channel).

1.3 PHYSICAL DESCRIPTION

Principal components of the ADM-3 are as follows:

a. A molded case comprising a base and a cover. The base contains the power switch, power transformer, beeper speaker, and intercomponent cabling. The main circuit board rests on supports molded in the base and is held in place by two guide pins.

   The cover contains the monitor CRT and other monitor subassemblies. It is hinged at the rear so that all components of the ADM-3 are accessible when it is opened. The cover is easily removed by swinging it back as far as it will go, and then sliding it to the left, off the hinge pins. (The monitor-connecting cable must be disconnected.)

b. The main circuit board which contains all elements of the ADM-3 except monitor, power switch and transformer, and beeper speaker. The keyboard consists of integrated key rows and is built directly on the main circuit board.

   The main circuit board rests on supports within the base and is held in place by guide pins. Two connectors on the rear edge of the board provide the RS-232C and current loop (optional printer port) interface at both the main and extension ports.

c. The CRT monitor which comprises three subassemblies, as follows:

   1. The CRT itself. The CRT is mounted in a metal frame with its face held against the cover bezel by two brackets, each retained by a single screw.

2. A printed circuit board (video board) containing most circuits of the monitor. The video board is held in place by the cover molding on one side, and by pressure of the flyback assembly on the other.

3. The flyback assembly, which is held in place by a single screw. Bosses in the cover molding assembly surface retain the edge of the video board.

1.4 SPECIFICATIONS

DISPLAY

Screen

12-inch (diagonally measured) rectangular CRT with P4 white phosphor and etched non-glare surface.

Display Format

Standard: 960 characters, 12 lines of 80 characters
Optional: 1920 characters, 24 lines of 80 characters

Character Set

Generated: 128 ASCII characters (upper and lower case, numeric, punctuation and control)
Displayed: Standard – 64 ASCII characters (upper case, numeric, punctuation)
Optional – 95 ASCII characters (upper and lower case, numeric, punctuation)

Character Generation

5 x 7 dot matrix, 0.18 in. high x 0.075 in. wide

Cursor

Underline, homes to lower left of screen

Data Entry

New data enters on bottom line of screen; line feed causes upward scrolling of entire display page with top-of-page overflow.

Refresh Rate

60Hz or 50Hz, dependent on an internal switch set to match power line frequency.

KEYBOARD

59-key solid-state keyboard designed similar to a teletypewriter layout and containing the following keys:

47 alphanumeric keys	CTRL (Control)
RETURN	BREAK
LINE FEED	CLEAR
RUB	REPT (Repeat)
HERE IS	ESC (Escape)
SHIFT	Space Bar

COMMUNICATIONS

Modem Interface

EIA standard RS-232C and 20mA current loop (switch selectable)

Extension Interface

Extension RS-232C port for interfacing serial asynchronous auxiliary device (e.g., hard copy printer, magnetic tape recorder or additional data terminals).

Optionally, the extension port is available with both RS-232C and 20mA current loop interfaces.

Communication Rates

75, 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200 baud (switch selectable)

Send/Receive Modes

Full duplex and half duplex (switch selectable)

Word Structure

Total word length is switch selectable to 9, 10 or 11 bits consisting of the following:

7-bit data word	1 start bit
8th bit - parity, odd or even	1 or 2 stop bits
OR	
forced to 1 or 0	
OR	
8th bit suppressed	

PHYSICAL AND ELECTRICAL

Dimensions

13.5 in. high x 15.5 in. wide x 19 in. deep

Weight

25 pounds

Power Consumption

80 watts @ 115 Vac ± 10%

50Hz or 60Hz, switch selectable
Optional 230Vac

Operating Environment

5 - 55°C (41 - 122°F), 5 - 95% relative humidity without condensation.

MONITOR ELECTRICAL SPECIFICATIONS

TABLE 1-1. MONITOR INPUT DATA SPECIFICATIONS

	Video	Vertical Drive Signal	Horizontal Drive Signal
Input Connector	(Necessary Accessory — Available) Printed circuit board card edge connector — Viking No. 2VK10S/1-2 or Amphenol No. 225-21031-101		
Pulse Rate or Width	Pulse Width: 100 nsec min.	Pulse Rate: 47 to 63 pulses/sec	Pulse Rate: 15,000 to 16,500 pulses/sec
Amplitude	Low = Zero $^{+0.4}_{-0.0}$ volts High = 4 ± 1.5 volts		
Signal Rise and Fall Times (10% to 90% amplitude	Less than 20 nsec	Less than 100 nsec	Less than 50 nsec

DATA DISPLAY SPECIFICATIONS

Input Impedance

	Minimum Shunt Resistance	Maximum Shunt Capacitance
(a) Video Input:	3.3 K ohms	40 pF
(b) Vertical Drive Input:	3.3 k ohms	40 pF
(c) Horizontal Drive Input:	470 ohms	40 pF

Video Amplifier

(a) Bandwidth:	12 MHz (−3 dB)
(b) Rise and Fall Times (10% to 90% amplitude):	Less than 35 nsec (linear mode)
(c) Storage Time:	315 nsec, maximum (linear mode)

Retrace and Delay Times

(a) Vertical:	900 sec retrace, maximum
(b) Horizontal:	7 sec retrace plus 4 sec delay, maximum

TABLE 1-2. CRT DISPLAY SPECIFICATIONS

Nominal Diagonal Measurement (inches)	Phosphor	*Resolution (TV Lines)	
		Center	Corner
12	P4	900 at 40 fL	800 at 40 fL

*Resolution is measured in accordance with EIA RS-375 except Burst Modulation (or (Depth of Modulation) is adjusted for 100 percent.

Geometric Distortion

The perimeter of a full field of characters shall approach an ideal rectangle to within ±1.5% of the rectangle height.

Power Requirements

Input Connector	Receptable, Molex No. 03-06-1041 Supplied with Unit Mating Plug, Molex No. 03-06-2041 — Necessry Accessory (Available)
Input Voltage	105 V to 130 V rms (120 V nominal); 50/60 Hz
Input Power	24W (Nominal)
Output Voltages	+15 V DC (short circuit protected) +12 kV DC; 12.6 V rms

ENVIRONMENTAL SPECIFICATIONS

Temperature (Chassis or Custom Unit)

Operating Range:	5°C to 55°C Ambient
Storage Range:	−40°C to 65°C

Humidity

5 to 95 percent (Noncondensing)

Altitude

Operating Range:	Up to 10,000 feet

HUMAN FACTORS SPECIFICATIONS

X-Ray Radiation

These units comply with DHEW Rules-42-CFR-Part 78

SECTION 2
INSTALLATION

2.1 GENERAL

This section contains information to aid in installing the ADM-3 and preparing it for use. Included are instructions and information for inspecting the ADM-3, installing it in a suitable environment, setting internal switches, connecting cables, and turning-on power.

2.2 VISUAL INSPECTION

It is recommended that you save the orginal shipping carton and all packing materials to prevent damage should you wish to transport or ship the terminal.

Carefully inspect your ADM-3 for signs of damage during shipping. The terminal has undergone stringent quality inspections and operational tests prior to shipping; it left the factory in perfect operating condition.

If the unit is damaged, notify the carrier immediately. Save the damaged shipping container as evidence for inspection by the carrier.

Only the consignee may register a claim with the carrier for damage during shipment. However, Lear Siegler Data Products will cooperate fully with the customer should such action be necessary.

2.3 INSTALLATION

The ADM-3 is designed to operate in a wide range of environmental conditions:

5 - 55°C (41 - 122°F), 5 - 95% relative humidity without condensation.

The unit is designed to set on a table or desk top, or any other suitable hard, flat surface.

CAUTION

In cold climates, care should be exercised to allow the temperature of the terminal to equalize with room temperature before removing the unit from the shipping carton; this will prevent moisture from condensing on a cold terminal exposed to warm air. Avoid operating the unit on a soft surface, such as carpeting, which would obstruct the flow of cooling air up through the bottom of the chassis. This could result in overheating and damage to the unit.

2.4 SETTING INTERNAL SWITCHES

Twelve slide switches located inside the ADM-3 case on the printed circuit logic board are used to select various terminal operating characteristics. These switches are set at the factory during pre-shipping checkout according to operating parameters specified by the customer when ordering the terminal. Only the parameters listed on the Ordering Form packed inside the shipping carton have been selected at the factory. Any required switch setting changes should be made before attempting to operate the terminal. Locations of the internal switches are shown in Figure 2-1.

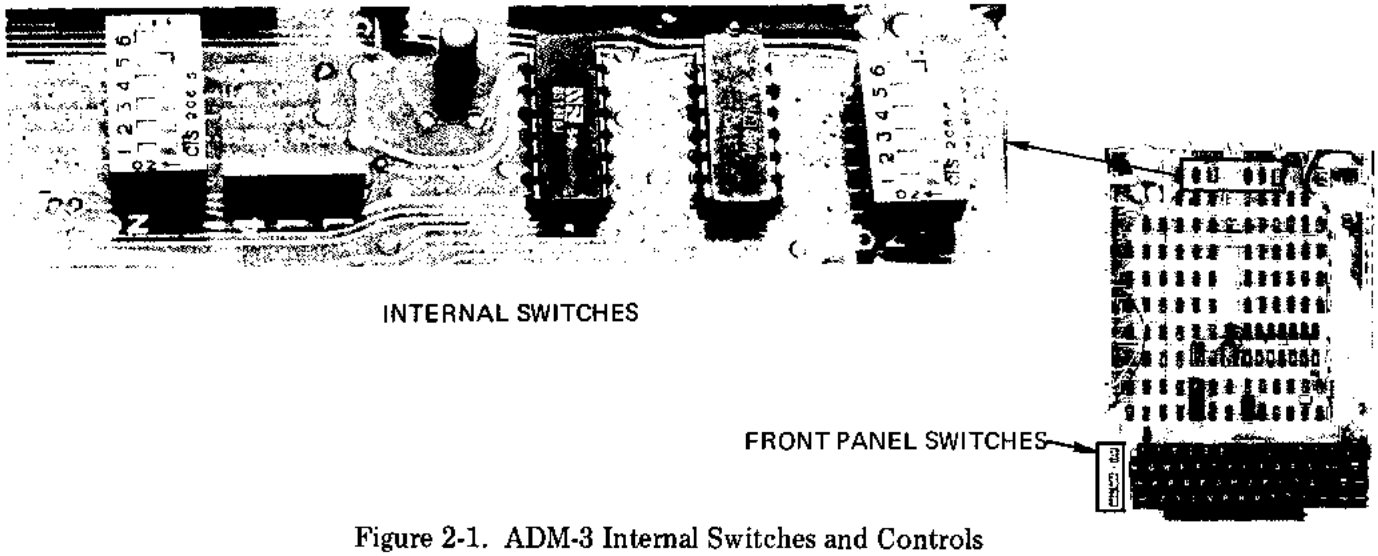


Figure 2-1. ADM-3 Internal Switches and Controls

WARNING

Always disconnect the ac power cord from the power source before opening the ADM-3 case to access any internal component.

Switch functions are described below:

SPACE — ADV

In SPACE position, selects destructive cursor. Pressing the space bar or receiving a space code ALWAYS overwrites the display memory location with a space code and advances the cursor.

In ADV position, selects non-destructive cursor between a Return and subsequent Line Feed only; the cursor may be advanced but a space code does not overwrite display memory locations. The space code is destructive between a Line Feed and the next Return.

UC DISP — U/L DISP

In UC DISP position, allows display of upper case characters only. Lower case codes are transmitted as such but are converted to upper case for display. If lower case is not installed or if it is not to be utilized, the switch must stay in the UC DISP position.

In U/L DISP position, allows display of upper and lower case characters if the terminal is equipped with the Upper/Lower Case option.

DISABLE — KB LOCK

In DISABLE position, prevents locking of keyboard.

In KB LOCK position, allows keyboard to be electrically disabled (locked) by remote control codes.

DISABLE — CLEAR SCREEN

In DISABLE position, prevents clearing of displayed information except by executing repetitive line feeds.

In CLEAR SCREEN position, allows computer to clear ADM-3 screen by transmitting a control code (CTRL Z).

50Hz — 60 Hz

Selects 50Hz or 60Hz display refresh rate; must be set to correspond with input power frequency.

12 LINE — 24 LINE

If terminal is equipped with 24-line display option, this switch may be used to select 12 or 24 line display.

On terminals with standard 12 line display this switch must be set to the 12 LINE position.

LOCAL — OFF
103 — OFF
202 — OFF

These three switches are used to select ADM-3 operation for one of the following methods of interfacing to the computer: (1) without modems (direct, local connection), (2) with 103-type modems, or (3) with 202-type modems. The appropriate switch is set (left position) according to the connection method used; the other two switches must be set to the OFF positions.

Setting the LOCAL switch causes line CA (Request to Send) to rise and fall with each character transmitted.

Setting the 103 switch holds CA high, if required.

Setting the 202 switch enables 202-type operation using the secondary channel or turnaround code to change the direction of data over the primary data channel (half-duplex operation).

With all three switches off, CA is held low all the time.

CODE — SEC CHAN

This switch is active only with the 202 switch (described above) in the on position. It is used to select the method of line turnaround for half-duplex operation with 202-type modems.

In SEC CHAN position, enables line turnaround using the secondary channel. 202 modem operation is summarized in the back of this handbook.

The CODE position allows line turnaround control by a turnaround code transmitted over the primary data channel. The turnaround code may be either ETX or EOT, as selected by the switches described below.

EXT — OFF
EOT — OFF

One of these two switches is set to the on (left) position to select the line turnaround code for primary chanel operation with 202-type modems. (See CODE - SEC CHAN switch description.) With 202 and CODE selected, one of these switches must be on and the other off; with 202 and SEC CHAN selected, or 202 off, both the ETX and EOT switches must be set to the OFF positions.

2.5 SETTING FRONT PANEL SWITCHES

Twenty slide switches for selecting the primary terminal operating characteristics are accessible from the ADM-3 front panel without opening the case or removing power to the unit. To gain access to these switches, remove the screw securing the identification plate on the left side of the keyboard and remove the ID plate. The switches are shown in Figure 2-2.

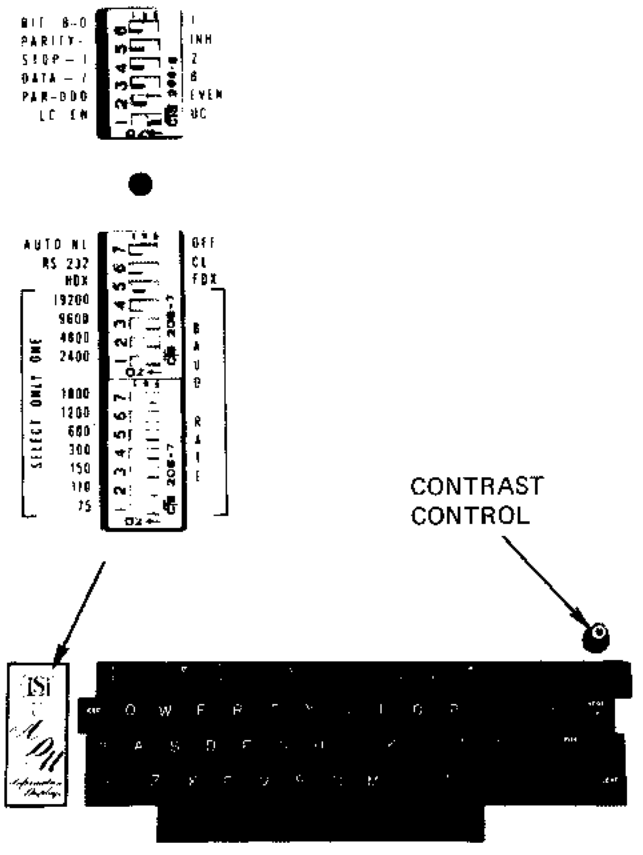


Figure 2-2. ADM-3 Front Panel Switches

It is recommended that you check the positions of these switches before operating the terminal for the first time. Switch functions are described below:

BIT 8-0 — 1

This switch has effect only with the DATA-7 – 8 switch in the 8 position.

In BIT 8-0 position, bit 8 is forced to a zero value.

In the 1 position, bit 8 is forced to a one value.

PARITY — INH

In PARITY position, the bit following the 7 - or 8 - bit data word is a parity bit (parity enabled).

In INH position, no parity bit will be generated (parity inhibited). The bit following the data word will be the (first) stop bit.

STOP - 1 — 2

In STOP-1 position, one stop bit is generated.

In the 2 position, two stop bits are generated.

DATA - 7 — 8

In DATA-7 position, 7-bit data word length is selected.

In the 8 position, 8-bit data word length is selected. (The 8-bit word consists of the standard 7-bit data word plus an 8th bit forced to one or zero according to the setting of the BIT 8-0 – 1 switch.)

PARITY-ODD — EVEN

This switch has effect only with the PARITY – INH switch in the PARITY position.

In PARITY-ODD position, selects odd parity.

In EVEN position, selects even parity.

LC EN — UC

In LC EN position, the SHIFT key is fully operational allowing generation of both upper and lower case alphabetic character codes.

In UC position, only upper case alphabetic characters will be generated regardless whether of not the SHIFT key is held down. The SHIFT key remains operational for all non-alphabetic keys.

AUTO NL — OFF

In AUTO NL position, typing in the 80th character position will automatically cause the cursor to move to the first position of the bottom line and the display to scroll upward one line. The operator continues typing on the next new line.

In OFF position, the automatic New Line function is disabled. Continued typing at the 80th character position transmits each new character and changes the 80th character on the display.

RS232 — CL

In RS-232 position, selects RS-232C communications at the MODEM (computer) interface connector on the rear panel.

In CL position, selects 20mA current loop communications at the MODEM interface connector.

HDX — FDX

In HDX position, selects half duplex operation. Characters typed are transmitted and automatically echoed back from the ADM-3 I/O Channel for display.

In FDX position, selects full duplex operation. Characters typed are displayed only if echoed back by the computer or modem.

Communication Rate Switches

19200		
9600	B	These switches are used to select the send/receive rate for data communications with the computer and auxiliary device. Setting one switch to the left-hand (BAUD RATE) position selects the associated rate.
4800	A	
2400	U	
1800	D	
1200		
600	R	
300	A	
150	T	
110	E	
75		

NOTE

Only one BAUD RATE switch may be selected (left position) at a time.

2.6 SETTING DISPLAY CONTROLS

Contrast

The Contrast control is located to the right of the keyboard on the ADM-3 front panel. It is used by the opertor to adjust brightness of the characters for optimum readability. The Contrast knob is turned clockwise to increase character brightness, counterclockwise to decrease brightness.

Background Intensity

A Background Intensity potentiometer is located inside the ADM-3 case on the circuit board in the top of the case. (See Figure 2-1.) Background intensity is adjusted at the factory before the terminal is shipped and should not require re-adjustment prior to using the terminal.

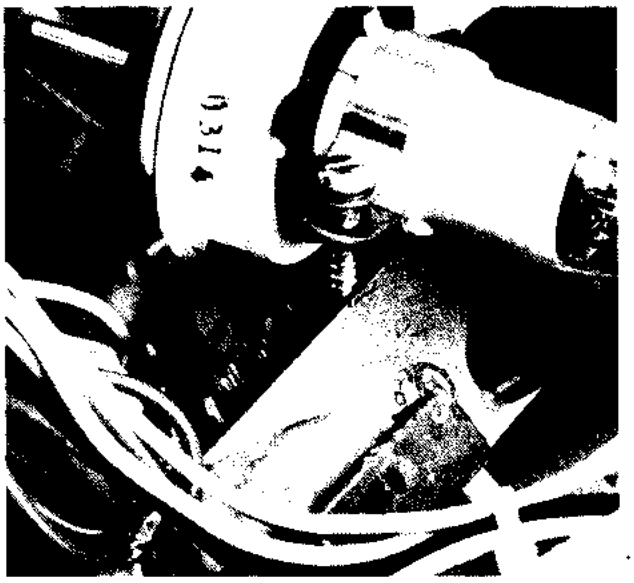


Figure 2-3. Background Intensity Control (located in top of case)

WARNING

Because the Background Intensity control must be adjusted with the ADM-3 case open with power on, it should be adjusted only by qualified service personnel.

ON/OFF Switch

The power ON/OFF switch is located on the ADM-3 rear panel.

2.7 CONNECTING CABLES AND TURNING ON POWER

a. With the ON/OFF switch in the OFF position, plug the ADM-3 power cord into the proper AC power outlet.

b. Connect the interface cable from the computer or modem to the MODEM interface connector on the ADM-3 rear panel.

c. Connect the inteface cable from the auxiliary device (if present in your system) to the EXTENSION interface connector on the ADM-3 rear panel.

d. Check the settings of all front panel switches to verify that the terminal is set up for proper operation in your system. Make switch setting changes if necessary.

e. Set the ON/OFF power switch to the ON position.

f. Allow approximately 20 seconds for the unit to warm up. The cursor should appear near the bottom of the screen.

   If the cursor does not appear, adjust the Contrast control on the front panel for proper intensity.

NOTE

If the Full-Duplex mode is selected, typing at the keyboard will not display characters unless echo-back is provided by the computer or modem. If half-duplex is selected, data will be displayed only if clear-to-send is present or cable is disconnected.

SECTION 3

OPERATION

3.1 GENERAL

This section contains information and instructions for using the ADM-3 keyboard facilities, and for programming control functions at the computer. The keyboard allows the operator to generate and transmit to the computer (and/or auxiliary device) all 128 USASCII character codes.

3.2 DISPLAYING CHARACTERS

In the standard ADM-3, 64 characters are displayed on the screen (upper case alphabet, numbers and most symbols and punctuation). When a non-displayable lower case character is typed, the proper lower case code is transmitted but the character is displayed as upper case.

If your terminal contains the Upper/Lower Case Display feature, 95 characters will be displayed (upper and lower case alphabet, numbers and all punctuation and symbols).

NOTE

Typing at the keyboard always generates codes which are transmitted; however, in order for characters to be displayed and control codes to affect the ADM-3 display the codes must be echoed back to the ADM-3 display memory and control logic, either by the computer (FDX) or the ADM-3 I/O Channel (HDX).

All display actions described in the key descriptions that follow assume the generated codes are echoed.

3.3 SPECIAL FUNCTION KEYS

In addition to the displayable character keys, the ADM-3 keyboard contains a number of other keys for various terminal and system control functions. Use of these keys is described below:

RETURN Key

The code generated by this key moves the cursor to the first character position of the bottom line.

If the front panel SPACE-ADV switch is in the ADV position, the space code is non-destructive after typing the RETURN key; that is, the operator or computer can space over data on the line without overwriting each character with a space. The space bar remains non-destructive following a RETURN function until a LINE FEED code is generated.

LINE FEED Key

The code generated by this key causes the entire display to move upward one line, leaving the cursor positioned on the next new (bottom) line. LINE FEED does not return the cursor to the first character position of the new line.

SHIFT Keys

Either of the two SHIFT keys is held down while typing another key to generate upper case alphabetic characters or to generate the character shown in the upper portion of a typed key.

NOTE

Setting the "LC EN - UC" switch under the front panel ID plate to the UC position causes upper case alphabetic characters to be generated with or without the SHIFT key depressed. The SHIFT key remains operational for all non-alphabetic keys.

RUB (Rubout) Key

This key (typed while holding down the SHIFT key) transmits a non-displayable Rubout code (ASCII DEL) to the computer. The cursor is not advanced and the character code stored in the ADM-3 display memory is not overwritten.

The Rubout function is normally used to tell the computer that a previous character should be deleted.

The lower case RUB key transmits/displays an underline.

REPT (Repeat) Key

This key can be held down while pressing a character key to repeat the character at a rate of 12.5 per second. (If the terminal is operating at a baud rate that will not permit 12.5 cps transmission, the repeat rate is reduced to the transmission rate.)

Space Bar

The Space Bar is considered a displayable character key.

Pressing the Space Bar causes the ASCII code for a space to be transmitted and stored in the ADM-3 display memory and a blank space to appear on the screen. (For the only exceptions see RETURN Key).

CTRL (Control) Key

This key, when held down while typing another key, modifies the code pattern of the typed key. The code is forced to one of the two control code columns in the ASCII Code chart.

Of the 32 control code combinations possible from the keyboard, four may be used to effect actions within the ADM-3:

Backspace (CTRL/H). Each time the H key is typed while holding down the CTRL key, the cursor moves non-destructively one character position to the left. The CTRL/H backspace code is transmitted to the computer. CTRL/H may be used in conjunction with the Repeat key.

Bell (CTRL/G). Sounds the audible beep in the ADM-3 and transmits the CTRL/G bell code.

Return (CTRL/M). Duplicates the function of the RETURN key.

Line Feed (CTRL/J). Duplicates the function of the LINE FEED key.

Lock Keyboard (CTRL/O). Electrically locks (disables) the ADM-3 keyboard, preventing any further keyboard activities. The keyboard can only be unlocked by a control code from the computer, or by switching power to the terminal off, then on again.

ESC (Escape) Key

This key transmits to the computer an ASCII Escape code, the function of which is entirely dependent on the computer.

CLEAR Key

Typing the CLEAR key while holding down the SHIFT key clears the entire screen to spaces. (This function may be disabled by the internal CLEAR SCREEN — DISABLE Switch.)

HERE IS Key

If your terminal is equipped with the Automatic Answer Back feature, typing this key transmits a identification message (stored in the ADM-3 in a special memory) to identify your terminal and alert the computer that a message is to follow.

In terminals without Automatic Answer Back capability, this key has no function.

BREAK Key

This key activates the standard teletypewriter Break function, normally used to interrupt an incoming message.

NOTE

The Break function is sustained as long as the BREAK key is held down. Holding the key down for an extended period may cause the computer to disconnect from your terminal.

3.4 PROGRAMMING AND WORD STRUCTURE

The computer to which the ADM-3 is interfaced has full control over the terminal. All control functions which are possible from the ADM-3 keyboard, plus a few additional functions, can also be executed from the computer.

The computer controls the ADM-3 by transmitting the appropriate ASCII codes. Displayable character codes will be displayed, and valid control codes will be recognized and acted upon.

3.4.1 Remote Control Functions

The remote computer can perform the following control functions:

Backspace BS (CTRL/H). Moves the cursor non-destructively one character position to the left.

Bell BEL (CTRL/G). Sounds the audible beep in the ADM-3.

Return CR (CTRL/M). Moves the cursor non-destructively to the first character position of the present line.

Line Feed LF (CTRL/J). Causes the entire display to move upward one line, leaving the cursor positioned in the same character position on the next new line.

Lock Keyboard SI (CTRL/O). Electrically locks the ADM-3 keyboard, disabling all keyboard functions.

Unlock Keyboard SO (CTRL/N). Unlocks the ADM-3 keyboard, restoring all keyboard functions.

Clear Screen SUB (CTRL/Z). Clears all character positions in the ADM-3 display memory and clears the screen to blank spaces. (This function may be disabled by the internal DISABLE – CLEAR SCREEN switch.)

The Reference Tables 3-1 and 3-2 of this manual show the actual binary codes generated by the ADM-3 and used for computer control of the terminal.

Table 3-1. ADM-3 Control Codes

Code	ASCII Mnemonic	Function ADM-3
CTRL/@	NUL	
CTRL/A	SOH	
CTRL/B	STX	
CTRL/C	ETX	Available as secondary channel line turnaround code for 202 modem operation
CTRL/D	EOT	Available as secondary channel line turnaround code for 202 modem operation
CTRL/E	ENQ	Initiates ID message in terminals with automatic "Answer Back" option*
CTRL/F	ACK	
CTRL/G	BEL	Sounds audible beep in ADM-3
CTRL/H	BS	Backspace
CTRL/I	HT	
CTRL/J	LF	Line Feed
CTRL/K	VT	
CTRL/L	FF	
CTRL/M	CR	Return
CTRL/N	SO	Unlock Keyboard*
CTRL/O	SI	Lock Keyboard*
CTRL/P	DLE	
CTRL/Q	DC1	
CTRL/R	DC2	
CTRL/S	DC3	
CTRL/T	DC4	
CTRL/V	NAK	
CTRL/V	SYN	
CTRL/W	ETB	
CTRL/X	CAN	
CTRL/Y	EM	
CTRL/Z	SUB	Clear Screen
CTRL/[	ESC	
CTRL/×	FS	
CTRL/]	GS	
CTRL/	RS	

*Executable only from computer.

Table 3-2 USASCII Character Codes

		CONTROL		GRAPHIC CHARACTER SET					
BITS	BITS	0	1	2	3	4	5	6	7
4321	765	000	001	010	011	100	101	110	111
0000		NUL	DLE	SP		@	P	`	p
0001		SOH	DC1	!	1	A	Q	a	q
0010		STX	DC2	"	2	B	R	b	r
0011		ETX	DC3	#	3	C	S	c	s
0100		EOT	DC4	$	4	D	T	d	t
0101		ENQ	NAK	%	5	E	U	e	u
0110		ACK	SYN	&	6	F	V	f	v
0111		BEEP	ETB	'	7	G	W	g	w
1000		BS	CAN	(	8	H	X	h	x
1001		HT	EM	)	9	I	Y	i	y
1010		LF	SUB	*	:	J	Z	j	z
1011		VT	ESC	+	;	K	[	k	{
1100		FF	FS	,	<	L	\	l	|
1101		CR	GS	-	=	M	]	m	}
1110		SO	RS	.	>	N	^	n	~
1111		SI	US	/	?	O	+	o	DEL

Control Codes (Generated by holding CTRL key while typing the corresponding key shown in columns 4 and 5.)

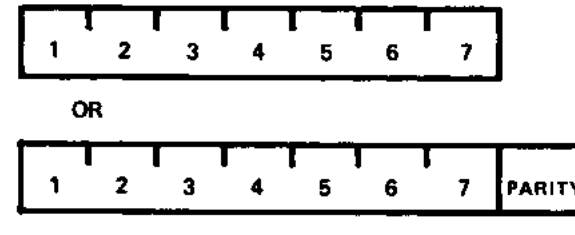
Displayable in standard ADM-3

Displayable with ADM-3 Upper/Lower Case Display feature.

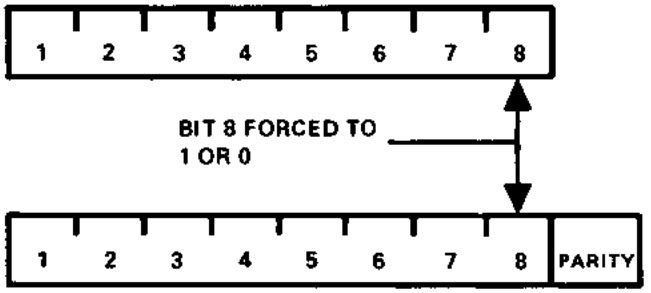
3.4.2 Data Character Format

The ADM-3 uses USASCII (United States of America Standard Code for Information Interchange). USASCII is a 7-bit code. But because many of the computers and other devices to which the ADM-3 may be interfaced use 8-bit words (plus parity or without parity), the ADM-3 offers a wide choice of word formats selectable by the user.

The data character may be 7 bits in length, with or without an optional parity bit generated on transmission:

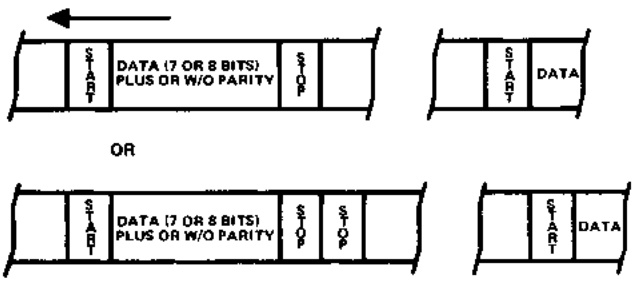


The data character may be 8 bits in length, plus or without the optional parity bit. In the case of 8-bit characters, bit 8 is always forced to 1 or 0 as selected by the user.



3.4.3 Data Transmission Format

The ADM-3 uses asynchronous transmission. This means each character is transmitted as a complete, self-contained message consisting of the data character with or without parity, preceded by a start bit and followed by one or two stop bits.



When the start bit is received, a clock signal is initiated to clock in the remainder of the word. The one or two stop bits are used to signify the end of the word and terminate the receive clock.

Generally, transmission rates of 110 baud and lower use two stop bits, and rates of 150 and higher use one stop bit.

The ADM-3 control codes and the USASCII code set are shown in tables 3-1 and 3-2, respectively.

SECTION 4
THEORY OF OPERATION

4.1 GENERAL

This section describes the manner in which the ADM-3 performs its different functions. Logic is first described with reference to an overall block diagram, and then each element shown in the block diagram is described with reference to specific illustrations and to logic diagrams contained in Section 6 of this manual (Drawings).

4.2 GENERAL FUNCTIONAL DESCRIPTION

The general organization of logic in ADM-3 is shown in figure 4-1. This figure divides ADM-3 logic into functional blocks and shows the relationships between blocks. It also indicates the sheet of the logic diagram on which logic in any block is detailed.

4.2.1 Display Generation

Signals that cause a display to be generated and maintained on the screen are furnished by a string of counters (display counter logic).

The first counter (the dot counter) is clocked by pulses from an oscillator. This clock is the primary timing signal in the ADM-3. The purpose of the dot counter is to time the presentation of the sequential address to the character generator and the presetting of the video serializer. Each increment of the counter defines the position of a single dot in any line (dot row) of any character in the display. Any character is made up of a 5 x 7 array of dots (figure 4-2). A character position is seven dots wide and nine dots high to provide 2-dot spacing between characters both horizontally and vertically.

A single horizontal sweep of the CRT beam produces all dots in a given dot row for all characters in the character row. The character dot counter is incremented for every seventh dot column to define the position of each character in the row. At the end of each dot row, the line counter is incremented and the next dot row is scanned out. The character row counter is incremented by every ninth dot line to define the position of the next character row.

The four display counter outputs control memory addressing, character generation, and many other functions of ADM-3 logic.

4.2.2 Display Refresh Operation

Except when received data is being loaded, the contents of the refresh memory (an entire "page" of data) are continuously presented on the screen. Memory address logic requires only sequential character and row counts (CCn and RCn) to read out the memory contents to the storage latches.

Each character read from the refresh memory is stored for presentation to the ROM character memory (and to data transmitter logic for read-back test operation).

The ROM character generation decodes the stored USASCII-coded character and produces a five-bit output specifying dots to be displayed for each dot row. That is, the character is presented to the ROMs for each dot row as the character row is generated. The count CCn selects the dot pattern for each dot row.

4.2.3 Monitor Video and Drive Circuits

The 5-bit dot row data read from the ROM character generator is presented to the monitor video circuits as a serial data stream, continuous except during CRT retrace periods. Character position and row counts are used to generate CRT sweep drive signals, with horizontal drive triggered by the start of each dot row, and vertical drive triggered when the character row count reaches 12 (standard) or 24 (optional).

4.2.4 Receiving and Storing Data

Data transmission rates are selected in the ADM-3 to match those devices on the other end of the line. Baud rates are derived from the LSB of the dot count, DC1. The receive clock and the transmit clock may be the same or different rates (split baud rate option).

Received data is clocked into the refresh memory, which is addressed by memory address logic. The memory address, during loading, is

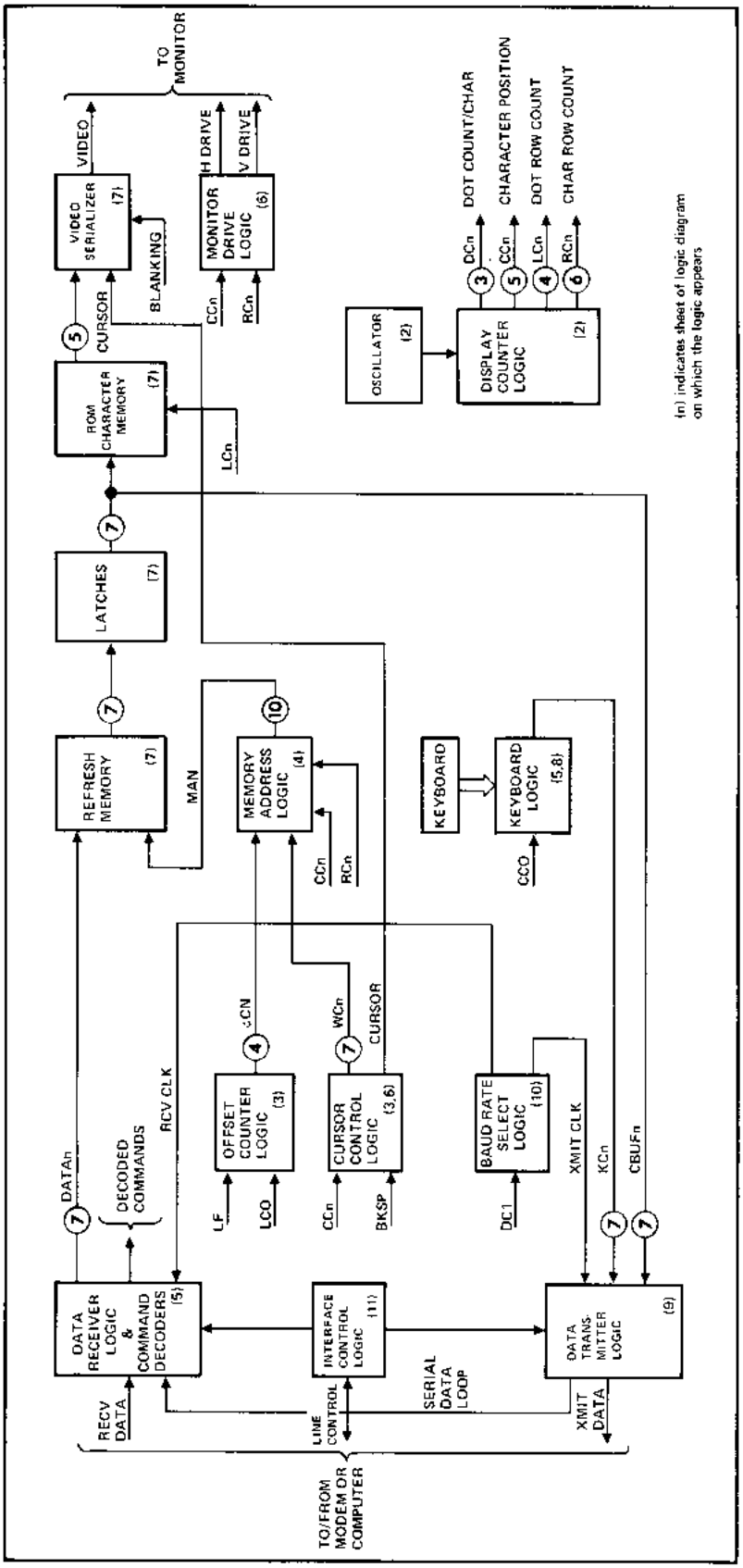


Figure 4-1. ADM-3 Interactive Display Terminal, Functional Block Diagram

formed by summing the character row count with an offset address (OCn) incremented by each input Line Feed command. This summation is necessary because data is not actually moved in the refresh memory. In effect, OCn is a virtual address pointing to the last character row on the screen.

Received commands are decoded and used to control ADM-3 logic. Commands include Line Feed, Backspace, Carriage Return, and other functions.

4.2.5 Cursor Generation

The cursor marks the position in the bottom character row in which the next character will appear. Data is always entered in the bottom row: Line Feed causes the display to roll upward. The cursor is formed by displaying five dots in the eighth and ninth dot rows of the character position in which it rests. Cursor information is ORed into video output logic along with character bits read from the ROMs.

The cursor may be moved either forward or backward one character position in response to a received BKSP command.

The cursor position code WCn is used to address the refresh memory in read-back test operation.

4.2.6 Keyboard Logic

The keyboard and associated logic are used to compose data for display and simultaneous transmission. As a character is typed by the operator, it appears (as KCn) at data transmitter logic, and (in half-duplex transmission) is loaded into the refresh memory for display. In full-duplex, communications characters originating at the keyboard appear on the display only if they are echoed back from the computer or modem.

4.2.7 Data Transmitter Logic

Data transmitter logic receives characters generated at the keyboard (or generated at optional answerback logic and put on KCn lines) and converts the seven-bit character into serial-bit form along with start, parity, and stop bits, and sends the formatted data word to the modem or computer.

In read-back test operation, the contents of the memory buffer (CBUFn) may be accepted for

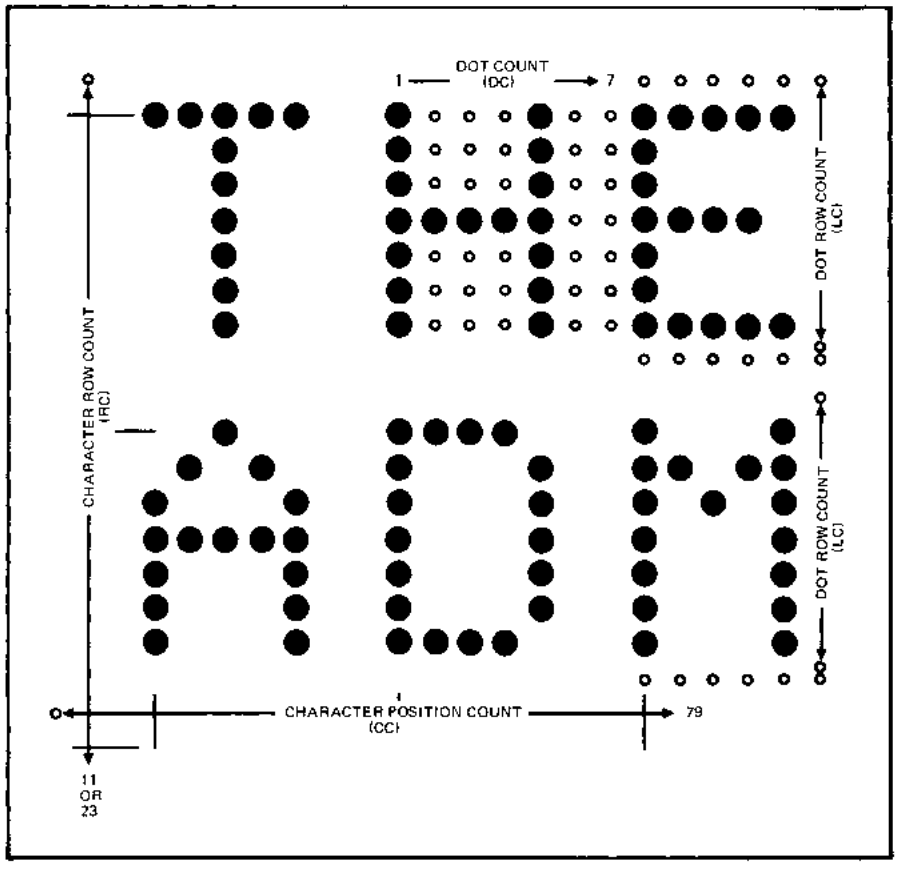


Figure 4-2. CRT Display Matrix

transmission in the same manner as data on the KCn lines.

4.2.8 Interface Control Logic

This logic controls Clear-to-Send and Request-to-Send exchanges between modem or computer and the ADM-3. Either a code-turnaround or a reverse-channel system may be used to transfer control from one end of the communication line to the other.

Switches adapt the logic to interface with the common type 103 or 202 modems, or to operate under internal control.

4.2.9 CRT Display Monitor

The CRT display monitor employed in the ADM-3 is a solid-state unit for use in industrial and commercial installations where reliability and high-quality video reproduction are desired.

The monitor features printed circuit board construction for reliability and uniformity. All circuits of the TV monitor are transistorized.

4.3 LOGIC DESCRIPTION

The following paragraphs describe the operation of logic represented by each block in the overall block diagram, figure 4-1, as well as logic and circuits performing functions not indicated in figure 4-1. Refer to block and timing diagrams that accompany the text, as well as to the logic diagram included in Section 6 in this manual.

4.3.1 General Clear Circuit

Circuits shown on sheet 6 of the logic diagram cause all control logic in the ADM-3 to be initialized when applied power causes the +V dc supply to rise.

As the supply voltage reaches the trigger level of a retriggerble one-shot, the one-shot creates the reset signal CLEAR, which is distributed to ADM-3 logic through six inverters. In circuit board testing, the signal TESTER INITIALIZE simulates the action of the one-shot.

4.3.2 Display Counters

The display counters provide a count of dot positions and dot rows, character position in a character line, and character rows. These counts define the position of each dot in a character matrix, and the position of each character in the total display. Figure 4-3 is a block diagram of this logic, and timing is shown in figure 4-4.

The basic clock is a 10.8864-MHz signal generated by a simple oscillator circuit. The clock frequency is twice the video frequency. The clock (CLK) drives the dot counter.

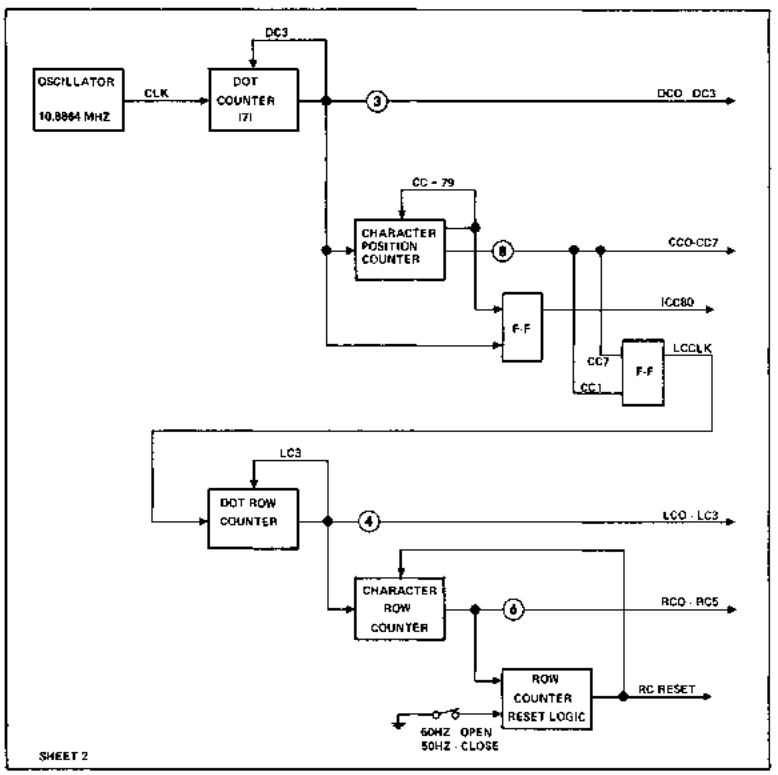


Figure 4-3. Display Counters, Block Diagram

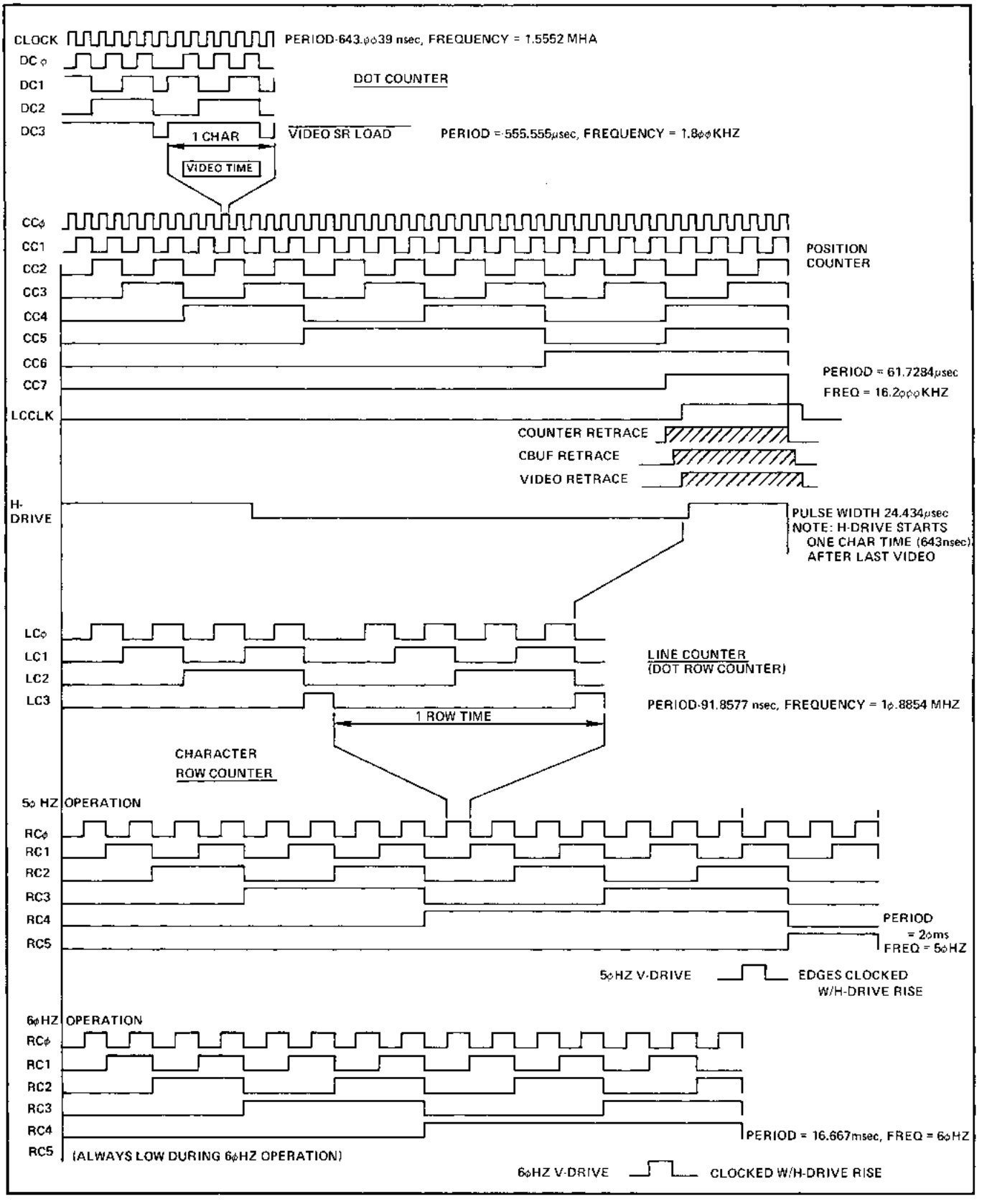


Figure 4-4. Display Counter Timing

The dot counter counts the seven dot columns comprising each character. The character is preset to 10 at the count of zero, counts through the overflow at 15, and is again preset at zero. Its final count, DC3, clock successive addresses to the character ROMs, and triggers the character position counter.

The eight-stage character position counter controls the position of each character on the 80-character raster line, and controls horizontal retrace time. The counter provides a total count of 96 (80 counts for character position, and 16 count for the retrace). The character position counter counts from zero to 79, presets to 240, counts through the overflow at 255, and then resets to zero. Outputs CC0 through CC6 are binary counts, but CC7 has a value of 80. That is, CC7 is low while 80 character positions are counted, and high during retrace time.

A flip-flop produces the signal ECC80 for the first count of retrace time. ICC80 indicates the time at which a command at the I/O interface may be acted upon. The output of the LCCLK flip-flop clocks the character line counter.

The character line counter counts the lines that form each row of characters. The counter counts nine. Counts 0 and 8 form spaces between characters, and dot rows are formed by counts 1 through 7. The last count, LC3, clocks the character row counter at a frequency of 1.8 KHz.

The character row counter counts the 24 character rows appearing vertically on the display, and counts through vertical retrace time (six counts for a 60-Hz power line, and 12 counts for a 50-Hz line). A switch sets up logic to produce RCRESET at the proper time, resetting the counter to zero to begin the next character row count.

4.3.3 Offset Counter Logic

When a character is stored in the RAM memory, it remains in the same cell even though line feeds cause data to "roll" upwards on the screen, and does not move until the character row in which it resides is itself "rolled" off the top of the screen. Consequently, to correctly address the memory a count of line feeds must be kept and used in forming the memory address. This is the purpose of the offset counter (figure 4-5).

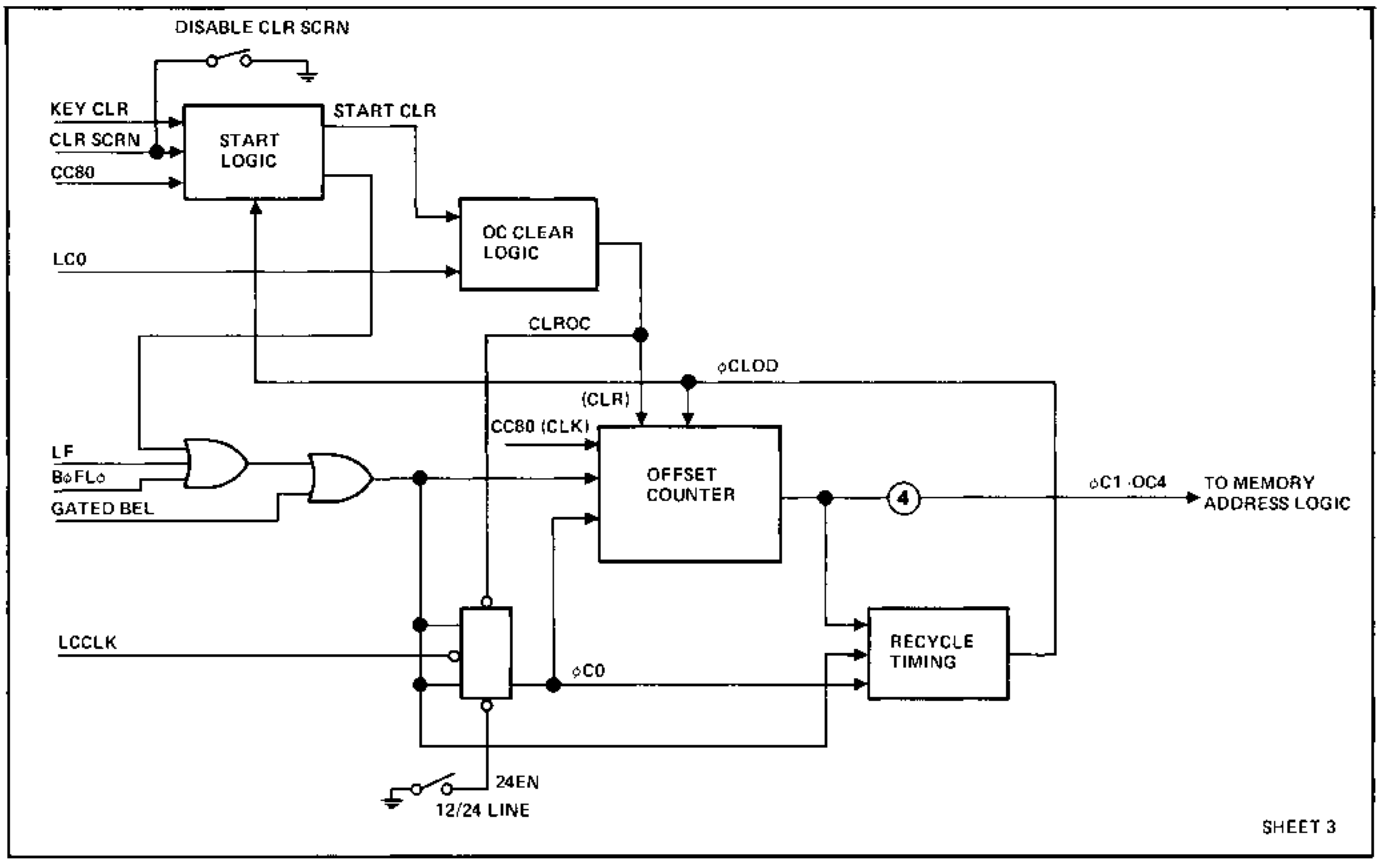


Figure 4-5. Offset Counter Logic, Block Diagram

When the 12/24 line switch is set for 24 lines, the offset counter counts from zero through 23 and returns to zero. Set for 12 lines, the counter counts only odd-numbered input pulses from zero through 23. Events that increment the counter are as follows:

a. A Line Feed (LF) code received at the I/O interface.

b. BOFLO, which occurs at cursor counter overflow when the AUTO NEW LINE switch is open.

c. START, which occurs with a received CLEAR SCREEN code or a Keyboard Clear input. START is cleared by the counter recycle signal OCLOD between counts 23 and zero.

The offset counter is cleared after START is set and WRITE PULSEs are then generated at the normal rate, 80 per character row. At the end of each row, the offset counter is incremented (once or twice, depending on the 12/24 LINE switch). Consequently, a 24-line display is cleared in about 1.5 msec. (Figure 4-6 shows timing of clear-screen operation.)

4.3.4 Cursor Control Logic

The cursor appears on the display as a double underline under the character to which it is addressed. As shown in figure 4-7, an up/down counter keeps track of the cursor position along a character row, either forespacing or backspacing.

In normal forespace operation, the counter is incremented by CC80 pulses gated by the following terms:

a. DOIT, which indicates that a new code has been put in the data input buffer and action is required.

b. DEL, to prevent the cursor from advancing for a Delete code.

c. CTRL CHAR, to prevent the cursor from advancing for a received control code.

The cursor counter can also be incremented during a Read Back operation (test only) by XLOAD. XLOAD falls when the code marked by the cursor had been loaded for transmission and the cursor may be advanced to the next character position.

The cursor counter is decremented one count each time a backspace command (BKSP) is received and decoded.

The cursor counter is cleared by any one of three events, as follows:

a. A Carriage Return (CR) command is received and decoded.

b. START is set by a master clear signal, a received CLR SCRN command, or a keyboard-initiated clear signal.

c. UNDERFLOW is set because a backspace was attempted from the "home" position on the left-hand side of the screen. The cursor does not do a reverse wrap-around operation but remains at "home". The cursor register is cleared to maintain the cursor's previous location.

If the cursor count has been incremented past the end of the character row, term WC=80 enables LCCLK to set OVERFLOW. OVERFLOW re-loads preset information into the counter. If the AUTO NL (Automatic New Line) switch is closed, OVERFLOW loads zero into the counter. Therefore, when a character is typed into the last location on the screen, the screen is rolled and the cursor is returned to "home".

When AUTO NL is open, OVERFLOW loads 79 into the counter and the screen does not roll. Further typing will overwrite the last position in the character row and the cursor will not move.

In the read-back test operation the contents of the counter (WC0-WC6) are compared with the dynamic character count (CC0-CC6) to cause the cursor to appear at the correct position on the character row. Because the display counters operate two character times earlier than the display, flip-flops delay the "equals" signal so that CURSOR rises coincidently with appearance of the character on the screen.

Terms RC1, RC3 and RC4 permit the cursor to be written in the character position only in the two lines under the character.

CURSOR is ORed into the monitor video line along with serialized character data.

4.3.5 Memory Address Logic

Logic that manipulates the refresh memory address is shown in figure 4-8. The 7-bit by 2K-word memory is addressed by the 10-bit binary code MA0-MA9.

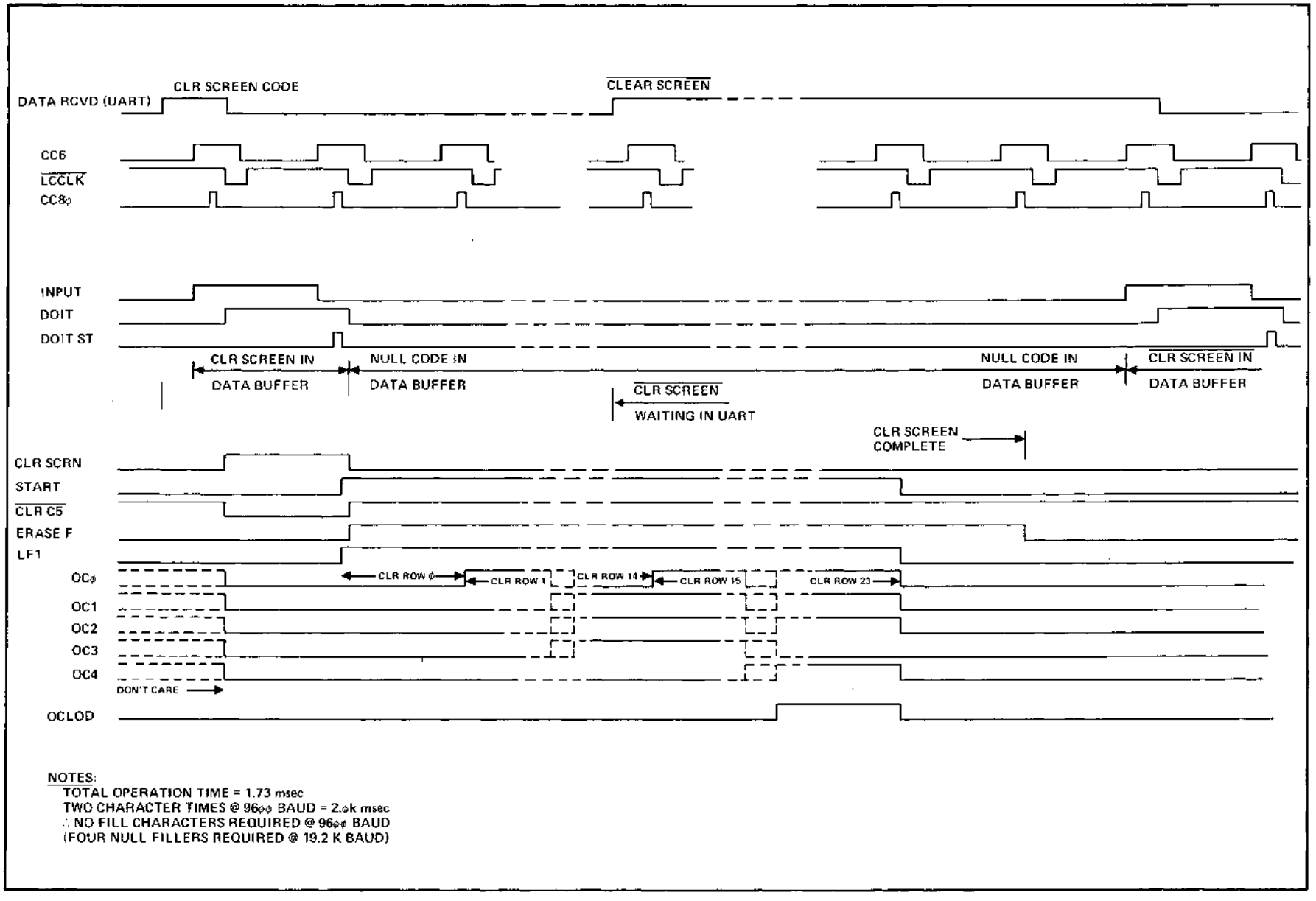


Figure 4-6. Clear Screen Timing

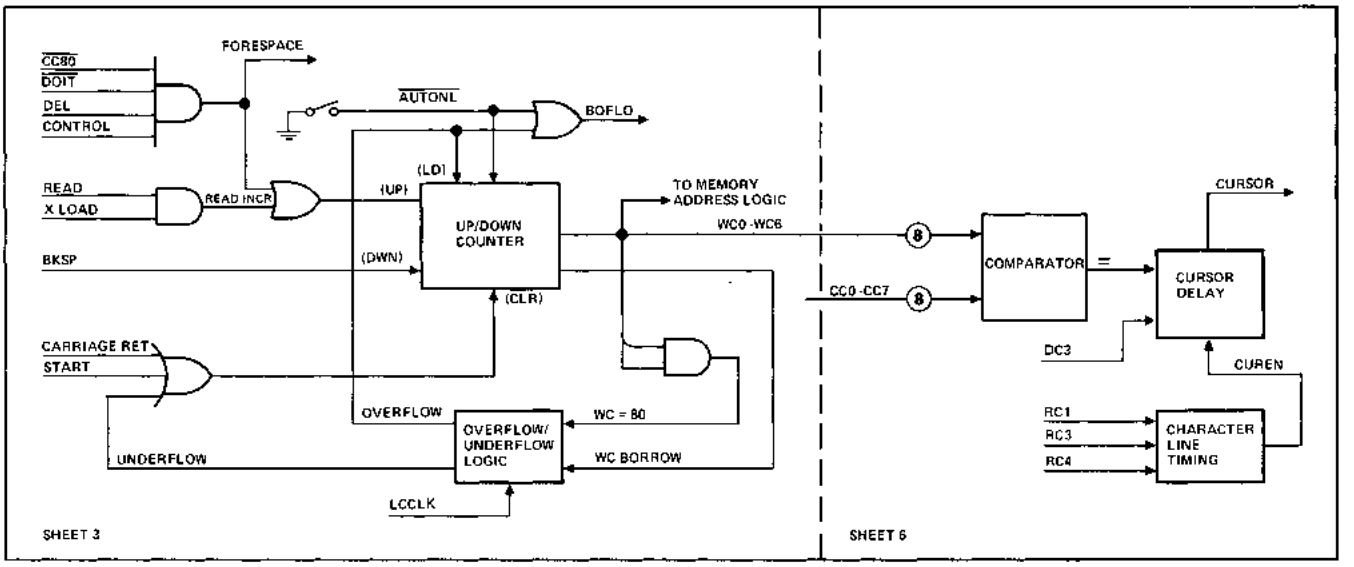


Figure 4-7. Cursor Control Logic, Block Diagram

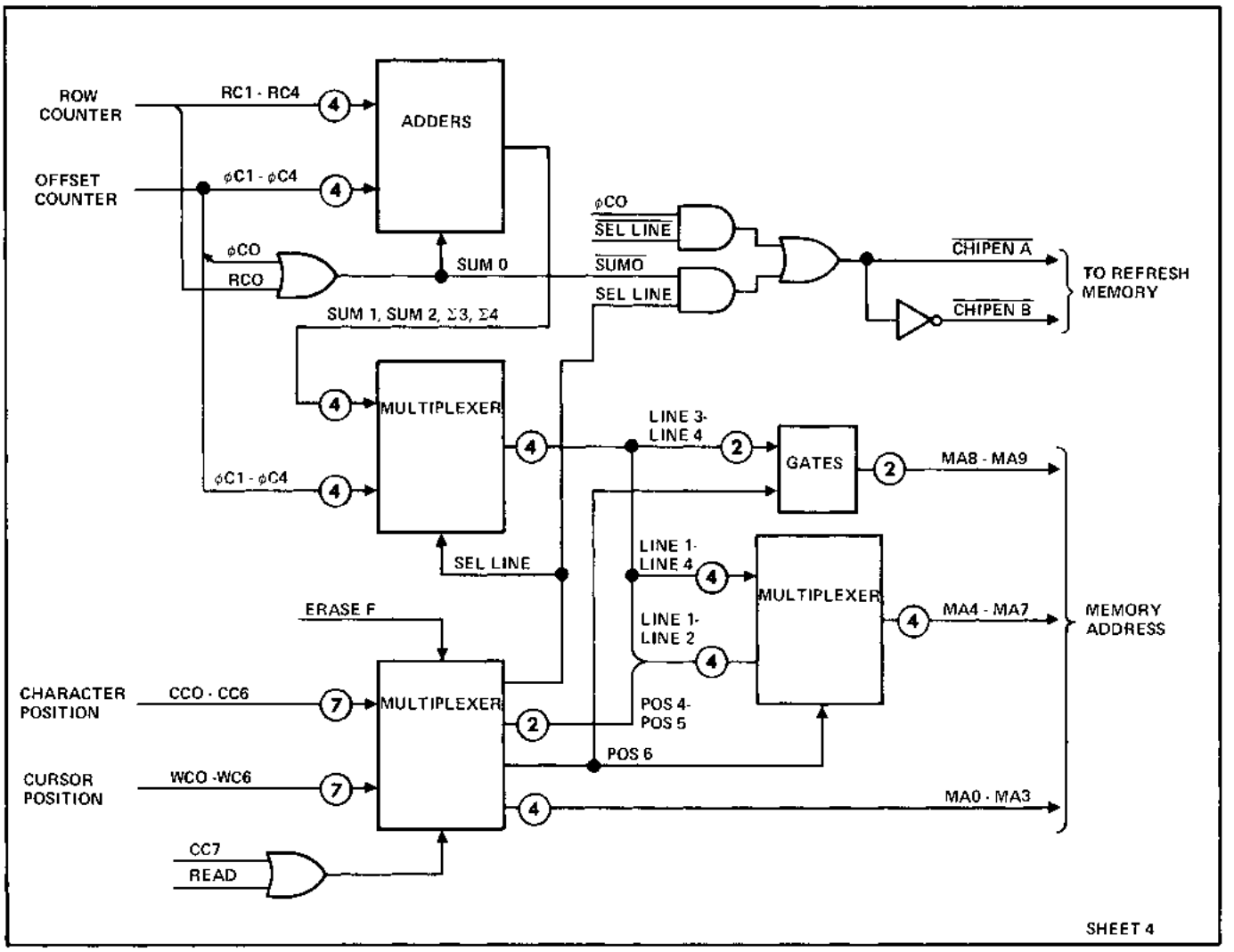


Figure 4-8. Memory Address Logic, Block Diagram

The inputs used to address the memory relate each memory cell to a single character position on the display screen. That is, character or cursor position codes (CCn or WCn) relate to the position on the 80-position character row, and row count and offset count codes (RCn and OCn) relate to any of up to 24 character rows.

The cursor position code WCn is selected to memory address lines in read-back test operation, and when data input buffers contain a character to be loaded into the refresh memory. Term CC7 is the horizontal border time during which any input operation occurs.

The character position code CCn is selected to MAn lines during screen refresh time to provide data to the ROM character memory. CCn is also selected when ERASEF causes a character row to be erased by SPACE codes.

When loading a character into the refresh memory, the character row is expressed by the contents of the offset counter OCn. The offset counter counts the number of line feeds that have been performed. The OCn is actually a virtual address pointing directly at the bottom line of the screen.

To create an address for video display, this logic sums the row count and the offset count as follows:

$$\text{Adder Out} = \text{OCn} + \text{RCn} + 1$$

The +1 is needed to roll the top row to the bottom. In the initialized ADM-3, the top row is Row 1. Therefore, incrementing the offset counter once from its initialized state changes the bottom row from Row 0 to Row 1, performing the "roll" operation in essentially zero time.

Adder logic provides the character row address in two steps. In summing OCn + RCn +1, a sum greater than 23 is illegal. A second summation converts the illegal address into a legal address to be multiplexed to logic that further manipulates it. Figure 4-9 shows the actual video display address obtained for any values of row count and offset count.

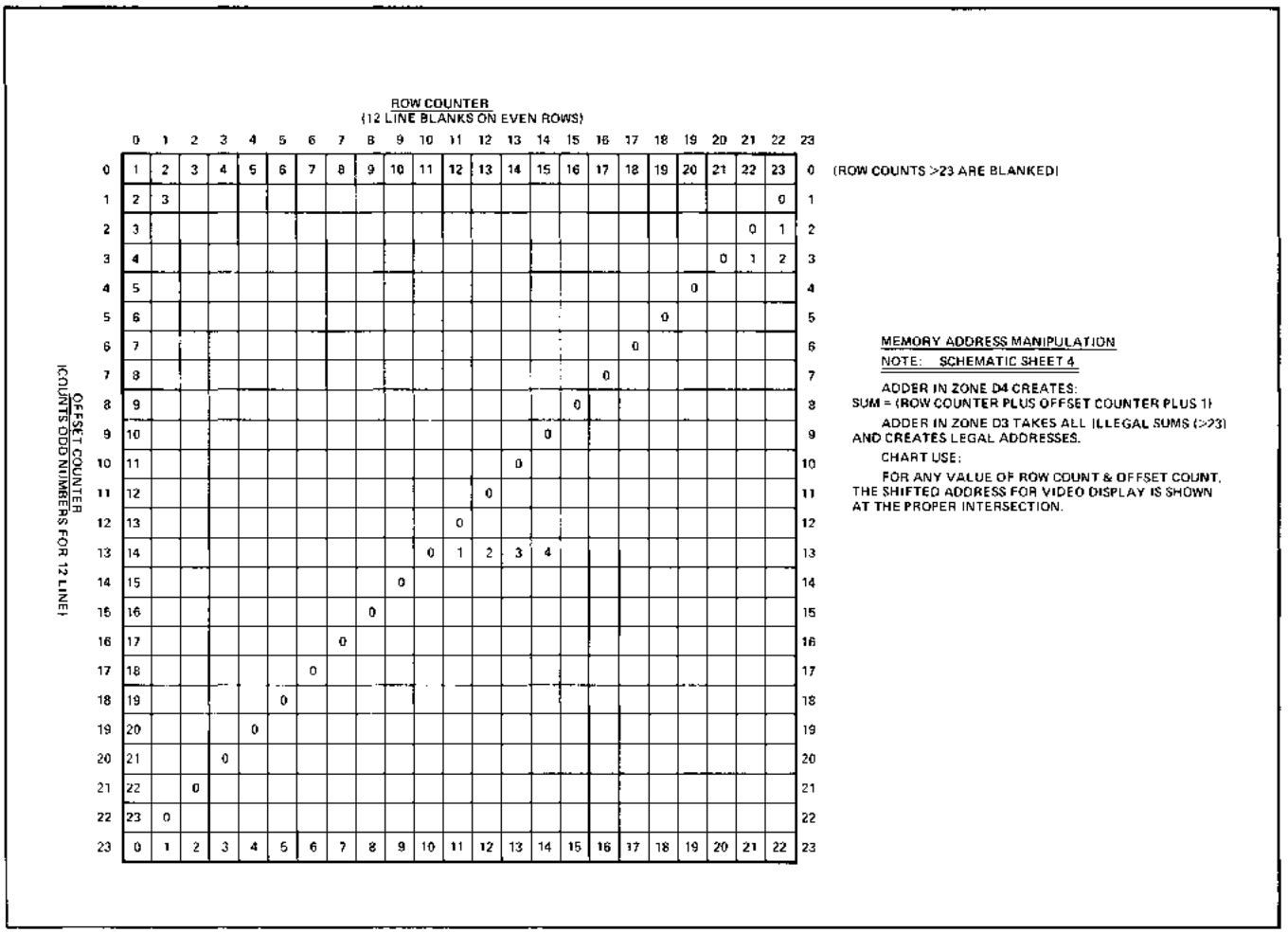


Figure 4-9. Manipulation of Display Address

The address must be further manipulated because the character row contains 80 positions – a non-binary number. If the character position and row address were used directly to address the memory, a much larger memory would be required. Another multiplexer and associated gates cause the memory to be addressed as if the display were made up of 30 rows, each comprising 64 characters. Figure 4-10 shows the organization of this display, and how the address is manipulated when the character position address is greater than 63.

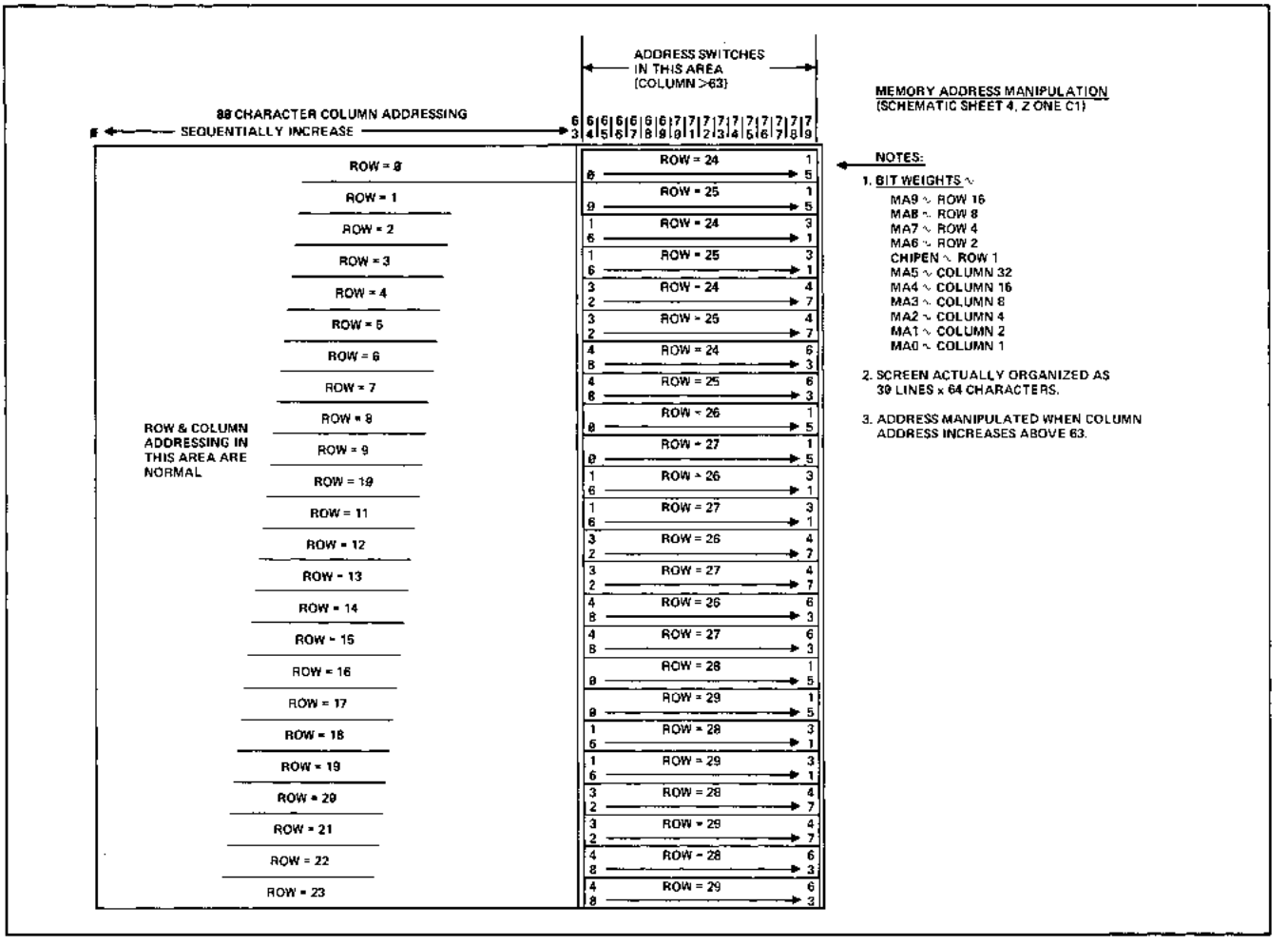


Figure 4-10. Organization of Display Data in Refresh Memory

Terms CHIPENA and CHIPENB turn on either half of the refresh memory. That is, CHIPENA turns on cells for the first 12 rows, and CHIPENB turns on cells for the last 12 rows of a 24-row display.

Note that, generally, the character position and row loading addresses (WCn and OCn) are not used simultaneously with refresh addresses CCn and SUMn. When the bottom line of screen is erased, however, the character row loading address OCn is used together with CCn (selected by ERASEF). This occurs during one raster scan in a "roll" operation and during multiple scans when the screen is cleared.

4.3.6 Refresh Memory and Character ROM Logic

Figure 4-11 shows logic comprising the refresh memory, buffer latches, and character memory ROMs.

The refresh memory is made up of 2K, 7-bit semiconductor RAM devices in one of four configurations as follows:

a. Six RAMs for upper-case only, 12-line display.

b. Seven RAMs for upper/lower-case, 12-line display.

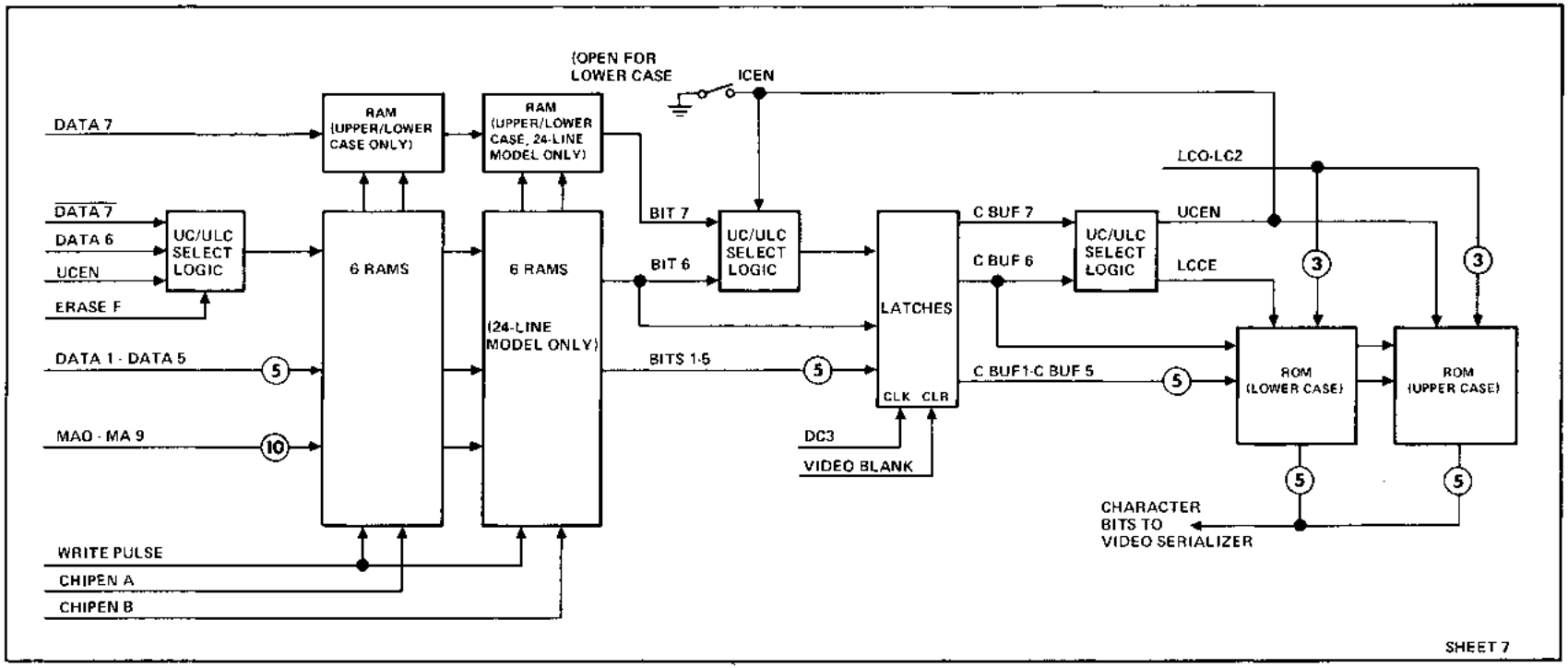


Figure 4-11. Refresh Memory and Character ROM Logic, Block Diagram

c. Twelve RAMs for upper-case only, 24-line display.

d. Fourteen RAMs for upper/lower-case, 24-line display.

A switch (UCEN) sets up the logic to operate with, or without, the lower-case RAMs. UCEN alters data to adapt the logic for either 6-bit codes (upper-case only) or 7-bit codes (upper/lower case). Term ERASEF causes the logic to force bit 6 high, creating a SPACE code in place of the received NULL code.

Data from the input buffer (DATA1-DATA7) is loaded into, or read from, the refresh memory by address lines MA0-MA9. The memory is clocked, for each character time, by WRITE PULSE.

CHIPENA is high as data is loaded into, or read from, RAMs storing the first 12 lines of display data. CHIPENB turns or RAMs storing the last 12 lines in a 24-line display.

At the end of each character period, DC3 clocks an addressed character into buffer latches which store the character to be encoded by the ROMs. The buffer latches are cleared by VIDEO BLANK. Because CBUF6 is normally inverted, however, a SPACE code, rather than NULL, is presented to the ROMs.

Two ROMs decode CBUFn characters and produce a 5-bit output code that provides the dot pattern for each line in the character matrix. Each of the seven lines in the character matrix is identified by the line count LC0-LC2. The parallel-bit information output by the ROMs is serialized for presentation to the video monitor.

One ROM contains upper-case characters, and the other contains lower-case characters. Select logic senses states of CBUF6 and CBUF7 to enable either ROM device.

CBUFn is available at data transmitter logic for transmission in read-back test operation.

4.3.7 Erase Logic

A display line is erased by logic shown on sheet 3 of the logic diagram. The ERASEF signal is turned on by LF1 which enables the offset counter. When the offset counter is incremented by Line Feed (LF) or BOFLO, START is low and ERASEF is turned off by LCCLK after a single character row has been erased.

When START has been raised by a CLEAR SCRN code, ERASEF remains high until START is turned off by the overflow of the offset counter. Consequently, the entire screen (12 or 24 lines) is erased.

4.3.8 WRITE PULSE Logic

The WRITE PULSE signal clocks the refresh (RAM) memory. Logic that generates WRITE PULSE is shown in sheet 3 of the logic diagram.

WRITE PULSE consists of gated pulses clocked by dot count DC2, and is normally gated on by FORESPACE (the input of the cursor counter) or ERASEF.

The non-destructive space code feature allows writing a SPACE code (040_8) into the RAM memory any time between a Line Feed (LF) code and a Carriage Return (CR) code, with writing of SPACE inhibited between the CR code and the next LF code. This permits the computer or operator to write a display on the screen, issue a CR code, and space over the previously written data, with the cursor, without writing over the data.

The NO WRITE signal inhibits FORESPACE so that WRITE PULSE is not generated during that period. A switch permits inhibiting the non-destructive space code feature.

4.3.9 Keyboard Logic

Keyboard logic is shown on sheet 8 of the logic diagram (except for lock/unlock logic shown on sheet 5). Timing of keyboard logic functions is shown in figure 4-12.

The keyboard is encoded by generating the complete sequence of 7-bit USASCII codes at high speed, and trapping the code that matches a depressed key. The codes are generated continually and repetitively unless a key is pressed. The code sequence is clocked at a counter by KBCLK, which is the gated character rate signal CC0.

The four least-significant bits of the count (KC1-KC4) encode the 16 rows of the USASCII code chart. The three remaining bits (KC5-KC7) encode the eight columns of the chart.

When no key is depressed, KEY DATA is high and KBCLK cycles the counter, and bounce

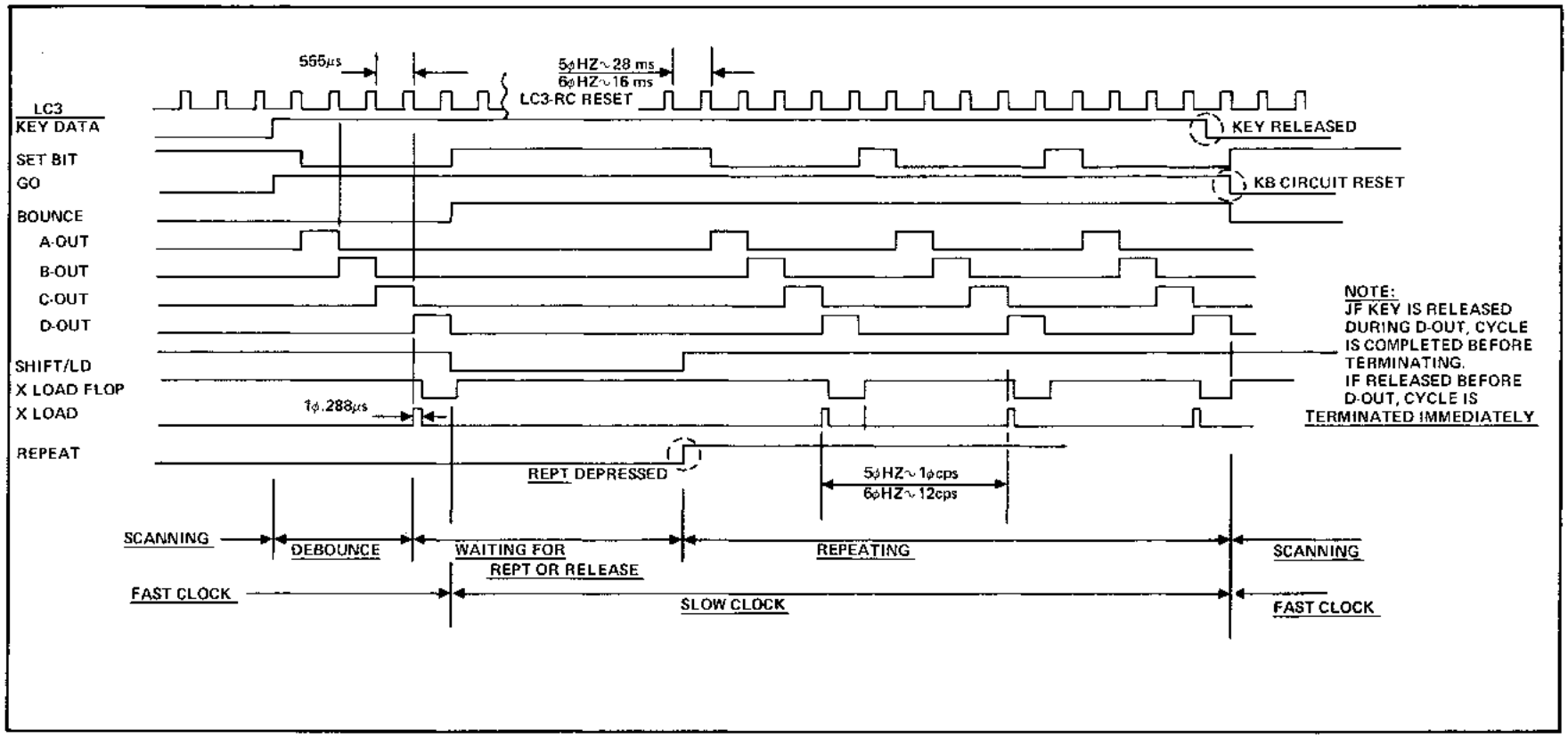


Figure 4-12. Keyboard Logic Timing

logic holds BOUNCE high. When a key is depressed and then the corresponding code appears on lines KC1-KC7, KEY DATA' falls, preventing generation of further KBCLK pulses so that the code is held on KCn lines. KEY DATA also causes GO to rise, causing bounce logic to count 1.8-KHz LC3 pulses until a fifth pulse has completed a 2.78-msec delay period.

At the end of the key-bounce delay period, BOUNCE becomes true, inhibiting further counts of LC3. If the key is released, KEY DATA immediately rises and counter cycling resumes. If the key is held down, along with the REPT (Repeat) key, however, the high BOUNCE signal permits RCRESET pulses (at the ac power line frequency) to clock the bounce delay period, generating the GO signal at a rate of 12.5 characters per second at 60-Hz, or 10 characters per second at a 50-Hz line rate. Consequently, the character is repeated at that rate until either key is released.

The term THRE limits the repeat rate if the period of the selected baud rate creates a character time longer than the repeat cycle.

When the CTRL (control) key is pressed, bits KC6A and KC7A are forced to zero, forcing any generated code into column 0 or 1 of the USASCII code chart. Bit KC5A selects either column 0 (when false) or column 1 (when true). For example, when the "2" key is pressed (0110010) along with CTRL, the effective code becomes control code DC2 (0010010).

With either SHIFT key depressed, bit 6 (KC6A) is inverted to select upper-case alpha characters (USASCII column 4 or 5, instead of column 6 or 7). Also, INVERT 5 selects codes in USASCII column 2 instead of column 3, to encode the "upper-case" symbols on numeral and symbol keys. Terms COL2 and COL3 identify those codes in the shift logic. Row 0 codes in columns 2 and 3 (SP and 0) are excluded from this action because they have no "upper case" functions.

The UPPER CASE key is used in units that do not include the lower-case alpha characters. When the key is depressed, use of the SHIFT key has no effect on alpha keys. Lower-case alpha codes are encoded in USASCII columns 6 and 7. Therefore, the gated term KC6 KC7 causes INVERT6 to maintain upper-case codes without use of the SHIFT key. Other codes in columns 4 through 7 are identified by KC7 SHIFT EN which permits normal shifting up and down.

The BREAK key is depressed to signal the computer that the operator wishes to terminate data transfer. The Break function is maintained for as long as the key is held down. The signal BREAK appears at interface control logic where it forces the primary data transmit line to the "space" state if the unit is transmitting, or forces the secondary transmit line to the "mark" state if data is being received and the interface is in the secondary-channel mode of operation.

When the CLEAR key is pressed, and the SHIFT key is also depressed (SHIFT EN), KEY CLR clears keyboard lock logic, the refresh memory, and interface control logic.

The HERE IS key activates an optional Answer Back function which causes a unique, fixed message to be sent to the computer. The message, up to 32 characters long, is contained in a PROM device. Either the level from the HERE IS key, or an ENQ command received from the computer, causes the IDENT signal to activate logic on the Answer Back board.

Keyboard lock logic (sheet 5) permits the computer to enable or disable the keyboard logic. The KBLOCK signal is set-enabled locally by KEY CLR, or by the decoded UNLOCK command, and reset-enabled by the decoded LOCK command. Keyboard lock logic by CC80. KBLOCK prevents DOIT from generating GO, inhibiting any keyboard action. A switch permits holding KBLOCK true regardless of received LOCK commands.

4.3.10 Beeper Logic

Beeper logic produces an audible signal as a near-end warning. The signal that drives the speaker (sheet 3 of the logic diagram) is the character row rate LC2, which has a rate of 1.8 KHz.

The rate LC2 is enabled to the speaker during the "on" period of a one-shot circuit. The one-shot is triggered on by WRITE CHAR as the 71st character is written in any line (WC0 WC1 WC2 WC3 WC6). The one-shot is triggered when a BEL code is received at the I/O interface.

Because a read-back operation is initiated by a BEL code, the term READ is used to disable the one-shot so that the BEL code cannot cause the audible signal.

The OVERFLOW signal is used to turn-off the one-shot when a baud rate higher than 2400 baud is used. Because the period of the one-shot is greater than the period between successive 71st characters in this case, the beeper would otherwise remain energized continuously while data is being received.

4.3.11 Data Receiver and Command Decoder Logic

This logic (figure 4-13) receives data from the computer through either a standard RS232 interface, or a current loop interface. Serial data is received through the RS232 interface by an RS232 receiver which sends the data to an OR circuit which also receives data from the current loop receiver.

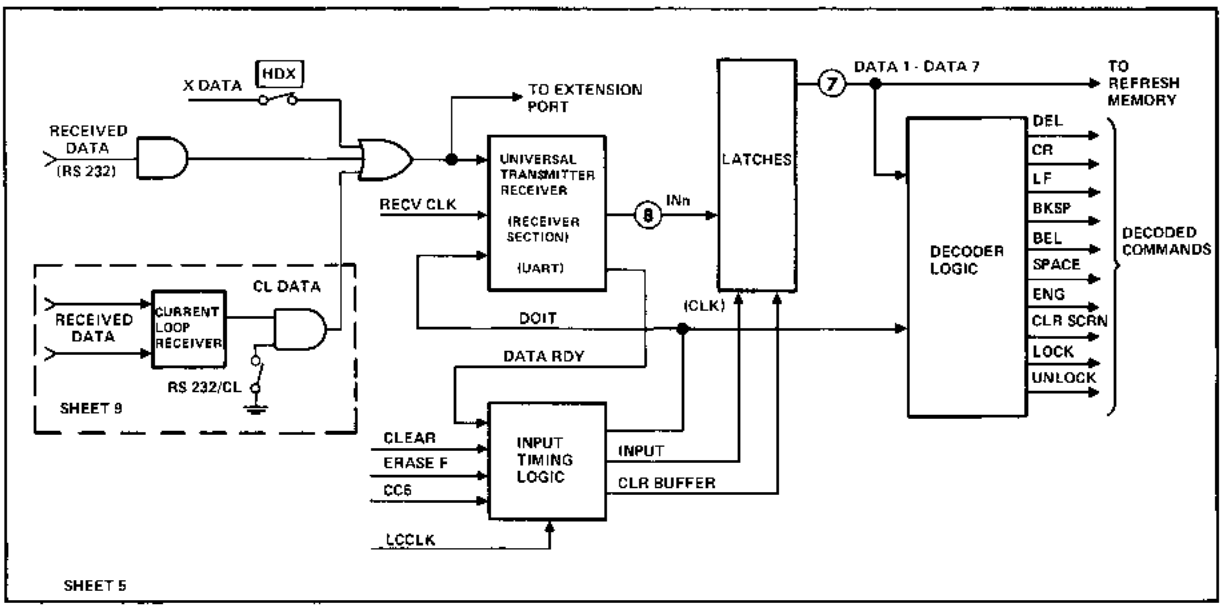


Figure 4-13. Data REceiver Logic and Command Decoders

The current loop receiver is a bipolar circuit and responds to current in either direction. The receiver comprises a rectifier/limiter which drives an optical coupler, and a single-transistor amplifier driven by the optical coupler. If the RS232/CL switch is open, the amplifier output appears at the OR logic that furnishes the UART input.

A third input to the OR logic is data being transmitted from the ADM-3 (XDATA) and appears if the HDX (half duplex) switch is closed.

The received serial data, from whatever source, is clocked into the UART by RECV CLK (at the selected baud rate). In the UART, each received character is stored and presented in parallel-bit form to latches, with the most-significant bit appearing on the IN7 line. (IN8 is not used in the ADM-3.)

The character stored in the UART is clocked into latches by INPUT as DATA RDY is output by the UART (unless ERASEF inhibits INPUT). INPUT rises when CC6 occurs at the end of every horizontal scan. Then LCCLK turns on DOIT, which remains on for the next full horizontal scan period during which the last received command is executed.

The data character stored in the latches is decoded to obtain the different control command signals. The three least-significant bits are used as chip-enable codes and are made effective by DOIT. Consequently, control commands are not effective until execution time.

4.3.12 Data Transmitter Logic

Data transmitter logic is shown in figure 4-14. Data that may be applied to the transmitter section of the UART are:

a. Keyboard characters KCn, and the XLOAD signal from keyboard logic, when READ is false (normal operation).

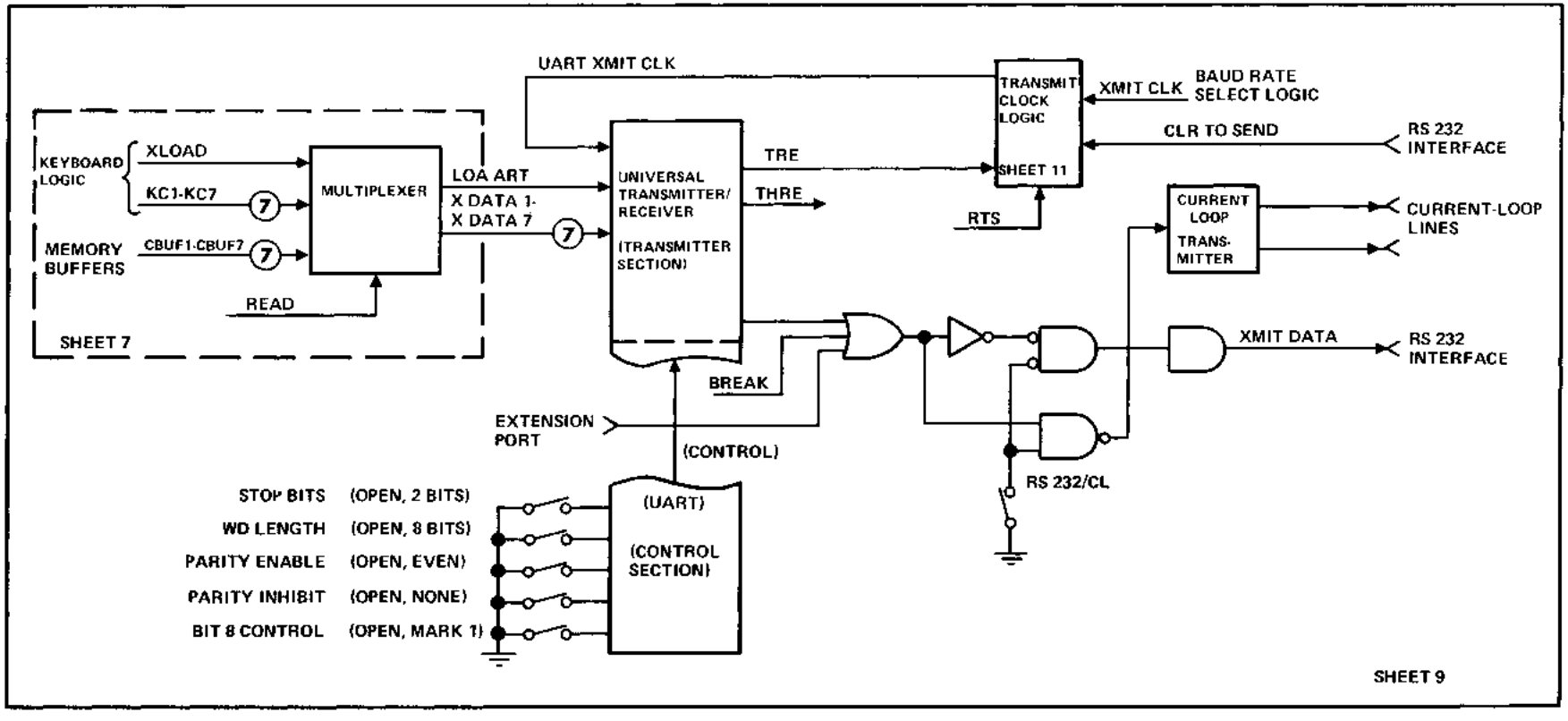


Figure 4-14. Data Transmitter Logic, Block Diagram

b. Characters of the answer-back message, applied through KCn lines, when the answer-back option is included in the ADM-3, and READ is false.

c. The contents of the refresh memory buffer (CBUFn) when READ is true (in read-back test operation).

The UART XMIT CLK that clocks the UART is the gated XMIT CLK selected at baud rate select logic and is 16 times the baud rate. The UART is loaded from XDATAn lines by LOA ART, which is normally high.

The UART XMIT CLK is enabled when CLR TO SEND appears at the interface, and further controlled by TRE. TRE and THRE are output by the UART. THRE falls when XDATA loads the holding register in the UART. If the serializer (which is loaded from the holding register) is empty, TRE is high. With the holding register full and the serializer empty, the UART automatically transfers the character into the serializer. At this time THRE rises, ready to accept the next character, and TRE falls to indicate that the serializer is busy. Both THRE and TRE are high when the UART holds no data.

Transmit clock logic is reset by the next Request to Send (RTS) signal from the interface.

Five switches permit formatting the transmitted character. First transmitted is always the Start bit, followed by the seven data bits (LBS first). The parity bit, odd or even, then follows (if enabled); followed by one or two Stop bits.

The serial bit stream is ORed to transmitter circuits through a gate which also receives data which may appear (from another device) at an extension port. If the BREAK key is depressed, the XMIT DATA line is forced to the high (SPACE) level.

Data is sent through either the RS232 or current loop interface, depending on the position of the RS232/CL switch. The unselected interface maintains a marking level. The RS232 interface comprises a simple driver. The current loop interface uses an optical coupler to couple the TTL data to an amplifier, and then through a diode output network to the current loop.

The optical coupler completely isolates the current loop transmitter rom the ADM-3. One leg of the current loop may be tied through a register to +12V dc to create a current source. As an alternative, a ground strap may be used instead of the resistor, to act as a sink for an external positive source, or a current source for an external negative voltage.

4.3.13 Video Blanking and Serializer Logic

Logic that controls blanking during horizontal and vertical retrace time, and converts the parallel-bit ROM outputs to a serial bit stream, is shown in figure 4-15.

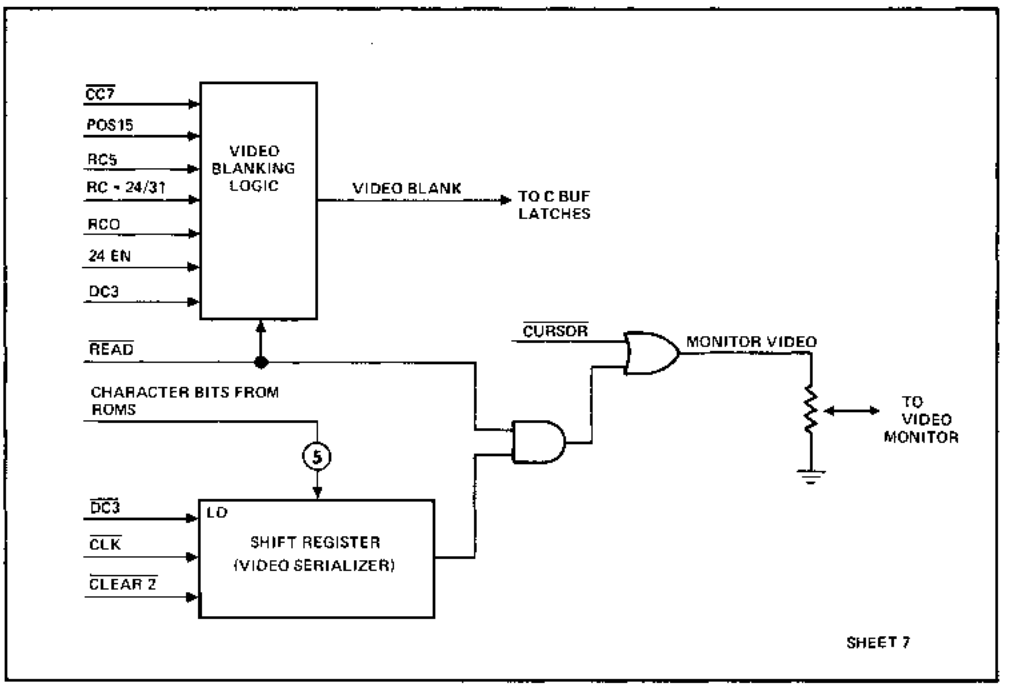


Figure 4-15. Video Blanking and Serializer Logic, Block Diagram

Terms CC7, POS15, and RC5 control blanking for row counts of 32 and higher, and are effective only when the ADM-3 is operating at a vertical rate of 50-Hz (the count reaches only 29 in 60-Hz operation). For counts below 32, term RC=24/31 controls blanking.

Terms RC0 and 24EN cause all even-numbered character rows to be blanked if the ADM-3 is operating with a 12-line display.

In every case, VIDEO BLANK is clocked to the memory buffer latches by BDC3 as the current character is completed. VIDEO BLANK clears the buffer latches but, because bit 6 is normally inverted, the USASCII SPACE code is presented to the ROMs, instead of NULL.

During a read-back test operation, READ blanks the video but permits sending CBUFn data to transmitter logic.

The video serializer is an 8-bit shift register. Term DC3 loads it with the ROM output character bits every 643 nsec, and the bits are shifted (by CLK) at a rate of 10.8864 MHz. The shift register output is ORed with cursor information to produce the MONITOR VIDEO signal. The video level adjustment potentiometer is located at these circuits.

4.3.14 Monitor Drive Logic

This logic (shown on sheet 6 of the logic diagram) generates signals that trigger horizontal and vertical drive cycles in the monitor. To obtain the horizontal drive signal HDRIVE, character position counts are decoded to set HDRIVE false at the start of a row. HDRIVE is set true one count after the rise of CC7 to start the video retrace period.

The vertical drive cycle is begun by VDRIVE. This signal is generated by decoding character row counts RCn, and setting the VDRIVE flip-flop one count after the last character of the last line has been written. The flip-flop is clocked by the HDRIVE signal for the line just completed.

The level 60EN controls timing for 50-Hz or 60-Hz power lines. Refer to figure 4-4 for timing diagrams.

4.3.15 Baud Rate Select Logic

Figure 4-16 diagrams logic used to generate and select baud rates for data transmission and reception.

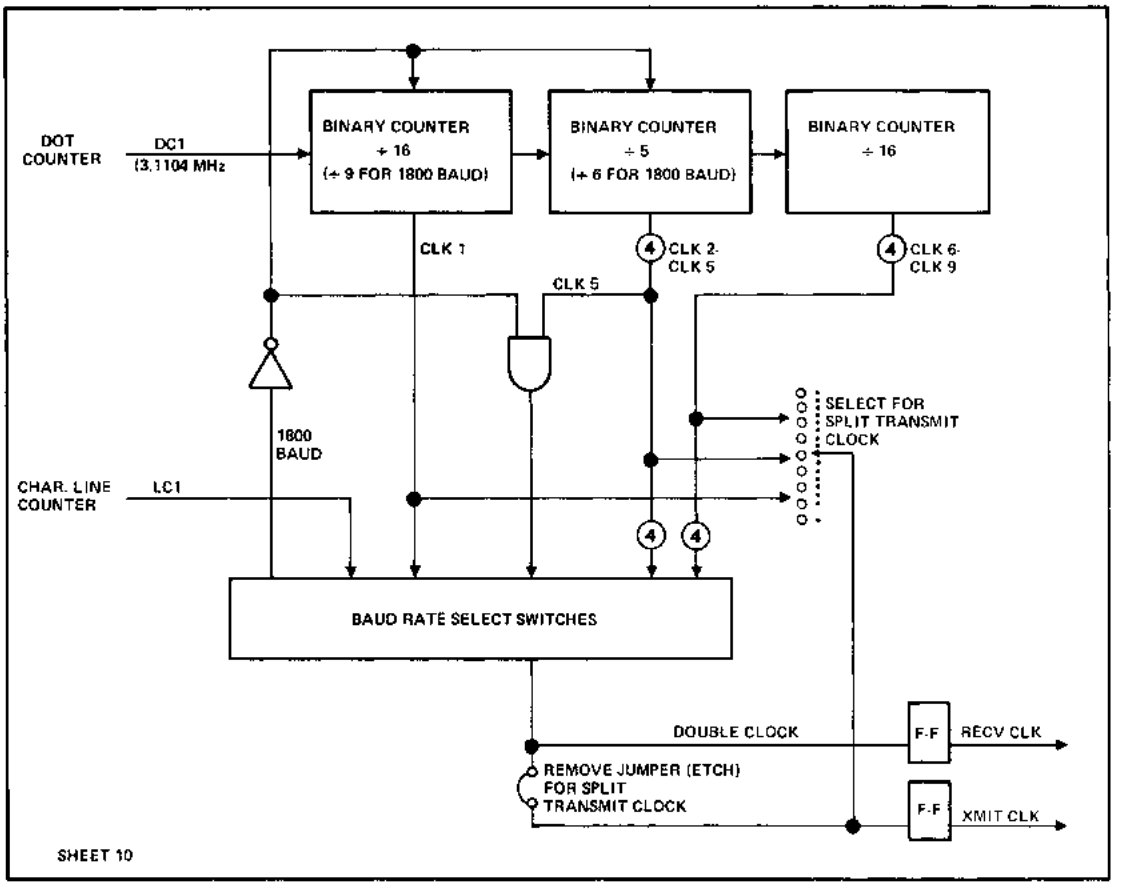


Figure 4-16. Baud Rate Select Logic, Block Diagram

The basic clock used in this logic is the 3.1104-MHz pulse stream DC1, which is from the display dot counter. Except when an 1800-baud rate is selected, the three binary counters divide pulse rates by 5, 16, and 16 respectively; for 1800 baud, 6, 9, and 16, respectively.

The various rates, from 75 to 19,200 baud except for 110 baud) are obtained from the counters, and one is selected by means of a BAUD RATE switch. The 110-baud rate is obtained directly from the character line counter term LC1.

When BAUD RATE switch 1800 is on, the first two counters are set up to divide by 6 and 9, respectively, and CLK5 is selected as the double clock.

The double clock rate is divided by flip-flops to provide the RECV CLK and XMIT CLOCK signals. Normally, both flip-flops are clocked by the same rate. However, when a split clock is required, the XMIT CLOCK may be derived from another rate selected by means of a rotary switch located inside the ADM-3 case.

When the common clock is used, the rotary switch must be in position 12.

When a split clock is used, the printed circuit joining clock inputs of both flip-flops must be cut. Note that if 1800 baud is selected with front panel switches, the only useful rate available for XMIT CLOCK is 110 baud.

4.3.16 Interface Control Logic

Interface control logic appears on sheet 11 of the logic diagrams. This controls request-to-send and clear-to-send communications for the ADM-3.

CLR TO SEND (high) permits data transmission logic to produce UART XMIT CLK, sending data from the ADM-3. If CLR TO SEND falls while a byte is being transmitted, TRE maintains the transmit clock until the byte has been completed, and then falls to shut off the clock and return the line to the marking state.

REQ TO SEND (RTS) may be controlled in any of four ways, as follows:

a. RTS may originate at an extension port.

b. If switches 202, 103, and LOCAL are all open RTS remains low all the time.

c. If only switch 103 is closed, RTS remains high all the time.

d If only the LOCAL switch is closed, signals THRE and TRE control RTS. RTS rises to transmit each character, and falls when the character has been shifted out of the ADM-3.

e. If only the 202 switch is closed, RTS may be controlled through the ADM-3 interface in either code-turnaround, or reverse-channel operation.

4.3.16.1 Code-Turnaround Control. Either an ETX code or an EOT code may be selected to initiate turnaround, depending on the position of the ETX-EOT switch. When the selected code appears in the input data, LATCHED CODE is set. When CARRIER DETECT falls (figure 4-17), indicating that the remote end of the line has dropped, RTS is set.

RTS is reset when ETX' or EOT is again decoded, and the logic switches to the receive mode. Following a turnaround command, no further command will be recognized for approximately 250 msec. This interval gives the modem time to propagate its signals. The interval is timed-out by two flip-flops and a counter, and the signal SBEN controls resetting of RTS.

4.3.16.2 Reverse-Channel Control. In reverse-channel operation RTS is controlled by SEC RECV DATA (SB) and CARRIER DETECT (CF) from the modem. When SB goes low, RTS is unconditionally reset (figure 4-18), switching the interface to receive data. In normal reverse-channel receive operation, CF is high at this time, causing SEC XMIT DATA to rise.

When the remote end of the line raises SB, and then drops its RTS (and CF), the ADM-3 turns on its RTS. The ADM-3 will then ignore further commands for a 250-msec period while the modem propagates its signals.

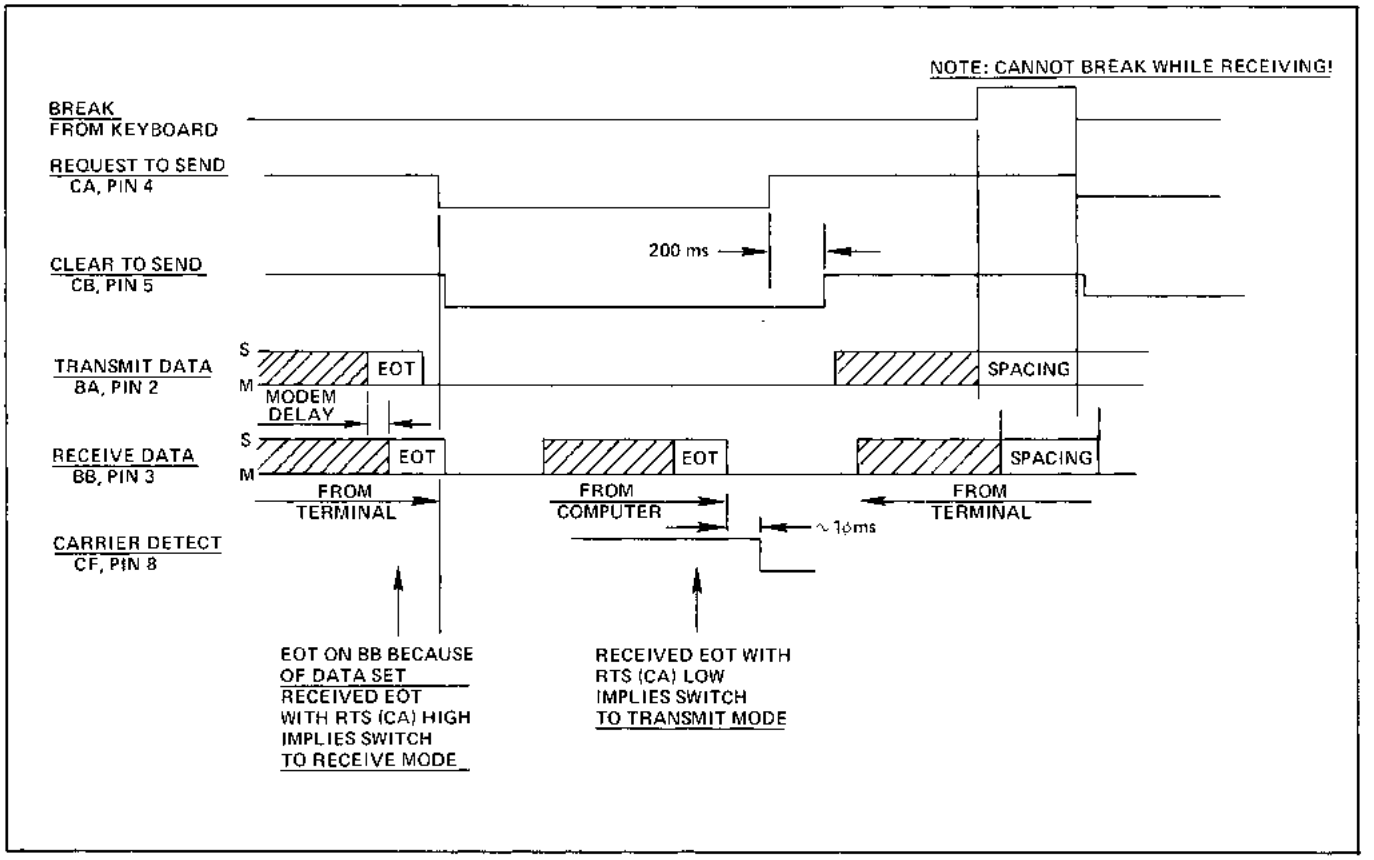


Figure 4-17. Interface Timing for Code Turnaround

4.3.17 Power Supplies

AC power is applied to the transformer through the ON/OFF switch on the rear of the ADM-3. The different stepped-down ac voltages connect to the main circuit board through connectors J3 and J4.

Rectifiers, filter capacitors, and voltage regulators are all located on the main circuit board. Four type 7805 devices provide the +5V dc logic supply, and two type 7812 devices furnish +12V dc to operate memory devices.

A +15V dc supply required by the monitor is made up of a type 7812 device and a simple transistor shunt regulator. The output voltage is adjustable.

4.3.18 CRT Display Monitor Logic

VIDEO AMPLIFIER

The video amplifier consists of Q101 and its associated circuitry.

The incoming video signal is applied to the monitor through the contrast control through R109 to the base of transistor Q101.

Transistor Q101 and its components comprise the video output driver with a gain of about 17 Q101, operating as a class B amplifier, remains cut off until a DC-coupled, positive-going signal arrives at its base and turns on the transistor. R111 adds series feedback which makes the terminal-to-terminal voltage gain relatively independent of transistor variations as well as stabilizes the device against voltage and current changes caused by ambient temperature variations.

The negative going signal at the collector of Q101 is DC-coupled to the cathode of the CRT. The class B biasing of the video driver allows a larger video output signal to modulate the CRT's cathode and results in a maximum available contrast ratio.

The overall brightness at the screen of the CRT is determined by the negative potential at the grid and is varied by the brightness control.

VERTICAL DEFLECTION

Transistor Q102 is a programmable unijunction transistor, and together with its external circuitry, forms a relaxation oscillator operating at the vertical rate. Resistor R115, variable

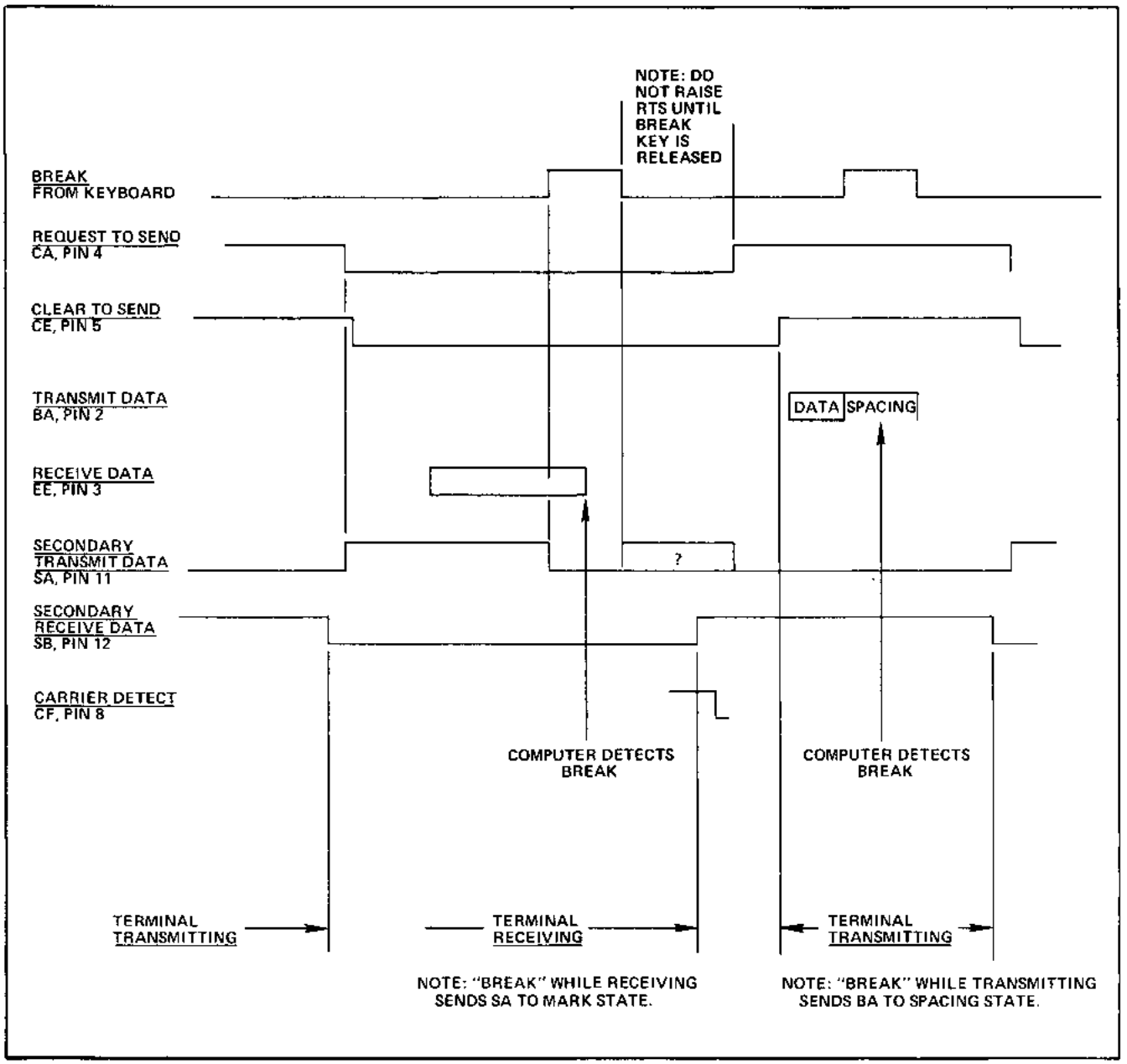


Figure 4-18. Interface Timing for Reverse-Channel Operation

resistor R116 and Capacitors C105 and C106 form an RC network providing proper timing.

When power is applied, C105 and C106 charge exponentially through R115 and R116 until the voltage at the junction of R116 and C105 equals the anode "A" firing voltage. At this time, one of the unijunction's diodes that is connected between the anode and anode gage "G" becomes forward biased allowing the capacitors to discharge through another diode junction between the anode gate and the cathode "K" and on through R120.

R117 and R118 control the voltage at which the diode (anode-to-anode gate) becomes forward

biased. This feature "programs" the firing of Q102 and prevents the unijunction from controlling this parameter. Therefore, the changing of firing points from one device to another, together with the temperature dependency of this parameter, is no longer a problem as it can be with conventional transistors.

The vertical oscillator is synchronized externally to the vertical interval from the vertical drive pulse at R113. At the time of the vertical interval, an external negative pulse is applied through R113, C104, and CR101 to the gate of Q102, causing the firing level of the unijunction to decrease.

The sawtooth voltage at the anode of Q102, is directly coupled to the base of Q103. Q103 is a driver amplifier and has two transistors wired as a Darlington pair; their input and output leads exit as a three-terminal device. This device exhibits a high input impedance to Q102, and thereby maintains excellent impedance isolation between Q102 and Q104.

The output waveform from the unijunction oscillator is not suitable, as yet, to produce a satisfactory vertical sweep. Such a waveform would produce severe stretching at the top of the picture and compression at the bottom. C105 and C106 modify the output waveform to produce satisfactory linearity. The sawtooth waveform output at Q103 is coupled through R122, the vertical linearity control R121, and on to C106 where the waveform is shaped into a parabola. This parabolic waveform is then added to the oscillator's waveform and changes its slope. Slope change rate is determined by the position of the variable resistor R121.

Q103 supplies base current through R123 and R124 to the vertical output transistor, Q104. Height control R124 varies the amplitude of the sawtooth voltage present at the base of Q104 and, therefore, varies the size of the vertical raster on the CRT.

The vertical output stage, Q104, uses a power type transistor which operates as a class A amplifier. No output transformer is required since the output impedance of the transistor permits a proper impedance match with the yoke connected directly to the collector. C107 is a DC-blocking capacitor which allows only AC voltages to produce yoke current. L1 is a relative high impedance compared to the yoke inductance. During retrace time, a large positive pulse is developed by L1 which reverses the curent through the yoke and moves the beam from the bottom of the screen to the top. Resistor R126 prevents oscillations by providing damping across the vertical deflection coils.

HORIZONTAL DEFLECTION

To obtain a signal appropriate for driving Q106, the horizontal output transistor, a driver stage consisting of Q105 and T101, is used. The circuitry associated with Q105 and Q106 has been designed to optimize the efficiency and reliability of the horizontal deflection circuits.

A positive going pulse is coupled through R127 to the base of Q105. The amplitude and duty cycle of this waveform must be as indicated in the electrical specifications (Section 1.2) for proper circuit operation.

The driver stage is either cut off or driven into saturation by the base signal. The output signal appears as a rectangular waveform and is transformer-coupled to the base of the horizontal output stage. The polarity of the voltage at the secondary of the driver transformer is chosen such that Q106 is cut off when Q105 conducts and vice versa.

During conduction of the driver transistor, energy is stored in the coupling transformer. The voltage at the secondary is then positive and keeps Q106 cut off. As soon as the primary current of T101 is interrupted due to the base signal driving Q105 into cut off, the secondary voltage changes polarity. Q106 starts conducting, and its base current flows. This gradually decreases at a rate determined by the transformer inductance and circuit resistance.

The horizontal output stage has five main functions: to supply the yoke with the correct horizontal scanning currents; develop a "C" VDC supply voltage for use with the CRT; develop a "B" VDC supply voltage for the video output stage; and develop a "D" VDC for the CRT bias.

Q106 acts as a switch which is turned on or off by the rectangular waveform on the base. When Q106 is turned on, the supply voltage plus the charge on C113 causes yoke current to increase in a linear manner and moves the beam from near the center of the screen to the right side. At this time, the transistor is turned off by a positive voltage on its base which causes the output circuit to oscillate. A high reactive voltage in the form of a half cycle

negative voltage pulse is developed by the yoke's inductance and the primary of T2. The peak magnetic energy which was stored in the yoke during scan time is then transferred to C109 and the yoke's distributed capacity. During this cycle, the beam is returned to the center of the screen.

The distributed capacity now discharges into the yoke and induces a current in a direction opposite to the current of the previous part of the cycle. The magnetic field thus created around the yoke moves the scanning beam to the left of the screen.

After slightly more than half a cycle, the voltage across C109 biases the damper diode CR103 into conduction and prevents the flyback pulse from oscillating. The magnetic energy that was stored in the yoke from the discharge of the distributed capacity is released to provide sweep for the first half of scan and to charge C113 through the rectifying action of the damper diode. The beam is then at the center of the screen. The cycle will repeat as soon as the base voltage of Q106 becomes negative.

C113, in series with the yoke, also serves to block DC currents through the yoke and to provide "S" shaping of the current waveform. "S" shaping compensates for stretching at the left and right sides of the picture tube because the curvature of the CRT face and the deflected beam do not describe the same arc.

L101 is an adjustable width control placed in series with the horizontal deflection coils. The variable inductive reactance allows a greater or lesser amount of the deflection current to flow through the horizontal yoke and, therefore, varies the width of the horizontal scan.

The negative flyback pulse developed during horizontal retrace time is rectified by CR104 and filtered by CR110. This produces approximately "D" VDC which is coupled through the brightness control to the cathode of the CRT (V1).

This same pulse is transformer-coupled to the secondary of transformer T2 where it is rectified by CR2, CR106, and CR105 to produce rectified voltages of approximately 12 kV (9 and 12 inches) or 9 kV (5 inches), "C" VDC, and "B" VDC respectively. 12 kV or 9 kV is the anode voltage for the CRT, and "C" VDC serves as the source voltage for grids No. 2 and 4 (focus grid) of the CRT. The "B" VDC potential is the supply voltage for the video output amplifier Q101.

LOW VOLTAGE REGULATED SUPPLY

All models use a series-pass, low voltage regulator designed to maintain a constant DC output for changes in input voltage, load impedance and temperature. Also included is a current limiting circuit designed to protect transistors connected to the "A" VDC output of the regulated supply from accidental output short circuits and load malfunctions.

The low voltage regulator consists of Q201, Q202, Q1, VR201, and their components. Q203 and its circuitry control the current limiting feature.

The 120 VAC primary voltage (220/240 V, optional) is stepped down at the secondary of T1 where it is rectified by a full wave bridge rectifier CR1. Capacitor C1 is used as a filter capacitor to smooth the rectified output of CR1. Transistor Q1 is used as a series regulator to drop the rectified voltage to "A" VDC and to provide a low output impedance and good regulation. Resistor network R207, R208 and R209 is used to divide down the "A" VDC voltage to approximately +6 VDC and apply this potential to the base of Q202. A reference voltage from zener diode VR201 is applied to the emitter of Q202. If the voltages applied to the base and emitter of Q202 are not in the proper relationship, an error current is generated through Q202. This error current develops a voltage across R202 which is applied to the base of emitter follower Q201 and then applied to the base of Q1 to bring the output voltage back to its proper level. R201 and C201 provide additional filtering of the rectified DC voltage.

Operation of this regulator may be better understood by assuming a certain operation condition has caused the output voltage to increase above normal. This positive increase of voltage is transferred to the base of Q202 where it is compared to the zener of VR201. The increase of forward bias of Q202 causes the collector voltage to drop as a result of the increased collector current through R202. This voltage is directly coupled to the base of Q1 through Q201 where it causes Q1 to conduct less and brings the regulated voltage back to its proper state.

The short circuit protection or current limiting action can be explained as follows. Assume the "A" VDC bus becomes shorted to ground. This reduced output voltage is sensed by the base of

Q202 turning that transistor off because of the reverse bias across its emitter and base junction. Simultaneously, the increased current through R204 increases the forward voltage drop across the base and emitter junction of Q203 and turns it on. Prior to the short circuit condition, Q203 was cut off. The increased collector current through R202 decreases the collector voltage of Q203 which is detected by the base of Q201 and direct-coupled to the base of Q1 causing that conductor to conduct less. This closed loop operation maintains the current available to any transistor connected to the "A" VDC bus at a safe level during a short circuit condition. Circuit breakers and fuses are not fast enough to protect transistors.

4.3.19 ADM-3 Answer Back

The ADM-3 answer back option provides the transmission of a predetermined message of up to 32 characters in length. This message can be sent by depressing the "here is" key on the keyboard or by the computer command "ENQ." The message is stored in a read only memory (ROM) and is supplied at time of purchase. This message can be exchanged by LSI customer service.

4.3.20 ADM-3 Extension Port Current Loop

The extension port of the ADM-3 provides an auxiliary port for interfacing other peripheral devices in a loop through or daisy chain environment.

The addition of current loop to this port adds to the flexibility and allows more devices to hook up in this manner.

The transmitted data output for current loop is on pin 25 of connector J-2 and does not supply current (external source). Received data is inputed on pin 2 and is internally grounded (Terminal sync.).

4.3.21 ADM-3 Numeric Pad

The numeric pad option provides 14 keys for operator convenience. These keys consist of 10 numeric (0-9), 3 punctuation ("-", ".", ",") and an "Enter" key. The codes associated with these are transmitted as such with the exception of "Enter" which transmits the ASCII character "RETURN."

NOTE

The numeric keys on the Key pad parallel the numeric on the standard Keyboard, therefore, if the shift key is depressed when using the keypad, the shifted characters will be generated as on the standard keyboard.

SECTION 5
MAINTENANCE

5.1 GENERAL

This section contains instructions and information for performing routine and corrective maintenance of the ADM-3. It is assumed that the maintenance technician is thoroughly familiar with information in Sections 1 through 4 of this manual.

5.2 INSTALLATION

It is assumed that the ADM-3 has been installed and set-up for operation in accordance with procedures outlined in Section 2. Any operating problem following installation should be approached initially by checking settings of internal switches and front panel switches located under the identification plate, and checking interface cables. Figure 5-1 shows assignments of terminals in interface connectors J1 and J2.

5.3 ROUTINE MAINTENANCE

The operator is expected to keep the exterior of the ADM-3 clean. The case should be cleaned using a household cleaner and a soft, damp, lint-free cloth or paper towel. **NEVER** use a petroleum-base solvent such as lighter fluid which could damage the plastic or painted surface.

Be careful not to wipe dust into the keyboard, and don't let excessive spray cleaner run between the keys.

Other than cleaning, the ADM-3 needs no routine maintenance.

5.4 OPENING ADM-3 COVER

To remove the cover of the terminal (along with the monitor CRT) for access to adjustments or for other maintenance, proceed as follows:

a. Remove the two slot-head screws located under the front corners of the terminal base.

b. Lift the cover from the front, lifting it upwards and rearwards until it is lowered to rest on the table.

c. To remove the cover from the base, disconnect the cable connecting the monitor to the printed circuit board, slide the cover towards the left on its hinge pins, and then remove the cover from the base.

   Note that all components on the ADM-3 circuit board are accessible for inspection and voltage measurement when the cover is fully open.

5.5 ADJUSTMENTS

All adjustments in the ADM-3 are associated with the CRT monitor.

5.5.1 Contrast Adjustment

Contrast may be adjusted for best viewing by the operator. The control is located at the upper right-hand corner of the keyboard.

5.5.2 Brightness Adjustment

The brightness (background intensity) control is located on the video board assembly within the ADM-3 cover.

WARNING

Brightness must be adjusted with power applied to the ADM-3. To avoid hazardous electrical shock, adjust using a non-conductive screwdriver and considerable care.

Adjust brightness just to the level at which the white raster is extinguished. The optimum contrast can then be obtained when a video signal is applied.

5.5.3 Low Voltage Supply

The 15V dc supply for the monitor is located on the main circuit board. Measure voltage at the junction of R114 and R130 on the monitor video board, and adjust to obtain +15V dc +0.1V dc.

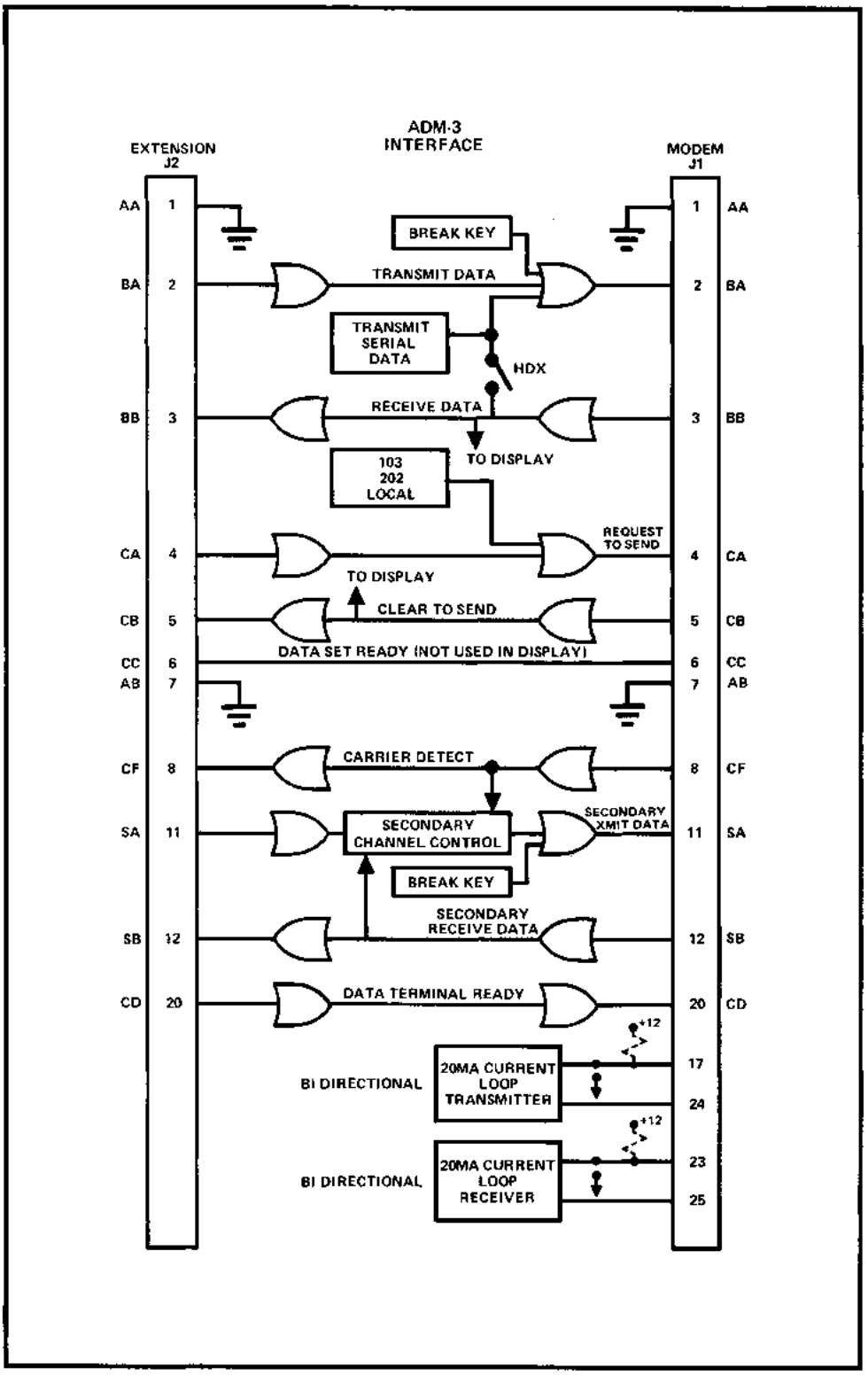


Figure 5-1. Interface Connector Terminal Assignments

5.5.4 Vertical Adjustment

There is a slight interaction among the vertical frequency, height, and linearity controls. A change in the height of the picture may affect linearity.

a. Apply video and synchronization signals to the monitor.

b. Set the vertical frequency control (R116) near the mechanical center of its rotation.

c. Adjust the vertical height control (R124) for desired height.

d. Adjust the vertical linearity control (R121) for best vertical linearity.

e. Remove the vertical drive signal from the unit. Or, alternatively, use a short jumper lead, and short the vertical drive input terminal of the printed circuit card edge connector to ground.

f. Readjust the vertical frequency control (R116) until the picture rolls up slowly.

g. Restore vertical drive to the monitor.

h. Recheck height and linearity.

5.5.5 Horizontal Adjustments

Raster width is affected by a combination of the low voltage supply, width coil L101, and the horizontal linearity sleeve located on the neck of the CRT beneath the yoke.

a. Apply video and synchronization signals to the monitor. Insert the horizontal linearity sleeve about 2/3 of its length under the yoke. (If you received a monitor from the factory in which the placement of the linearity sleeve has been determined, make a mark on the sleeve and reinsert the sleeve to this mark when removal of the yoke and linearity sleeve are required.)

   If the linearity sleeve is inserted farther than necessary, excessive power will be consumed and the horizontal output circuitry could be overstressed.

b. Adjust the horizontal width coil (L101) for the desired width.

c. Insert the linearity sleeve further under the yoke to obtain the best linearity. Although this adjustment will affect the raster width, it should not be used solely for that purpose. The placement of the linearity sleeve should be optimized for the best linearity.

d. Readjust L101 for proper width.

e. Observe final horizontal linearity and width, and touch up either adjustment if needed.

No horizontal hold control is used in this monitor.

5.5.6 Focus Adjustment

The focus control (R107) adjusts best overall display focus. However, because of the construction of the gun assembly in the CRT, this control does not have a large effect on focus.

5.5.7 Centering

If the raster is not properly centered, it may be repositioned by rotating the ring magnets behind the deflection yoke.

Do not use ring magnets to offset the raster from its nominal center position; this will degrade the resolution of the display.

If the picture is tilted, rotate the entire yoke.

5.6 CORRECTIVE MAINTENANCE

Corrective maintenance consists of locating the cause of a malfunction and repairing it. The cause may be isolated only to the module level, with the failed module sent to a repair facility or returned to Lear Siegler for repair or replacement; or the user may choose to isolate the cause to the component level and replace the failed component.

Repair at the component level should not be attempted except by trained personnel using suitable tools and test equipment.

5.6.1 Failure Analysis

Troubleshooting of the ADM-3 is straightforward and conventional. Suggested steps in troubleshooting are:

a. Get the facts. Learn the state of the machine when the malfunction occurred. Look for operator error, blown fuses, or modem or computer failure.

b. Operate the ADM-3 to determine which functions have failed. For example: Does it receive but not transmit? Has a single function (like Clear Screen or Backspace) failed? Intelligent use of this information will speed fault isolation.

c. Isolate the cause of the failure to a specific module (for example, to the CRT, a keyboard row, the flyback assembly, or the main circuit board).

d. If the failed module is to be repaired at the machine site, further isolate the cause to a failed component (or components). Refer to information in Section 4 and to the logic and assembly drawings in Section 6 of this manual.

e. Replace the failed module or component and test by running the ADM-3 in the same mode of operation in which the failure occurred.

f. Record the symptoms, cause, troubleshooting procedure, and mode of repair for future reference.

Following are useful ideas to speed troubleshooting and repair:

a. After warm-up, the cursor should appear at its "home" position (under the first character position of the bottom character row), with no data in the unit. If it does not, enter data from the keyboard (with the HDX/FDX switch in the HDX position) and see if it appears on the screen. If it does not, proceed to check power supply voltages, intensity and contrast control settings, clock and display counter operation, monitor sweep drive signals, and monitor video and drive circuits, in that order.

b. To verify operation of transmitter logic, simply see that data generated at the keyboard appears on the screen (HDX/FDX switch in the HDX position only!). This checks all transmitter logic except the inverter F4-10 and driver A8-3.To check FDX, create a short in pins 2 and 3 of the modem connector. This will also check the inverter F4-10 and the driver A8-3.

c. It is possible to use internal turnaround switches (LOCAL, 103 and 202) to force Request to Send to either state, or put it under ADM-3 control. Intelligent use of these switches, and reference to paragraph 4.3.16, may simplify interface troubleshooting.

5.6.2 Troubleshooting the Monitor

Following is a guide to troubleshooting the CRT monitor. It is assumed that sweep drive and video signals from the main circuit board are normal (see figure 5-2).

a. Screen is dark. Check settings of brightness and contrast controls. Check +15V dc supply at junction of R114 and R130. Check security of all monitor connectors.

b. No video. Check setting of contrast control, check Q101 (refer to monitor schematic diagram in Section 6 of this manual).

c. Overheating and excessive power consumption. Check horizontal linearity sleeve (para. 5.5.5). Check Q105 and Q106.

Refer to the monitor voltage waveforms (figure 5-3), and component layout (figure 5-4), and to cabling and schematic diagrams in Section 6 of this manual.

5.6.3 Removing and Replacing Monitor CRT and Subassemblies

WARNING

Be sure to discharge anode voltage to ground before attempting to remove any monitor subassembly or CRT.

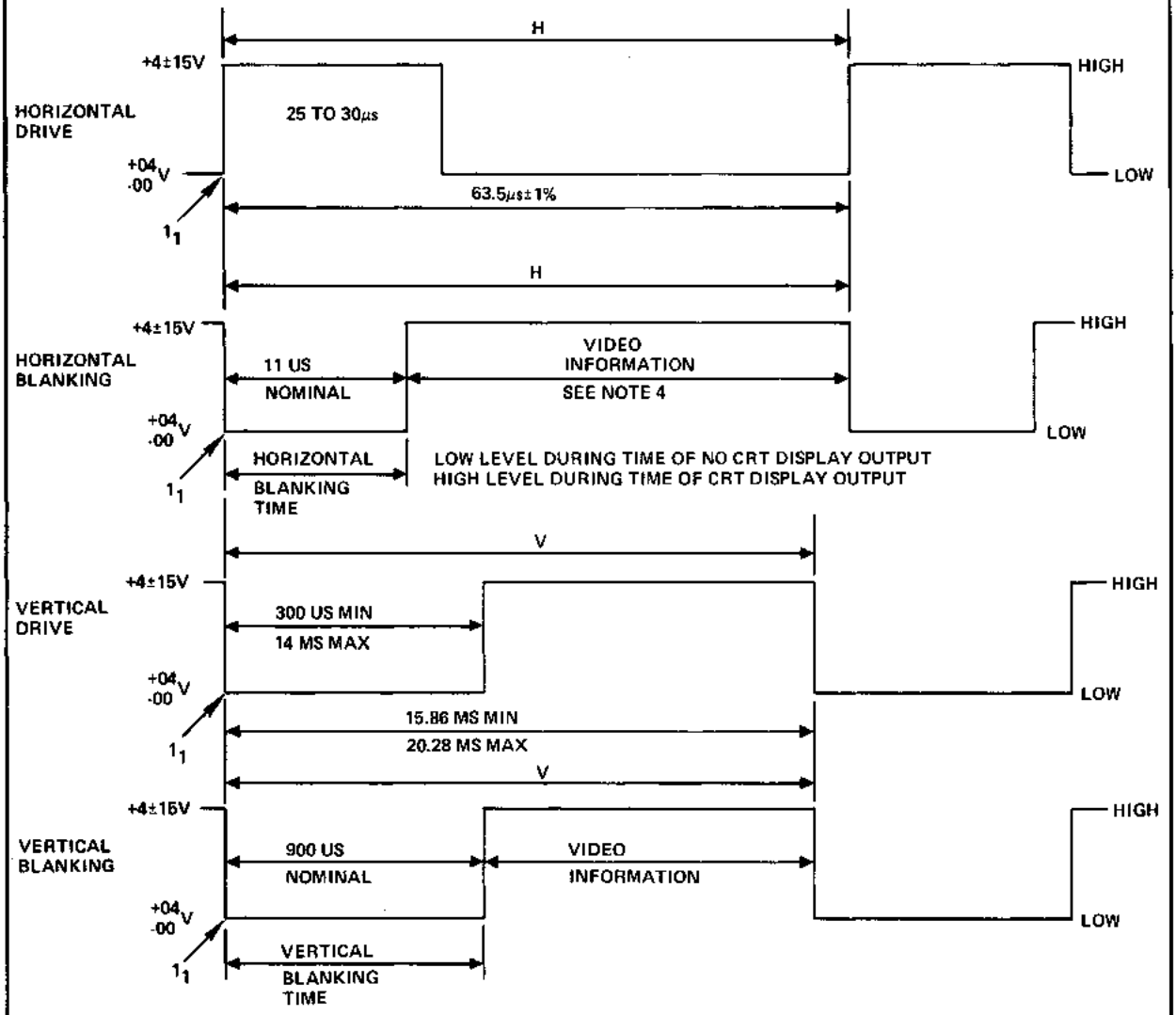
The monitor comprises the CRT with its steel mounting frame, the flyback assembly, and the circuit board.

To remove the CRT, proceed as follows:

a. Unhook (at both ends) the spring that lies across the CRT.

b. Remove connector from the base of the CRT.

c. Remove the anode connector from the lower surface of the CRT.



NOTES

1. The leading edges of Drive and Blanking waveforms must start at time tp. Nominal Blanking times should be observed.
2. H = time from start of one line to start of next line.
3. V = time from start of one field to start of next field.
4. Video pulse width should be equal to or greater than 100 nsec.

Figure 5-2. Inputs to Monitor, Timing Diagram

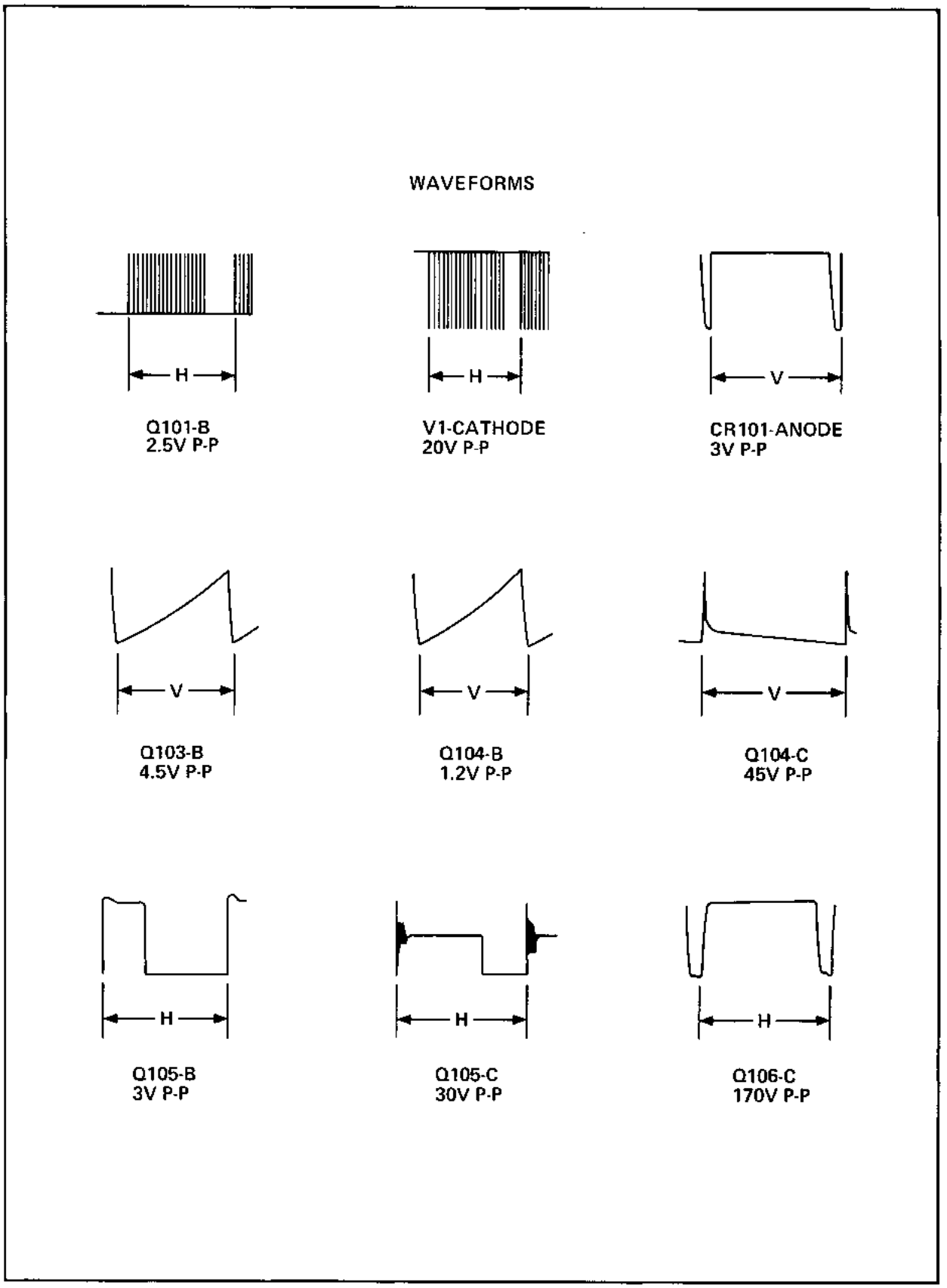


Figure 5-3. Monitor Voltage Waveforms

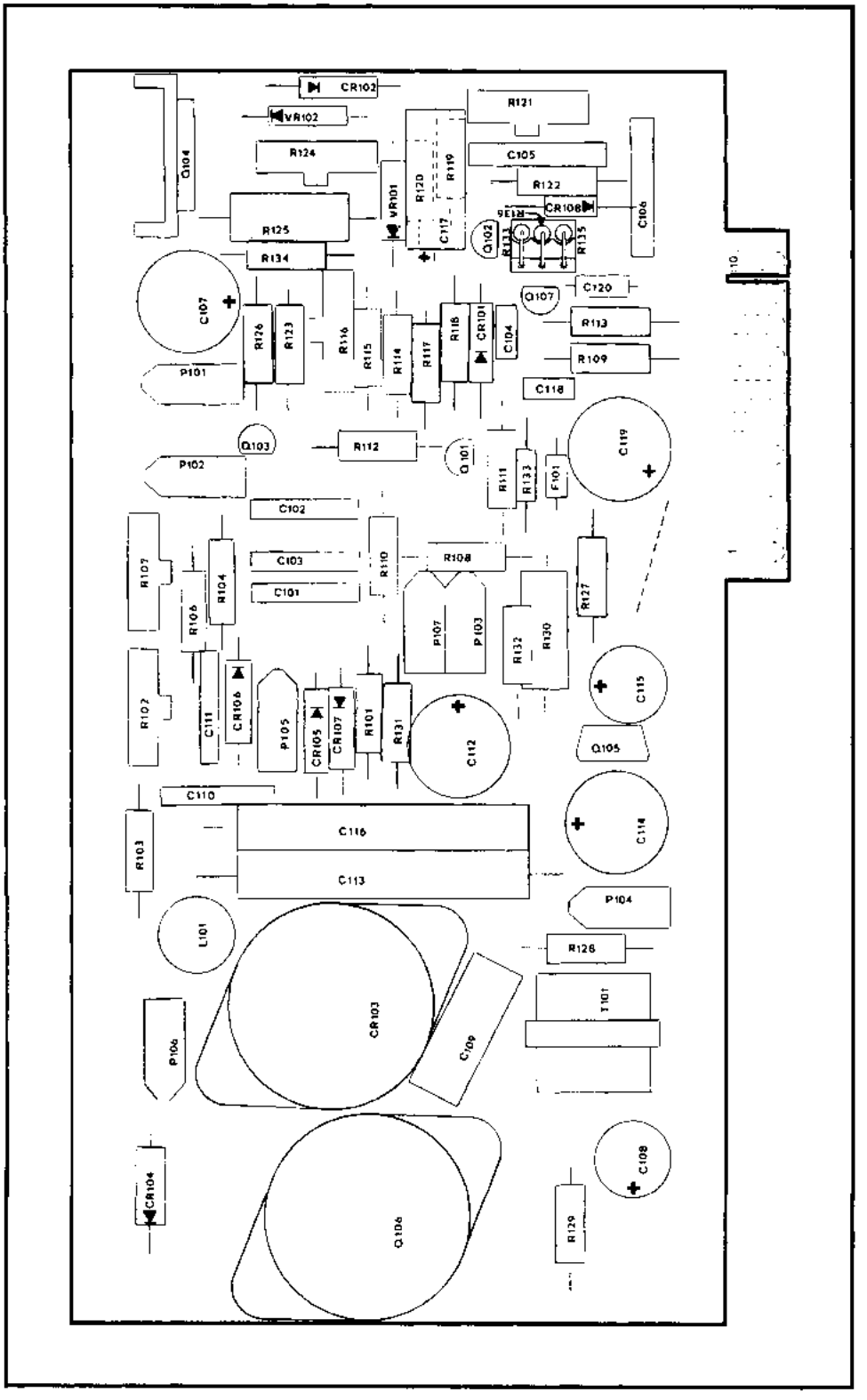


Figure 5-4. Monitor Video Board, Component Layout

d. Using a socket wrench or screwdriver, loosen the clamps at both sides of the CRT frame until the clamps can be turned to clear the CRT frame.

e. Grasping the CRT securely, lift it upwards and out of the ADM-3 cover and set it aside.

To install a new CRT, follow the preceding steps in reverse order.

To remove the flyback assembly, proceed as follows:

a. Disconnect anode connector from CRT.

b. Disconnect Molex connector that connects flyback assembly to the monitor circuit board.

c. Using a screwdriver, loosen the hex-head screw that clamps the flyback assembly to the molded cover.

d. Lift flyback assembly upwards until the screw clears the slot in the mounting plate, then remove assembly from the cover.

To remove the monitor circuit board, proceed as follows:

a. Remove the flyback assembly (refer to preceding steps).
b. Disconnect all Molex connectors from the monitor circuit board.

c. Slide circuit board from the slots in the molded cover and remove.

To replace monitor circuit board and flyback assembly, perform the preceding steps in reverse order.

5.6.4 Troubleshooting the Main Circuit Board

Troubleshooting of the main circuit board is based essentially on the principles outlined in paragraph 5.6 – that is, the technician must be familiar with the theory of operation (Section 4) and must be equipped with suitable test equipment.

With the ADM-3 cover opened, all components on the main circuit board are accessible to probes and other test devices. Components are generally identified on the board; but reference may be made to the component layout drawing, and the logic diagrams in Section 6 of this manual.

Table 5-1 lists connectors on the board and defines all terminal assignments.

5.6.5 Removing and Replacing the Main Circuit Board

To remove the main circuit board, proceed as follows:

a. Remove external cables from connectors J1 and J2 at the rear of the ADM-3.

b. Remove all cable connectors from the upper surface of the circuit board.

c. Lift circuit board straight upwards to clear the guide pins, then remove from the base.

Note that there are no fasteners to hold the circuit board, which is kept in place by the two steel guide pins and the closed cover.

Replace the circuit board by performing removal procedures in reverse order.

5.6.6 Removing and Replacing Key Switch Contacts

The tools required to remove the key switch contacts from the keyboard are:

insertion tool and guide
soldering iron (low temperature)
wicking device
short-nosed needle nose pliers
with serrated jaws

The procedure is as follows:

a. Remove the solder from the contact (dewick) with a low-heat soldering iron so as not to damage circuit pads. The contacts will protrude about 1/32 inches beyond the back of the logic board. Make sure that the contacts are completely free of any solder by brushing them with your finger, the contacts should move freely.

b. Turn the board over so that the keyboard is up.

c. Remove the key top whose contacts need to be replaced.

d. With the pliers, firmly grasp the plunger in the corner (see figure 5-5). Pull straight up with a firm pull.

Table 5-1. Main Circuit Board Connector Terminals

Connector/Symbol		Pin	Signal
RS232 Interface	(J1)	1	Frame Ground
		2	BA (Transmit Data)
		3	BB (Receive Data)
		4	CA (Request to Send)
		5	CB (Clear to Send)
		6	CC (Data Set Ready)
		7	Signal Ground
		8	CF (Carrier Detect)
		9,10	(not used)
		11	SA (Secondary Transmit Data)
		12	SB (Secondary Receive Data)
		13-16	(not used)
		17,24	Current Loop Transmitter
		20	CD (Data Terminal Ready)
		18-22	(not used)
		23,25	Current Loop Receiver
RS232 Extension	(J2)	1	Frame Ground
		2	BA (Transmit Data)
		3	BB (Receive Data)
		4	CA (Request to Send)
		5	CB (Clear to Send)
		6	CC (Data Set Ready)
		7	Signal Ground
		8	CF (Carrier Detect)
		9,10	(not used)
		11	SA (Secondary Transmit Data)
		12	SB (Secondary Receive Data)
		13-19	(not used)
		20	CD (Data Terminal Ready)
		21-25	(not used)
Low-Voltage AC Power	(J3)	1,2	Input to +V dc rectifier
		3,5	Input to +12V dc rectifier
		4	Ground
Monitor Low-Voltage AC Power	(J4)	1,2	Input to +V dc rectifier
Beep Speaker	(J5)	1,2	Drive to beeper speaker
Keyboard Interface to 10-Key Pad	(J6)	2,3,16	Col 3, 2, 0
		5,9,10	Row 0, 1, 2
		11,12,13	Row 3, 4, 5
		14,8,7	Row 6, 7, 8
		5,1,15,4	Row 9, C, D, E
Monitor Interface	(J7)	1	
		2	
		3	
		4	Video to monitor
		5,6,7	Ground
		8	Horizontal drive to monitor
		10	Ground
		11	+15V dc to monitor

CAUTION

The plunger is fragile; pulling to the side can break plunger or housing.

e. Remove the spring.

f. With the pliers, grasp the contact and pull vertically; remove both contacts.

g. Place the insertion tool guide in the switch housing making sure that the keyway is towards the front of the keyboard. (See figure 5-6).

h. Insert the solid contact (P/N 373-30052-2) in the insertion tool with the bend to the outside and the solder end up (see figure 5-7). Insert the split contact (P/N 373-30053-2) with the split end in first (see figure 5-8).

i. Place the insertion tool into the guide matching keyway slot and key. Press the tool firmly straight down until the contacts are seated firmly (the tool clicks). (See figure 5-9).

j. Remove the tool and the guide.

k. Replace the spring.

l. Replace the plunger making sure that the bar is parallel with the contact opening. Work the plunger down slowly, separating the contacts with the crossbar of the plunger (see figure 5-10).

m. Press the plunger firmly down until it is seated (it clicks).

n. Replace the key top.

o. Turn the board over and verify that the contacts extend about 1/32 inch past the board.

p. Resolder the contacts in place.

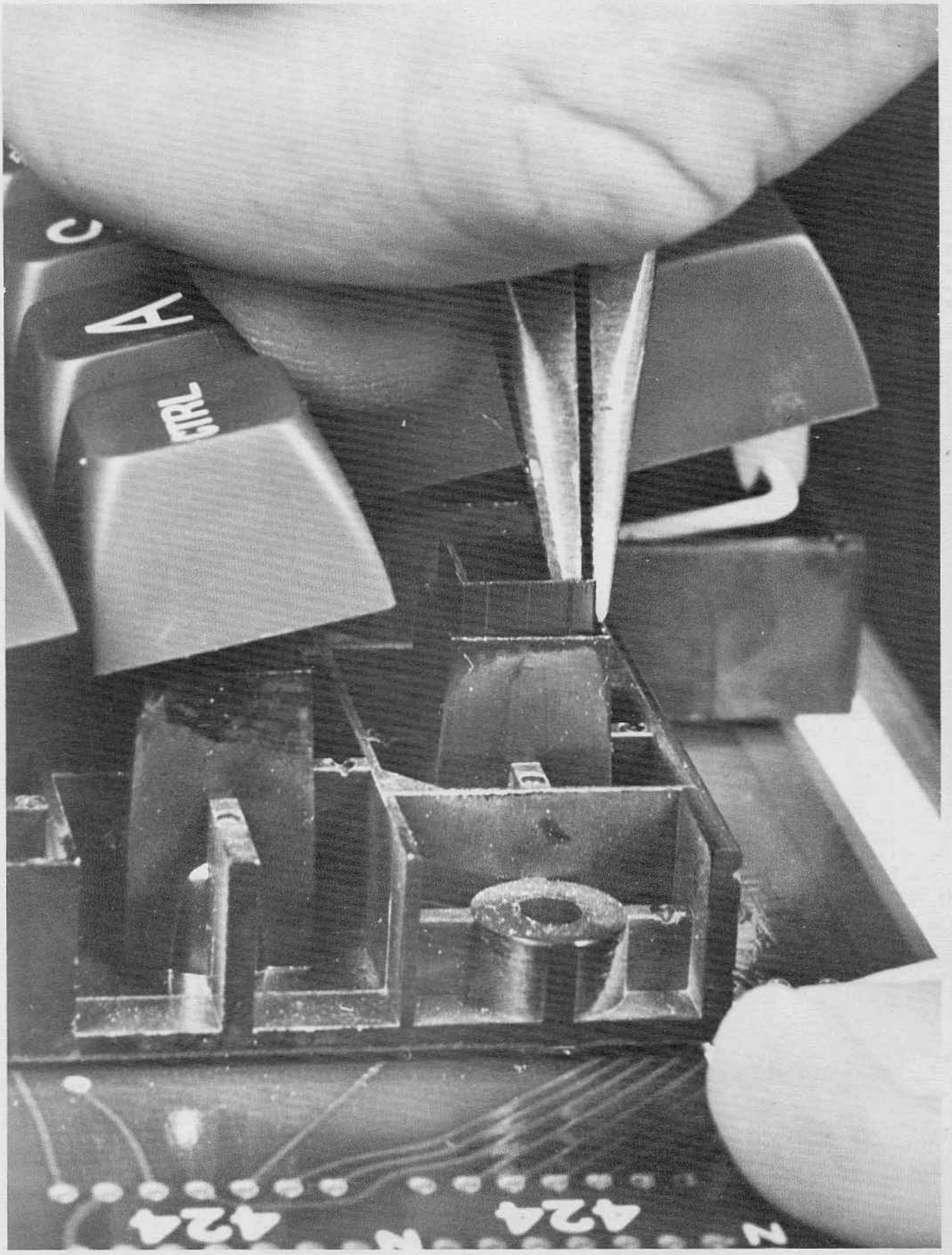


Figure 5-5.

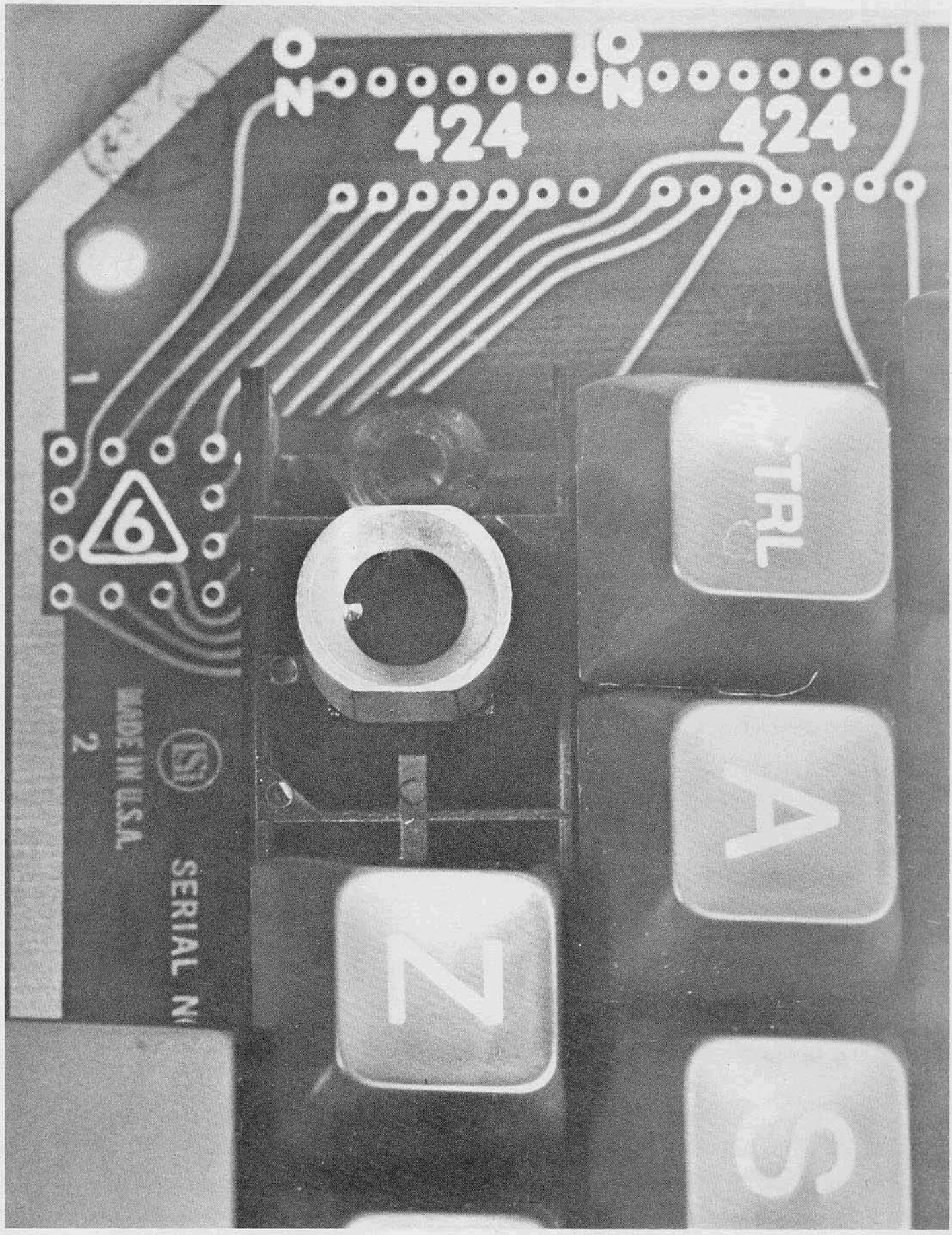


Figure 5-6.

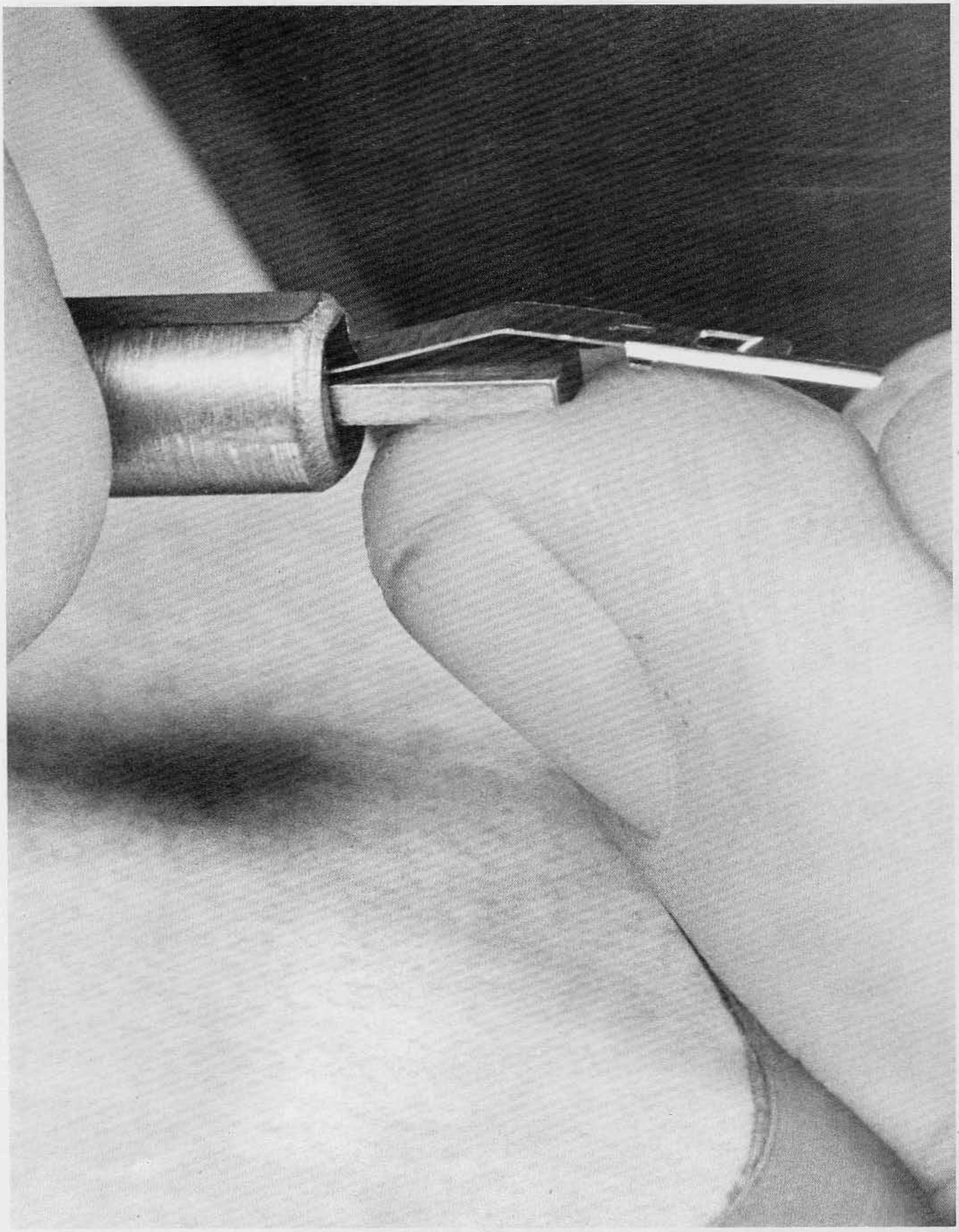


Figure 5-7.

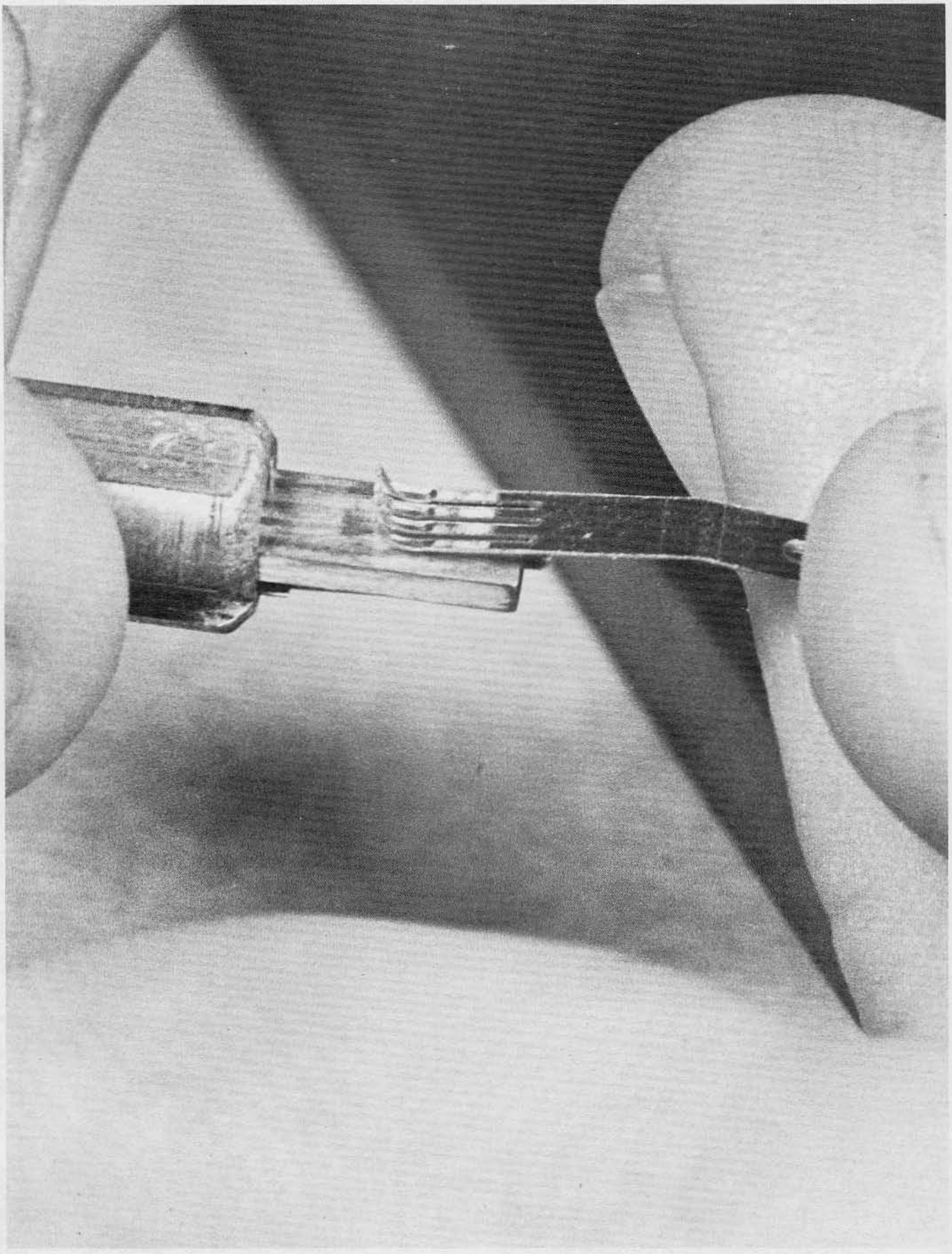


Figure 5-8.

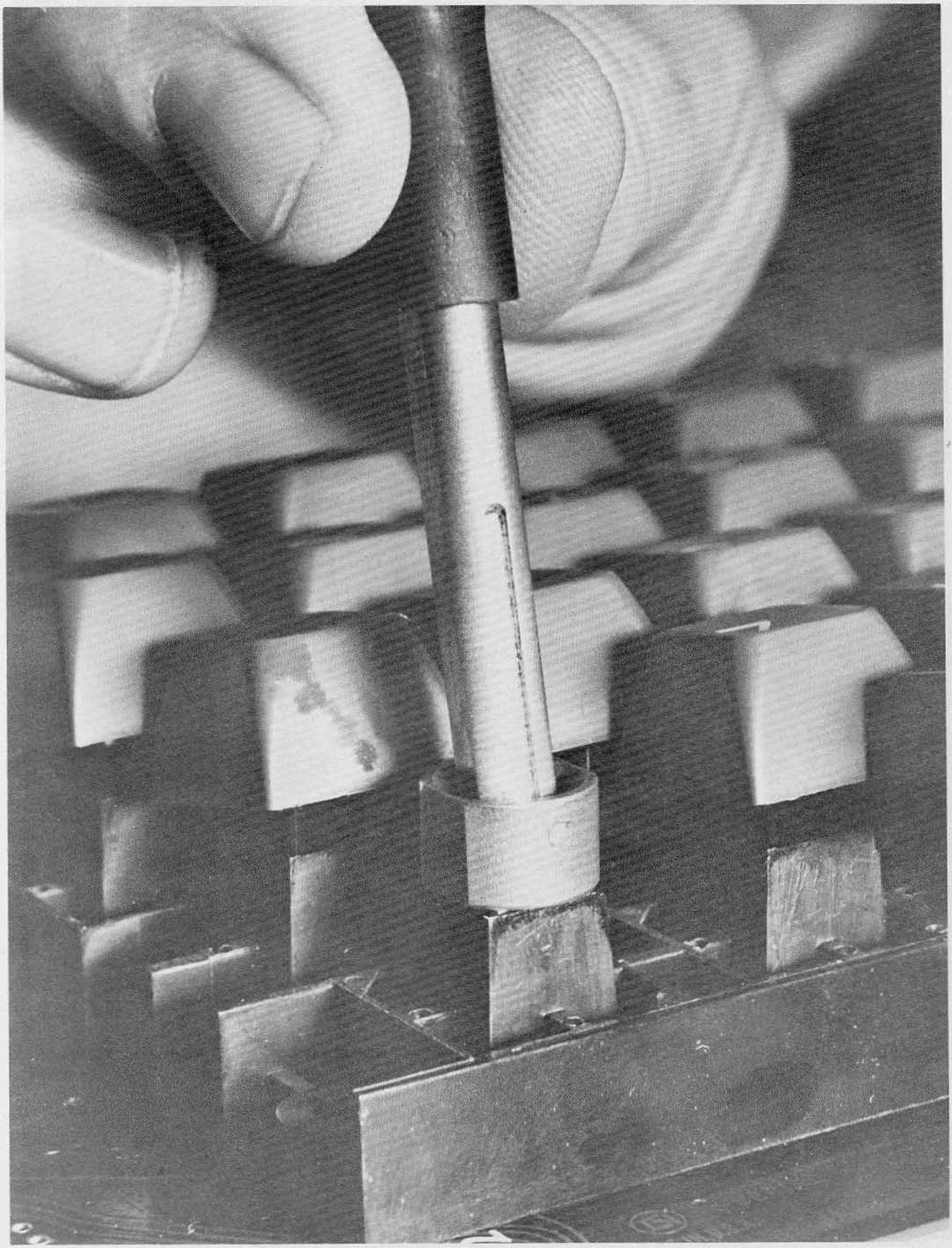


Figure 5-9.

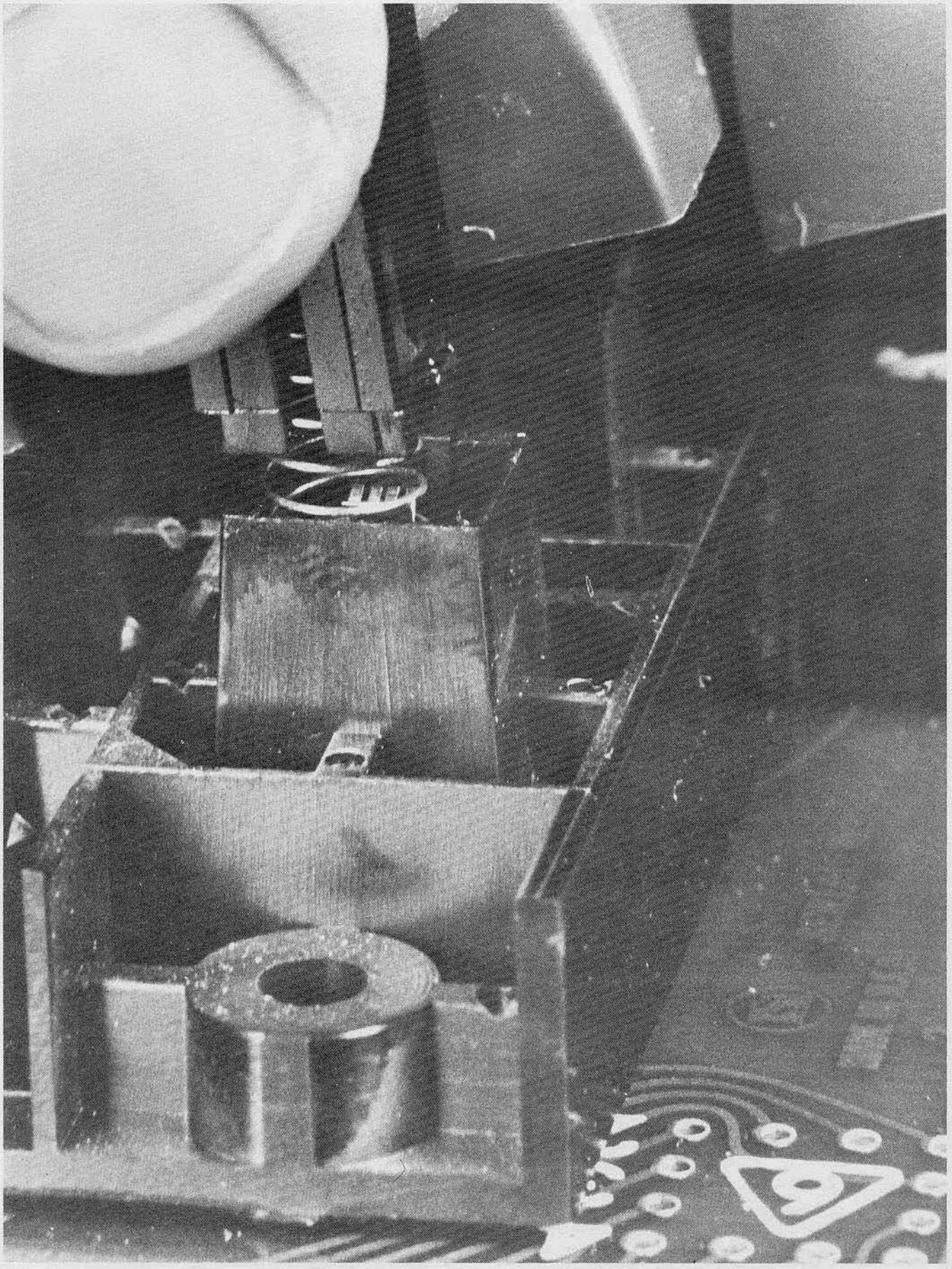


Figure 5-10.

SECTION 6
DRAWINGS

This section contains drawings of the functional areas of the ADM-3 as well as a technical description of the logic in each area. The basic logic was presented in Section 4 (Theory of Operation).

6.1 SCHEMATIC SHEET #2 — SYSTEM COUNTERS

The oscillator located in zone D4 provides the basic clocking for the entire display unit. It oscillates at a frequency of 10.8864 MHz (period = 91.8577 nsec.) which is twice the frequency of the video going to the monitor. This clock also goes to the DOT counter which counts the seven dot positions horizontally in a character position. This DOT counter (74161 – zone D2) has seven different states. It begins its cycle by presetting to a count of 10, counts through the overflow at 15, and presets again at a count of 0. The purpose of this counter is to time the presentation of the sequential addresses to the character generator and the presetting of the video serializer. Its final output, DC3, has a duty cycle of 85.7% and a frequency of 1.5552 MHz. It also is the clock to the next counter in line.

The CHARACTER counter (zone C3) has eight stages and is used to time the positioning of the eighty characters and the horizontal retrace time along one video raster line. The total division provided by this counter is 96, 80 for the video portion of the raster line and 16 for the horizontal retrace. The actual count goes from 0 to 79, presets to 240, and counts out to the overflow point at 255 and restarts another cycle for the next raster line. Stages labeled CC0 through CC6 are straight binary counts while CC7 actually has a weight of 80. This means that all CHARACTER counter decodes less than 80 have CC7 low and all decodes 80 and higher have CC7 high. In practical usage, CC7 low indicates that the unit is operating in the video portion of the raster and CC7 high indicates horizontal retrace time.

The flip-flop labeled ICC80 (zone C2) actually represents the decode CHAR COUNTER = 80 or one count into the horizontal retrace. This term is utilized internally to indicate the time when a command received from the normal I/O interface can be acted upon. The LCCLK circuit (zone B1) provides the clock for the following counter.

The next counter in line is the LINE counter which counts the raster lines in one row of characters. This counter divides by nine and is a straight binary count. Counts 0 and 8 indicate the two raster lines vertically between two rows of characters while counts 1 through 7 are the raster lines during which the video is being generated. The final stage out of this counter provides the clock for the ROW counter and has a frequency of 1.800 KHz.

The ROW counter (zone A2) is a variable counter. Its purpose is to count the rows of characters appearing vertically down the screen. It also counts through the vertical retrace time. Its count changes from a division by 30 for 60 HZ refresh to a division by 36 for 50 HZ refresh. The 50/60 HZ switch is positioned according to the frequency of the primary input power line. The ROW counter progresses in a straight binary fashion up to its selected maximum count and presets to zero.

The tri-state buffers (74125) located in zones D3, C4 and A4 are for the use of the automatic test equipment and essentially have no effect on the normal operation of the display unit.

6.2 SCHEMATIC SHEET #11 — INTERFACE CONTROL

This schematic essentially shows the request-to-send and clear-to-send operation for the ADM-3. The flip-flop K12 (7474, zone D3) is the CLEAR TO SEND control flop. If clear to send is high at the RS232 level, then the UART transmit clocks are turned on and the unit can transmit at any time. If CTS falls during the time a byte is being transmitted, the ADM-3 will continue to transmit the remainder of that byte then shut down in the "marking" state.

There are four ways that REQUEST-TO-SEND can be controlled in the ADM-3. First, RTS can be low all of the time which is accompanied by opening all three of the switches located in zone A2. Then RTS can rise before the transmission of a character, stay up during the transmission of that one character, and fall as soon as it clears the UART. This is done by closing the switch

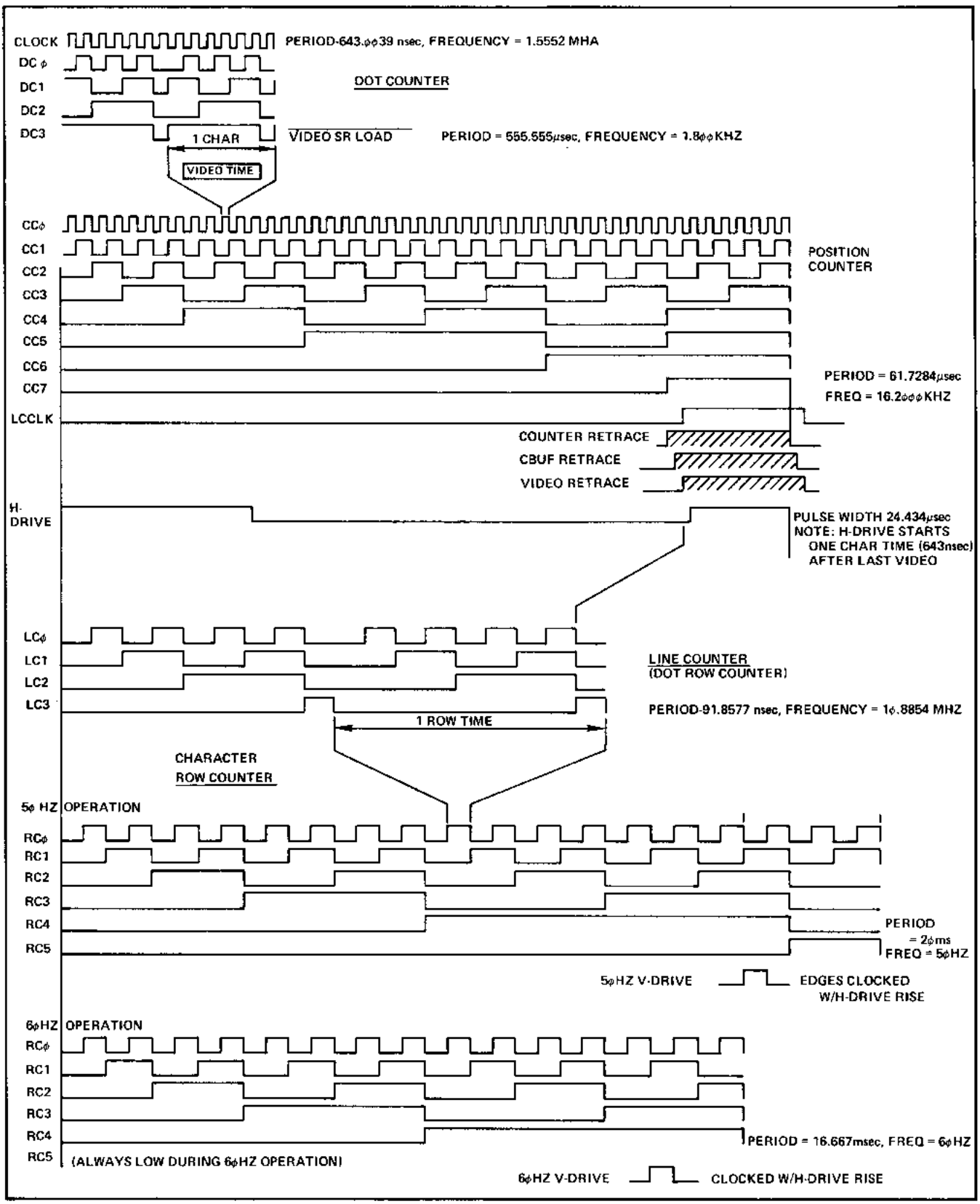


Figure 6-1. Display Counter Timing

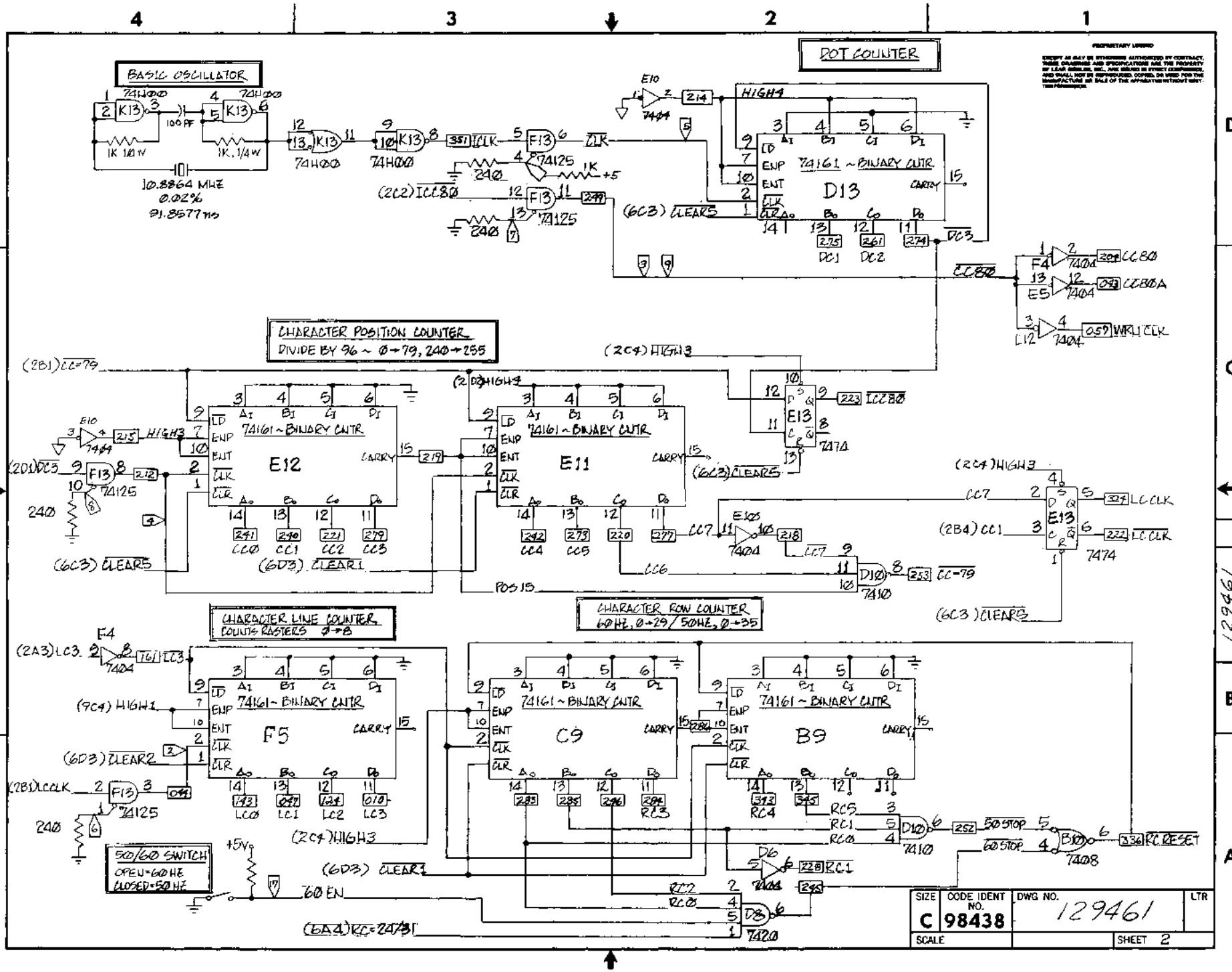

DOT COUNTER
BASIC OSCILLATOR
CHARACTER POSITION COUNTER
DIVIDE BY 96 ~ 0→79, 240→255
CHARACTER LINE COUNTER
COUNTS RASTERS 0→8
CHARACTER ROW COUNTER
60 HZ, 0→29 / 50 HZ, 0→35
50/60 SWITCH
OPEN=60 HZ
CLOSED=50 HZ
74161 ~ BINARY CNTR
D13
E12
E11
F5
C9
B9
E13
F4
E5
L12
E10
E10
E10
D10
D8
D6
B10
10.8864 MHZ
0.002%
91.8577 ns
1K 1/8 W
1K, 1/4 W
100 PF
240
1K
+5V
+5
60 EN
HIGH4
HIGH3
HIGH1
CLEAR5
CLEAR1
CLEAR2
CC=79
CC7
CC6
POS 15
RC RESET
50 STOP
60 STOP
CCLOCK
CCLOCK
WR1 CLK
CCBØ
CCBØA
RC1
RC2
RC=247?
7404
7400
7408
7410
7420
7474
7425
7430
DC1
DC2
DC3
CC0
CC1
CC2
CC3
CC4
CC5
LC0
LC1
LC2
LC3
RC4
RC5
RC3
RC0
CARRY
ENP
ENT
CLR
LD
SIZE
C
CODE IDENT NO.
98438
DWG NO.
129461
LTR
SCALE
SHEET 2

Figure 6-2
6-3

marked LOCAL. If the switch labeled 103 is closed, then RTS will be held high all of the time. A device setting on the extension port can also exercise RTS control through Pin 4 of connector J2. The last switch on this section is labeled "202". If this RTS CONTROL switch is closed, then one other selection must be made. The two choices are RTS control utilizing code turn-around and RTS under reverse channel control. This selection is made using switch in zone C4. If code turn is selected, then the actual code to be used must be specified. This is done by closing one of the two switches located on gate input D2-2 (7427, zone C4) which are labeled ETX or EOT. These are the only two selections provided for in the ADM-3. When the selected code is received into the INPUT DATA BUFFER, this information is latched into flop E1-6 (74S113, zone C3) labeled LATCHED CODE. This information is allowed to toggle flop B8-11 (74H106, zone B2) if CARRIER DETECT (zone B4) has gone low, indicating that the distant end has dropped off.

If another of the selected codes is then received, the unit will immediately switch to receive without waiting for carrier detect since our RTS was maintaining CARRIER DETECT high.

If reverse channel operation is selected, then the two inputs that control RTS are SECONDARY RECEIVE DATA and CARRIER DETECT (SB and CF respectively). If SB goes low, the ADM-3 will unconditionally switch to the receive mode (RTS low). If CF is also low, SECONDARY TRANSMIT DATA will go low. If CF is high, indicating that the distant end has turned on, SECONDARY TRANSMIT DATA (SA) will go high. This last condition is the normal receive condition in reverse channel operation. In order to switch to the trarnsmit mode, the distant end controlling the terminal raises SECONDARY RECEIVE DATA (SB). Then, the only other condition that has to be met is that CARRIER DETECT (CF) must fall, indicating that the distant end has dropped its RTS. At that time, the ADM-3 will turn RTS on within 62msec. In this reverse channel operation, if a command is given to turn RTS, then no further commands will be recognized for a period of approximately 250msec. This gives the modem time to propagate its signals. This timing is accomplished with the counter and two flops located in zones C1, C2, D1, and D2. All controlling inputs and controlled outputs can be driven from the extension port.

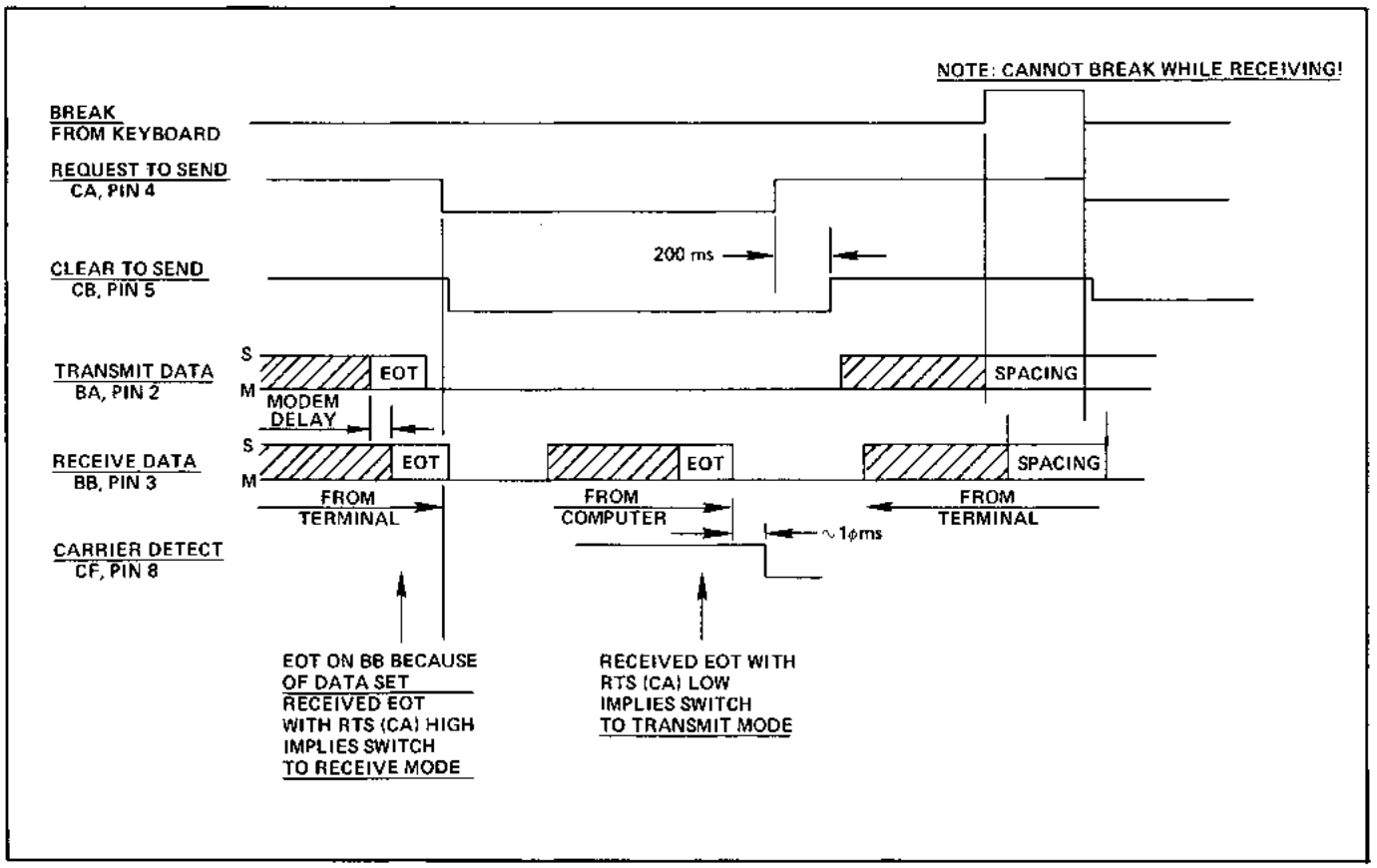


Figure 6-3. Interface Timing for Code Turnaround

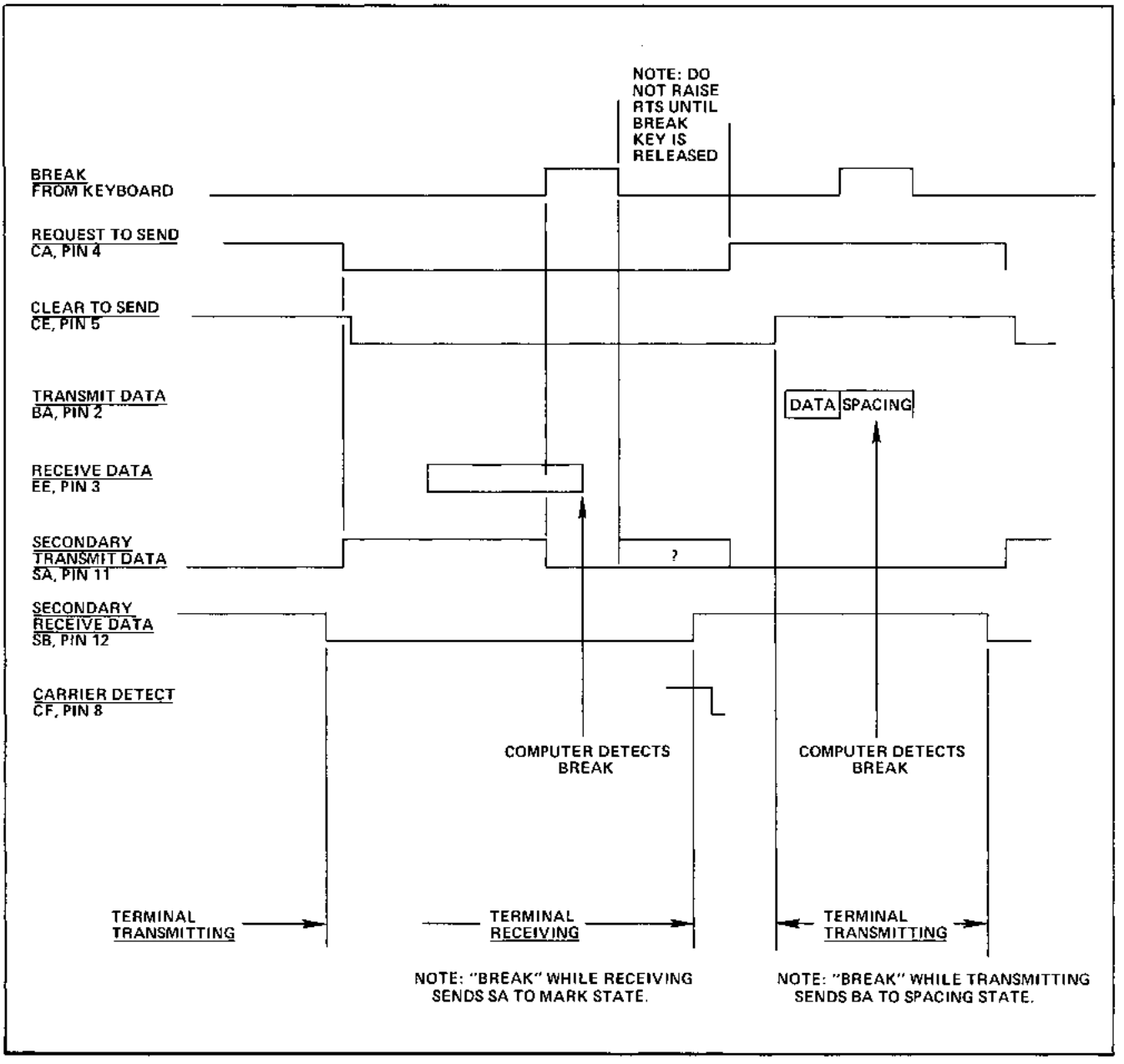


Figure 6-4. Interface Timing for Reverse-Channel Operation

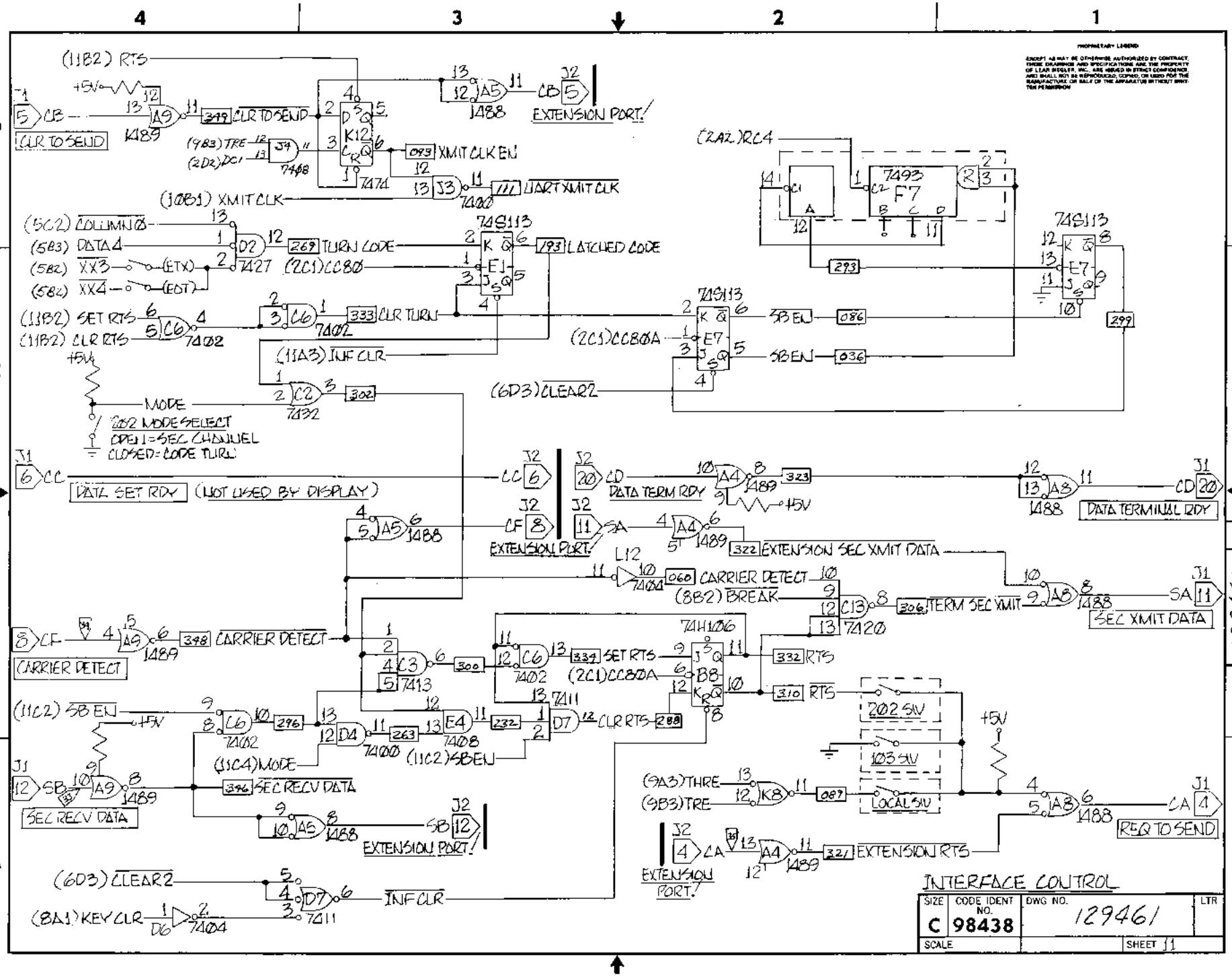

INTERFACE CONTROL
SIZE C
CODE IDENT NO. 98438
DWG NO. 129461
LTR
SCALE
SHEET 11
(11B2) RTS
CLR TO SEND
XMIT CLK EN
UART XMIT CLK
(10B1) XMIT CLK
(5C2) COLUMN Ø
(5B3) DATA 4
(5B2) XX3
(5B2) XX4
TURN CODE
LATCHED CODE
(2C1) CC8Ø
(11B2) SET RTS
(11B2) CLR RTS
CLR TURN
(11A3) INF CLR
MODE
202 MODE SELECT
OPEN = SEC CHANNEL
CLOSED = CODE TURN
(2A2) RC4
SB EN
(2C1) CC8ØA
(6D3) CLEAR 2
DATA SET RDY
(NOT USED BY DISPLAY)
DATA TERM RDY
DATA TERMINAL RDY
EXTENSION PORT
CARRIER DETECT
(8B2) BREAK
TERM SEC XMIT
SEC XMIT DATA
SET RTS
(2C1) CC8ØA
RTS
CLR RTS
(11C2) SB EN
(J1C4) MODE
SEC RECV DATA
(9A3) THRE
(9B3) TRE
202 SW
103 SW
LOCAL SW
REQ TO SEND
EXTENSION RTS
(8A1) KEY CLR
INF CLR
PROPRIETARY LEGEND

Figure 6-5
6-6

6.3 SCHEMATIC SHEET #3 — OFFSET COUNTER CURSOR REGISTER BEEPER CIRCUIT

6.3.1 OFFSET COUNTER

The OFFSET COUNTER has the job in the ADM-3 of counting the number of line feeds that have been issued to the unit. The reason this is needed is that at the time that data is "rolled" upward on the screen (LF code, AUTO NL, etc.) there is actually no data movement in the refresh memory. Once a code is written initially into memory in the ADM-3, it physically remains in the same cells until the time it is "moved" off the top line of the display. It is for this reason that the number of times the screen has been rolled must be remembered. The OFFSET COUNTER (74161, D9, zone C3), in the 24 line mode, counts from zero after power on clear to a maximum count of twenty-three and recycles to zero. In the 12 line mode, the OFFSET COUNTER only counts on the odd numbers between zero and twenty-three. The three inputs affecting this counter are as follows. First, a LINE FEED code received from the line increments the counter by one. (Two in the case of a 12 line unit.) The signal BOFLO, entering the OFFSET counter circuit at D2-11 (zone C4), can also increment the counter by one or two depending on the 12/24 line switch. However, this signal, originating at D3-4 (zone B1), is active only if the AUTO NEW LINE function switch is "on". The input to the OFFSET counter circuit is also active if the START flip-flop C5-9 (zone D4) becomes set. This flop sets only if a CLEAR SCREEN operation is activated by the receipt of a CLEAR SCREEN code or the simultaneous depression of the SHIFT and CLEAR keys. The combining of these two activating signals is accomplished in the 7432 C2-6 (zone D4) which goes to the "J" input of the START flop. The START flop clears when the OFFSET counter overflows at the transition between count 23 and count 24.

This overflow condition occurs when OCLOD (7420, D8-8, zone C2) goes to the low state. The clearing of the memory occurs in the following manner. Upon receipt of the CLEAR SCREEN code and the setting of the START flop, the OFFSET COUNTER is cleared. Write pulses are then generated at the normal video addressing rate, eighty per horizontal raster scan. At the end of each raster scan, the OFFSET COUNTER is incremented once or twice, depending on the 12/24 line switch. Therefore, a 24 line display is cleared in approximately 24 raster times or in about 1.5 msec.

Any erasing of data from the display memory is accomplished by setting the flip-flop C5-5 (74S113, zone D2) labeled ERASEF. This flop sets when the input to the OFFSET COUNTER is enabled and is cleared when the START flop clears. Therefore, when the OFFSET COUNTER is moved by either LINE FEED or BOFLO, which produces one line roll, the ERASEF stays on for only one raster scan and erases only one line. It clears after this one raster scan because the START flop was never set. However, if the ERASEF was set because the START flop was also set (clear screen operation) then the ERASEF will not clear until OCLOD and START both go low.

Gates C4-6, 8, and 11 (7400, zone D2) all work to allow the generation of the proper number of write pulses to the refresh memory. The actual duration of the write pulse is derived from the output of flop D5-8 (74S113, zone D1). (See timing diagram.) The flip-flop D5-6 (74S113, zone C1) labeled NO LD SPACE is there to accomplish the non-destructive space code feature. This feature allows the writing of a SPACE code into the refresh memory between the receipt of a LINE FEED code and the next CARRIAGE RETURN code. The writing of this octal 040 code is inhibited between the receipt of a CARRIAGE RETURN code and the next LINE FEED code. This allows the computer or the operator to write a format on the screen, issue a CARRIAGE RETURN and space over the previously written data since the writing of the code is inhibited but the cursor still advances. Notice that a switch is provided to inhibit this feature if desired.

6.3.2 CURSOR REGISTER

The bottom half of this schematic is the CURSOR register (C11, C12, 74193, zones B2 and B3). This register keeps track of the position of the cursor on the bottom line and is composed of two up/down counters to allow backspacing. Gate F3-8 (7425, zone B4) decodes the condition for which the cursor will forespace during normal operation. CC80 (F3-13 is the actual clocking term and is used to time the forespace operation properly. This term occurs once every horizontal raster scan, has a width of 643 nsec, and occurs during the first character time of the horizontal border time. (See timing diagram.) The term DOIT tells the forespace circuit that the data input buffer has a new code that requires action. The forespace is inhibited if the code received is a CONTROL code (F3-12) or the DEL code (octal 177, F3-9). This

pulsed signal reaches the CURSOR register through the 7402 (D3) located in zone B4. The other means by which the cursor can be incremented is during a READ BACK operation which is normally used for test only. This is accomplished by D3-10 (7402, zone B4). The signal on D3-9 is low only during this read operation and is called READ. XLOAD on D3-8 goes low when the code under the cursor has been loaded into the transmit section of the UART and the cursor can be incremented in preparation for the transmission of the next character.

The down clock input of the CURSOR register (C12-4, zone B3) is simply the decode of the BACKSPACE control code (USASCII BS, octal 010).

The gate E6-12 (7410, zone B3) combines the three ways that the cursor register gets cleared. The first way is the decoding of a CARRIAGE RETURN code in the input data buffer. The function of this code is to return to the "home" position (lower left corner of the screen). This decode is or'ed in at E6-13. The next way to clear the CURSOR register is the signal called UNDERFLOW entering this circuit at E6-1 and originating in zone B1. This signal is an indication that a BACKSPACE operation was attempted from the "home" position. The ADM-3 does not do a wraparound operation when this is attempted and remains in the "home" position. Therefore, when the UNDERFLOW flop (7474, B4-9, zone B1) sets, the CURSOR register is cleared to maintain the previous location of the cursor. The last way to clear the CURSOR register occurs at E6-2. It is cleared when the START flop sets (zone D4). This accomplishes two things: (1) The cursor is initialized when a clear screen operation is initiated and (2) power on clear also "homes" the cursor.

The gate C4-3 (7400, zone A2) decodes the fact that the cursor has been incremented beyond the end of the line and is labeled WC = 80. This information is latched into flop B4-6 (7474, zone A1) which is called OVERFLOW. When OVERFLOW rises, the preset inputs to the CURSOR register go low thereby loading information from the parallel inputs into the register. The information that is loaded depends upon the position of the AUTO NL switch located in zone B1. If this switch is closed (AUTO NL enabled), then the CURSOR register will preset to zero and the screen will roll. Therefore, with the switch in this position, typing into the last location on a line will automatically roll the screen and home the cursor. If the AUTO NL switch is open (AUTO NL disabled), the register will preset a binary 79 (last position) and the screen will not roll. Therefore, with the switch in this position, further typing will overwrite the last position of the line and the cursor will not move.

6.3.3 BEEPER Circuit

The last function on this sheet is the BEEPER feature. The actual sound is created by putting one of the system counts (LC2, F1-12, 74H01, zone A2) through a speaker (zone A2). The duration of the "beep" is governed by the one-shot (D1, 74123, zone A2). Gate D2-6 (7427, zone A3) triggers the one-shot if a character is being written into the 71st position of the line which is used as a line end warning. Gate J3-3 (7400, zone A3) triggers the one-shot if the USASCII BEL code has been received into the data input buffer. Gate D3-1 (7402, zone A3) controls the clear input to the one-shot. The signal READ clears the 74123 through input D3-3 and is present because the initiation of the READ BACK feature is triggered with the receipt of a BEL code which normally initiates the beeper. Therefore, to avoid the noise, the one-shot is disabled when the READ BACK is started.

The OVERFLOW signal also clears the beeper one-shot because when operating at a rate higher than 2400 baud and writing an entire screen of data, the beeper one-shot never clears unless this signal is present. This is because when a character is written into the 71st position, the one-shot triggers because of the signal LINE END. Before the 74123 can time out, the 71st position of the next line is reached and the one-shot is retriggered. Therefore, a continuous beep would be heard for the entire duration of the transmission from the computer. At lower baud rates, the duration of the sound is normal.

6.4 SCHEMATIC SHEET #4 — MEMORY ADDRESS GENERATION

This sheet provides all of the memory address manipulation required by the ADM-3. The two 74157's (F11 & F12) located in zones A3 and B3 multiplex the addresses corresponding to the position in the line. The "A" inputs of the 2:1 multiplexers come from the CURSOR registers. This set of inputs is primarily utilized when there is a character to be loaded into the refresh memory from the data input buffers. The CURSOR register outputs are also gated to the memories when the refresh memory is being

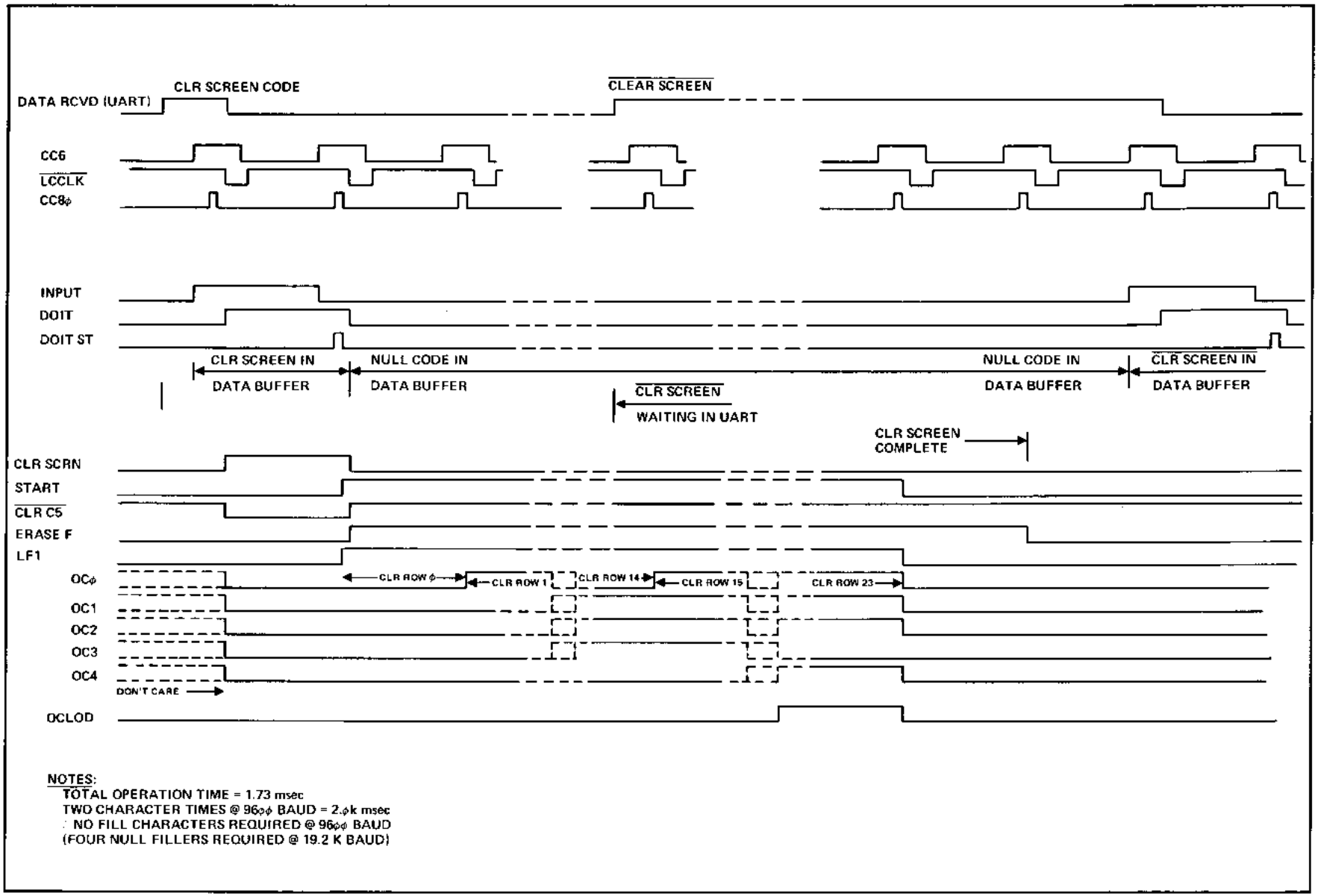


Figure 6-6. Clear Screen Timing

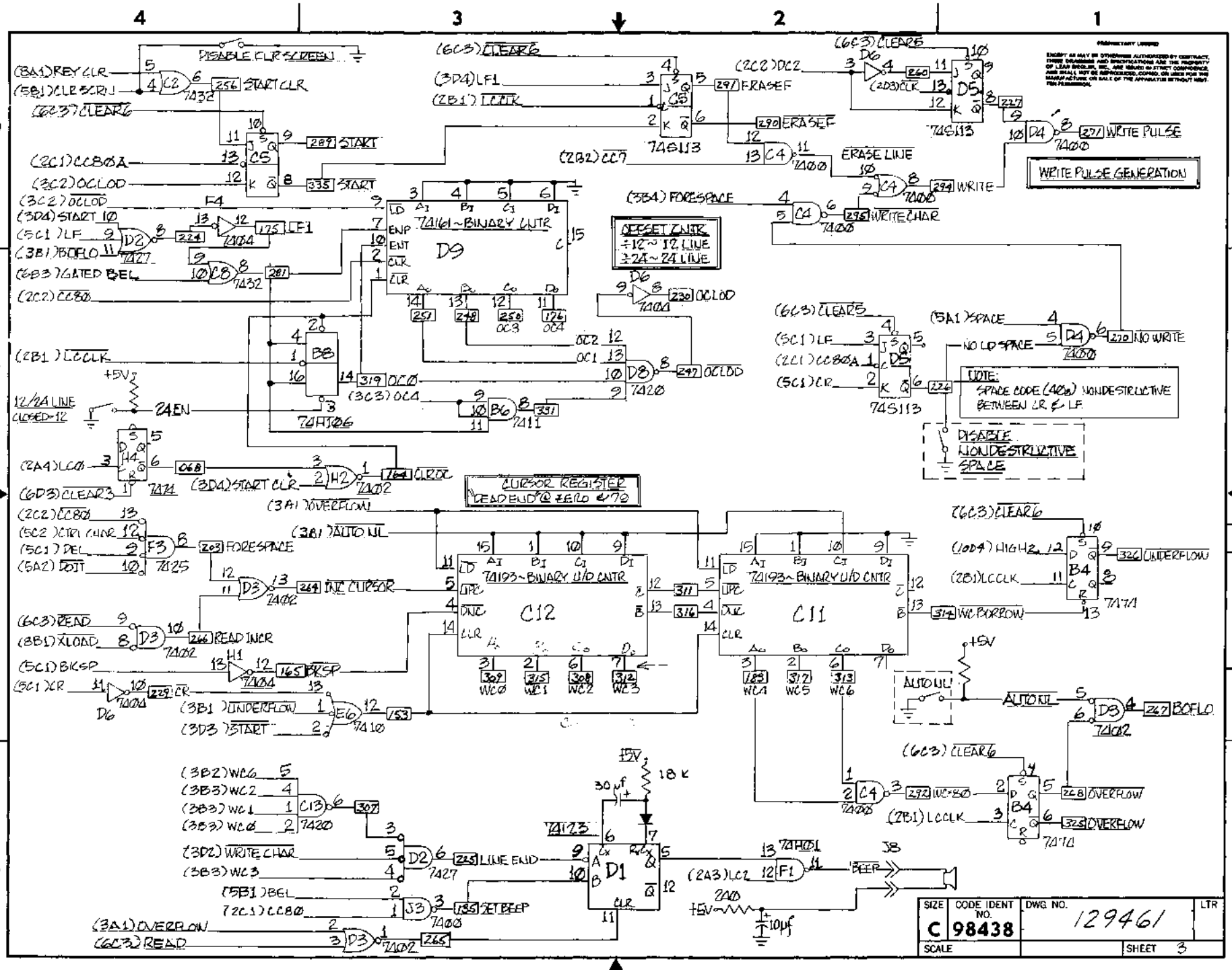


Figure 6-7
6-10

read using the READ BACK feature in test. The "B" inputs to the multiplexer come from the CHARACTER POSITION counters. This set of inputs is primarily used to provide data to the character generators during screen refresh time. However, they are also utilized when there is an entire line to be erased to SPACE codes. The selection of addresses is accomplished through gate C10-10 (7402, zone B4). The CURSOR register outputs are sent to the memory when either of the inputs is high. The signal CC7 (C10-9) designates the horizontal border time which is when any input operation takes place. When the READ flop is set, the CURSOR outputs are also enabled. This is an unconditional gating term, therefore, no video is generated on the screen while the unit is in the READ BACK mode.

The 74157 located in zone C2 (F9) is used to multiplex the character line count for video display which is the "B" inputs, and the character line count for character loading into the refresh memory ("A" inputs). Notice that the "A" inputs for character loading come directly from the OFFSET counter. Remember that the offset counter counted the number of LINE FEEDS accomplished by the unit. In practice, the OFFSET counter holds the virtual address which points directly at the bottom line on the screen. Remember that on the ADM-3 the cursor never moves off the bottom line of the display. The character line address for video display is created in the following manner. The full adder (7483, zone D4) E9, in conjunction with the 7432 (C8, zone C4) and the 7486 (C7, zone C4) essentially sums the OFFSET counter and the ROW counter.

Adder out = OFFSET plus ROW plus 1

The +1 in the equation is there because in a display, ROW=0 is normally the top of the screen and in the ADM-3 ROW=0 is at the bottom. Therefore, in an initialized ADM-3, the top row is really ROW=1. Therefore, looking at the equation above, imcrementing the OFFSET counter once from the initialized state effectively makes the address of the bottom line on the display change from ROW=0 to ROW=1 and the top line change from ROW=1 to ROW=2. Therefore, it can be seen that simply incrementing the OFFSET counter accomplishes the normally time-consuming roll operation in "zero" time. It can further be seen that once a code is written into the refresh memory, it never has to be moved. The second adder (E8, 7483, zone D3) provides for the fact that the sum out of adder E9 can exceed the maximum line address of 23. The second adder then changes an input of 24 to an output of 0, 25 to 1, etc. Gate E4 (7408, zone D3) detects addresses between 24 and 31 and gate F8 (7432, zone D3) combines this information with the detection of sums of 32 and greater. The actual operation accomplished in full adder E8 is that if the first sum is equal to 24 or greater, forty is added to it to create a legal sum. For example, if the first sum is 24 which is illegal, the adder out would be 24 + 40 = 64. Since the 64 weighted bit is not looked at by the memory, the address created would be 0. (See chart labeled MEMORY ADDRESS MANIPULATION.)

The 74157 (F10, zone B1) and the two 7432's (f8-8, 11) located on the right side of the schematic account for the fact that the line length in the ADM-3 is a non-binary number (80). Therefore, if the line and position address was sent directly to the memory, it would take a 4K memory to hold the 1920 bytes required for a 24 line by 80 character display. Therefore, what these parts accomplish is to essentially make the ADM-3 a 30 line by 64 character display. In this manner, the binary line length allows the addressing to "fill in the blanks" and make maximum utilization of the 2K bytes available. The organization of this 30 by 64 screen is shown on the next page. Notice that the last 16 characters of each line reside in a different row than the first 64. The reason that rows 24 through 29 are on every other line is for the 12/24 line option. The odd rows must remain odd throughout the entire line.

Normally, during the multiplexing of the two address sources (74157's, F9, F11, F12) are not mixed. That is the character loading position address (WC) remains with the character loading line address (OC) and the refresh position address (CC) remains with the refresh line address (SUM). However, there is one operation where the refresh position address (CC) is used in conjunction with the character loading line address (OC). This happens when the bottom line of the screen is to be erased (ERASEF low, F11-13, zone B3). This happens for one raster scan during a roll operation and multiple scans when the screen is cleared. This combination is accomplished by essentially driving the character line select input with the ERASEF signal (F9, zone B2). Write pulses are also generated to the memory during the appropriate raster scans.

6.5 SCHEMATIC SHEET #5 — DATA RECEIVER/DECODER

There are three data sources for the input section of the ADM-3. The signal labeled XDATA

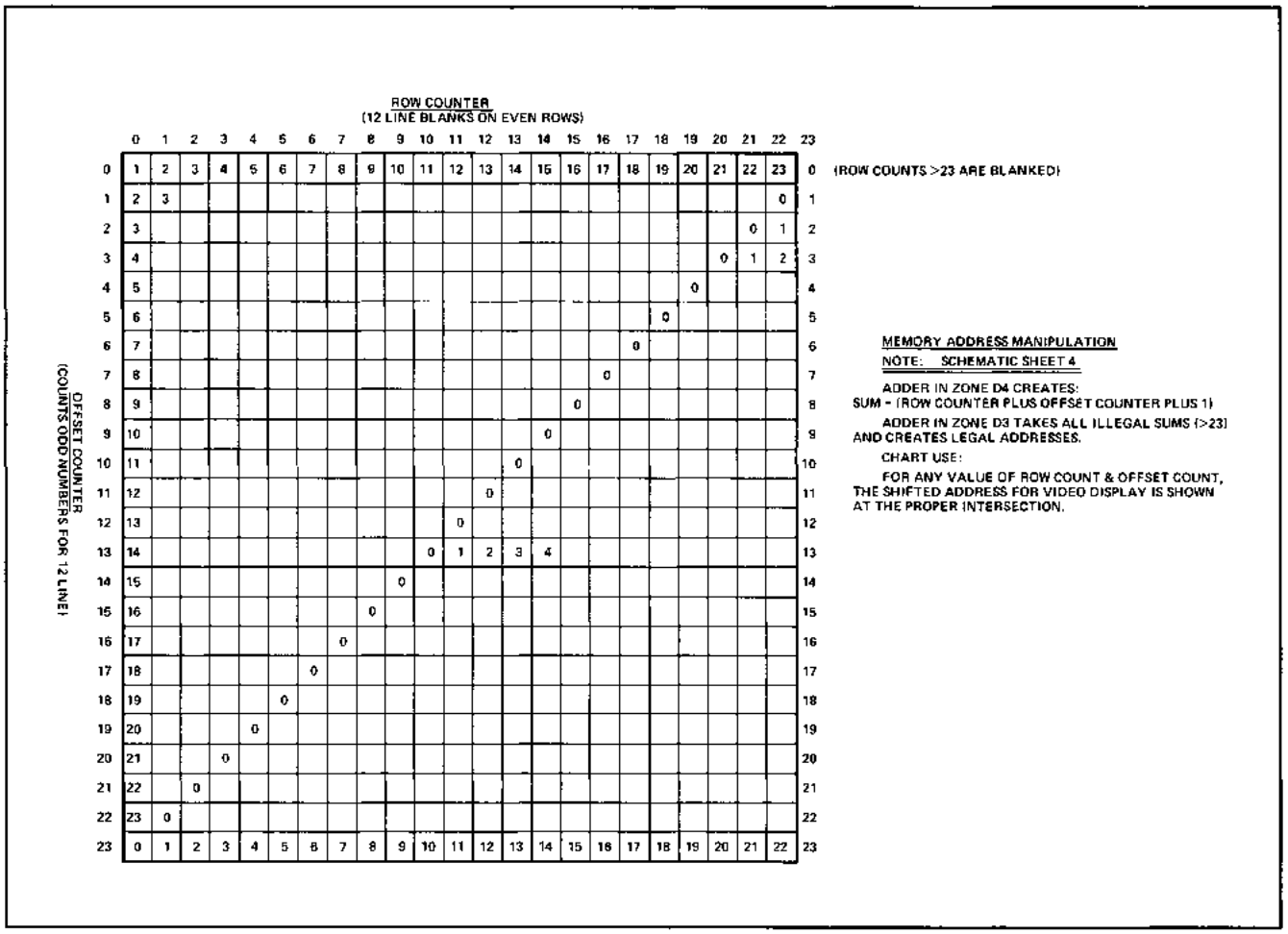


Figure 6-8. Manipulation of Display Address

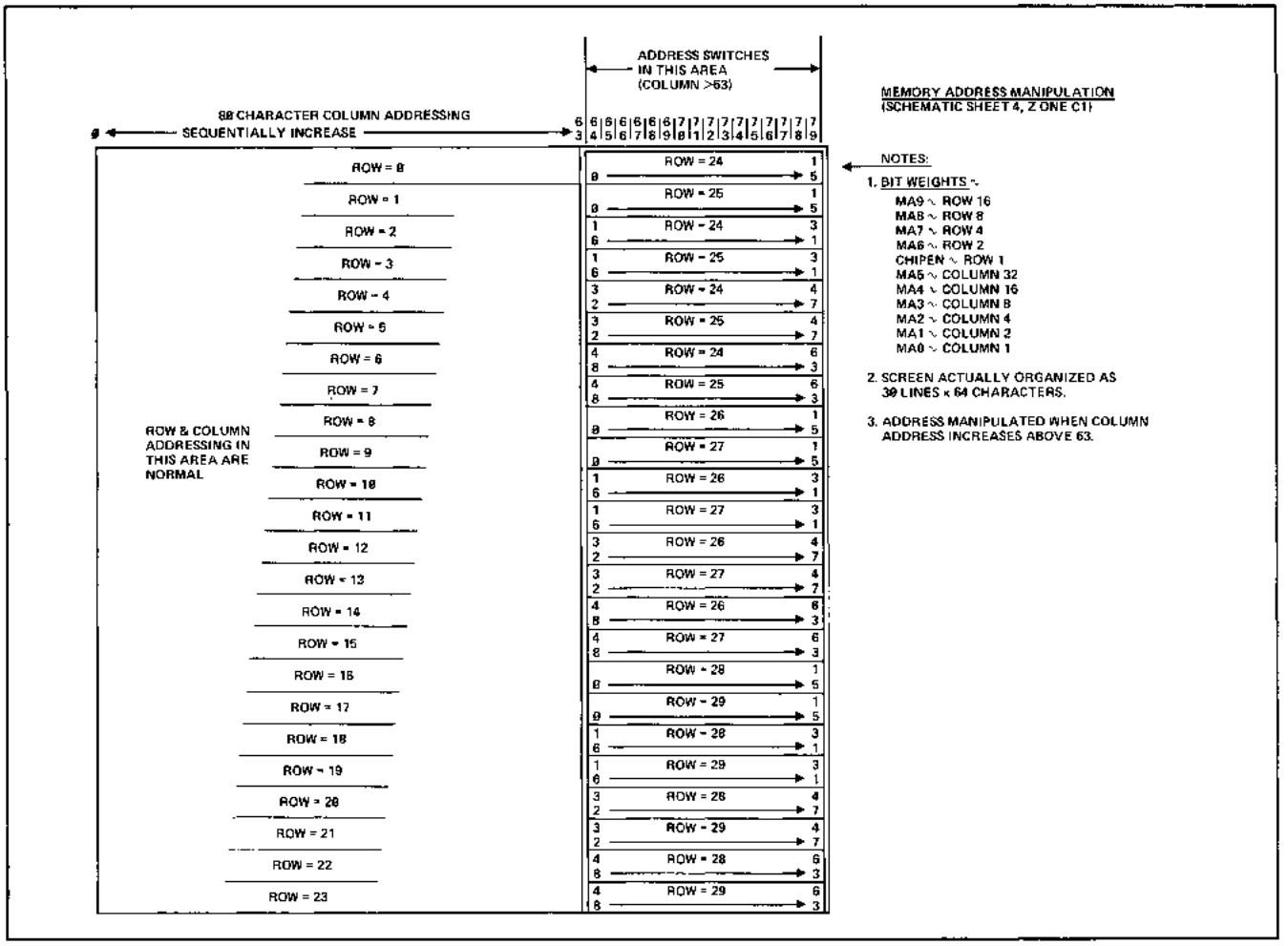


Figure 6-9. Organization of Display Data in Refresh Memory

(zone D4) is actually the data being transmitted out of the unit and normally originating from the keyboard. This signal can be coupled to the input section via the HDX (half duplex) switch. Therefore, in the HDX mode, every code transmitted out of the unit is sent to the receiver and is indistinguishable from a code sent in from the computer. This HDX data path remains as a TTL level and is never shifted to the RS232 voltage levels. The second data input path to the unit originates at the main I/O connector and is the normal RS232 received data line. This signal is level shifted through a 1489 (A9-3, zone D4) and is combined with the HDX feedback signal at the 7411 (E3-10) located in zone D3. The last input data source comes from the current loop receiver located on sheet 9, zone D1 and is labeled CL DATA. This signal enters the data path at E3-11 (zone D3). Therefore, the signal created at E3-8 (zone D3) is the combination of all the data sources regardless of origination that the ADM-3 will see. This signal is level shifted through a 1488 (A5, zone D2) and is sent to the extension port. The same signal is also sent to the UART, pin 20 which is the serial data input (zone C4). The receiver section of the UART is located in zones A4, B4, and C4. The two additional inputs to this receiver section are the RECV CLK originating at 10B1 and DOIT coming from this sheet, zone A2 and utilized as the data received reset (DRR). Note that the three error conditions (PARITY ERROR, FRAMING ERROR, and OVERRUN ERROR) are ignored in the ADM-3. Therefore, there are nine outputs used out of the UART. The first eight are the parallel data lines of which RR8 (MSB of the input word) is essentially ignored although it is sent to the input data buffer K4-4 (zone C3). Notice that the outputs K4-2 and K4-3 are unused and are open. The other seven data lines (IN1 to IN7) are sent to the input data buffers (74175, L4, zone B3) (74175, K4, zone C3) and are latched when the data received signal out of the UART is recognized. This data received signal (DR, pin 19, zone A3) is sampled by flip-flop H4 (7474, zone A3) once every horizontal raster scan time (61.728 sec) utilizing signal CC6 which originates at 2B2 (see overall timing diagram). This DR sample is then timed for actual execution by flip-flop H3 (zone A2) which clocks on with LCCLK and generates the signal DOIT. This flip-flop output will remain high for one horizontal raster time (61.728msec) and designates the time to accomplish the received command.

The data input buffers hold the code received from one of the previously designated data sources and is decoded by the rest of the circuitry on this sheet. The three least significant bits are decoded through the 7442 (L3) located in zone B2. Notice that the D input is used as a chip enable and has the signal DOIT. Therefore, no decodes are available until the actual execution time. Bit 4 of the input data word goes directly to the 7427's used in the final decodes. Bits 5, 6, and 7 are combined to decode a control character and a column 0 character. The control character (columns 0 or 1) is recognized at the 7402, located in zone C2, and labeled CTRL CHAR (zone C2, H2-10). The column 0 code is decoded by J3-6 (7400, zone C2) and labeled COLUMN 0. Column 1 codes are recognized by gate J3-8, a 7400 located in zone B2 and labeled COLUMN 1. All of these decodes are combined properly in the 7427's located down the right side of the page to completely decode all of the codes recognized by the ADM-3. The DEL code (J2-12, zone C1) is created to specifically exclude this code from entry into the memory. This is done because the DEL code is not normally used as part of data but is recognized by the computer for other purposes. A complete decode is done because all other column 7 codes are used as normal data. The CR, LF, BKSP codes are decoded for obvious reasons. The BEL decode is decoded for the normal activation of the bel circuit but also has another use in the ADM-3. This code is used to activate the READ BACK feature that is used for internal LSI testing only. This feature will be explained in further detail on a later page. The signals labeled LOCK and UNLOCK are used to control the KEYBOARD LOCK flip-flop located in zone D1 of this sheet. The code used to unlock the keyboard is an USASCII SO (octal 016) and the code used to lock is an USASCII SI (octal 017). The CLEAR SCREEN function is activated by USASCII SUB (octal 032). The SPACE decode is created in H2-4 (7402, zone A1) to recognize this code for the nondestructive cursor feature. The USASCII ENQ is used to activate the ANSWER BACK option (if installed). This decode is combined with the depression of the HERE IS key on the keyboard schematic (sheet #8).

The flip-flop located in zone D1 is used to control the locking and unlocking of the keyboard circuit. Notice that there is a switch on the LOCK input to disable this feature if the particular application dictates that the USASCII SI code be used for other purposes. There are two ways to unlock a previously locked keyboard. The first is the receipt of the USASCII SO code. The keyboard can also be unlocked by the simultaneous depression of the SHIFT and CLEAR keys which generate the signal named KEY CLR.

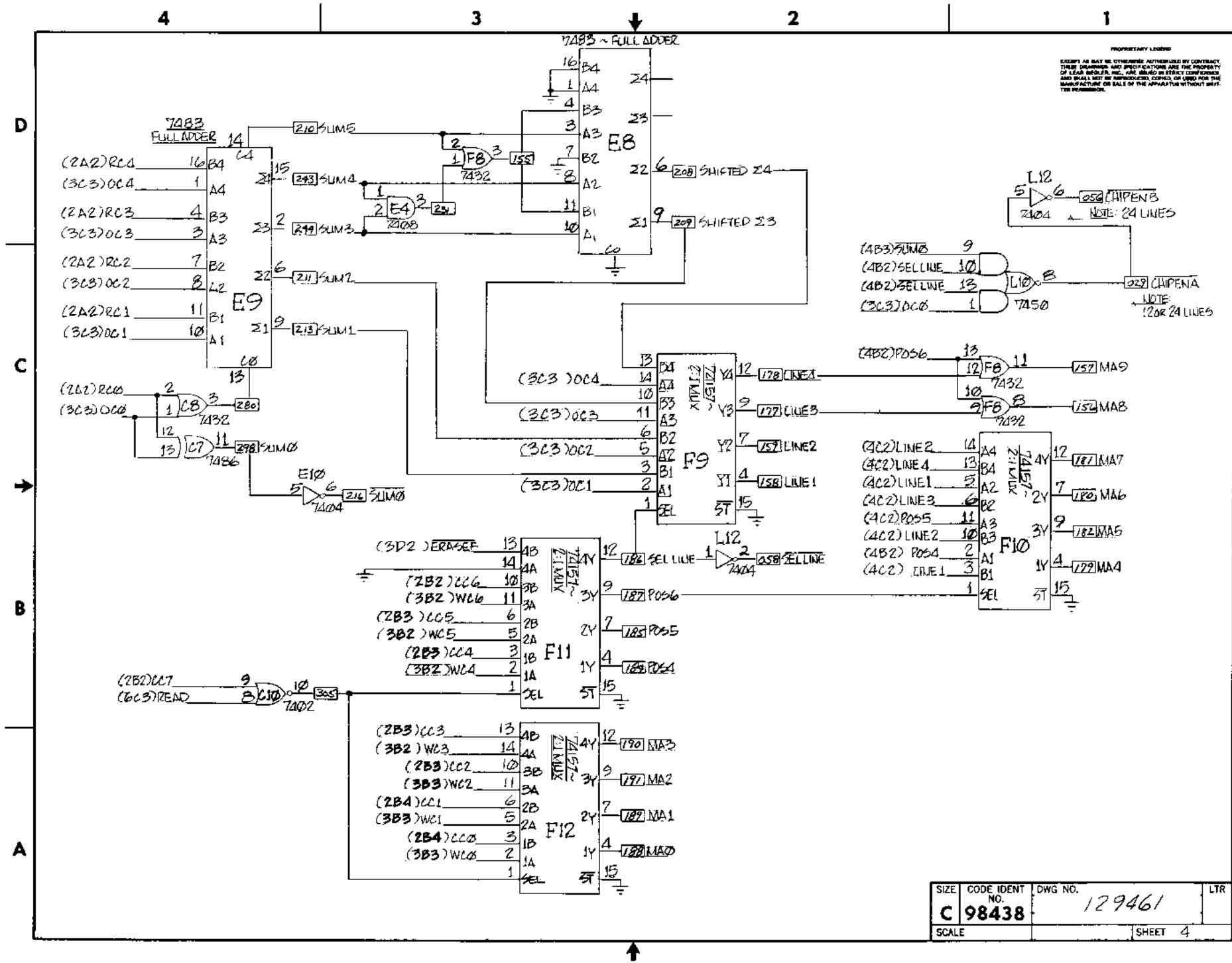


Figure 6-10
6-15

6.6 SCHEMATIC SHEET #6 — CLEAR CIRCUIT READ BACK MONITOR DRIVE SIGNALS CURSOR GENERATION

6.6.1 CLEAR Circuit

The 74123 (retriggerable one-shot, D1,) located in zone D4 provides the power on clear signal. The RC circuit is connected to the positive trigger input. Therefore, when the power is up and the capacitor finally charges to the input threshold, the one-shot triggers off and creates the reset signal. This unit is unusual in that every single storage element in the system is reset with the CLEAR pulse except for the refresh memories. This was done to accommodate the automatic board testers. The signal labeled TESTER INITIALIZE, entering the circuit at D4-1 (7400, zone C3) accomplishes the same function as the power on clear except that the signal is generated by the automatic tester. These two clearing sources are combined at D4-3 (7400, zone C3) and is called CLEAR. A positive level at this point is the clearing level. This signal is buffered through six inverters to create the negative-going CLEAR signal. Each inverter has only 10 loads and they were used instead of a power buffer because of automatic board tester restrictions.

6.6.2 READ BACK

The flip-flop located in zone C3 (B5-6, 74S113) is part of the READ BACK feature. This flop can set only if pin 22 on the main I/O connector J1 is held to ground. READ BACK is a test only feature therefore only internal test cables should have this pin grounded. This function is initiated by issuing an USASCII BEL code (octal 007) through the normal data input which sets this flip-flop. The ADM-3 then responds by sending all data on the top line of the display from the cursor position to the end of the line inclusive. The screen is rolled one line but the data remains on the screen and the bottom line is not erased. The cursor remains on the last character position transmitted which is the last position on the line. The READ flip-flop is cleared at the end of the operation when the CURSOR register overflows.

6.6.3 MONITOR DRIVE Signals

The monitor drive signals, HDRIVE and VDRIVE are generated in zones C1 and D1. The horizontal drive signal, HDRIVE never moves regardless of the position of the 50/60 Hz selection switch. However, the VDRIVE signal changes between 50 Hz and 60 Hz refresh in order to maintain the same relative position of the video display on the display screen. (See the MAIN TIMING DIAGRAM for the positioning of these drive signals.

6.6.4 CURSOR Generation

The circuit at the bottom of this schematic generates the cursor position for the video presentation on the display screen. It uses only two 7485 comparators because the cursor can only reside on one line of the display. It essentially compares the CURSOR register (WC) against the dynamic value of the CURSOR POSITION counters (CC). This comparison is really two character times before the actual display times since the system counters are always two character times earlier. Therefore, the two flip-flops (B12-5 and B12-9, zone A1) delay the compared output by two character times before the video cursor is generated. The flop B11-6 (7474, zone A3) labeled CUR STOP and gate B10-8 (7408, zone A3) combine to position the cursor display on the proper two raster lines. This occurs below the bottom line of the screen.

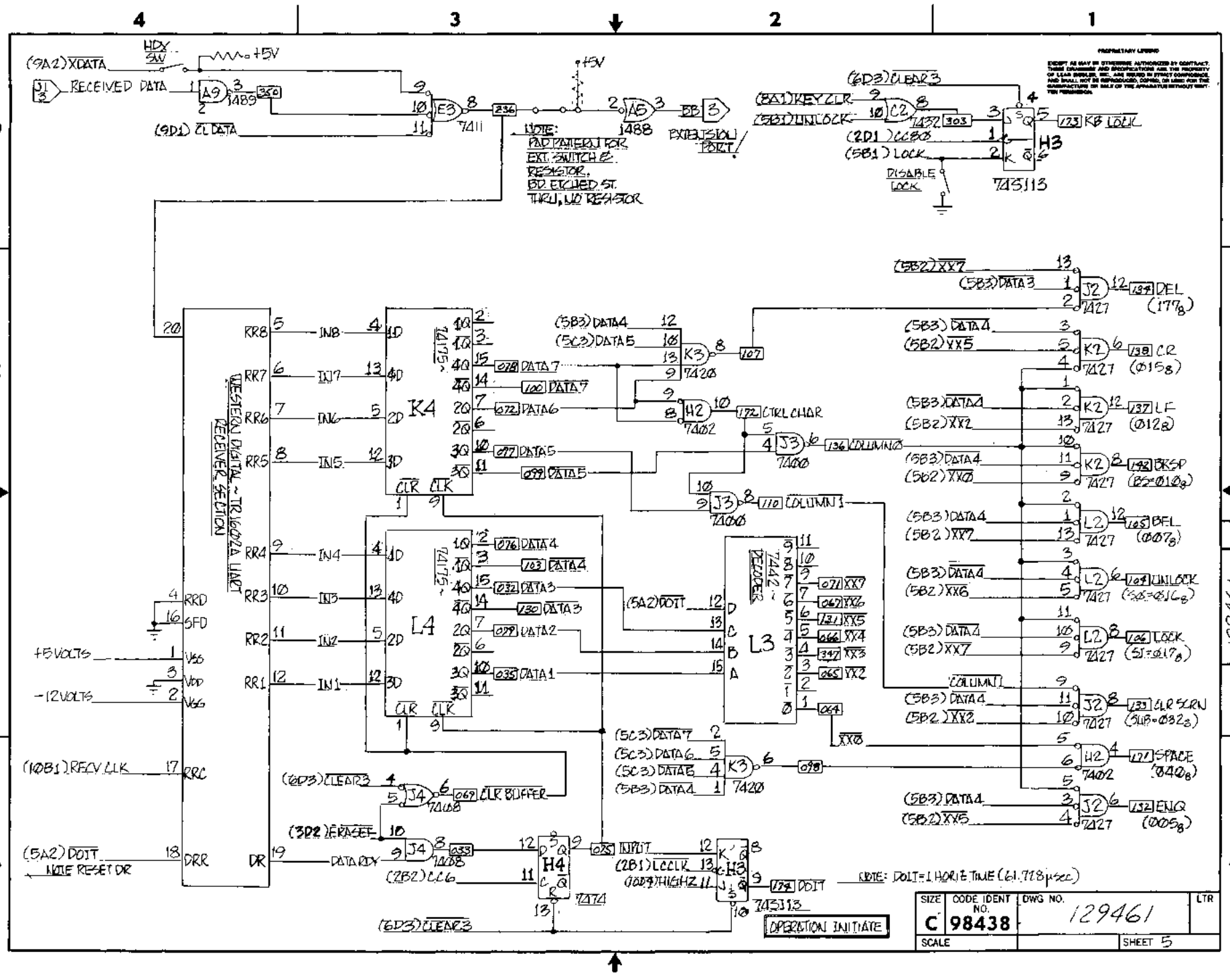
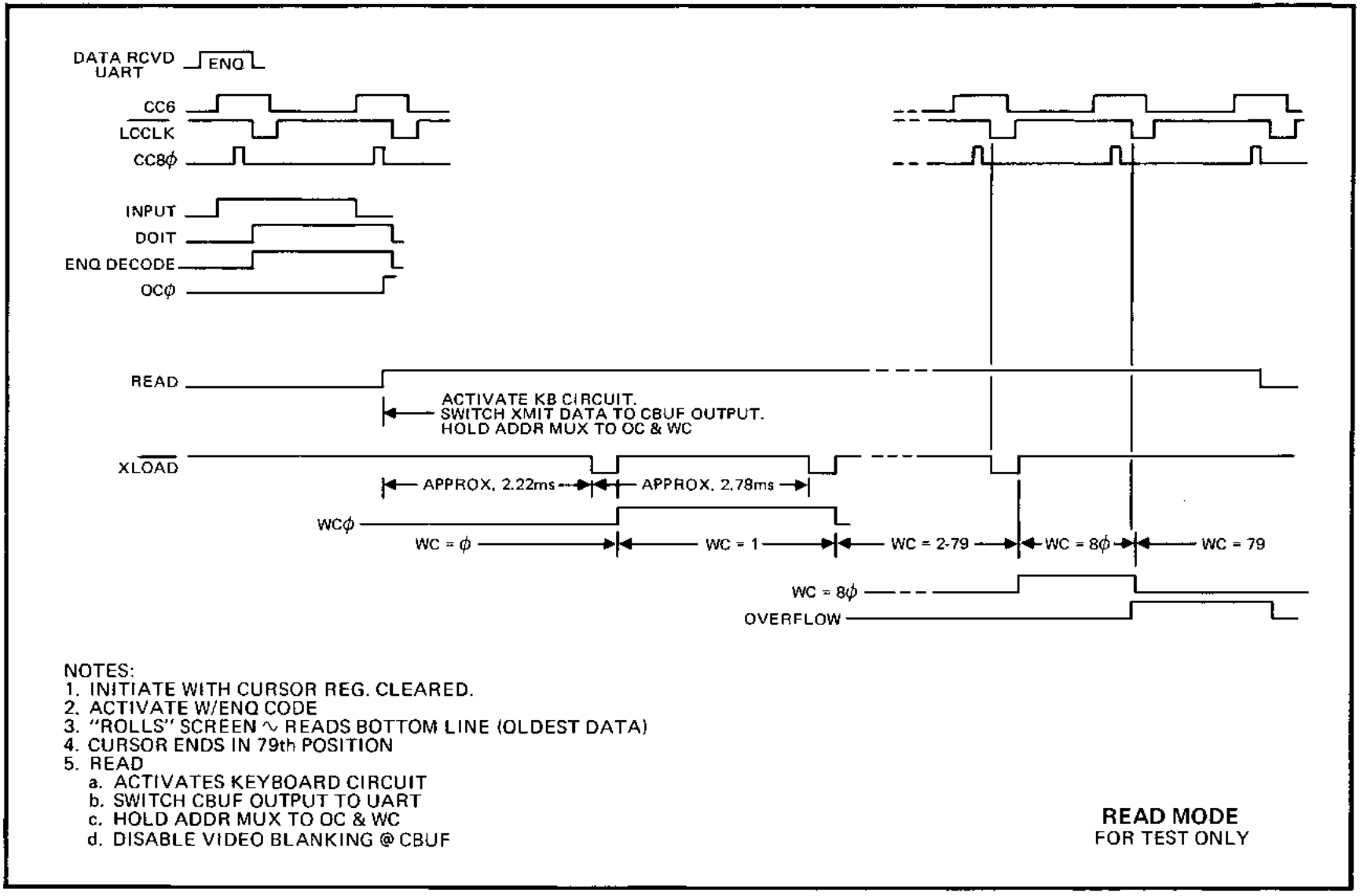


Figure 6-11
6-17



NOTES:
1. INITIATE WITH CURSOR REG. CLEARED.
2. ACTIVATE W/ENQ CODE
3. "ROLLS" SCREEN ∿ READS BOTTOM LINE (OLDEST DATA)
4. CURSOR ENDS IN 79th POSITION
5. READ
   a. ACTIVATES KEYBOARD CIRCUIT
   b. SWITCH CBUF OUTPUT TO UART
   c. HOLD ADDR MUX TO OC & WC
   d. DISABLE VIDEO BLANKING @ CBUF

READ MODE
FOR TEST ONLY

Figure 6-12. Read Mode

6.7 SCHEMATIC SHEET #7 — REFRESH MEMORY CHARACTER GENERATORS VIDEO SERIALIZER TRANSMIT DATA MULTIPLEXERS

6.7.1 Refresh Memory

The refresh memory is composed of 14 - 2101 RAMs which have 500 nsec access times. These RAMs are organized as a 2K by 7-bit memory which hold the 1920 USASCII codes for screen refresh. There are four configurations of memory in the ADM-3. The first configuration is six RAMs which is used for the upper case only, 12 line display. Then seven RAMs are used for the upper/lower case, 12 line version. Twelve RAMs are required if upper case only, 24 lines. Then all 14 rams are installed if the fully configured upper/lower case, 24-line combination is desired.

The move between 12 and 24 lines is made with a switch located on sheet 3, zone C4. Zone A4 of this schematic has the switch labeled UC EN which switches the unit from upper case only to upper/lower case display. The 74157 sections located in zones C4 and C3 (2:1 Mux, H7) alter the data properly for 7 bit USASCII to 6 bit USASCII for upper case only display. The output H7-9 (zone C4) selects between two sources for bit 6 storage. Upper case only display utilizes DATA7 while upper/lower cases uses DATA6. Gate F8-6 simply forces bit 6 to a high level when the ADM-3 is erasing a line. This converts the NULL code coming in to a proper SPACE code. The 7486 in zone C4 (k9-3) has the function of being able to clear the memory to zeros with the activation of a switch located internally but normally not installed.

6.7.2 Character Generators

The circuitry located above the refresh memory is used to blank the video display at selected times. This function is normally accomplished at the video serializer but was placed here to allow the automatic board tester to shut the video off without affecting the character generators or the video serializer.

The horizontal blanking is accomplished with gate C10-1 (zone D4, 7402). The term RC5, entering the circuit at C10-5 does the blanking for row counts 32 and higher. This signal is active only if the unit is operating at 50 Hz since the 60 Hz units reach a maximum count of 29. The term RC=24/31 accounts for the blanking immediately below the video and up to row count 31. Gate C8-11(7402, zone D4) generates the term that blanks every other line if the ADM-3 is operating in the 12 line mode. The combined blanking term, called VIDEO BLANK and going to the clear inputs of the two 74175's (H6 and J6, zones B3 and C3) used as the character generator input buffers, is generated in the flop F6 (7474, zone D3). Notice that clearing the CBUF registers does not present a NULL code to the character generator inputs. The outputs associated with bit 6 are inverted. Therefore, when VIDEO BLANK is active, the CBUF outputs present an USASCII SPACE code to the character generators.

The two character generator ROMs are rather straight forward. The upper case ROM is a standard masked part (2513) but the lower case ROM is a custom masked part. The one unusual thing about this is that all of the address lines into the lower case character generator are inverted.

6.7.3 Video Serializer

The video serializer used is a 74166, eight bit shift register which is preset once every 643 nsec and shifted at an input clock rate of 10.8864 MHz. Gate E2-3 (7400, zone A1) is used to blank the video during a READ BACK operation. This is required because the CBUF registers are used to send memory data to the transmit UART without regard to its effect on the video display. Since the result is quite unusual, this gate was installed. Gate F1 (74H01, zone A1) is used as the video driver and is also the point at which the video cursor is ORed in.

6.7.4 Transmit Data Multiplexers

The two multiplexers (74157, K6 and L6, zones D1 and D2) are used to select between keyboard or refresh memory as the source of the data going to the transmit UART. The refresh memory is selected during the READ BACK operation and the keyboard output is selected at all other times.

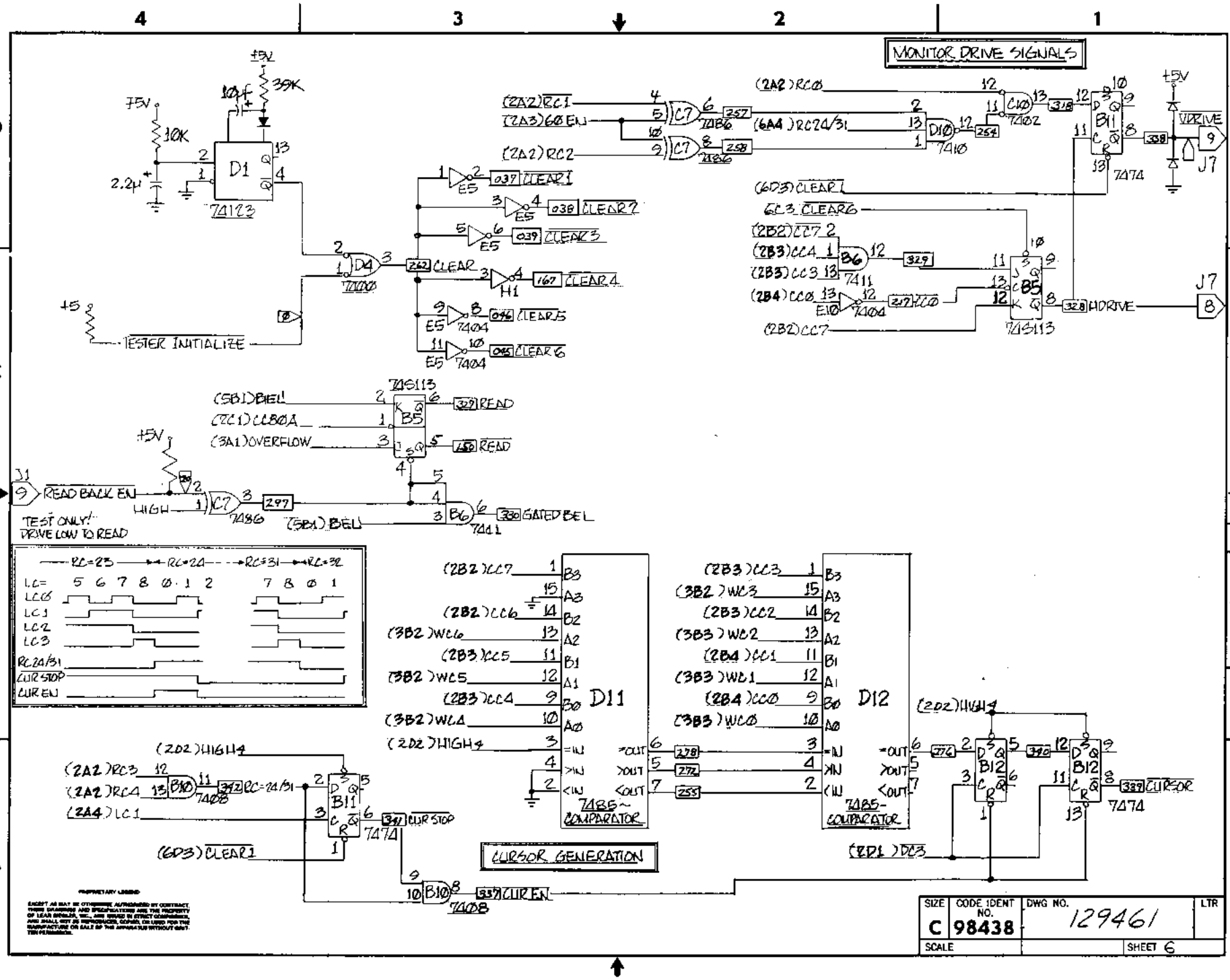


Figure 6-13
6-20

SIZE	CODE IDENT NO.	DWG NO.	LTR
C	98438	129461	
SCALE		SHEET 6	

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6.8 SCHEMATIC SHEET =8 — KEYBOARD CIRCUIT

The keyboard is encoded utilizing a normal scanning-type circuit. The two counters (7493) located in zones D3 and D4 clock through all possible 128 USASCII codes. The four least significant bits are decoded through the 1 of 16 decoder (74154-L8) whose outputs appear as one side of the encoding matrix. The three most significant bits, K5 through K7, operate the selection inputs of the 8 to 1 multiplexer (74151-L9). The inputs of this multiplexer represent the second side of the encoding matrix. This encoding matrix has a direct relationship with the USASCII code chart. The outputs of the decoder represent the rows of the chart while the inputs of the multiplexer represent the columns. The key switches are then placed selectively within this matrix on the intersection that generates the lower case code associated with that particular switch.

The detection of a switch closure occurs in the following manner. When none of the keys are depressed (all switches open), the output of the multiplexer L9 is high and the clock (KBCLK) to the code generating counters is running. While KEY DATA is high, the signal labeled GO (zone C1) will be held low, which clears the shift register F2 (zone C2) and holds flop E1 (zone D1) in the key debouncing state. This is the normal idling state with the counters cycling, KEYDATA high, shift register F2 cleared, and BOUNCE high. When an encoded key is depressed, the counters continue cycling until the selected ROW and COL are simultaneously enabled. At this time the low level signal from the row decoder is propagated through the key switch, through the multiplexer, to gate E3 (zone B2) which effectively shuts off the clock to the code generating counters. When KEY DATA goes low, the signal labeled GO is enabled, thereby releasing the shift register and the Bounce flop. At this time the signal BOUNCE is high which enables every cycle of the clock LC3 to propagate through gate E4, located in zone D2, to the clock input of the shift register. This clock (1.800 KHz) determines the length of time allowed for the mechanical key switch to stop bouncing. It allows five cycles of this clock (2.78 msec) to pass before the decision is made that the code is stable. At the end of these five cycles, the signal BOUNCE goes high which does two things. First, the clock input to the shift register is disabled through gate E2 at zone D2. Secondly, the SHIFT/LD line to the shift register is taken to the loading state by gate C2 in zone D2. The circuit is now waiting for one of two things to happen; the key is released or the REPT key is depressed. In the event that the key is released, KEY DATA will immediately go high and the entire circuit will revert to the idling state. If the REPT key is depressed without releasing the first key, the SHIFT/LD line goes to the shift state because of C2-13 (zone D2). Notice now that when BOUNCE went high at the end of the first shift register cycle, the term RCRESET was allowed to gate the clock LC3 effectively cutting its rate to 60 Hz to 50 Hz depending on the position of the 50/60 Hz selection switch. This new clock rate will now determine the repeat rate from the keyboard. The shift register will now shift at the lower rate, generating a load pulse every time DOUT goes high and continuing until the REPT key is released or the primary key is released. The repeat rate is 12.5 char/sec at 60 Hz and 10 char/sec at 50 Hz. The term THRE into gate J4-2 (zone D2) is there to slow the repeat rate if the baud rate selected has a character time longer than the period of the repeat cycle. The terms READ and READ in this circuit are activated by the read-back circuit which is used for internal LSI testing only. In normal operation, the ADM-3 memory cannot be read by the computer. When the read-back is activated, the keyboard control circuit is fooled into thinking that it is repeating a code. The one difference is that the circuit now repeats utilizing the debouncing clock and not the slower clock. The data lines are naturally switched to the memory output which occurs on schematic sheet, 7, zones D1 and D2.

There are three methods by which the code generated by the scanning circuit can be "gidged". First, the depression of the CTRL key (zone A2) unconditionally drives bits 6 and 7 to the low state. This means that the code generated will be driven to columns 0 or 1 depending on the state of bit 5. This is the means by which control codes, not on individual keys, are generated. The next way that the code can be altered is by inverting bit 5. This is used to create the shifted (upper case) codes in USASCII columns 2 and 3. Gate K11 (7400) in zone A4 identifies the code generated as a column 2 or 3 code. Row 0 is eliminated from this shifting because the SPACE code and the ZERO code are not affected by the shift key. This is done at L11-9 (zone A3). The last to alter the code is by inverting bit 6. This is used to shift from the lower case alpha codes in column 6 and 7 to the upper case codes in columns 4 and 5. There are two ways to effect this bit 6 inversion. The normal shift keys and the UPPER CASE ALPHA switch.

The UPPER CASE ALPHA switch is used on systems where no lower case alpha codes are tolerated. Therefore, while in this mode, the

normal SHIFT keys have no effect on the alpha keys. Upper case alpha is always generated. This is accomplished at gate L11 (zone B4). L11-3 and L11-4 decode the fact that the code originates in columns 6 or 7. Notice that in the matrix above, the only codes in columns 6 or 7 are the twenty-six lower case alpha codes. The six remaining non-alpha codes are placed in columns 4 and 5. Therefore, the KC6 KC7 decode in gate L11 definitely picks out only the lower case alpha codes. The normal SHIFT function for columns 4 through 7 is accomplished in gate K11 (zone B4). If KC7 is set, identifying it as columns 4 through 7, and the SHIFT key is depressed, bit 6 is unconditionally inverted.

The CLEAR key, located in zone A2, is utilized in conjunction with the SHIFT key to clear the refresh memory, clear the KEYBOARD LOCK circuit, and clear the I/O interface circuitry. This combination is done in gate K10 located in zone A1.

The BREAK key (zone B3) is used to signal the computer that I/O termination is desired. When depressed, this key has one of two effects, depending on whether the unit is in the transmit or receive mode. If the unit is transmitting when the BREAK is activated, the primary transmit data line (BA, pin 2) is driven to the "spacing" state for as long as the key is depressed. If the unit is receiving data and is in the 202, reverse channel mode, the SECONDARY TRANSMIT DATA line (SA, pin 11) is driven to the "marking" state.

The last function on this sheet is the HERE IS circuit. If the ADM-3 has this option installed, the depression of this key initiates the transmission of a unique message to the computer. This message is contained in PROM in the option and can be up to 32 characters long. This transmission can also be activated with the receipt of an ENQ code from the computer. An ENQ code generated at the local keyboard will not be recognized because of gate K8 (zone A2). The only way an ENQ code can be generated from the keyboard is to depress the CTRL key. Therefore, the simultaneous combination of the CTRL key being depressed and the receipt of the ENQ code identifies it as being locally generated. The signal labeled IDENT (zone A1) goes to the ANSWER BACK pc board through the cables installed at locations K6 and L6.

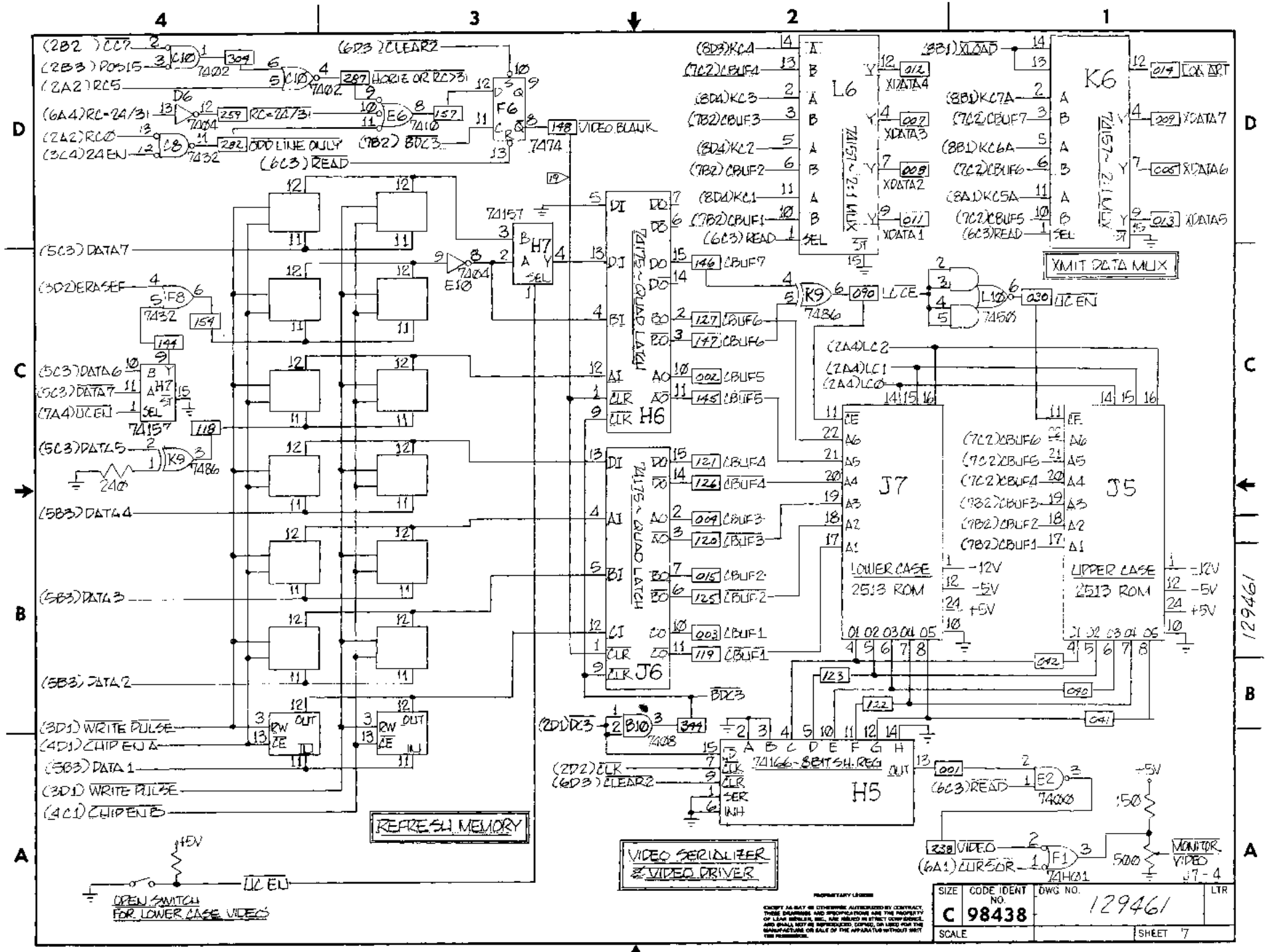


Figure 6-14
6-23

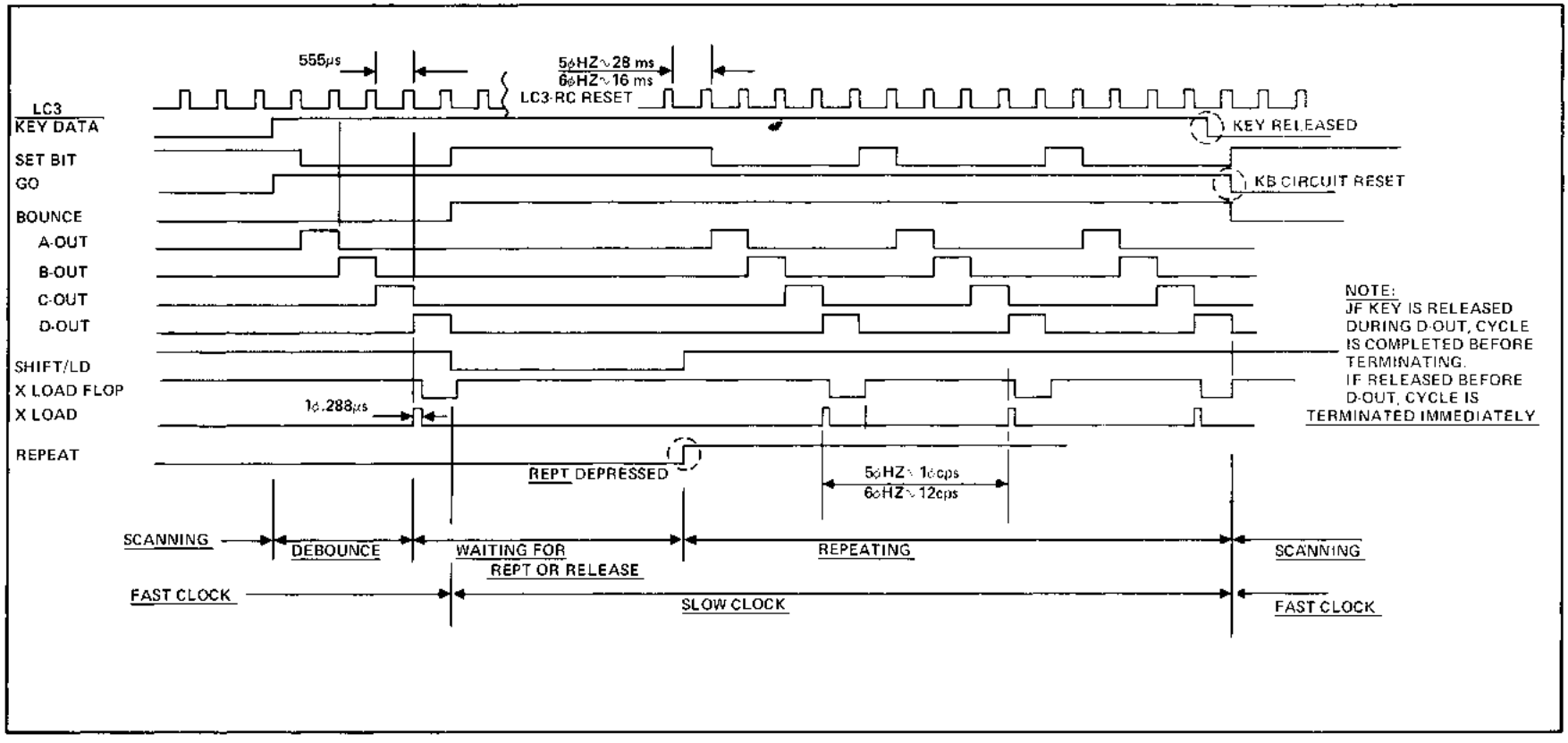


Figure 6-15. Keyboard Logic Timing

6.9 SCHEMATIC SHEET #9 — DATA TRANSMITTER CONTROL SECTION OF UART CURRENT LOOP XMTR/RCVR

6.9.1 Data Transmitter

The transmitter and control sections of the UART are shown on this schematic. Indicated on UART pins 26 through 32 are the seven bits which comprise the USASCII code. XDATA7 is the most significant bit and XDATA1 the least significant. This code to be transmitted to the line comes from one of three sources. In normal operation, the keyboard circuit and the ANSWER BACK option can generate the code. However, during testing the contents of the memory are sent through the UART during READBACK. Pin 40 of the UART is the transmitter clock input. The source of this clock comes from sheet 11 where it is controlled by CLEAR TO SEND (sheet 11, zone D3). If there is no CTS, this input will remain high. In normal operation, the clock on this line will be the same as receive clock input. The frequency will be 16 times the desired transmit baud rate. However, with the split clock option, the transmit and receive rates can be different. The receive rate is always controlled by the main baud rate switches under the cover, while with the split speed option, the little rotary switch in front of the keyboard controls the transmit rate. This rotary switch is accessible only when the unit is open. All baud rates are available on this switch except for 1800 baud. With the split speed option, the selection of 1800 baud as the receive rate limits the selection of the transmit rate to 110 baud. No other baud rates are legal.

Pin 23 on the UART is the loading signal for the transmitter section. The normal state of this line is high and it only goes low when serial transmission of the data present on the XDATA input pins 26 through 32 is desired. The two sources of this loading signal are the keyboard circuit and the ANSWER BACK option board.

Two control signals are utilized from the transmitter section. There are TRANSMITTER HOLDING REGISTER EMPTY (THRE) and TRANSMIT REGISTER EMPTY (TRE). The UART utilized in this unit is buffered on the transmitter data input lines and therefore, when the loading signal is given on pin 23, the XDATA lines are transferred to a buffer register instead of directly to the serializer. When this buffer, called the TRANSMITTER HOLDING REGISTER is loaded, the signal THRE (zone A3) goes low. The transfer of the data from this buffer to the serializer is contingent on the transmitter clocks being present (CTS high) and the serializer being empty. If the serializer is empty, the signal TRE (zone B3) is high. If both conditions are present, the buffer data will be automatically transferred to the serializer on the next clock. At this time, TRE will go low to indicate that the serializer is being used. When both signals are high, the transmitter section is completely empty. These two UART signals are combined to create the "bouncing" REQUEST TO SEND signal selectable on the interface. When either of these signals, THRE or TRE, is low it will cause RTS to be high. Therefore, the RTS signal will "surround" the transmitted character.

The last signal out of the UART transmitter section is, naturally, the serial data. This line marks in the high state and the indication of character starting is this line going low for the start bit of the character. The data bits in the following byte are then sent in a serial manner with the least significant bit first, through data bit 7, followed by the parity bit (if enabled) and the one or two stop bits. The data at this point is "true" data, that is a "one" is indicated by a high level and a "zero" by a low level. This data is then sent through gate E6 (zone A3). E6-4 accepts the signal from the BREAK key shown on drawing 8, zone B3. The depression of this key takes the transmit data line to the spacing (high) state. Input E6-3 accepts data generated by the device connected to the extension port and received by the 1489 EIA receiver A4 (zone A4). This combined data signal (E6-6, 7410, zone A3) is then sent to both the EIA and CURRENT LOOP transmitters. The selection of the transmitter to be used is governed by the switch schematically represented in zone C3 and labeled RS232/CL. This switch is physically located under the little plate next to the keyboard. When the switch is positioned to the left (closed), the EIA transmitter is selected. When one transmitter is selected, the unused transmitter will maintain a marking output to the outside world. Therefore, the RS232/CL switch can be used for "local" operation where data is desired out the extension port but not out of the main I/O port. The transmitted EIA data is level shifted through the 1488 A8 located in zone A1 and out to the EIA connector, pin 2.

6.9.2 Control Section of UART

The control section of the UART is also shown on schematic #9. The MASTER CLEAR is driven high when the UART is to be cleared (pin 21). There are five characteristics of the transmitted

data that can be selected by the toggle switches under the panel. First is the STOP BIT SELECT input on pin 36. When this line is held low, one stop bit will be attached to the transmitted byte while a high signal will select two stop bits. The next input controls the WORD LENGTH SELECT. A high input selects an 8 bit data word while a low level selects a 7 bit data word. UART pin 39 is EVEN PARITY ENABLE which it would do if this pin is allowed to go high. Odd parity is selected by moving the switch to the left and driving this input low. PARITY INHIBIT is located on UART pin 35. Parity generation is inhibited if the switch is to the right and the input is high. If this input is low then the UART control will read the parity selection input (pin 39). If this input is high, then pin 39 is ignored. The last control input is pin 33, BIT 8 CONTROL. This input is active only if the ORD LENGTH SELECT input (pin 38) is high and an 8 bit word is selected. This control input is then used to choose a "mark" or a "space" in the eighth data bit position.

6.9.3 Current Loop XMTR?RCVR

The last item on this sheet is the CURRENT LOOP transmitter/receiver combination. The current loop differs from the circuits in the ADM-1 and 2 primarily because it is bipolar. That is, current direction is immaterial. The transmitter and receiver can run completely isolated from the ADM-3 which is its normal operating mode. However, provision has been made inside the unit to tie one leg of the transmitter or receiver to +12 volts through a resistor to create a current source. As an alternative, a ground strap can be installed, in place of the resistor, to act as a current sink in the case of a positive external voltage source or as a current source in the case of a negative source. The CURRENT LOOP operation is still limited to 20V/20ma.

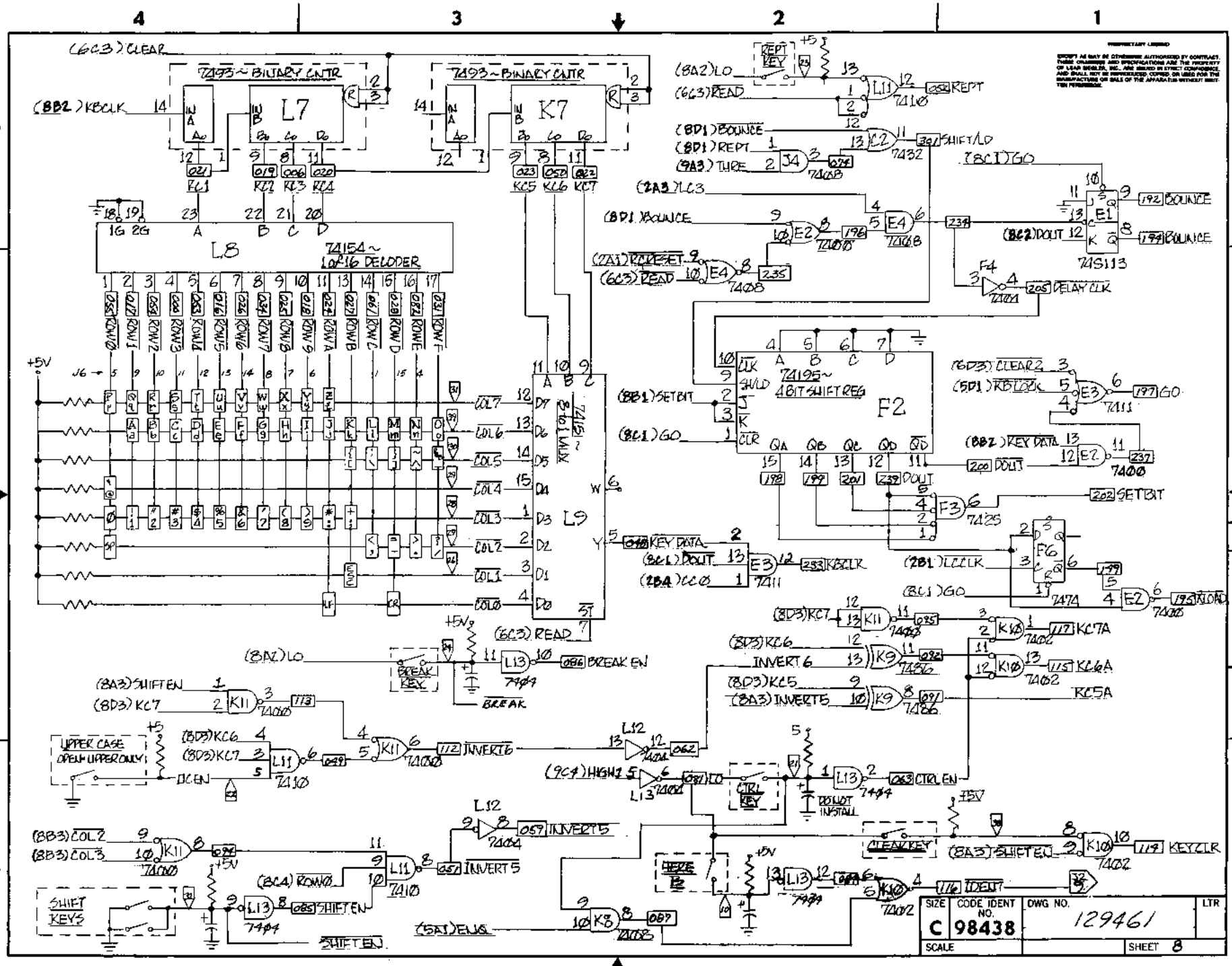


Figure 6-16
6-27

6.10 SCHEMATIC SHEET #10 — BAUD RATE GENERATION

This schematic covers the clock generation required by the UART transmitter and receiver sections for the various selectable baud rates. The basic clock utilized in this counter chain is DC1 which is a stage of the DOT COUNTER located on sheet #2, zone D2. It has a frequency of 3.1104 MHz. The first counter J1 (zone D3) has a division of 5 normally and switches to a division by 6 when the 1800 baud switch is enabled. Counter K1 (74161,zone D2) normally divides by sixteen and switches to a division by nine with 1800 enabled. Counter L1 (74161,zone D1) always divides by 16. Therefore, it can be seen that when 1800 baud is enabled, all normal baud rates except 110 baud are lost. This is because 110 baud is picked off the system counter chain at LC1 (sheet 2, zone A3). The individually generated baud clocks are then run through the baud rate selection switches under the plate and to flip-flops M2-3 and M2-11 (zone B1). The clock inputs to the transmit and receive flops actually run at twice the desired clock rate and are run through the flops to achieve a better duty cycle. The split baud rate option is also shown on this page. The secondary lines labeled in zones A2 and B2 actually go to a small rotary switch physically located at the front left edge of the keyboard inside the case. The cut indicated in zone B1 must be made if the rotary switch is set to any position other than position 12. Position 12 is the "common" position which again makes the inputs to the two flops the same. The main thing to remember with the split rate option is that if 1800 baud is selected on the main baud rate switches (receive clock) then 110 baud is the only legal clock on the rotary switch.

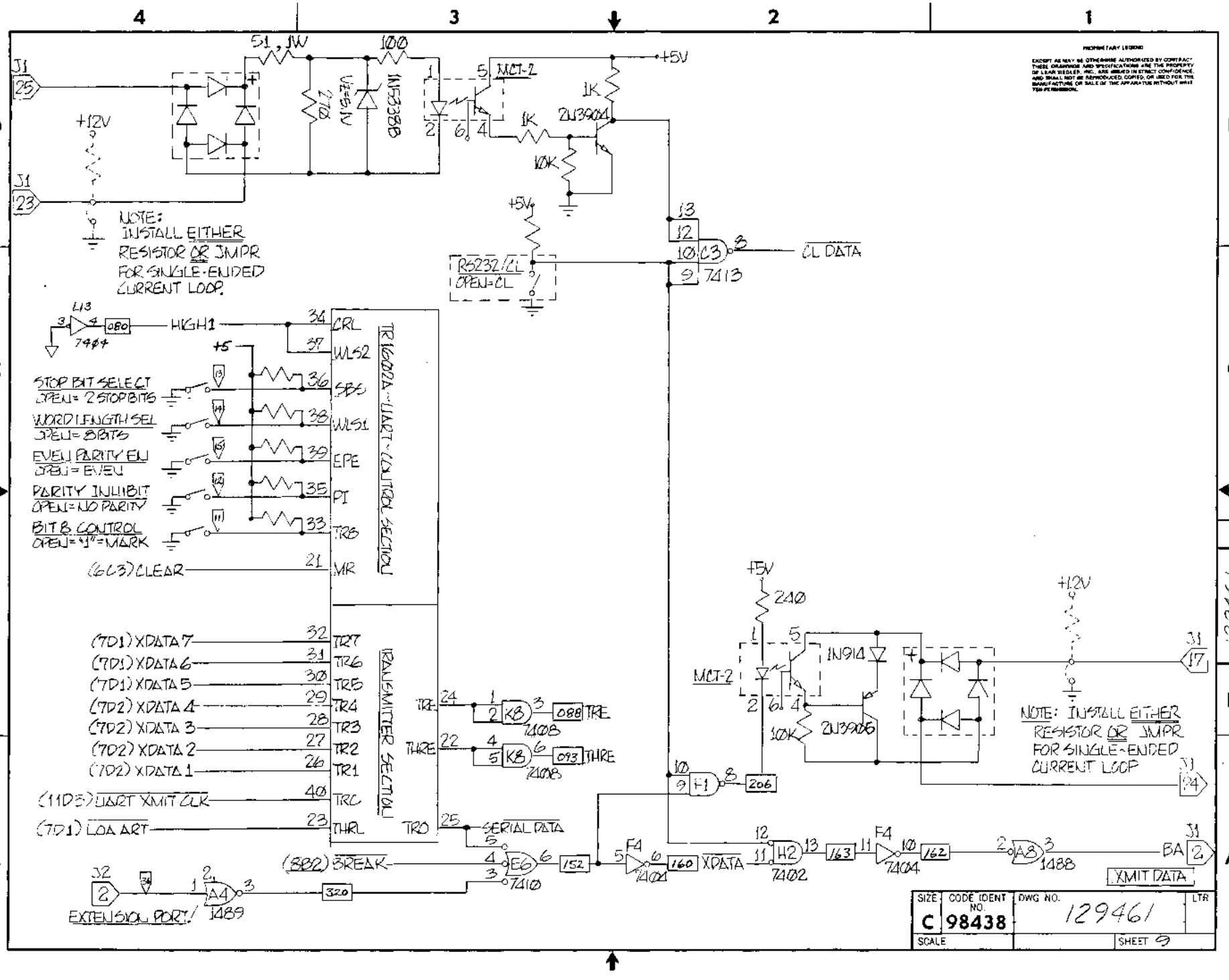


Figure 6-17
6-29

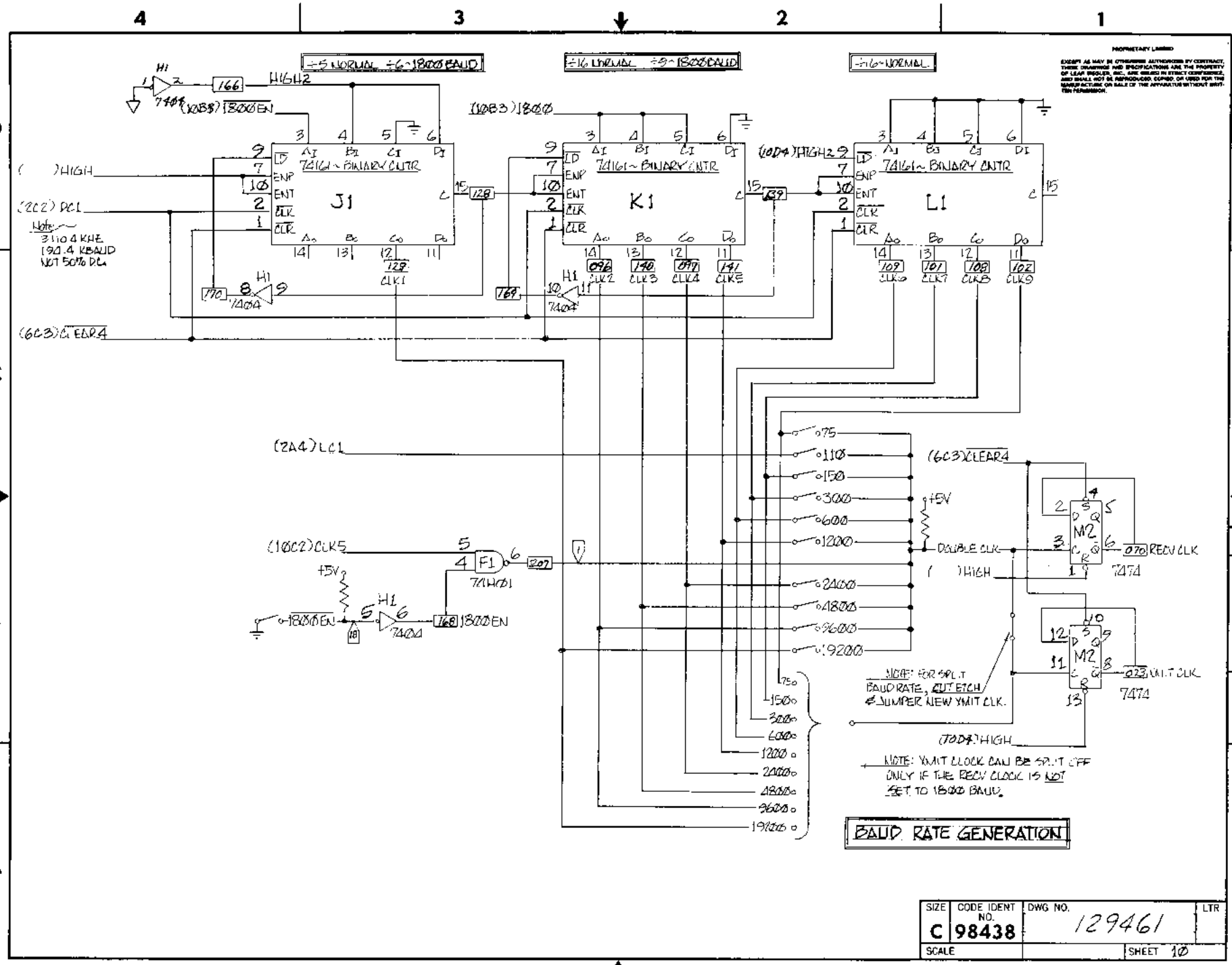


Figure 6-18
6-30

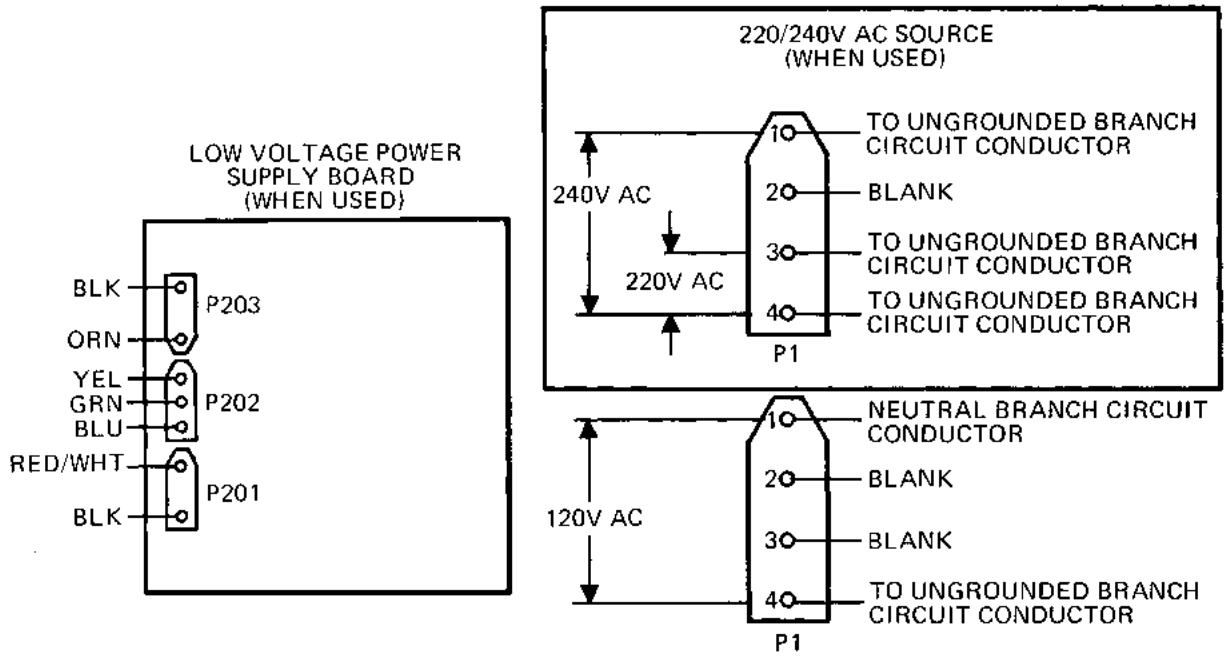
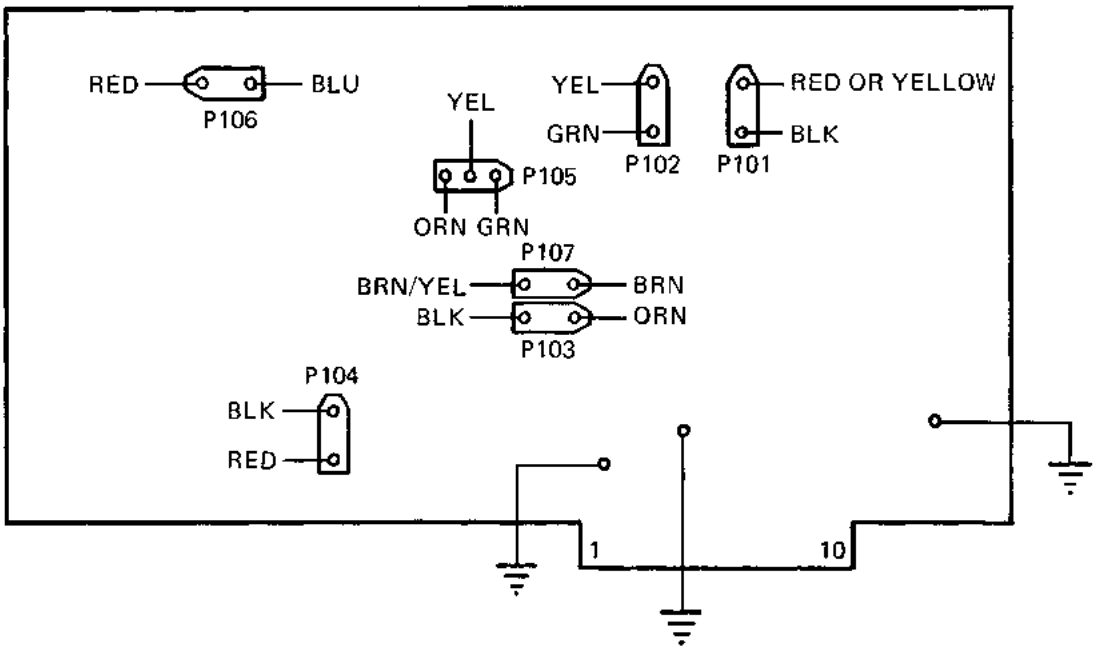
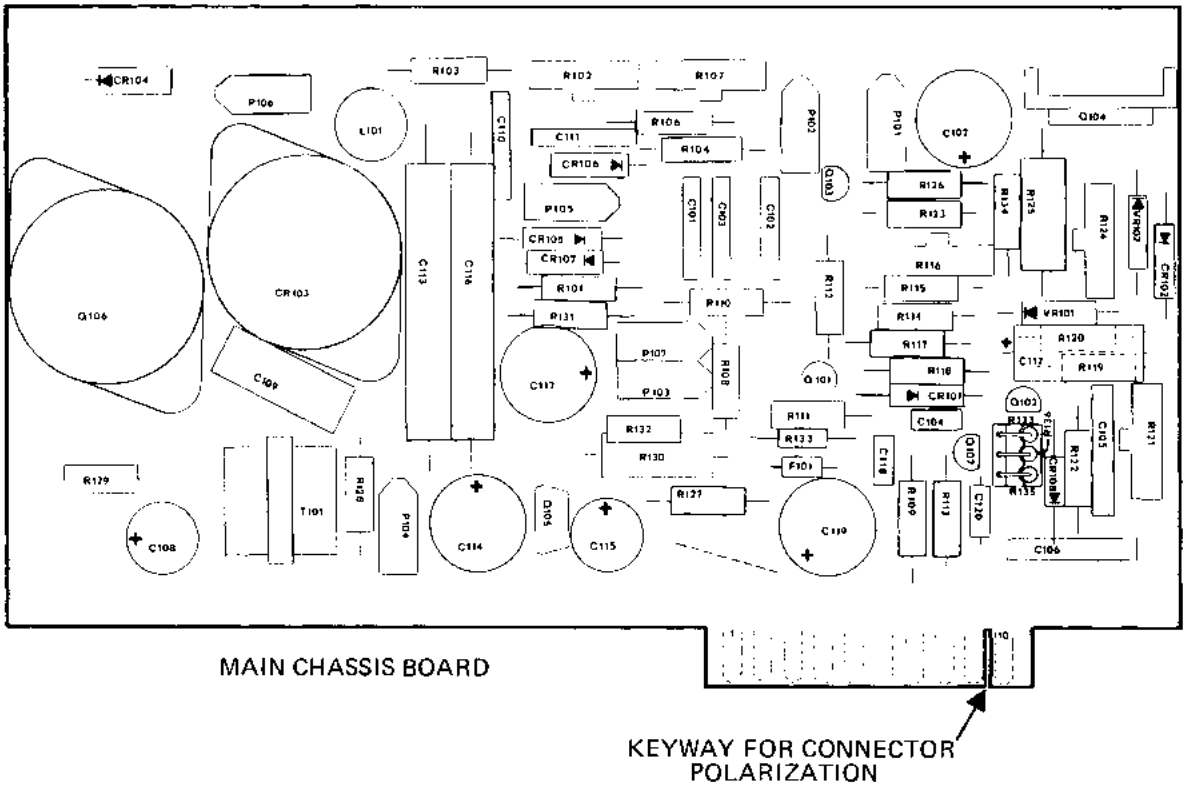


Figure 6-19. Monitor Interconnecting Cabling Diagram





NOTE:
F101 AND R108 ARE USED ONLY WHEN LOW VOLTAGE POWER SUPPLY IS NOT SUPPLIED.

Figure 6-20. Monitor Circuit Board Components Location

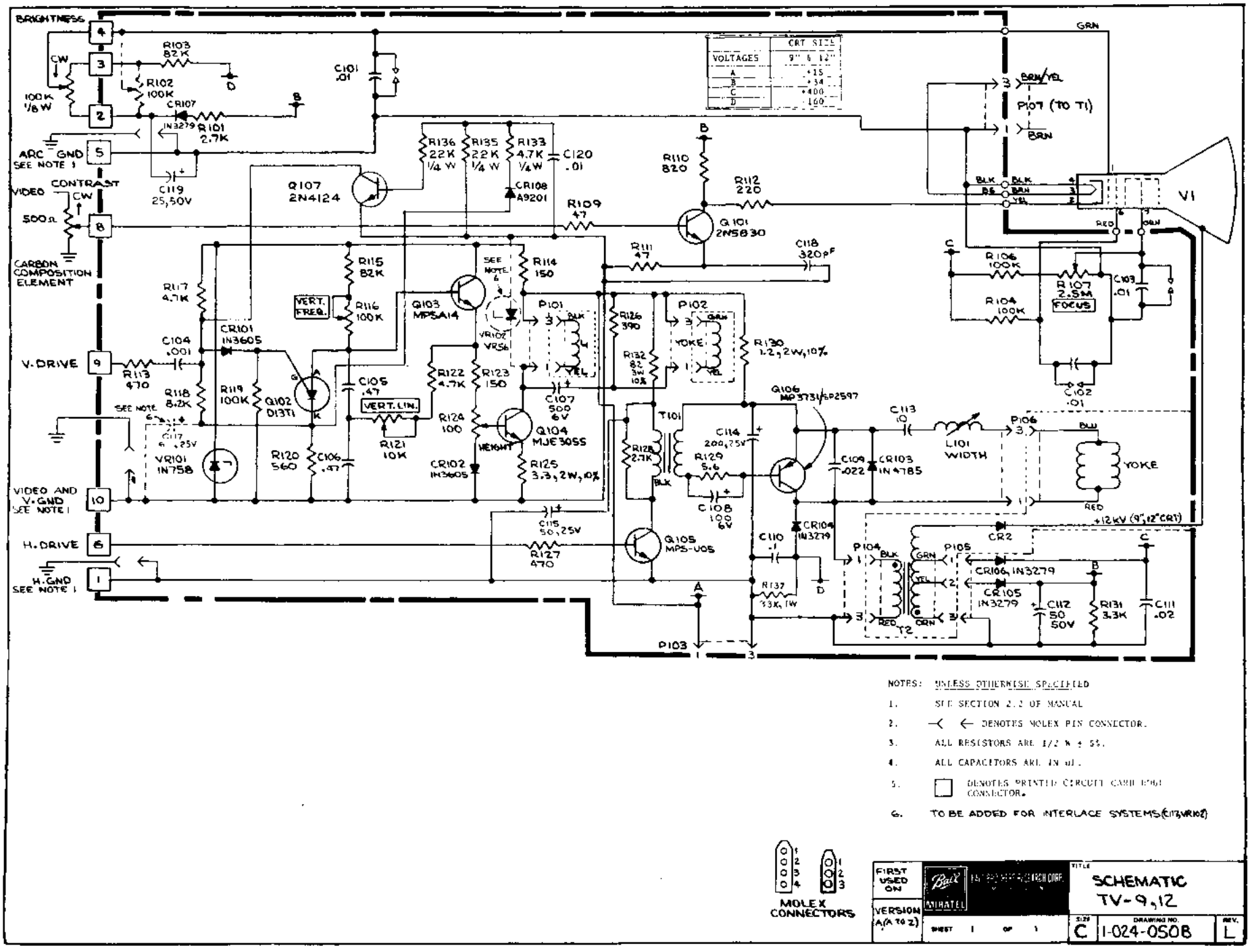


Figure 6-21. Schematic, TV 9 and 12 With Power Supply

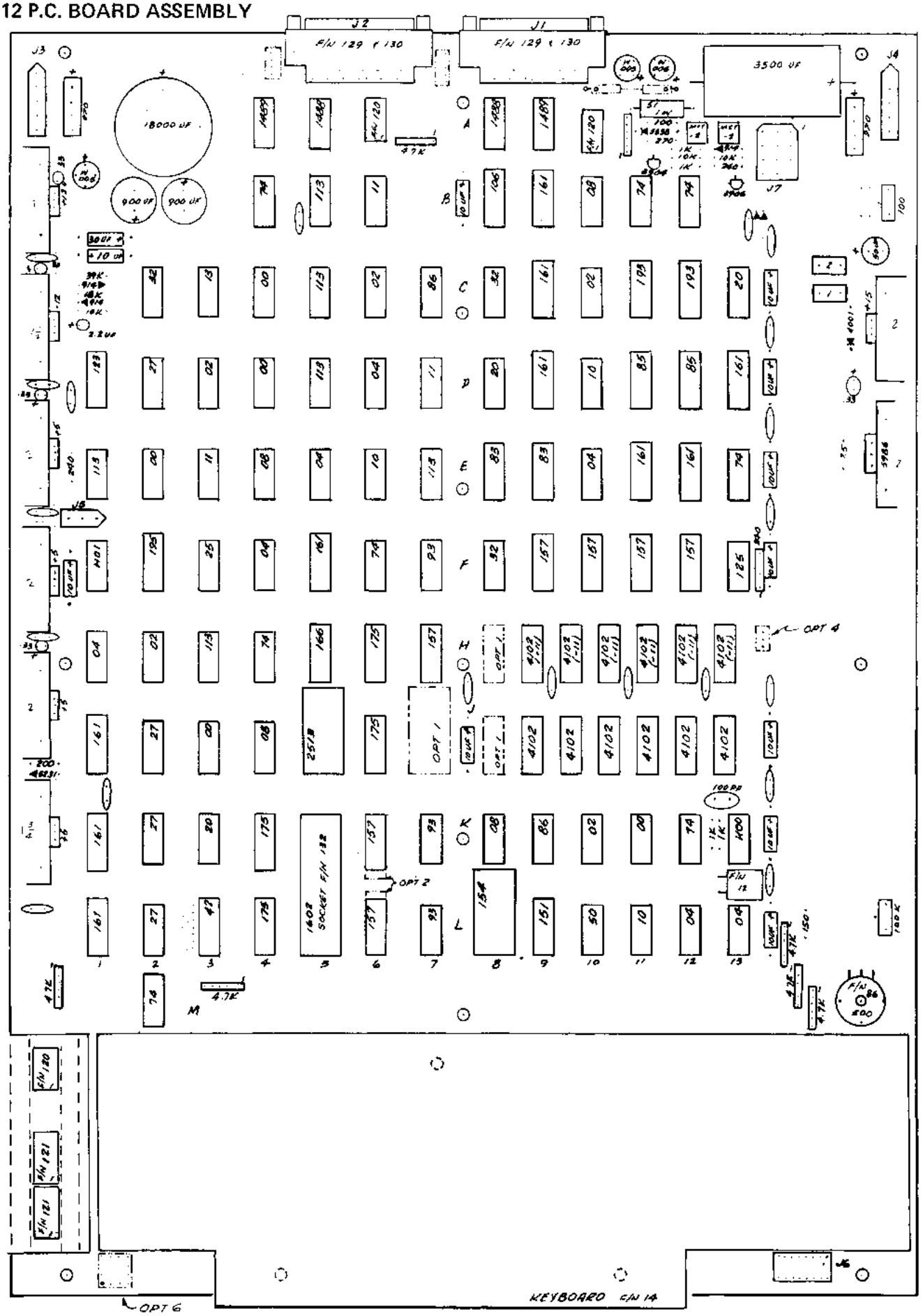

J2
J1
J3
J4
J7
3500 UF
18000 UF
900 UF
900 UF
OPT 1
OPT 2
OPT 4
OPT 6
KEYBOARD F/N 14

Figure 6-22

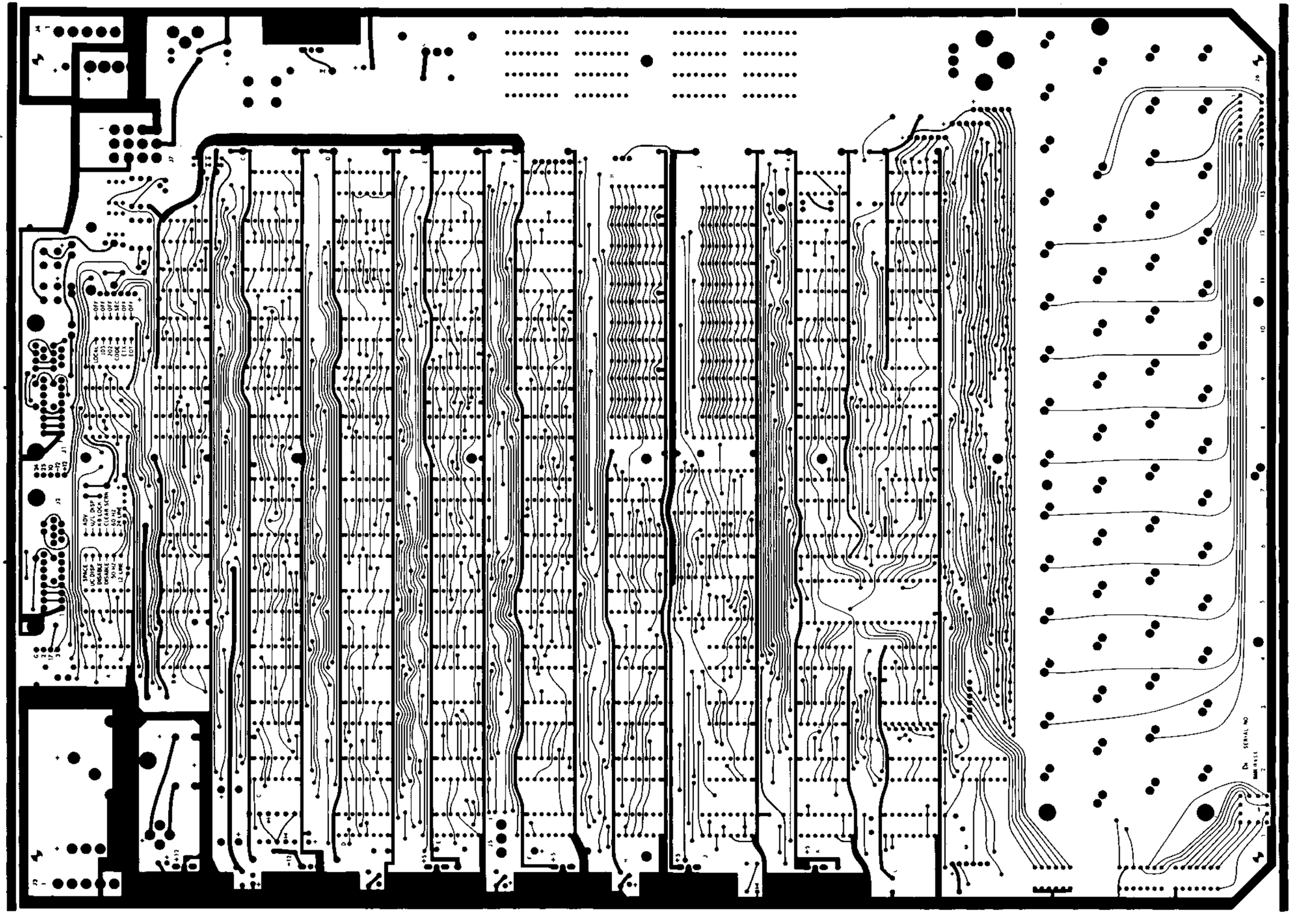


Figure 6-23

6.14 CIRCUIT BOARD BACK

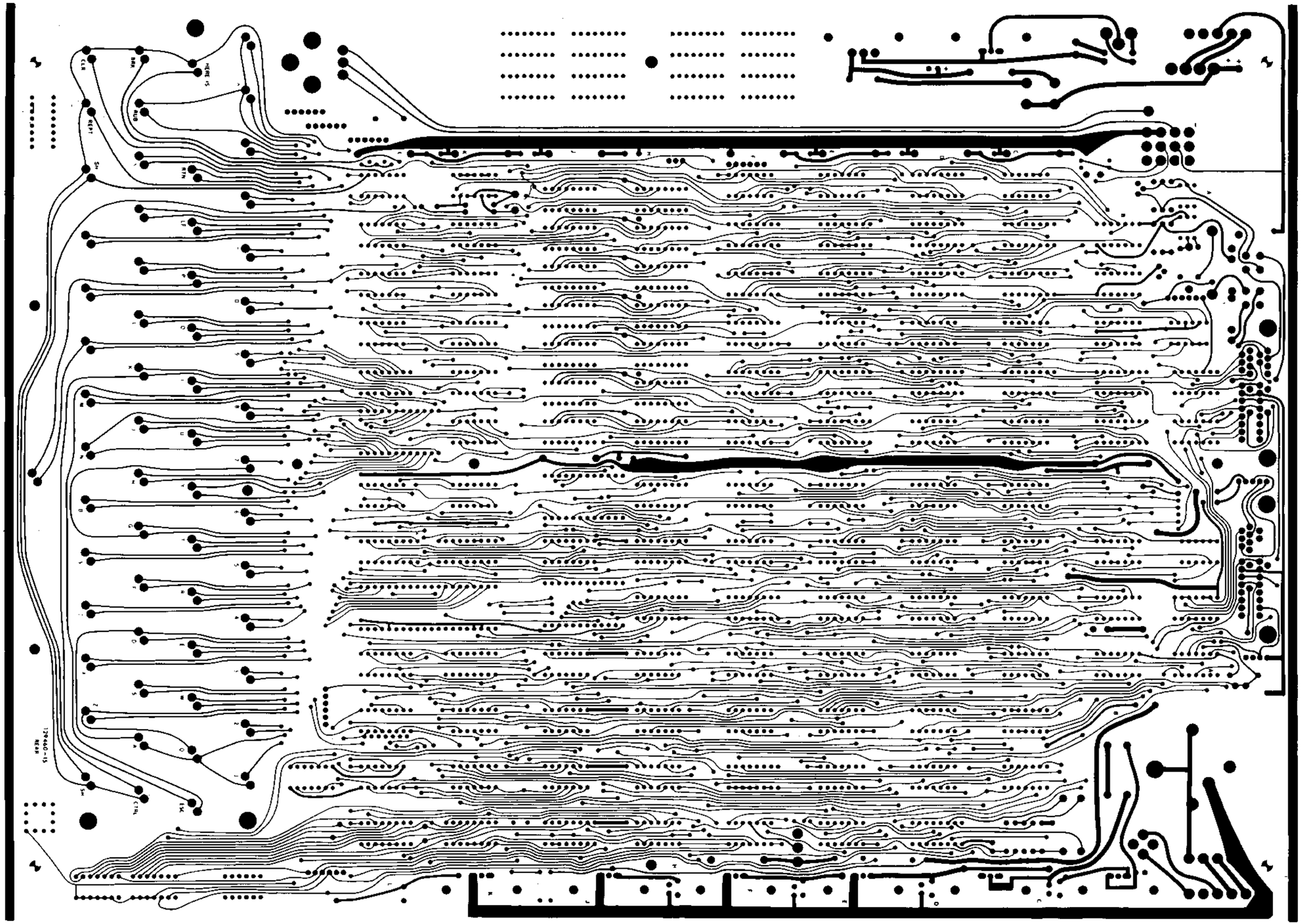


Figure 6-24 6-36

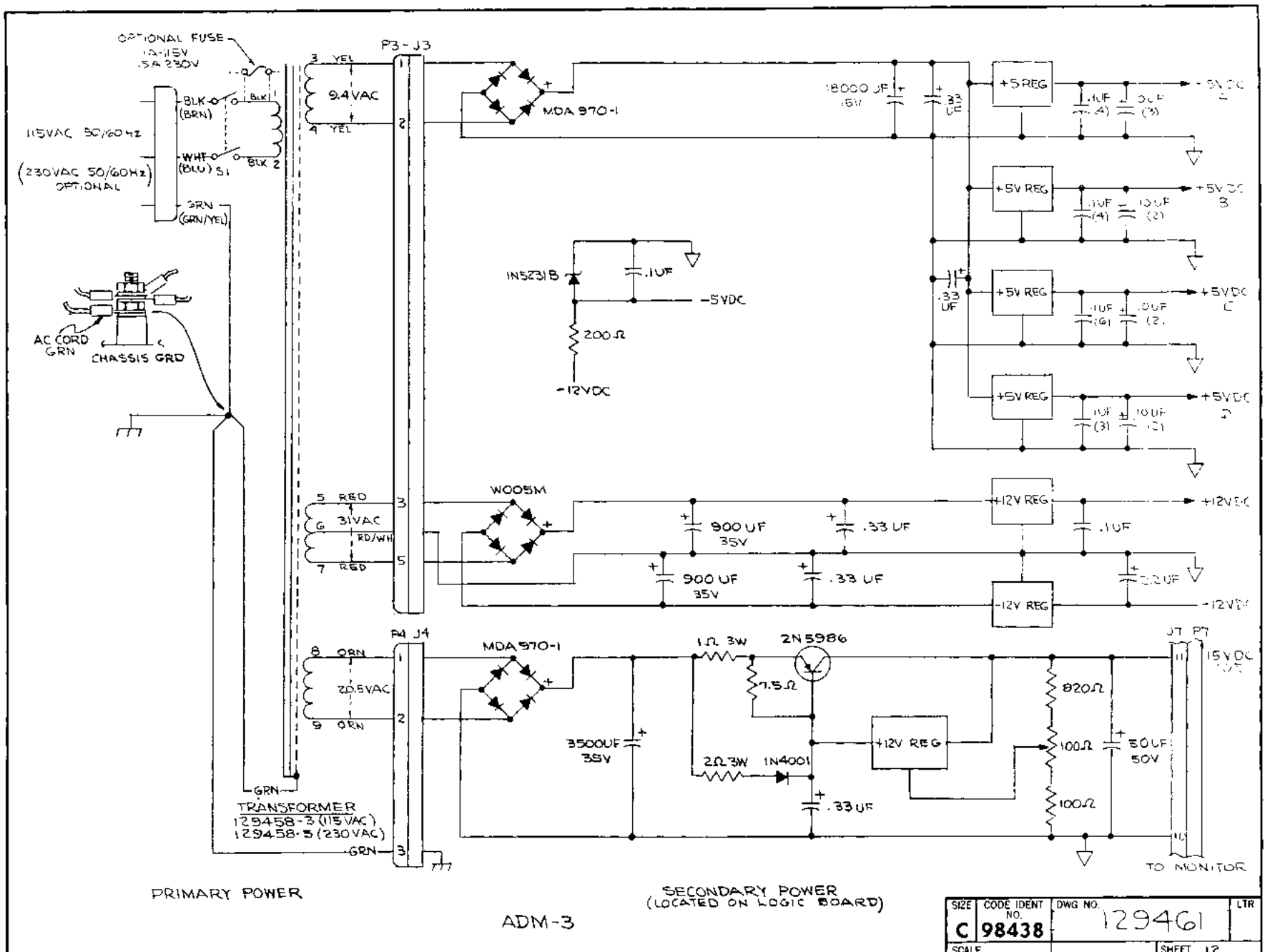

OPTIONAL FUSE
1A-115V
.5A 230V
115VAC 50/60Hz
(230VAC 50/60Hz)
OPTIONAL
BLK (BRN)
WHT (BLU)
GRN (GRN/YEL)
BLK 1
BLK 2
S1
AC CORD GRN
CHASSIS GRD
P3 - J3
3 YEL
9.4VAC
4 YEL
MDA 970-1
18000 UF 16V
.33 UF
+5 REG
.1UF (4)
.01UF (3)
+5V DC A
+5V REG
.1UF (4)
.01UF (2)
+5V DC B
+5V REG
.1UF (6)
.01UF (2)
+5VDC C
+5V REG
.1UF (3)
.01UF (2)
+5VDC D
1N5231B
.1UF
-5VDC
200Ω
-12VDC
5 RED
6
31VAC
RD/WH
7 RED
W005M
900 UF 35V
.33 UF
900 UF 35V
.33 UF
+12V REG
.1UF
+12VDC
2.2UF
-12V REG
-12VDC
P4 J4
8 ORN
20.5VAC
9 ORN
MDA 970-1
3500UF 35V
1Ω 3W
2N5986
7.5Ω
2Ω 3W
1N4001
.33 UF
+12V REG
820Ω
100Ω
100Ω
50UF 50V
J7 P7
15VDC OUT
TO MONITOR
GRN
TRANSFORMER
129458-3 (115VAC)
129458-5 (230VAC)
GRN
PRIMARY POWER
SECONDARY POWER
(LOCATED ON LOGIC BOARD)
ADM-3
SIZE C
CODE IDENT NO. 98438
DWG NO. 129461
LTR
SCALE
SHEET 12

Figure 6-25

SECTION 7
PARTS LIST

Included in this section are lists of both the major components as provided by Lear Siegler and the general parts which are a part of the major components.

ADM-3 REPLACEABLE PARTS INFORMATION

Spare parts and renewal parts for the ADM-3 are available from Lear Siegler Electronics Instrumentation Division. When ordering parts, include the following information.

1. ADM-3 Serial Number
2. Part Description
3. LSI or Manufacturer's Part Number

Routine parts orders may be mailed to:

Lear Siegler, Inc.,
Electronics Instrumentation Division
Data Products Customer Service
714 North Brookhurst Street
Anaheim, California 92803

Emergency parts orders may be placed by telephoning:

Data Products Customer Service
Telephone (714) 774-1010

or by teletype to:

TELEX 655444
TWX 910-591-1157

ADM-3 SPARE PARTS LIST

Logic Board	P/N 129460-15
Monitor Assembly	P/N Type 3
Tube Assembly	P/N 129479-01
Yoke Assembly	P/N 129479-03
Flyback Assembly	P/N 129479-05
Video Amplifier	P/N 129479-02
Inductor	P/N 129479-04
Lower Housing	P/N 129452-5
Upper Housing	P/N 129452-3
Transformer	P/N 129458-03 (115 V 47-63 HZ)
Power Switch	TGC0411-TWB (imprinted on-off) carling
Power Cord	P/N 129455-03 115V
Speaker Assembly	P/N 129487-01 (no wires)

Options

Lower Case Character Generator	P/N 129323-02
Lower Case Kit	P/N 129502 Opt #1
Answer Back	P/N 129489-01
Cables Ribbon Kit	P/N 129502 Opt. #2
Cables Ribbon	CAD-18/02-261-CC-014 (circuit assembly)
Current Loop Extension	P/N 129488-01
Current Loop Kit	129502 Opt. #5
Keyboard Repair Tool	
Keyboard Repair Kit	
1 Split Contact	P/N 373-30052-2
1 Solid Contact	P/N 373-30053-2
Plunger	P/N 373-40103
Springs	P/N 373-10012

ADM-3 ASSEMBLY PARTS LIST 129450

Ref. Des.	Description	LSI Part No.	Mfg. Part No. MIL Type Des.	Mfg. Code	Qty. 01	Qty. 011	Note
1	ADM-3 Assy, (12 Line)	129450-01					
2	ADM-3 (24 Line)	129450-11					
3	Housing-Top	129452-03			1	1	
4	Housing-Bottom	129452-05			1	1	
5	Logo	129453-03			1	1	
6	Power Cord	129455-03			1	1	
7	Nameplate	129456-03			1	1	
8	Transformer, Power	129458-01			1	1	
9	Wiring	129459-01			1	1	
10	P.C. Board Assy. (12 Line)	129460-01				1	
11	P.C. Board Assy. (24 Line)	129460-11			1		
12	T.V. Monitor	12949-01			1	1	
13	CRT Bracket Assy.	129480-01			1	1	
14	Cable, Monitor	129481-01			1	1	
15	Retainer Bracket, CRT	129483-03			1	1	
16	Screen	129484-03			2	2	
17	Baffle Plate	129485-03			2	2	
18	Speaker	129487-01			1	1	
19	Switch, Rocker (imprinted Code)		TGCO411-TW-B	Carling	1	1	
20	Strain Relief		SR-6L-1	Heyco	1	1	
21	Pop Rivet		AD66ABSLF	USM-Corp	4	4	
22	Screw - Pan Head, Steel, Slotted Cadmium Plated		10-32 x 3/4 long	Fed. Screw or equivalent	2	2	
23	Screw - Indented Hex Washer Head Slot, Steel, Cad Plated		10-32 x 7/16 long	Fed. Screw or equivalent	3	3	
24	Screw - Slotted, Pan Head, Nickel Plated Steel		4 - 40 x 3/16 long	Fed. Screw or equivalent	1	1	
25	Plastite Screw, Pan Head, Slotted Cad Plated		4(.123) - 20 5/16 long	Continental Screw Co.	4	4	
26	Nut, Electronic Size - 10-32 Brass Nickel Plated		9041-NP	Fed. Screw or equivalent	2	2	
27	Washer, No. 10 Brass Nickel Plated		97255	Fed. Screw or equivalent	1	1	

MONITOR REPLACEABLE PARTS INFORMATION

ORDERING PARTS

Most parts contained in the monitor are available commercially from electronic parts outlets. When it is necessary to order spare or replacement parts from BBRC, Miratel Division, include the part description, part number, model and serial number data of the monitor as listed on the serial number plate and, if applicable, the schematic reference number listed in the parts list. Orders for these parts should be sent to:

Ball Brothers Research Corporation
Miratel Division
1633 Terrace Drive
Roseville, Minnesota 55113

For rapid service:

Telephone area (612) 633-1742
or
Teletype area (910) 563-3552

RETURNING PARTS

When the monitor requires service or repair in accordance with the enclosed warranty, return the unit or part to:

Ball Brothers Research Corporation
Miratel Division
1633 Terrace Drive
Roseville, Minnesota 55113
Attn: Customer Service
Telephone area (612) 633-1742
Teletype area (910) 563-3552

Unnecessary delays may be avoided when parts are returned to Miratel Division using the following procedures:

1. Package the unit or part in accordance with the method of shipment. Enclose a list of the material being returned and the reason for returning it.

2. Send the unit or part, transportation prepaid, to the address stipulated for returning parts.

All equipment and parts described in the warranty will be replaced, provided Miratel's examination discloses that the defects are within the limits of the warranty. If damages or defects are not within the limits of the warranty, the customer will be notified of the extent of repairs required and the cost. The unit will be repaired and returned upon agreement.

MONITOR PARTS LIST

Symbol	Description	Mfg.	Mfg. Part Number	BBRC Part Number
	Capacitor, Fixed; μF Unless Otherwise Stated			
C1	3300; 60V, Electrolytic	BBRC		1-012-2156
C101	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C102	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C103	0.01; 1000V, Ceramic Arc Gap	CRL	Type DG-63	1-012-0112
C104	0.001 + 10%; 1000V, Ceramic Disc	ERIE	Type 801	1-012-0540
C105	0.47 + 10%, 100V, Mylar	PAK	MF830	1-012-1005
C106	0.47 + 10%; 100V, Mylar	PAK	MF830	1-012-1005
C107	500; 6V, Electrolytic	BBRC		1-012-2158
C108	100; 6V, Electrolytic	BBRC		1-012-2160
C109	0.022 + 10%, 400V, Mylar	SPRA	Type 225P	1-012-0800
C110	.1 + 10%; 200V, Mylar	PAK	MF580	1-012-0870
C111	0.02 + 20%; 1000V, Ceramic Disc	ERIE	Type 841	1-012-0780
C112	50; 50V, Electrolytic	BBRC		1-012-2157
C113	10 + 10%, 63V, Mylar	BBRC		1-012-1130
C114	200; 25V, Electrolytic	BBRC		1-012-2159
C115	50; 25V, Electrolytic	BBRC		1-012-2165
C116	20; 150V, Electrolytic	BBRC		1-012-1260
C117	6μf; 25V, Electrolytic	SPRA	TE1203	1-012-2066
C118	820pf + 5%; 500V, Dipped Mica	ARCO	Type DM	1-012-0482
C119	25; 50V, Electrolytic	BBRC		1-012-2193
C120	.01 + 20%; 1000V; Ceramic Disc	ERIE	Type 811	1-012-0740
C201	50; 50V, Electrolytic	BBRC		1-012-2157
C202	0.01 + 20%; 1000V; Ceramic Disc	ERIE	Type 841	1-012-0780
C203	50; 50V, Electrolytic	BBRC		1-012-2157
CR1	VS148, Bridge Rectifier	VARO	VS148	1-021-0413
CR2	H510, High Voltage Rectifier	VARO	H510	1-021-0424
CR101	1N3605	SYL	1N3605	1-021-0410
CR102	1N3605	SYL	1N3605	1-021-0410
CR103	1N4785	RCA	1N4785	1-021-0360
CR104	1N3279	DI	1N3279	1-021-0380
CR105	1N3279	DI	1N3279	1-021-0380
CR106	1N3279	DI	1N3279	1-021-0380
CR107	1N3279	DI	1N3279	1-021-0380
CR108	1N3605	SYL	1N3605	1-021-0410
F1	Fuse, 0.6A-250V, ¼ x 1¼, Slo-Blo	LF	Type AGC	1-028-0244
or	Fuse, 0.6A-250V, 9/32 x 1¼, Slo-Blo (TV-B12)	BUSS	Type MDM	1-028-0245
F101	Fuse, 2A-125V, Picofuse	LF	276002	1-028-0247
L1	Vertical Choke	BBRC		6-003-0321
L101	Coil, Width	BBRC		1-016-0303
	TRANSISTOR			
Q1	2N3055	RCA	2N3055	1-015-1134
Q101	2N5830	MOT	2N5830	1-015-1172
Q102	D13T1	GE	D13T1	1-015-1157
	Resistor, Film: ½W + 5% Unless Otherwise Stated			
R133	4.7K; ¼W			70-16-0472
R134	Not Used			
R135	22K			70-16-0223

MONITOR PARTS LIST (Continued

Symbol	Description	Mfg.	Mfg. Part Number	BBRC Part Number
R136	22K			70-16-0223
R137	33K; 1W Composition			1-011-2448
R201	1K			1-011-2270
R202	1K			1-011-2270
R203	10K			1-011-2294
R204	0.68 Ω + 10%; 2W, Wirewound	IRC	Type BHW	1-011-2217
R205	1.5K			1-011-2274
R206	470 Ω			1-011-2262
R207	470 Ω			1-011-2262
R208	Var; 500 Ω + 20%; 1/5W, Composition	CTS	Type 201	1-011-5604
R209	470 Ω			1-011-2262
	TRANSFORMER			
T1	Power	BBRC		1-017-5390
T2	High Voltage (TV-12C, TV-12, & TV-E12)	BBRC		6-003-0320
or	High Voltage (TV-B12, TV-TC12, & TV-C12)	BBRC		6-003-0325
or	High Voltage (TV-T12)	BBRC		6-003-0326
or	High Voltage (TV-D12)	BBRC		6-003-0333
T101	Horizontal Driver	BBRC		1-017-5338
VR101	1N758	T1	1N758	1-021-0180
VR102	VR56	ST	VR56	1-021-0420
	MISCELLANEOUS			
	Socket, CRT (TV12)	BBRC		1-022-0427
	Fuseholder, Extractor Post, Fuse Size: ¼ x 1¼	LF	342012	1-028-0210
	Fuseholder, Extractor Post, Fuse Size: 9/32 x 1¼ (TV-B12 Only)	BUSS	Type HCM	1-028-0246
	Low Voltage Circuit Board Assembly	BBRC		6-003-0459
	Main Chassis Circuit Board Assembly	BBRC		6-003-0500
	Main Chassis Circuit Board Assembly (TV-T12)	BBRC		6-002-0476
	Main Chassis Circuit Board Assembly (TV-TC12)	BBRC		6-002-0502
	Main Chassis Circuit Board Assembly (TV-C12)	BBRC		6-002-0504
	Main Chassis Circuit Board Assembly (TV12, Tektronics)	BBRC		6-002-0506
	Cable Assembly; 8 Inch	BBRC		6-004-0630
	Cable Assembly; 5 Inch	BBRC		6-004-0631
	Power Supply Module (TV-12, 120VAC)	BBRC		6-003-0371
	Power Supply Module (TV-12, 220VAC)	BBRC		6-003-0372
	Power Supply Module (TV-B12, 120VAC)	BBRC		6-003-0368
	Power Supply Module (TV-B12, 220VAC)	BBRC		6-002-0370
	Deflection Coil Assembly	BBRC		6-004-0314
	Deflection Coil Assembly (TV-B12)	BBRC		6-004-0321
V1	CRT, 12 Inch, P4 Phosphor	BBRC		1-014-0737
	Power Cable Assembly, 120VAC	BBRC		6-003-0645
	Power Cable Assembly, 200VAC	BBRC		6-003-0652

MONITOR VENDOR CODES AND LOCATIONS

Code	Manufacturer	Location
BBRC	Ball Brothers Research Corporation, Miratel Division	Roseville, Minnesota
BUSS	Bussman Manufacturing	St. Louis, Missouri
CRL	Centralab	Milwaukee, Wisconsin
CTS	CTS Corporation	Elkhart, Indiana
DI	Diode, Inc.	Chatsworth, California
ERIE	Erie Technological Products, Inc.	Erie, Pennsylvania
GE	General Electric	Syracuse, New York
IRC	IRC Corporation	Philadelphia, Pennsylvania
LF	Littelfuse Company, Inc.	Des Plaines, Illinois
MALL	P. R. Mallory Company, Inc.	Indianapolis, Indiana
MOT	Motorola Semiconductor Products	Phoenix, Arizona
NPC	Neucleonics Products	Los Angeles, California
PAK	Paktron	Alexandria, Virginia
RCA	RCA Semiconductor Division	Harrison, New Jersey
SPRA	Sarkes Tarzian, Inc.	Bloomington, Indiana
SYL	Sylvania Electric Products	Seneca Falls, New York
TI	Texas Instrument	Dallas, Texas
VARO	Varo Corporation	Garland, Texas

CRT BRACKET ASSEMBLY 129480

Ref. Des.	Description	LSI Part No.	Mfg. Part No. MIL Type Des.	Mfg. Code	Qty. 01 011	Note
1	Bracket Assembly	129480-01				
2	Bracket	129454-03			2	
3	Tab (.197 Stud) Tin Plated Brass		61499-1	Amp Inc.	1	
4	"POP" rivet		AD66ABSLF	USM Corp.	4	

P.C. BOARD ASSEMBLY, ANSWER BACK

Ref. Des.	Description	LSI Part No.	Mfg. Part No. MIL Type Des.	Mfg. Code	Qty. 01 011	Note
1	P.C. Board Assy., Answer Back	129489-01				
2	I/C	128348-02			1	
3	I/C	128348-74			1	
4	I/C	128348-93			1	
5	I/C	128348-113			2	
6	I/C	128348-157			4	
7	Capacitor .1 μF	129329-104			2	
8	Capacitor 10 μF	129469-106			2	
9	P.W. Board	129489-05			1	
10	Prom, 82S23 Type	129493			1	
11	Socket, 16 Pin		CA-16S-10SD	Circuit Assy.	3	
12	Socket, 18 Pin		CA18S-10SD	Circuit Assy.	2	

ADM-3 P.C. BOARD ASSEMBLY

Ref. Des.	Description	LSI Part No.	Mfg. Part No. MIL Type Des.	Mfg. Code	Qty. 01	Qty. 011	Note
1	P.C. Board Assembly (12 Line)	129460-01					
2	P.C. Board Assembly (24 line)	129460-11					
3	Printed Wiring Board	129460-09			1	1	
4	I/C	128348-00			1	1	
5	I/C	128348-01			1	1	
6	I/C	128348-02			5	5	
7	I/C	128348-08			4	4	
8	I/C	128348-11			2	2	
9	I/C	128348-13			1	1	
10	I/C	128348-25			1	1	
11	I/C	128348-27			4	4	
12	I/C	128348-32			3	3	
13	I/C	128348-42			1	1	
14	I/C	128348-50			1	1	
15	I/C	128348-74			8	8	
16	I/C	128348-83			2	2	
17	I/C	128348-85			2	2	
18	I/C	128348-86			2	2	
19	I/C	128348-93			2	2	
20	I/C	128348-106			1	1	
21	I/C	128348-113			5	5	
22	I/C	128348-123			1	1	
23	I/C	128348-125			1	1	
24	I/C	128348-151			1	1	
25	I/C	128348-154			1	1	
26	I/C	128348-157			7	7	
27	I/C	128348-161			10	10	
28	I/C	128348-166			1	1	
29	I/C	128348-175			4	4	
30	I/C	128348-193			2	2	
31	I/C	128348-195			1	1	
32	I/C	128348-1488			2	2	
33	I/C	128348-1489			2	2	
34	I/C	128348-1602			1	1	
35	RAM	128348-4102			12	6	
36	I/C	128348-2513			1	1	
37	I/C	128578-00			5	5	
38	I/C	128578-04			6	6	
39	I/C	128578-10			3	3	
40	I/C	128578-20			3	3	
41	Capacitor - 1150	129329-104			21	21	
42	Keyboard	129451-01			1	1	
43	Capacitor, 18000115	129468-189			1	1	
44	Capacitor, 900135	129468-907			2	2	
45	Capacitor, 50/50	129468-506			1	1	
46	Capacitor, 3500135	129469-358			1	1	
47	Capacitor, 10125	129469-106			11	11	
48	Heat Sink - Regular	129474-03			8	8	
49	Resistor Network	129476-241			1	1	
50	Resistor Network	129476-472			7	7	
51	Connector	129478			2	2	
52	Crystal 10.8864 MHZ		800-A	Stan. Crystal	1	1	
53	Optical Isolator		MCT-2	Motorola	2	2	
54	Regulator +5		MC-7805C	Motorola	4	4	

Ref. Des.	Description	LSI Part No.	Mfg. Part No. MIL Type Des.	Mfg. Code	Qty. 01	Qty. 011	Note
55	Regulator +12		MC-7812C	Motorola	1	1	
56	Regulator +15		MC-7815C	Motorola	1	1	
57	Regulator −12		MC-7912C	Motorola	1	1	
58	Bridge		MDA970-1	Motorola	2	2	
59	Bridge		W005	General Inst.	1	1	
60	Capacitor 2.2/25		196D225 x.0025 HAI	Sprague	1	1	
61	Capacitor .33/35		196D334 x.0035 HAI	Sprague	5	5	
62	Potentiometer - Video		See note 2	CTS	1	1	See sch. p. 4
63	Brightness		X-201-SS-100K	CTS	1	1	
64	Resistor 100		CB 1015	Allen Bradley	1	1	
65	Resistor 150		CB 1515	Allen Bradley	1	1	
66	Resistor 200		CB 2015	Allen Bradley	1	1	
67	Resistor 240		CB 2415	Allen Bradley	2	2	
68	Resistor 270		CB 2715	Allen Bradley	1	1	
69	Resistor 1K		CB 1025	Allen Bradley	4	4	
70	Resistor 2.7K		CB 2725	Allen Bradley	1	1	
71	Resistor 3.3K		CB 3325	Allen Bradley	1	1	
72	Resistor 10K		CB 1035	Allen Bradley	3	3	
73	Resistor 18K		CB 1835	Allen Bradley	1	1	
74	Resistor 39K		CB 3935	Allen Bradley	1	1	
75	Resistor 7.5		CB 75G5	Allen Bradley	1	1	
76	Resistor 51 Ω1W		GB 5105	Allen Bradley	1	1	
77	Resistor 2 Ω3W		PC 5802	Ohmite	1	1	
78	Resistor 1 Ω3W		PC 5800	Ohmite	1	1	
79	Capacitor		DM15-101	Elmenco	1	1	
80	Diode		1N914		4	4	
81	Diode		1N4001		1	1	
82	Transistor		2N3904		1	1	
83	Transistor		2N3904		1	1	
84	Transistor		2N5986		1	1	
85	Zener Diode 5.1V 5%		1N5231B		1	1	
86	Zener Diode 5.1V 5%		1N5338B		1	1	
87	Black Knob		IRQ-5000-1	Buckeye	1	1	
88	Switch 6 Position		01-70-0106	Molex	3	3	
89	Switch 7 Position		01-70-0107	Molex	2	2	
90	Wafer Con. 3 Cir. Key@1		09-18-5031	Molex	1	1	J8
91	Wafer Con. 5 Cir. Key@1		09-18-5051	Molex	1	1	J3
92	Wafer Con. 5 Cir. Key@1 & 2		09-18-5059	Molex	1	1	J4
93	Jackscrew		205817-1	AMP	2	2	
94	Socket, 40 Pin		CA-40S-10S0	Circuit Assy.	1	1	
95	Socket, 16 Pin		CA-16S-10S0	Circuit Assy.	1	1	
96	Nut, Hex 6-32, NIPL		F-560-M	Waldom	7	7	1
97	Washer, Flat,NIPL		MW-402-M	Waldom	7	7	
98	Lockwasher, STL, CAP PL		MW-423-M	Waldom	7	7	
99	Screw No. 4 x 1/2		F-596-M	Waldom	16	16	
100	Screw No. 6 x 3/8		F-504-M	Waldom	7	7	

Ref. Des.	Description	LSI Part No.	Mfg. Part No. MIL Type Des.	Mfg. Code	Qty. 01 011	Note
101	Nut No. 4		F-557-M	Waldom	2 2	
102	Screw No. 4 x 1/2		F-021-M	Waldom	2 2	
103	FL. Washer No. 4		MW-401-M	Waldom	2 2	
104	L. Washer No. 4		MW-411-M	Waldom	2 2	
105	Insulator		43-77-1	Thermalloy	3 3	
106	Screw Insulator, Nylon		No. 4 x 1/32	Product Components Corporation	3 3	

SECTION 8

RETURNING EQUIPMENT FOR REPAIR

Equipment returned to LSI must be shipped prepaid and must have a Return Goods Authorization (RGA) number on the outside top of the carton or the shipment may be lost, misrouted or returned to you.

STEP 1

Prepare the following information:

Model type of equipment to be returned
Serial number
Reported symptom (if failure)
Type of modification or option to be installed (if applicable)

STEP 2

Please call (714) 774-1010 ext. 371 or write to

Lear Siegler Inc./EID
714 N. Brookhurst St.
Anaheim, Ca. 92803
Attn: Customer Service

Please state that you would like a Return Goods Authorization number. At this time, we will record the information you prepared as well as a purchase order number, if applicable.

STEP 3

You will then be provided with an RGA number and the address of the depot where we request that you return the equipment.

NOTE

All modifications and repairs are FOB Anaheim, California, or Philadelphia, Pennsylvania, whichever depot is used. Warranty repairs are to be sent to the repair depot with freight prepaid. They will be returned to you with the freight prepaid.

Section 9
PAINT

DRYING:

POLANE T®, catalyzed with POLANE® Catalyst V66 V 27, air-dries to touch and handle in 30-60 minutes, and can be force dried for 30 minutes at 180°-200°F. POLANE T® catalyzed with POLANE® Catalyst V66 V 29 air dries to touch and handle in 2-4 hours and can be force dried in 30 minutes at 200°-250°F.

POT LIFE:

POLANE T® is a two-component system — but this does not affect its production versatility. Finish coats have an 8 hr. working pot life after catalyzation. If it's necessary to "carry" catalyzed material over a week-end, simply add 80% uncatalyzed material to the mixture to extend pot life. On Monday, the required amount of catalyst is added.

PRECAUTIONS:

Do not spray hot. Heat will shorten pot life.

Do not pump from drums into circulating systems. Friction heat developed by pumps and circulation will shorten pot life.

Do not dip.

Do not flo-coat.

The catalyzing ratios as outlined have been established to provide optimum hardness, flexibility and chemical and solvent resistance. Slight over or under catalyzation will not seriously affect performance.

Excessive over catalyzation will result in increased hardness with marked brittleness and less flexibility. The gloss will also be increased. In the case of the spray fillers and glazing fillers, sanding will become more difficult.

Excessive under catalyzation will produce insufficient hardness, poor adhesion and poor chemical and solvent resistance.

POLANE T® should be applied only in well-ventilated areas. Wearing of a chemical cartridge respirator is recommended.

CHARACTERISTICS:

The tests below were conducted on standard POLANE T®quality. Test surface — Panels of Parker Bonderite 1000 with 1 to 1.2 mil dry film thickness of POLANE T®.

All tests conducted after fourteen days air curing period.

1. 5% salt spray — 500 hours, plus. Excellent
2. 100% relative humidity — 500 hours. No effect.
3. Water immersion — fresh, salt, distilled — 100 hours, plus. No effect.
4. Lacquer thinner, acetone, gasoline, Xylol resistance. 20 rubs with saturated cloth.
5. Excellent resistance to lubricating oils, coolants and phosphate ester hydraulic fluids.
6. 24 hours builing water. Excellent.
7. Cold check: 16 cycles; 24 hours, 100% humidity; 24 hours, −10°F; 24 hours −72°F. — excellent.
8. Pencil hardness — H to 2H.
9. Flexiblity — ⅛ inch conical mandrel. No effect.
10. Excellent abrasion resistance. Taber abrasion — CS17 wheel, 1000 gm. load: 2,500 revolutions/1 mil removal; 0.090 gm. loss/1,000 cycles.

Gloss — textured finish gloss range 10°-30°, measured on 60° photovoltmeter. Higher ranges are available.

APPLICATION CATALYZATION:

POLANE T® is a two-component finish, and must be catalyzed 6 parts base materials to 1 part POLANE® Catalyst V66 V 27 or V66 V 29. This mixture is then split into two batches — one for the smooth and one for the spatter coat that is necessary to obtain the textured effect.

Prior to application, the smooth base coat should then be reduced three parts catalyzed material to one part POLANE® Reducer R7 K 69.

The spatter coat is not reduced.

POLANE® Catalyst V66 V 27 is recommended for interior use. POLANE® Catalyst V66 V 29 is recommended for exterior use. The use of POLANE® Catalyst V66 V 27 on an exterior exposure would lead to premature chalking or loss of gloss. The POLANE® Catalyst V66 V 29 produces a more chalk resistant coating with excellent gloss retention. POLANE® Catalyst V66 V 29 does however increase the cure time requirement.

REDUCTION:

POLANE T® Reducer R7 K 69 is a medium to fast evaporating solvent recommended for reducing catalyzed POLANT T® first smooth coat to spraying viscosity.

For more specific information on the catalyzation and reduction of POLANE T® materials, follow instructions on the direction label or request a detailed data sheet on the particular POLANE T® material in question.

SPRAYING:

POLANE T® Base coat can be applied with standard pressure or suction feed spray equipment. The texture coat must use pressure equipment.

Polane T® First (Base) Coat

Pressure feed — Use DeVilbiss MBC gun with E tip and needle and No. 765 air cap.
5-8 p.s.i. fluid pressure.
40-45 p.s.i. atomizing pressure.

Suction feed — Use DeVilbiss MBC fun with E tip and needle and No. 30 air can.
40-50 p.s.i. atomizing pressure.

The smooth first coat should be sprayed to approximately 1 mil dry. Allow 5 minutes to flash-off before application of the spatter coat.

Polant T® — Second Texture Coat

Use DeVilbiss MBC gun with E tip and needle and No. 70 air cap or Binks No. 19 gun with 66-66PD nozzle combination.
15 p.s.i. fluid pressure.
15-20 p.s.i. atomizing pressure.

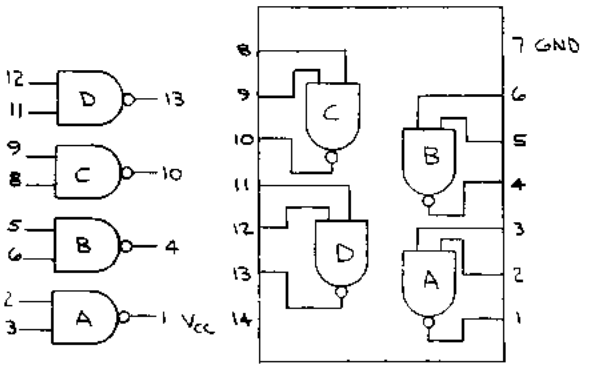
For application by Ransburg, DeVilbiss or Nordson electronstatic hand guns, the solvent balance can generally be adjusted to the proper polarity using R7 K 69 reducer to produce satisfactory wrap of base coat.

These adjustments will vary with the particular POLANE T® material involved, and specific recommendations should be requested from the laboratory before conducting trial runs or tests.

In regard to the texture coat, the texture may be varied by balancing the atomizing against the fluid pressure until the desired size is obtained. The lower the atomizing pressure, the larger the pattern. The flatness of the pattern can be set by adjusting the viscosity of the spatter coat. The lower the viscosity, the flatter the texture. Recommendations above indicate no reduction for the spatter coat to obtain an acceptable pattern: however, reduction may be necessary to obtain special effects. Once the variables — viscosity, atomizing and fluid pressure — have been set, it is a simple matter to obtain a consistent texture on each part.

APPENDIX A

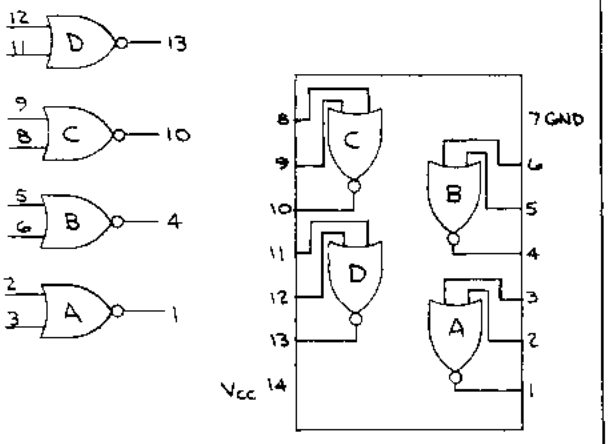
MFG. NO. SN7401N



HEX 1 NAND (OC)

SIZE	CODE IDENT		REV
A	98438	01	N/C
SCALE NONE		SHEET	

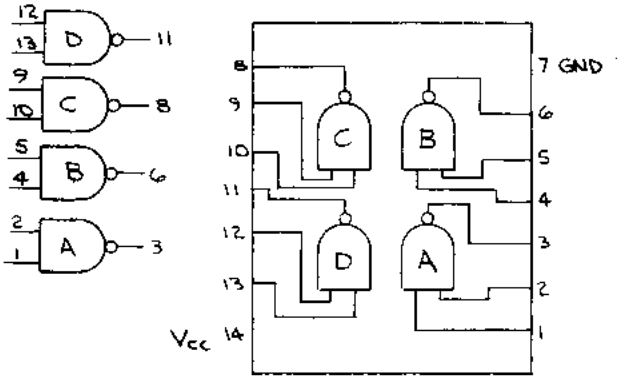
MFG. NO. SN7402N



QUAD 2 NOR

SIZE	CODE IDENT		REV
A	98438	02	N/C
SCALE NONE		SHEET	

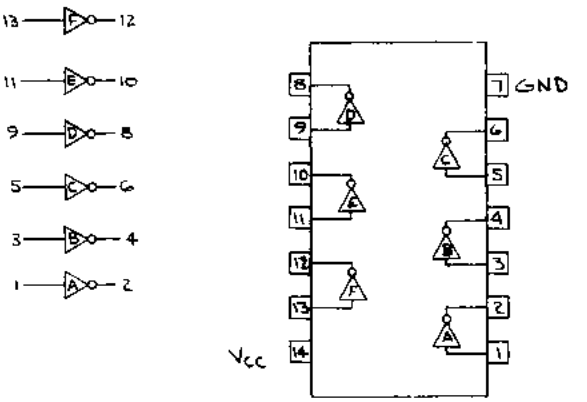
MFG. NO. SN7403N



QUAD 2 NAND (OC)

SIZE	CODE IDENT		REV
A	98438	03	N/C
SCALE NONE		SHEET	

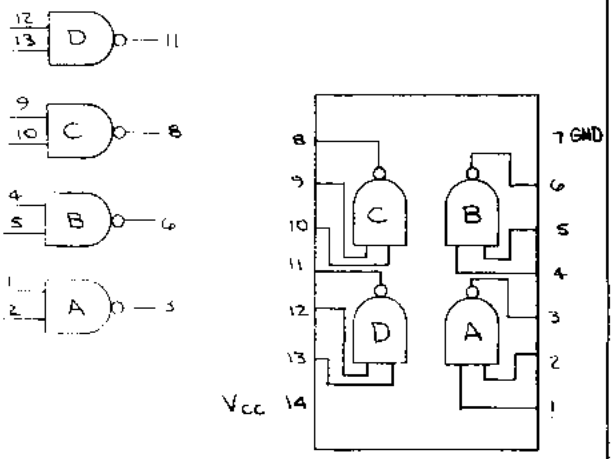
MFG. NO. SN74H04N
SN7404N
SN7405N



HEX 1 NAND

SIZE	CODE IDENT		REV
A	98438	04/05	N/C
SCALE NONE		SHEET	

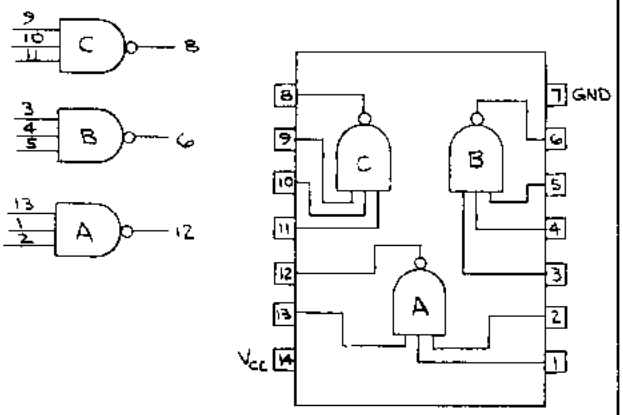
MFG. NO. SN74H01N
SN74H00N
SN7400N
SN7426N
N 8H80A



QUAD 2 NAND

SIZE	CODE IDENT			REV
A	98438	00 / 08	H01 / 26	N/C
SCALE NONE		SHEET		

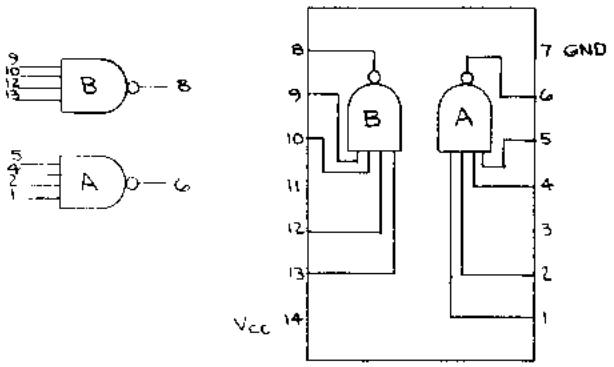
MFG. NO. SN74H10N
SN7410N
SN74H11N
U6A900359X



TRIPLE 3 NAND

SIZE	CODE IDENT		REV
A	98438	10/11	N/C
SCALE NONE		SHEET	

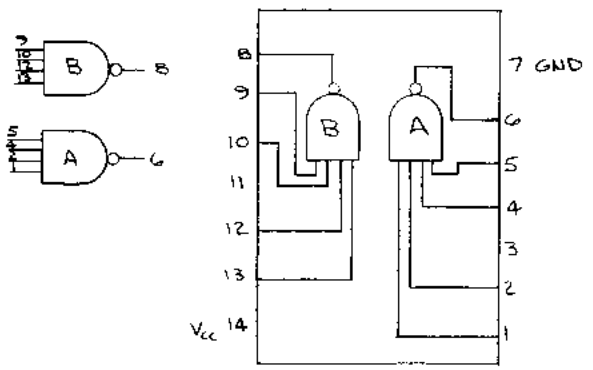
MFG. NO. SN74H20N
SN7420N
SN74H21N



DUAL 4 NAND

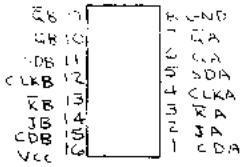
SIZE	CODE IDENT		REV
A	98438	20/21	N/C
SCALE NONE		SHEET	

MFG. NO. SN74H22N

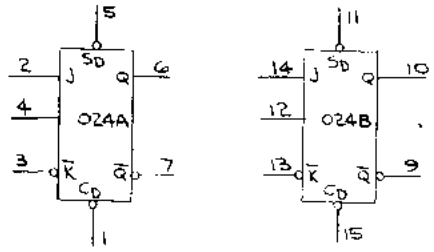


DUAL 4 NAND(OC)

SIZE	CODE IDENT		REV
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SCALE NONE		SHEET	



MFG. NO. U6B902459X

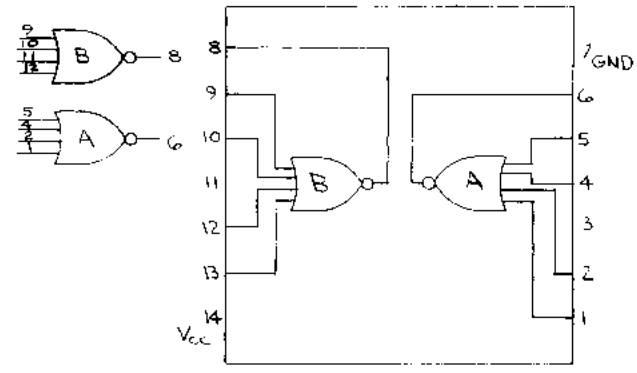


V_{CC} = PIN 16
GND = PIN 8

DUAL J-K F/F

SIZE	CODE IDENT		REV
A	98438	024	N/C
SCALE NONE		SHEET	

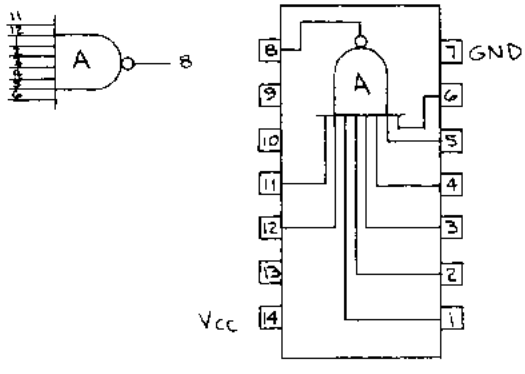
MFG. NO. 8815A



DUAL 4 NOR

SIZE	CODE IDENT		REV
A	98438	25/815	N/C
SCALE NONE		SHEET	

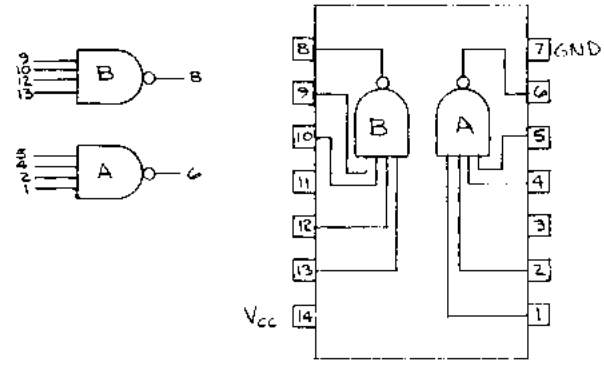
MFG. NO. SN74H30N
SN7430N



SINGLE 8 NAND

SIZE	CODE IDENT		REV
A	98438	30	N/C
SCALE NONE		SHEET	

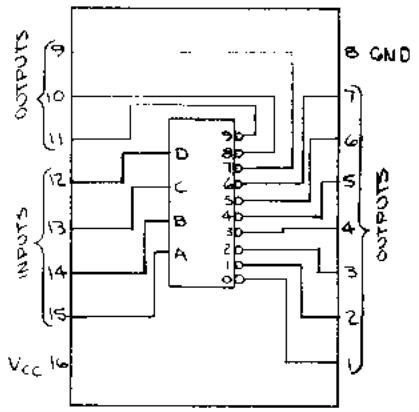
MFG. NO. SN74H40N
SN7440N



DUAL 4 NAND BUFFER

SIZE	CODE IDENT		REV
A	98438	40	N/C
SCALE NONE		SHEET	

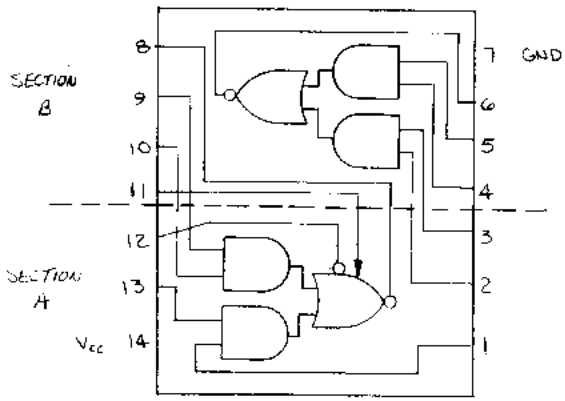
MFG. NO. SN7442N



1 OF 10 DECODER

SIZE	CODE IDENT		REV
A	98438	42	W
SCALE NONE		SHEET	

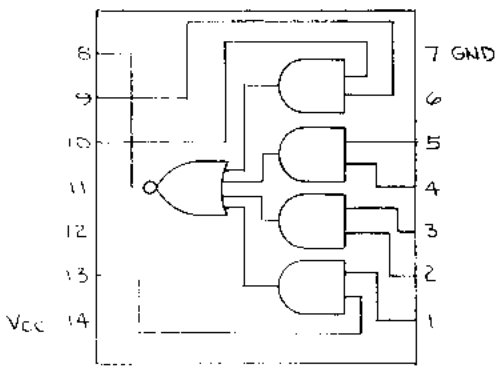
MFG. NO. SN74H51N



DUAL 2 AND/OR

SIZE	CODE IDENT		REV
A	98438	H51	
SCALE		SHEET	

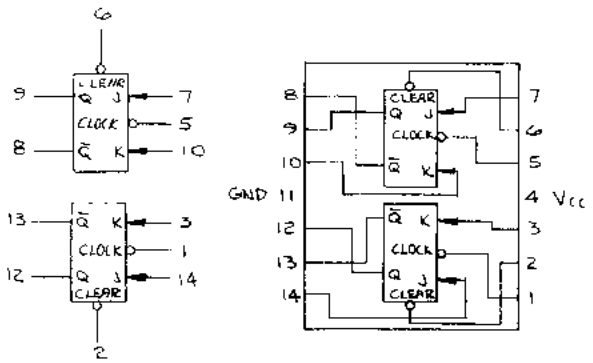
MFG. NO. SN7454 N



4-WIDE 2-INPUT AND-OR-INVERT GATE

SIZE	CODE IDENT		REV
A	98438	54	
SCALE NONE		SHEET	

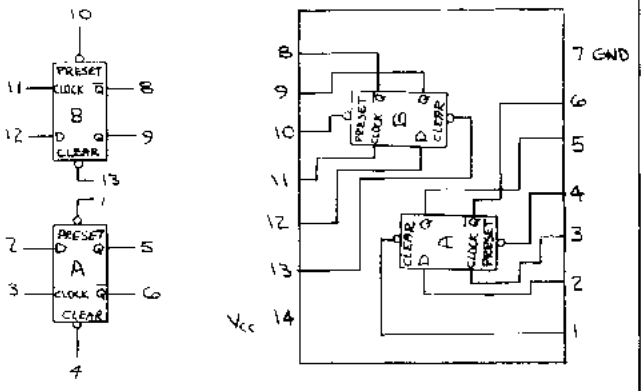
MFG. NO. SN7473N



DUAL J-K MASTER-SLAVE FLIP-FLOP

SIZE	CODE IDENT		REV
A	98438	73	
SCALE NONE		SHEET	

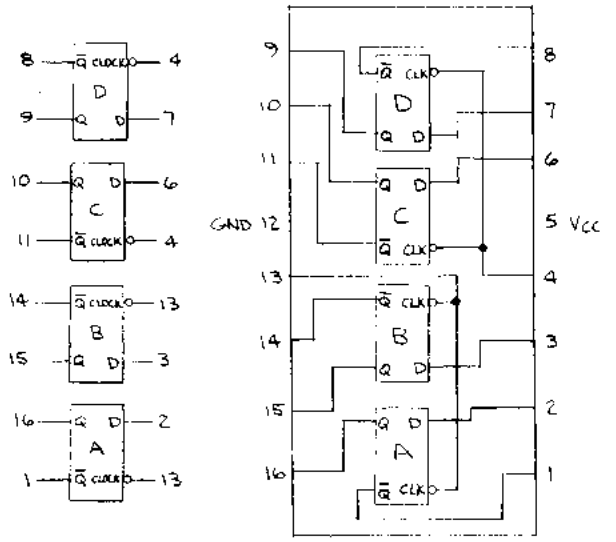
MFG. NO. SN7474N



DUAL D FLIP-FLOPS

SIZE	CODE IDENT		REV
A	98438	74	N/C
SCALE NONE		SHEET	

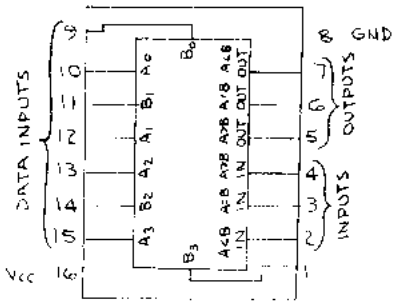
MFG. NO. SN7475N



4 BIT BISTABLE LATCH

SIZE	CODE IDENT		REV
A	98438	75	N/C
SCALE NONE		SHEET	

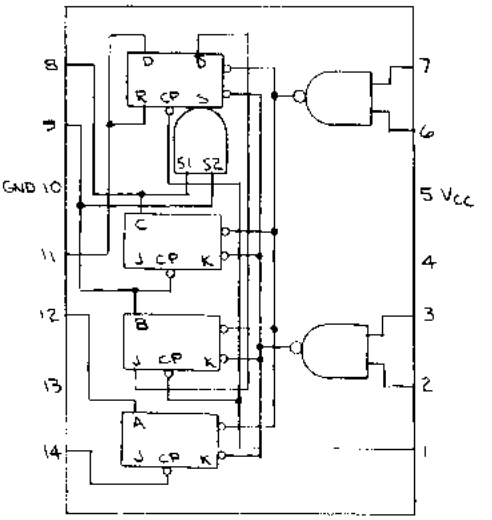
MFG NO. SN74H85



4-BIT COMPARATOR

SIZE	CODE IDENT		REV
A	98438	H85	
SCALE		SHEET	

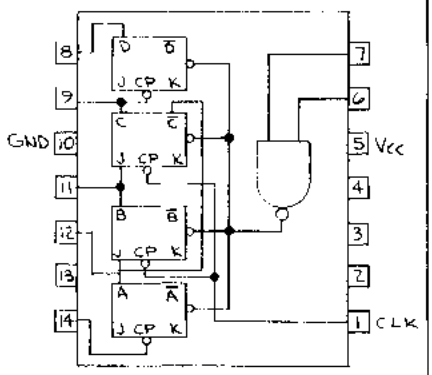
MFG NO. SN7490N



DECADE CTR

SIZE	CODE IDENT		REV
A	98438	90	N/C
SCALE NONE		SHEET	

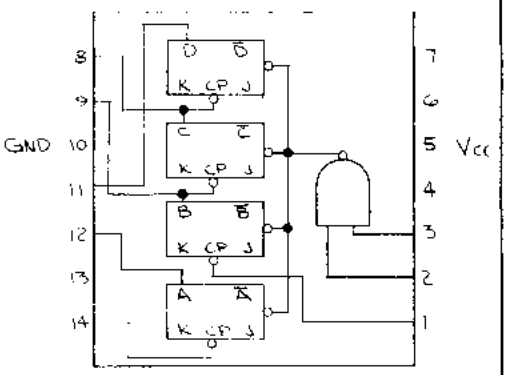
MFG. NO. SN7492N



÷12 CTR

SIZE	CODE IDENT		REV
A	98438	92	N/C
SCALE NONE		SHEET	

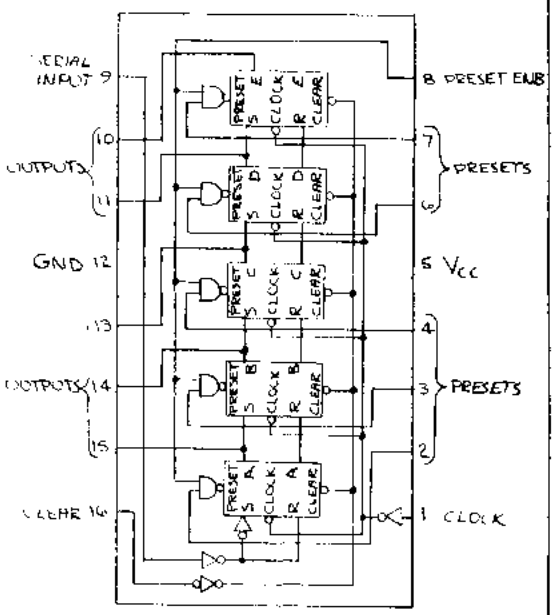
MFG. NO. SN7493N



4-BIT BINARY COUNTER

SIZE	CODE IDENT		REV
A	98438	93	
SCALE NONE		SHEET	

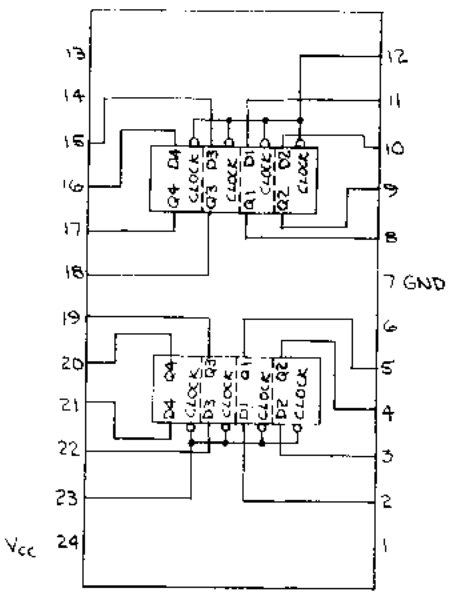
MFG. NO. SN7496N



5-BIT SHIFT REG

SIZE	CODE IDENT		REV
A	98438	96	N/C
SCALE NONE		SHEET	

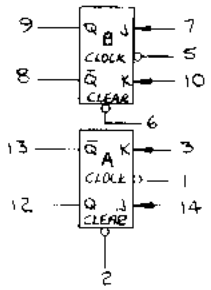
MFG. NO. SN74100N

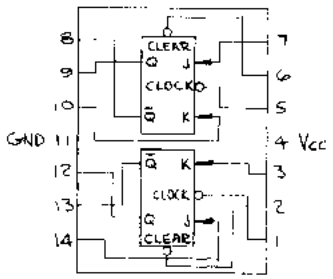


8-BIT BISTABLE LATCH

SIZE	CODE IDENT		REV
A	98438	100	N/C
SCALE NONE		SHEET	

MFG. NO. SN74H103N

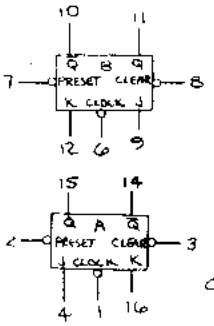


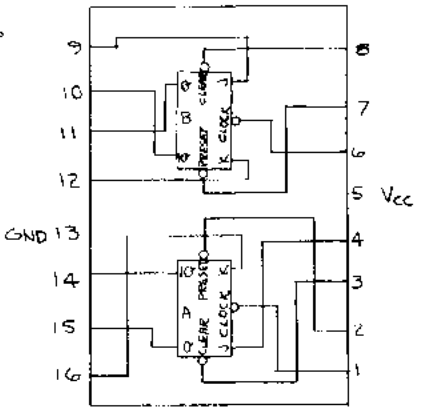


DUAL J-K FLIP-FLOP

SIZE	CODE IDENT		REV
A	98438	H 103	
SCALE NONE		SHEET	

MFG. NO. SN74H106N

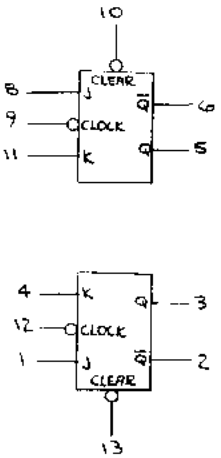


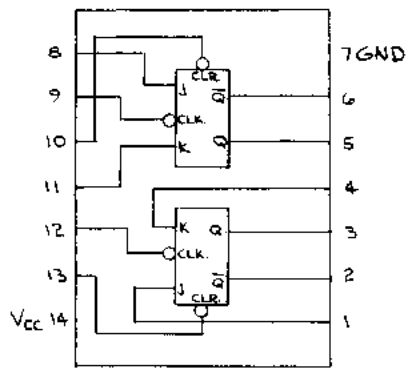


DUAL J-K FLIP-FLOPS

SIZE	CODE IDENT		REV
A	98438	H106	N/C
SCALE NONE		SHEET	

MFG. NO. SN74107N

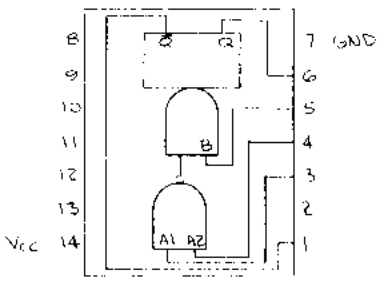




DUAL J-K F/F

SIZE	CODE IDENT		REV
A	98438	107	N/C
SCALE NONE		SHEET	

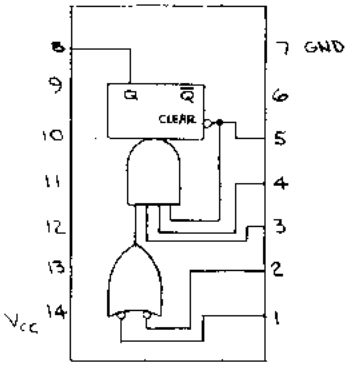
MFG NO SN74121N



MONOSTABLE MULTIVIBRATOR

SIZE	CODE IDENT		REV
A	98438	121	
SCALE NONE		SHEET	

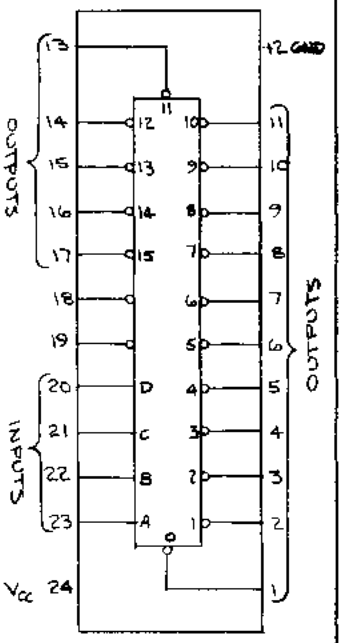
MFG NO. SN74122N
U6A9660159X



ONE SHOT

SIZE	CODE IDENT		REV
A	98438	122	N/C
SCALE NONE		SHEET	

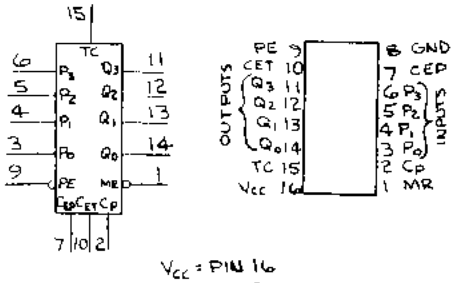
MFG. NO. SN74154N



1 OF 16 DECODER

SIZE	CODE IDENT		REV
A	98438	154	N/C
SCALE NONE		SHEET	

MFG. NO. U6B9316659X
U6B9310159X
74161N

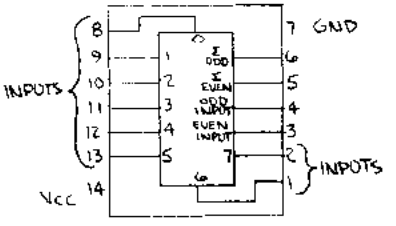


V_{CC} = PIN 16
GND = PIN 8

BINARY HEX. CTR.

SIZE	CODE IDENT		REV
A	98438	161	N/C
SCALE NONE		SHEET	

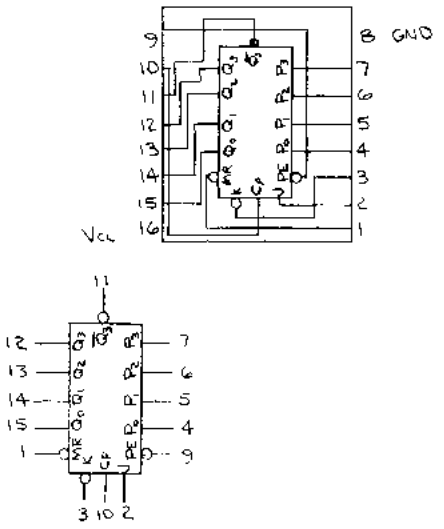
MFG. NO. SN74180



PARITY GENERATOR

SIZE	CODE IDENT		REV
A	98438	180	
SCALE NONE		SHEET	

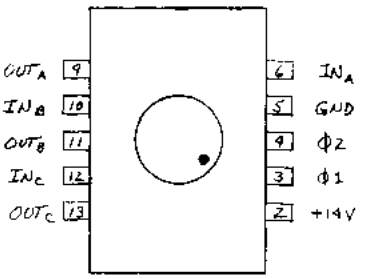
MFG. NO. UGB930059X



UNIVERSAL SHIFT REG

SIZE	CODE IDENT		REV
A	98438	300	
SCALE		SHEET	

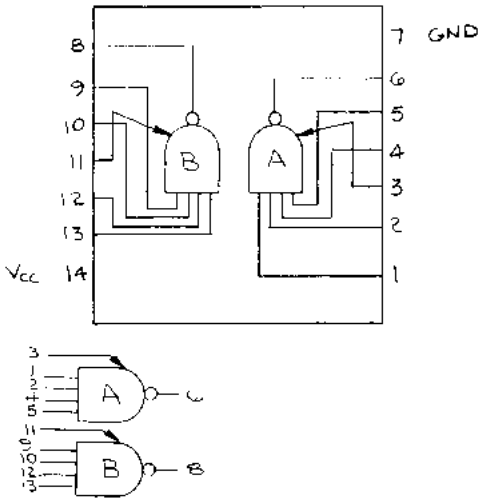
TMS 3304 LR



TRIPLE 66 SR

304

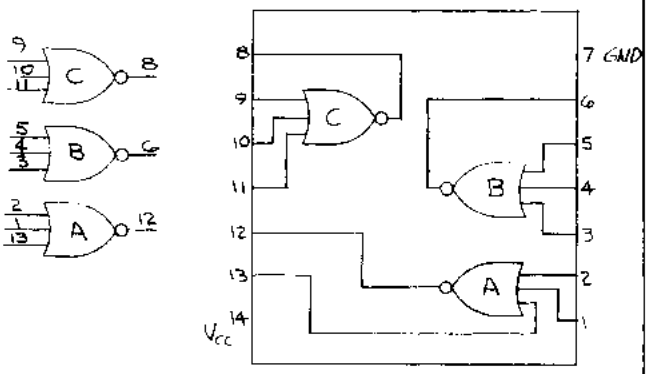
MFG. NO. 8416A



DUAL 4 NAND-EXP

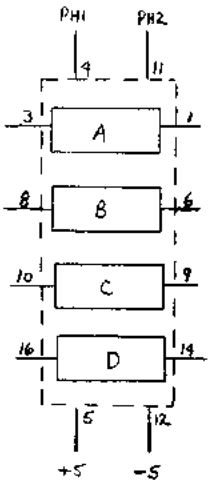
SIZE	CODE IDENT		REV
A	98438	416	
SCALE		SHEET	

MFG. NO. 8875A
SN7427N



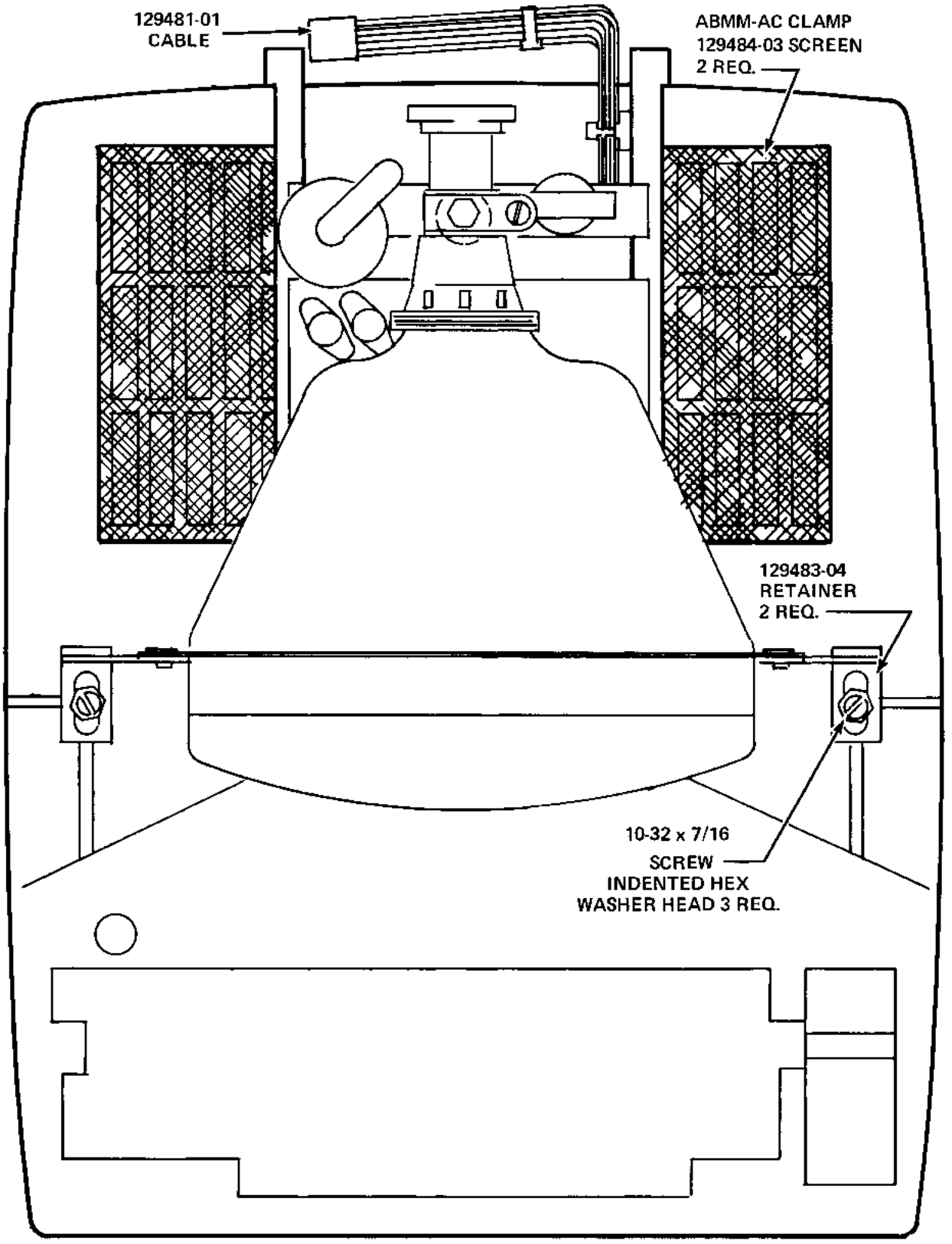
TRIPLE 3 NOR

SIZE	CODE IDENT		REV
A	98438	875/27	NL
SCALE NONE		SHEET	

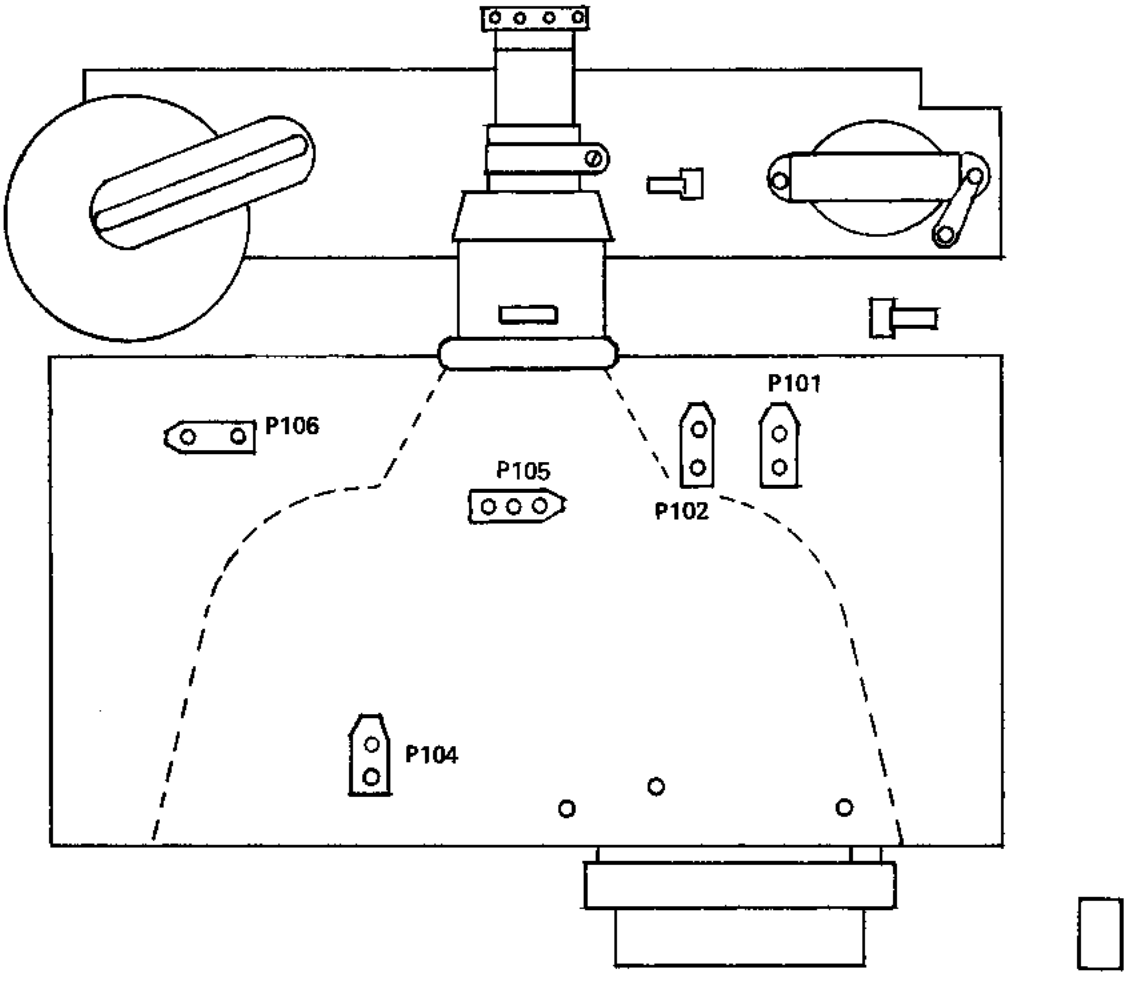


1402

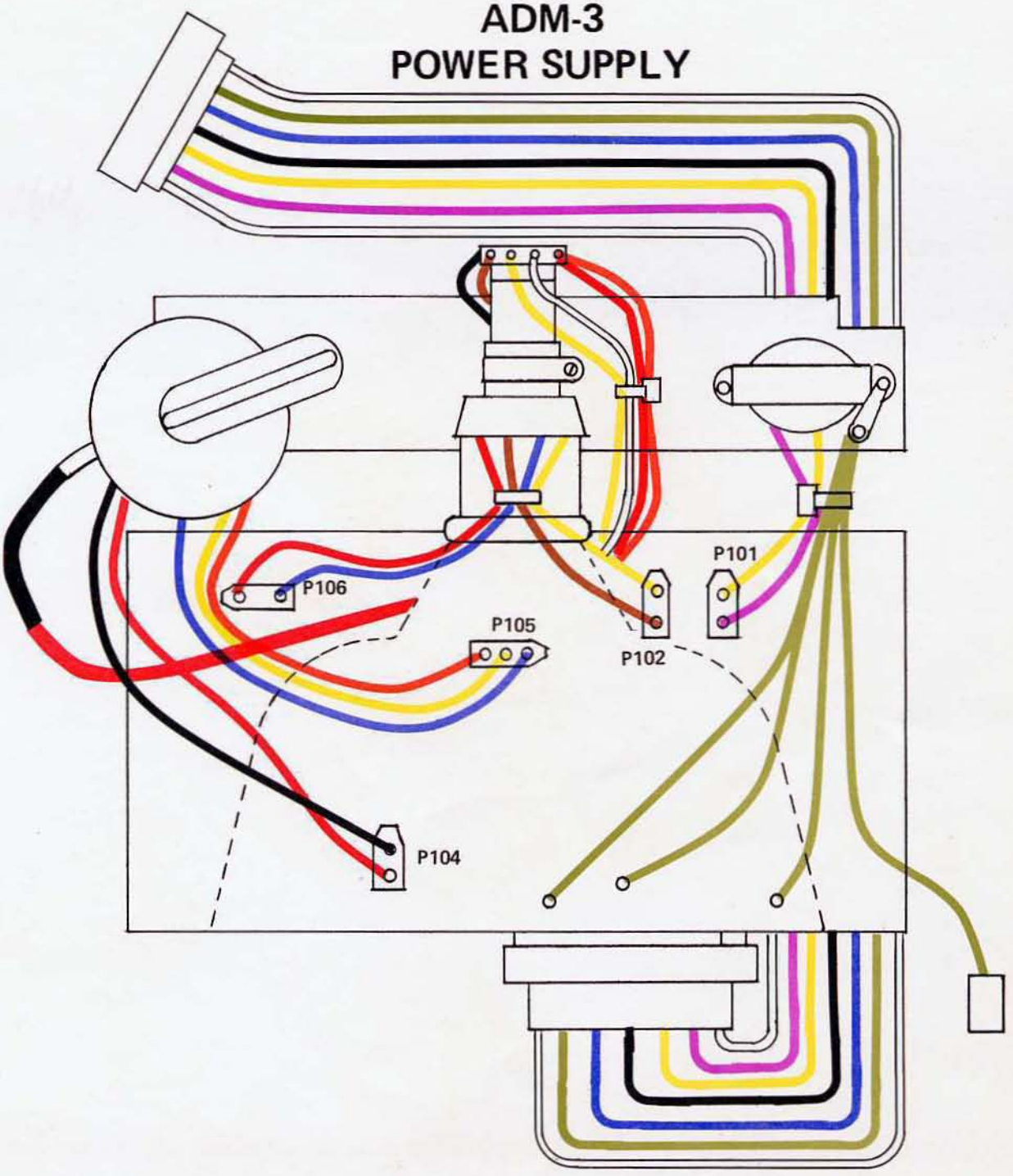
APPENDIX B


129481-01
CABLE
ABMM-AC CLAMP
129484-03 SCREEN
2 REQ.
129483-04
RETAINER
2 REQ.
10-32 x 7/16
SCREW
INDENTED HEX
WASHER HEAD 3 REQ.

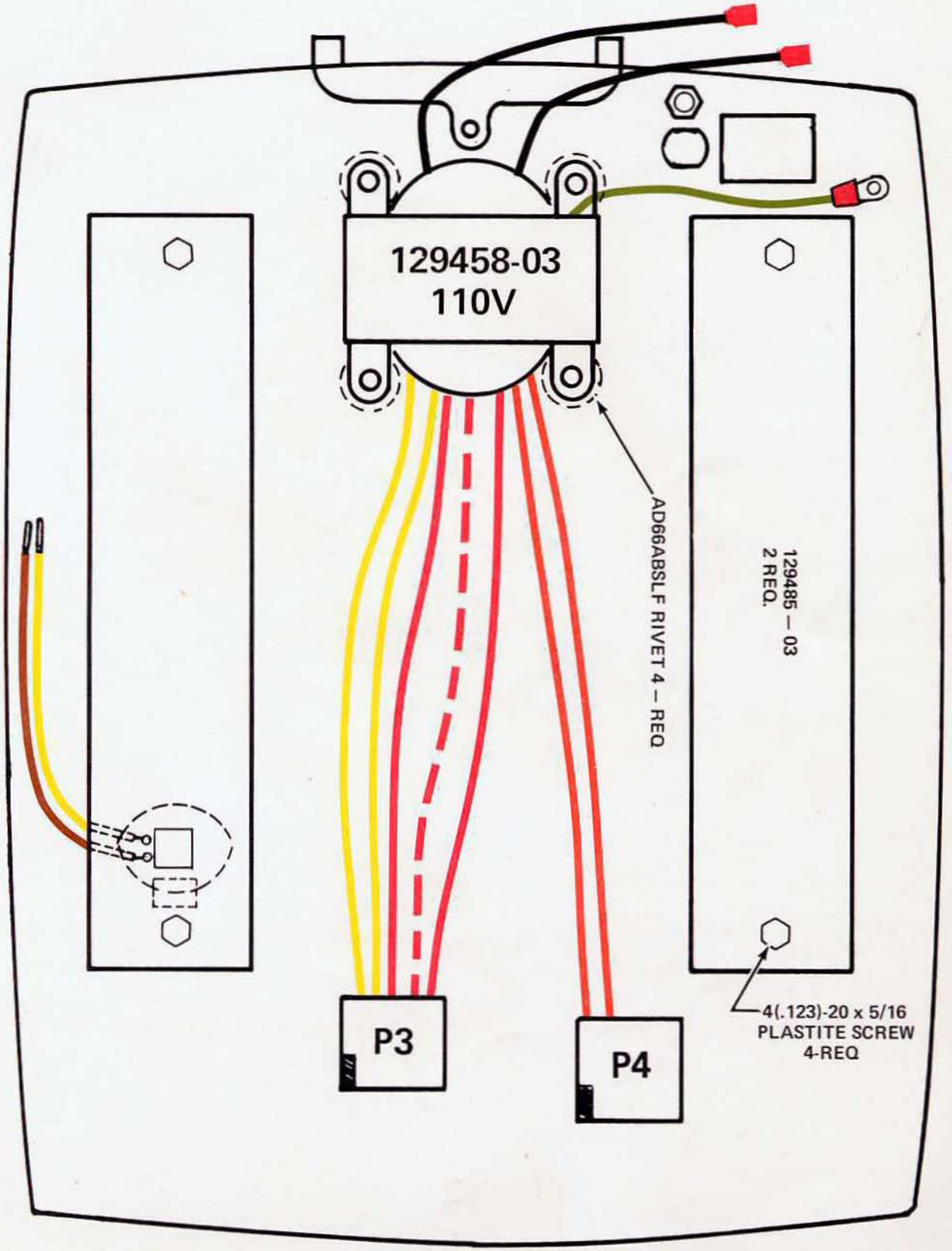
ADM-3
POWER SUPPLY



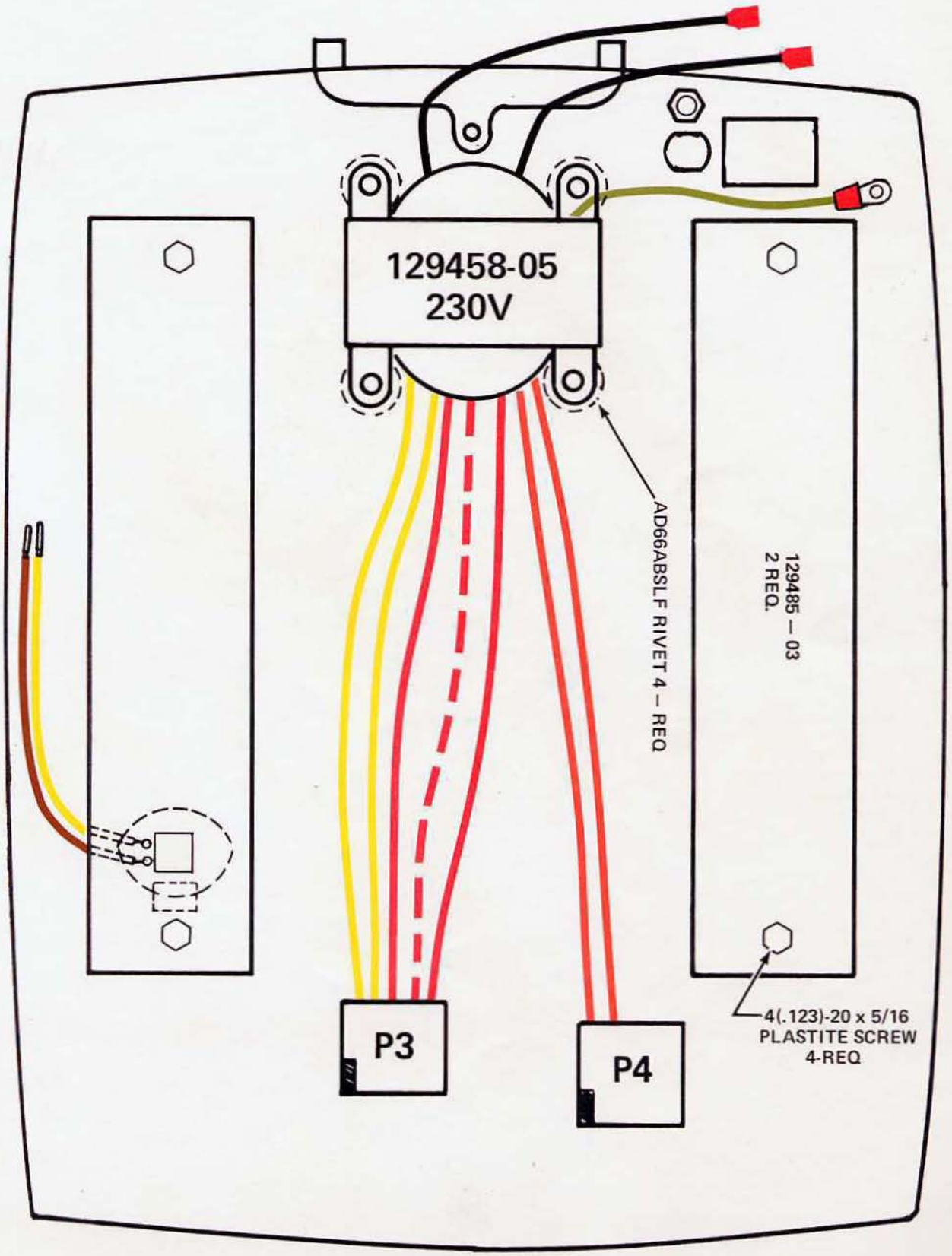
ADM-3
POWER SUPPLY



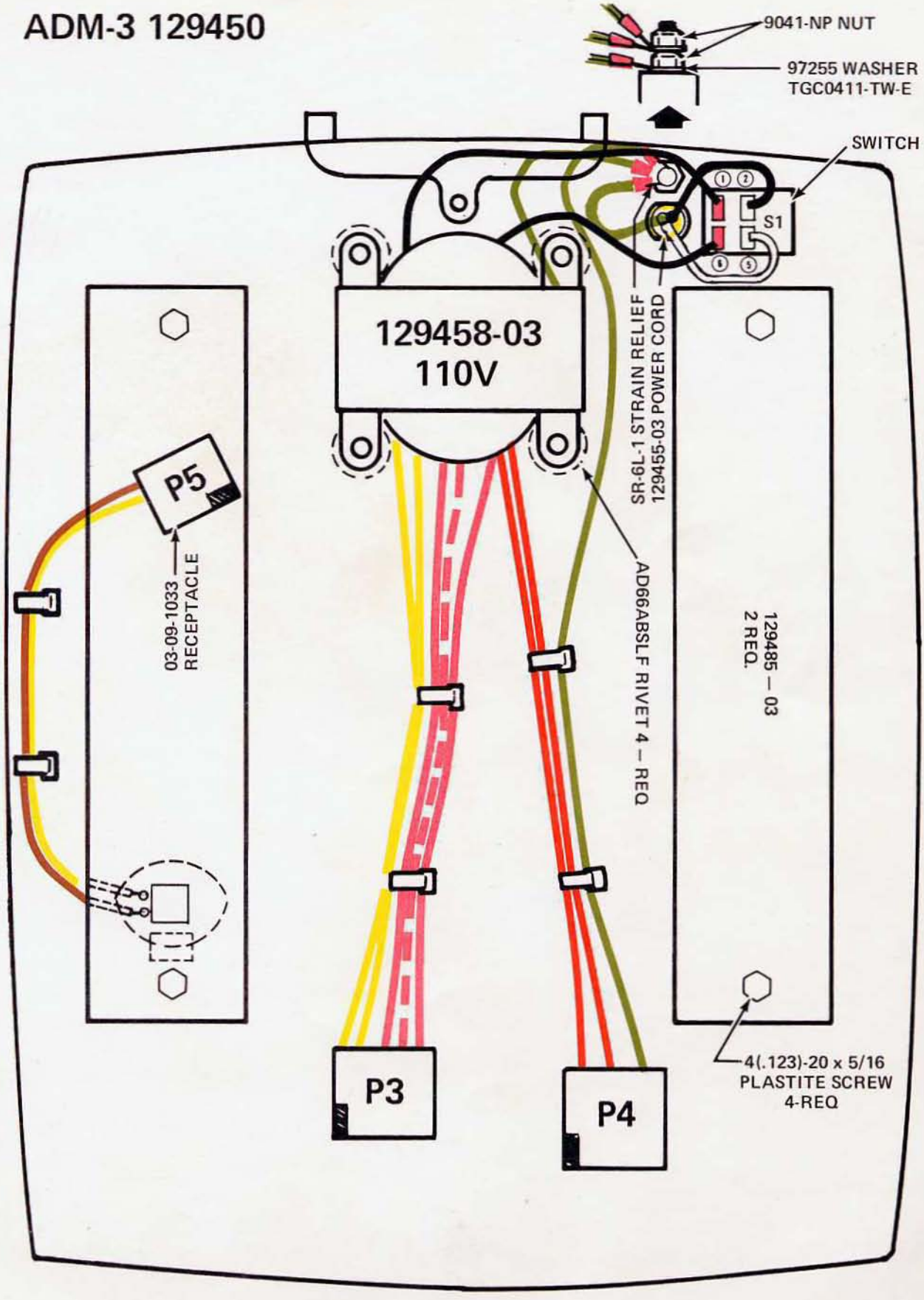
ADM-3 129450


129458-03
110V
AD66ABSLF RIVET 4 – REQ
129485 – 03
2 REQ.
P3
P4
4(.123)-20 x 5/16
PLASTITE SCREW
4-REQ

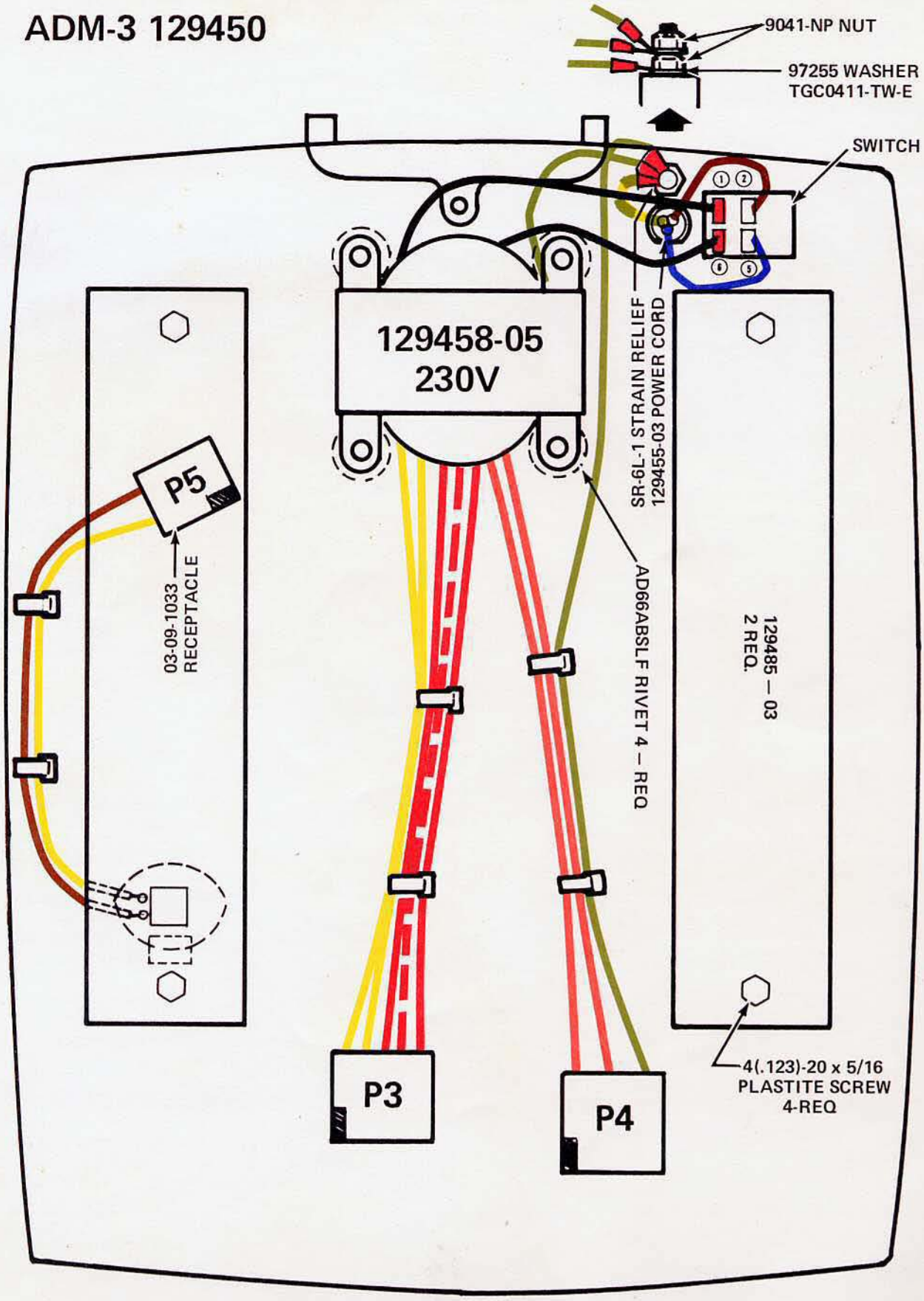
ADM-3 129450


129458-05
230V
AD66ABSLF RIVET 4 – REQ.
129485 – 03
2 REQ.
P3
P4
4(.123)-20 x 5/16
PLASTITE SCREW
4-REQ

ADM-3 129450


9041-NP NUT
97255 WASHER
TGC0411-TW-E
SWITCH
S1
129458-03
110V
SR-6L-1 STRAIN RELIEF
129455-03 POWER CORD
AD66ABSLF RIVET 4 — REQ
129485 — 03
2 REQ.
P5
03-09-1033
RECEPTACLE
P3
P4
4(.123)-20 x 5/16
PLASTITE SCREW
4-REQ

ADM-3 129450


9041-NP NUT
97255 WASHER
TGC0411-TW-E
SWITCH
129458-05
230V
SR-6L-1 STRAIN RELIEF
129455-03 POWER CORD
AD99ABSLF RIVET 4 — REQ
129485 — 03
2 REQ.
P5
03-09-1033
RECEPTACLE
P3
P4
4(.123)-20 x 5/16
PLASTITE SCREW
4-REQ

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