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TECHNICAL DATA

LeCroy

2228A HIGH PRECISION TIME-TO-DIGITAL CONVERTER
2229 HIGH PRECISION TDC, ECL INPUTS
4204 MULTISOURCE TDC, SINGLE CHANNEL
4208 MULTIHIT TDC, WIDE RANGE

- Full Scale Ranges from 100 nsec to 167 msec
- LSB from 30 psec to 2.56 µsec
- Single and Multiple Input Digitizers
- Single Hit, Multihit and Multisource Devices
- No (Real Time) or Very Low Conversion Time
- NIM, TTL and ECL Signal Level Compatibility

WWW - LeCroy Data Sheet

FLEXIBLE CONFIGURATIONS FOR PRECISE MEASUREMENTS

LeCroy time digitizers offer precise, fast measurements of time intervals in a large variety of industrial, government laboratory and university research environments. Applications for LeCroy time digitizers include time-of-flight spectroscopy, particle beam accelerator monitoring, Muon Spin Rotation measurements, laser induced chemical studies and digital signal analysis.

Electronic time interval measurement involves digitizing the time between two or more pulses. The first pulse is usually called START and the latter called STOP. For many devices a single COMMON input is used, against which INDIVIDUAL inputs are timed. Other configurations may also be employed. A MULTIHIT digitizer accepts a COMMON input, then digitizes several INDIVIDUAL pulses which arrive on the same cable. A second variation is called MULTISOURCE, where many inputs are present but only the first to arrive is digitized.

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2228A Precision Time-to-Digital Converter
2229 Precision TDC, ECL Inputs
4208 Multihit TDC, Wide Range

- Full Scale Ranges from 100 nsec to 8.3 msec
- LSB from 30 psec to 1 nsec
- Single Hit, Multihit Devices
- No Conversion Time (Real Time) or Very Low Conversion Time
- NIM and ECL Signal Level Compatibility

FLEXIBLE CONFIGURATIONS FOR PRECISE MEASUREMENTS

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FUNCTIONAL DESCRIPTION

Model 2228A and Model 2229 Octal Time Digitizers

The LeCroy Models 2228A and 2229 are Octal Time Digitizers packaged in single-width CAMAC modules. Internally, the 2228A and 2229 are identical. They differ only in that the 2228A accepts NIM level inputs while the 2229 requires complementary ECL (Emitter Coupled Logic) logic levels.

The Models 2228A and 2229 have eight independent channels, each of which measures the time from the leading edge of a common START pulse to the leading edge of its individual STOP pulse. Each channel disregards any STOP pulses received before a START signal and will accept only one STOP for every START.

Conversion begins upon receipt of the START signal and proceeds until one of the following: a STOP

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signal is received; the cycle is terminated by the application of a front-panel CLEAR signal; or the digitizer reaches full scale.

The 2228A or 2229 converts the measured time intervals into 11-bit digital numbers using a 20 MHz internal clock for a full-scale digitizing time of 100 µsec. Rear-panel control of full scale and conversion slope permits digitization to fewer bits and correspondingly shorter conversion time if desired. The conversion clock is started in phase with the TDC start signal to assure synchronization and eliminate the inaccuracy introduced by the free-running oscillators in conventional designs. A CAMAC LAM (Look-At-Me), if enabled, is generated at the end of the conversion interval to signal readout.

Three switch-selectable full-scale time ranges, 100, 200 and 500 nsec, are digitized to 95% of 11 bits (2048 counts) and provide 50, 100 and 250 psec resolutions respectively. Longer time ranges (up to 10 µsec) may be provided on request at slight expense of stability and accuracy.

On-line testing is facilitated by either a front-panel COMMON STOP input or by a CAMAC command. A signal at the COMMON STOP input generates simultaneous stops for each channel, permitting accurate testing of the module.

Excessive system dead time due to false starts may be eliminated through use of the FAST CLEAR input. Accepting NIM level signals, this input allows the digitizer to be cleared at any point in its conversion cycle without the necessity for CAMAC operations.

Model 4208 Wide Range, Octal Time Digitizer

The LeCroy Model 4208 Time Digitizer is designed to cover applications where time measurements must be performed in real time, and which require wide dynamic range with high resolution.

The 4208 has eight independent channels. Each one measures the time from the leading edge of a COMMON input to the leading edge of its INDIVIDUAL input pulse.

Common Start Input Mode as well as Common Stop Input Mode can be used. The digitizer will encode input pulses preceding the COMMON input as negative times and input pulses arriving after the COMMON input as positive times.

The 4208 also may operate as a single input, 8-hit time digitizer. In this strap-selectable mode, all eight inputs are cascaded. As each input is hit, it enables the next one. The unit may also be configured as two 4-hit time digitizers, four 2-hit digitizers or as any of several other combinations of inputs and hits.

The 4208 converts the measured time intervals into a 23-bit digital word plus a sign bit. The sign bit indicates whether or not the COMMON input has preceded or followed the INDIVIDUAL input. The dynamic range is ±8.3 msec (which can be expanded with an external clock and appropriate logic circuits). See LeCroy Application Note AN-4002.

The module is equipped with a high stability crystal-controlled 125 MHz clock. The 1 nsec resolution is achieved by digital interpolation between two clock pulses. Dead time after an event has occurred is negligible and data readout can occur immediately after the event. An external clock input is provided to permit synchronous operation of several modules with an external 125 MHz time base.

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Note that several other TDCs are available from LeCroy. Please see the TDC table at the end of this data sheet.

SPECIFICATIONS

Model 2228A and 2229

2228A INPUTS

Stop Inputs: 8, one per channel, 50 ohm impedance; Lemo-type connectors; direct-coupled; input amplitude > -450 mV; ineffective unless preceded by a "Start" input. Can be cascaded by factory modification for multihit operation.

Common Start Input: One, common to all channels, 50 ohm impedance; Lemo-type connector; input amplitude > -450 mV.

Common Stop Input: One, common to all channels, 50 ohm impedance; Lemo-type connector; input amplitude > -450 mV; functions identical to individual "Stop Inputs" above; used for on-line testing.

Fast Clear: One input, common to all channels; Lemo-type connector; 50 ohm impedance; -450 mV or greater clears; minimum duration 50 nsec. Requires 1.4 µsec after start of clear signal to settle to 1 ±1 counts. (However, if the unit is always cleared at a fixed time before each start, it will settle to a constant offset with a small uncertainty, effectively permitting fast reset times on the order of 500 nsec.)

2229 INPUTS

Stop Inputs: 8, using a 2 x 8 pin connector (mates with LeCroy 403211016 or 3M 3452-6016 or equivalent); accepts differential ECL input levels; 110 ohm input impedance pin-to-pin; direct-coupled; inputs ignored unless preceded by a "Start" input.

Common Start Input: One, common to all channels, using a pin pair on the control group, 2 x 8 pin connector (mates with LeCroy 403211016 or 3M 3452-6016 or equivalent); accepts differential ECL input levels; 112 ohm input impedance pin-to-pin; direct-coupled; 5 nsec minimum width.

Common Stop Input: One, common to all channels, input characteristics identical to Common Start. Functions identical to the individual "Stop Inputs" above, used for on-line testing.

Fast Clear: One input, common to all channels; input characteristics identical to Common Stop except50 nsec minimum width. Requires 1.4 µsec after start of clear signal to settle to 1 ±1 counts. (However, if the unit is always cleared at a fixed time before each start, it will settle to a constant offset with a small uncertainty, effectively permitting fast reset times on the order of 500 nsec.)

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2228A and 2229 GENERAL

Full Scale Time Range: 11-bit binary output corresponds to 100, 200, and 500 nsec nominal, switch-selectable (with longest range field-adjustable up to 1 µsec). Larger full scales possible by factory option up to 10 µsec (specify MOD200 for 1, 2, & 5 µsec full scale). Shorter range of 60 nsec is available as a factory option (2229/400). Both the full scale value and conversion slope are rear-panel adjustable, permitting faster conversion at the expense of range.

Integral Non-linearity: < ±2 counts (20 nsec to full scale).

Differential Non-linearity: Channel widths vary by < ±10% (10 nsec to full scale); < ±30% for long-range option.

Time Resolution: 50 psec on 100 nsec range; 100 psec on 200 nsec range; 250 psec on 500 nsec range. Internal adjustments allow 500 psec resolution with 1 µsec full scale. A 30 psec resolution is available as factory option 2229/400.

Temperature Coefficient: Typically (±0.02% of full scale ±0.01% of reading) per degree C.

Digitizing Time: Approximately 100 µsec for 11 bits; rear-panel adjustable for fewer bits, shorter conversion time.

Readout Time: Readout may proceed at the fastest rate permitted by the CAMAC standard after digitizing is complete.

Test Functions: An internal start/stop is generated with approximately 80% of full scale time in response to an F(25) command. On-line testing and calibrations can be done with common start and common stop above.

Data: The proper CAMAC function and address command gates the binary data of the selected channel onto the R(1) to R(11) (20 to 210) dataway bus lines. The full scale number of bits, and thus the conversion time, can be selected by a rear-panel pot and test point. (Conversion curve provided with unit.) The overflow flag is always presented on R(12).

Q and LAM Suppression: A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The Q and LAM suppress features can be disabled with side-panel switches.

Packaging: In conformance with CAMAC standard for nuclear modules. (ESONE Report EUR4100 or IEEE Report #583.) RF-shielded CAMAC #1 module.

Power Requirements: 25 mA at +24 V; 140 mA at -24 V; 600 mA at +6 V; 600 mA at -6 V.

Model 4208

INPUTS

8 Individual Inputs: One Lemo-type connector per channel, impedance 50 ohm; protected to ±3 A for

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0.5 µsec, clamping at +6 V and -6 V; each input is followed by a fast discriminator, minimum input pulse width is 4 nsec threshold is common to the 8 channels and is adjustable by a front-panel potentiometer (IND TH) from -1.5 V to +1.5 V; threshold precision ±20 mV; 10 x threshold monitor on the front-panel. Multihit selectable by internal straps.

Common Input (COMMON): One Lemo-type connector, impedance 50 ohm; protected to ±3 A for 0.5 µsec, clamping at +6 V and -6 V; the input is followed by a fast discriminator, minimum input pulse width is 4 nsec threshold adjustable by a front-panel potentiometer (TH) from -1.5 V to +1.5 V; 10 x threshold monitor on the front-panel.

Individual Veto Inputs (IND): Two bridged Lemo-type connectors, high input impedance; accepts NIM levels; the eight individual inputs are inhibited for the duration of the veto; active for the first hit only in multihit mode.

Common Veto Inputs (VTO): Two bridged Lemo-type connectors, high input impedance; accepts NIM levels; the common input is inhibited for the duration of the veto.

End of Time Window (EDW): Two bridged Lemo-type connectors, high input impedance; accepts NIM level pulses; LAM is generated in response to the leading edge allowing readout of the unit. Internal monostable provided, range adjustable from 0.2 to 8 msec (set at factory to 8 msec); OR'd with the external EDW input; can be disabled via internal strap.

Fast Clear Input (CLR): Two bridged Lemo-type connectors, high input impedance; accepts NIM levels; the unit is ready to operate approximately 50 nsec after the trailing edge of the Fast Clear Input. Clear input width: > 50 nsec. Does not clear the LAM.

External Clock Input (CK IN): Two bridged Lemo-type connectors, high input impedance; NIM input active in external clock mode only. Permits absolute time accuracy improvement, and time range expansion (clock suppression during "no event dead time"). Note: If the duty cycle of external clock is not 50% ±5%, time linearity can be affected.

OUTPUTS

Busy Output (B and B): Two Lemo-type connectors; two NIM levels are started by a nine-input OR of the eight individual inputs and the common input, and are stopped by the clear; allow various input veto logic combinations; complementary outputs are provided.

GENERAL

Integral Non-Linearity: ±1 count.

Dynamic Range: 23 bits + 1 bit for sign.

Resolution: ±1 nsec.

Encoding Time: None, the time is encoded in real time.

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Multihit Dead Time: Inherent dead time (time reference at front-panel Lemo-type connector); 3 nsec typical.

Packaging: Single width CAMAC standard module.

Power Requirements: 1.5 A at +6 V; 3.3 A at -6 V; 17 mA at +24 V; 17 mA at -24 V.

CAMAC COMMANDS

Model 2228A and Model 2229 Octal Time Digitizers

CAMAC COMMANDS

Z or C: All registers are simultaneously cleared by the CAMAC "Clear" or "Initialize" command. Requires "S2". "Start" input is inhibited during CAMAC "inhibit" command.

Q: A Q = 1 response is generated in recognition of an F0 or F2 Read function, or an F8 function if LAM is set for a valid "N" and "A", but there will be no response (Q = 0) under any other condition. The Q response for empty modules is suppressed (see Q and LAM suppression).

X: An X = 1 (Command Accepted) response is generated when a valid F, N and A command is generated.

L: A Look-At-Me signal is generated from end of digitizing until a module Clear or Clear LAM. LAM is disabled for duration of N, can be permanently enabled or disabled by the Enabled or Disable function command, and can be tested by Test LAM. Switch-selectable option causes LAM to be suppressed by empty modules.

CAMAC FUNCTION CODES

F(0): Read registers; requires N and A; A(0) through A(7) are used for channel address.

F(2): Read registers and clear module; requires N, A and S2. Clears on A(7) only.

F(8): Test Look-At-Me; requires LAM, N and any A from A(0) to A(7). Q is generated if LAM is present and enabled.

F(9): Clear module (and LAM); requires N and any A from A(0) to A(7) and S2.

F(10): Clear Look-At-Me; requires N, S2 and any A from A(0) to A(7).

F(24): Disable Look-At-Me; requires N, S2, and any A from A(0) to A(7).

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F(25): Test module; requires N, S2 and any A from A(0) to A(7).

F(26): Enable Look-At-Me; requires N, S2 and any A from A(0) to A(7). Remains enabled until Z or F (24) applied.

Caution: The state of the LAM mask will be arbitrary after power turn-on.

Q and LAM SUPPRESSION

A module receiving no stop inputs will produce no Q response or LAM and appears during readout as an empty CAMAC slot, thus reducing readout time. A Command Accepted response is still generated. The Q and LAM suppress features can be disabled with side-panel switches.

Bit 21: Set if a second pulse arrives on the same multi-source input channel that was first hit (double pulse resolution 50 nsec).

F(2)·A(0-3): Reads time interval data (24 bits) at S1, resets register and LAM at S2.

F(2)·A(8): Same as F(2)·A(0-3) plus starts test "0" at S2; a subsequent read function will read the result of the test.*

F(2)·A(9): Same as above, but for test "1".*

F(2)·A(10): Same as above, but for test "2".*

F(2)·A(11): Same as above, but for test "3".*

**The tests defined above are mainly for calibration purposes and not for normal customer use.*

F(8)·(0-3): Tests LAM, Q response if LAM on.

F(9)·A(0-3): Sets the router register to zero; in multi-source mode, clears the hit pattern word; clears only the last event being processed or already processed; clear time < 500 nsec.

F(10)·A(0-3): Clears LAM and data register.

F(16)·A(0-3): Writes offset register, 24 bits.

F(17)·A(0-3): Selects multi-source mode and writes router command word.

Data Format:

Bit 1 to 8: Number of router cycles = 0 for multi-source mode.

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Bit 9 to 23: Number of router increment steps (step size 256 channels).

Bit 24: Multi-source mode; if = 1, generates overflow condition if number of hits at multi-source input > 1. Normal Mode: if = 1, external router will not loop.

F(18)·A(0-3): Writes command word on the following format:

Bit 1 to 4: Time Resolution Range.

Bit 5 to 24: Time Overflow Setting.

F(24)·A(0-3): Disables module (in this state, the offset plus router value can be read with F(0) or F(2).

F(25)·A(0-3): Increments router counter by one. Must not be used in multi-source mode.

F(26)·A(0-3): Enables module.

Model 4208 Wide Range, Octal Time Digitizer

CAMAC COMMANDS

Z, C: Initialize module; clears all channels and clears the LAM.

I: Inhibits all channel inputs during CAMAC inhibit command.

Q: Conditional response for F(0), F(2), F(8), and F(10).

X: X = 1 response is generated for each valid function.

L: When enabled (jumper option), LAM is generated by the unit in response to either the "End of Time Window" input or the internal monostable pulse, which ever comes first.

CAMAC FUNCTION CODES

F(0)·A(0-7): Addressed readout; read data on Read Lines (2s complement convention); Q = 0 if an empty channel is read; Q = 1 otherwise.

F(2)·A(0-7): Addressed readout as for F(0); F(2)·A(7) clears the unit at S2; does not clear the LAM.

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F(8)·A(0): Test Look-At-Me; Q = 1 if LAM is present.

F(9)·A(0): Clears unit; resets LAM and all channels.

F(10)·A(0): Test and clear Look-At-Me; Q = 1 if LAM is present.

CAMAC TDC SELECTION CHART

Model	2228A	2229	3377	4208	4300B
Channels	8	8	32	8	16
Input Levels	NIM	Differential ECL	Differential ECL	-1.5 V to +1.5 V; 50 ohm input impedance	Differential
Dynamic Range	11 bits	11 bits	16 bits	23 bits + sign	11 bits
Least Count	50 psec; 100 psec; 250 psec*	30 psecÝ; 50 psec; 100 psec; 250 psec*	500 psec	±1 nsec	Typical 50 psec to 500 psec
Time Range	0-100 nsec; 0-200 nsec; 0-500 nsec*	0-61 nsecÝ; 0-100 nsec; 0-200 nsec; 0-500 nsec*	32 µsec	±8.3 msec	Typical 100 nsec to 1 µsec
Conversion Time	100 µsec; (Rear-panel adjustment for fewer bits/shorter time)	100 µsec; (Rear-panel adjustment for fewer bits/ shorter time)	1.6 µsec + 100 nsec per hit	none (real time technique)	8.5 µsec
Comments	*Internally adjustable to 1 µsec full scale, 500 psec resolution. Up to 10 µsec available as a factory MOD. May be configured	*Internally adjustable to 1 µsec full scale, 500 psec resolution Up to 10 µsec available as a factory	Multihit operation, 16 edge capacity per channel, leading and/or trailing edge. Double edge	May be set to multihit via jumpers. Multihit dead time 3 nsec between	Both the 4300B ADC and a time-to-charge converter (4303 or 3420) is required, thus two CAMAC

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	to be multihit via factory MOD. Dead time of 10 nsec between stops.	MOD. ÝAvailable as the 2229/400.	resolution is < 10 nsec. See separate data sheet.	stops.	slots. See separate data sheets.
Power +6 V -6 V +24 V -24 V	600 mA 550 mA 25 mA 140 mA 10.9 W	600 mA 600 mA 25 mA 140 mA	1.1 A 2.0 A 0.025 A 0.17 A	1.5 A 3.3 A 17 mA 17 mA	3.1 A 4.5 A 1.55 mA 250 mA
CAMAC Size	#1	#1	#1	#1	
The Model 3377 Time-to-Digital Converter and the Model 4300B with a Time-to-Charge Converter (e.g. Model 4303) were included for completeness. See separate data sheet for more details.					

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