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Find the *Teledyne / LeCroy 4222* at our website: ***Click HERE***

Model 4222

The LeCroy Model 4222, Quad, Wide Range, Gate and Delay Generator, produces long, precise time delays and time intervals synchronously with a random Trigger input. All 4 channels of the 4222 are started by a common Trigger input. Each channel provides a programmable time delay of up to 16.7 msec in 1 nsec increments. All programming is under CAMAC control.

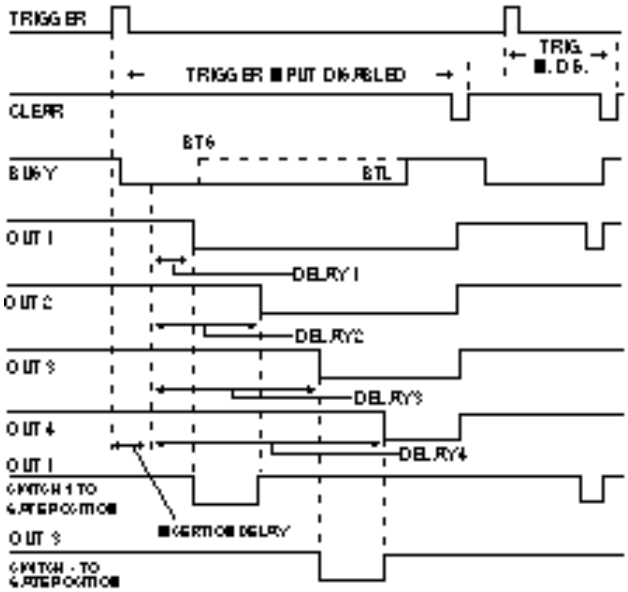
A set of side-panel switches permits the selection of coupled window outputs for channels 1 and 2, or 3 and 4. When coupled, Channel 1 (3) output (OUT) goes "true" when time delay 1 (3) has elapsed and goes "false" when time delay 2 (4) has elapsed; delay 1 (3) < delay 2 (4). Channel 2 (4) output (OUT) goes "true" when delay 2 (4) has elapsed and is reset by Clear or by the next Trigger if the Retrigger Mode has been selected.

NIM level BUSY outputs are also provided by the 4222. Busy goes "true" in response to a Trigger and remains "true" until the end of the shortest or longest delay is selected by an internal switch.

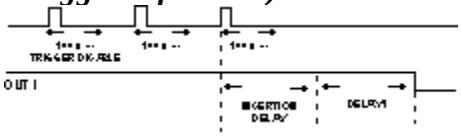
Three outputs are provided for each channel. One output provides NIM-level signals which go "True" after the programmed time delay and is reset by the Clear. Another output gives complementary NIM logic output. Each channel has a corresponding delayed pulse output that provides a 5 V fast rise time signal into 50 W occurring after the programmed time delay.

MODEL 4222 Trigger Timing Diagrams

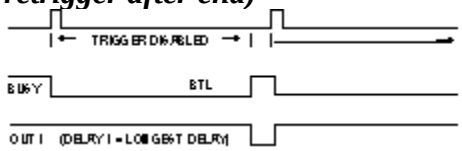
Non-Retrigger Mode (Retrigger Action Switch: set to retrigger disable) Diagram



Retrigger Before End of Delay (Retrigger Action Switches: set to retrigger enable retrigger before end)



Retrigger After End of Delay (Retrigger Action Switches: set to retrigger enable retrigger after end)



The Model 4222 may be set to retrigger mode permitting the unit to retrigger without being reloaded by a side -panel switch. In Retrigger Mode, two options are possible, before or after the delay period. The unit may be retriggered at any time (> 100 nsec after the last trigger) or any time after the longest delay has elapsed.

Synchronization of many 4222 Gate and Delay Generators is possible. An external clock may be used to feed several 4222 modules with an identical time base. Stability and accuracy are then determined by the external clock.

SPECIFICATIONS

Model 4222

INPUT

Trigger Input (TRIG): Two bridged front-panel Lemo-type connectors; high input impedance, positive/negative edge selection via side-cover switch; threshold level adjustable between -1.5 V and +1.5 V with a front-panel potentiometer; 10X threshold monitor on front panel; minimum input width is 5 nsec; unused input must be terminated in 50 ohm.

Clear Input (CLR): Two bridged front-panel Lemo-type connectors; high input impedance accepts NIM level pulses; minimum input width is 50 nsec; unused input must be terminated in 50 ohm.

Clock Input (CK): Two bridged front-panel Lemo-type connectors; high input impedance, selected by internal strap; NIM level inputs; unused input must be terminated in 50 ohm. Clock input frequency must be 31.25 MHz

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±0.1%. Stability determines the long-term accuracy of the time delays.

OUTPUT

BUSY and BUSY* Outputs (B & B*): Two front-panel Lemo-type connectors; NIM level outputs. BUSY output state goes true in response to a valid Trigger and remains true until either the end of the shortest delay or the end of the longest delay as selected by an internal switch.

Delayed Level Outputs (OUT & OUT*): Two front-panel Lemo-type connectors per channel; NIM level outputs; both direct (OUT) and complementary (OUT) outputs are provided. A set of side-panel switches permits the selection of either independent outputs or coupled window outputs:

&shyp; INDEPENDENT: 1, 2, 3, and 4: Each channel output (OUT) goes "true" when the corresponding programmed time delay has elapsed; output is reset by the Clear or by the next Trigger if the Retrigger Mode has been selected.

&shyp; COUPLED: 1 and 2, or 3 and 4: Channel 1 (3) output (OUT) goes "true" when time delay 1 (3) has elapsed and goes "false" when time delay 2 (4) has elapsed; delay 1 (3) < delay 2 (4). Channel 2 (4) output (OUT*) goes "true" when delay 2 (4) has elapsed and is reset by Clear or by the next Trigger if the Retrigger Mode has been selected.

Delayed Pulse Output (P1-P4): One front-panel Lemo-type connector per channel. Each channel's PULSE OUT delivers a 1 nsec rise time 5 V pulse (into 50 ohm) when the corresponding time delay has elapsed; pulse width 100 nsec ±10%.

GENERAL

Delay Range: 170 nsec to 16.777215 msec in 1 nsec increments.

Accuracy: ±200 psec ± time base error.

Jitter: 150 psec R.M.S. maximum; up to 1 msec delay (see manual for additional information).

Insertion Delay: 170 nsec.

Crosstalk: < 500 psec when delays differ by less than 8 nsec, 0 otherwise.

Internal Time Base: High stability quartz oscillator:
f/f0 : ±5 · 10^-6 initial frequency tolerance;
Tc : < 0.5 ppm/°C;
Aging : < 3 · 10^-9/day.

Packaging: Single-width standard CAMAC module.

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Power Requirements: 40 mA at +24 V; 1.3 A at +6 V; 2.5 A at -6 V; 130 mA at -24 V.

CAMAC COMMANDS

Model 2323A Dual Programmable Gate and Delay Generator

CAMAC COMMANDS

C or Z: Stops channels A and B gates.

X: X response is generated for each valid function.

Q: Q response is generated for each valid function unless otherwise specified.

CAMAC FUNCTION CODES

F(1)·A(0): Read channel A programming word.

F(1)·A(1): Read channel B programming word.

F(9)·A(0): Stop channel A gate.

F(9)·A(1): Stop channel B gate.

F(17)·A(0): Write channel A programming word.

F(17)·A(1): Write channel B programming word.

F(25)·A(0): Start channel A gate.

F(25)·A(1): Start channel B gate.

Model 4222 Quad, Wide Range Gate and Delay Generator

CAMAC COMMANDS

Z: Initializes module, resets all channels, disables trigger input and enables CAMAC access (does not reset data registers).

C: Resets all channels (does not reset data registers) equivalent to front-panel Clear input.

I: Disables trigger input when present.

X: X response is generated for each valid function.

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Q: Q response is generated for each valid function unless otherwise specified.

CAMAC FUNCTION CODES

F(0)·A(0-3): Reads selected program delay for channels 1-4 in 24 bits; Q = 1 always; 24-bit unsigned integer convention.

F(1)·A(0): Reads status via READ lines 1-4: R1 = 1 if shortest delay elapsed; R2 = 1 if longest delay elapsed; R3 = 1 if Model 4222 is ready for trigger; R4 = 1 if CAMAC access enabled. All states are strobed by the leading edge of the CAMAC N signal.

F(9)·A(0): Resets all channels (does not reset data registers) equivalent to external Clear input.

F(16)·A(0-3): If CAMAC access enabled, writes delay to selected channel 1-4 in 24 bits. Q = 1 if CAMAC access enabled; Q = 0 otherwise. 24-bit unsigned integer convention.

F(24)·A(0): Disables unit; enables CAMAC access.

F(25)·A(0): Triggers the unit (OR'd with the external front-panel Trigger input): Q = 1 if unit was ready for trigger; Q = 0 otherwise.

F(26)·A(0): Enables unit; disables CAMAC access.

GENERAL	**4222**
Packaging	Single-width CAMAC
START Input	-1.5 V to +1.5 V
STOP Input	NIM (Clear Input)
GATE WIDTH	
Range	170 nsec to 16.777215 msec
Jitter	150 psec R.M.S. max.
Accuracy	±200 psec ±time base error
Resolution	1 nsec
Input to Output Delay	170 nsec typical

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DELAYED OUT	
Width	Latched until reset by CLEAR or next trigger if retrigger mode is selected
Occurs	At end of delay
Rise Time	1 nsec
Signal	OUT: Standard negative NIM at end of delay. OUT*: Complement of OUT.
Miscellaneous	Delay setting programmable from 170 nsec to 16.777215 msec
ADDITIONAL INPUTS AND OUTPUTS	
Delayed Pulse	P1 - P4. Each Channel PULSE OUT delivers a 1 nsec rise time 5 V pulse (into 50 ½W) when the corresponding time delay has elapsed; pulse width 150 nsec ±10%.
BUSY	NIM BUSY output state goes true in response to a valid Trigger and remains true until the end of the shortest delay or the end of the longest delay as seen by an internal switch.
OR	Ñ
BLANK	Ñ
POWER	
24 V	+40 mA/-130 mA
12 V	Ñ
6 V	+1.3 A/-2.5 A
	26.9 W
**Taken from +12 V if +6 V unavailable.*	

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