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6103 Dual Amplifier/Trigger Generator

- Selectable Input Options
- Broad Bandwidth
- High Density Packaging
- Flexible Trigger Generation
- High Voltage Inputs
- Cascading Amplification

FOR AMPLIFICATION AND ATTENUATION OF INPUT SIG NALS

The LeCroy Model 6103 Dual Amplifier/Trigger Generator provides amplification and attenuation of analog signals for matching the user's signal to the input range of one of LeCroy's wide selection of modular waveform digitizers. It is efficiently designed as a multichannel package providing space and cost economy for multiple channel digitizing systems.

The 6103 is a general purpose amplifier. However, it has been optimized for use with LeCroy high-speed digitizing module TR8828D. Total programmability is incorporated into the Model 6103. It also incorporates a trigger genera tion section for triggering digitizer modules.

FUNCTIONAL DESCRIPTION

LeCroy signal conditioning modules are designed for general applications and for matching signals from the test device to the fixed input range of LeCroy modular digitizers. For system versatility the Model 6103 dual channel amplifier offers full programmability of its multiple gain and input options and it provides power-up protection (settings default to high impedance and high voltage input range). The LeCroy 6103 allows both bipolar and unipolar inputs to be matched (via programmable input offset) to the input of the digitizer or other instrument over plus and minus the input sensitivity. Excellent offset stability is maintained on the 6103 via self-calibration per formed each time offset, gain or filtering is programmed. Upon power up and after temperature stabilization, offset calibration should be performed to assure best operation.

A low pass filter is selectable under program control in the 6103. Thus, undesired frequencies (e.g., unwanted harmonics above the Nyquist limit) can be attenuated. The 6103 is shipped with a 20 MHz plug-in filter but the design is user-configurable.

The trigger generator section of the Model 6103 is designed to cover a wide range of input signal conditions and to give flexible control over the conditions of generating a trigger pulse. Selectable trigger source, coupling, level and slope are programmable on the 6103.

SPECIFICATIONS

INPUT CHARACTERISTICS

Channels: 2 single-ended channels; 1 Mohm/50 pF and 50 ohm selectable input impedance; AC or DC cou pling for 1 Mohm/ impedance.

Sensitivity: 50 mV p-p to 50 V p-p in 10 ranges for 1 Mohm/ inputs, 50 mV p-p to 5 V p-p in 6 ranges for 50 ohm/ inputs, to provide 0.5 V p-p at output (Table 1); gain accuracy ±5% of full scale; total harmonic distortion (to 50 MHz) is < -40 dB.

Offset: Programmable over ± full input range in 0.4% increments. Built-in auto-calibration provides error correction; should be performed after system warm-up and stabilization.

Frequency Response: DC to 150 MHz (-3 dB) for 50 ohm inputs; DC to 100 MHz (-3 dB) for 1 Mohm input; with bandwidth limit ON, 20 MHz (-3 dB).

Rise Time: 50 ohm input <2.5 nsec, 1 Mohm input < 3.5 nsec.

Overshoot: 10% for input pulse rise time 3 nsec.

Recovery Time: Recovers to 1% from x2 overdrive in 10 nsec.

Input Protection: Maximum safe input voltage at 1 Mohm is 250 V (DC + peak AC), at 50 ohm is 5 VDC (500 mW) or ±10 V peak AC or 50 V peak for 10 µsec transient.

OUTPUT CHARACTERISTICS

Nominal Full Scale Output: ±250 mV nominal (±300 mV linear range).

Output Impedance: Matched to 50 ohm loads.

Noise: 2 mV R.M.S. at output.

Channel-to-Channel Isolation: A to B, < 40dB at 100 MHz with both at same sensitivity setting (B to A is slightly higher).

TRIGGER GENERATOR

Source: Amplifier channel A, B, external, external/10; trigger bandwidth DC to 100 MHz; slope selectable, + or -; external trigger input impedance 1 Mohm; coupling selectable as DC, AC, LF reject, HF reject.

Level: External, -2 V to +2 V; external/10, +20 V to -20 V; Channel A or B, + to -2x full input range setting. Settable in all cases in 0.4% increments; DC level accuracy +10% of full scale.

Trigger Output: Two TTL 50 ohm outputs allow triggering two LeCroy waveform recorders; maximum propaga tion delay 35 nsec; output width 50 nsec.

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GENERAL

Connectors: All front-panel connectors are female BNC.

Control: All functions programmable and readable via Dataway.

Module ID: Upon query from controller, module returns "6103" as identification.

Environment: Proper operation of module requires +15 ° C to +25° C intake air with sufficient airflow to maintain temperature rise of exhaust air to < 15° C (+30° C intake air allowed if sufficient airflow to maintain temperature rise of exhaust air to < 10° C). Operating humidity range up to 90% relative humidity non-condensing at +25 ° C. Operating altitude <10,000 ft. above sea level (< 3,045 m). Non-operating temperature range is -10 ° C to +50° C.

Power Requirements: At +6 V, 1.8 A; at -6 V, 800 mA; at +24 V, 550 mA; at -24 V, 350 mA. (Use LeCroy Model 8007 or 8025 mainframes.)

Table 1: Gain/attenuation vs. max. input to generate digitizer full scale level (500 mV).

PACKAGING

RF-shielded modules in conformance with the CAMAC (IEEE-583) Standard.

Size (HxWxD): Size 1; 221 mm x 17 mm x 292 mm.

CAMAC COMMANDS

CAMAC COMMANDS

X, Q: Generated for all valid functions.

I: Inhibits trigger outputs.

Z, C: Are ignored.

CAMAC FUNCTION CODES

F(0)·A(0): Read; sets input coupling A; 2 bits.

F(0)·A(1): Read; sets input coupling B; 2 bits.

F(0)·A(2): Read; Sensitivity A; 4 bits.

F(0)·A(3): Read; Sensitivity B; 4 bits.

F(0)·A(4): Read; Offset A; 8 bits.

F(0)·A(5): Read; Offset B; 8 bits.

F(0)·A(6): Read; Bandwidth limit A; 1 bit.

F(0)·A(7): Read; Bandwidth limit B; 1 bit.

F(0)·A(8): Read; trigger source; 2 bits.

F(0)·A(9): Read; trigger level; 8 bits.

F(0)·A(10): Read; trigger slope; 1 bit.

F(0)·A(11): Read; trigger coupling; 2 bits.

F(0)·A(12): Read; enable trigger; 1 bit.

F(3)·A(0): Read; Model number 6103; 16 bits.

F(16)·A(0): Write; sets input coupling A; 2 bits.

F(16)·A(1): Write; sets input coupling B; 2 bits.

F(16)·A(2): Write; Sensitivity A; 4 bits.

F(16)·A(3): Write; Sensitivity B; 4 bits.

F(16)·A(4): Write; Offset A; 8 bits.

F(16)·A(5): Write; Offset B; 8 bits.

F(16)·A(6): Write; Bandwidth limit A; 1 bit.

F(16)·A(7): Write; Bandwidth limit B; 1 bit.

F(16)·A(8): Write; trigger source; 2 bits.

F(16)·A(9): Write; trigger level; 8 bits.

F(16)·A(10): Write; trigger slope; 1 bit.

F(16)·A(11): Write; trigger coupling; 2 bits.

F(16)·A(12): Write; enable trigger; 1bit.

F(25)·A(0): Write; offset recalibration; 0 bits.

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