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QUAD 10-BIT
TRANSIENT DIGITIZER
MODEL 8210



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LeCroy Corporation, 1816 Holmes Street, Bldg. E
Livermore, California 94550

European Customers can contact:

LeCroy Ltd.
Elms Court
Botley
Oxford OX2 9LP England

LeCroy, SA
101 Route Du Nant-D'Avril
1217 Meyrin 1-Geneve
Switzerland

LeCroy, S.a.r.l.
Avenue du Parana
Z.A. De Courtaboeuf
F-91940 Les Ulis, France

LeCroy, GmbH
Werderstrasse 48
Postfach 10 37 67
6900 Heidelberg
West Germany

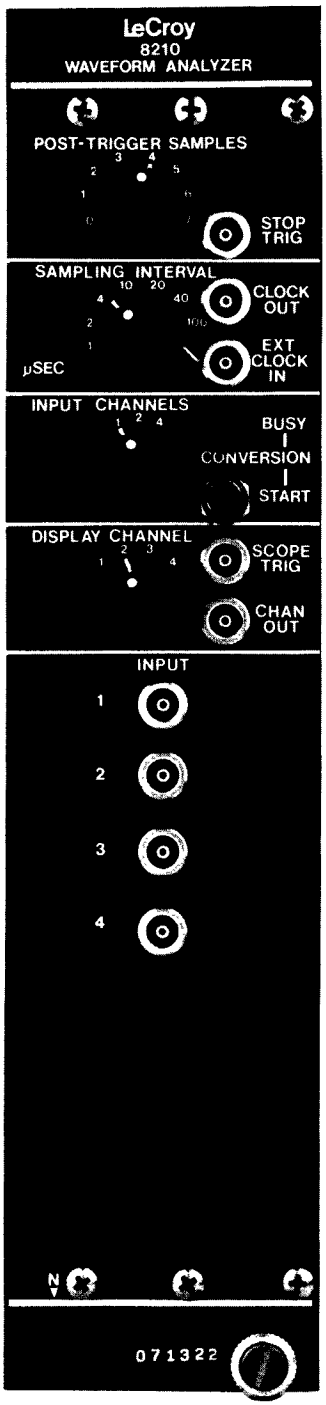
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LeCroy



Model 8210
Quad 10-Bit Transient Digitizer

- **4 Analog inputs**
- **10-bit resolution**
- **10mV/count sensitivity**
- **±100 psec aperture uncertainty**
- **Simultaneous sampling (<5 nsec uncertainty)**
- **5 MHz analog bandwidth**
- **Front-panel post-trigger sample select**
- **Large scale expandable memory of 32K words/module**
- **Protected inputs**
- **Built-in display driver**
- **System compatibility—part of a LeCroy digitizer family**
- **Varying clock rates possible**

The LeCroy Model 8210 Quad 10-Bit Transient Digitizer is part of an expanding line of LeCroy products for the study of transient phenomena. The 8210 offers the user a medium speed, high performance, modular waveform digitizer designed in accordance with CAMAC standards, providing high data transfer rates and system flexibility. Up to 4 analog inputs to the 8210 are sampled simultaneously by track-and-hold circuits having analog bandwidths greater than 5 MHz and channel-to-channel sampling uncertainty of <5 nsec. The analog signal is digitized by a 10-bit, successive approximation ADC. The data is stored in the Model 8800A memory module under the control of the 8210. Each 8800A module has a capacity of 32K, 10-bit words; up to 3 memory modules may be used in a serial fashion. The memory per channel is the total memory divided by the number of active channels. (Further expansion possible as factory option.)

The data is read out through the memory control circuitry in the Model 8210. Each of the four channels can be separately addressed. Readout is non-destructive, and a DAC display is provided for presentation on any scope.

The flexibility of the design concept also allows the external clock frequency to be varied with time, permitting "importance" sampling along a single waveform. LeCroy's CAMAC Model 8501 Programmable Three-speed Clock Generator provides a wide range of clocking capabilities including "importance" sampling under CAMAC control.

The flexibility of 8210 may be enhanced through the use of the Model 8100 Dual Programmable Differential Amplifier. This module affords excellent common mode rejection and offers a wide range of CAMAC-programmable gain.

The 8210 system digitizes continuously, which allows retention of waveform data recorded before the stop trigger. This pretrigger sampling capability allows recording the baseline value previous to the occurrence of the meaningful signal or allows triggering from a feature of the signal while retaining previous detail.

The Model 8210 is packaged in a #3 width CAMAC module. All integrated circuits are socketed, and boards are hinged for easy maintenance.

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SPECIFICATIONS
CAMAC Model 8210
QUAD 10-BIT TRANSIENT DIGITIZER

Input Characteristics:

Number of Inputs:	1, 2 or 4, switch selectable.
Analog Input Impedance:	1 MΩ (50 Ω optional).
Full-Scale Amplitude Range:	±5 volts—10 volt range.
Input Analog 3 dB Bandwidth:	5 MHz.
Overvoltage Protection:	±65VDC, ±100V for 1sec, ±200V for 10msec.
Stop Trigger Input:	LEMO connector, TTL level required to terminate conversion cycle after preset number of samples.
Input Connectors:	Coaxial LEMO.
Input Coupling:	Direct.

Digitizing Sections:

Internal Clock:	Front-panel switch selects rate: 1 MHz, 500 KHz, 250 KHz, 100 KHz, 50 KHz, 25 KHz, and 10 KHz, or EXT.
External Clock Input:	One coaxial LEMO-type connector (500Ω impedance, TTL level). Minimum duration of clock pulses, 100 nsec. Valid frequency range 0 to 1 MHz. Time varying frequencies allowed to achieve "importance" sampling along a single waveform.
Sensitivity:	9.8 mV/count.
Analog-to-Digital Conversion:	10 bits or 1 part in 1024.
Linearity:	±0.2% of full scale.
Aperture Uncertainty:	±100 psec maximum, defined as the uncertainty in the actual sample-taking time relative to the leading edge of the clock. This corresponds to a capability of frequency reconstruction of 1.5 MHz with 10-bit accuracy.
Channel-to-Channel Sampling Uncertainty:	≤5 nsec.
Memory Organization:	The memory is contained in separate modules which can be cascaded each capable of storing up to 32,768 10-bit words. (See further description of LeCroy Model 8800). Memory is divided equally among the active channels.
Display:	A built-in display driver allows the digitized waveform to be viewed on any real time oscilloscope. A channel select switch is located on the front panel.
Post Trigger Sampling:	The number of samples taken after the stop trigger is set by a front panel switch in multiples of 1K (2K optional).

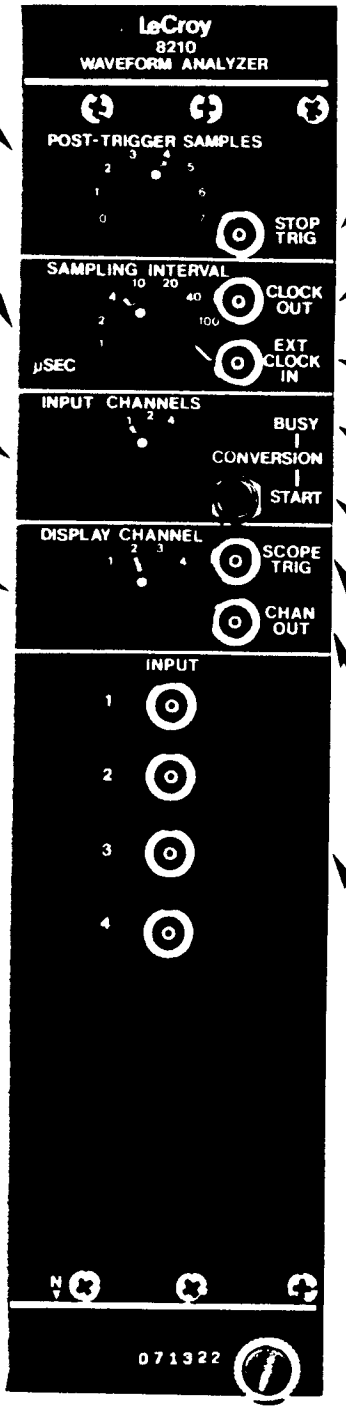
Readout Characteristics:

Readout Scheme:	The standard CAMAC organization is used permitting readout at the maximum rate allowed by CAMAC unless 4 channels are active (2μsec/word). Word count and Q-switching DMA transfers are possible. Readout is non-destructive. Data from individual channels is accessible and the first word corresponds to the earliest sample taken. Readout is serial, but readout can be terminated for a given channel at any point.
CAMAC Commands:	L: A Look-At-Me signal is generated at the end of the final sampling sequence. Q: A Q=1 response is generated in recognition of a F(2)•N only when a valid word is being read. After all data has been read for a given input channel, the next readout will generate a Q=0 response. The size of the memory, which depends upon the number of memory modules used, is programmed into the 8210 by a jumper option. Q=1 also returned on F(8) if internal LAM is on. Z: The continuous sampling cycle is reinitiated; requires S2. C: Same effect as Z. X: An X=1 (Command Accepted) response is generated when a valid F and N are generated.
CAMAC Function Codes:	F(1): Reads out front-panel switches (number of post-trigger samples, number of channels and internal clock frequency). F(2): Read data registers; requires N. Successive F(2)•N commands will read successive 10-bit words from memory. F(8): Test for LAM F(9): Initialize module. F(10): Clear LAM. F(16): Select channel to be read. F(16)•A(0) through A(3) selects channel 1–4 of the quad unit. F(24): Disable Look-At-Me (LAM); requires N • S2. F(25): Generates a "Stop Trigger." F(26): Enable LAM and stop DAC display. This command is necessary for any computer readout of the module. There may be as much as a 20 msec latency period (for 1 memory module) to allow the DAC to cycle through the rest of memory. (Caution: the state of the LAM mask, and hence the state of the display, may be arbitrary after turn-on.) No latency time if issued before stop trigger.
Packaging:	In conformation with the CAMAC standard for nuclear instrumentation modules. (IEEE Standard 583, or European Esone Report #EUR4100e.) RF shielded CAMAC #3 module. Approximate current requirements are within CAMAC standards for a #3 width.
Power Requirements:	2.2 A at +6 V 13 mA at −6 V 490 mA at +24 V 310 mA at −24 V

SPECIFICATIONS SUBJECT TO CHANGE

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Front-Panel Photograph and Description



Switch selects number of samples taken after the stop trigger

Switch selects number of microseconds between samples.

Switch selects number of input channels and determines highest possible frequency

Switch selects channel to be displayed

TTL level pulse initiates post-trigger run down scaler.

Drives 50 Ω load to TTL level at the internal clock sampling rate.

Leading edge of TTL pulse causes unit to take a sample in all channels

LED lights when unit is digitizing

Manual pushbutton initiates sampling

Separate scope trigger allows manipulating of scope gain, time base, etc., without losing trigger.

Display output proportional to input signal at a flicker free refresh rate.

Individual Inputs: 1 MΩ impedance.

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1. OPERATIONAL DESCRIPTION

1.1 General

The LeCroy Model 8210 Multichannel Waveform Digitizer is a 10-bit (.1% resolution) analog-to-digital converter which can process signals from four different sources simultaneously. The maximum sampling rate is 1 MHz for each channel. Data is stored in an external ^2K word memory module which divides memory si e equally among the input channels. The memory can be e^panded to ^,32K word modules.

The A/D conversion for each sample is effected by an independent sample-and-hold and ADC for each channel. Data is converted within 1 µsec independent of the master clock frequency. The digital data is then directed by internal circuitry to the 8210 output connector along with timing and control signals appropriate for interfacing with LeCroy Model 8800A cascadable memory modules. This allows the data to be stored in a memory of up to 96K 10-bit words, in 32K increments.

The Model 8210 also contains circuitry which sequentially reads the memory and sorts the data such that the digital data for any selected channel can be placed on the CAMAC dataway or reconverted to analog form by an internal DAC for viewing on an external scope.

1.2 Front-Panel Inputs Controls and Indicators

Analog INPUTS: Four Lemo input connectors. Input impedance 1 MΩ, bandwidth greater than 5 MHz. Full scale amplitude range is ±5.00 V, ±1% of full scale.

SAMPLING INTERVAL Switch: The sampling period per channel may be internally set to the rates indicated at the first seven positions of the switch; 1, 2, 4, 10, 20, 40 and ˙00 µsec. When the switch is in the External Clock position, the sampling period is determined by the frequency of the external clock

EXTERNAL CLOCK INPUT: Allows user to determine sampling rate per channel by input from a TTL level clock generator. Input impedance is 50 Ω. The maximum allowable external clock frequency is 1 MHz (also applies to internally selected clock rates). Conversion is initiated on the positive edge of the clock.

To allow for "importance sampling", the clock rate may vary over the allowable range (minimum time between rising edges is 1 µsec).

NUMBER OF INPUT CHANNELS SWITCH: Programs digital multiplexer to select data from channel one only in the 1 position, from channels one and two only in the 2 position and from channels one through four in the 4 position.

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CONVERSION START Button: Resets internal logic and starts continuous sample, convert, and store cycling This button must be pushed after changing the INPUT CHANNELS switch.

BUSY Indicator: LED adjacent to conversion start button lights during sample, convert and store operations, remains off during readout and display operations.

STOP-TRIGGER Input: Lemo connector, 510 Ω input impedance, requires positive going TTL pulse of at least 50 nsec duration. A stop-trigger will stop the data conversion and storage process after the selected number of post-trigger samples have been taken

POST-TRIGGER SAMPLES Switch: The position of this switch controls the number of samples converted and stored per input channel following the stop-trigger pulse. The switch has positions 0 through 7. Normally the unit is programmed (wire jumpers) such that the numbers correspond to thousands of post-trigger samples i e., position 7 means 7K post-trigger samples per channel. The programming of the switch is done on a wire jumper platform (See Appendix A for jumper options

DISPLAY CHANNEL Switch: Digital data of the selected channel is reconverted to an analog signal for display on a scope. The signal is available from the CHANNEL OUT connector.

***NOTE:** During operation the DISPLAY CHANNEL switch and POST-TRIGGER SAMPLES switch may be changed at any time. The other panel switches should be preset before a conversion is initiated however and not changed until a new conversion-readout cycle is to be initiated under new conditions The internal timing may be upset by changing these switches so that the logic must be reset by starting a new conversion cycle to restore the proper timing as determined by the settings of the switches.

1.3 Front-Panel Outputs

Internal CLOCK OUT: Drives 50 Ω load to TTL levels. Permits synchronization of multiple 8210s by timing all sampling with respect to a single clock

CHANNEL Display OUTPUT: Lemo connector. After a stop-trigger and the selected number of post-trigger samples per channel has been digitized the Model 8210 will enter the scope display output mode (unless the LAM is enabled - see CAMAC section). The data from any input channel may be displayed on an oscilloscope by setting the display channel switch to the desired channel number. The amplitude of the output signal into a high impedance scope input is between 0 V and +10 V (the scope display output should not be terminated). The data points are displayed at an approximate rate of 1 μsec per point in the one-channel mode, 2 μsec per point in the two-channel mode, and 4 μsec per point in the four-channel mode. The scope sweep rate is set by the user to display the desired number of points

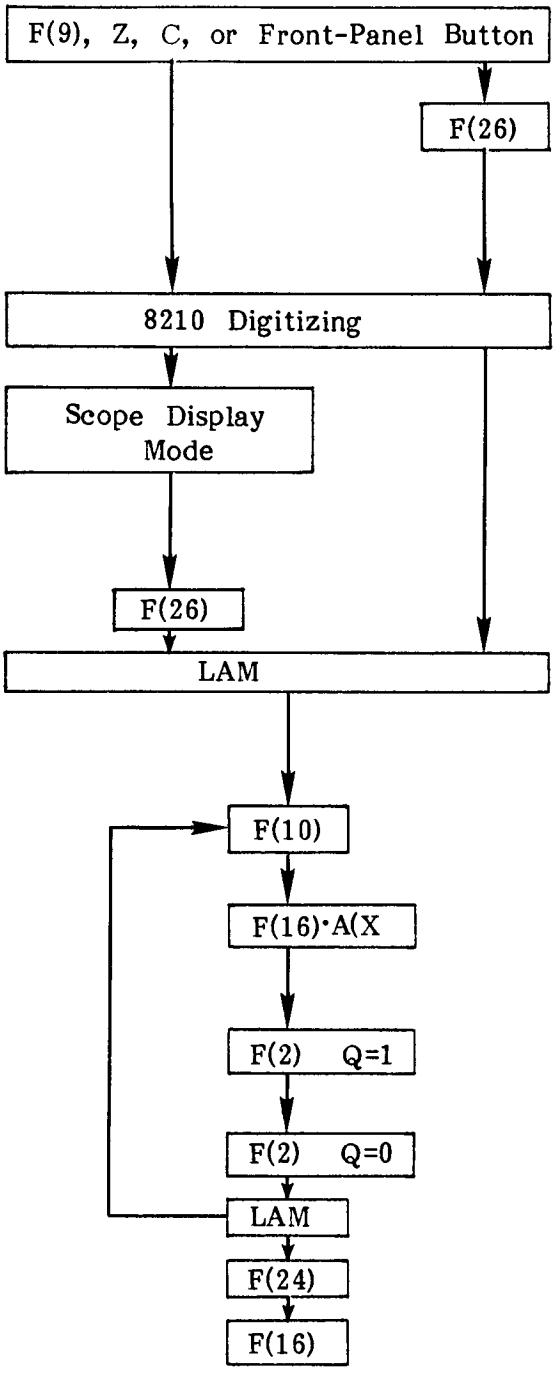
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SCOPE TRIGGER Out: Lemo Connector. A TTL positive going pulse occurring at the time the first data word is output for display. This pulse may drive the external trigger input of a scope so that the sweep will always start with the earliest data point. This output should not be terminated

Jumper Platform: The 8210 digital board contains a jumper platform (socket 3L) which in conjunction with the front-panel POST-TRIGGER SAMPLES switch programs the number of post-trigger samples. It also programs the number of 8800A memory modules (max. three) to be used.

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EXAMPLE OF 8210 CAMAC CONTROL SEQUENCE



Initiate Sampling

Enable LAM (only necessary if 8210 is to enter CAMAC readout mode after conversion completed).

Stop Trigger pulse OR F(25)

8210 enters scope display mode unless F(26) command was performed above.

8210 ready for CAMAC readout (Read LAM or test for LAM by Q=1 in response to F(8)).

Reset LAM

Select channel for readout (see Table I)

READ DATA for selected channel.

Readout complete

Disable LAM

Enable scope display.

Figure 1

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SELECTING CHANNELS FOR CAMAC READOUT

TABLE I

CAMAC Command	No. of Channels Selected On Front Panel	Result
F(16)·A(0)	1, 2 or 4	Select Channel number 1
F(16)·A(1)	2 or 4	Select Channel number 2
F(16)·A(2)	4	Select Channel number 3
F(16)·A(3)	4	Select Channel number 4

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TABLE II

A) F(1) reads the setting of the POST-TRIGGER SAMPLES switch, the sampling period switch, number of channels switch and odd/even samples flag.

(a POST-TRIGGER SAMPLES Switch Setting	2^2 R3	2^1 R2	2^0 R1	(Code) (CAMAC R Lines)
7	0	0	0	
6	0	0	1	
5	0	1	0	
4	0	1	1	
3	1	0	0	
2	1	0	1	
1	1	1	0	
0	1	1	1	

(b) SAMPLING INTERVAL Switch Setting	2^2 R6	2^1 R5	2^0 R4
Ext.	0	0	0
100 µsec	0	0	1
40 µsec	0	1	0
20 µsec	0	1	1
10 µsec	1	0	0
4 µsec		0	1
2 µsec		1	0
1 µsec	1	1	1

(c` No. of INPUT CHANNELS Switch Settings	2^1 R8	2^0 R7
4	1	1
2	0	1
1	0	0

(d ODD/EVEN Flag - If running in the single channel mode, the 8210 will truncate the last sample if it is to be stored in the first half of the ^800A memory. This condition is flagged on R9 during F(1).

R9=0: No Sample Truncated - Earliest sample = 32K·(No. of 8800A's - Post-trigger samples from trigger.

R9=1: One Sample Truncated - Earliest sample = (32K·(No. of 8800A's)- Post-trigger samples from trigger +1.

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2. FUNCTIONAL DESCRIPTION

2.1 General

The Model 8210 is a multichannel waveform digiti er composed of analog to digital converter (ADC oards and a controller board which contains digital circuits needed to control the storage of data in the Model 8800A memory modules. This board also contains the circuitry needed to read the data from the memory and either places the data on the CAMAC Dataway under CAMAC control or reconstructs the analog signal in any channel for display on a lab scope. Other circuitry on the board permits reading the settings of the front panel switches as a digital code on the CAMAC Dataway

In the following functional description of the instrument the operation of the boards will be discussed separately, and each board will be divided in several logical subsections.

2.2 ADC Boards

The ADC boards for the 8210 are composed of a track-and-hold circuit followed by a 0-bit, successive approximation ADC The ADC converts one sample in one msec. The track-and-hold timing is folded into the ADC timing to achieve a 1 megasample/sec throughput rate without degrading the high frequency performance of the system.

The digital data from the ADC is held in tristate output latches after the conversion is completed During the next sample the controller board sequentially scans these latches and stores the data in memory.

2.3 Controller Board

General description - refer to first paragraph in the functional description section

Master CLK: The Master CLK pulses come from a digital multiplexer (74LS151) which multiplexes several gates of different frequencies from the outputs of a divider (74LS390) clocked by a MHz crystal oscillator. An input from an external connector also may be selected by the multiplexer for external control of the sampling rate. The 74LS151 is programmed by the sampling rate switch on the front panel.

Memory Strobe and Refresh Generator: After data has been entered into the FIFO's (9403s) it bubbles through toward the FIFO output register. Status signals from the FIFO output and clock signals from a 5 MHz oscillator (74LS324) then control the shifting of the data out of the FIFO's onto the memory datalines in sync with memory strobe pulses This control is accomplished by the memory strobe and refresh pulse generator logic. This logic generates refresh pulses about every 10 μsec and ensures that memory strobe pulses and refresh pulses do not overlap and are properly timed with respect to

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one another. (See Model 8800A for detailed timing diagrams).

Data Display/CAMAC Readout Control: This section controls the readout of the data from the FIFO's and selects the data words to be latched into the DAC input register and the tristate buffer registers which output to the CAMAC dataway. As soon as the first word flag and first data word appear at output registers of the FIFO's the internal logic is set up to begin readout. Readout may proceed in a continuous cyclic mode or in a interrupted single memory scan under control of CAMAC F(2) read commands depending on the state of the CAMAC ENABLE line. If this line is low the readout will be under control of the FIFO's and Readout control logic alone and will proceed automatically at a rate depending on FIFO timing and the timing of monostables inside the readout control section itself. A scope trigger pulse is intiated when the first word flag is up so that the display sweep may be triggered at the earliest sample in the data.

Selection of the channel to be displayed is done by: (1) the display channel switch and ´2) the programmable sequencer made up of a 74LS195(4J), a 74LS151 (5J), a 74426 (5K), a 74LS173 (5I), a 74LS74 (6H) and other logic gates. This circuitry decides at the beginning of a read cycle how many data words are skipped before a latch pulse is sent to the output registers. It does this on the basis of input data from the 2^1 and $^{\sim}0$ terminals or the "Display Channel" switch on CAMAC A1, A2 information latched into the 74LS173 by an ´F16)·S2 command when CAMAC controlled readout is to be done. After this initial positioning of the first latch pulse at the first word of the channel to be displayed, the circuitry decides how many words are to be skipped before another latch pulse is produced. It does this on the basis of input from the INPUT CHANNELS switch. For example, in the single channel mode no words are skipped, in the two-channel mode one word is skipped and in the four-channel mode three words are skipped between latch pulses

When the CAMAC ENABLE line is set high by an F(26) command, a LAM will be raised when the first word flag and first word appears at the FIFO output registers. Now an F(16)·S1 pulse latches A1, A2 information in the 74LS173 to determine which channel is to be read (see previous paragraph F(16)·S2 starts the normal readout process discussed before and the first dataword is latched into the output latches and readout proceeds until the next word from the selected channel appears. No latch pulse is produced and readout stops until the first word has been placed on the CAMAC data lines by an F(2) command which enables the register output. The next word is then latched into the register on the trailing edge of the F(2)·S2 pulse and readout proceeds until the next word appears at the register inputs but again halts until another F(2)●S2 releases the previous word to the dataway and then latches this next word into the register and restarts the readout. Readout proceeds in this fashion until the first word flag and the accompanying data word appear again, at which time readout stops until another F(16) is received. If an F(24) command is issued the CAMAC ENABLE line goes low, the LAM is disabled and the F(16) command will reset the logic into

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the data display mode.

CAMAC Control Logic: This section uses 74LS154 (5A) and some other logic gates to decode the CAMAC function lines and generate the CAMAC control and response signals. For a complete description of these commands and responses see the CAMAC command and function code section of the data sheet and the CAMAC command sequence.

Memory Enable Control: This circuitry consists of chips 5M (74LS279) and 2C (74S08). The intiate pulse sets the Memory Enable line low, enabling the first memory strobe pulse 'enabling is done by high to low transition). When the last memory is full a memory enable return pulse is sent back to the controller and causes the memory enable line to go low reenabling the first memory again. For more details see the Model 8800A manual.

Auxiliary and Monitoring Circuitry: Allows digital codes associated with each front-panel switch (except DISPLAY CHANNEL switch) to be gated onto the CA AC dataway by appropriate CAMAC commands through tristate buffers (74LS240A) located at 3K.

A 7485 (4K) monitors the DISPLAY CHANNEL and INPUT CHANNELS switches and disables the display DAC if the DISPLAY CHANNEL switch is set to a channel which does not have its input switched into the multiplexer (determined by the setting of the INPUT CHANNELS switch).

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2.4 CONTROL SEQUENCING

(Refer to diagram in Figure 1.)

Initiate Sampling: The 8210 will start sampling after depressing the front-panel pushbutton or by computer command of a Z, C or F(9). The unit will remain in the sampling mode, continually cycling through memory until detecting a stop-trigger.

Stop Sampling: After detecting a stop-trigger (either using the external TTL pulse or CAMAC F(25) the 8210 will execute the required number of post-trigger samples (as determined by the front-panel switch) and then enter the readout mode. The user should not apply a stop-trigger until the 8210 has cycled completely through memory after "initiate sampling"; otherwise the memory will contain old and new data. The time required to cycle through memory once is given by:

$$T_{cycle} = 32768 \cdot NOM \cdot T_S/NOC$$

T_{cycle} = cycle time through memory in seconds

NOM = number of 8800A memory modules

NOC = number of active channels (1, 2, 4)

T_S = sampling interval (front-panel switch or external) in seconds.

Readout:

1) After entering the readout mode the 8210 will either display data on the scope or await CAMAC readout commands. If the user issued a F(26) command before the stop-trigger. the unit will automatically enter the CAMAC readout mode. If F(26) was not issued. the unit will display data on the scope display until F(26) is issued.

2) When the 8210 is ready to begin CAMAC readout it will turn the LAM on. The user can detect this by enabling interrupts or issuing F(8) commands and testing for Q=1. Upon detecting the LAM (or Q=1 on F(8)) the user should execute a F(10) command to clear the LAM. If the LAM is not cleared the unit will not read data from another channel later in the control sequence (step 6).

3) The user now selects which channel he wants to read by executing the appropriate F(16)·A(X) command (see Table I).

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4) Data is read by issuing successive F(2)s commands. The data is read as offset binary (see Table I). Data can be read in one of two modes:

   a) Block Transfer - The number of F(2)s issued equals the number of words to be read.*

   b) Q Transfer - User executes F(2) until Q=0 is detected. Issuing F(2) after all data is read* does not affect the 8210.

5) The maximum readout speed is:

   a) 1 MHz in the one-channel mode

   b) 500 KHz in the two-channel mode

   c) 250 KHz in the four-channel mode

   Exceeding the maximum readout speed will result in a Q=0 response on F(2).

6) Once all data has been read from the selected channel, the LAM is set again. To read another channel, execute the same steps from 2) on. To reenable the scope display the user must issue a F(24) followed by F(16)·A(0).

7) If all the data from the selected channel is not read out with F2 commands the short read cycle sequence must be done or else the 8210 will be left in an undefined state and data readout from another channel will not be possible. See the short read cycle procedure in Figure 2.

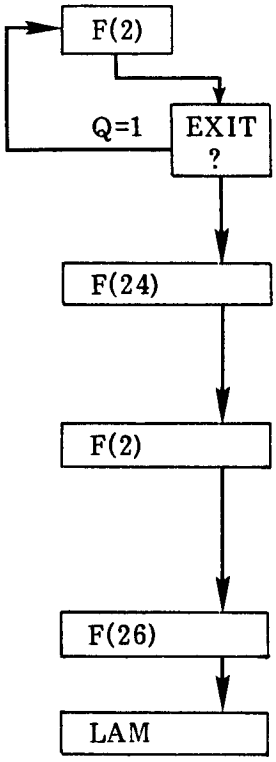
*NOTE: The amount of memory allocated to each channel depends on the number of channels selected and the number of ^800A memory modules:

Memory/Channel = 32768·NOM/NOC
NOM = number of 8800A memory modules
NOC = number of channels (1, 2, 4) active

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SHORT CYCLE READ SEQUENCE FOR 8210

If user does not want to read all data from a selected channel he can "short cycle" the unit at any time by executing a F(24) followed by a F(2).



User performs F(2)

User decides to read another channel before reading all data from the selected channel

One more F(2) needed to put unit back in scope display mode

8210 now displaying on scope

User decides to read next channel

Sequence is now the same as in the manuals for selecting and reading channels

Figure 2

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3. OPERATIONS SECTION

3.1 Introduction

This manual is not written as a basic trouble-shooting guide but rather as a detailed operational description of the 8210 circuits. It is assumed that the reader is familiar with the basic operation of the 8210 and understands digital/analog circuitry.

3.2 ADC Board

The 8210 contains two identical ADC boards, each of which contains two track-and-hold circuits, two analog-to-digital converters, and logic to provide control and output buffering. Circuitry on the board can be separated into two major blocks; 1) the track-and-hold circuits and 2) the A/D converter and controls section.

3.3 Track-and-Hold Circuits

As shown in the block diagram in Figure 3.1, the track-and-hold circuit is a conventional open-loop circuit made up of an input buffer amplifier. switch storage capacitor and output buffer amplifier, plus feedthrough and pedestal cancellation circuits

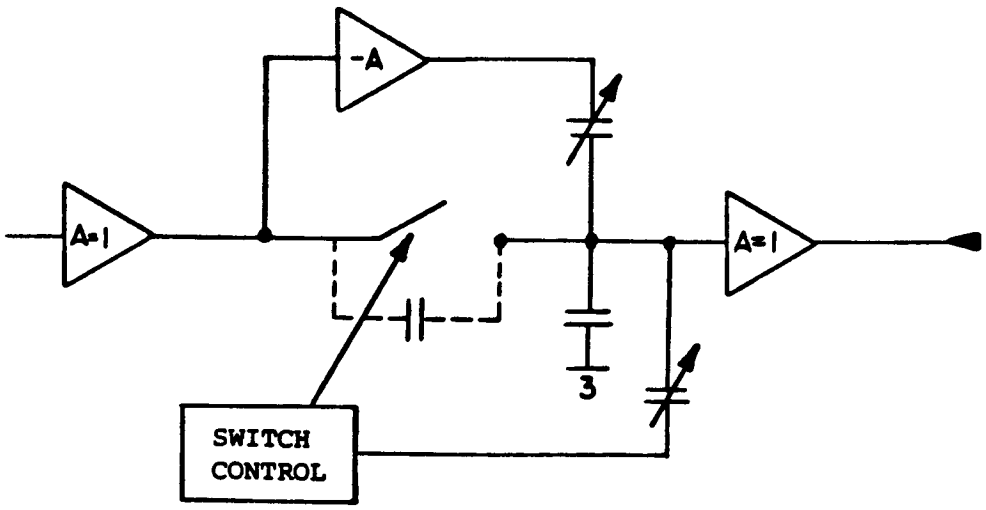


Figure 3.1

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Transistors Q2, Q3, and Q5 form a class AB power driver to provide slewing currents to the sample capacitor. Q3 generates a voltage drop that turns Q2 and Q5 on. R4 adjusts the bias current through Q2 and Q5 by setting the voltage drop across Q3. R77 sets the input impedance of the buffer and R1, C13, CR3, and CR4 are an input overvoltage protection network.

The track-and-hold itself (see Fig 3.3) is made up of Q7, an N-channel MOS FET, which functions as the analog switch, and C17, the signal storage capacitor. Gate drive for the FET is provided by differential pair Q12 and Q13, which also provide level translation for the TTL HOLD command signal appearing at the junction of R30, R26, ad C18. Q11 provides emitter bias current for Q12 and Q13; Op Amp 7A (output pin 7) assures temperature stability for that current. 7A (output pin 1) sets the switching threshold voltage for Q12 and Q13. R27, together with the emitter bias current provided by Q11, sets the gate drive amplitude. Pedestal cancellation is achieved by feeding the inverted gate drive signal to C17 through C16, thus cancelling the effects of gate-drain capacitance in Q7.

Transistors Q9 and Q10 provide an OFF reference voltage to Q7. This reference follows the analog signal to allow full gate signal amplitude without overdrive. This is necessary because of the relatively large input analog signal swing (+5V). Q9 and Q10 form an emitter-coupled gate. ensuring that the $\overline{\text{OFF}}$ voltage for the gate drive will be either the output voltage (via Q10) or the input voltage (via Q9 and Q6), whichever is more negative. CR8 and CR9 prevent emitter-base breakdown in Q9 and Q10; R21 provides a minimum bias current to the pair.

Source-to-drain feedthrough is cancelled by inverting the input signal via Q6 and summing it into C17 through variable capacitor C14. The signal at the junction of CR8 and CR9 is also inverted via Q8 and summed to C17 through C15 to reduce feedthrough from Q7's gate. CR6 and CR10-12 are used for DC level shifting.

The output buffer stage (Fig. 3.4) is identical to the input buffer, except that it does not contain the input protection and impedance-setting circuitry. It provides a very high impedance discharge path to the hold capacitor, and has a low output impedance to drive the A/D converter.

A good way to do DC adjustments on the circuit or to troubleshoot failure is to remove 3C, which disconnects both track and hold circuits from the logic portion of the board and switches both T and H circuits to "Track" mode. In this situation, the voltages marked on Figures 3.2-3.4 should apply (assuming no input signal).

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TRACK-AND-HOLD INPUT BUFFER

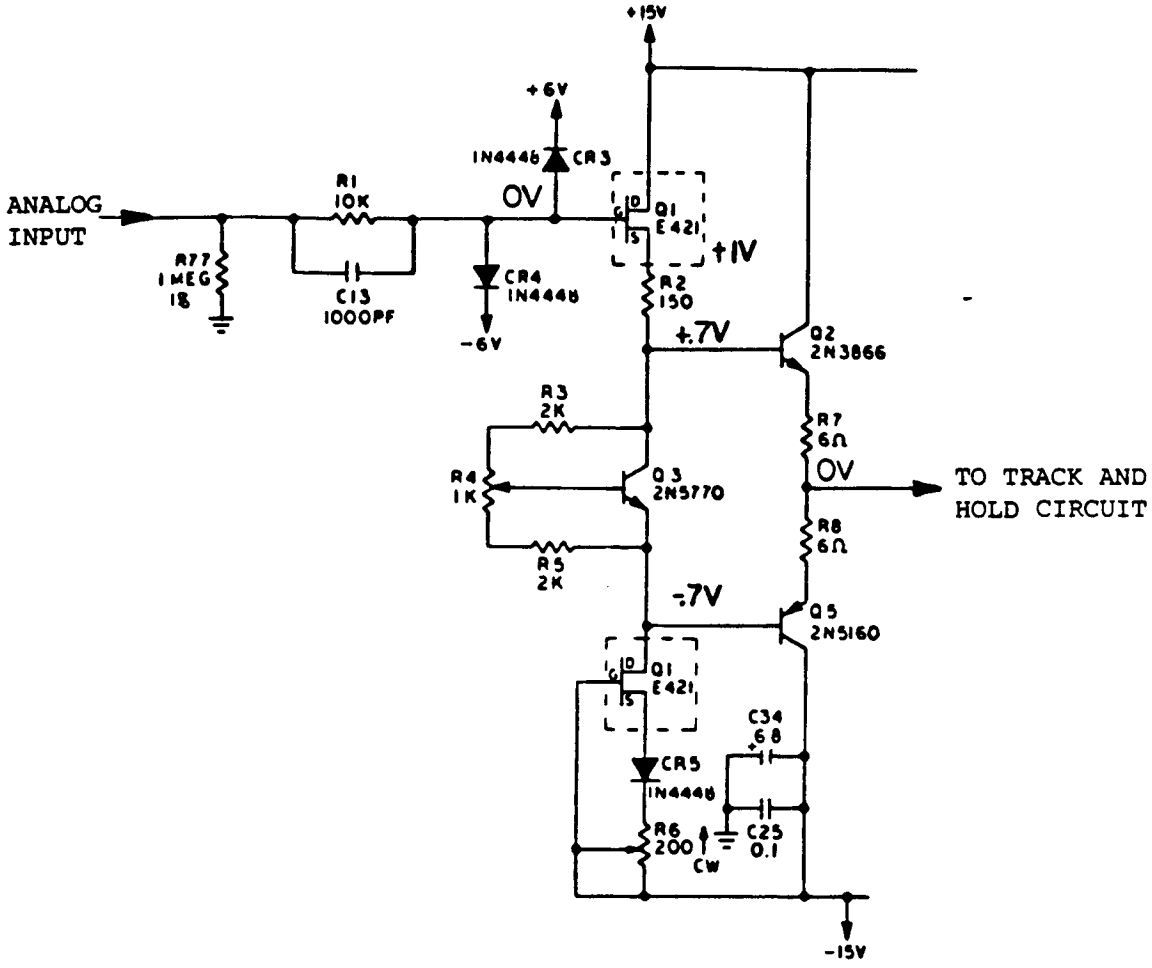


Figure 3.2

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Both channels on the board have identical circuits, so only one will be described.

The input buffer is shown in Fig. 3.2. Q1 is a matched pair of N-channel junction FET's connected to form a "zero offset" source follower, with the lower FET, CR5 and R6 acting as a current source and the upper FET providing the signal path. The voltage drop across R2 compensates for the voltage drop across R6. CR5 provides an additional drop to compensate for the emitter-base voltage of Q2, giving the buffer amplifier a very low DC offset: R6 permits adjustment of that offset.

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TRACK-AND-HOLD

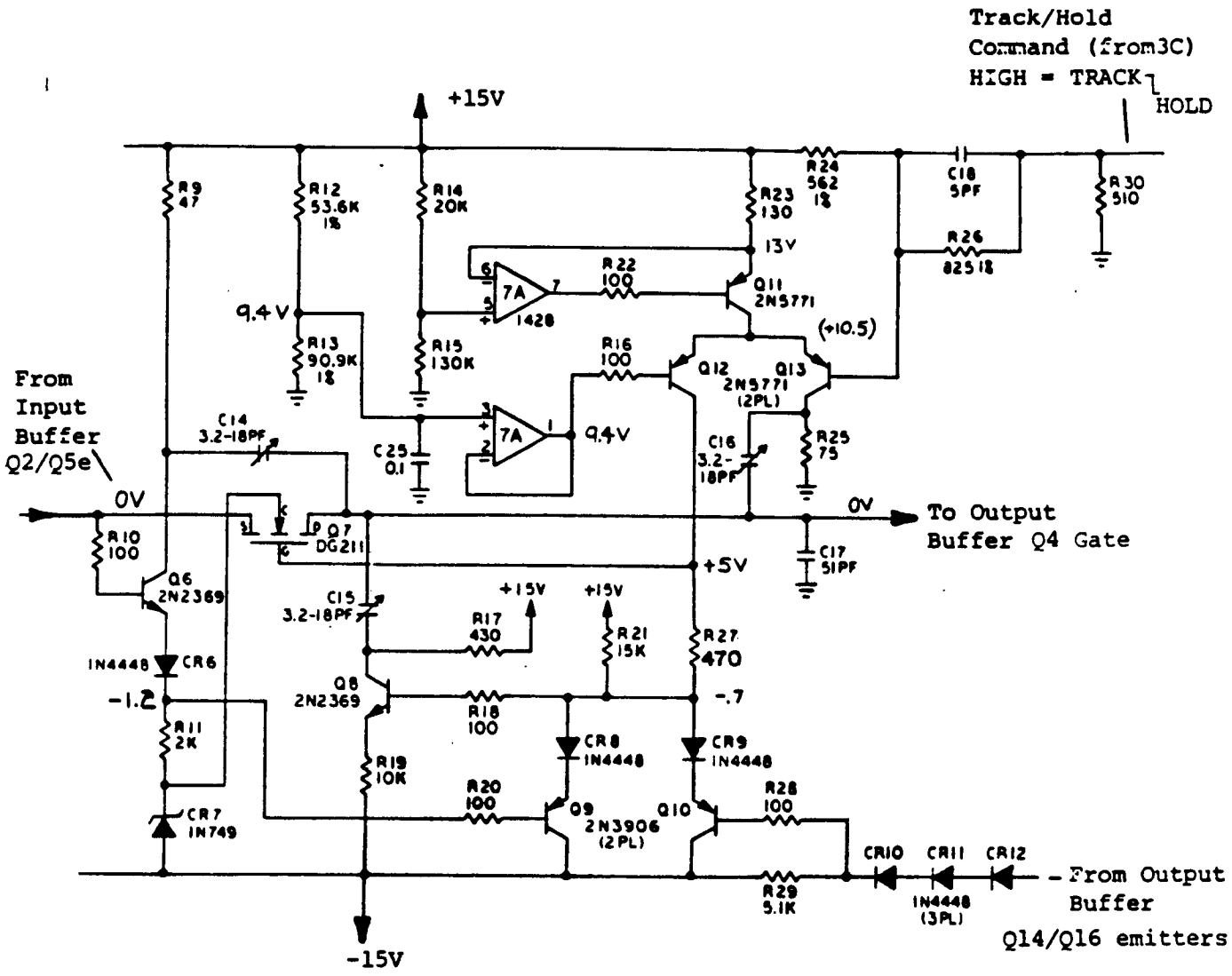


Figure 3.3

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Like most analog circuits, this one has many failure modes, and it's beyond the scope of this manual to detail them all. It may be worth mentioning one symptom as a starting point, however. If with 3C removed, the output of this circuit becomes fixed at a positive DC voltage and will return to zero if an oscilloscope probe is touch to C17, then Q7 is not being turned on.

TRACK-AND-HOLD OUTPUT BUFFER

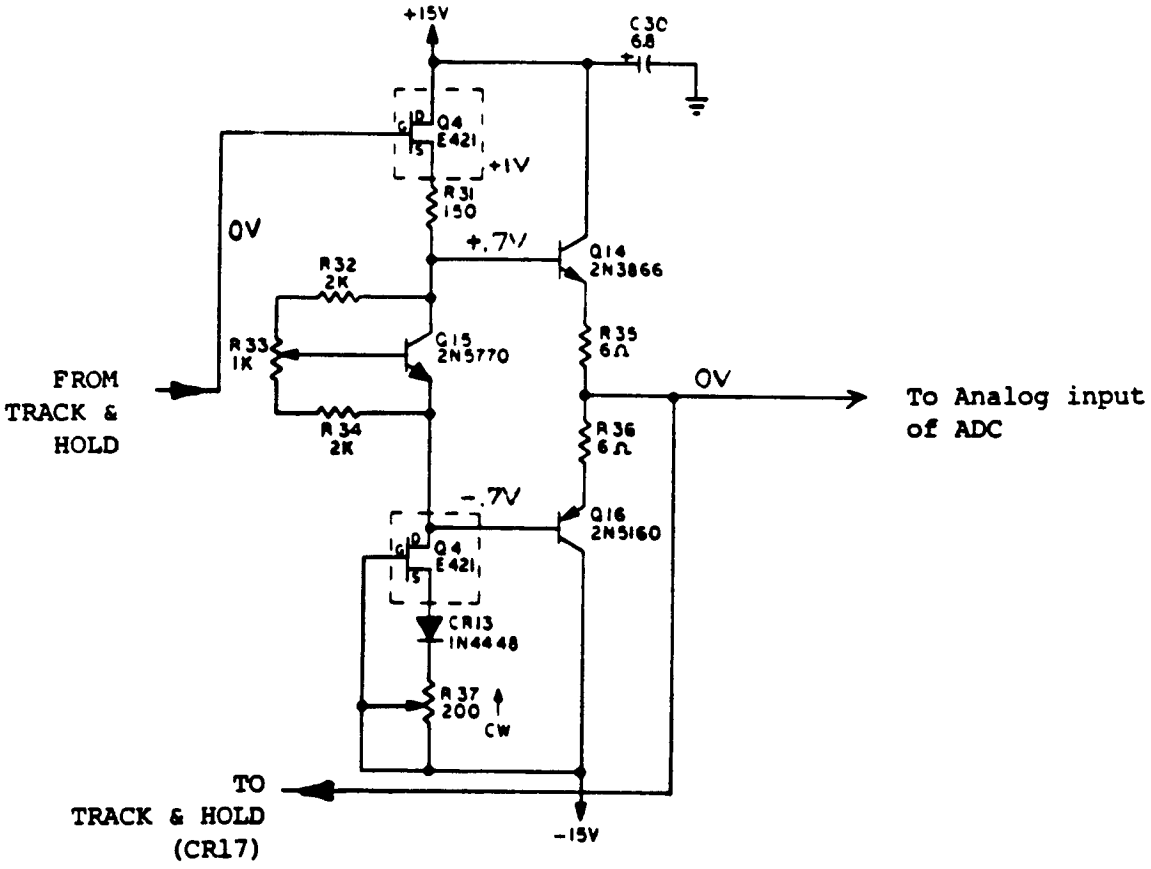
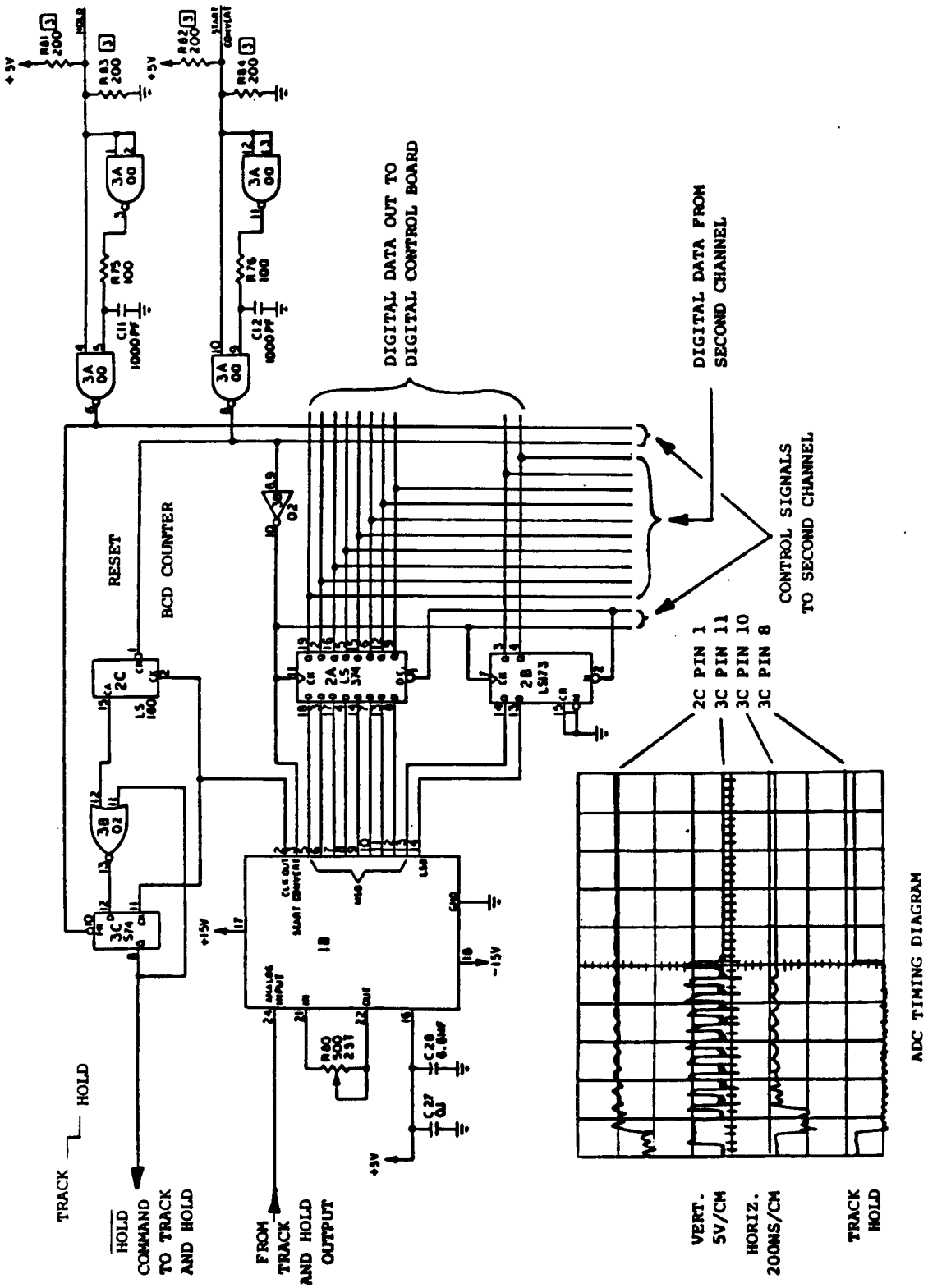


Figure 3.4

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ADC and CONTROL CIRCUITS

Figure 3.5

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If the gate drive voltage is at 5.5 V, the FET is probable faulty; if not, the gate drive circuitry should be investigated

One note of caution: if parts are replaced in either the input or the output buffer circuits, the output stage bias current adjustment pot for the relevant buffer (R4 in the input buffer stage, for example) should be set full clockwise to prevent overheating the output transistors. Follow the procedure in the alignment section

3.4 A/D Converter and Digital Controls

The A/D converter used on the 8210 is a modular successive approximation type; i.e. during the conversion cycle, it makes 10 "tests", one for each bit starting with the most significant bit to arrive at the output word. An output clock from the converter shows when each bit is being clocked into the converter output register.

The 8210 makes use of this clock to switch the track-and-hold circuit to Track Mode as soon as the converter has clocked out its last bit (Refer to Figure 3.5). BCD counter 2C is reset at the beginning of a conversion, and counts each of the converter's decisions, using the converter's cycle clock (2C pin 2). 2C reaches overflow one count before the conversion is complete (2C-15 high) and 3C pin 8 goes high on the next clock pulse (See timing diagram, Figure 3.5). 3B-13 assures that 3C-8 does not change state early in the cycle, since the Hold command does not come until slightly after the convert command is given 3C-8 is switched to the HOLD position (3C-8 high) by a command pulse at 3C pin 10. 2A and 2B are registers which hold the A/D converter's output word until the memory can accept it. They are clocked by the convert command pulse and their outputs are enabled (2B-2 and 2A-1) by commands from the control board.

The HOLD and CONVERT command signals are common to both channels on the board and are derived from signals that come from the digital control board. The digital board's signals are formed into 100 nsec wide pulses by gate 3A and delay networks C11-R75 and C12-R76.

The other channel on the board is identical to the one described.

Both the Track-and-Hold circuit and the A/D converter use $\pm$15 V supplies, which are derived on the board from the $\pm$24 V CAMAC lines by two 1C regulators, 5A (-15 V) and 6A (+15 V).

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4. ALIGNMENT PROCEDURES

Equipment Required

1. Oscilloscope with 15 MHz bandwidth.
2. Digital voltmeter with isolated inputs.
3. DC voltage source capable of ±5 V output range.
4. Means of reading out data (CAMAC tester computer system, etc.).

Introduction

Since the two channels on the analog board are identical, the reference designations for the upper channel will be shown first, with the lower channel reference designation following in parenthesis. All four channels must be adjusted separately

1) Track-and-Hold; DC Adjustment

Preliminary: It is not necessary for the board to be connected to the unit for DC adjustments; all that is required is an source of power to the rear CAMAC connector. If the board remains in the unit, it should be swung out on its hinges to allow easy access to the adjustment potentiometers. Before turning the power on, remove the 74S74 in position °C from its socket, and turn adjustment pots R4, R33, and R41 and R70 fully clockwise. Removing the I.C. forces both track-and-hold circuits into Track Mode. Turn on the power. Allow five minutes for the unit to warm up

A) Output Drive Bias Adjust:

Connect an isolated DVM between the emitters of Q2 (Q19) and Q5 (Q20). Slowly adjust R4 (R41) until the voltage reads 60 mV. Wait a few minutes, then recheck and readjust, as the reading will increase as the transistors warm up.

Repeat the above procedures after connecting the meter between the emitter of Q14 (Q30) and Q16 (Q32), using R33 (R70) for adjustments.

B) DC Offset Adjust:

1) Short circuit the analog inputs to the circuit to ground. Connect the DVM leads between the junction of R7 (R44) and R8 (R45) and ground. Adjust R6 (R43) until the DVM reads 0 V±5 mV.

2) Reconnect the meter leads between the junction of R35 (R73) and R36 (R74) and ground, and adjust R37 (R72) until the DVM reads 0 V±5 mV.

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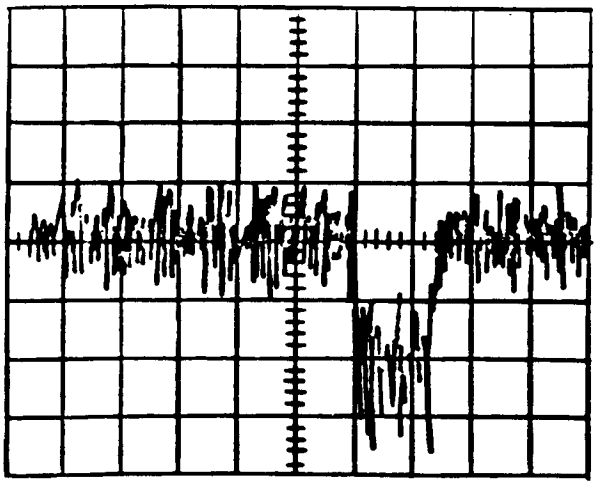
NOTE: If B(2) adjustment cannot be made, and the offset is positive and large (1 V) check to see if the gate of Q7 (Q22) is at about +5 V. If not, and the I.C. at 3C is removed, then the drive circuitry is faulty and should be repaired before proceeding. If so, Q7 (Q22) may be faulty. This can be checked by clipping a short circuit between source and drain; if the offset disappears, then the FET is faulty.

This completes the DC alignment of the track and hold.

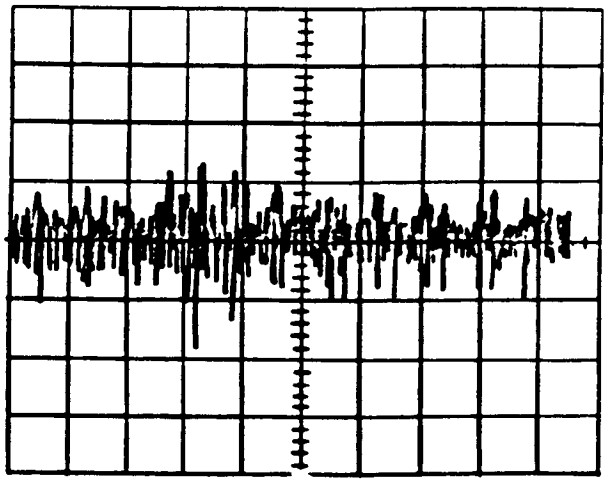
C) Pedestal Adjustment:

Turn off the power, replace 3C and reconnect the board to the instrument, using extender cables so that the board can be swung out for access to the adjustments. Set the unit internal clock for a 1 μsec interval and turn on the power. Using the external synchronizing input on the oscilloscope, synchronize the oscilloscope to the 8210 clock output. Connect a scope probe to the junction of R35 (R74) and adjust C16 (C22) for minimum pedestal. See photographs below.

BEFORE ADJUSTMENT



AFTER ADJUSTMENT



VERT: 50mV/CM
HORIZ: 100nS/CM
(Same for both diagrams)

Figure 4.1

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D) DC Calibration:

Preliminary: For this and the next part of the procedure, the unit must be connected to the memory and to a computer system that can read out the memory and translate the digital data into a voltage readout (The computer readout is not necessary for the next section).

1) Connect a DC source to the analog input and adjust it to output +4.900 V. Taking successive readings on the computer (sample rate 1 μsec) adjust R33 (R70) until the computer readout is +4.900 ± 10 mV.

2) Adjust the DC source to output -4.900 V. Taking successive readings with the computer (sample rate still 1 μsec) adjust R80 (R79) until the computer readout is -4.900 V ± 10 mV.

3) Repeat #1 and #2 until no change in readout occurs.

This completes the DC calibration of the unit.

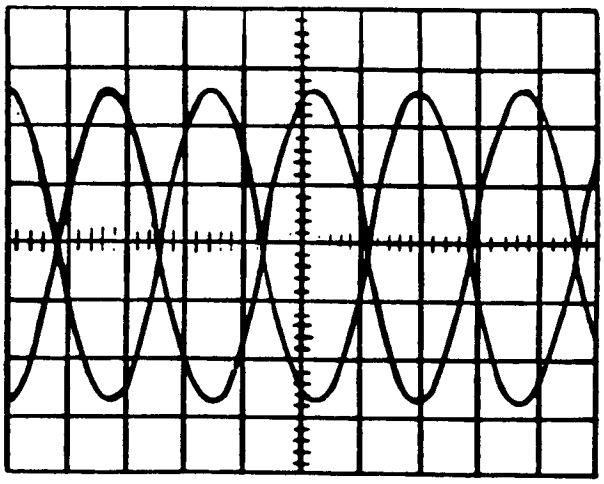
E) High-Speed Adjustments:

Connect the CHANNEL OUT connector on the 8210 to the oscilloscope inputs. Connect SCOPE TRIG output to the oscilloscope's "External Trigger" input. Set the scope input sensitivity to 2V/cm and trigger externally. Connect a sine wave generator to the appropriate input channel, and adjust it to output a 10 V p-p sine wave at 500 KHz. Set the 8210 time base to 1 μsec the INPUT CHANNELS switch to 4 and the DISPLAY CHANNEL switch to the channel to be adjusted. To take a recording, press the START button and after a pause, input a TTL signal to the STOP TRIG input (connecting the clock out to the stop trig works well here). Adjust scope time base to display entire channel memory (assuming only 1 memory module is connected to the unit). Carefully adjust the generator frequency, taking recordings after each adjustment, until the oscilloscope wave form looks like the photograph in Fig 4.2.

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Figure 4.2

SCOPE VERT.
-2V/CM
HORIZ.

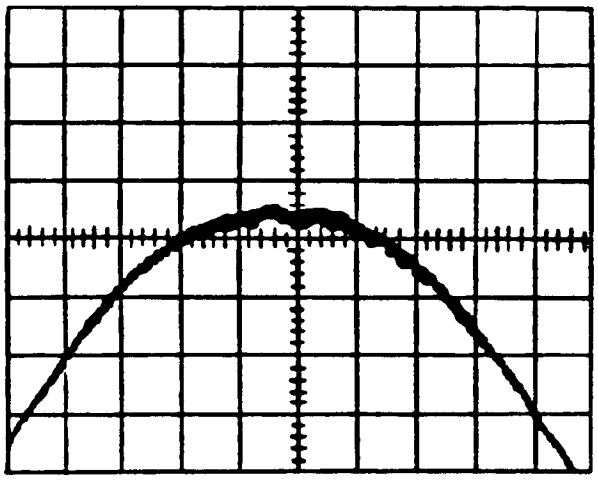


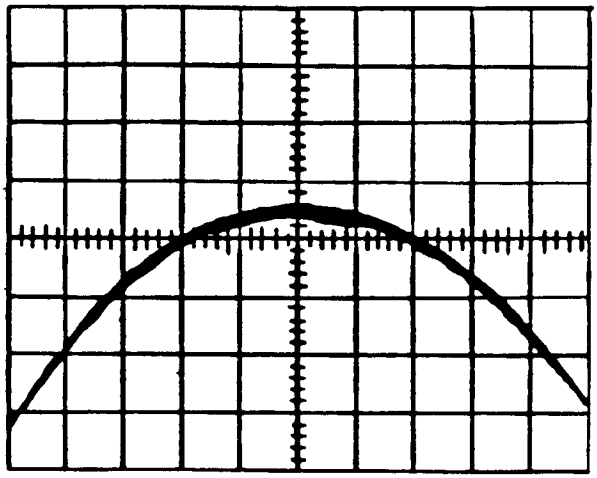
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Expand this waveform X10 horizontally and change the vertical sensitivity to .5 V/cm. Examine the upper portion of the waveform. Adjust C14 (C20) and C15 (C21), taking a recording after each adjustment, until the waveform resembles the ones in Figure 4.3B.

INCORRECT HIGH SPEED ADJUSTMENT

CORRECT HIGH SPEED ADJUSTMENT





NOTE: VERTICAL = 5V/CM (BOTH DIAGRAMS)

A.

B.

Figure 4.3

This completes the alignment of the unit.

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5. 8210 - CONTROL

Refer to "Basic Control Diagram"

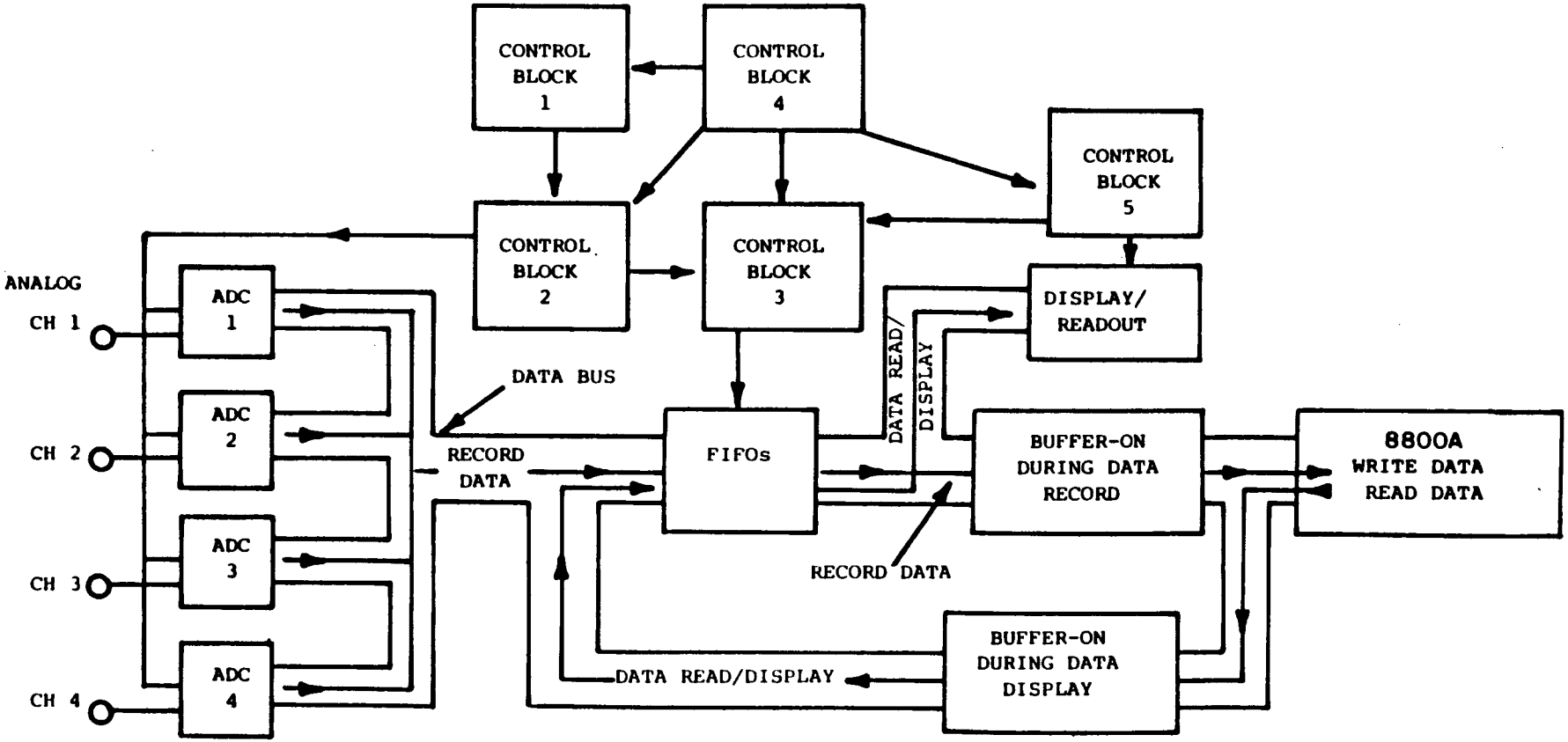
The 8210-2 digital board controls the flow of data from the four analog-to-digital converter (ADC) channels to the 8800A memory module during data recording. When reading or displaying data the 8210-2 board will read data out of the memory to the display circuitry or out to the CAMAC interface.

The data bus used (see diagram) is tristate and allows data to be bused in both directions. When recording data, the ADC's are active, supplying data to the FIFO's which then store data in the memory module. When reading/displaying data, the ADC's are inactive and data is recirculated from the memory to the FIFO's and out to the display/readout circuitry.

Control Blocks 1-5 control the flow of data and are described in this manual. Briefly they are:

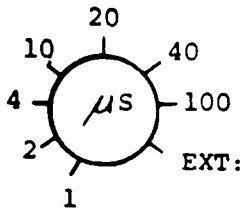
CONTROL BLOCK #	FUNCTION
1	Master clock control for data recording.
2	Control of data input from ADC's.
3	Controls FIFO input and output, timing, and 8800A.
4	Control of timing when switching from data record to data readout/display.
5	Control of data display/readout.

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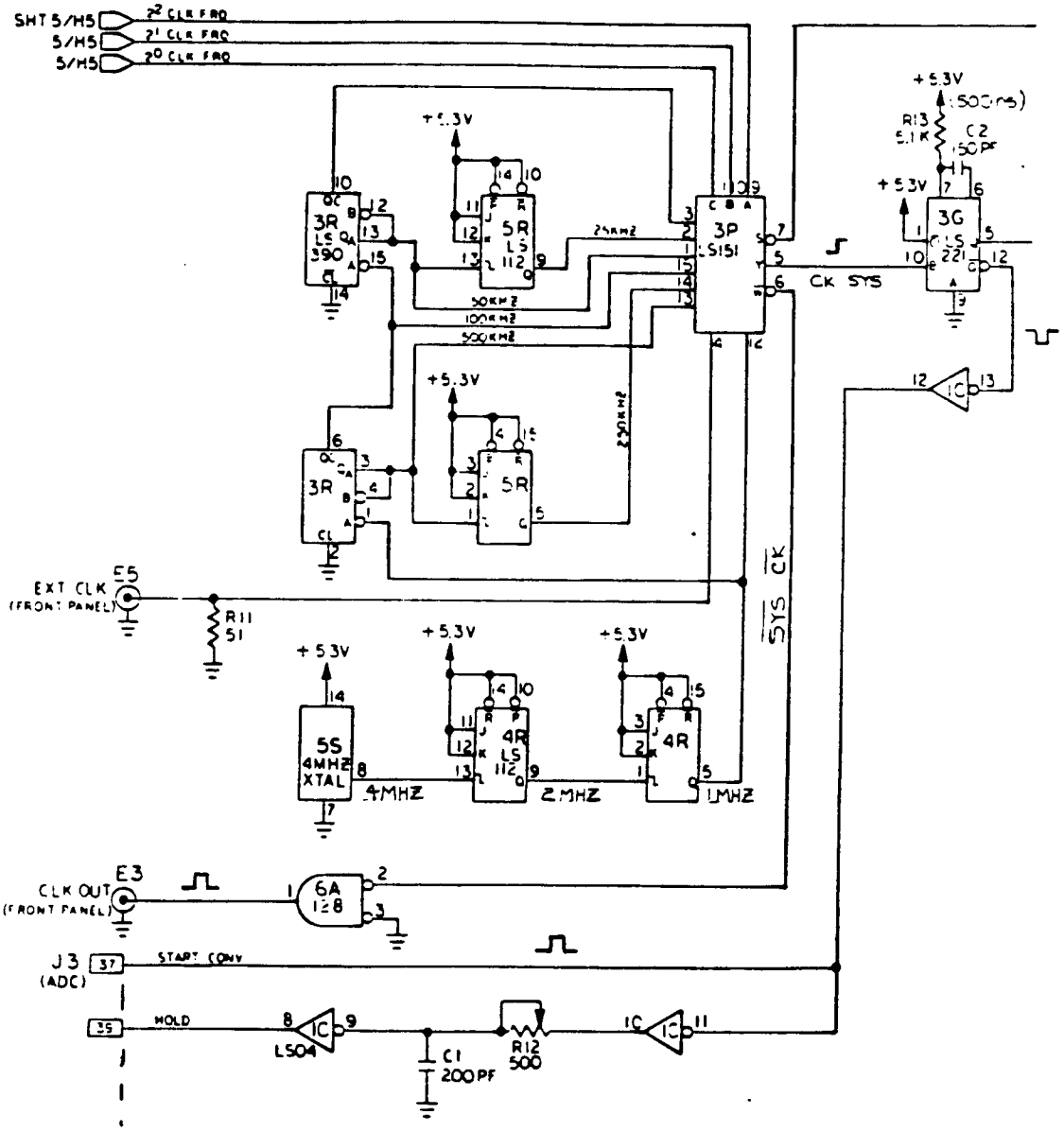
8210 - BASIC CONTROL

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CONTROL BLOCK 1

SAMPLING INTERVAL FRONT PANEL SWITCH

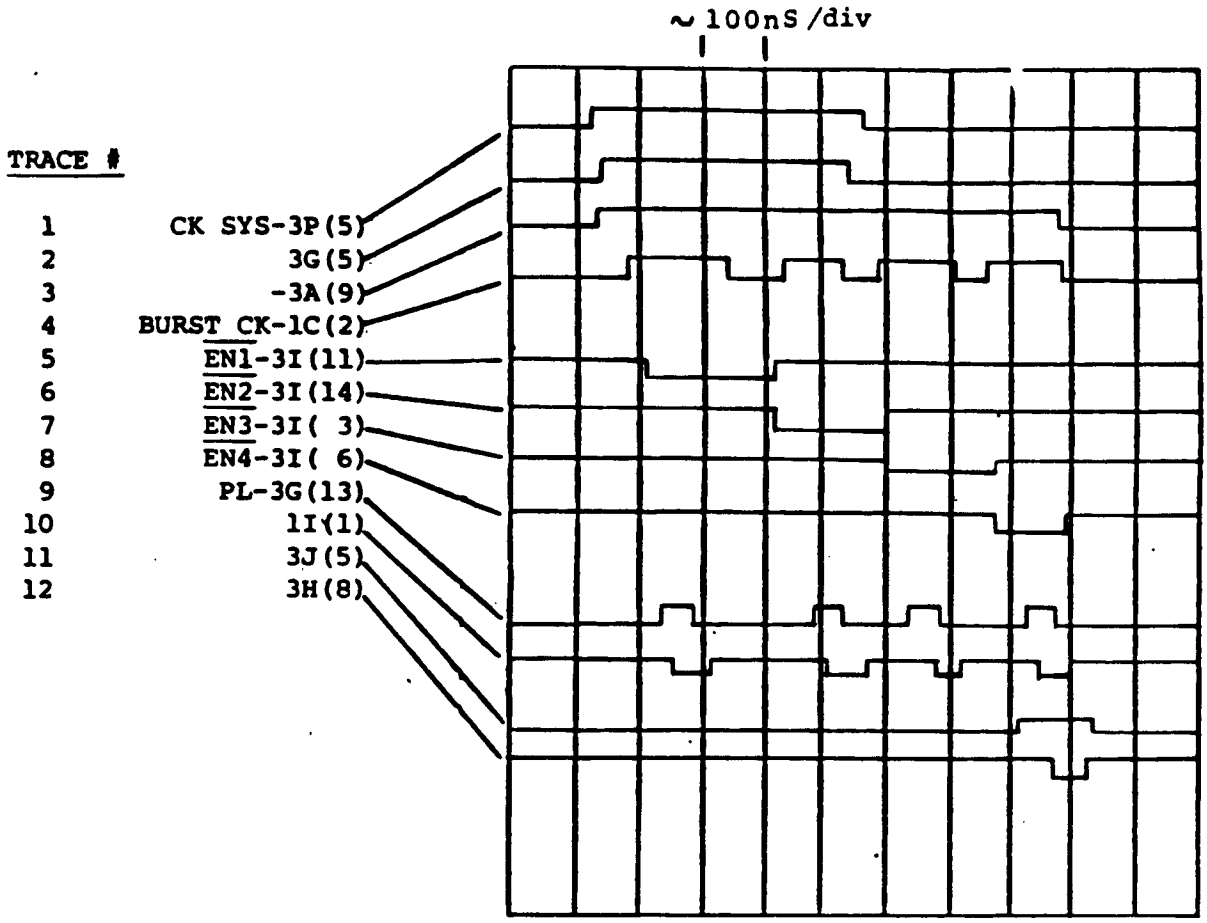


TO ADC BOARD
Int. Cct. 3A

Fig 3-5

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TIMING DIAGRAM FOR CONTROL BLOCKS 1 AND 2



SETUP: 4 Channel sampling mode

1 µsec sampling rate
Scope trigger = Clock out

Diagram 5.1

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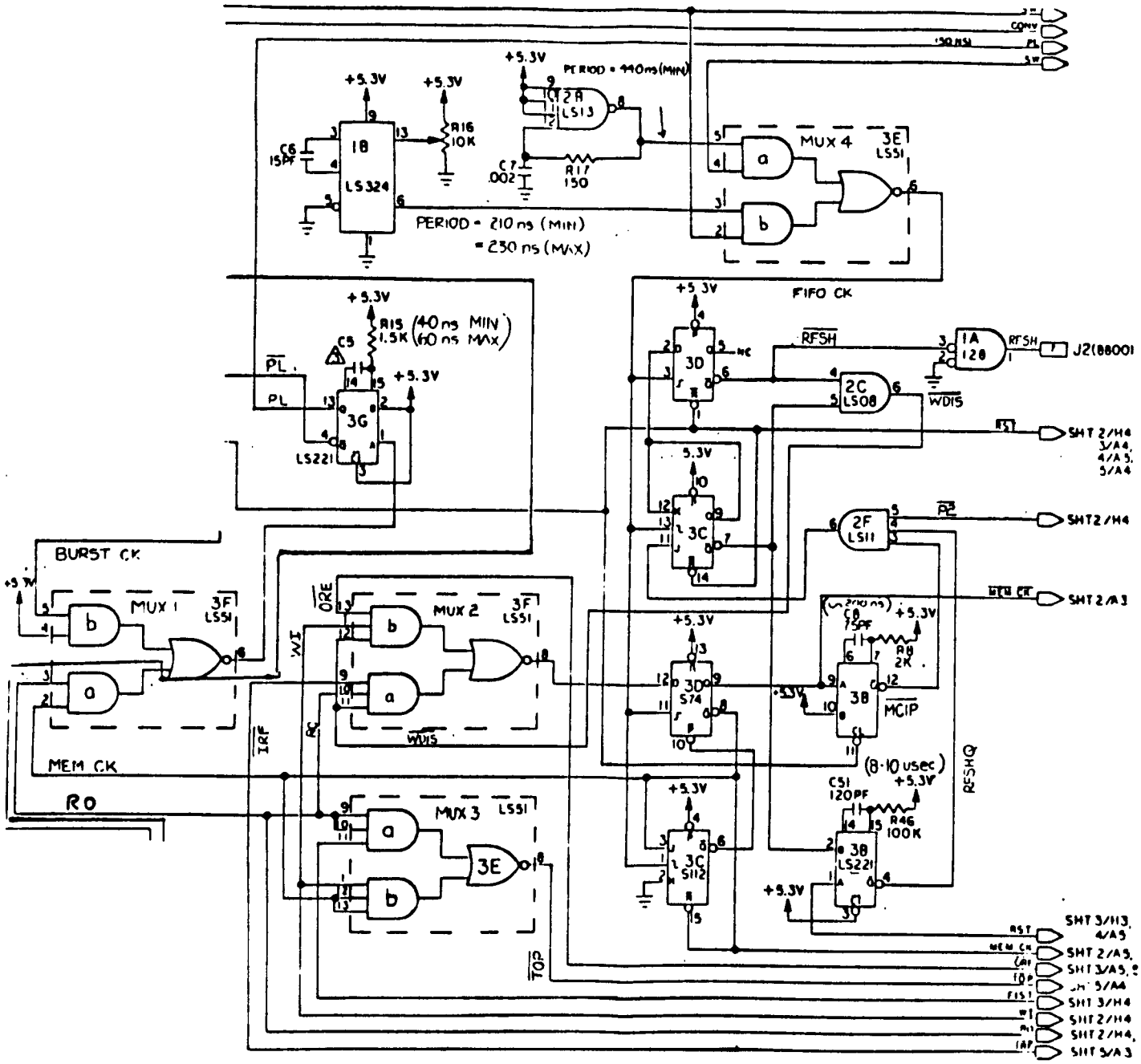


Fig 5-3 CONTROL BLOCK 3

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CONTROL BLOCK 1

SYSTEM CLOCK GENERATOR

(Refer to Diagram 5.1)

FUNCTION: Generates - a) Clock for system timing; b)"Hold" and "Start Conv." commands for ADC Boards; c) and triggers Control Block 2 to input data from ADC data storage latches.

DESCRIPTION: A 4 MHz crystal oscillator (5s) is divided down to 1 MHz (4R). This output is fed to other dividers (5R and 3R) and all clocks are then fed to clock multiplexer (3P). Output of 3P (Ck Sys.) is the sampling clock which controls system timing when recording data. The output frequency of 3P depends on the position of the front-panel switch which controls 3P (9, 10, and 11). The positive edge of 3P (5) triggers 3G (trace 2), a 500 nsec monostable, which generates the hold-and-the hold and start convert pulses for the ADC boards. 3G(5) also triggers control block 2 to input data from the ADC's and temporarily store the data in the 9403 FIFO's.

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CONTROL BLOCK 2

STORAGE OF ADC DATA INTO FIFO

(Refer to Figure 5.1)

FUNCTION: Control Block 2 is triggered by the positive edge of 3G (5). Once triggered it will fetch data from the ADC storage latches and temporarily store in the 9403 FIFO's. The number of data words fetched depends on the position of the front-panel switch INPUT CHANNELS.

DESCRIPTION: The positive edge of 3G (5), trace 2, triggers 3A (9) to turn on (trace 3). This enables the "Burst Ck", (trace 4) to turn on. The number of pulses in the burst depends on the number of channels selected (1, 2 or 4). This is controlled by shift register 3I and multiplexer 3J. As a "1" is shifted through 3I, the "Enable Data" signals to the ADC boards are generated (trace 5, 6, 7, 8). When an "Enable Data" line is low, data from the corresponding ADC storage latch will appear and be loaded into the FIFO's. The shift sequence is terminated by multiplexer (3J) which is controlled by the INPUT CHANNELS switch. After 3J (5) goes positive, the sequence will be terminated (traces 11 and 12). Burst Ck also is gated through MUX 1 (3F) to trigger 3G (trace 9). The output of 3G is the parallel load pulse (PL) to the FIFO's which loads the data into the FIFO's. Once a FIFO has accepted data it responds with "INPUT REGISTER FULL", trace 10, which means that no more data can be stored until this signal goes high again. The lower half of MUX 1-3F (3 and 2) is disabled during the data taking mode. Similarly the upper half -3F (5) is disabled in the readout and display mode.

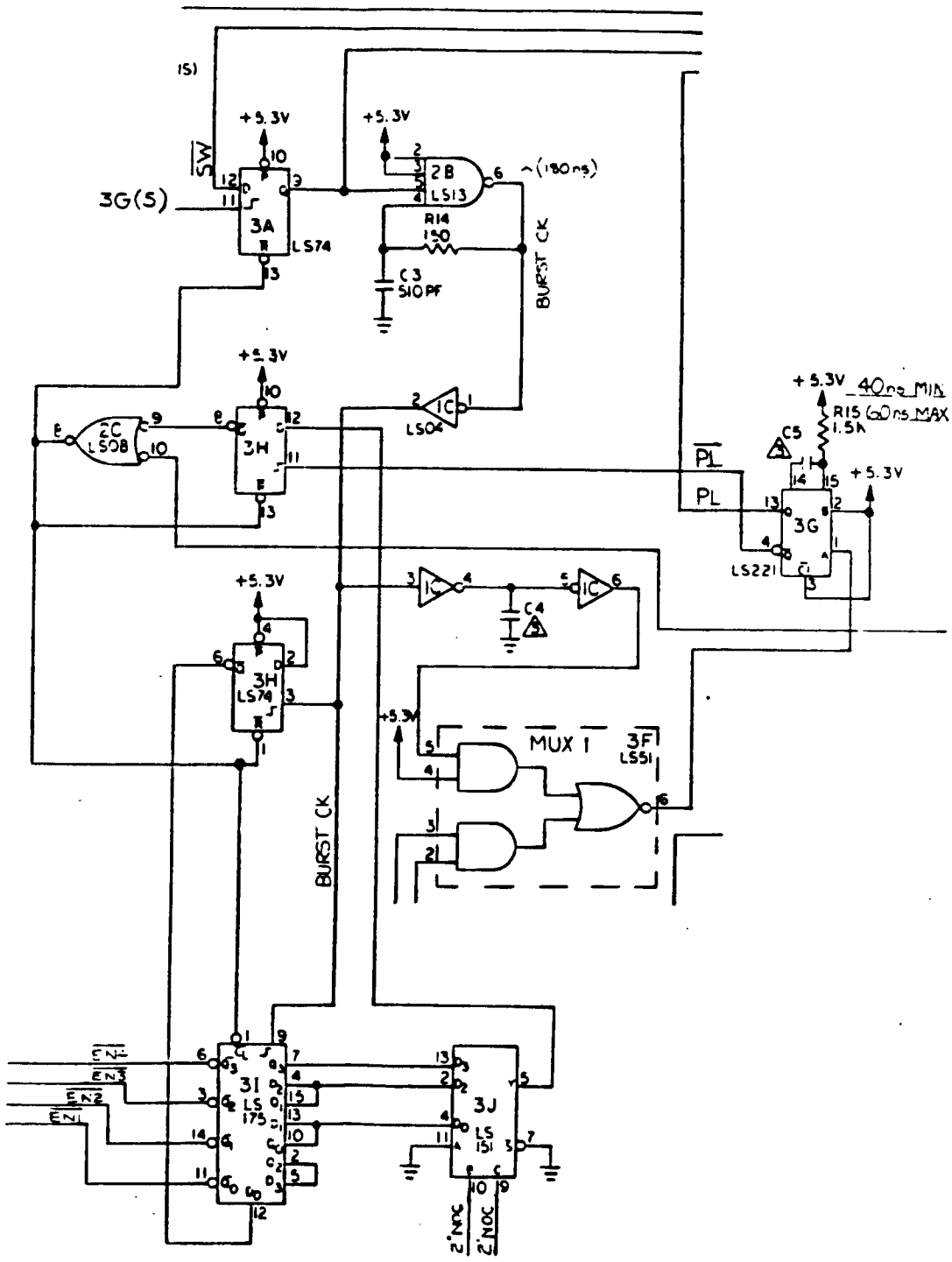
POSSIBLE PROBLEMS:

1. The Burst Ck does not terminate its sequence properly and free runs. This may be caused by the period of 2B - "Burst CK" being too short.

2. In the data taking mode the FIFO's data are always unloaded faster than loaded. This means that IRF "INPUT REGISTER FULL" should always be high when PL goes high. If it is not then the FIFO is bad or data is not being unloaded fast enough and the FIFO is overfilling. Overloading of the FIFO's can be detected by noting if all three of the IRF lines from the three FIFOs are low together when a PL is performed.

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CONTROL BLOCK 2



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CONTROL BLOCK 3

(Refer to Figure 5.2)

FUNCTION: Control block 3 has two functions; 1) In the data recording mode it controls the unloading of data from the FIFO's and writing and refreshing of the 8800A memory. 2) In the readout and display mode it controls the loading of data into the FIFO's and readout and refreshing of the 8800A.

CONDITIONS: Data recording mode: MUX 1b, 2b, 3b, 4b enabled (chips 3F, 3E).

MUX 1a, 2a, 3a, 4a disabled (chips 3F, 3E).

Readout and display mode: MUX 1a, 2a, 3a, 4a enabled (chips 3F, 3E).

MUX 1b, 2b, 3b, 4b disabled (chips 3F, 3E).

DESCRIPTION:

a) Data Recording Mode:

After data is stored in the FIFO's by PL it bubbles to the top. By lowering the ORE signal (pin 23 of 1I, 1H, 1F) the FIFO indicates that data is available to be removed. These signals propagate through MUX 2b and appear as a TTL low at 3D (12) (Trace 1). On the next positive edge of the FIFO Ck (Trace 2), 3D (9) changes state (Trace 3) which generates a MEM CK to the 8800A module. On the positive edge of MEM CK the 8800A will store the data appearing at the FIFO outputs. MEM CK also propagates through MUX 3b to generate TOP (transfer out parallel) which transfers the data word out of the FIFO. It should be noted that the purpose of chip 3C (3, 1, 6, 15) is to pulse shape MEM CK. MEM CK is turned on by the positive edge of FIFO CK and then turned off by the FIFO CK negative edge via 3C (6). When MEM CK goes high it triggers MCIP-3B (12) (Trace 4) which indicates a Memory Cycle in Progress. This signal is used to block refreshing of the memory during a memory read or write cycle. Note: Overlap of MEM CK and RFSH will cause invalid data to be read or written in the 8800A. There must be a minimum of 400 nsec between positive edges of MEM CK and RFSH.

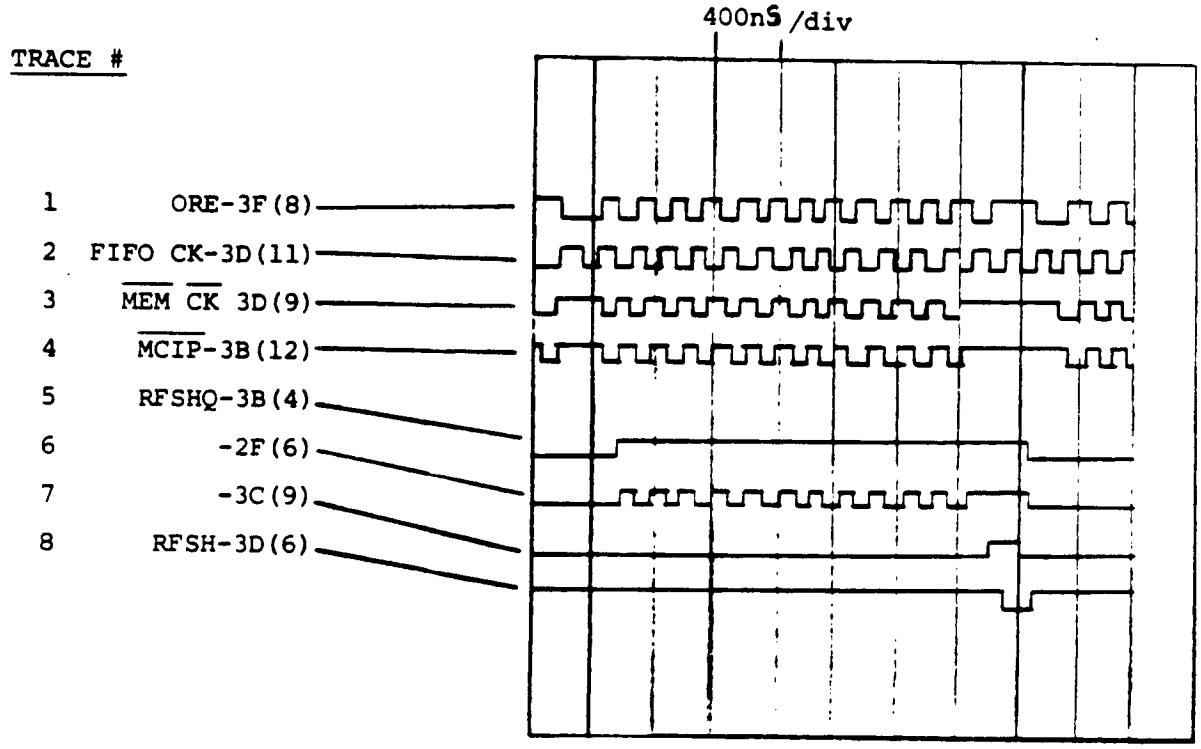
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Every 8 to 10 μsec, Control Block 3 will insert a refresh cycle to refresh the dynamic memory in the 8800A. When RFSHQ-3B (4), Trace 5, goes high, then it is time to do a refresh. Since the FIFO's are always unloaded faster than they are loaded (in the data recording mode) there will be some FIFO CK periods during which there is no data available for storage into the 8800A. It is only during these times that refreshes are allowed. Note that "RFSH"-3D (6), Trace 8, occurs only when MCIP is not present even though RFSHQ, Trace 5, has been present for many FIFO CK periods Once a refresh cycle is started WDIS (Write disable) - 2C (6), is lowered to stop MEM CK from being generated during the refresh (Trace 7).

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TIMING DIAGRAM FOR CONTROL BLOCK 3

Figure 5.2



SETUP: 4 Channel mode

1 μsec sample rate

Data recording mode

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CONTROL BLOCK 4

SWITCH OVER TIMING

(Refer to figure 5.4 and sheet 2 of schematic)

FUNCTION: Controls the switching of control functions from the data recording mode to the readout and display mode.

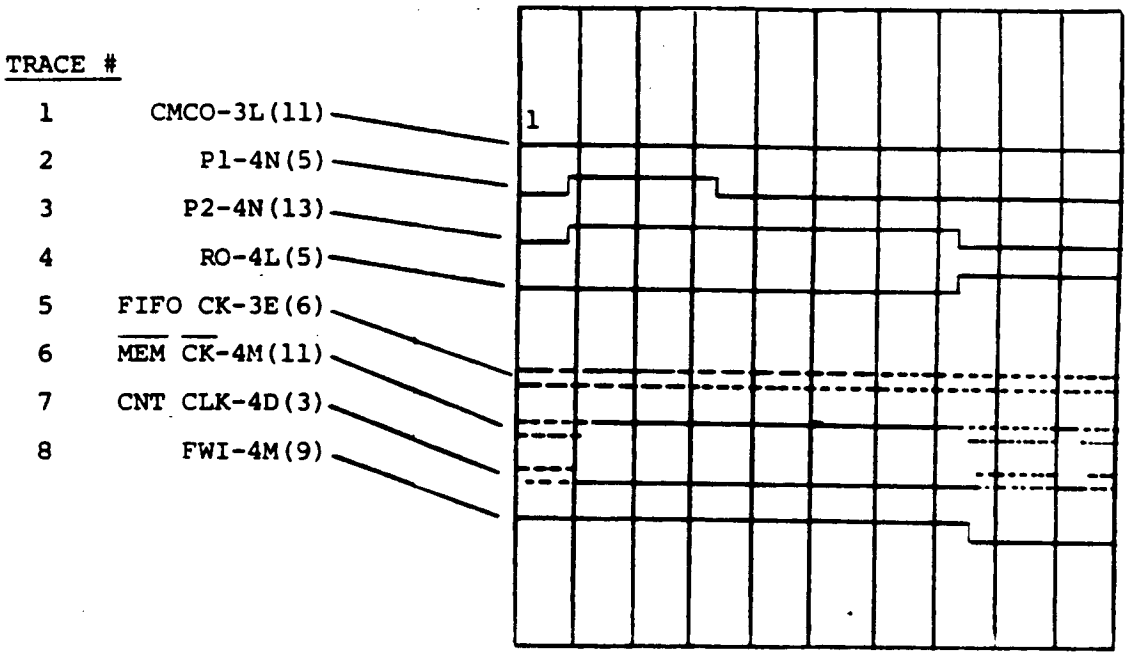
DESCRIPTION: Counters 3N, 2N, 2M, and 3M perform two functions. In data record mode they count the number of post-trigger samples and then trigger the logic to switch from data record to the readout/display mode. In the readout/display mode they count the number of words read out of the 8800A. At the beginning of each 8800A readout scan they trigger FWI (First Word In) into the FIFO's. FWI indicates that the data word being loaded into the FIFO's corresponds to the earliest sample digitized in Channel 1. After FWI emerges from the FIFO's (now called FWO-First Word Out) it initializes the readout/display circuitry.

After the post-trigger samples have been performed CNCO-3L (11), Trace 1, is generated. This triggers PL (Trace 2) which triggers P2 (Trace 3). P1 and P2 are used to create pauses between the data recording mode and the display/readout mode. These pauses are necessary to allow a clean change of control functions. P1 must be at least 10 µsec longer than P1. During P1 and P2 all multiplexing logic is switched and the 8800A is changed from the write-in to the readout state.

NOTE: This sequence is most easily seen by issuing F(9)s at a 10 cycles/sec rate; pull pin 5M (2) out of the socket and jumper connect to pin 2C (2). This will cause the 8210 to go into the display mode after the 8800A fils memory once. The front-panel LED will be flickering on and off at 10 Hz/sec. Trigger scope on 3L (11) to see the se uence.

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TIMING DIAGRAM FOR CONTROL BLOCK 4



SETUP: 4 Channel Mode

1 μsec Sample Rate

Fig 5-4

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CONTROL BLOCK 5

DISPLAY/READOUT CONTROL

(Refer to Figure 5.5)

FUNCTION: To decode the 8800A data for output to the display generator or CAMAC readout.

DESCRIPTION: Display Mode: (in this mode 4H (6) is always TTL high and 5G (all), 4G (11, 12, 13), 4F (1, 2, 3), and 5H (9, 11, 12) are inactive - these IC's are active only during CAMAC readout.

The data decode circuitry is activated by a low transition of 4P (3) (Trace 1). This indicates that data is ready to be outputted from the FIFO's. The first data word to come out of the FIFO's corresponds to the earliest sample digitized in channel 1 and is flagged by FWO (First Word Out), Trace 3 being high. When 4P (3) goes low it triggers 6R (13), Trace 2, and this is gated with FWO at 4F (11), Trace 4. This signal, in turn, activates flop 5H (5 and 6). The purpose of this circuitry is to scan the correct number of channels and then latch the proper data into the display latches (1L and 2K). Assume that the front-panel display switch is set to channel 3 (number of channels = 4). The data coming out of the 8800A will look like:

CH 1	SAMPLE 1	(FWO)
CH 2	SAMPLE 1	
CH 3	SAMPLE 1	
CH 4	SAMPLE 1	
CH 1	SAMPLE 2	
CH 2	SAMPLE 2	
CH 3	SAMPLE 2	
CH 4	SAMPLE 2	
CH 1	SAMPLE 3	
CH .	. .	
CH .	. .	
CH .	. .	

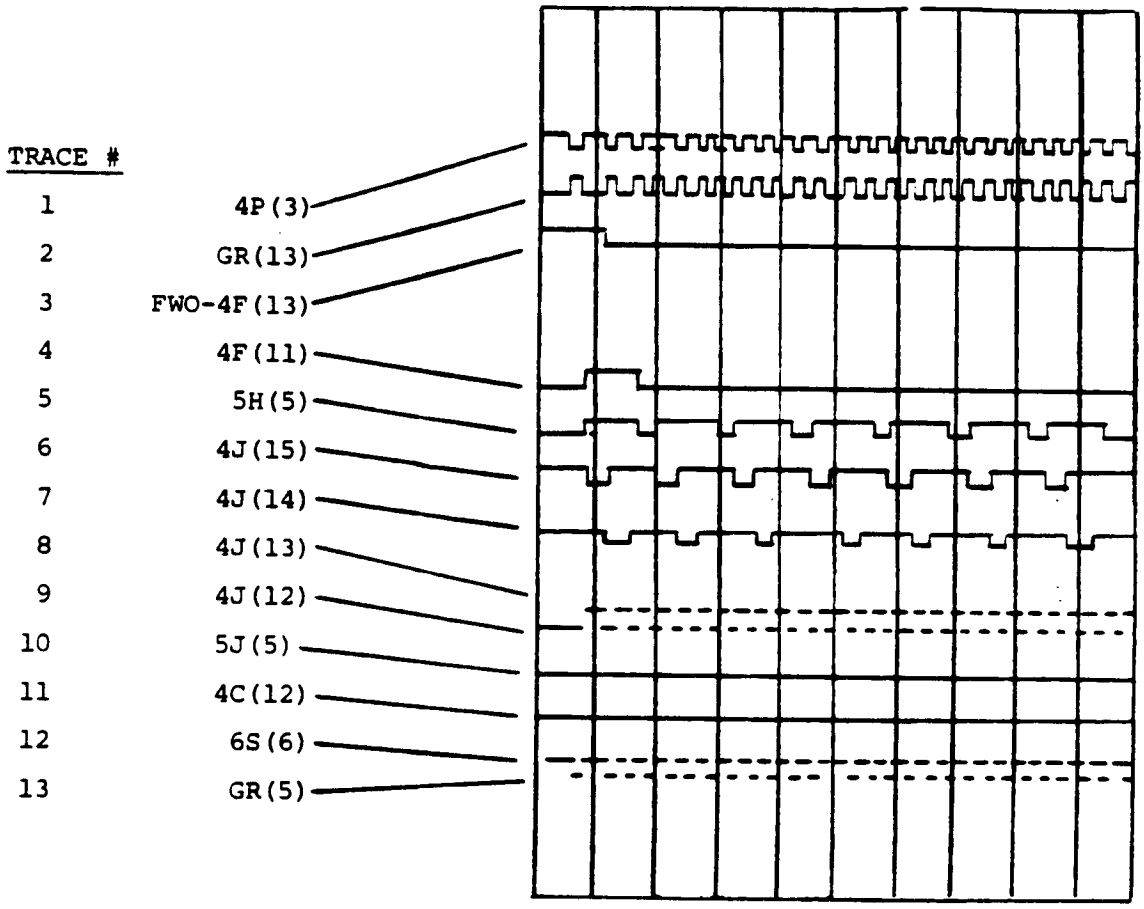
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The decode circuitry must first scan through CH1, sample 1 and CH2, sample 1, and then latch CH3, sample 1 into display latches. From this point on channels 4, 1 and 2 are rapidly scanned and then CH3 data latched again. That is, on the first pass, two data words are discarded and the third latched; from then on, three data words are discarded and the fourth latched. The circuitry works in a similar fashion for displaying other channels. The circuitry which determines when to latch the proper data is composed of 5H, 5K, 4J, and 5J. I.C., 5K is a tristate buffer which is connected to the front-panel switches. When 5H (5) goes high, it activates 5K (4 and 1) which places the DISPLAY CHANNELS switch position of 5J (1 and 11). 5J is a multiplexer which selects one of four inputs which are sequentially lowered from 4J. When 4J (15) is low, it indicates that the data being output from the FIFO's is from CH1. Similarly 4J (14) indicates CH 2 data and so on (Traces 6, 6, 8, and 9). When displaying CH 3, the output of 5J (5) (Trace 10) will go low as soon as 4J (13) goes low indicating that CH 3, sample 1 data is ready to be latched. This signal then propagates through 4C (12) to become the latch pulse. Note that the output of 4F (8) resets 4J and 5H. This enables 5K (10 and 13) to place the INPUT CHANNELS switch position on 5J. From now on 4J will scan through to 4J (12) (Trace 9) and generate latch pulses. This latches in every fourth data word. Data is removed from the FIFO's when GR(5) triggers (Trace 13).

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Figure 5.5

TIMING DIAGRAM FOR CONTROL BLOCK 5



CONDITIONS: Display mode

4 Channel/1 μsec Sampling Rate

Displaying Ch. 3

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DATA READOUT AND DISPLAY MODE:

In this mode the control block functions as before except that:

1) Data is loaded into the FIFO's from the 8800A and unloaded into the DAC display and readout latches.

2) Data is unloaded. This is because data must be inputted into the DAC display latches at a constant rate in order to prevent display jittering.

3) The MEM CK pulse (which now reads data out of the 8800A) is triggered by IRF which means there is room to store a word in the FIFO's. MEM CK then triggers PL which in turn actually loads the data.

4) FIFO CK runs at a slower speed (440 nsec) since the 8800A readout speed cannot exceed 400 nsec/cycle.

5) TOP is generated by the display and readout control block.

POSSIBLE PROBLEMS:

a) If "FIFO CK" is set too fast (210 necs) then the 8800 may not have time to complete a memory cycle in the data recording mode.

b) If "FIFO CK" is set too slow (230 necs) the FIFO's may not be unloaded fast enough resulting in data overflow in the data recording mode.

c) In the readout mode, setting FIFO CK faster than 440 nsec may not give the 8800A time to complete the readout cycle. Slower than 500 necs may result in display jitter.

NOTE: When viewing these signals on a normal scope it will be hard to see the pattern shown on diagram 2 as RFSHQ, ORE and FIFO CK are all asynchronous to one another. For correct operation check that:

1) Monostable and FIFO CK timing is correct.

2) RFSH does not occur during MEM CK and vice versa.

3) Make sure that 3C is a 74S112 and 3D is a 74S74 not 74LS112 or 74LS74.

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6. APPENDIX A- POST-TRIGGER SAMPLES

This appendix describes the post-trigger sample (PTS) control header located at position 3L on the 8210-2 (digital) board. The header sets the range of PTS that are available by the front-panel PTS switch and also sets the amount of total memory connected to the 8210.

The number of PTS taken per channel after receipt of the stop trigger is controlled by programming a 16-bit binary number. Three bits of this number are controlled by the front-panel switch and the remaining 13 are set by jumper options. The position of the three controllable bits within the 16-bit word is set by jumpers on the platform pin assignments. Before receipt of the stop trigger, the 16-bit data word is loaded into the counters. Afterwards, the counters count up until the appropriate overflow is detected. The number of PTS is independent of the number of channels selected. There is, however, a constraint that the maximum PTS is one-half of the total memory size. (Total memory size is 32K times the number of memory modules).

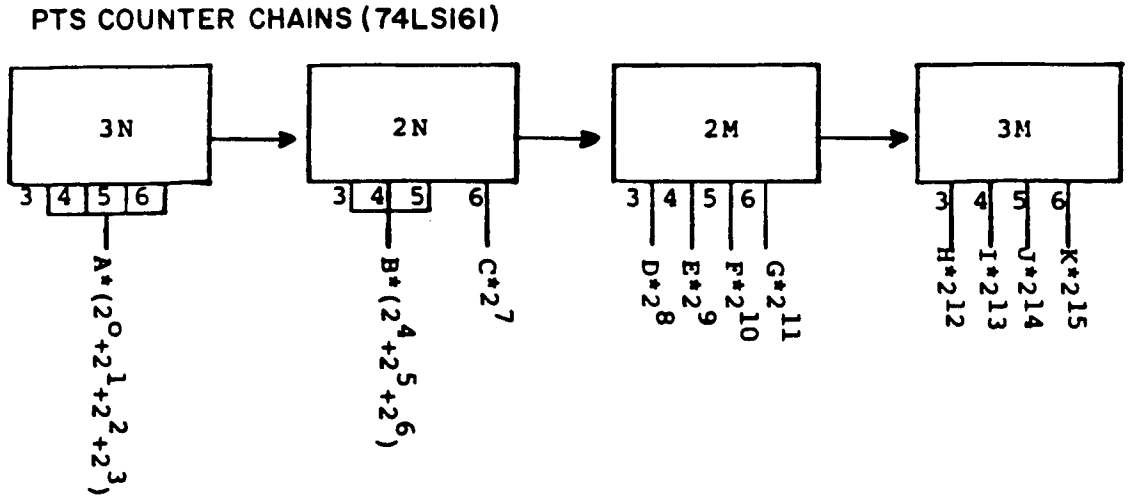
To program the range of PTS that is controllable from the front-panel switch, find the PTS table desired and then program the header according to the table.

Each table has three columns labeled "PTS CONTROL" that show where the front-panel PTS switch is wired into the 16-bit counter word. Connect the header pins 2^0, 2^1, and 2^2 to the corresponding letter designated pin. (Example: for table 8, connect PTS switch bit 0 (2^0) to F, bit 1 (2^1) to G, and bit 2 (2^2) to H). Connect the other pins to "1" or "0" as shown. A "1" means the pin should be left open (there are internal pull-up resistors) and a "0" means the pin should be tied to one of the ground pins (pin 12 or 13). Note that the counter bits labeled A,B,C,D,E are permanently set to a "1" and are not brought out to the header platform. Thus, only tables 8, 10, and 12 may be used without internally modifying the 8210. The other tables are included for reference and for use with models 8212 and 2264 digitizers.

Note that the pins labeled J and K (pins 5 and 6) are slightly different than the other letter designated pins. For one memory operation (32K total memory) J must be tied to ground ("0") and K may be either open ("1") or tied to ground ("0") (don't care). For two-memory operation (64K total memory) J must be left open (a "1") and K must be tied to ground (a "0"). For three memory operation (96K total memory) J must be grounded and K left open.

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Figure 6.1

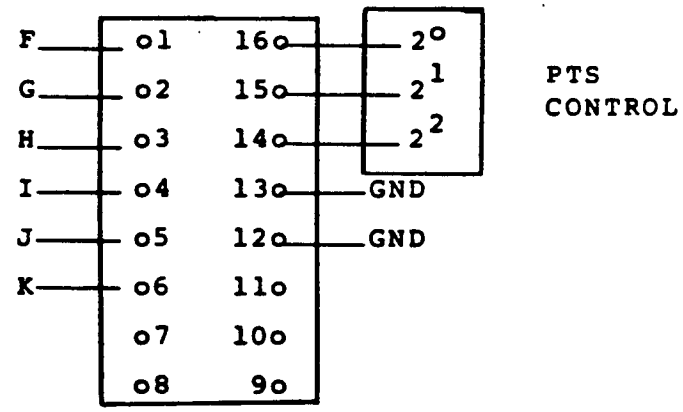


A, B, C, D, E = 1
F, G, H, I, J, K = 0 or 1

PTS CONTROL (2^2 2^1 2^0)	FRONT PANEL SWITCH SETTING
0 0 0	7
0 0 1	6
0 1 0	5
0 1 1	4
1 0 0	3
1 0 1	2
1 1 0	1
1 1 1	0

HEADER CONFIGURATION *

(SOCKET 3L)



(AS VIEWED FROM COMPONENT SIDE)

*NOTES: 1) A "1" is programmed for F,G,H,I,J or K by not installing a jumper. A "0" is programmed by jumpering to gnd.

2) Connect 10 to 11 for one memory module (32K) or 9 to 11 for two memory modules or 8 and 11 for 3 memory modules.

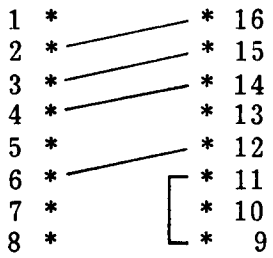
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To program the total memory size, connect pins 8,9,10, and 11 as follows:

Total memory size (in K)	Install jumper between pins
32 (1 memory)	10 and 11
64 (2 memory)	9 and 11
96 (3 memories)	8 and 11

Example:

To make a platform for use with two memories with four active channels and post-trigger samples ranging from 1 to 14337, the pins should be connected as follows:



With this configuration, each of the four channels will take the following number of samples after a stop trigger; (data from table 10)

PTS switch setting	post-trigger samples
0	1
1	2049
2	4097
3	6145
4	8193
5	10241
6	12289
7	14337

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Figure 6.2

1.

						CONTROL 2^2		$2^1 2^0$			
K	J	I	H	G	F	E	D	C	B	A	PTS
0	0	1	1	1	1	0	0	0	0	0	1024
						0	0	1			8967
						0	1	0			7688
						0	1	1			6404
						1	0	0			5123
						1	0	1			3845
						1	1	0			2566
						1	1	1			1287

2.

						CONTROL $2^2 2^1 2^0$					
K	J	I	H	G	F	E	D	C	B	A	PTS
0	0	1	1	1	1	0	0	0	1	1	897
						0	0	1			769
						0	1	0			641
						0	1	1			513
						1	0	0			385
						1	0	1			257
						1	1	0			129
						1	1	1			1

3.

					PTS CONTROL $2^2 2^1 2^0$						
K	J	I	H	G	F	E	D	C	B	A	PTS
0	0	1	1	1	0	0	0	0	0	0	2048
					0	0	1				1792
					0	1	0				1536
					0	1	1				1280
					1	0	0				1024
					1	0	1				768
					1	1	0				512
					1	1	1				256

4.

					PTS CONTROL $2^2 2^1 2^0$						
K	J	I	H	G	F	E	D	C	B	A	PTS
0	0	1	1	1	0	0	0	1	1	1	1793
					0	0	1				1537
					0	1	0				1281
					0	1	1				1025
					1	0	0				769
					1	0	1				513
					1	1	0				257
					1	1	1				1

5.

				PTS CONTROL $2^2 2^1 2^0$							
K	J	I	H	G	F	E	D	C	B	A	PTS
0	0	1	1	0	0	0	0	0	0	0	4096
				0	0	1					3584
				0	1	0					3072
				0	1	1					2560
				1	0	0					2048
				1	0	1					1536
				1	1	0					1024
				1	1	1					512

6.

				PTS CONTROL $2^2 2^1 2^0$							
K	J	I	H	G	F	E	D	C	B	A	PTS
0	0	1	1	0	0	0	1	1	1	1	3585
				0	0	1					3073
				0	1	0					2561
				0	1	1					2049
				1	0	0					1537
				1	0	1					1025
				1	1	0					513
				1	1	1					1

FOR TWO MEMORIES, SET J=1 AND K=0 FOR SAME PTS AS SHOWN IN TABLES.
FOR THREE MEMORIES, SET K=1 AND J=0, FOR SAME PTS AS SHOWN IN TABLES.

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Figure 6.3

PTS TABLE

7

K	J	I	PTS CONTROL 2^2 2^1	2^0	F	E	D	C	B	A	PTS
0	0	1	H	G							
			0	0	0	0	0	0	0	0	8 1 9 2
			0	0	1						7 1 6 8
			0	1	0						6 1 4 4
			0	1	1						5 1 2 0
			1	0	0						4 0 9 6
			1	0	1						3 0 7 2
			1	1	0						2 0 4 8
			1	1	1						1 0 2 4

8.

K	J	I	PTS CONTROL 2^2 2^1	2^0	F	E	D	C	B	A	PTS
0	0	1	H	G							
			0	0	0	1	1	1	1	1	7 1 6 9
			0	0	1						6 1 4 5
			0	1	0						5 1 2 1
			0	1	1						4 0 9 7
			1	0	0						3 0 7 3
			1	0	1						2 0 4 9
			1	1	0						1 0 2 5
			1	1	1						1

9

K	J	PTS CONTROL 2^2 2^1	2^0	I	F	E	D	C	B	A	P T S
0	0	H	G								
		0	0	0	0	0	0	0	0	0	1 6 3 8 4
		0	0	1							1 4 3 3 6
		0	1	0							1 2 2 8 8
		0	1	1							1 0 2 4 0
		1	0	0							8 1 9 2
		1	0	1							6 1 4 4
		1	1	0							4 0 9 6
		1	1	1							2 0 4 8

10.

K	J	PTS CONTROL 2^2 2^1	2^0	I	F	E	D	C	B	A	P T S
0	0	H	G								
		0	0	0	1	1	1	1	1	1	1 4 3 3 7
		0	0	1							1 2 2 8 9
		0	1	0							1 0 2 4 1
		0	1	1							8 1 9 3
		1	0	0							6 1 4 5
		1	0	1							4 0 9 7
		1	1	0							2 0 4 1
		1	1	1							1

FOR TWO MEMORIES, SET J=1 AND K=0 FOR SAME PTS AS SHOWN IN TABLES.
FOR THREE MEMORIES, SET K=1 AND J=0 FOR SAME PTS AS SHOWN IN TABLES.

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Figure 6.4

11

	PTS CONTROL $2^2 2^1 2^0$													
K	J	I	H	G	F	E	D	C	B	A	P	T	S	
0	0	0	0	0	0	0	0	0	0	0	3	2	7	6	8
	0	0	1								2	8	6	7	2
	0	1	0								2	4	5	7	6
	0	1	1								2	0	4	8	0
	1	0	0								1	6	3	8	4
	1	0	1								1	2	2	8	8
	1	1	0									8	1	9	2
	1	1	1									4	0	9	6

12.

	PTS CONTROL $2^2 2^1 2^0$													
K	J	I	H	G	F	E	D	C	B	A	P	T	S	
0	0	0	0	1	1	1	1	1	1	1	2	8	6	7	3
	0	0	1								2	4	5	7	7
	0	1	0								2	0	4	8	1
	0	1	1								1	6	3	8	5
	1	0	0								1	2	2	8	9
	1	0	1									8	1	9	3
	1	1	0									4	0	9	7
	1	1	1												1

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