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# MM8206A LIST MODE MEMORY

- High Capacity: 64K Words
- High Density: Single-Width CAMAC Module
- High Speed: Better than 2.5 MHz Read/Write Speed on External Port
- Random/Sequential Access on CAMAC Port
- Sequential Access on External Port
- Simple Memory Cascading on External Port: Up to 1 Mword of Memory

## LIST MODE MEMORY FOR SPECTROSCOPY ADCs AND TDCs

The Model MM8206A Dual Port Memory Module provides 64K word memory density in an economical CAMAC package. This packaging density allows a single CAMAC crate to hold almost 1.5 megawords of 16-bit memory.

The CAMAC read and write port allows both random and sequential operation (for block transfers) with the address auto-increment feature. The external port has sequential access in both read and write modes. The straightforward structure of the external bus simplifies interfacing of custom data sources to the convenient CAMAC standard. By simple interconnection, multiple memory modules can be cascaded to a total of sixteen modules of up to 1 megaword of memory. In addition, a two-module circular buffer can be configured to provide a simple CAMAC interface for continuous data sources, since the LAM generated when one memory module is filled can initiate a readout of that module, while the second module continues to store data. Other applications include local memory in a crate for the host processor, communications and data transfer points for multiprocessor CAMAC systems, and convenient source of data words to interface a control scheme to CAMAC.

Several specific data acquisition and control functions are implemented by part and preset LeCroy modules in conjunction with the MM8206A.

## SPECIFICATIONS

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### MEMORY

**General:** Organized as a dual port memory with access by one port at a time. CAMAC commands determine which port is currently enabled. 64K x 16 bit Dynamic RAM ICs are used. Both the CAMAC and external ports operate in the auto-refresh mode. However, the external port may be operated in an access-refresh mode which permits higher access rates.

**Speed:** The CAMAC port will operate up to the maximum 1 MHz rate. The external port will operate in auto

-refresh mode from DC to > 1.0 MHz and in access-refresh mode from 75 kHz to > 2.5 MHz.

## CAMAC PORT

**Memory Read Operation:** The CAMAC Memory read operation F(2) is buffered through an output register. This register is loaded at the time of an address write operation F(18), so the subsequent read operation F(2) reads out data from that location. In addition, the read operation causes the register to be updated. Consequently, the address auto-increment mode F(25) allows sequential access to the memory for block transfers of data. (Note: Such block transfers require one additional read operation F(2), following an address write operation F(18). Refer to manual.)

**Memory Write Operation:** The CAMAC memory write operation F(16) writes directly into the current memory address. Address auto-increment mode F(25) provides for sequential access for block transfers.

## EXTERNAL PORT

**General:** The external data bus is on a rear-panel connector, which mates with Model DC8800 Data Cable. External port is a read or write sequential port (memory address auto-increment must be enabled). Memory strobe is assumed to be an external device on the data bus. The external port can be daisy-chained with other modules to achieve cascading of multiple memory modules. Memory control is then accomplished by connecting the Cascade Control output of a module to the External Port Enable input of the next module.

### Data Bus Signals:

&shy; Memory Strobe &shy; 50 nsec minimum width, TTL level. Strobed a positive-going edge.

&shy; R/W-TTL high to read, low to write.

&shy; Refresh Control TTL low disables internal auto-refresh and enables access-refresh mode. Refresh control line is ignored when Refresh Enable side-panel switch is in ON position.

&shy; Data 16 bidirectional read/write lines. Data is to be established no later than 50 nsec after the memory strobe for the write mode. Data is available 550 nsec after memory strobe for reading in the auto-refresh mode and 220 nsec after memory strobe for reading in the access-refresh mode.

**Refresh Mode:** The External port may be operated in either auto-refresh or access refresh modes when Refresh Enable side-panel switch is the OFF position. The auto-refresh mode allows operation at rates from DC to > 1 MHz. The access-refresh mode accomplishes refresh during read and write cycles resulting in allowable memory strobe rates of 75 kHz to > 2.5 MHz. Switching between the two modes is controlled by the refresh-control line. The access refresh mode is only operative if the external port is in no way disabled. If the port is disabled for any reason, the auto-refresh mode becomes operative. No memory strobe may occur within 330 nsec of the beginning or end of an access-refresh period.

**LMW Disable:** Module may be configured (Cascade side-panel switch) to disable the external port when memory is full. The external port is then subsequently re-enabled by a positive-going TTL edge at the External Port Enable input or by enabling the external port from CAMAC F(11).

## PORT ENABLE LEDs

**CAMAC:** Lights when CAMAC port is enabled.

**External:** Lights when external port is enabled. Note that either front-panel disable of LMW Disable will extinguish the LED.

## COAXIAL CONNECTORS

**External Port Enable (Input):** TTL low level disables external port. Open input or TTL high level enables external port if external port has been enabled from CAMAC F(11) and if LMW Disable is not active. Transition from low to high at this input resets LMW Disable status; > 8 mA source current.

**LMW (Output):** TTL pulse, 500 nsec width, generated when memory is full. Drives 50 ohm.

**Cascade Control (Output):** TTL level, drives 50 ohm. Transition from low to high occurs when last memory word is addressed or under CAMAC Command F(27). High-to-low transition occurs when External Port Enable receives positive-going TTL edge, or when External port is enabled, F(11) Output is intended to permit cascading of memory modules at the external port by connecting this output to the External Port Enable input or the next module.

## GENERAL

**Cascade Switch:** Side-panel switch set to ON causes external port to be disabled after last memory word has been accessed. Otherwise, subsequent external port memory operations access sequential memory addresses within the module beginning at zero. LNW Disable status is reset (port enabled) by a memory configuration of multiple modules. See manual.

**Refresh Enable Switch:** In the ON position, this switch allows only auto-refresh mode. The OFF position causes the refresh-control line of external port to determine refresh mode when external port is active.

**External Port Clock Termination Switch:** ON position terminates external port clock line in 100 ohm for improved performance for longer bus lines. For cascaded memory modules, only the last module should be terminated.

**Packaging:** IEEE Std. 583-1975. RF-shielded, single-width CAMAC module.

**Power Requirements:** 500 mA at +6 V plus 50 (60) mA per bit word size for 16K word (64K word) version.

## CAMAC COMMANDS

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### CAMAC COMMANDS

**L:** A LAM is generated when last memory word is accessed, if previously enabled by F(26)·A(0).

**X:** An X = 1 response is generated for any valid code.

**Q:** A Q = 1 response is generated in response to F(2). F(2), F(16), and F(18) operations if CAMAC port is enabled and to F(8) if LAM is set. Otherwise, Q = 0.

**Z:** INITIALIZE clears and disables LAM, and enables CAMAC port and address auto increment.

### CAMAC FUNCTION CODES

**F(0)·A(0):** Read memory address register on lines R1-R16.

**F(2)·A(0):** Read data from memory at the address register. If auto increment is enabled the address register will be subsequently incremented. Data buffered through Data Output Register.

**F(8)·A(0):** Test LAM. Q = 1 if LAM is set.

**F(9)·A(0):** Clear module. Sets memory address to zero, clears and disables LAM, and enables CAMAC port and address auto increment.

**F(10)·A(0):** Clear LAM.

**F(11)·A(0):** Enable external port.

**F(16)·A(0):** Write data to memory at the address in the address register. If auto increment is enabled, the address register will be subsequently incremented.

**F(17)·A(0):** Disable address auto increment.

**F(18)·A(0):** Load memory address register from CAMAC lines W1-W16.

**F(19)·A(0):** Disable external port.

**F(24)·A(0):** Disable LAM.

**F(25)·A(0):** Enable address auto increment.

**F(26)·A(0):** Enable LAM.

**F(27)·A(0):** Set Cascade Control output to high state.

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