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Find the *Lumistar LS-50-V* at our website: ***Click HERE***

LUMISTAR

LS-50-V VME Multi-function PCM Decommutator

Data Sheet

Description:

The Lumistar LS-50-V VME Multi-function PCM Decommutator offers the greatest flexibility in the industry by incorporating up to 10 functions typically encountered in test applications in a single VME card slot. Five functions are accomplished on the main board and additional functions are achieved through the use of low-profile daughter-boards. The main VME board shown below contains a PCM Simulator which can also operate as a BERT, PCM Decommutator, IRIG Time Code Reader, and IRIG Time Code Generator. Two unique daughter-boards are accepted by the LS-50-V but only one can be used at a time due to the physical size of the VME board. One of these is the LS-40-DB-10, LS-40-DB-20 or LS-40-DB25 *Bit Synchronizer Daughterboard*, and the other the LS-55 *Multi-function Decom Daughterboard*. The LS-40-DB accepts PCM inputs up to 10 or 25 Mbps (depending on the model selected) and corrects for corruption by noise, phase jitter, amplitude modulation, or baseline variations. The LS-55-DB allows the addition of a second multi-function board with 5 additional functions, including second decom, second simulator with BERT capability, time code reader, time code generator.



The IRIG Time Code Reader and Generator operate with IRIG A, B, or G time code formats. The Time Code Generator creates and outputs time information in accordance with IRIG Time Code Standards. The Time Code Reader is typically used to insert time information into the PCM minor frame block of data. The Lumistar LS-50 Decom can be used for extremely large formats (16,383 words per minor frame by 1,024 frames deep) and contains dual ping-pong data buffers with 128K bytes of memory. When used with the LS-55-DB, the second decom can be used for an independent PCM data stream or an embedded data stream in accordance with the IRIG-106 Standard. The PCM simulator generates common, unique, and waveform pattern data words. When used with the LS-55-DB daughterboard, the user can also generate complex data streams with embedded PCM data, or two totally independent data streams.

Key Features:

- **Multifunction PCM Decommutator – up to 10 functions in single VME card slot**
  - **PCM Simulator with BERT Mode**
  - **PCM Decommutator**
  - **IRIG Time Code Reader and IRIG Time Code Generator**
  - **Bit Error Tester**
- **Accepts LS-55-DB Multi-function Decom Daughterboard**
- **Accepts LS-40-DB Bit Synchronizer Daughterboard**

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LUMISTAR

LS-50-V VME Multifunction PCM Decommutator

Data Sheet

SPECIFICATIONS:

PCM DECOMMUTATOR:

Input Data Rate	10 bps to 20 Mbps
Input Signals	NRZ-L data & 0 degree clock
Input Levels	Single-ended TTL & RS-422
Word Length (VWL)	Variable from 3 to 16 bits per word on a word-by-word basis
CRC checker	CRC16/CCITT
Minor Frame Length	2 to 16,383 words per minor frame
Major Frame Length	Up to 1024 minor frames per major frame
Bit Order	MSB or LSB-first (word-by-word basis)
Frame Sync Pattern	Up to 64 bits (any pattern with don't care bits (X) may be used)
Frame Sync Location	Beginning or end of the frame
Frame Sync Strategy	Adaptive mode (search-lock-verify) & burst mode (search-lock)
Sync Error Tolerance	0 to 15 bits (selectable)
Sync Slip Window	1 or 3 bits wide (selectable)
Data Polarity	Normal, inverted or automatic
Subframe Sync	FCC (FAC), SFID or URC (Optional)
URC Location	Any 64 bit window within the first minor frame not including the last bit in the minor frame
SFID Location	Any series of contiguous bits not including the last bit in the minor frame
System Output	Buffered output with status, time, & data

IRIG A/B/G READER/GENERATOR:

Time Reader Input Format	IRIG A, B, or G
Input signal level	1V p-p nominal
Latency	2µsec (maximum)
Data Outputs	Automatic time tags for PCM data blocks (time accessible in register space)
Time Generator Output	IRIG A, B, or G

BERT: (Requires bit sync user SW)

Pseudo-random patterns	11 and 15 bit
Bit Error Rate	Would be indicated on Software
Error Count	Would be indicated on Software
Forced Error Capable	Yes
History Log	Would be indicated on Software

PCM SIMULATOR:

Outputs	Data, 0 degree clock & minor frame strobes
Output Levels	Single-ended TTL & RS-422
Output Data Rate	64 bps to 20.0 Mbps (NRZ codes) 64 bps to 10.0 Mbps (all other codes)
PCM Codes	NRZ-L/M/S, BIϕ-L/M/S DM-M/S, RNRZ-L (2^{11}-1, 2^{15}-1)
Word Length (VWL)	Variable from 3 to 16 bits per word on a word-by-word basis
CRC Generator	CRC16/CCITT
Minor Frame Length	2 to 16,383 words per minor frame
Major Frame Length	Up to 1024 minor frames per major frame
Bit Order	MSB or LSB-first on a word-by-word basis
Frame Sync Pattern	Up to 64 bits (any series of 0s or is 1s may be used)
Sub-Frame Sync	FCC (FAC), SFID & URC; URC location may be any 64 bit window within the first minor frame not including the last bit in the minor frame
Common Words	May be a single value or selected from a group of one minor frame or 2048 words whichever is less. Data may be changed while operating.
Unique Words	Seven may be programmed in any mainframe, super-commutated, or subcommutated channel. Data may be changed while operating.
Waveform Words	Five may be programmed to appear in every frame at the same location. Data may be changed while operating.

MECHANICAL:

VME Decom Form Factor	6U
Daughterboard Form Factor	LS-40-DB for Bit Synchronizer LS-55 for Universal Daughterboard

ENVIRONMENTAL:

Temperature (Operating)	0 to 50 ^{o}C
Temperature (Non-Op)	-25 to +70 ^{o}C
Humidity (Operating)	10% to 90% Non-Condensing
Humidity (Non-Op)	Packaging must prevent contact with moisture and contaminants
Special Handling	Standard ESD methods required

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Specifications are subject to change. Please verify the latest specifications at time of order. ***10-26-10***

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