VMEbus Compatible

MVC Sierra & MVC High Sierra 16-Port Communications Multiplexors

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Appendix A - Technical Information

Introduction

Macrolink's MVC Sierra Asynchronous Serial I/O Commux (MVCS) is an advanced high-speed controller for VMEbus D32 applications. Available with 8 or 16 asynchronous serial ports, it supports individual line rates up to 1.5 Mbps, and an aggregate throughput of 48Mbps. Independent baud rates for each port and a wide variety of I/O interfaces allows you to tailor the MVCS for your needs. UART interrupts are combined and presented at paced intervals to the VMEbus, dramatically reducing interrupt handling overhead by the system's Host CPU.

The MVCS combines innovative hardware design with an industry standard 16C650 Serial I/O application interface. The MVCS uses the latest generation UARTs with 64-byte internal FIFOs, resulting in less interrupt overhead and less load on your system. The High Sierra adds deeper transmit and receive buffering FIFOs between the VMEbus and UARTs, lowering VMEbus bandwidth requirements while supporting VMEbus burst rates of over 30 MB/s.

Our serial line conditioners allow the MVCS to handle any mix of line disciplines on the same board in 4-port groups. Up to 4 different serial line conditioners can be installed with up to 8 signals per port for full modem control. Serial connections are via two 100-pin, high-density front panel connectors. A version of the MVCS is available that moves the 100-pin serial I/O connectors and serial line conditioners to an I/O board that is attached to the rear of the MVCS through the P2 VMEbus connector.

Features

- VMEbus Write Posting speeds up card accesses
- Interrupt Processing and Pacing engine significantly reduces system overhead
- UARTs have 64-Byte Deep FIFOs — High Sierra version adds even deeper High-Performance FIFO buffers between the VMEbus and UARTs
- Standard A32/D32 VME Slave Interface
- 8 or 16 ports
- Data rates to 1.38 Mbs with standard oscillator. Data rates to 1.5Mbs when optional 48 MHz auxiliary oscillator is installed.
- Mix RS-232, 422, 485, buffered TTL and MIL-STD-188 — Removable serial line conditioners allow flexibility in changing line disciplines

Unpacking And Inspection

Each MVCS is shipped in a sturdy, reusable padded carton. Optional accessories may be shipped in a separate carton and include I/O interface panels and cables. The shipping carton and packaging material should be retained for future use in moving, shipping, or storage of the board and accessories. Carefully inspect the shipping carton for signs of damage. If any shipping damage is evident, do not open the package. Notify Macrolink and the freight carrier immediately to receive further instructions.

☞ The MVCS uses sensitive electronic circuitry that can be easily damaged by electrostatic discharge. Personnel handling the board must exercise proper static control methods. Open the shipping carton only at an approved static-controlled workstation. An anti-static bag, anti-static bin, or the original packaging material must be used when transporting the board.

Remove the static shielding bag containing the MVCS from the shipping container, then remove the MVCS from the bag. Inspect the board for damage prior to installation. Claims for shortage or damage must be filed within seven days of receipt of the shipment.

Board Configuration

Address Switches

The base address of the MVCS is selected via rotary switches SW 1 and SW 2. SW1 is the most significant nibble of the board's address. Refer to Figure 1-1 to locate the address switches. For example, when the MVCS is located in A32 space and the switches are set to D3, the address of the MVCS will be 0xD3000000.

MVCS Jumpers

The MVCS has two user configuration jumpers. The remaining jumpers are set at the factory and must not be changed. Refer to Figure 1-1 to locate the configuration jumpers.

E3 - Oscillator Select

When this jumper is installed at positions 2&3 (default), the UART clock source is the oscillator at location U25, divided by two. When installed at positions 1&2, the UART clock source is the 14.7456 MHz auxiliary oscillator installed at location U30. The auxiliary oscillator is **not** divided by two.

E4 - Address Space Disable

These jumpers are used to set the address space in which the MVCS is mapped.

Address Space Disable Jumpers

Location	Description
1-2	Removed = Enable A24 Address Space from VMEbus Installed = Disable A24 Address Space from VMEbus
3-4	Removed = Enable A32 Address Space from VMEbus Installed = Disable A32 Address Space from VMEbus

Both jumpers can be removed at the same time. When both jumpers are removed, the MVCS appears in both A24 and A32 address spaces. The MVCS register interface is replicated in both spaces. It is not recommended that you remove both jumpers unless it is required for your installation.

If both jumpers are installed, the MVCS card will not appear in any VMEbus address space.

Replaceable Serial Line Conditioners

The MVCS uses field-replaceable 100-pin Single Inline Module (SIM)-style serial line conditioners that allow easy reconfiguration or repair. To remove a serial line conditioner, release the locking clips at both ends and tilt it towards the front panel of the MVCS. Lift the module from the socket.

To install a serial line conditioner, gently insert it into the socket, with the top of the serial line conditioner angled about 30 degrees towards the front panel. The pin 1 end of the serial line conditioner is oriented towards the bottom edge of the board. The serial line conditioners are keyed to prevent improper insertion. Tilt it to the vertical position until the two locking clips snap into place.

When changing interface types (such as from RS-232 to RS-485), remember to update the driver configuration file, if applicable.

Installing The MVCS

The MVCS must be installed in a backplane that has both P1 and P2 connectors. Remove or open the interrupt acknowledge (IACK IN/OUT) jumpers or switches, as applicable, for the slot in which the MVCS is to be installed. The Bus Request (BR0-3 In/Out) signals are automatically jumpered by the MVCS and do not have to be opened. Slide the board into the slot, ensuring that it is fully seated into the backplane connectors. Tighten the lock down screws to secure the board and guarantee proper RF shielding.

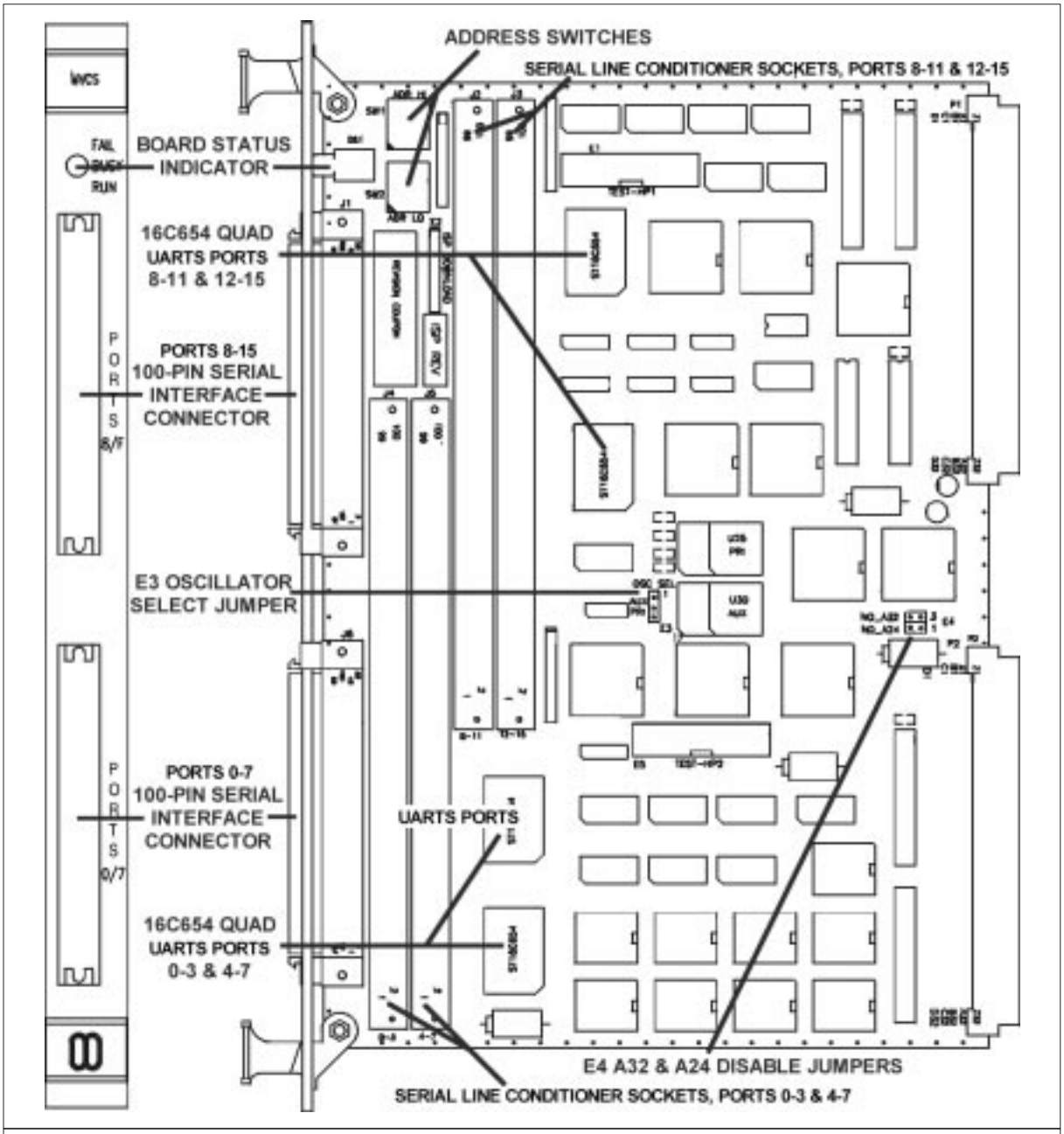


Figure 1-1 – MVCS board layout

Cabling

The MVCS uses high-density 100 pin connectors for the I/O ports. The lower connector provides the interface for ports 0 through 7. If the MVCS is configured as an 8 port board, only the lower connector is installed. The upper connector provides the interface for ports 8 through F. See Figure 1-1 to locate the I/O connectors.

☞ The pins used on the connectors are delicate. Be sure the connectors are properly aligned when installing the cables to avoid bending or breaking the pins. NEVER FORCE THE CONNECTORS TOGETHER.

The standard interface cable sold for use with the MVCS is 6 feet long. Cables in other lengths are available; contact Macrolink for ordering information. Macrolink supplied cables should be used to avoid excessive RF radiation in violation of FCC limits.

Figure 1-2 illustrates connection of two DB25 I/O panels to the MVCS using shielded cables. Figure 1-3 illustrates connection of an RJ45 I/O panel to the MVCS using shielded cables. The I/O panels may be installed in free space in either the front or the back of your CPU chassis. Contact Macrolink for cable and I/O panel ordering information.

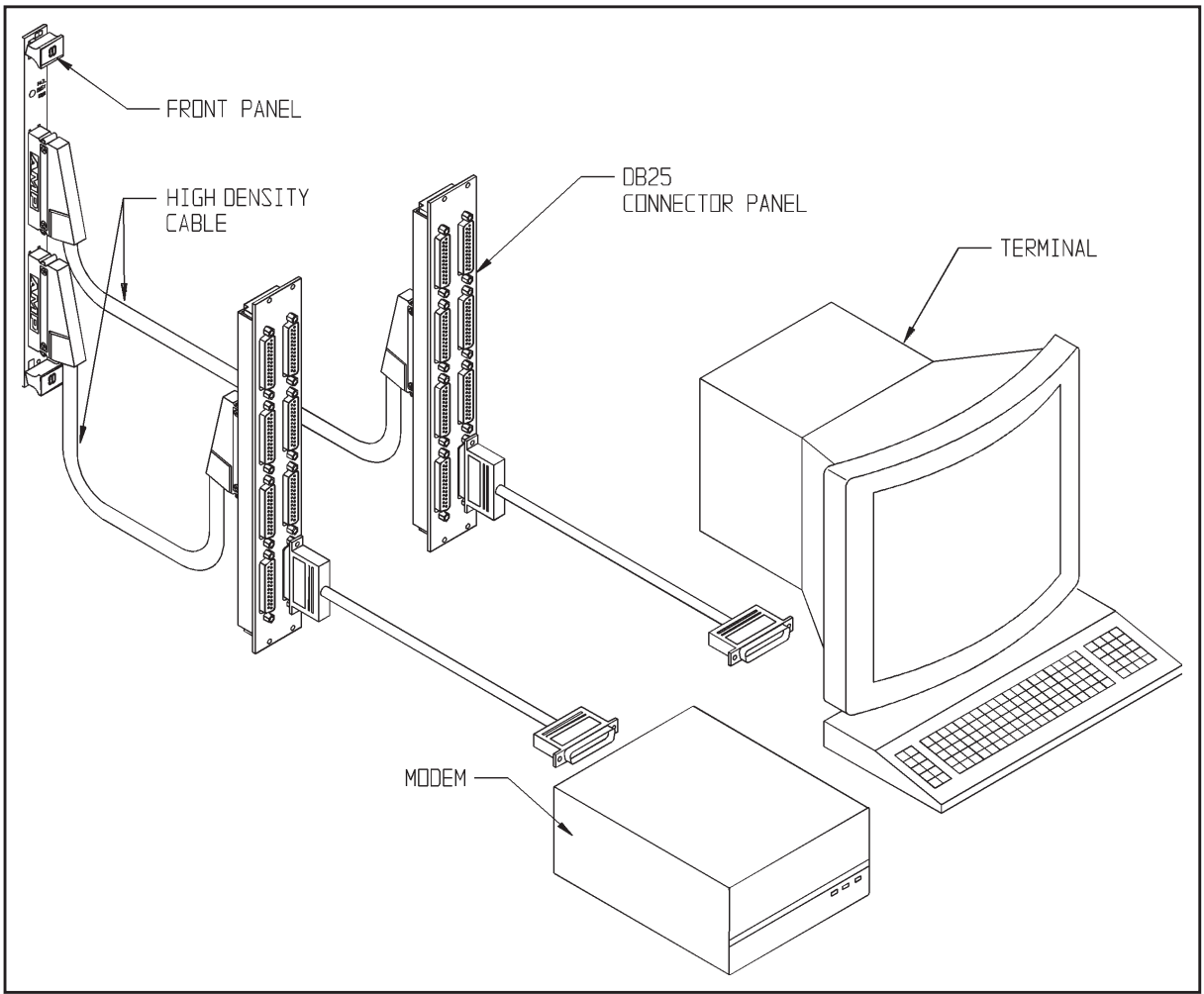


Figure 1-2 – DB25 I/O Panel Connection

I/O through P2 Connector

An adapter panel is available that allows the MVCS serial I/O signals to be routed through the VME P2 connector. The P2 I/O adapter is equipped with two 100-pin high-density connectors similar to those on the front panel. This allows the interface cables to be kept in the rear of the chassis, and is an ideal solution where front panel space is at premium. The P2 I/O adapter is plugged into the P2 connector of the slot in which the MVCS is installed, and the interface cables to the I/O panels are attached to it. The MVCS must be factory configured to support the P2 I/O option.

The serial line conditioners are installed on the P2 I/O interface adapter (factory-built P2-interface versions of the MVCS have no serial line conditioner sockets on the board). The P2 I/O adapter must never be used with an MVCS that has serial line conditioners installed.

Contact Macrolink for more information regarding the P2 I/O adapter.

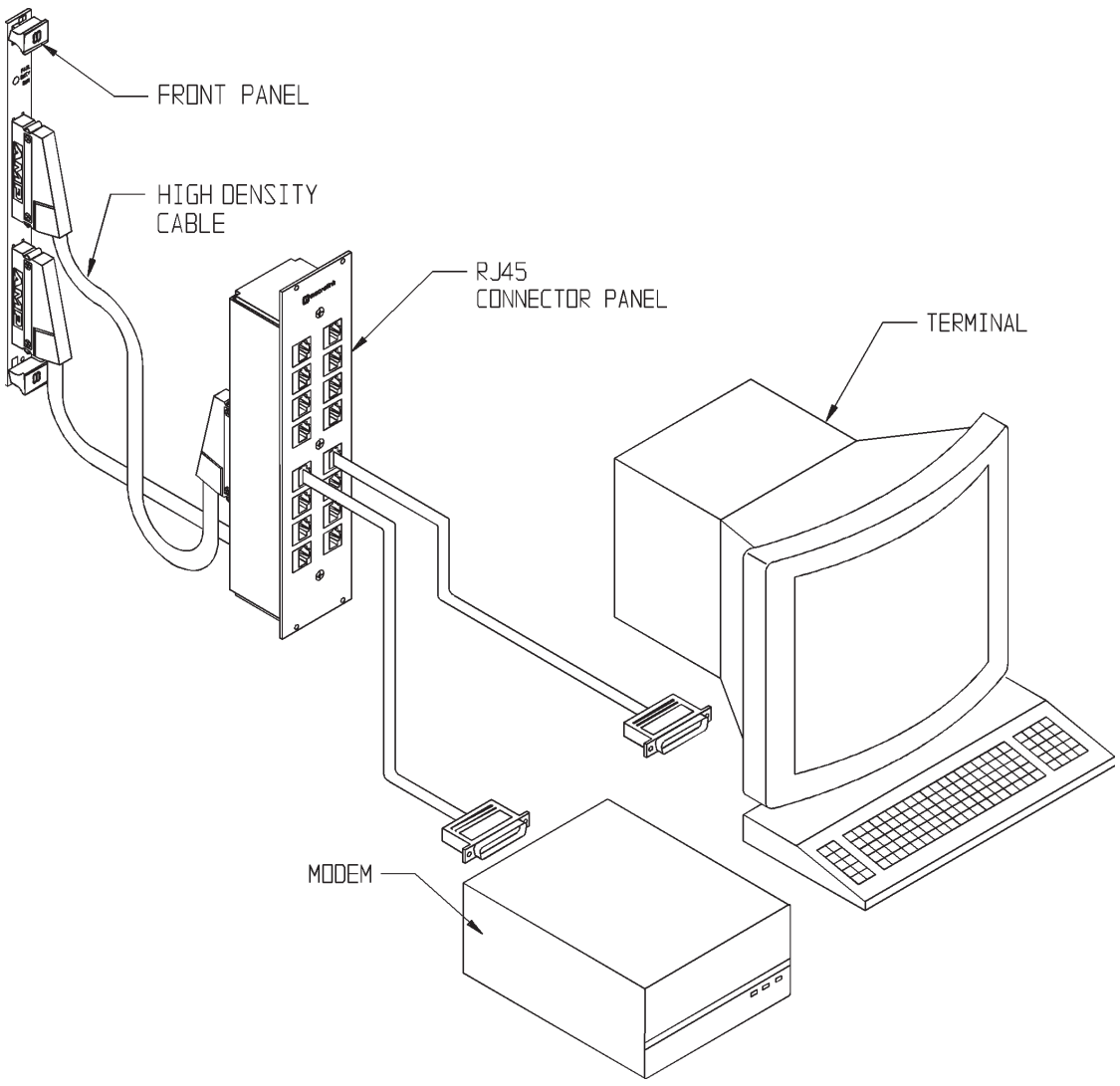


Figure 1-3 – RJ45 I/O Panel Connection

Driver Software

Specific instructions for installing the Macrolink MVCS driver software are contained in README files included in the driver distribution. The driver software is available on several different media types and in a variety of data formats. Contact Macrolink for information on support for your platform.

The MVCS driver distribution contains a hierarchical directory tree of source code files that have been converted to a single file by an archiving tool. Some archive formats also contain command scripts that run automatically when the distribution is installed. In all distribution formats, the README files can be accessed when the source files are loaded, without building the driver.

☞ Please read all of the README files before building the host adapter driver. The README files will contain important installation and configuration information, as well as any changes that have occurred since the release of this manual.

How To Find The README Files

"TAR" format distributions contain pathnames that are relative to the current directory. They can be loaded into any directory. The main README file is found in or near the top level directory. Review any README file in the directory tree. Change directories (cd) to the desired directory for the driver software and extract the product files under that directory by running the following command:

```
tar xvf /dev/rfd0
```

This example assumes that /dev/rfd0 is the device file for the drive that contains the distribution media. Your device file name may vary.

The README filenames may take the form READMExxx or README.xxx, where xxx may refer to a particular function or file included in the distribution. Be sure to read them all, even if you do not think they will apply to your installation.

Solaris 2.x Driver

"PKG" format distributions contain pathnames that are relative to a "base directory" instead of the current directory. To view the README file(s) before installation, transfer the package to the default spool directory for the package (/var/spool/pkg). Run the following command:

```
pkgtrans /dev/rfd0 /var/spool/pkg MLINKmcs
```

This will put the product files under the directory /var/spool/pkg/MLINKmcs. This example assumes that /dev/rfd0 is the device file for the drive that contains the distribution media. Your device file name may vary. Review any README file in the directory tree before installation. Caution: do not modify any configuration file before the product is installed; files under /var/spool/pkg/MLINKmcs must not be modified. The package can be installed with the command:

```
pkgadd MLINKmcs
```

Upon installation, the README file{s) can be found under the base directory, /opt/MLINKmcs. Adding the package does not install the driver in the kernel. First verify the driver configuration. If the MVCS board(s) have been installed at an address other than the configuration defaults, modify the driver configuration file, mcs.conf. The README file describes how to modify the default configuration file and successfully install the driver. To install the driver in the kernel, execute the install script:

```
sh install
```

Solaris 2.x Driver Configuration

The MVCS Solaris driver is configured via property arrays in the file 'mcs.conf'. There are three groups of properties. The first group is used by Solaris to assign host system resources to the MVCS. They are documented in man pages vme(4) and driver.conf(4).

Group 1 Property Definitions		
Property	**Description**	**Default**
name	Unique card type known to driver	No default
class	Parent bus type: VME	No default
reg	VME bus space id and address	No default
interrupts	VME bus interrupt level & vector	No default

Properties in the second group are unique to the MVCS driver and specify configuration information that affects the MVCS as a whole. They describe MVCS hardware configuration and specify a limit to the amount of host interrupt bandwidth the MVCS is allowed to use. These properties are all integer and of the form *Prop_name=single_value*

Group 2 Property Definitions		
Property	**Description**	**Default**
pri_osc_hz	Primary Oscillator Frequency in Hz	44236800
aux_osc_hz	Auxiliary Oscillator Frequency in Hz. To use the auxiliary oscillator for clock rate source, set to 14745600 and move jumper E3 to positions 1&2. This allows support for a baud rate of 307.2 Kbps but limits the maximum baud rate to 921.6 Kbps	0
prescale_by	Oscillator scale factor, 1 or 4	1
intr_pacing	Interrupt Pacing throttle time. See description below.	3
rs485_intr_pacing	Alternate Interrupt Pacing throttle time	2

Interrupt Pacing throttle time specifies the minimum allowed time between consecutive VME interrupt requests from the Sierra card. Pacing is disabled if specified throttle value is zero. For a value of 1, the pacing interval is one tick time, where a single tick time in seconds is 8192 divided by the primary oscillator frequency.(8192/44236800 = 0.000185, or 185 usec). For values 2-7, the pacing interval doubles for each value. For a non-zero throttle value T and tick time C, the interval time isequal to C * $(2^{(T-1)})$

Alternate Interrupt Pacing throttle time is for use with a port configured for RS-485. This interval is used while the port is waiting for the transmitter to drain. It should be set to decrease the normal pacing interval to quickly detect the drained condition and lower RTS to disable the transmitter. It is ignored if no RS-485 ports are configured. Values are the same as intr_pacing.

Properties in the third group are unique to the MVCS driver and specify hardware and driver configuration information that affect individual ports. They describe the hardware interface type of each port and specify driver port configuration values that override the host system defaults. These properties are all integer properties, but accept variable length lists of tuples (sets of elements) in the following form. This example shows two tuples, each of which is three integer elements long, followed by an ellipsis. (...)

```
prop_name=port_mask1,value1A,value1B,port_mask2,index2A,value2B ...
```

where "port_mask" starts each tuple and is an integer value in which each of the low order 16 bits corresponds to a port number. The lowest order bit corresponds to port 0. The number of values that follow the "port_mask" to finish the tuple is unique to each property type and varies from 0 to 2. So, each tuple is one, two, or three integers, de-

pending on which property it is associated with. Additional tuples can be appended as needed to fully specify a property for all ports.

The simplest tuple is used with boolean properties. Only a single "port_mask" element is required to fully specify which ports are to have the property asserted. For example, *soft_carrier=0x00ff* would assert the "soft_carrier" property on ports 0-7. Ports 8-15 would be left in the default negated state.

Some properties require a single value to be associated with each "port_mask." For example, the property *port_modules=0xf00f,1,0x0f00,7* would specify that ports 0-3 and 12-15 have type 1 interfaces (RS-422) and ports 8-11 have type 7 interfaces (2-wire RS-485). Ports 4-7 are not specified and would default to type 0 (RS-232).

Each "new_speed" property tuples contain a port_mask field followed by two integer values. This property overrides baud rates specified by termios CBAUD, CBAUDEXT, CIBAUD, CIBAUDEXT fields. Each tuple of this property specifies one value for the index to be overridden and a second value for the new baud rate. For example, *new_speed=0xff00,10,691000,0xff00,11,1380000* contains two tuples and would change two baud rates on ports 8-15. Baud rate select 10 (B1800) would be changed to set 691 Kbps and baud rate select 11 (B2400) would be changed to set 1.38 Mbps.

Group 3 Property Definitions

Property	Description	Default
port_modules	Interface type for each port. Each list element consists of: port_mask,interface_type. Types are: 0: RS-232, MIL-188C, TTL 1: RS-422 5: RS-485 (4 wire) 7: RS-485 (2 wire)	0 (RS-232)
soft_carrier	DCD assumed ON if mode is asserted. Each list element consists of: port_mask. Soft carrier mode is asserted for each port selected by the port_mask bit pattern.	off
new_speed	List of overrides for baud rates. Each list element consists of: port_mask,index,speed. where index is the termio number that corresponds to the baud rate that is being changed, and speed is the new baud rate in bits/sec.	No default
new_cflag	List of overrides for port setup. Each list element consists of: port_mask,cflag. where cflag is termio cflag value that will replace the system default for the ports selected by the port_mask bits. Overrides cflag field of global ttymodes property from the Solaris options node.	ttymodes

Configuration Examples:

All ports are local RS-232 connections. No modems are involved. The auxiliary oscillator is selected (jumper E3 in position 1&2) for the UART clock source so that the card can support a baud rate of 307.2 Kbps.

```
 name="mcs" class="vme" reg=0x4d,0xd8000000,0x1000 interrupts=4,0xd8
soft_carrier=0xffff aux_osc_hz=14745600
```

Default Device Definitions:

```
name="mcs" class="vme" reg=0x4d,0xd8000000,0x1000 interrupts=3,0xd8
        soft_carrier=0xffff new_speed=0xffff,21,0
;
name="mcs" class="vme" reg=0x4d,0xd9000000,0x1000 interrupts=3,0xd9
        soft_carrier=0xffff new_speed=0xffff,21,0
;
```

The default definitions show that baud rate select 21 (B307200) is not supported with the primary 44.2368 oscillator.

MVCS Performance Features

Interrupt Pacing Engine

The MVCS features an interrupt pacing engine that prevents the VMEbus from getting swamped by interrupts as the UARTs process characters. Interrupt pacing on the MVCS is controlled in part by the UARTs, which have the ability to interrupt on programmable transmit and receive thresholds and after they have reached receive inactivity intervals. There is also a minor trade-off with interrupt latency that is minimized by the receive data timeout in the UART.

The minimum possible interrupt pacing time is a function of the baud rate and the internal UART FIFO depth. This is illustrated as follows:

Minimum Interrupt Pacing Time

FIFO Depth	Baud Rate	Interrupt Rate
32	9600	32 mSec
64	9600	64 mSec
32	38.4K	8 mSec
64	38.4K	16 mSec
32	460K	640 uSec
64	460K	1.2 mSec
32	1.4M	230 uSec
64	1.4M	460 uSec

Thus, if the baud rates are all slow (9600 baud class), then the interval can be set to the maximum value of 11.84 mSec without dropping any characters.

The Interrupt Throttle is set to match the maximum board data rates multiplied by the internal UART FIFO depth in bytes (56 usable typically). It should be set as high as possible factoring in maximum data latency requirements as well. For instance, for an internal UART FIFO depth of 56 bytes, a baud rate of 460 Kbaud yields an interrupt every 1.1 mSec. In that case, setting the interrupt to 740 uS or 1.48 mS should allow the data to be handled without turning handshaking off (note a possible startup condition of one cycle to get aligned, requiring a handshake to not lose data). The interrupt pacing mechanism prevents the CPU from being swamped by the interrupt repetition rate of the card. With the default 44.2368 MHz oscillator, the selectable interrupt pacing values are:

Interrupt Pacing Values

Value	Interrupt Rate
1	185 uSec
2	370 uSec
3	740 uSec
4	1.48 mSec
5	2.96 mSec
6	5.92 mSec
7	11.84 mSec

The interrupt vector is programmed on a per-board basis. There is one interrupt vector per board. The level and vector are both programmable from the host, and are set in a configuration file when the Macrolink driver is utilized. The MVCS can not be used in a multi-host scheme unless one of the hosts is assigned to handle interrupts.

Write Posting

Both versions of the MVCS (Sierra and High Sierra) support write posting which increases the performance of the board. This feature benefits single write operations performed to the MVCS. Writes are acknowledged very quickly to the VMEbus. Subsequent read or write accesses to the MVCS card are held off while the write is still in progress.

High Sierra Version Features

The sections that follow detail key performance benefits of the High Sierra version of the MVCS over the standard (Sierra) version of the board.

D32 Data Path - High Sierra Option

The performance of the MVCS is limited by the ability to move data to and from the UARTs a byte at a time. On the standard version of the MVCS, throughput is limited by the narrowness and the relatively slow speed of the interface to the UARTs.

The High Sierra version of the MVCS adds high-performance FIFO buffers which are size matched to the possibility of all UART channels being filled at once. Without buffering FIFOs, a single MVCS could consume all of the total available backplane bandwidth (16 ports at 1.5 Mb/s (with an optional oscillator), data in both directions, taking 300 ns per transfer is 200% of total VMEbus bandwidth). The High Sierra improves on that by an order of magnitude, allowing the board to be read and written at much faster VMEbus slave access rates. This advantage is best realized when performing D32 burst transfers to or from the MVCS.

While host CPUs with D32 support are not required for this option, they are needed to realize the full potential of the MVCS. It is also beneficial if the VME Bus Master is capable of performing block transfers.

Transmit Buffering FIFO - High Sierra Option

Separate buffering FIFOs are used to for reads and for writes. The Transmit Buffering FIFOs have been selected to provide a depth matching the maximum depth of the internal FIFOs in the UARTs times the maximum number of channels. Thus, 16 channels at 64-bytes per channel of internal UART buffering yields a total of 1 KB of Transmit Buffering FIFO. Writes of data in sizes other than 32-bits are possible, but the total depth of the Buffering FIFO is fixed at 256 entries.

The host uses the status of the internal FIFOs, as reported by the UART interrupt status register, as an indication of how much data a port is able to take. Regardless of whether there are Buffering FIFOs, the host is able to determine how much data that each serial port is ready to take.

Receive Buffering FIFO - High Sierra Option

In the receive data direction, the data is placed into the Receive Buffering FIFOs for presentation to the VMEbus by state machine logic that examines the value of the RXRDY pins for all UART channels. When the pin indicates that there is receive data on the UART channel, the state machine first reads the status from the UART status register for that channel, and then reads the data from that UART channel. The status is placed into a status buffering FIFO and the data is placed into a data buffering FIFO.

The depth of the Receive Buffering FIFO is selected to match the expected aggregate data rates divided by the service rate from the host. The Receive Buffering FIFO has the status and data in one single 16-bit read; a 32-bit read produces two data and two status values. The standard version of the High Sierra card has 512 pairs of status/data entries. With all receive channels running at 1.38 Mbits/sec, this results in receive data interrupts about every 3.7 msec. The Receive Buffering FIFO Depth Counter can be read and the appropriate number of data pairs extracted from the VMEbus.

Interrupt Operation

Interrupts are handled differently on the High Sierra version of the MVCS than on the standard version. Data is sent through the external Transmit Buffering FIFOs and brought in through the Receive Buffering FIFOs in High Sierra mode. In normal mode, the UARTs are directly accessed and there are no Buffering FIFOs.

The operation of MVCS interrupts is summarized as follows:

Direction	Normal Mode	High Sierra Mode
RX	RCVR_HLDG_REG_INT Pull Interrupt Depth from UART Poll receive until empty RX_TIMEOUT Poll receive until empty	RFNEF0, RFNEF1 Read Count Short cleanup, if needed Empty as longs Short Cleanups
TX	XMTR_HLDG_REG_INT Fill internal UART FIFOs	XMTR_HLDG_REG_INT Fill Buffering FIFOs

When in normal operating mode, interrupts are only enabled for receive data level trigger and receive timeout for the UART direct access channels. In High Sierra mode, receive data level trigger and receive timeouts are not enabled since the receive FIFO causes the interrupt..

When in either mode, the TX Triggers are used as flags. In High Sierra mode, the data is written to the Buffering FIFOs. In normal mode, the data is written to the UARTs directly, but in either case, the cause of the interrupt is the same.

In High Sierra mode, only as much data as the UART can accept should be written to the buffering FIFOs. The function of the FIFOs is to match the high speed of the VMEbus to the much lower interface speed of the UARTs. The interrupt from the UART that indicates the Transmit Buffering FIFO threshold has been crossed triggers all write operations.

Front Panel Status Indicator

The MVCS uses a tri-color LED for status indication. The LED is controlled by the application running on the host system, and thus the status indicated by the various color combinations is program-dependent. The operational states indicated by this LED when used with a Macrolink-supplied driver are shown in the table below.

Board Status Indicator	
Status Indication	**Color**
Board has failed driver initiated tests	Red
Board has not been initialized by the driver	Yellow
Board has been initialized	Green

Refer to Figure 1-1 to locate the board status indicator.

Returning Products For Repair

Before returning a product for repair, you must obtain a Return Material Authorization (RMA) number from Macrolink. This number must appear on the outside of the shipping container. Products returned without an RMA number will be refused. When requesting an RMA number, please be prepared to provide the following information:

- Product name or part number.
- Serial number.
- Failure description. An inspection fee may be assessed on items returned without an adequate failure description.

Shipping expenses to Macrolink are to be paid by the customer. Macrolink will pay for standard return shipping for products under warranty.

FCC Compliance

This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with this manual, may cause interference to radio and television reception. This equipment has been tested and found to comply with the limits for a Class A computing device in accordance with the specifications in Subpart J of Part 15 of the FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference requiring the user, at the user's own expense, to take whatever measures may be necessary to correct the interference.

If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference in one or more of the following ways:

1. Reorient the receiving antenna.
2. Relocate the computer with respect to the receiver.
3. Move the computer away from the receiver.
4. Plug the computer into a different outlet, so that the computer and receiver are on different circuit branches.
5. Ensure that the mounting screws, attachment connector screws, and grounding connections are securely tightened.
6. Ensure that good quality, shielded and grounded cables are used for data communications.

If necessary, the user should consult the dealer or an experienced radio/television technician for additional suggestions. The user may find the booklet *How To Identify And Resolve Radio-TV Interference Problems* prepared by the Federal Communications Commission helpful. This booklet is available from the U.S. Government Printing Office, Washington, D.C. 20420, Stock No. 004-000-0345-4.

Technical Information

This appendix provides signal name and pinout information for the interface connectors used on the MVCS, information regarding Macrolink's implementation of the RS485 interface, and loopback connector pinouts.

DB25 Interface Panel Signals

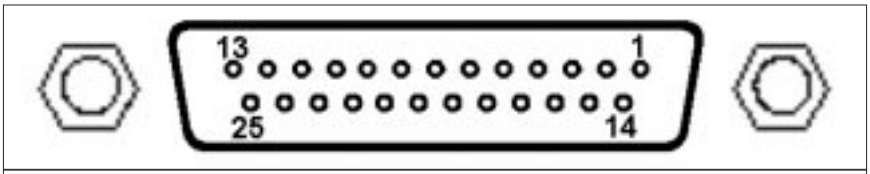
The interface panels used with the MVCS are also used with other members of Macrolink's family of synchronous commuxes. For use with the MVCS, the configuration jumpers inside the interface panel must be set to the RI/DCD position, which is the factory default. Do not set the jumpers to the TXCLK/RXCLK position. Refer to the documentation provided with the interface panel for more information.

The sections that follow define the pin designations for the DB-25 connectors for the various line disciplines. A pin number identification reference drawing is shown below. The DB-25 panel uses standard pitch female gender connectors.

RS232/MIL188C Signals

RS232/MIL188C DB25 Signals

Signal	Pin	Description
CGND	1	Protective Ground
TXD	2	Transmit Data
RXD	3	Receive Data
RTS	4	Request to Send
CTS	5	Clear to Send
DSR	6	Data Set Ready
SGND	7	Signal Ground
DCD	8	Data Carrier Detect
DTR	20	Data Terminal Ready
RI	22	Ring Indicate



DB-25F Connector Pinout - I/O panel front view

RS422/485 Signals

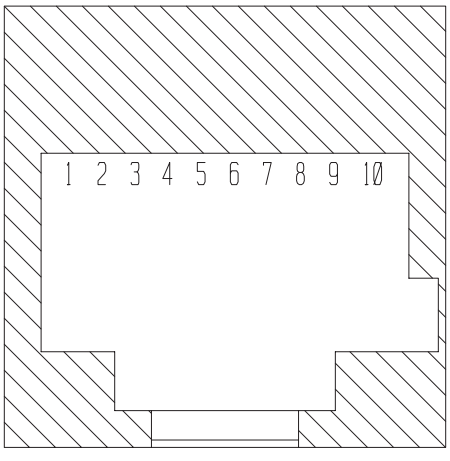
RS422/485 DB25 Signals		
Signal	**Pin**	**Description**
CGND	1	Protective Ground
TXDA	2	Transmit Data A
RXDA	3	Receive Data A
RTSA	4	Request to Send A
CTSA	5	Clear to Send A
SGND	7	Signal Ground
CTSB	13	Clear to Send B
TXDB	14	Transmit Data B
RXDB	16	Receive Data B
RTSB	19	Request to Send B

Note: Request To Send and Clear To Send are not provided as outputs on the RS485 modules.

RJ45 Interface Panel Signals

The interface panels used with the MVCS are also used with other members of Macrolink's family of synchronous commuxes. For use with the MVCS, the configuration jumpers inside the interface panel must be set to the RI/DCD position, which is the factory default. Do not set the jumpers to the TXCLK/RXCLK position. Refer to the documentation provided with the interface panel for more information.

The sections that follow define the pin designations for the RJ-45 connectors for the various line disciplines. Mating 10-pin connectors are Stewart Connector Systems part number 937-SP-301010 or equivalent. A pin number identification reference drawing is shown below.



RJ45 Connector Pinout - I/O panel front view

RS232/MIL188C Signals

RS232/MIL188C RJ45 Signals		
Signal	**Pin**	**Description**
RI	1	Ring Indicate
DSR	2	Data Set Ready
RTS	3	Request to Send
CGND	4	Protective Ground
TXD	5	Transmit Data
RXD	6	Receive Data
SGND	7	Signal Ground
CTS	8	Clear to Send
DTR	9	Data Terminal Ready
DCD	10	Data Carrier Detect

RS422/485 Signals

RS422/485 RJ45 Signals		
Signal	**Pin**	**Description**
CTSB	1	Clear to Send B
RXDB	2	Receive Data B
RTSA	3	Request to Send A
CGND	4	Protective Ground
TXDA	5	Transmit Data A
RXDA	6	Receive Data A
SGND	7	Signal Ground
CTSA	8	Clear to Send A
TXDB	9	Transmit Data B
RTSB	10	Request to Send B

Note: Request To Send and Clear To Send are not provided as outputs on the RS485 modules.

MVCS RS485 Interface

The RS-485 standard specifies the electrical characteristics of drivers and receivers that can be used to implement a balanced multi-point line, also known as a "party line." The devices attached to this line will support 32 driver/receiver connect points. The transmission line used is 120 Ohm twisted pair terminated at both ends with a 120 Ohm resistor. A line length of 50 meters can be supported with this interface. When a driver is not actively driving the line it will be taken to a high impedance condition.

There is no implied protocol supported by RS-485 nor is there any hardware flow control. RS-485 as implemented by Macrolink does not have any collision recovery. It is intended to be used in a system employing one "talker or initiator" and multiple "listeners or targets." The jumpers on the I/O transition panel must be strapped to the RS-422 setting.

The MVCS supports 2-wire or 4-wire RS485 configurations.

2-Wire

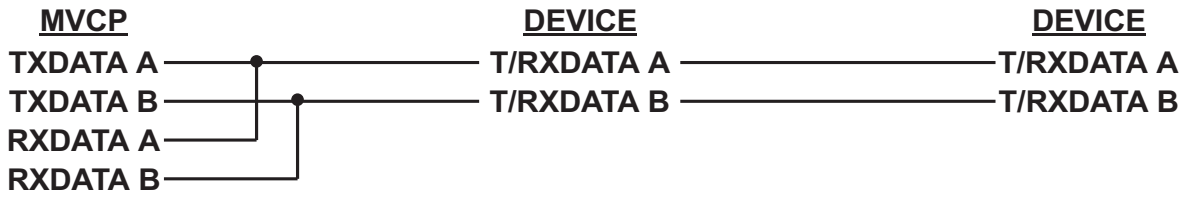
The 2-wire configuration transmits and receives data on the same pair of wires in a half duplex operation. A device that wants to transmit data must wait until the line is available before its data can be sent. The transmit and receive data signals are connected together to operate in 2-wire mode; TXDATA A is wired to RXDATA A and TXDATA B is wired to RXDATA B.

The receiver can be turned off under software control to keep from receiving the transmitted data. The RTS signal is used to tri-state the transmit data and clock drivers when they are idle. This function must be performed by the application.

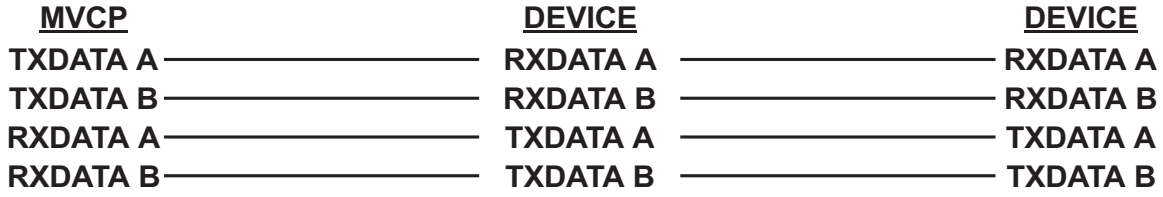
4-Wire

In 4-wire mode the data is transmitted on 1 pair of wires and received on another pair in a full duplex operation. The master device sends data down 1 pair of wires to slave devices (TXDATA A and B). Slave devices send data to the master device on the other pair of wires (RXDATA A and B).

RS485 2-WIRE INTERFACE



RS485 4-WIRE INTERFACE

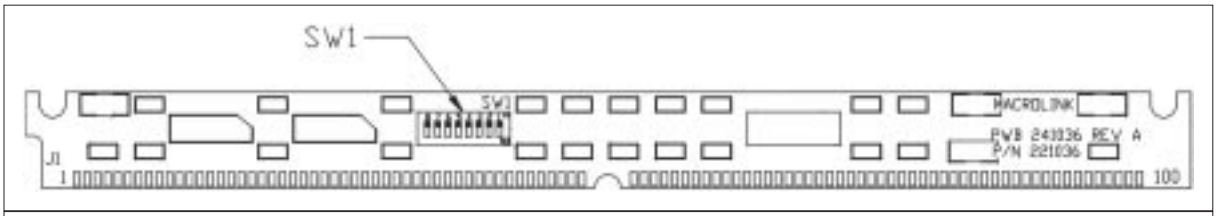


RS485 Termination

Termination is provided for the data lines. The RS485 bus must be terminated at both ends, but termination must be disabled on all other nodes. Switches are provided for each port on the RS485 modules for this purpose. In 2-wire mode, only one termination switch should be ON for each transmit/receive data pair.

RS485 Serial Line Conditioner Signal Termination Switches

Signal	Switch	Description	Ports
TXDATA	SW1-1	Transmit Data	0,4,8,C
RXDATA	SW1-2	Receive Data	0,4,8,C
TXDATA	SW1-3	Transmit Data	1,5,9,D
RXDATA	SW1-4	Receive Data	1,5,9,D
TXDATA	SW1-5	Transmit Data	2,6,A,E
RXDATA	SW1-6	Receive Data	2,6,A,E
TXDATA	SW1-7	Transmit Data	3,7,B,F
RXDATA	SW1-8	Receive Data	3,7,B,F



RS485 Serial Line Conditioner Switch Location

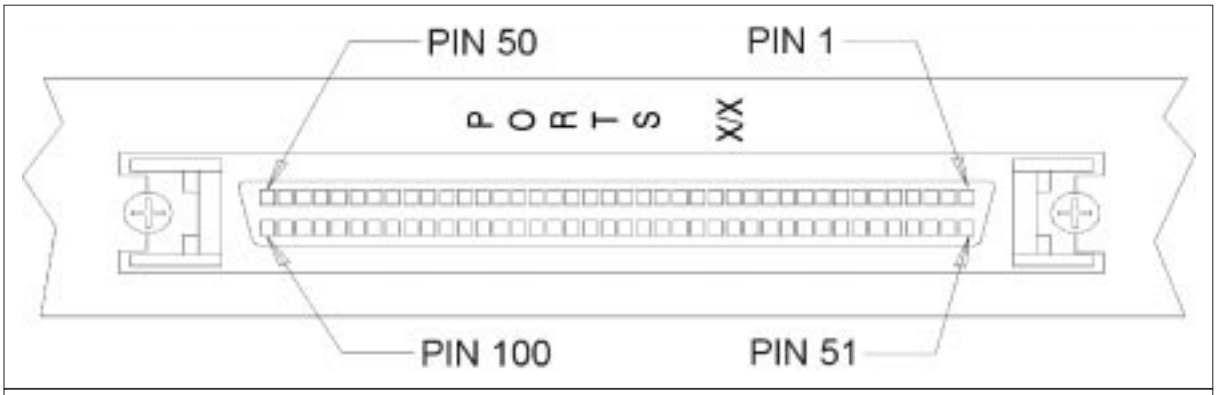
Front Panel I/O Connectors

The MVCS uses 100 pin high-density connectors for the serial interface. The mating connector is AMP catalog number 749621-9. The recommended backshells are AMP catalog number 749206-1 (right angle) or 749197-1 (straight).

The lower connector on the front of the MVCS (J1) interfaces to ports 0 through 7. The upper connector (J6) interfaces to ports 8 through F.

The table on the next two pages contains the pinout of the front panel connectors. A pin number reference drawing is shown below. Pins designated in the table as No Connect are reserved. Make no external connection to these pins.

Note: Request To Send and Clear To Send are not provided as outputs on the RS485 modules.



High-Density 100 Pin Connector, as viewed from the front panel

	RS232/MIL188C Interface		RS422/485 Interface	
J1, J6 Pin	Signal	Description	Signal	Description
1	TXD0/8	Transmit Data Port 0/8	TXDA0/8	Transmit Data A Port 0/8
2	DTR0/8	Data Terminal Ready Port 0/8	TXDB0/8	Transmit Data B Port 0/8
3	RXD0/8	Receive Data Port 0/8	RXDA0/8	Receive Data A Port 0/8
4	DSR0/8	Data Set Ready Port 0/8	RXDB0/8	Receive Data B Port 0/8
5	N/C	No Connection	N/C	No Connection
6	N/C	No Connection	N/C	No Connection
7	N/C	No Connection	N/C	No Connection
8	N/C	No Connection	N/C	No Connection
9	RTS0/8	Request to Send Port 0/8	RTSA0/8	Request to Send A Port 0/8
10	CD0/8	Carrier Detect Port 0/8	RTSB0/8	Request to Send B Port 0/8
11	CTS0/8	Clear to Send Port 0/8	CTSA0/8	Clear to Send A Port 0/8
12	RING0/8	Ring Indicate Port 0/8	CTSB0/8	Clear to Send B Port 0/8
13	TXD1/9	Transmit Data Port 1/9	TXDA1/9	Transmit Data A Port 1/9
14	DTR1/9	Data Terminal Ready Port 1/9	TXDB1/9	Transmit Data B Port 1/9
15	RXD1/9	Receive Data Port 1/9	RXDA1/9	Receive Data A Port 1/9
16	DSR1/9	Data Set Ready Port 1/9	RXDB1/9	Receive Data B Port 1/9
17	N/C	No Connection	N/C	No Connection
18	N/C	No Connection	N/C	No Connection
19	N/C	No Connection	N/C	No Connection
20	N/C	No Connection	N/C	No Connection
21	RTS1/9	Request to Send Port 1/9	RTSA1/9	Request to Send A Port 1/9
22	CD1/9	Carrier Detect Port 1/9	RTSB1/9	Request to Send B Port 1/9
23	CTS1/9	Clear to Send Port 1/9	CTSA1/9	Clear to Send A Port 1/9
24	RING1/9	Ring Indicate Port 1/9	CTSB1/9	Clear to Send B Port 1/9
25	GND	Signal Ground	GND	Signal Ground
26	GND	Signal Ground	GND	Signal Ground
27	TXD2/A	Transmit Data Port 2/A	TXDA2/A	Transmit Data A Port 2/A
28	DTR2/A	Data Terminal Ready Port 2/A	TXDB2/A	Transmit Data B Port 2/A
29	RXD2/A	Receive Data Port 2/A	RXDA2/A	Receive Data A Port 2/A
30	DSR2/A	Data Set Ready Port 2/A	RXDB2/A	Receive Data B Port 2/A
31	N/C	No Connection	N/C	No Connection
32	N/C	No Connection	N/C	No Connection
33	N/C	No Connection	N/C	No Connection
34	N/C	No Connection	N/C	No Connection
35	RTS2/A	Request to Send Port 2/A	RTSA2/A	Request to Send A Port 2/A
36	CD2/A	Carrier Detect Port 2/A	RTSB2/A	Request to Send B Port 2/A
37	CTS2/A	Clear to Send Port 2/A	CTSA2/A	Clear to Send A Port 2/A
38	RING2/A	Ring Indicate Port 2/A	CTSB2/A	Clear to Send B Port 2/A
39	TXD3/B	Transmit Data Port 3/B	TXDA3/B	Transmit Data A Port 3/B
40	DTR3/B	Data Terminal Ready Port 3/B	TXDB3/B	Transmit Data B Port 3/B
41	RXD3/B	Receive Data Port 3/B	RXDA3/B	Receive Data A Port 3/B
42	DSR3/B	Data Set Ready Port 3/B	RXDB3/B	Receive Data B Port 3/B
43	N/C	No Connection	N/C	No Connection
44	N/C	No Connection	N/C	No Connection
45	N/C	No Connection	N/C	No Connection
46	N/C	No Connection	N/C	No Connection
47	RTS3/B	Request to Send Port 3/B	RTSA3/B	Request to Send A Port 3/B
48	CD3/B	Carrier Detect Port 3/B	RTSB3/B	Request to Send B Port 3/B
49	CTS3/B	Clear to Send Port 3/B	CTSA3/B	Clear to Send A Port 3/B
50	RING3/B	Ring Indicate Port 3/B	CTSB3/B	Clear to Send B Port 3/B

	RS232/MIL188C Interface		RS422/485 Interface	
J1, J6 Pin	Signal	Description	Signal	Description
51	TXD4/C	Transmit Data Port 4/C	TXDA4/C	Transmit Data A Port 4/C
52	DTR4/C	Data Terminal Ready Port 4/C	TXDB4/C	Transmit Data B Port 4/C
53	RXD4/C	Receive Data Port 4/C	RXDA4/C	Receive Data A Port 4/C
54	DSR4/C	Data Set Ready Port 4/C	RXDB4/C	Receive Data B Port 4/C
55	N/C	No Connection	N/C	No Connection
56	N/C	No Connection	N/C	No Connection
57	N/C	No Connection	N/C	No Connection
58	N/C	No Connection	N/C	No Connection
59	RTS4/C	Request to Send Port 4/C	RTSA4/C	Request to Send A Port 4/C
60	CD4/C	Carrier Detect Port 4/C	RTSB4/C	Request to Send B Port 4/C
61	CTS4/C	Clear to Send Port 4/C	CTSA4/C	Clear to Send A Port 4/C
62	RING4/C	Ring Indicate Port 4/C	CTSB4/C	Clear to Send B Port 4/C
63	TXD5/D	Transmit Data Port 5/D	TXDA5/D	Transmit Data A Port 5/D
64	DTR5/D	Data Terminal Ready Port 5/D	TXDB5/D	Transmit Data B Port 5/D
65	RXD5/D	Receive Data Port 5/D	RXDA5/D	Receive Data A Port 5/D
66	DSR5/D	Data Set Ready Port 5/D	RXDB5/D	Receive Data B Port 5/D
67	N/C	No Connection	N/C	No Connection
68	N/C	No Connection	N/C	No Connection
69	N/C	No Connection	N/C	No Connection
70	N/C	No Connection	N/C	No Connection
71	RTS5/D	Request to Send Port 5/D	RTSA5/D	Request to Send A Port 5/D
72	CD5/D	Carrier Detect Port 5/D	RTSB5/D	Request to Send B Port 5/D
73	CTS5/D	Clear to Send Port 5/D	CTSA5/D	Clear to Send A Port 5/D
74	RING5/D	Ring Indicate Port 5/D	CTSB5/D	Clear to Send B Port 5/D
75	GND	Signal Ground	GND	Signal Ground
76	GND	Signal Ground	GND	Signal Ground
77	TXD6/E	Transmit Data Port 6/E	TXDA6/E	Transmit Data A Port 6/E
78	DTR6/E	Data Terminal Ready Port 6/E	TXDB6/E	Transmit Data B Port 6/E
79	RXD6/E	Receive Data Port 6/E	RXDA6/E	Receive Data A Port 6/E
80	DSR6/E	Data Set Ready Port 6/E	RXDB6/E	Receive Data B Port 6/E
81	N/C	No Connection	N/C	No Connection
82	N/C	No Connection	N/C	No Connection
83	N/C	No Connection	N/C	No Connection
84	N/C	No Connection	N/C	No Connection
85	RTS6/E	Request to Send Port 6/E	RTSA6/E	Request to Send A Port 6/E
86	CD6/E	Carrier Detect Port 6/E	RTSB6/E	Request to Send B Port 6/E
87	CTS6/E	Clear to Send Port 6/E	CTSA6/E	Clear to Send A Port 6/E
88	RING6/E	Ring Indicate Port 6/E	CTSB6/E	Clear to Send B Port 6/E
89	TXD7/F	Transmit Data Port 7/F	TXDA7/F	Transmit Data A Port 7/F
90	DTR7/F	Data Terminal Ready Port 7/F	TXDB7/F	Transmit Data B Port 7/F
91	RXD7/F	Receive Data Port 7/F	RXDA7/F	Receive Data A Port 7/F
92	DSR7/F	Data Set Ready Port 7/F	RXDB7/F	Receive Data B Port 7/F
93	N/C	No Connection	N/C	No Connection
94	N/C	No Connection	N/C	No Connection
95	N/C	No Connection	N/C	No Connection
96	N/C	No Connection	N/C	No Connection
97	RTS7/F	Request to Send Port 7/F	RTSA7/F	Request to Send A Port 7/F
98	CD7/F	Carrier Detect Port 7/F	RTSB7/F	Request to Send B Port 7/F
99	CTS7/F	Clear to Send Port 7/F	CTSA7/F	Clear to Send A Port 7/F
100	RING7/F	Ring Indicate Port 7/F	CTSB7/F	Clear to Send B Port 7/F

VMEbus Interface Signals

VMEbus Interface Signals		
Signal	**Pin**	**Description**
A01	P1A-30	Address Bus
A02	P1A-29	Address Bus
A03	P1A-28	Address Bus
A04	P1A-27	Address Bus
A05	P1A-26	Address Bus
A06	P1A-25	Address Bus
A07	P1A-24	Address Bus
A08	P1C-30	Address Bus
A09	P1C-29	Address Bus
A10	P1C-28	Address Bus
A11	P1C-27	Address Bus
A12	P1C-26	Address Bus
A13	P1C-25	Address Bus
A14	P1C-24	Address Bus
A15	P1C-23	Address Bus
A16	P1C-22	Address Bus
A17	P1C-21	Address Bus
A18	P1C-20	Address Bus
A19	P1C-19	Address Bus
A20	P1C-18	Address Bus
A21	P1C-17	Address Bus
A22	P1C-16	Address Bus
A23	P1C-15	Address Bus
A24	P2B-4	Address Bus
A25	P2B-5	Address Bus
A26	P2B-6	Address Bus
A27	P2B-7	Address Bus
A28	P2B-8	Address Bus
A29	P2B-9	Address Bus
A30	P2B-10	Address Bus
A31	P2B-11	Address Bus
D00	P1A-1	Data Bus
D01	P1A-2	Data Bus
D02	P1A-3	Data Bus
D03	P1A-4	Data Bus
D04	P1A-5	Data Bus
D05	P1A-6	Data Bus
D06	P1A-7	Data Bus
D07	P1A-8	Data Bus
D08	P1C-1	Data Bus

VMEbus Interface Signals		
Signal	**Pin**	**Description**
D09	P1C-2	Data Bus
D10	P1C-3	Data Bus
D11	P1C-4	Data Bus
D12	P1C-5	Data Bus
D13	P1C-6	Data Bus
D14	P1C-7	Data Bus
D15	P1C-8	Data Bus
D16	P2B-14	Data Bus
D17	P2B-15	Data Bus
D18	P2B-16	Data Bus
D19	P2B-17	Data Bus
D20	P2B-18	Data Bus
D21	P2B-19	Data Bus
D22	P2B-20	Data Bus
D23	P2B-21	Data Bus
D24	P2B-23	Data Bus
D25	P2B-24	Data Bus
D26	P2B-25	Data Bus
D27	P2B-26	Data Bus
D28	P2B-27	Data Bus
D29	P2B-28	Data Bus
D30	P2B-29	Data Bus
D31	P2B-30	Data Bus
Strobes, Active Low (*=0)		
AS*	P1A-18	Address Strobe
DS0*	P1A-13	Data Strobe Zero
DS1*	P1A-12	Data Strobe One
DTACK*	P1A-16	Data Transfer Acknowledge
Master Mode Signals, Active Low		
BBSY*	P1B-1	Bus Busy
BCLR*	P1B-2	Bus Clear
BERR*	P1C-11	Bus Error
BG0IN*	P1B-4	Bus Grant In Zero
BG1IN*	P1B-6	Bus Grant In One
BG2IN*	P1B-8	Bus Grant In Two
BG3IN*	P1B-10	Bus Grant In Three
BG0OUT*	P1B-5	Bus Grant Out Zero
BG1OUT*	P1B-7	Bus Grant Out One
BG2OUT*	P1B-9	Bus Grant Out Two
BG3OUT*	P1B-11	Bus Grant Out Three
BR0*	P1B-12	Bus Request Zero
BR1*	P1B-13	Bus Request One

VMEbus Interface Signals

Signal	Pin	Description
BR2*	P1B-14	Bus Request Two
BR3*	P1B-15	Bus Request Three
Interrupt Lines, Active Low		
IRQ1*	P1B-30	Interrupt Request One
IRQ2*	P1B-29	Interrupt Request Two
IRQ3*	P1B-28	Interrupt Request Three
IRQ4*	P1B-27	Interrupt Request Four
IRQ5*	P1B-26	Interrupt Request Five
IRQ6*	P1B-25	Interrupt Request Six
IRQ7*	P1B-24	Interrupt Request Seven
IACK*	P1A-20	Interrupt Acknowledge
IACKIN*	P1A-21	Interrupt Acknowledge In
IACKOUT*	P1A-22	Interrupt Acknowledge Out
Miscellaneous Signals, Active Low		
LWORD*	P1C-13	Longword, 32 Bit Transfer
WRITE*	P1A-14	Write
SYSRESET*	P1C-12	System Reset
Power		
+5V	P1A,B,C-32	Plus Five Volts DC
+5V	P2B-1,13,32	Plus Five Volts DC
GND	P1A-9,11,15	Signal Ground
GND	P1A-17,19	Signal Ground
GND	P1B-20,23	Signal Ground
GND	P2B-2,12,22,31	Signal Ground
GND	P1C-9	Signal Ground

P2 I/O Interface Signals

This section defines the signals available when the MVCS has been factory-configured for serial interface via the VME P2 connector. The P2 I/O Adapter supports the Transmit and Receive Data, Request To Send, Clear To Send, Data Terminal Ready, and Carrier Detect signals. The P2 I/O Adapter requires a backplane with five-row compatible connectors.

The P2 I/O Adapter is plugged into the P2 connector of the slot in which the MVCS is installed, and the interface cables to the I/O panels are attached to it. Complete installation instructions appear in the manual provided with the P2 I/O Adapter.

WARNING!

- ☞ The P2 I/O adapter can not be used with the front panel I/O version of the MVCS.
- ☞ The P2 I/O adapter must never be installed on a backplane slot containing any board other than a properly-configured MVCS. Serious damage to the board, the P2 I/O adapter, or both may result.

The following signals are provided on the P2 I/O Adapter:

P2 I/O Interface Signals

Signal	Pin	Description	Signal	Pin	Description
TXD0	A1	Channel 0 Transmit Data	RTS0	C1	Channel 0 Request To Send
RXD0	A2	Channel 0 Receive Data	CTS0	C2	Channel 0 Clear To Send
TXD1	A3	Channel 1 Transmit Data	RTS1	C3	Channel 1 Request To Send
RXD1	A4	Channel 1 Receive Data	CTS1	C4	Channel 1 Clear To Send
TXD2	A5	Channel 2 Transmit Data	RTS2	C5	Channel 2 Request To Send
RXD2	A6	Channel 2 Receive Data	CTS2	C6	Channel 2 Clear To Send
TXD3	A7	Channel 3 Transmit Data	RTS3	C7	Channel 3 Request To Send
RXD3	A8	Channel 3 Receive Data	CTS3	C8	Channel 3 Clear To Send
TXD4	A9	Channel 4 Transmit Data	RTS4	C9	Channel 4 Request To Send
RXD4	A10	Channel 4 Receive Data	CTS4	C10	Channel 4 Clear To Send
TXD5	A11	Channel 5 Transmit Data	RTS5	C11	Channel 5 Request To Send
RXD5	A12	Channel 5 Receive Data	CTS5	C12	Channel 5 Clear To Send
TXD6	A13	Channel 6 Transmit Data	RTS6	C13	Channel 6 Request To Send
RXD6	A14	Channel 6 Receive Data	CTS6	C14	Channel 6 Clear To Send
TXD7	A15	Channel 7 Transmit Data	RTS7	C15	Channel 7 Request To Send
RXD7	A16	Channel 7 Receive Data	CTS7	C16	Channel 7 Clear To Send
TXD8	A17	Channel 8 Transmit Data	RTS8	C17	Channel 8 Request To Send
RXD8	A18	Channel 8 Receive Data	CTS8	C18	Channel 8 Clear To Send
TXD9	A19	Channel 9 Transmit Data	RTS9	C19	Channel 9 Request To Send
RXD9	A 20	Channel 9 Receive Data	CTS9	C20	Channel 9 Clear To Send
TXD10	A 21	Channel 10 Transmit Data	RTS10	C21	Channel 10 Request To Send
RXD10	A 22	Channel 10 Receive Data	CTS10	C22	Channel 10 Clear To Send
TXD11	A 23	Channel 11 Transmit Data	RTS11	C23	Channel 11 Request To Send
RXD11	A 24	Channel 11 Receive Data	CTS11	C24	Channel 11 Clear To Send
TXD12	A 25	Channel 12 Transmit Data	RTS12	C25	Channel 12 Request To Send
RXD12	A 26	Channel 12 Receive Data	CTS12	C26	Channel 12 Clear To Send
TXD13	A 27	Channel 13 Transmit Data	RTS13	C27	Channel 13 Request To Send

P2 I/O Interface Signals

Signal	Pin	Description	Signal	Pin	Description
RXD13	A 28	Channel 13 Receive Data	CTS13	C28	Channel 13 Clear To Send
TXD14	A 29	Channel 14 Transmit Data	RTS14	C29	Channel 14 Request To Send
RXD14	A 30	Channel 14 Receive Data	CTS14	C30	Channel 14 Clear To Send
TXD15	A 31	Channel 15 Transmit Data	RTS15	C31	Channel 15 Request To Send
RXD15	A 32	Channel 15 Receive Data	CTS15	C32	Channel 15 Clear To Send
DTR0	Z1	Channel 0 Data Terminal Ready	N/C	D1	No Connect
RSV	Z2	Reserved	N/C	D2	No Connect
DTR1	Z3	Channel 1 Data Terminal Ready	CD1	D3	Channel 1 Carrier Detect
RSV	Z4	Reserved	CD0	D4	Channel 0 Carrier Detect
DTR2	Z5	Channel 2 Data Terminal Ready	N/C	D5	Channel 0 Carrier Detect
RSV	Z6	Reserved	CD2	D6	Channel 2 Carrier Detect
DTR3	Z7	Channel 3 Data Terminal Ready	N/C	D7	No Connect
RSV	Z8	Reserved	CD3	D8	Channel 3 Carrier Detect
DTR4	Z9	Channel 4 Data Terminal Ready	N/C	D9	No Connect
RSV	Z10	Reserved	CD4	D10	Channel 4 Carrier Detect
DTR5	Z11	Channel 5 Data Terminal Ready	N/C	D11	No Connect
RSV	Z12	Reserved	CD5	D12	Channel 5 Carrier Detect
DTR6	Z13	Channel 6 Data Terminal Ready	N/C	D13	No Connect
RSV	Z14	Reserved	CD6	D14	Channel 6 Carrier Detect
DTR7	Z15	Channel 7 Data Terminal Ready	N/C	D15	No Connect
RSV	Z16	Reserved	CD7	D16	Channel 7 Carrier Detect
DTR8	Z17	Channel 8 Data Terminal Ready	N/C	D17	No Connect
RSV	Z18	Reserved	CD8	D18	Channel 8 Carrier Detect
DTR9	Z19	Channel 9 Data Terminal Ready	N/C	D19	No Connect
RSV	Z20	Reserved	CD9	D20	Channel 9 Carrier Detect
DTR10	Z21	Channel 10 Data Terminal Ready	N/C	D21	No Connect
RSV	Z22	Reserved	CD10	D22	Channel 10 Carrier Detect
DTR11	Z23	Channel 11 Data Terminal Ready	N/C	D23	No Connect
RSV	Z24	Reserved	CD11	D24	Channel 11 Carrier Detect
DTR12	Z25	Channel 12 Data Terminal Ready	N/C	D25	No Connect
RSV	Z26	Reserved	CD12	D26	Channel 12 Carrier Detect
DTR13	Z27	Channel 13 Data Terminal Ready	N/C	D27	No Connect
RSV	Z28	Reserved	CD13	D28	Channel 13 Carrier Detect
DTR14	Z29	Channel 14 Data Terminal Ready	N/C	D29	No Connect
RSV	Z30	Reserved	CD14	D30	Channel 14 Carrier Detect
DTR15	Z31	Channel 15 Data Terminal Ready	N/C	D31	No Connect
RSV	Z32	Reserved	CD15	D32	Channel 15 Carrier Detect

Loopback Connectors

If you wish to write a loopback test to run on the MVCS, you will need loopback connectors. The information in this section is a suggested pinout for those who wish to fabricate their own. The signals can connect to each local port, for example, TXD for port 0 connects to RXD for port 0, or adjacent port numbers (0 to 1, 2 to 3, etc.) can be tested.

RS-232C Loopback Connections

RS-232C Loopback Connections	
Signal	**Connects To**
TXD	RXD
RTS	CTS and RING
DTR	DSR and CD

RS-422 and IEEE-188C Loopback Connections

RS-422/IEEE-188C Loopback Connections	
Signal	**Connects To**
TXD	RXD
RTS	CTS

RS-485 Loopback Connections

RS-485 Loopback Connections	
Signal	**Connects To**
TXD	RXD

Specifications

Specifications	
VMEbus	
Compliance	Compliant with the VMEbus revision C.1 specification IEC 821 & IEEE P1014/01.2
Slave Data Transfer	A32/A24 — D32/D16/D08/D32BLT Standard Supervisory (3C, 3D, 3E, 3F) Extended Supervisory (0C, 0D, 0E, 0F) Standard non-privileged (38, 39, 3A, 3B) Extended non-privileged (08, 09, 0A, 0B) Slave Write Posting supported
Interrupt Request	IRQ1 through IRQ7. Programmable selection of all lines. Programmable Pacing Interval timing from 185 uS to 11.84 ms.
Transfer Rate	D32 mode: DMA burst: >30MB/s (with external FIFOs option) Sustained: 4.8MB/s (line speed dependent; 16 ports x 1.5Mbps x 2 = 4.8MB/s)
Address Pipelining	VMEbus address pipelining support standard
Serial Interface	
Signal Support	8 ports per connector, 10 signals per port — TXD, DTR, RXD, DSR, Spare, CGND, RTS, CD, CTS, RI
P2 Serial Interface	A version of the MVCS is available that provides the serial interface connections through unused pins on rows A & C of the P2 connector. Signal support is provided for TXD, RXD, RTS, and CTS with three-row connector. DCD and DTR are added when using five-row 160 pin DIN connectors.
Electrical Interfaces	Up to 4 electrical interfaces per card in 4 port groups; RS-232, RS-422, RS-485, MIL-STD-188C & TTL *(other interfaces available; contact factory)*
Line Programming	Independently programmable on a port-by-port basis Port-by-port hardware/software flow control
Data Rates	Asynchronous: Up to 1.5Mbps with an optional 48 MHz oscillator
Serial Controllers	Exar ST16C654 Quad UARTs
General	
Dimensions	6U Dual-height Eurocard (160mm x 233mm). Front Panel: Single-width. P2 transition module: 180mm high x 15.5mm wide x 73mm deep
Connectors	Front Panel: One 100-pin high-density per 8 port group Backplane: P1/P2 5-row DINs
Status LED	Tri-color LED used to indicate overall board status
Power	5 VDC @ 5 Amps (maximum with RS232 serial line conditioners installed) +12 VDC @ .25 Amps (maximum with RS232 serial line conditioners installed) -12 VDC @ .10 Amps (maximum with RS232 serial line conditioners installed)
Dissipation	75 BTU/hr.

Specifications	
Temperature	0º to 50ºC (32º to 120º F) operating -40º to 68º C (0º to 150º F) storage
Humidity	5% to 95% non-condensing
MTBF	8 port configuration: >80,000 P.O.H. 16 port configuration: >80,000 P.O.H (per MIL-HDBK-217E)
MTTR	.25 hrs
Certification	FCC Part 15 Class A
Warranty	
Standard	2 year return to factory
Extended	Available; contact factory