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TECHNICAL MANUAL

MAINTENANCE INSTRUCTIONS
WITH
ILLUSTRATED PARTS BREAKDOWN

DEPOT LEVEL

RECEIVER-TRANSMITTER RT-1319/URC
PART NUMBER 914858-801
NSN 5820-01-112-0050

Magnavox Government and Industrial Electronics Company

Contract No. F04606-81-C-0017

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FO-17	0	FO-56 blank	0	FO-95	0
FO-18 blank	0	FO-57	0	FO-96 blank	0
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NOTE

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SAFETY SUMMARY

The following cautions appear in the text in this volume, and are repeated here for emphasis. The page number is referenced on which each caution appears.

CAUTION

Do not allow transmitter to become too hot to comfortably touch during tests. (5-6), (5-18), (5-22)

CAUTION

Do not allow 24 VDC current to exceed 1.4A during alignment of this section to avoid damaging Q1 and Q3. (5-18), (5-19)

CAUTION

Do not allow 24 VDC current to exceed 5.5A during alignment of this section to avoid damaging Q1, Q3 or Q4. (5-22)

CAUTION

Remove RF input power and turn off power supplies before soldering circuitry. (5-23)

CAUTION

The following inputs are considerably above normal input levels. Use only as long as required to observe audio output measurements. (5-82) (5-116)

CAUTION

Use less RF input power if output power is over 15 watts during alignment. (5-22)

INTRODUCTION

This manual was prepared in accordance with military specifications MIL-M-38784A and MIL-M-38798B. This manual provides the depot level maintenance of the Receiver-Transmitter RT-1319/URC.

Chapter 1 provides a general description of the receiver-transmitter, applications for the rt, and general data concerning functions.

Chapter 2 contains information relative to receiving and unpacking of the rt.

Chapter 3 contains instructions for preparation and use and preparation for reshipment of the rt.

Chapter 4 contains two sections. Section I is a broad overview of the functions of the receiver assemblies and is presented from the basis of signal, power and control functions. Section II gives a piece-part description of the functions of the circuits contained in each assembly.

Chapter 5 discusses the levels of maintenance, depot maintenance performance testing of assemblies. Section III includes instructions to perform an overall test of a rt in a bench environment.

Chapter 6 contains block and schematic diagrams of circuits of the rt.

Chapter 7 is the illustrated parts breakdown.

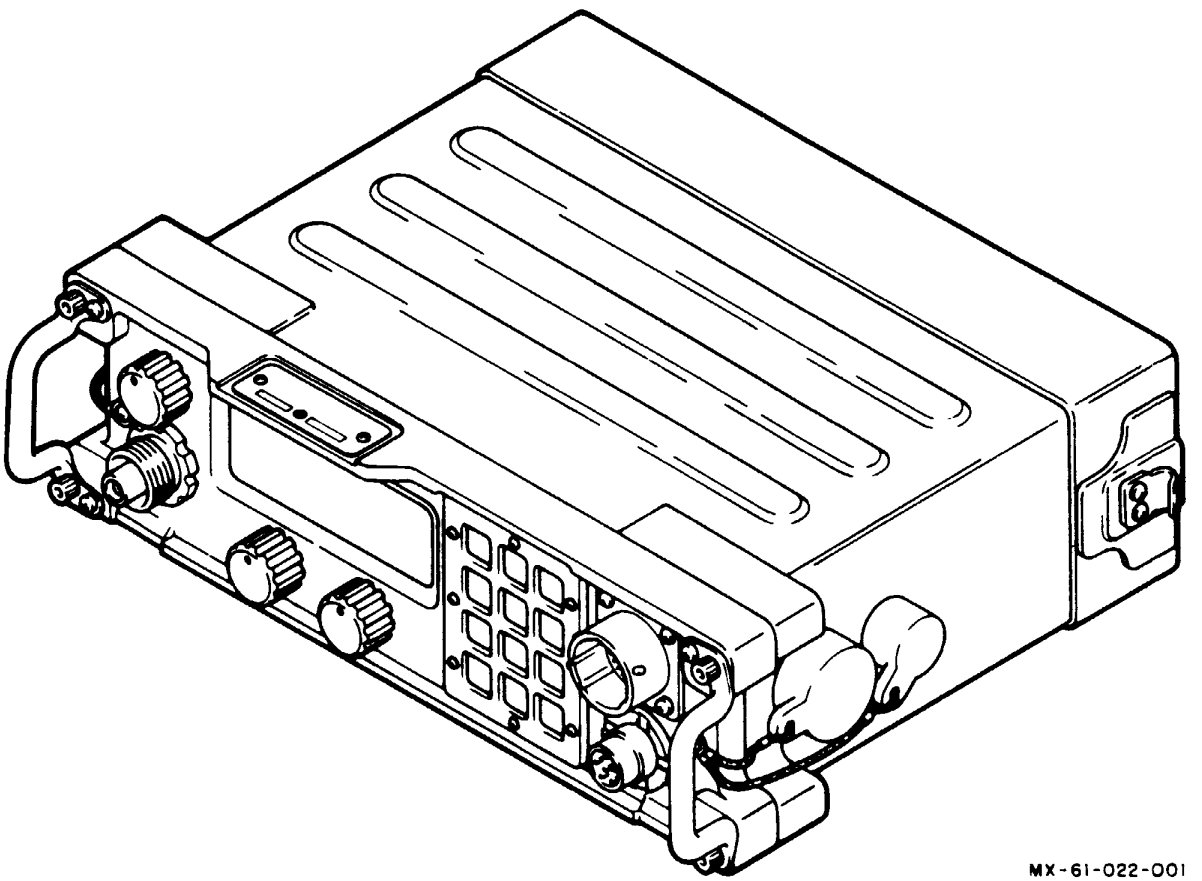


Figure 1-1. Receiver-Transmitter RT-1319/URC.

CHAPTER 1

GENERAL INFORMATION

1-1. DESCRIPTION AND PURPOSE. Receiver-Transmitter RT-1319/URC (RT) is a two band UHF and VHF Amplitude Modulation (AM) receiver-transmitter. It is a major component of the AN/PRC-113(V), AN/VRC-83(V) and AN/TRC-176. When the RT is configured in the AN/VRC-83(V) it also provides UHF and VHF band communications for the AN/GRC-206(V). The RT is illustrated in figure 1-1 and applications for the RT are shown in figure 1-2.

a. Frequency Range. The RT operates on frequencies selected from 7000, 25 kHz spaced UHF channels (225.000 MHz through 399.975 MHz) and 1360, 25 kHz spaced VHF channels (116.000 MHz through 149.975 MHz).

b. RT Control. The RT is controlled by front panel controls and keyboard or radio set control units interfaced to the front panel REMOTE connector.

(1) Local Control. Local control of the RT is accomplished by input keying through the keyboard matrix. This controls all RT functions except OFF-VOLUME, squelch (SQL) adjust, and the illumination level (DIM) of the display. These functions are adjusted by manual rotary controls. Front panel connectors are provided for connection of a VHF or UHF 50 ohm antenna, an audio connector compatible with the H-250/U handset or H-157/AIC headset and secure voice devices. Local control by means of keyboard entries permit the following:

(a) Manual selection of frequency.

(b) Programming any combination of up to eight preset channel frequencies.

(c) Selection of any of the preset channels.

(d) Guard receiver on/off.

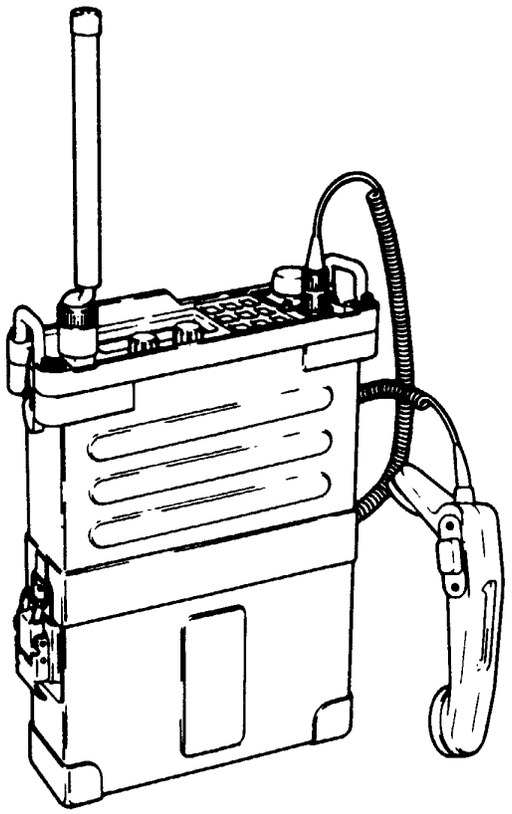
(e) Main receiver squelch on-off.

(f) Direction finding (DF) tone on-off.

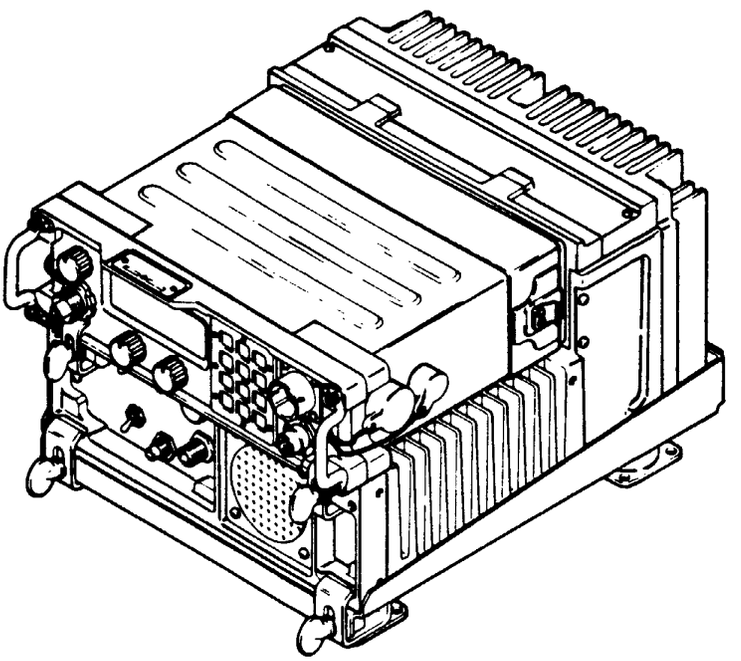
(g) Two-watt or ten-watt transmit power mode selection.

(h) Clearing of incorrect entries.

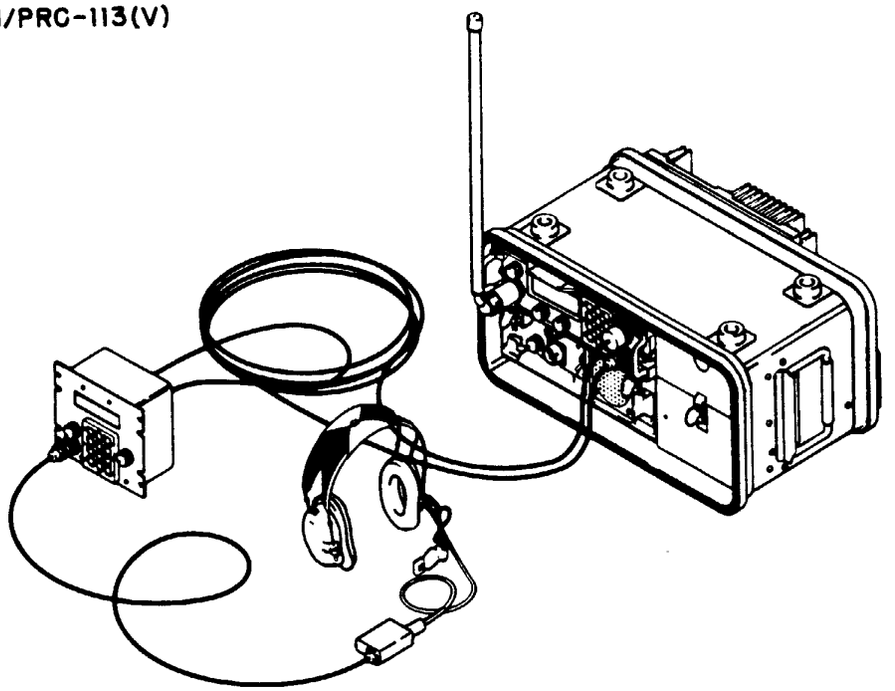
(i) Entry of frequency or relighting of display after battery saver turnoff.



AN/PRC-113(V)



AN/VRC-83(V)



AN/TRC-176(V)

MX-61-022-002

Figure 1-2. Radio Set Applications Using RT-1319/URC.

c. Reception. The RT contains two receivers, the main receiver and the guard receiver. The main receiver is a voice, tone, or secure voice, dual conversion amplitude modulated (AM) receiver. The guard receiver is a voice or tone, single conversion AM receiver operating at the single input frequency of 243.000 MHz.

d. Transmission. The transmitter is capable of voice, tone or secure voice AM transmission output within the frequency bands. When modulated at 90 $\pm$ 5%, output power may be selected at either 2 or 10 watts.

e. Power Sources. The dc supply voltages required by the RT derived from a battery pack, vehicular +28 Vdc supplies or ac/dc supplies capable of supplying +28 Vdc at the required current levels. Input power to the RT is routed through the two connectors located on the rear of the case. The two connectors are electrically isolated by diodes. During battery operation the diodes prevent charging/discharging from one battery to the other and protect against accidentally applying the wrong power source polarity.

1-2. LEADING PARTICULARS. The leading particulars for the RT are listed in table 1-1. They include the mechanical, electrical, cabling, storage and environmental characteristics and requirements.

1-3. CAPABILITIES AND LIMITATIONS. Table 1-2 contains the functional characteristics, individual component characteristics and environmental conditions.

1-4. EQUIPMENT SUPPLIED. A list of major components furnished with the RT is contained in table 1-3. No external cables, batteries or antennas are furnished when the RT is returned for depot level maintenance.

1-5. EQUIPMENT REQUIRED BUT NOT SUPPLIED. The test equipment required for maintenance of the radio set is listed in table 1-4.

1-6. SPECIAL TOOLS AND TEST EQUIPMENT. No special tools are required. The special test equipment required for maintenance of the radio set is listed in table 1-5.

1-7. RELATED TECHNICAL MANUALS. Table 1-6 lists the related technical manuals by publication titles, publication numbers and equipment nomenclature.

1-8. DEFINITIONS OF TERMS AND ABBREVIATIONS. Some terms and abbreviations used within this manual are contained in table 1-7. Other terms and abbreviations found within this manual may be found in Military Standard 12D.

Table 1-1. Leading Particulars

Characteristic	Requirement
PRIMARY POWER REQUIREMENTS	(dependent upon configuration)
Batteries	+24 Vdc (2) BA-5590/U Lithium Organic batteries, non-rechargeable OR +24 VDC (2) BB-590 (U)/Nickel-Cadmium batteries, rechargeable.
+28 Vdc Supply	+20 Vdc to +30 Vdc
EQUIPMENT DIMENSIONS AND WEIGHT	
DIMENSIONS	
Width	8.73 inches
Height	3.00 inches
Depth	6.5 inches
WEIGHT	6.5 lbs
CABLING REQUIREMENTS	The basic RT is not provided with external cables. Cabling requirements are determined by radio set configuration.
STORAGE CONDITIONS	
High Temperature	+155 F (+68°C)
Low Temperature	-70 F (-57°C)
Altitude	40,000 ft (maximum)

Table 1-2. Capabilities and Limitations

Capability/limitation	Description
Frequency	116 to 149.975 MHz (VHF) (1360 channels) 225 to 399.975 MHz (UHF) (7000 channels)
Guard Receiver	243.000 MHz
Channel Spacing	25 kHz
Preset Channels	8, Using nonvolatile electronic memory
Operating Mode	AM voice, AM secure voice, tone
Control Modes	Local and Remote
Frequency accuracy	± 400 Hz maximum
Receiver Sensitivity (Main and Guard)	3 microvolt (HARD) for 10 dB S+N to N @ 30% modulation
Receiver selectivity (Main)	6 dB bandwidth ± 11 kHz minimum 50 dB bandwidth ± 25 kHz maximum
Receiver selectivity (Guard)	6 dB BW ± 30 kHz minimum 60 dB BW ± 75 kHz maximum
Normal audio output	10 mW (minimum), 300 to 3500 Hz at 3 dB points. Distortion less than 10% at 50% modulation.
Communication security compatibility	TSEC/KY-57
Nuclear Hardening	Conforms to Sacramento Air Logistics Center Engineering Specification MMC 77-027D.
Transmitter modulation capability	87% ± 7.5%
Normal audio input	2 mV at 150 ohms for 90% modulation, 300 to 3500 Hz at 3 dB points
Tone modulation	1000 Hz at 90% modulation
Output power	2W, 10W (Operator selectable)
Operating temperature range	155°F (68°C) high -60°F (-51°C) low (without batteries)

Table 1-3. Equipment Supplied

Nomenclature/common name/ reference designation	Purpose	Description
RT-1319/URC, Receiver-Transmitter, A1	Provides UHF/VHF-AM signal reception and transmission.	Consists of case assembly, radio assembly with plug in chassis wiring, and removable flexible interconnecting cable.
Radio Case Assembly, A1A1	Provides the electronic assemblies for radio signal transmission and reception.	Consists of electronic chassis assembly, flexible cable assembly, coaxial cables, chassis wiring and electrical assemblies for transmission, reception, power and signal distribution. Provides connectors to mate with antenna, remote controllers, handset/headsets and secure voice devices.
Data Converter Assembly, A1A1A1	Provides control and display interface function.	Microprocessor controlled data interface. Provides LCD display, mode control, synthesizer frequency control, remote control and voltage monitoring. Consists of four circuit card assemblies (CCA) and a bracket assembly.
Transmitter Assembly, A1A1A2	Provides short range, tactical ground-to-ground, transmissions.	Voice, tone and secure voice AM transmitter. Consists of a CCA, bracket assembly and reflectometer assembly.
Modulator Assembly, A1A1A3	Provides the means by which the carrier frequencies are modulated.	Contains audio circuits, tone oscillator, mode switching circuits, low level RF stages, and the voltage variable attenuator which provides amplitude modulation and carrier level control. Consists of a CCA and bracket assembly.
Main Receiver Assembly, A1A1A4	Provides reception of short range, tactical ground-to-ground, and ground-to-air transmissions.	Voice, tone and secure voice dual conversion AM receiver. Consists of a CCA and bracket assembly.

Table 1-3. Equipment Supplied-Continued

Nomenclature/common name/ reference designation	Purpose	Description
Guard Receiver, A1A1A5	Provides reception of emergency voice AM transmissions.	Voice, tone, dual conversion AM receiver. Consists of a CCA and bracket assembly.
Synthesizer Assembly, A1A1A6	Provides the injection frequency for the main receiver, and carrier frequency. Also supplies 800 kHz clock reference to the data converter assembly.	Provides receiver and modulator injection frequency. Consists of a CCA and bracket assembly.
Power Regulator CCA, A1A1A7	Provides regulated supplies, and reference voltage for low battery indicator.	Outputs +6.3 Vdc, -29 Vdc, -13.5 Vdc, and +12 Vdc reference. Supplies battery sense line to the data converter assembly. CCA is screw mounted to the rear of the RT.
Electrical Chassis Assembly, A1A1A8	Provides interface of CCA's and provides slide mounts for assemblies A1A1 through A1A6. Power switch and regulator are mounted on the rear of chassis.	Consists of a front panel assembly, chassis assembly and a coaxial cable assembly.
Power Switch Assembly, A1A1A9	Switches +24 volt battery, +28 Vdc supplies and ac/dc supplies capable of supplying nominal +24 Vdc to the power regulator.	Converts +24 Vdc input to switched +24 Vdc. CCA is screw mounted to the rear of RT.
Flex Cable Assembly, A1A1W1	Provides interconnection of all assemblies.	Multi-layered flexible wiring assembly with connectors to interface CCA's and chassis wiring assembly.
Coaxial Cable Assemblies A1A1W2 through A1A1W7	Provides interconnection of RF signals between requiring assemblies of the RT.	Semirigid coaxial cables.

Table 1-4. Equipment Required But Not Supplied

Type-designation	Alternate type designation	Figure no.	Nomenclature	Use
ME-426/U	Equivalent	NA	RF voltmeter	Performance test and trouble-shooting.
8300A Fluke	Equivalent	NA	Digital Multi-meter	Performance test and trouble-shooting.
AN/USM-398	Equivalent	NA	Oscilloscope	Performance test and trouble-shooting.
HP436A Hewlett-Packard	Equivalent	NA	Power Meter	Performance test and trouble-shooting.
HP-6443B Hewlett-Packard	Equivalent	NA	Power Supply	Performance test and trouble-shooting.
HP-778D Hewlett-Packard	Equivalent	NA	Directional Coupler	Performance test and trouble-shooting.
HP-8640B Hewlett-Packard	Equivalent	NA	Signal Generator	Performance test and trouble-shooting.
HP-339A Hewlett-Packard	Equivalent	NA	Distortion Analyzer	Performance test and trouble-shooting.
HP-5245L/ 5253B Hewlett-Packard	Equivalent	NA	Electronic Counter	Performance test and trouble-shooting.
CV 2343/U	Equivalent	NA	Balanced Mixer	Performance test and trouble-shooting.
HP-1615A Hewlett-Packard	Equivalent	NA	Logic Analyzer	Performance test and trouble-shooting.

Table 1-4. Equipment Required But Not Supplied-Continued

Type-designation	Alternate type designation	Figure no.	Nomenclature	Use
HP-8558B Hewlett-Packard	Equivalent	NA	Spectrum Analyzer	Performance test and trouble-shooting.
HP-8444A Hewlett-Packard	Equivalent	NA	Generator Tracking	Performance test and trouble-shooting.
HP-8754A Hewlett-Packard	Equivalent	NA	Network Analyzer	Receiver front-end alignment.
HP-8502A Hewlett-Packard	Equivalent	NA	Transmission/ reflection test set	Receiver front-end alignment. Used with HP8754A.
HP-182C Hewlett-Packard	Equivalent	NA	Oscilloscope Main Frame	Performance test and trouble-shooting.
445 AilTech	Equivalent	NA	Power Oscillator	Performance test and trouble-shooting.
185 AilTech	Equivalent	NA	Plug In Unit	Performance test and trouble-shooting.
186 AilTech	Equivalent	NA	Plug In Unit	Performance test and trouble-shooting.
931-2912009 amperes) Weston	Equivalent	NA	Ammeter	Multiple range (10/5/1 for performance test and trouble-shooting.
TRD-54A Telonic	Equivalent	NA	RHO-Tector kit	Reflection indicator to calibrate rf equipment to a VSWR of 1.5.
2HL-1-2W Mini-Circuits Lab	Equivalent	NA	2 Watt amplifier	Signal amplification for modulator test.

Table 1-5. Special Tools and Test Equipment

Type-designation	Alternate type designation	Figure no.	Nomenclature	Use
TS-4091/URC Magnavox	None	1-3	RT-1319 Receiver Test Set, PN 812539-801	Provides power and test equipment interconnection to main and guard receivers.
TS-4090/GRC 206(V) Magnavox	None	1-4	Power Converter Test Set, PN 812540-801	Provides power and test equipment interconnection to power regulator.
TS-4094/URC Magnavox	None	1-5	Multi-Module Test Set, PN 812541-801	Provides power and test equipment interconnection to the RT power switch.
TS-4093/URC Magnavox	None	1-6	Transmitter Module Test Set, PN 812542-801	Provides power and test equipment interconnection, heat dissipation and control signals to RT transmitter assembly.
TS-4092/URC Magnavox	None	1-7	Modulator Test Set PN 812544-801	Provides power and test equipment interconnection to RT modulator.
TS-4141/URC Magnavox	None	1-8	Synthesizer Test Set PN 815155-801	Provides test points, indicators, and connectors to perform synthesizer performance tests and diagnostics for maintenance and trouble-shooting.

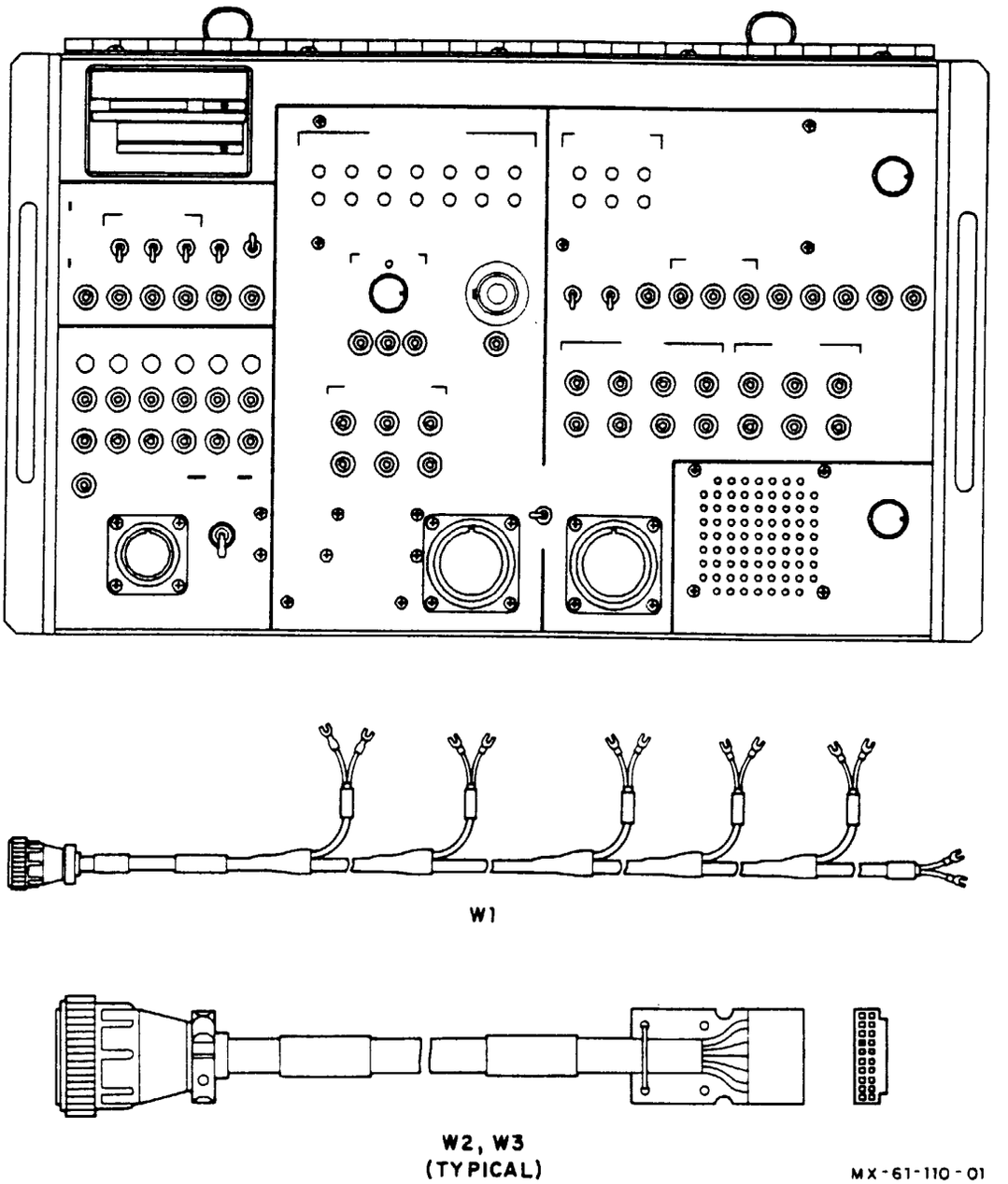


Figure 1-3. RT-1319 Receiver Test Set, TS-4091/URC

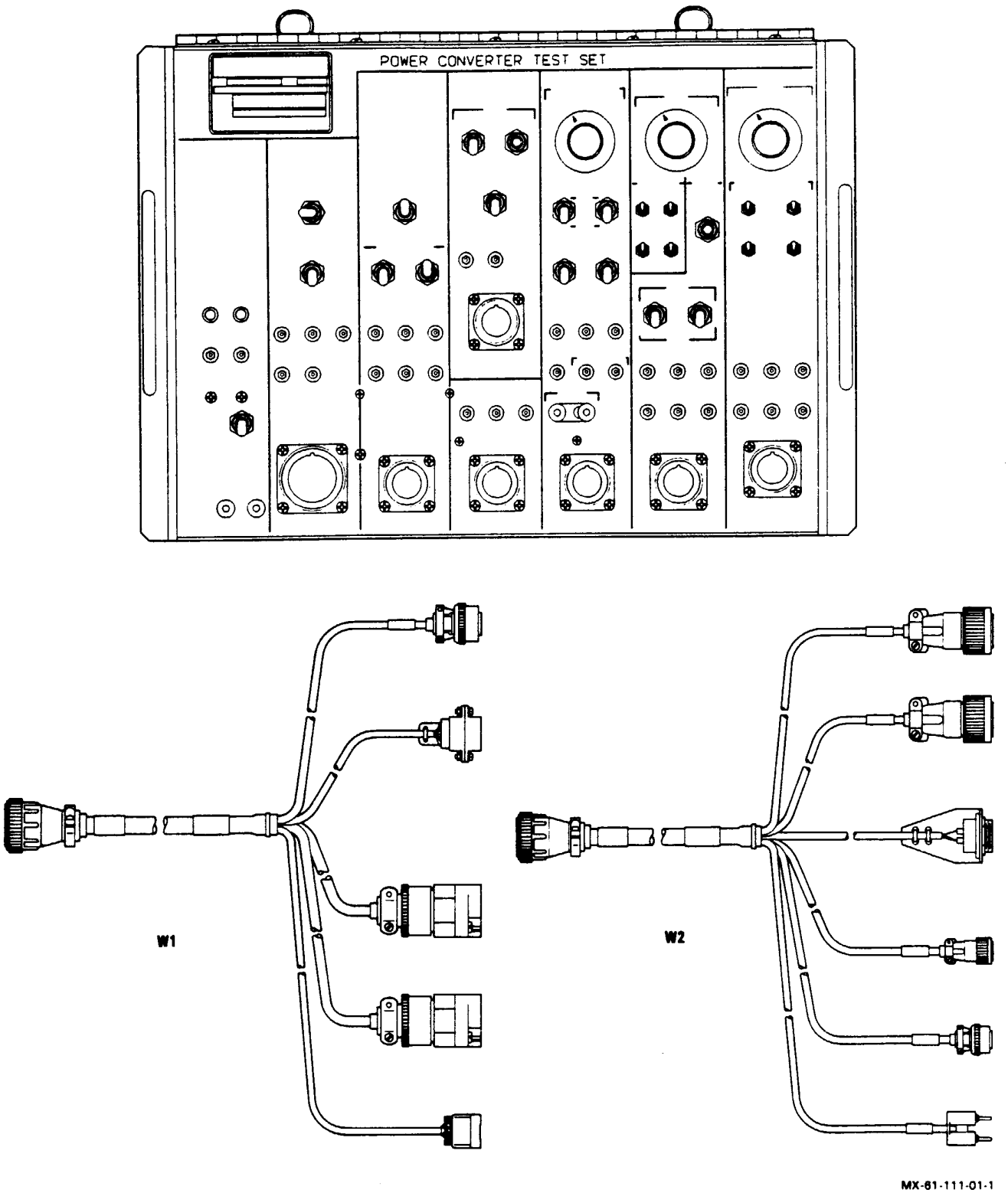


Figure 1-4. Power Converter Test Set, TS-4090/GRC-206(V) (Sheet 1 of 2)

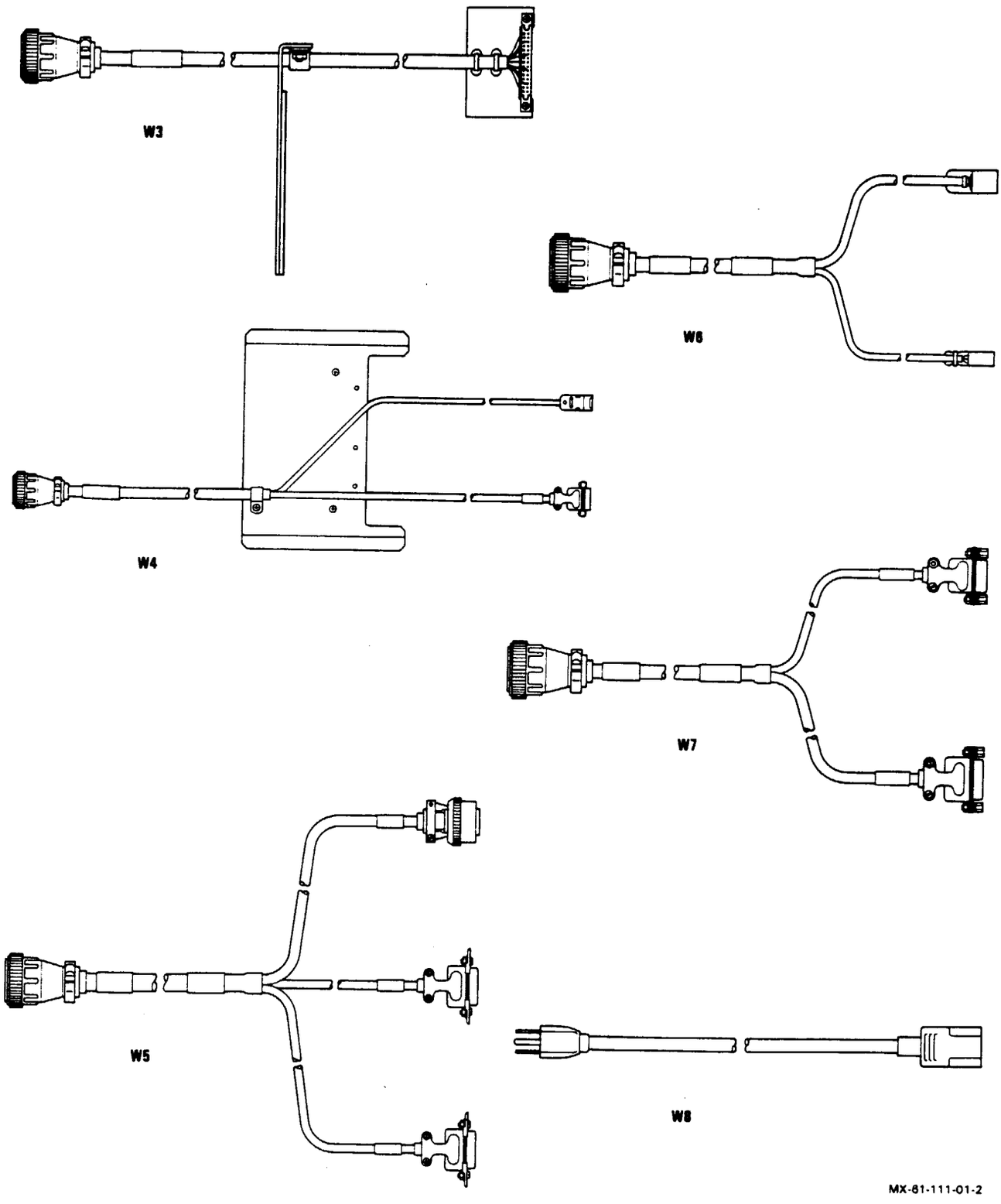


Figure 1-4. Power Converter Test Set, TS-4090/GRC-206(V) (Sheet 2 of 2)

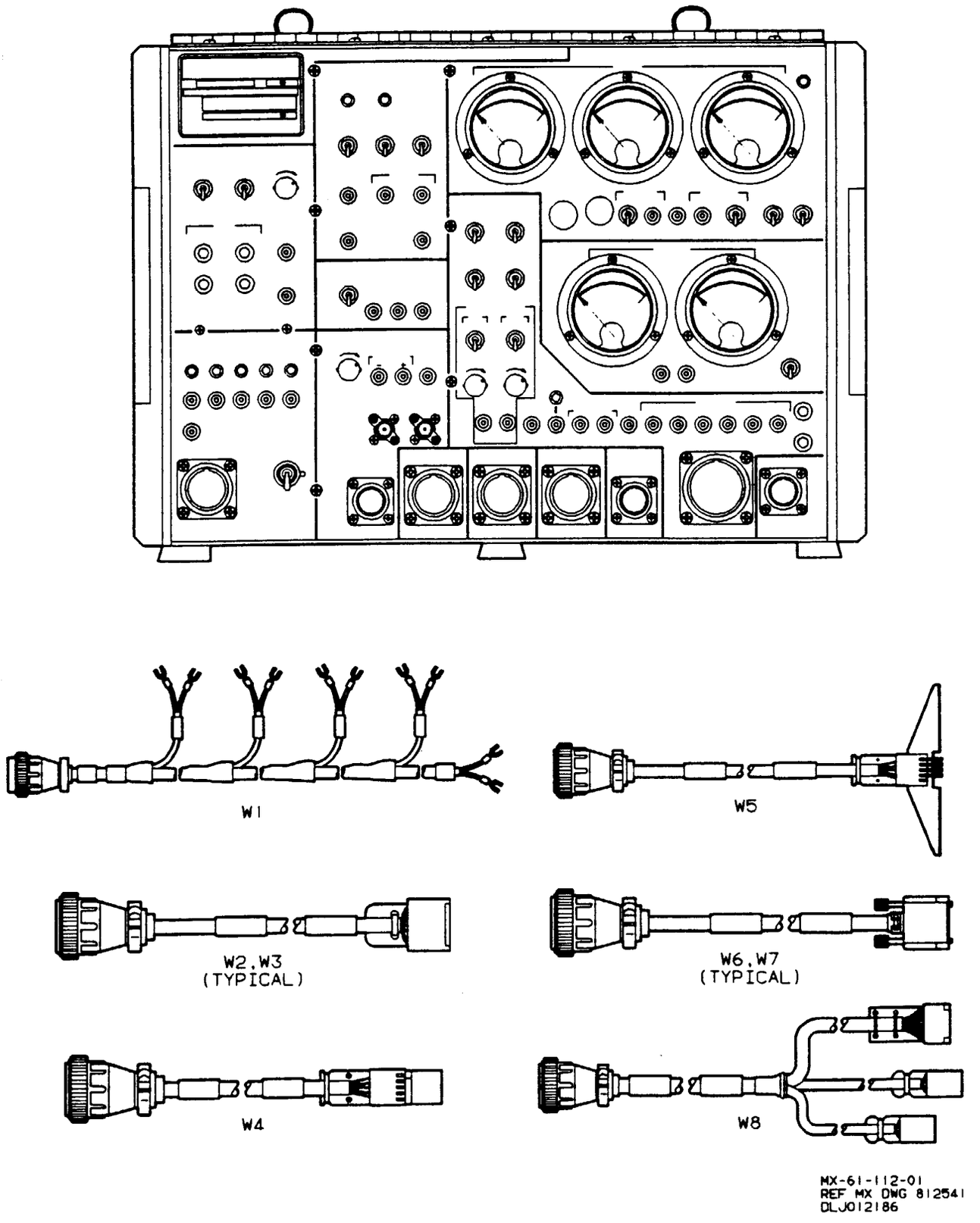


Figure 1-5. Multi-Module Test Set, TS-4094/URC

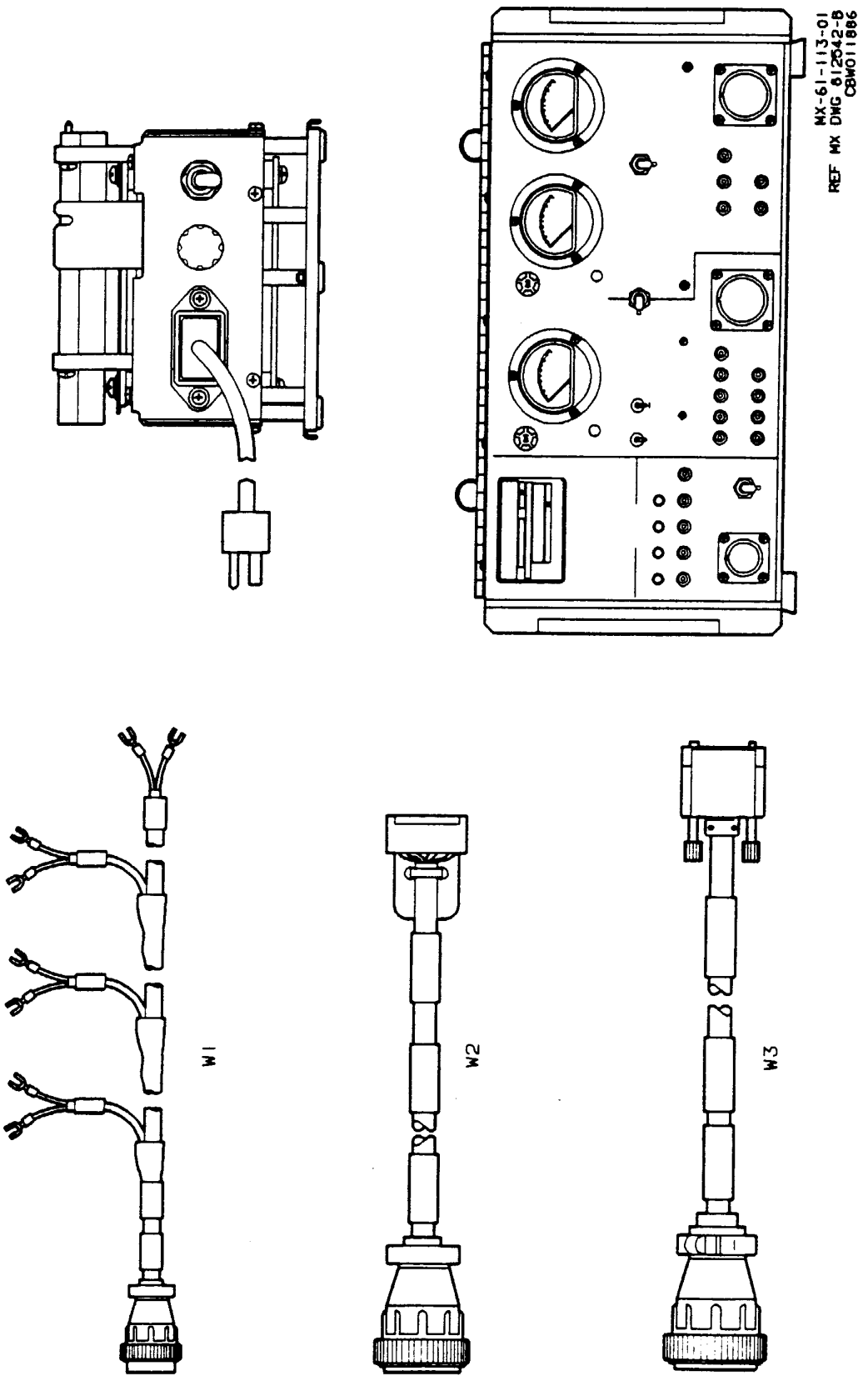


Figure 1-6. Transmitter Module Test Set, TS-4093/URC

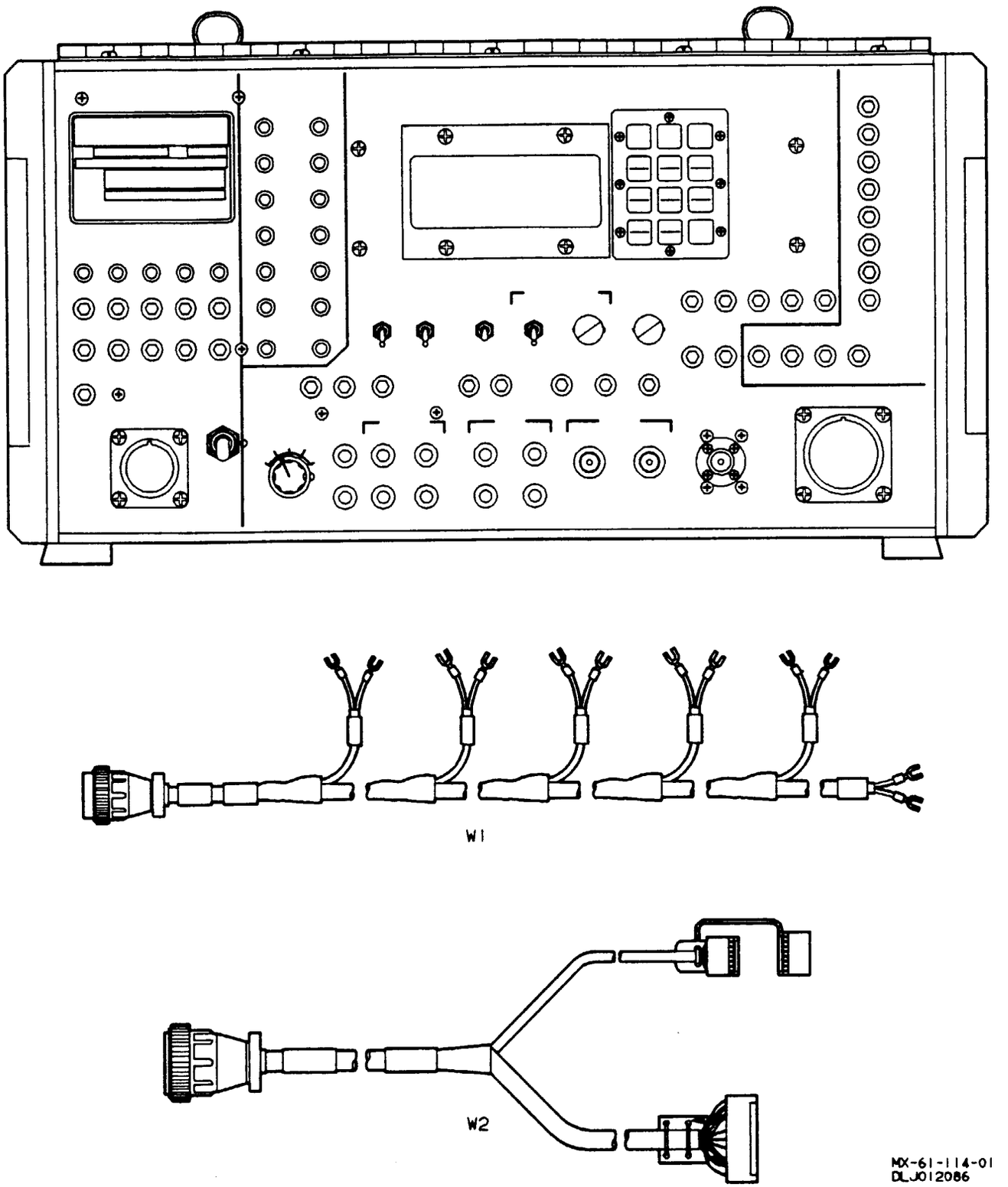


Figure 1-7. Modulator Test Set, TS-4092/URC

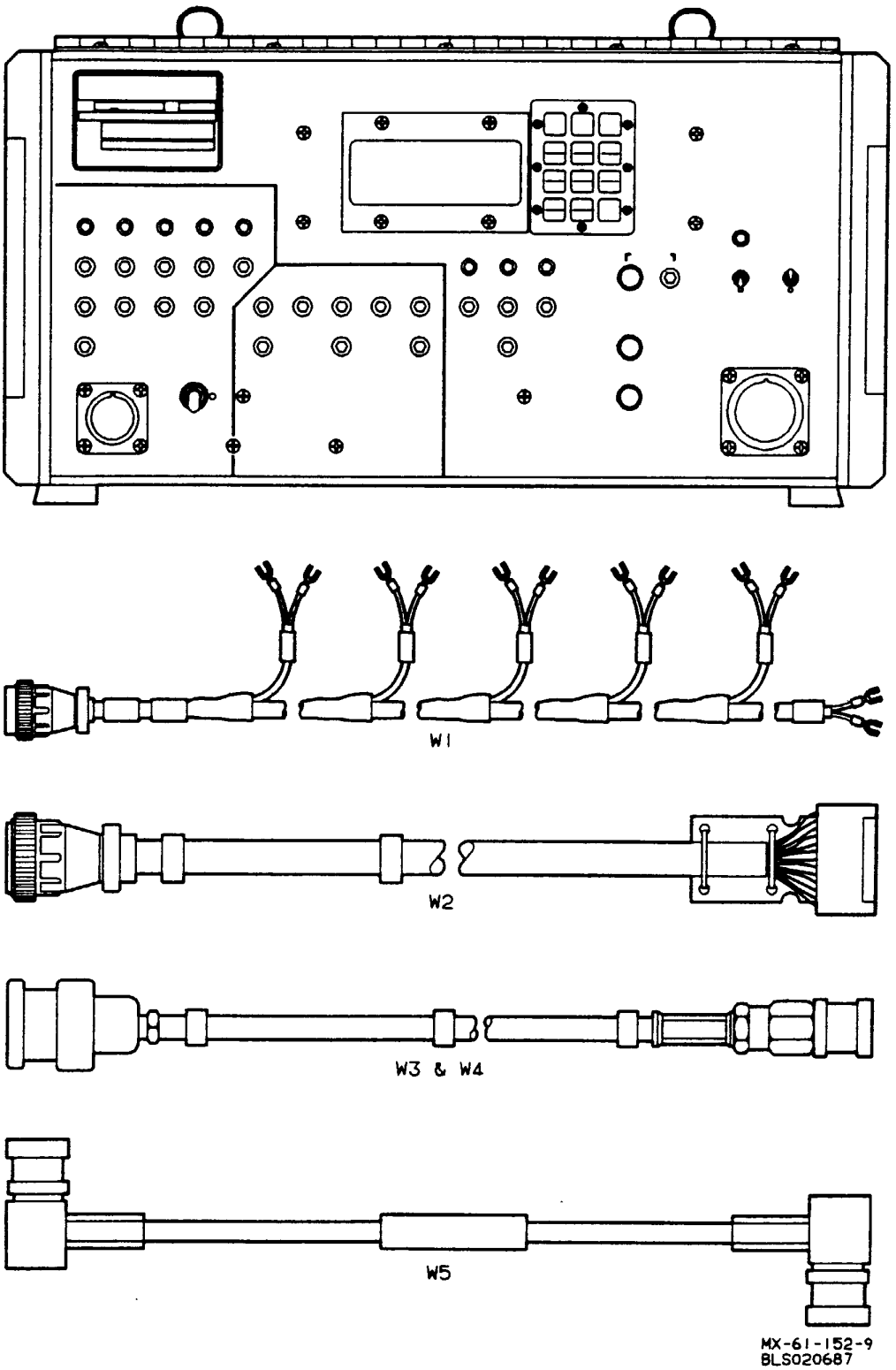


Figure 1-8. Synthesizer Module Test Set, TS-4141/URC

Table 1-6. Related Technical Manuals

Publication numbers	Publication titles	Equipment nomenclature
31R2-2URC-62	Maintenance Instructions with Illustrated Parts Breakdown, Intermediate Level, Receiver-Transmitter RT-1319B/URC	Receiver-Transmitter RT-1319/URC
33D7-50-720-1	Operation and Maintenance Instructions with Illustrated Parts Breakdown, Test Adapter OF-117/U	Test Adapter OF-117/U
33D7-36-51-1	Operation and Maintenance Instructions with Illustrated Parts Breakdown, RT-1319 Receiver Test Set TS-4091/URC	RT-1319 Receiver Test Set TS-4091/URC
33DA27-17-1	Operation and Maintenance Instructions with Illustrated Parts Breakdown, Power Converter Test Set TS-4090/GRC-206(V)	Power Converter Test Set TS-4090/GRC-206(V)
33D7-33-190-1	Operation and Maintenance Instructions with Illustrated Parts Breakdown, Multi-Module Test Set TS-4094/URC	Multi-Module Test Set TS-4094/URC
33D7-33-191-1	Operation and Maintenance Instructions with Illustrated Parts Breakdown, Transmitter Module Test Set TS-4093/URC	Transmitter Module Test Set TS-4093/URC
33DA48-25-1	Operation and Maintenance Instructions with Illustrated Parts Breakdown, Modulator Test Set TS-4092/URC	Modulator Test Set TS-4092/URC
33A1-5-497-1	Operation and Maintenance Instructions with Illustrated Parts Breakdown, Synthesizer Test Set TS-4141/URC	Synthesizer Test Set TS-4141/URC

Table 1-7. Definition of Terms and Abbreviations

Term/ abbreviation	Definition
AGC	Automatic gain control.
ALC	Automatic level control.
BITE	Built in test equipment.
BYTE	A series of data bits used to form a word or symbol.
Bit	A single unit a data.
CLR	Clear erase function.
CMOS	Complementary-Metal-Oxide-Semiconductor.
DF	Direction finding - RT 1000 Hz tone which modulates TX 90 $\pm$ 5%.
DB	Data bus.
DBC	Decibels Under Carrier
DMA	Direct memory access.
ECCM	Electronic counter-countermeasures.
EMI	Electromagnetic interference.
EMP	Electromagnetic pulse.
ENT	Enter.
EPROM	Erasable programmable read only memory.
ESD	Electrostatic discharge.
FET	Field effect transistor.
GD	Guard Display for guard receiver activation.
High level system	In positive digital logic, the more positive of the two binary logic levels.
I/O	Input-Output.
LCD	Liquid crystal display.
LPA	Linear power amplifier.

Table 1-7. Definition of Terms and Abbreviations-Continued

Term/ abbreviation	Definition
LPR	Low power (2 watt) transmit mode.
Low level system	In positive digital logic, the more negative of the two binary logic levels.
Logic 0 is	One of the two values of a binary digital signal. Logic 0 usually the lower of the two voltage levels.
Logic 1	The opposite of logic 0.
LSB	Least significant bit. In data, the bit at the right side when reading left to right.
Modulus	An integer designating the number of states through which a counter sequences during each cycle.
MOS	Metal Oxide Semiconductor.
MNOS memory	Metal-Nitrate Oxide Semiconductor used to generate nonvolatile element by charge storage at the nitrate-oxide interface.
MSB	Most significant bit. In data, the bit found at the left when reading left to right.
MSI	Medium scale integration.
PST	Preset.
PTT	Push-to-talk.
RAM	Random Access Memory. A device that stores data and permits individual interrogation in a random sequence.
ROM	Read-only-memory. A device used to store data for character generation and code translation.
RSC	Radio Set Control. The C11165/TRC-176 or C-11169/ GRC-206 used to remote functions of the RT.
RT	Receiver-Transmitter.
T-R	Transmit-Receive. Control signal to enable the transmit signal and disable receivers.

CHAPTER 2

INSTALLATION

Section I. INSTALLATION LOGISTICS

2-1. GENERAL. The Receiver-Transmitter RT-1319/URC (RT) is used with systems which have antennas, battery or power supplies, handset/ headsets, and remote control units. Installation procedures for the RT as a component of these systems are contained in the TO 31R2-2URC-62.

2-2. RECEIVING DATA. The unpackaged dimensions and weights of the equipment are provided in the table of leading particulars, table 1-1.

2-3. CABLES. No external cables are provided with the RT. Table 2-1 provides a listing of associated cables and equipment used to operate the RT in various radio sets. This listing is provided for the information of maintenance personnel and is not provided as a list of cables required for testing the RT.

2-4. UNPACKING. The RT is normally packaged and shipped as part of a radio set or system. Unpacking instructions are included in TO 31R2-2URC-62.

Section II. INSTALLATION PROCEDURES

2-5. GENERAL. The RT is a component of various systems. For installation instructions refer to the appropriate manual listed in TO 31R2-2URC-62.

Table 2-1. Handset, Headsets and Cables Associated with the Operation of the RT-1319/URC

Nomenclature	Part number
Handset (all configurations)	H-250/U
Input Power Cable Assembly (VRC-83)	565949-801
RF Input Cable Assembly (VRC-83)	565948-801
KY-57 Baseband Cable Assembly (AN/PRC-113, AN/VRC-83, TRC-176 configurations)	566084-808
Audio Cable KY-57 Cable Assembly (AN/TRC-176)	566701-801 566701-802
Remote Cable	565970-801
DC Power CAble Assembly (AN/TRC-176)	565969-801
KY-57 Power Cable Assembly	566007-801
AC Power Cable Assembly	56606-801
Remote Audio Cable Assembly	566651-801
headset	H-157/AIC
Headset Cable Assembly	566656-801

CHAPTER 3

PREPARATION FOR USE AND RESHIPMENT

Section I. PREPARATION FOR USE

3-1. PREPARATION FOR USE. This item is intended to be maintained to piece part level. General concepts of maintenance and employment do not normally require use of the RT-1319/URC at the depot. Refer to TO 31R2-2URC-62 for Intermediate Level Maintenance Activities.

Section II. PREPARATION FOR RESHIPMENT

3-2. SHIPMENT. The assemblies listed in table 3-1 contain electrostatic discharge sensitive devices (ESD) and special handling and packing is required. When packaging the RT for reshipment, the packaging method shown in figure 3-1 is recommended. If a replaceable assembly is to be shipped the packaging method of figure 3-2 should be used. Table 3-2 lists the item number, description and quantity of packing materials shown in figure 3-1. Table 3-3 lists the item number, description and quantity of packing materials in figure 3-2. No special disassembly is required prior to shipping the entire RT. Removal instructions for replaceable assemblies are provided in chapter 5. For special handling and labeling instructions refer to TO 00-25-234.

Table 3-1. List of Assemblies Containing Electrostatic Sensitive Devices

Assembly	Reference designator	Part no.
Data Converter	A1A1A1	914861-801
Interface CCA	A1A1A1A1	914870-801
Memory I/O CCA	A1A1A1A2	914871-805
CPU CCA	A1A1A1A3	914892-803
LCD CCA	A1A1A1A4	811947-801
Modulator	A1A1A3	811827-801
Main Receiver	A1A1A4	811826-801
Guard Receiver	A1A1A5	811955-801
Synthesizer	A1A1A6	811829-801

Table 3-2. Packing Materials for the RT-1319/URC

Item description	Quantity needed/unit
Item to be packed	1
Packaging Bag	1
Label	2
Tape	As required
Fiberboard Box	1
Cushioning Pads (various sizes)	6

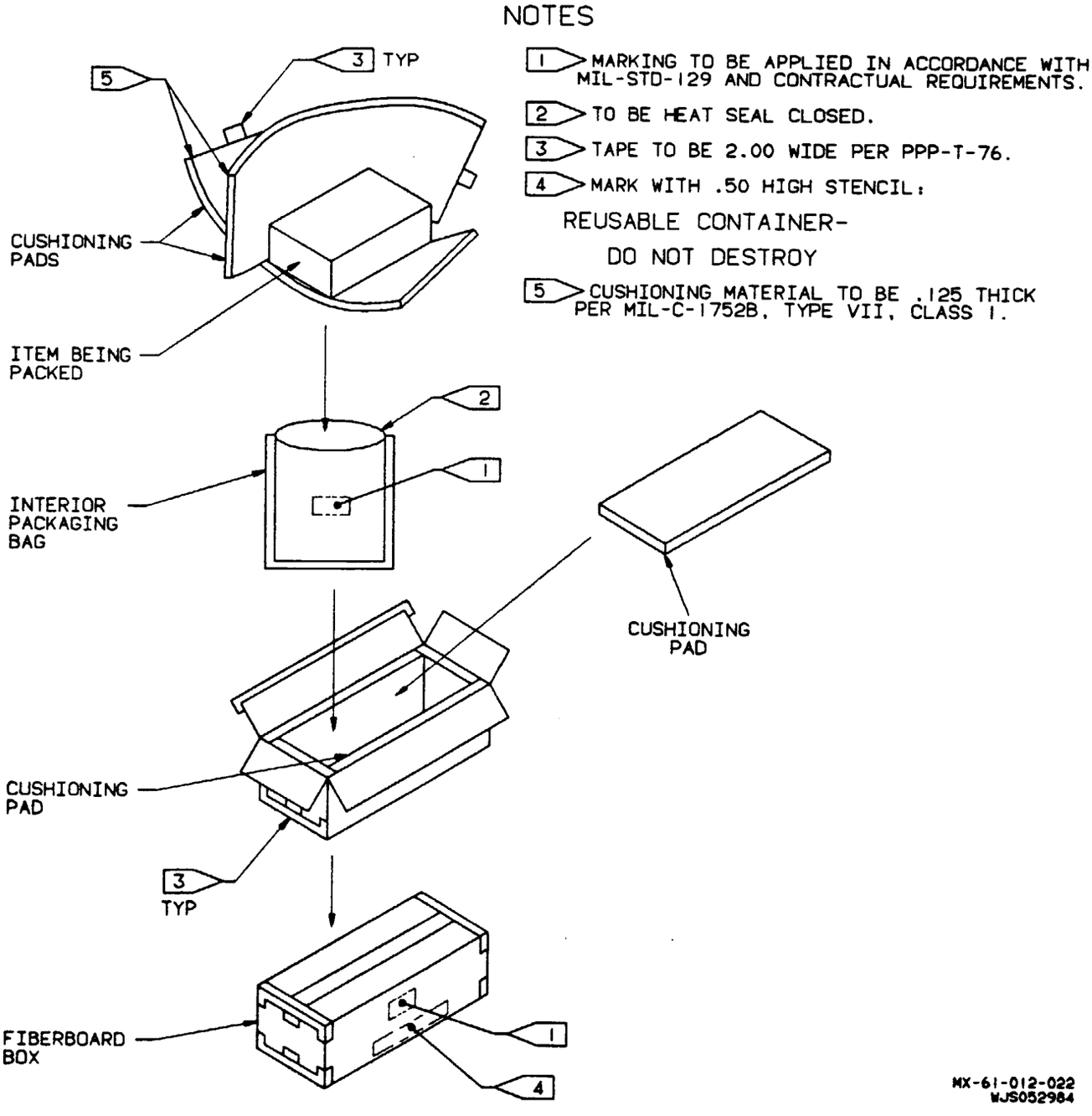


Figure 3-1. RT-1319/URC Typical Packaging Instructions

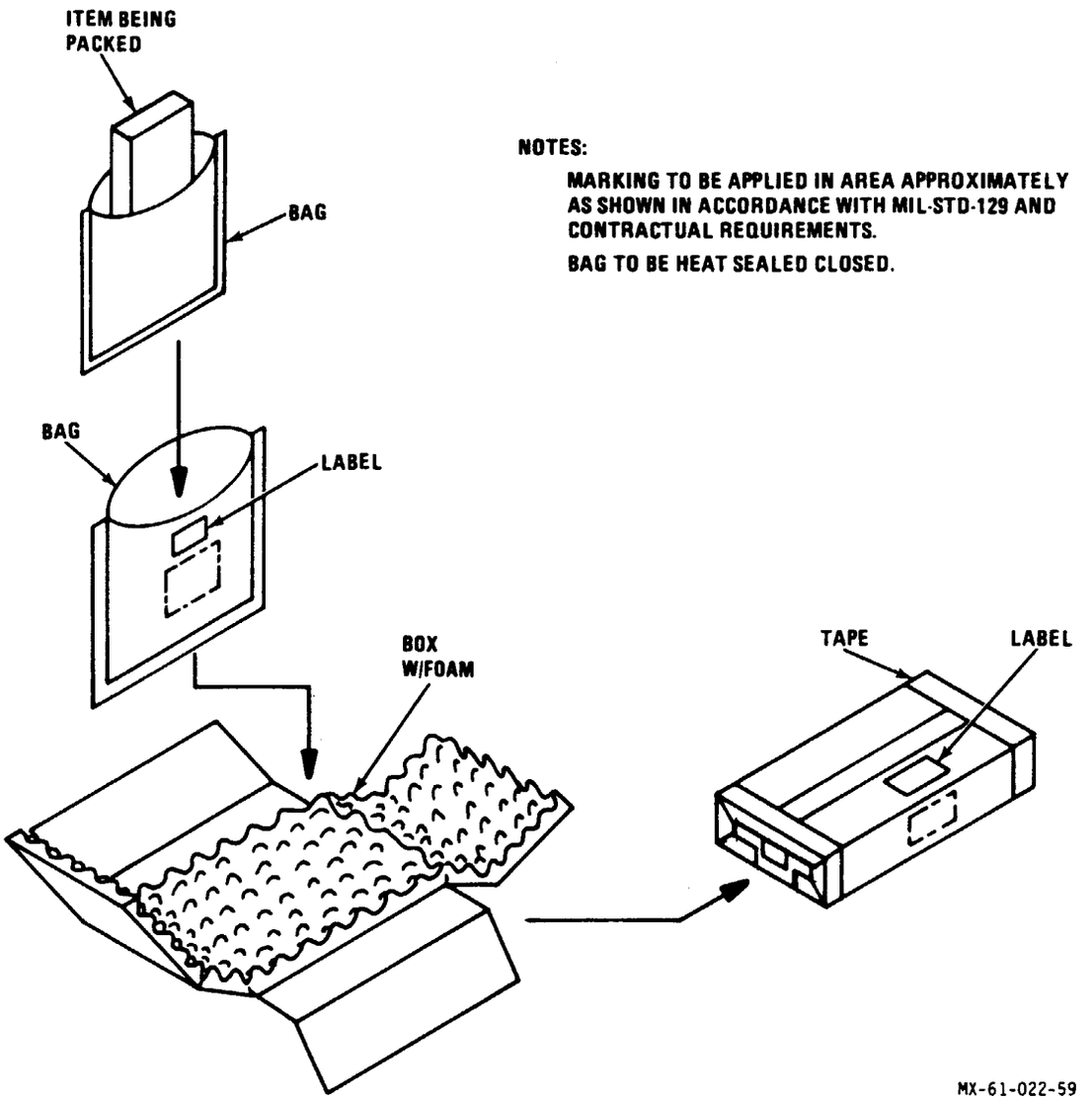


Figure 3-2. Replaceable Assemblies Typical Packing Instructions

CHAPTER 4

THEORY OF OPERATION

Section I. FUNCTIONAL SYSTEM OPERATION

4-1. RECEIVER-TRANSMITTER GENERAL DESCRIPTION. The Receiver-Transmitter RT-1319/URC (RT) is an amplitude modulated voice, tone or secure voice radio assembly. The RT operates on any of 8,360, 25 kHz spaced channels within two operating bands of 116.000 MHz through 149.975 MHz (VHF band) and 225.000 MHz through 399.975 MHz (UHF band). Front panel controls are used during local operation. A remote connector permits operation with a remote control unit. The RT is compatible with either plain text or cipher text operation using the TSEC/KY-57. Basic parameters such as frequency, mode and presets are stored in nonvolatile erasable memory which permits immediate use of the RT at turn-on from previously entered data. A signal flow description of the major functional circuit paths is provided in the following paragraphs, and is illustrated in figure 4-1. The RT-1319/URC schematic diagram is contained in FO-1 at the rear of this manual.

4-2. RECEIVE FUNCTIONS. The RT contains two modular receivers. The main receiver provides reception on selected VHF and UHF frequencies. The guard receiver is fixed tuned to the international guard frequency of 243.000 MHz. During reception, signals from the antenna are routed through the transmitter reflectometer, the transmit-receive (T-R) switch, and through the input connections of the guard receiver before entering the main receiver assembly.

a. Main Receiver Functions. The antenna RF input enters the main receiver and is applied to the input of either a UHF or VHF varactor tuned RF amplifier by means of diode switches. Data converter inputs via data latches determine which RF amplifier is powered and which diode switch passes the received signal.

(1) Mixers. The output of either the UHF or VHF RF stages is applied to a double balanced mixer (Z1) where it is mixed with the selected synthesizer frequency to produce the 30.1 MHz first IF frequency. For receive frequencies between 116 and 310 MHz, the synthesizer generates an injection frequency 30.1 MHz above the receive frequency and for receive frequencies above 310 MHz, the synthesizer generates a frequency 30.1 MHz below the receive frequency. The first IF frequency signal is amplified and applied to a crystal filter that determines receiver selectivity. The output of this filter is again amplified and applied to the second mixer. The second mixer uses a 28.387 MHz signal from a crystal oscillator produces a 1.713 MHz second IF frequency.

(2) AM/FM Detection. The second mixer output is applied to both an IF amplifier - AM detector and an IF amplifier - FM detector. The AM detector output provides the voltage for AGC control of the tuned RF stages, on-chip IF stages and the detected audio signal. The audio signal is coupled through a squelch gate and an audio amplifier to the guard receiver. The FM detector provides an output level which after noise detection becomes the squelch trigger to operate the squelch gate.

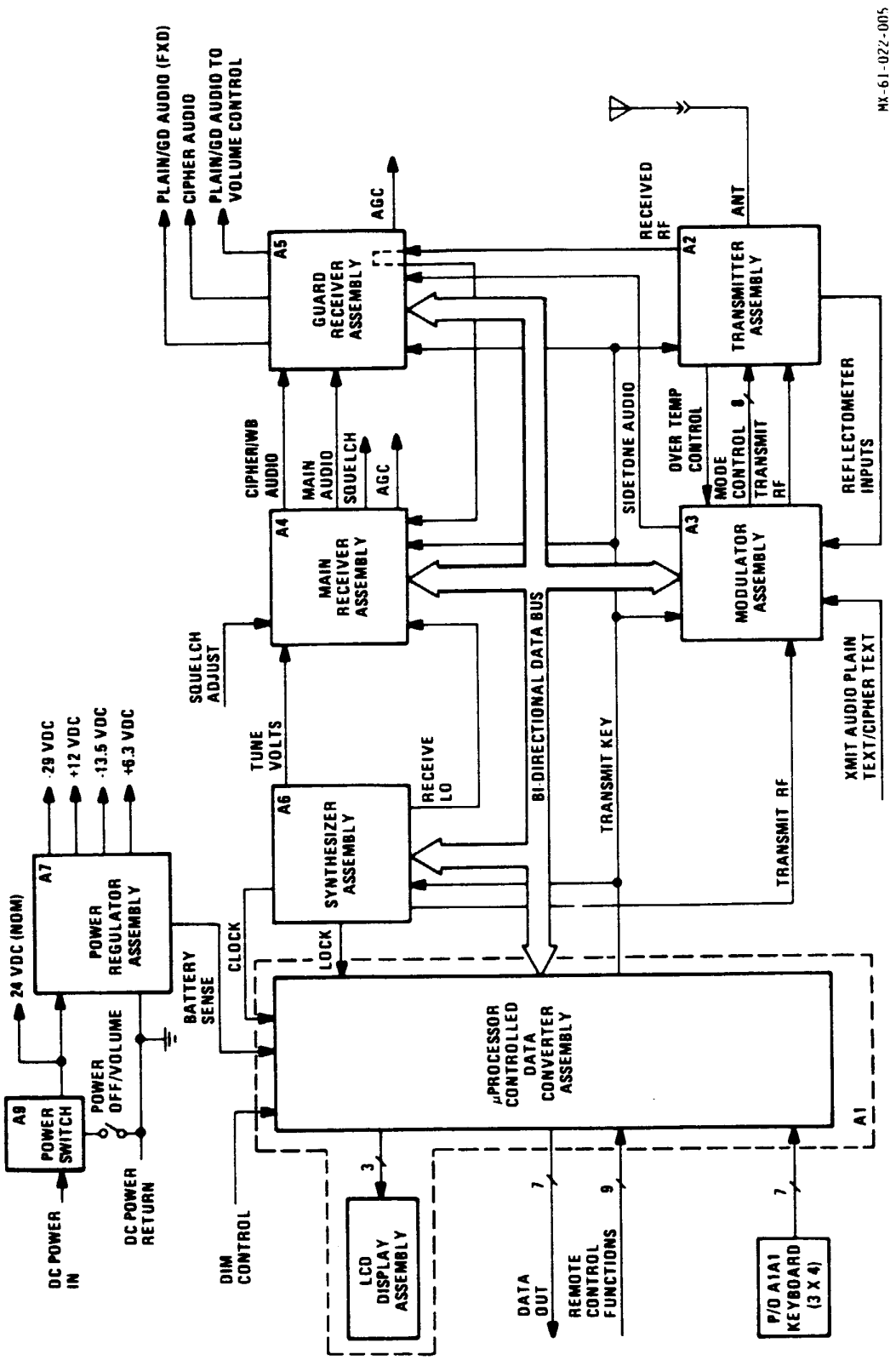


Figure 4-1. RT-1319/URC System Block Diagram

The front panel SQUELCH control determines the threshold at which the squelch gate will operate. Cipher audio does not pass through the squelch gate but is amplified and routed through the guard receiver directly to the audio connector.

(3) Tune Curve Generator. The linear tune voltage from the synthesizer is applied to a tune curve generator circuit contained on the main receiver assembly. The output of the tune curve generator is applied to varactor diodes of the VHF and UHF amplifier stages. The tune generator circuit contains selected resistor components that vary the tuning voltage to attain a consistent response over the input frequency range and overcome the nonlinearity of the varactor diodes.

b. Guard Receiver Functions. The guard receiver contains circuits to produce a common audio for plain text operation and plain text sidetone while in the transmit mode as well as receiving and detecting transmissions on the guard frequency. The guard receiver RF and IF stages are only powered when the guard channel function is selected via the keyboard. Full transmit and receive capability still exists on other VHF/UHF channels though the guard channel may be selected. When guard receiver operation is selected the 243 MHz RF input signal is applied to the fixed double tuned RF amplifier and +12 Vdc is applied to turn on the RF amplifier and the mixer stage. The guard receiver is only lightly coupled to the antenna to prevent reducing the main receiver sensitivity by loading. When the main receiver is tuned to the guard receiver frequency, the data converter disables the guard receiver via the data bus signals to the decoding latch in the guard receiver.

(1) Mixer Stage. The RF amplifier output is mixed with the local oscillator frequency of 212.9 MHz to produce the 30.1 MHz first IF frequency. The local oscillator generates the mixing frequency by doubling the 106.45 MHz signal from a crystal oscillator. To prevent interference, a crystal frequency is used such that no harmonics of the oscillator lies within the VHF band and only one harmonic (319.35 MHz) lies within the UHF band. The crystal filter determines the guard receiver selectivity. The 30.1 MHz IF output signal is mixed with a 28.387 MHz crystal oscillator output produces the 1.713 MHz second IF frequency. The second mixer output is applied to both an IF amplifier - AM detector and an IF amplifier-FM detector.

(2) AM Detection. The AM detector output is applied through the squelch gate to an audio power amplifier. The audio power amplifier output is summed with the audio from the main receiver and the sidetone audio from the modulator module. The audio amplifier output level is controlled by the front panel OFF/VOLUME control and routed to the AUDIO connector. A fixed level audio signal is amplified and applied through the battery connector for connection to audio amplifiers and the REMOTE connector for remote control units. The FM detector output is applied to a noise detector that rectifies noise produces a voltage that operates the squelch trigger of the guard receiver squelch gate.

4-3. TRANSMIT FUNCTIONS. The transmission circuitry is contained in the modulator and transmitter. Control of the modulator is almost entirely determined by software contained in the data converter assembly. This software, inputs from the transmitter and the transmit inhibit input from the data converter defines the operation of the modulator. When used in AN/VRC-83(V) radio sets, an additional

input for LPA fault is used for momentary transmit interruption during bypass switching and fault conditions. The modulator provides impedance matching, amplification, compression and limiting to input audio signals, generates a direction finding (DF) tone and imposes controlled modulation on the synthesizer produced RF carrier. The modulator controls operation of the transmitter assembly in response to data from the data converter, transmitter temperature sensor and reflectometer inputs. The transmitter incorporates 2 watt and 10 watt broadband RF power amplifiers, RF switching networks, output low pass filters and a thermal sensor to detect possible overheating. The reflectometer subassembly of the transmitter samples RF signals for control of output power and protection against high VSWR and recovers audio from the transmit signal for modulation control and sidetone amplification by the modulator.

a. Modulator Functions. Operating information is transmitted on a data bus to addressable latches in the modulator. Information held in these latches; the RT key signal, XMIT INHIBIT signal, LPA fault and over-temperature signal determine the operating mode of the modulator. There are two modes of operation; receive and transmit. During receive mode, the RT key signal will be a logic high and portions of the +12 Vdc, -13.5 Vdc and +5 Vdc power are switched off. Unswitched +12 Vdc, -13.5 Vdc and +5 Vdc maintain power to the data latches, transmitter pin diode drive circuits and audio peak limiter circuit. The unswitched -29 Vdc is applied to the transmitter pin diode drive circuits and the +24 Vdc supplies the power switches.

(1) Modulation Control Circuits. The modulation power control circuits maintain the transmitted carrier power and the modulation index to levels adjusted by the setting of potentiometers within the modulator. This circuit also reduces power output for mode changes (frequency, power level etc.), when faults are detected in the AM-7176/VRC-83 RF amplifier, during periods of excessively high temperature and high reflected power.

(a) Constant carrier output power. The forward power sample applied to the modulation control circuits from the reflectometer is a dc voltage and an audio signal offset by the dc level. The dc component of this error signal through a modulation control amplifier controls the RF resistance of the pin diode attenuator. Adjustment of a potentiometer establishes a carrier reference voltage that is compared to the dc voltage produced by the forward power sample. Voltage differences between the carrier reference and the detected forward power sample provides constant control of the carrier output by varying the resistance of the pin diode attenuator.

(b) Modulation control. Adjustment of a potentiometer sets the modulation index to approximately 90% modulation. The audio component that is returned with the forward power controls the percent of modulation if the transmit power is varied due to temperature, reflected power or decreased gain conditions.

(c) Mode change power reduction. During mode change, the transmit inhibit signal goes to a logic high. This causes the inhibit switch to remove a ground normally connected to the modulation control circuits and receive a negative dc error. This is of sufficient amplitude to reduce the RF output to nearly zero.

When the mode change is complete, the transmit inhibit signal from the data converter returns to a low logic level and the automatic level control (ALC) loop returns to normal operation.

(d) AM-7176/VRC-83 output power reduction. When the RT is operating in an AN/VRC-83(V) Radio Set, the RF amplifier control circuit provides sensing of operating voltage, temperature, high VSWR, and low gain failures. Normally the fault line is at a logic low and 2 watts of RF drive is applied to the RF amplifier. When faults are sensed in the RF amplifier the fault signal goes high, the RF amplifier switches to the bypass mode. During this change, the fault signal briefly causes the ALC circuit to bias the pin diodes for maximum attenuation and then return to normal attenuation. The duration of the maximum attenuation is determined by the time constant established by a resistor and capacitor time delay network.

(e) High temperature power output reduction. In the event of very high transmitter temperatures, the resistance of a thermistor within the transmitter reduces the voltage drop at the transmitter. When the drop in resistance in the thermistor reaches approximately 700 ohms, an over-temperature condition is sensed. This produces a low/high power interrupt signal through the low/high power logic circuit to the modulator control circuit. In the modulation power control circuit, the high temperature interrupt reduces the drive to the pin diode attenuators. This momentarily attenuates the carrier output to near zero so that the switch to low power operation will not damage the pin diodes in the transmitter assembly. The over-temperature control signal also causes the transmitter low/high power control circuit to output a low power signal to the pin diode switches in the transmitter assembly. When the thermistor in the transmitter cools as a result of low power operation, the over-temperature circuit senses the change and switches the transmitter low/high power control to high power. There is no momentary interruption of power when the circuit is switched from low power to high power operation, but the hysteresis of the circuit causes power to remain low until the thermistor recovers to approximately 1200 ohms.

(f) Reflected power. Reflected power caused by antenna failure or improper termination is sampled to produce a dc control voltage to the ALC circuit. Reflected power has the same effect as an increase in forward power. This causes the ALC loop to drive the output power down by increased loss through the pin diode attenuator. A high reflected power does not result in disabling the transmitter, but a VSWR of 2.5:1 decreases the power by 6 dB.

(2) Modulator Power Switches. The RT key line controls the RCV/XMIT pin drive circuit and the gating of the switched +12, -13.5 and +5 Vdc of the modulator. During receive, the RT key line is held high by the data converter I/O port output to the power switches. When the I/O port outputs a low as the result of depressing the push-to-talk (PTT) key, P-channel, enhancement mode MOSFETS are provided gating and components requiring switched voltages are then powered.

(3) Audio Signal Path. The front panel AUDIO connector audio signal is either plain audio from a handset/headset or cipher audio from a COMSEC device. The data converters plain/cipher audio control signals switches cipher audio directly to the summing amplifier or causes plain audio to receive controlled amplification. Plain

audio is input through a variable gain amplifier stage and a fixed gain amplifier stage. The gain of the variable gain amplifier is controlled by a compressor circuit. The compressor receives an input of the audio from the fixed amplifier, rectifies this voltage and uses the rectified voltage to control the gain of the first audio amplifier. This insures the audio signal is a constant amplitude through the second stage of amplification regardless of the volume of the input from a microphone. This compressor controlled audio output is applied to a high pass active filter which removes audio distortion that could produce harmonic distortion. The output of the filter is fed to a summing amplifier.

(a) Summing Amplifier/Peak Limiter. The summing amplifier provides unity gain to the cipher transmit audio, plain audio or 1 kHz tone generator (DF tone) signals. These signals are applied to an audio peak limiter. The audio limiter limits the peak-to-peak amplitude of the audio signal to 1.5 V p-p to prevent transient audio signals at the handset from overmodulating the transmitter. The output of the peak limiter is applied to the active low pass filters.

(b) Switched Low Pass Filters. The switched low pass active filters remove harmonic distortion introduced by the audio peak limiter and control the bandwidth of the transmitted signal. The condition of the cipher and audio control data from the data converter determines whether an active 3 kHz bandpass filter is selected for plain text operation or a 10 Hz to 11 kHz bandpass filter is selected for cipher operation. These filter inputs are in parallel and the outputs are switched. The output from the selected filter is applied to the transmit audio switch.

(c) DF tone mode. The DF tone is generated by a 1 kHz oscillator which feeds the tone into the summing amplifier. A low level DF tone control signal from the data converter RT data bus turns on the oscillator. The DF tone also passes through the audio peak limiter, the switched low pass plain audio filter and the transmit audio switch.

(d) Transmit audio switch. The switched output of the plain audio filter or cipher audio filter is applied to the transmit audio switch. The state of the AM control signal received via the RT DATA BUS from the data converter controls the transmit audio switch. When the AM control signal is low, the selected plain/cipher filter output is applied to both the modulation power control circuit and the power amplifier (PA) transmit control circuit. The modulator audio to the modulation power control circuit. An internal potentiometer adjusts to set the modulation level. The PA transmit audio output of approximately 0.8 Vrms is used in AN/VRC-83(V) configurations only.

(4) Low Level RF Amplifier. The synthesizer RF signal is applied to a low level RF amplifier. The amplifier raises the signal level prior to attenuation and isolates the synthesizer from the pin diode attenuator. The amplifier RF carrier is applied through the pin diode attenuator where modulation occurs.

(5) Pin Diode Attenuator. The pin diode attenuator adjusts the carrier level to maintain constant transmitted power and modulates the carrier amplitude with the selected signals. The pin diode attenuator contains diodes whose RF resistance is a function of the forward bias current flowing through them. This forward bias

forward bias current is controlled by the signal input from the modulator power control circuit. The signal is a composite signal consisting of both an audio and a dc component. The dc component of the signal controls the carrier level. The dc component is derived from the adjustment of the reference adjustment and is varied by the dc produced by the RF sample at the transmitter reflectometer. The audio component of the input signal is from cipher, plain or DF tone signals whose amplitude is also derived from an adjustment to a reference level and is also related to the sampled RF error signal. The audio component of the pin diode attenuator determines the modulation index.

(6) Sidetone Amplifier. The sidetone audio is recovered from the transmitter output sampling of the forward power at the reflectometer. This sample is sent back to the audio connector through the guard receiver circuit under control of the AM sidetone control signal. During secure voice (cipher) operation, the sidetone is disabled. Controlled switching of components permits the sidetone audio to remain constant to the guard receiver in both low and high power modes of operation.

(7) Transmitter Pin Diode Drive Circuit. The transmitter pin diode drive circuits control the selection of the UHF/VHF low pass filters in the transmitter and the transmitter T-R switch position. Control signals (UHF and VHF CONT) from the data converter are input to a data latch and applied to the drive amplifiers. In the receive mode, the T-R key signal turns on the receive pin drive amplifier and the data converter UHF and VHF control signals cause both the UHF and VHF pin drives to go to the receive state of -29 Vdc. In the transmit mode, the T-R key signal results in a receive pin drive signal of -29 Vdc. The same T-R key signal produces corresponding data converter signals which cause the UHF/VHF pin drive amplifiers to assume the output levels (+6 Vdc or -29 Vdc) consistent with the decoded UHF or VHF control signals.

(8) Low/High Power Logic Circuit. Mode selection of low or high power by keyboard operation results in a data converter 2W/10W control signal being received by the low/high power logic circuit. The output from this circuit is applied to the modulation power control circuit and the transmitter low/high power control circuit. This produces a low/high power signal to the transmitter assembly pin diode switches. This signal determines whether or not the output signal will be coupled to an additional 7 dB amplification stage. Since the reference signals in the modulation control circuit are fixed by their potentiometer settings, the feedback signals from the reflectometer could differ by 7 dB from the low to the high power state. The feedback loop would attempt to increase the transmitter power in the low power state to equal the power in the high power state. To prevent this error signal generation during low power operation, the forward power signal is increased by 7 dB by the low/high power logic circuit.

(9) Transmitter Low/High Power Control. The power signal from the low/high power logic circuit switches a comparator in this circuit to produce the LOW/HIGH PWR signal to the transmitter assembly pin diode switches. This selects the appropriate power level of RF amplification. During periods of excessive temperature in the transmitter, the low/high power logic circuit signal causes to output a low power signal to the transmitter pin diode switches.

b. Description of Transmitter Functions. RF signals from the modulator to the transmitter drive amplifiers are amplified 20 dB and routed through the power select switches. The feedback control circuit applies feedback to the two driver amplifiers to maintain uniform gain.

(1) Power Level Selection. The selection of the low (2 watt) or high (10 watt) modes of operation at the front panel determines the HI/LO PWR signal state. This signal is applied to the Low/High power control circuitry and produces the current required to set the states of the power select switches. During low power mode, the output of the driver amplifier is applied through the filter select switches. With high power mode selected, the 2 watt driver amplifier output is switched to an additional amplifier stage where the driver amplifier is amplified to the 10 watt level.

(2) Filter Selection. The keyboard frequency selection determines the state of the UHF and VHF line which switches in the correct low pass filter. The selected filter output is applied to the T-R switch through a second pin diode filter select switch.

(3) Reflectometer. The T-R switch connects either the receiver or transmitter circuits to the reflectometer. During transmission, the filter select switch output is applied through the T-R switch to the reflectometer. A sample of both the forward and reflected power output levels is rectified, filtered and sent to the modulator where it controls the modulator output level to the trans- mitter. The reflectometer output is applied to the antenna. During the receive mode, the antenna RF passes through the reflectometer and the T-R switch to the receiver circuits.

4-4. DISPLAY AND CONTROL FUNCTIONS. The display and control circuitry is contained in the data converter and synthesizer assemblies. The data converter permits operator interface and control of the RT. The data converter accepts operator inputs from the keyboard or a remote control unit connected to the front panel mounted REMOTE connector. The data converter supplies all the active operating parameters (e.g., frequency, modes, etc.) to the operator via the front panel LCD display. The active operating parameters are also supplied to any remote control unit connected to the front panel REMOTE connector. The data converter also controls the receive and transmit function of the RT. The receive or transmit function is selected by the state of an input PTT signal from a handset/headset. The data converter in conjunction with the synthesizer provides timing and frequency control for the RT.

a. Data Converter Functions. The data converter provides keyboard decoding, LCD display control, mode control for all RT functions and synthesizer frequency control. Central to the control functions exercised by the data converter is an 8 bit microprocessor. It accepts remote control signals through the REMOTE connector. Signals from the keyboard or REMOTE connector are coded by the microprocessor and sent to requiring RT assemblies via a bidirectional data bus. These coded signals also go to the REMOTE connector and the LCD display for operator interface.

(1) Keyboard Entries. Pressing a key on the keyboard shorts a pair of wires to provide a digital signal to the keyboard encoder. The encoder sets the data available latch and stores the keyboard entry in its internal storage register. During program execution, the microprocessor reads the flag set by the data available latch. Later, it enables the keyboard encoder and reads its contents.

(2) Clock Processing. The microprocessor clock source is from the synthesizer 800 kHz. The 800 kHz output is frequency doubled to 1600 kHz before going to the microprocessor clock output and system timing generator.

(3) Microprocessor. The data converter microprocessor is an eight bit CMOS microprocessor. The microprocessor communicates with the RT via an 8 bit data bus and a 16 bit multiplexed address bus. The microprocessor generates timing signals which control most of the signal processing within the RT. The most important of these timing signals are the TPA, TPB, MRD, MWR, NO, SCO and SC1. The TPA signal initiates an address transfer and therefore, defines when the upper address is valid. The TPB signal is used to set the timing for data transfer to and from the microprocessor. Therefore, the TPB signal defines when the data and lower address is valid. The MRD signal provides the clock timing to read data from the data bus. The MWR signal provides the clock timing to write data onto the data bus. The NO is used to reset the power-up reset (watchdog) circuit when the system software is functioning properly. The SCO and SC1 signals provide the timing for the DMA generator.

(4) System Timing Generator. The system timing generator includes the DMA generator and the TPC (timing pulse C) generator. These circuits provide the timing for the data converter memory and I/O devices, and establishes the timing reference for the software loops.

(a) DMA generator. The DMA generator produces the timing reference pulses for the software loops. The DMA generator is a free running oscillator and wave-shaping circuit that produces a 20 microsecond wide pulse every 35 milliseconds. The operating program for the microprocessor is provided with idle times at various points in the program. The microprocessor will not step past these programmed idles unless it receives a DMA pulse.

(b) TPC generator. The TPC generator sets up the required timing for the data converters memory and I/O devices. It uses the frequency doubled clock source in conjunction with the TPA and TPB timing pulses supplied by the microprocessor to produce the TPC pulse. The TPC pulse prevents the memory and I/O devices from out-putting data onto the data bus until the previous data is clear of the data bus.

(5) Memory Circuits. The data converter uses volatile and nonvolatile type storage mediums to provide storage of data required to operate the RT. All memory and I/O devices within the data converter are memory mapped. This permits the microprocessor to access any device in the same manner it accesses the main memory.

(a) Erasable programmable read only memories (EPROMs). The data converter uses EPROM type memory devices to store the operating program for the RT. The device is operated in the read only mode and contains all the allowable operating scenarios/parameters for the RT.

(b) Random access memory (RAM). The data converter uses RAM type memory devices to store temporary operating conditions which arise during normal operation of the RT. The information stored in this device will be lost when power to the RT is removed.

(c) Metal-nitride-oxide semiconductor memory (MNOS). The data converter uses a MNOS type memory device to store all user modifiable information which must be retained for long term storage. Such information as presets, last entered frequency and modes are stored in this device. This information will not be lost when the RT is turned off.

(6) RT Control Port. This port controls the transfer of addresses and data to and from the data converter along the address bus and bidirectional data bus. Seven strobes are generated by the RT control port to facilitate the transfer. Outside the data converter, the address bus is designated RT ADRS and the data bus RT DB. Internal to the data converter the RT designation is dropped.

(7) Remote I/O Ports. Remote ports within the data converter provide the interface which permits the data converter to communicate with a remote controller. These ports receive control information from the remote unit and outputs status information to the remote unit for operator interface.

(8) Watchdog Power-up Reset Circuit. The watchdog power-up reset circuit establishes the initial state of all system timing circuits and the microprocessor during power-up. The circuit also monitors the function of the system software during normal operation.

(a) Power-up. When power is applied to the RT, this circuit makes the clear (CLR) line to the microprocessor low for 30 milliseconds and then allows it to go high. This resets the microprocessor and and starts its power-up sequence. In addition, the DMA generator and the TPC generator are also reset.

(b) Normal operation. During normal operation of the RT, this circuit monitors the function of the system software by counting the number of DMA pulses per output instructions. It monitors the execution of an output instruction by the state of the NO line from the microprocessor. The microprocessor must toggle its NO line at least once every 60 milliseconds or this circuit will time out and reinitialize the RT. The circuit is configured to reset the system if two consecutive DMA pulses occur without the microprocessor toggling its NO line.

(9) Power Supply Monitoring Circuits. The data converter monitors two voltages required to operate the RT in the transmit mode; +6.3 and -13.5 Vdc. The following subparagraphs describe these voltages.

(a) Positive 6.3 Vdc. The +6.3 Vdc supply powers the RT control bus circuitry in the data converter. It also enables the transmit functions of the RT. When this voltage is lost, the RT control bus circuitry (e.g., RT data bus, RT address bus and strobes) is disabled. The supply is monitored by a low voltage detector circuit in the data converter. When the supply is lost, the output of this circuit enables I/O controllers internal to the microprocessor to read status information at a time determined by the program. Included in this status information is the state of the BATTERY SENSE input. When this input is below the required operating level, the microprocessor responds by enabling the low voltage indicator (blinking decimal point) on the front panel display. It also disables all transmit functions of the RT. Once normal power is restored, the low voltage detector circuit is reset, and the low voltage indicator and the transmit inhibit function is disabled.

(b) Negative 13.5 Vdc sensing. The -13.5 Vdc supply is not used by the data converter, but is monitored to insure proper operation of transmit functions provided by the modulator. When this supply becomes more positive than -5 Vdc, the transmit function is disabled by shutting off operating power to the modulator. This is accomplished by inhibiting the function of the T-R key. When the supply voltage returns to normal before the next operation of the PTT line, normal functioning resumes.

b. Description of Synthesizer Functions. The synthesizer is a digitally controlled phase-lock-loop synthesizer that derives all frequencies from a single crystal. The loop consists of a charge-pump-phase-detector, a low pass reference frequency filter, a voltage controlled oscillator (VCO) and a programmable digital divider (consisting of the main counter, swallow counter and divide by 80/81 counter). The reference input to the loop is the frequency supplied by the reference oscillator/divider. The output is the desired output frequency of the VCO. The signal flow within the synthesizer begins with the loading of the data latches with a count determined by the microprocessor in the data converter. When the counters reach a zero count, they are reset by an end-of-count signal and the counting cycle is repeated. The output from the counters is applied to one input of the charge-pump-phase-detector. The other input of the charge-pump-phase-detector is supplied by the divided down count of the temperature-compensated-crystal-oscillator (TCXO).

(1) Reference Oscillator and Divider. The temperature compensated crystal oscillator (TCXO) 3.2 MHz output frequency is divided by 4 to provide an 800 kHz clock to the data converter. This output is further divided by 32 to obtain the 25 kHz reference frequency for the charge-pump-phase-detector. The 25 kHz reference frequency determines the minimum spacing between channels. It also provides the reference against which the counter outputs are compared to produce the error voltage applied to the reference frequency filter. The 25 kHz components are removed from the error signal by the reference frequency filter and the resultant dc signal is integrated. The loop integrator control signal varies the loop integrator time constants to permit faster lockup during channel change. It also adjusts the loop gain variation within the phase-locked-loop to make it more uniform across the band. The integrated error signal is then applied to the VCO.

(2) Loop Output. The 225 to 400 MHz VCO output is applied to the VHF/UHF pin diode switch. The data bus VHF/UHF signal determines the state of this switch. When the frequency selected at the keyboard is a UHF frequency, the VCO output is applied to the T-R pin diode switch. When the RT is operating in the VHF band, the synthesizer VCO continues to operate at UHF frequencies but the output is divided by two and filtered before being applied to the T-R pin diode switch. The data bus R/T key signal determines the state of the T-R switch. When the PTT key on the handset/headset is depressed, the VCO output is routed through the T-R switch and applied to the modulator RF injection port. Otherwise, the VCO output is routed through the T-R switch and applied to the main receiver injection port. The phase-locked-loop is completed by the application of the VCO output to the divide by 80/81 counter whose output (the divided-down loop feedback frequency) is used to clock the main and swallow counters.

4-5. RT POWER FUNCTIONS. The input voltage is applied through a power switch circuit under control of the front panel OFF/VOLUME control to the input terminals of the power regulator. The power switch provides the switched +24 Vdc to the transmitter for power amplification stages and to the REMOTE connector. The power regulator provides four regulated dc voltages; +6.3, -29, -13.5 and +12 Vdc. A BATTERY SENSE signal is generated by the regulator and sent to the data converter to produce a visual alarm during low input voltage conditions.

a. Power Switch Circuit. The dc voltage from each of the battery connectors enters the power switch through isolation diodes. The two input diodes provide isolation of the batteries and prevent a discharged battery from placing a current drain on a fully charged battery. This input voltage is then applied to the drain terminal of a series pass P-channel FET. When the gate circuit of the FET is grounded by operation of the OFF/VOLUME control switch, the +24 Vdc is switched to the power regulator and transmitter RF stages. A SCR connected across the gate of the FET causes the FET to shut off during gamma radiation.

b. Power Regulator Circuit. The RT power regulator operates from input power supplied from 24 volt batteries or dc supply capable of supplying a nominal +24 Vdc at 4.2 ampere average and up to 10 ampere peak levels. The RF power amplifiers within the RT operate directly from the switched input supply voltage (+20 to +30 Vdc). All other circuits require regulated supply voltages.

The RT power regulator produces these regulated supplies. The switched +24 Vdc input from the power switch is filtered by a low pass inductive capacitive (LC) filter to the input circuits of two independent switching mode regulators. During the on cycle of the series switch in these regulators, the +6.3 Vdc and +12 Vdc is produced. A flyback winding on each of these regulators produces the -29 Vdc and -13.5 Vdc supplies when the series switches are off and the internal shunt diodes are conducting. A comparator circuit monitors the input voltage and compares a portion of it against a +1.3 Vdc reference voltage obtained from the +12 Vdc switching regulator. This comparator output provides the BATTERY SENSE input to the data converter. When the comparator senses input voltages below +18 Vdc, the BATTERY SENSE input to the data converter causes the decimal in The frequency display to blink.

Section II. FUNCTIONAL THEORY OF CIRCUIT OPERATION

4-6. GENERAL. This section provides a detailed theory of functional circuit operation of the RT. The overall wiring diagram of the RT and detailed schematic diagrams of the assemblies are contained in foldouts at the rear of this manual. Block diagrams are provided to illustrate the descriptions of each assembly.

4-7. MAIN RECEIVER ASSEMBLY A1A1A4. Refer to figure 4-2 for a block diagram that illustrates general signal flow. Refer to FO-9 at the rear of this manual for a detailed schematic diagram illustrating these circuits. The main receiver is a two band, dual conversion AM receiver. Band selection and turn on of the amplifiers is controlled by inputs from the RT data converter. Squelch override is manually selected by keyboard entry and squelch is adjusted by the RT front panel SQUELCH control. When squelch is in the closed position, the audio output is suppressed not less than 40 dB. When operated with the squelch mode selected, noise recovered by a

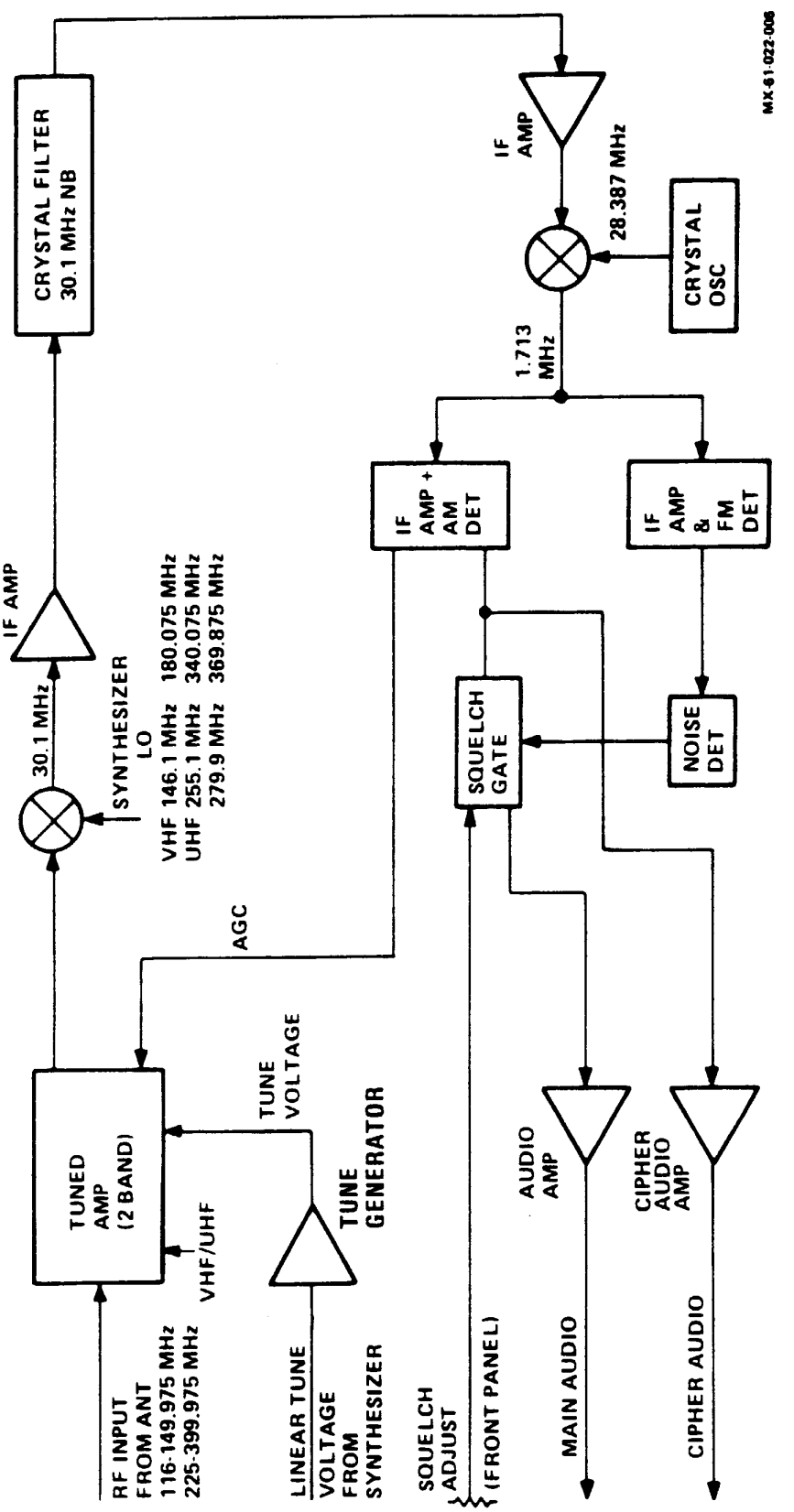


Figure 4-2. Main Receiver Assembly A4 Block Diagram

FM noise detector produces a dc control voltage. Amplification by the RF amplifier stages (normally between 10 and 20 db) is controlled by automatic gain control (AGC) voltages produced by the AM detector. The voltage produced by the AGC circuit increases in magnitude as the receive signal level increases. An injection frequency from the synthesizer provides the mixing frequency to the first mixer stage. Tuning voltage from the synthesizer is altered by the tune curve generator to provide the correct voltage to the varactors to tune the front end to the selected frequency. The second IF (1.713 MHz) is produced by mixing the first IF (30.1 MHz) with a crystal controlled 28.387 MHz. Audio detection produces two fixed audio outputs (narrow and wideband). A third audio produced from FM is also present in the main receiver, but is not used. The wideband output is used during cipher text operation and is routed through J3-17 to the guard receiver and to the front panel AUDIO connector. The narrowband audio signal at J3-13 is interconnected to the guard receiver audio amplifier stage. Audio distribution through the guard receiver to the front panel is discussed in the description of the guard receiver assembly. The following paragraph provides a detailed description of the theory of the main receiver circuits.

a. Data Latch. U1 is an 8 bit addressable data latch. Address conditions of the latches (Q0 through Q7) are contained in table 4-1. Control data is written into the addressed latch by the data contained on the RT data bus (RTDB0). Data can be read from the latches regardless of the state of the main receiver strobe, but data may only be written into the latches when the main receiver strobe (U1-4) is low. U1 is configured so that data written into the latch follows the input on the data bus, e.g., if the data condition on the bus is a high, information entered in the selected latch will also be high. Information written into the latch will remain until changed.

Table 4-1. Address Conditions of U1 Latches

Signal	Latch output	Address state A2	A1	A0	Interfacing device
VHF ON/OFF	Q0(Pin 9)	L	L	L	Base Q11
UHF ON/OFF	Q1(Pin 10)	L	L	H	Base Q10
SQL Disable	Q2(Pin 11)	L	H	L	U6A-9
AM Audio Sel	Q3(Pin 12)	L	H	H	U6B-8
FM Audio Sel	Q4(Pin 13)	H	L	L	U6D-16
WB/NB IF Sel	Q5(Pin 14)	H	L	H	U5B-6 (Not used in RT-1319/URC)
UHF/VHF Sel	Q6(Pin 15)	H	H	L	U5A-2
None	Q7(Pin 1)	H	H	H	Not used

NOTE: L=LOW (<0.4 Vdc), H=HIGH (>4.0 Vdc).

b. RF Amplifier Stages. RF signals at the antenna are switched by the T-R control within the transmitter assembly. During receive mode, signals are routed through the guard receiver assembly and then through J2 to the two band (VHF-UHF) amplifiers. The VHF stage consists of tunable input transformers, Q1 circuitry and tunable output stages. Manually tuned components L5, L7, L12, C4, C23 and C30 are adjusted for maximum gain and symmetrical response over the frequency range of 116.000 to 149.975 MHz. Input coupling is through L4 and L42 which are adjusted for minimum return loss. Gain of the VHF amplifier is controlled by delayed AGC input to MOSFET Q1-2 through R4. The UHF amplifier stages also consists of tuned input and output circuitry with MOSFETs Q2 and Q3. Manual tuning of the UHF amplifier consists of inductors L3, L8, L13, L15, and L17, and capacitors C9, C28, C31, C44 and C49. Delayed AGC input for the UHF amplifier stage is through R14 to MOSFET Q2-2. Electrical tuning of both the VHF and UHF amplifier stages is accomplished by the voltage variations from the tune curve generator to varactor diodes.

c. Tune Curve Generator. U4B is 1/4 of a linear operational amplifier. Tuning voltage from the synthesizer is routed through J3-3 to U4B-2. The tune voltage varies from approximately +1.7 Vdc at 225.000 MHz to +7.1 Vdc at 399.975 MHz when operating in the UHF band and from +2.5 Vdc at 116.000 MHz to +4.5 Vdc at 149.975 MHz when operating in the VHF band. Resistors R90, R92, R94, R107, R108 and R109 are selected components used to set the operating point of the tune generator to provide the correct voltage to the varactors so they can produce the proper capacitance to tune the tank circuits to the selected frequency. Tune voltage for RF amplifier stages is applied to varactors CR3 through CR6, CR7 through CR9 and CR56 and CR10 through CR13 when operating in the VHF band; CR14 through CR17, CR22 through CR25, and CR26 through CR33 when operating in the UHF band.

d. RF Band Selection. RF band selection and amplifier turn on is accomplished by control data through U1. In order that a RF amplifier stage operate, the selected amplifier (n-channel, enhancement mode MOSFETs) must be turned on. During VHF operation the data state of U1-15 is at a logic low. This is applied to inverter U5A-2 and a high condition exists at U5A-1. This high condition forward biases CR1 while reverse biasing CR2 (UHF amplifier input) and CR34 (UHF amplifier output). This produces a high input impedance to all RF signals present at the input to the UHF amplifier stage and Q2 and Q3 are turned off. When the VHF input is enabled, latch U1-9 is also at a logic high condition. This causes Q11 and Q8 to conduct and provides power to MOSFET Q1 through R3 and R7. During UHF operation, latch U1-15 is at a logic high condition. This high is inverted by U5A to a low condition and CR2 and CR34 are forward biased, enabling the input and output of the UHF amplifier stage. CR1 is reverse biased and present a high impedance to RF signals. Additionally, power is not applied to MOSFET Q1 and the input stage of the VHF amplifier is disabled. The high condition present from U1-9 causes Q10 and Q7 to conduct and power is applied to Q2 and Q3 are through R12, R18, R20 and R26.

e. First Mixer, IF Amplifier and Filter Stages. The phase-locked-loop synthesizer provides the mixer injection frequency at J1. The synthesizer input is routed to mixer Z1 and is mixed with the amplified RF signal to produce the 30.1 first IF frequency. Within the UHF band, when the operating frequency is below 310.000 MHz, the injection frequency is 30.1 MHz above the operating frequency. At 310.000 MHz and higher, the injection frequency is below the operating frequency by 30.1 MHz. The IF output of Z1 is transformer coupled to the IF amplifier, Q4. IF amplifier

MOSFET Q4 is turned on through R31 and R38 when either the VHF or UHF amplifier has power applied. The amplified IF is routed through the narrowband IF crystal filter (FL1).

f. Second Mixer Stage. The filtered 30.1 MHz IF is input to AGC controlled IF amplifiers at U3-18 and then to the mixer stage of U2-16. The 30.1 MHz is mixed with a crystal controlled oscillator signal of 28.387 MHz to produce a 1.713 MHz second IF that is returned to U3-13 for AM detection. The detected audio exits U3-15 to U4D-9. During clear text AM operation, a low is present on analog switch U6B-8 and it is operated in the closed position. When signal conditions are correct to close the squelch circuit or when squelch is turned off by the operator, U6C is closed. The audio is then input to U5D. Audio is also output from U4D to U5C, bypassing analog switches U6B and U6C to U5C as wideband audio.

g. Squelch Control Circuits. The 1.713 MHz IF at U2-3 is returned to U2-5 for amplification limiting. This signal is output to tuned circuitry at U2-7 and the filtered signal returned at U2-8. An FM demodulator within U2 produces audio and noise products that are sent to FM circuitry. Components C73, C74, C75 and R46 form a high-pass filter to filter noise above the audio range. This noise is detected by CR44 and CR45 and the representative dc voltage is sent to U4A. The threshold of U4A is determined by operator adjustment of the front panel mounted SQUELCH control and the amplitude of noise. When the RF input signal is sufficiently high, the amplitude of the rectified noise decreases below the level set by the squelch control and U4A outputs a high condition to U2-12. The low output at U2-13 closes the analog switch U6C. When squelch triggering is manually overridden by the operator (a low output from U1-11 causing U6A to close) a path is completed from the +6.3 Vdc bus to establish a logic high to U2-12 and U2-13 maintains a low output. When operating in the squelch mode, after the squelch is open, hysteresis of the squelch control circuit holds squelch open unless the receive signal level decreases below the level where it opened by 2 to 8 dB. The hysteresis keeps the squelch from opening and closing rapidly at a low level input.

h. Automatic Gain Control. AGC is developed by the detector internal to U3. This AGC controls the amplitude of the 30.1 MHz IF amplifier stages and a delayed AGC voltage is also output at U3-5 to U4C. The output of U4C is routed to the AGC inputs of the MOSFET RF amplifiers. Zener diode CR43 sets a voltage point so that the MOSFET AGC voltage can not be decreased to a point that damages the MOSFETS. During operation, AGC voltage measured at J3-11 is maximum (approximately +2.4 Vdc) during low signal conditions and minimum (approximately +2.1 Vdc) during high signal conditions.

4-8. GUARD RECEIVER ASSEMBLY A1A1A5. A block diagram of the guard receiver is contained in figure 4-3. The guard receiver detailed schematic diagram is contained in FO-10 at the rear of this manual. The guard receiver is tuned to the international UHF guard frequency of 243.000 MHz. Oscillators internal to the guard receiver produce 30.1 and 1.713 MHz IF frequencies. Gain through the first IF amplifier stage is between 16 and 18 dB. Cipher audio passes through the guard receiver but does not receive buffering or amplification. The transmit sidetone is amplified and placed on the common output line. Audio produced by the main receiver is input at J3-20. This audio is summed with the guard audio. The guard receiver provides two audio outputs; fixed audio and audio that is adjusted by the RT front panel OFF/VOLUME control. When the RT is in clear transmit mode, the guard receiver

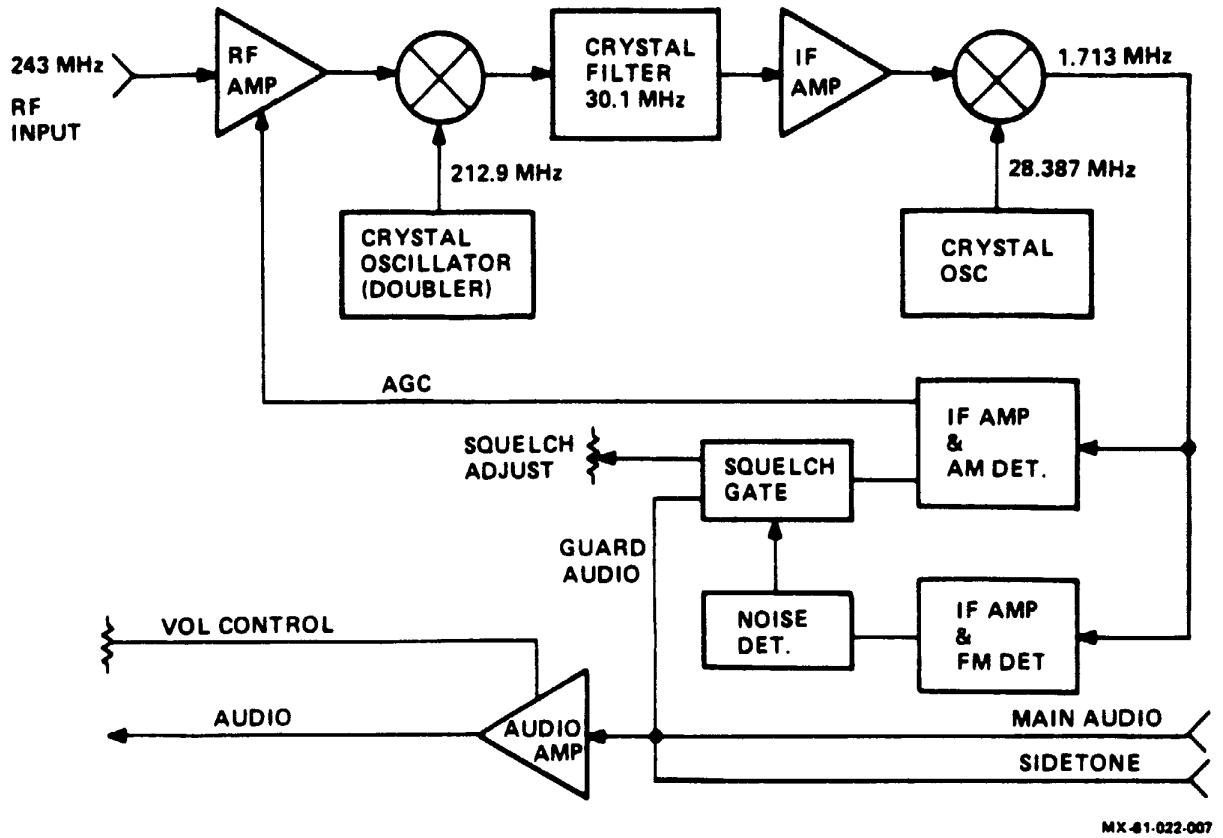


Figure 4-3. Guard Receiver Assembly A5 Block Diagram

provides the audio amplifier for the transmit sidetone. The following subparagraphs provide a detailed discussion of the guard receiver theory of operation.

a. Data Latch. The data latch is an 8 bit addressable data latch similar to the data latch of the main receiver. However, in the RT-1319/URC only the data from U1-11 controls the off-on selection of the guard receiver and U1-10 controls the output to remote control units connected to the RT REMOTE connector. Other outputs are terminated by resistors. The address for the data latches are the same as those contained in table 4-1. The guard receiver is on a high present at the output of U1-11. A high at U1-10 enables the audio out at J3-14 to be varied by the front panel OFF/VOLUME control. A low at U1-10 disables the front panel volume control and applies the maximum output to J3-14. As in the main receiver, a low on the guard receiver strobe enables the data latch write function and the data written into the addressed latch is the same state as that present on the RT data bus (RT DB0).

b. RF Amplifier. The RF amplifier consists of the tuned components and circuitry of Q1. Q1 is a n-channel enhancement mode MOSFET turned on when power is applied through Q4. This occurs when a logic high is latched through U1-11 and to the base of Q5. This high causes Q5 to conduct and turn on Q4 and switches the +12 Vdc source voltage on. Gain of the amplifier is controlled by delayed AGC voltages through R4. The tuned output of Q1 is through C14 to the MOSFET mixer. Mechanical tuning of the RF amplifier is accomplished by input tuning adjustment L3 and output tuning adjustments L6, L7 and L10.

c. MOSFET Mixer. The mixer is turned on by the switched +12 Vdc through R18, R20 and R24. MOSFET Q3 is connected to the output of the RF amplifier at gate input Q3-3 and to the output of the oscillator doubler at gate input Q3-2. The output of Q3 is through a tuned tank circuit that is adjusted by C29 to be resonant at 30.1 MHz. The output from the tuned tank goes through C20 to a crystal filter.

d. Oscillator Doubler. The circuits of Q9 provide a crystal controlled oscillator doubler. Crystal Y1 is resonant at 106.45 MHz. The output of this oscillator stage is tuned to twice the crystal frequency a mixing frequency of 212.90 MHz. The oscillator tuning adjustments are L11 and L12.

e. IF Amplifier Detector. The 30.1 MHz IF is fed to IF amplifier -AM detector U5-18. Internal to U5, the IF is amplified and then interstage coupled through U5-3 to U5-4 to a second on-chip amplifier stage. The output at U5-6 is routed to U6-16. The IF from U5 is mixed with a crystal controlled oscillator frequency of 28.387 MHz and produces a second IF of 1.713 MHz. The second IF is returned to U5-13 and applied to an AM detector circuit. The detector produces the audio that is applied to squelch gate U7B-12. The delayed AGC that controls the gain of MOSFET Q1 is applied to U7-2. Zener diode CR6 sets a voltage point so that the MOSFET AGC voltage can not be decreased to a point that will damage the MOSFET.

f. Squelch Control Circuit. Squelch voltage is detected noise products filtered by R73, C78, C79 and C80. During a high noise (low receive signal level) the output from U6-11 is high and a voltage is rectified by CR8 and CR7. Capacitor C76 is charged to a positive potential and this voltage is sensed at U7A-6 and inverted so that the output at U7A-7 is low. As the noise decreases because of higher signals at the antenna, it produces a negative going voltage and C76 will begin to discharge. This causes a negative going voltage at U7A-6, and when the threshold adjusted by R72 is overcome, the voltage at U7A-7 goes positive. This positive voltage forward biases CR10 and rapidly discharges C46 and applies a positive voltage to the squelch triggering circuit on U6-12. This positive voltage causes components within U6 to switch from a saturated state to a high impedance state. This high impedance removes the ground that is connected between U6-15 and U6-14 so it can no longer ground U7B-12. Audio then present at U7B is amplified and sent to the summing amplifier through C55 to U7D. Hysteresis of U6 causes the squelch to remain open until the input signal has decreased to 2 to 8 dB below the level where the squelch opened.

g. Audio Summing Amplification. Audio from the main receiver is input at J3-20 and is combined with the audio from the guard receiver at U7D-9. The amplified audio is sent from U7D-8 to U8C and to J3-9. U8C and U8D amplify the audio and route it to J3-2 as fixed audio at a level of approximately 0.8 Vrms. The audio routed to J3-9 is applied to the high side of the front panel OFF/VOLUME control adjustment and the wiper arm of this adjustment returns the adjusted audio to U8B for amplification. The adjusted audio is then routed through J3-14 and subsequently to the AUDIO connector at the front of the RT. When operating in the transmit mode, the sidetone developed in the modulator assembly is routed through the summing amplifier and then to the same circuits as plain audio.

4-9. MODULATOR ASSEMBLY A1A1A3. Figure 4-4 is a block diagram of the modulator assembly. The modulator detailed schematic diagram is contained in FO-8 at the rear

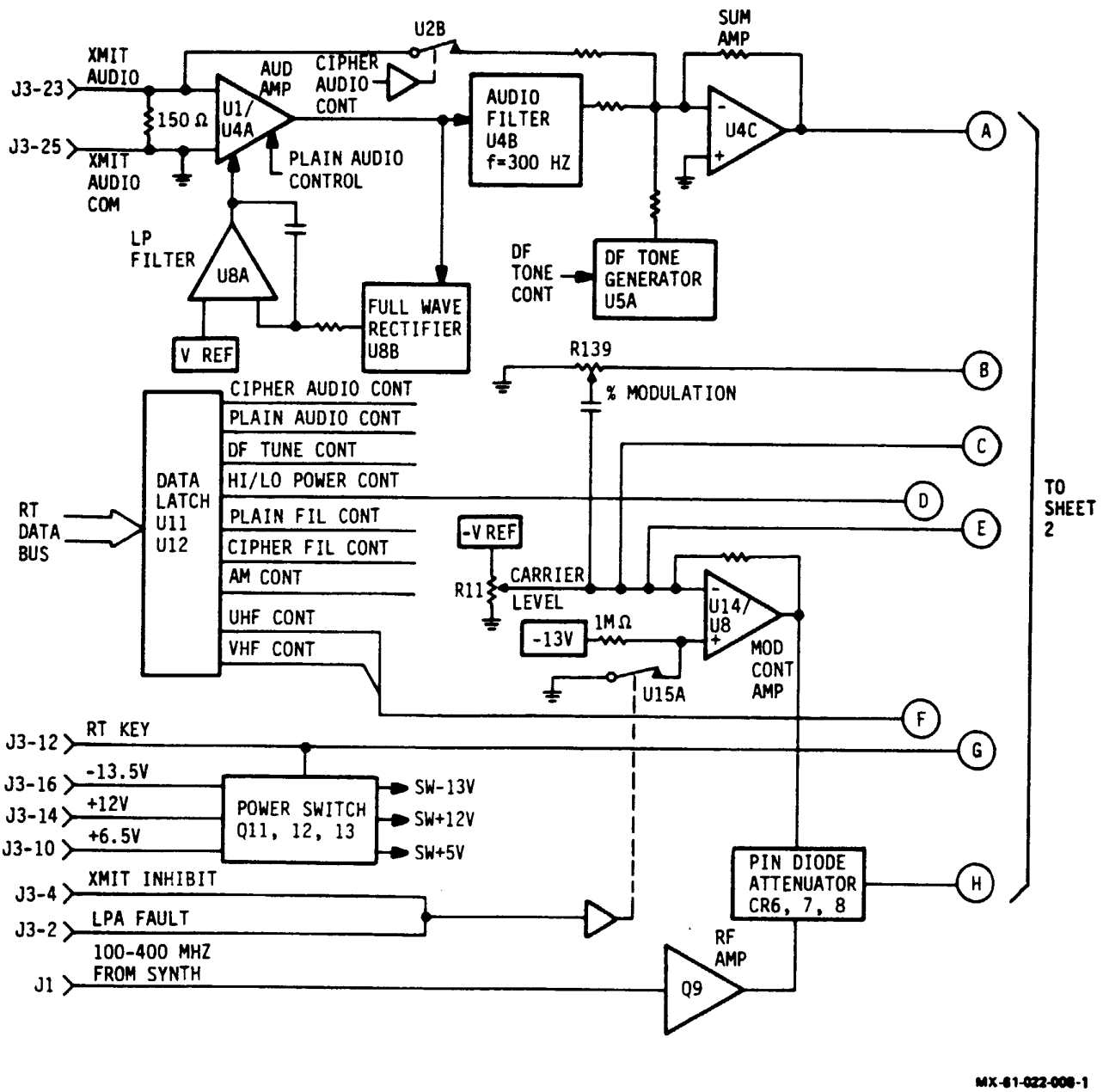


Figure 4-4. Modulator Assembly A3 Block Diagram (Sheet 1 of 2)

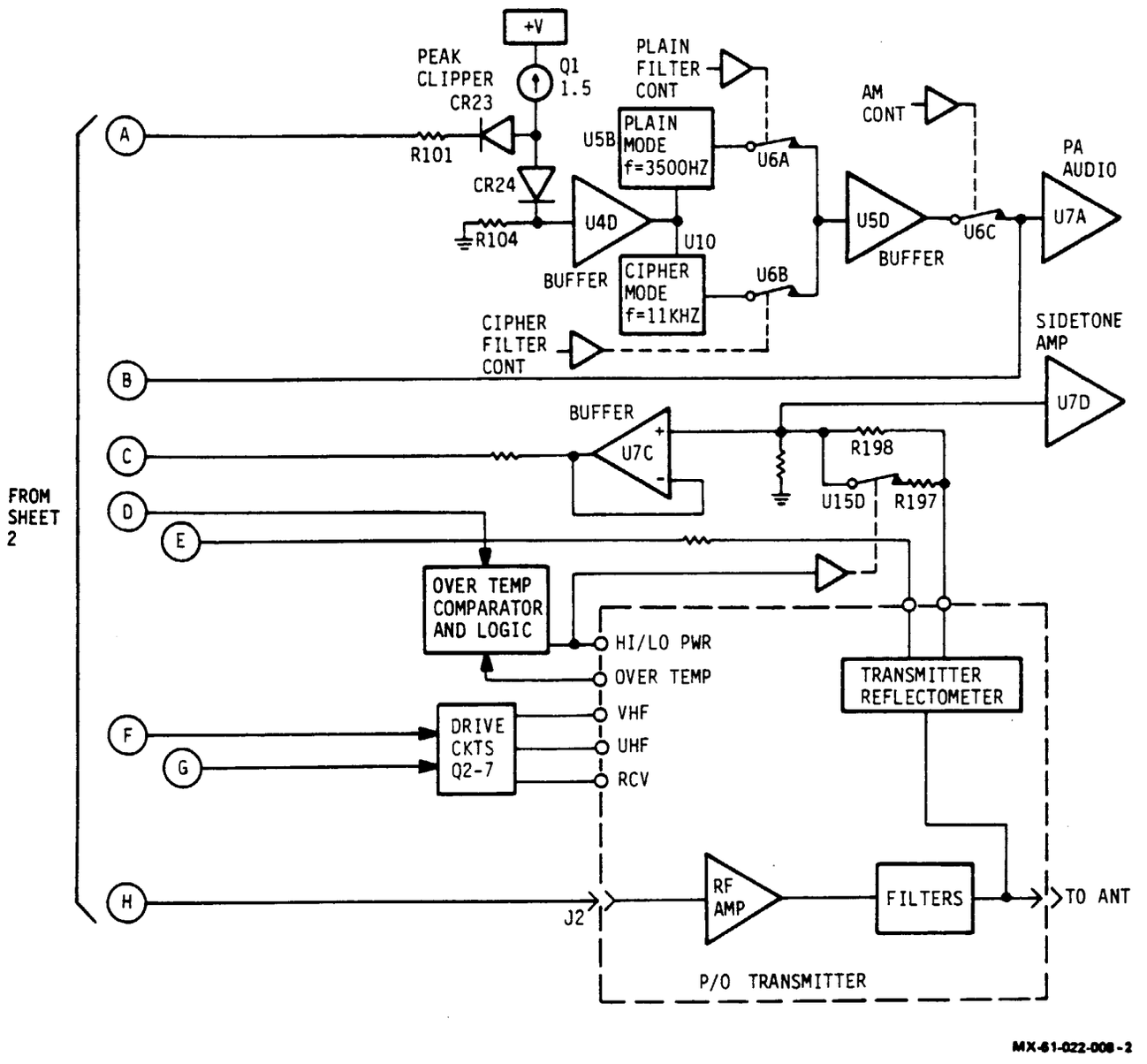


Figure 4-4. Modulator Assembly A3 Block Diagram (Sheet 2 of 2)

of this manual. Modulator assembly (1A1A1A3A1) modulates a CW carrier which produces an AM signal and controls the transmitter power output. For modulation the modulator uses integrated circuits and discrete components to condition the audio input, control the transmitter and compensate for variations caused by temperature, changes in drive level, reactance to frequency differences and termination. The modulator has two major modes of operation, transmit and receive. Operation of the modulator is almost totally dependent upon data converter software. This data, along with the state of the RT key line, transmit inhibit signal, forward and reflected power detector signals, and the thermal sensor within the transmitter defines the operation of the modulator. Controlling information, contained in several data signals, is input through two data latches (U11 and U12). Analog switches (U2, U6 and U15) that interconnect the control signals are operated to the closed position when switch control inputs are at a logic low. When used in an AN/VRC-83(V) an additional control signal (LPA FAULT) is used to momentarily disrupt the RF transmit functions while bypass switching occurs. Conditioning of the audio (impedance matching, compression, amplification, and clipping) and action of the ALC circuitry maintains the modulation of the synthesizer generated carrier to a modulation index set by manual adjustment of carrier and modulation level. Transmitter protection is accomplished by reducing drive to the transmitter when high VSWR and temperature is sensed. Internal oscillator circuits produce signals for special transmit functions such as direction finding (DF). The dc signal representing forward power from the transmitter also contains audio components which the modulator uses to produce the transmit AM sidetone during clear (nonsecure) operation and to guarantee the modulation envelope is an exact reproduction of the transmit audio signal. When in the transmit mode (RT keyed), should a change of parameter such as frequency or power level be input from the data converter, an accompanying XMIT INHIBIT signal attenuates the carrier to nearly zero to prevent damage or inadvertent interference.

a. Transmit Mode Power Circuits. When the RT key is low, RT key is a logic high and the transmit mode is set. In the receive mode of operation, +12, -13.5 and +5 Vdc are switched off to conserve the RT batteries. Circuits that must be kept alive (PIN diode drive, data latches and the peak limiter circuit Q1 and U4) are powered by unswitched power. The -29 Vdc and +24 Vdc are not switched. In the transmit mode, power switches (Q11, Q12 and Q13) are turned on by the low provided by the RT key line. The power switches are insulated gate n-channel enhancement mode MOSFETs. These exhibit very low resistance when the gate voltage is approximately 5 volts more positive than the source voltage, and a very high resistance when the gate and source voltages are nearly the same. The gate voltage of Q11 and Q12 is controlled by Q10, and will be approximately zero volts in the receive mode and approximately +24 Vdc in the transmit mode. The gate voltage for Q13 is controlled by Q12 and Q14. In the receive mode, the source voltage of Q12 is less than +2 Vdc and Q14 is turned off. This causes the gate voltage of Q13 to approximately equal the source. When entering the transmit mode, the source voltage of Q12 approaches +12 Vdc which turns Q14 on and drives the gate voltage of Q13 to about +11 Vdc and turns Q13 on.

b. Data Latches. Table 4-2 lists the address of U11 and U12 latches, the interfaced device and the signal designation. U11 and U12 are eight bit addressable data latches. The latches are configured with the reset at pin 2 at a constant low. Data may be written into the latches only when WRITE DISABLE is toggled from high to low by the modulator strobes (MOD STB 1 or MOD STB 2). Strobes are a momentary signal which enables data contained in the addressed latch to be changed. Data entered in

Table 4-2. Data Latch Address Codes

Latch output	Address state A2	A1	A0	Selected device/signal
PIN 9	L	L	L	U11 UHF CONTROL U12 10W/2W CONTROL
PIN 10	L	L	H	U11 VHF CONTROL U12 NOT USED
PIN 11	L	H	L	U11 Not used U12 Not connected
Pin 12	L	H	H	U11 PLAIN FILTER CONTROL U12 DF TONE CONT
PIN 13	H	L	L	U11 CIPHER FILTER CONTROL U12 AM SIDETONE CONTROL
PIN 14	H	L	H	U11 Not used U12 CIPHER AUDIO CONTROL
PIN 15	H	H	L	U11 AM CONTROL U12 PLAIN AUDIO CONTROL
PIN 1	H	H	H	U11 Not connected U12 Not used

NOTE: L=LOW (<0.4 Vdc), H=HIGH (>4.0 Vdc).

the latches has the same logic state as the state of the data present at RT DB 0. (If the data on the bus is high, the addressed latch accepts the high as its operating output.)

c. RF Amplifier. The carrier signal generated by the synthesizer is fed to modulator RF input J1 at approximately +9 dBm. Amplifier Q9 has a gain of approximately 12 dB. With the pin diode attenuator set for minimum attenuation, and +9 dBm injected at J1, the amplifier will produce an output at J2 of +21 dBm(min). L8, C18 and R37 in conjunction with C17 and R30 through 33 produce an input impedance of approximately 12.5 Ohms over the frequency range of 100 Mhz through 400 MHz. Transformer T1 transforms this to 50 Ohms at J1. VSWR is less than 2:1 across the band when J2 is terminated into 50 Ohms.

d. ALC Loop. Functional theory of U14 is given in detail to aid technicians in understanding a primary controlling circuit of the RT. Voltage and current values are theoretical, but are approximately those that would occur during normal operation with high power (10 watt) when the output from the transmitter is terminated into 50 Ohms.

(1) Modulation Control Amplifier. U14 is a inverting operational amplifier which amplifies and inverts any difference in potential between pins 2 and 3.

A negative feedback path is provided from the output at U14-6 through R2 to U14-2. This feedback cancels or balances any voltage difference between pins 2 and 3. During normal operation, U15A is closed and U14-3 is at ground potential. Therefore, feedback causes U14-2 to be a virtual ground. If U14-2 is considered as a current node and U14 has high input impedance, current flow through any resistor connected to U14-2 will be the quotient of voltage applied to that resistor, divided by its resistance. For the purpose of this description, assume the following conditions; R11 is set at a point that produces 706 mVdc at the wiper arm, reflected power is 0 Vdc, and the wiper arm of R139 (modulation adjustment) has 0 Vdc. This 706 mVdc is the carrier reference voltage and determines the carrier reference current (126 microampere) into the node of U14-2. Normal 10 watt output from the transmitter produces approximately +1 Vdc input from transmitter reflectometer at J3-19. U15D is open and the voltage drop (R198, R210) develops approximately 117.6 mVdc at the input of U7C. U7C is a unity gain, noninverting, buffer amplifier and its output will be 117.6 mVdc. This 117.6 mVdc, through R8, will produce 117.6 microampere. This results in a deficiency of 8.5 microampere of current between that set by R11, and that entering the node through R8. The negative feedback loop, to equalize the node, has 8.5 microampere of current flowing through R2. This produces +4 Vdc at U14-6. This bias to the base of Q8 then sets the value of bias on the pin diode attenuator circuit. Any decrease in forward power increases the deficit current. This, in turn results in increasing voltage at Q8 in a positive direction, increases the drive to the pin diode circuits and causes the carrier to be attenuated less. All changes that occur are extremely fast and results in a output power level that appears constant to most power measurement instruments.

(2) Reflected Power Input. An increase in reflected power would have approximately the same effect as an increase in forward power above that set by carrier adjustment R11. Reflected power detected by the transmitter reflectometer is routed through J3-21. This voltage, when correct termination of the transmitter output exists, is 0 Vdc. When reflected power increases, the voltage at J3-21 increases. This reduces the current deficit and current though R4 decreases. This produces a decrease in positive potential at U14-6, and Q8 decreases in conduction. Such a condition changes the bias of the pin diode attenuator network to increase the amount of attenuation to the RF signal. (Reflected power which produces a representative dc of +300 mVdc results in output power reduction of approximately 3 dB.)

(3) Modulating Audio. Modulating audio is external to the ALC loop and is similar to the variable voltage setting of R11. The variations caused by the audio produces the same effect that occurs if R11 could be made to rapidly vary the carrier reference adjustment. Voltage variations cause changes in the U14-2 node at an audio rate. This produces changes to the base of Q8 at the same rate and results in amplitude modulation of the injected carrier. Conditioning of the input audio amplitude to R3 determines the percent of modulation and is discussed in subsequent subparagraphs.

(4) High Power/Low Power Operation. The reference carrier voltage established by R11 remains the same during high or low power transmit. A high power-low power signal from comparator U9B is sent to the transmitter which selects the gain of transmitter stages. During low power, gain of the transmitter is lowered by 7 dB. Switch U15D is closed which prevents the ALC circuit from detecting low power selection as an error. This places R197 in parallel with R198 which decreases the forward power signal voltage drop and provides approximately the same voltage at

R210, U7C and R8 as is present in high power. R195 and C80 are also switched to adjust the ALC loop audio gain while operating in the low power mode.

e. PIN diode Modulator/Attenuator. The amplified RF signal is coupled to the pin diode attenuator through L6 and C15. The pin diode circuit attenuates the RF signal and produces carrier amplitude modulation and transmitter power control. The output is coupled through C16 to J2 to the transmitter assembly. The dc current through CR6, CR7 and CR8 varies the attenuation of the carrier. The bias state of CR6 and CR7 is inverse to the bias state of CR8, e.g., if conditions cause the series resistance of CR6 and CR7 to increase, the resistance of CR8 will decrease and provide a lower shunt resistance to the carrier. This permits more of the carrier to pass through R29, C19, CR8 and C20 to ground. During normal operating conditions, there is approximately +4 Vdc at the anodes of CR6, CR7 and the cathode of CR8, and approximately +4.5 at the anode of CR8. Therefore, CR8 presents a relatively high impedance during normal operation.

f. Overtemperature Protection. U9A is a comparator circuit with hysteresis. The transmitter assembly contains a thermistor that is connected electrically between ground and J3-13 of the modulator. The thermistor is 8000 Ohms at 25 degrees C and decays nonlinear to about 700 Ohms at 85 degrees C. When the thermistor value is 8000 Ohms, voltage division from -13.5 Vdc through R215 to the thermistor provides about -6 Vdc at U9-3. The dc voltage at U9-4 is dependent upon the output voltage at U9-1 and the voltage division from -13.5 through R214 and R212. Since there is no negative feedback, the output at pin 1 will be either +11.0 Vdc or -12.5 Vdc. If pin 1 is at +11.0 Vdc, the voltage at pin 4 is approximately -1.0 Vdc. If pin 1 is at -12.5 Vdc (CR34 now forward biased), the voltage at pin 4 is approximately -1.5 Vdc. The -6 Vdc potential at U9-3 causes U9-1 to be +11.0 Vdc, and both CR35 and CR36 are reversed biased. This permits the high/low power signal to assume either state. This is true so long as the dc voltage at U9-3 is more negative than the voltage at U9-4. As the thermistor heats up (resistance decaying), a point may be reached where the voltage at U9-3 is less negative than U9-4. When this occurs, the output from U9 switches from +11.0 Vdc to -12.5 Vdc and the voltage at pin 4 shifts from -1.0 Vdc to -1.5 Vdc. CR35 and CR36 are forward biased and the comparator U9B is forced to the low power state. The transmitter remains in that state so long as -12.5 Vdc is present at U9-1. As the transmitter cools and the thermistor increases in resistance, U9-3 would become more negative. However, the hysteresis of the circuit establishes that it must become more negative than -1.5 Vdc before U9-1 can reassume the +11 Vdc level and the transmitter return to high power. It should be noted the transition between low power and high power caused by temperature is not controlled by the data converter and will not be indicated on the LCD display.

g. Audio Signal Processing. The three sources of audio which modulate the carrier are plain text audio from a handset, cipher text audio from a COMSEC device and internally generated tones (i.e., DF tone). The following description pertains to plain text, the most complex form of modulation. The plain audio is direct from a handset/headset and the volume is a result of how forcefully and directly the operator speaks into the microphone. To compensate for the varying input levels an audio compression amplifier, a symmetrical peak clipper and premodulation filters insure consistent modulation. U1, U4A, U8A and U8B make up the compression amplifier. These circuits maintain the audio voltage at U4A-7 at approximately 1.3 Vrms while audio present at J3-2 may vary from 1.5 mVrms to 45 mVrms.

(1) Input Amplifier Stages. U4A has a fixed gain of about 17 dB. U1 is an operational transconductance amplifier. That is, the gain of U1 is controlled by the dc current at U1-5. This is established by circuitry of U8. The gain of U1 will vary from 40 dB with a low audio input to 10 dB with a high audio (45 mVrms) input. Inputs greater than 45 mVrms also results in further reduction of gain, however audio distortion may become objectionable.

(2) Compressor Rectifier. U8B is a precision full wave rectifier. To understand its operation, assume that the junction of R74 and R78 is ground. On the positive portion of the audio signal coupled through C39, current (I1) flows from ground through R74 and its magnitude is +E/10.2 Kilo-Ohms. The current through R78 (I2) is zero because U8B inverts the audio signal, reverse biasing CR14. At the same time, CR15 is forward biased and the voltage at U8B-3 is a virtual ground. When the audio signal at the junction of R74 and R80 is on the negative half cycle, current through R74 is of the same magnitude as in the positive cycle, but has the opposite polarity. However, under this condition current through R78 is not zero, but the quotient of +E/5.1 Kohms. The inversion by U8B now forward biases CR14 and reverse biases CR15, making the circuit a unity gain inverting amplifier (R79=R80). The net current flowing in the assumed ground node at the junction of R74 and R78 is -E/10.2 Kilo-Ohms plus E/5.1 Kilo-Ohms or +E/10.2 Kilo-Ohms; the same as in the positive half cycle. The current flowing at the junction of R74 and R78 is a result of the full wave rectification of the voltage at the junction of R74 and R80. The junction of R78 and R74 is not ground, but a virtual ac ground with a +0.6 Vdc offset. This does not change the operation as previously described, except the magnitude of the rectified current flowing is not a function of E but is a function of E minus + 0.6 Vdc.

(3) Compressor Integrator. U8A converts the rectified current pulses from U8B into a dc level proportional to the average magnitude of the pulses. During the following discussion, assume that U8 pins 6 and 7 are at +0.6 Vdc and pin 9 is at -6.0 Vdc. As current begins to flow from the junction of C43 and U8-7 toward R74 and R78 during the rectification process, voltage across C43 must start to increase. This causes U8-9 to become more negative and the voltage at U8-7 becomes more positive, creating a voltage difference between U8 pin 6 and pin 7. This difference is amplified and inverted and drive the amplifier output (U8-9) more positive. Since U8-9 was attempting to go in the negative direction, it in reality does not change at all, i.e., a dc level. Because the dc voltage across C43 is a function of the average current through it and U8 pins 6 and 7 are always at +0.6 Vdc, as the rectified current level increases due to the audio voltage at U4-7, the dc voltage at U8-9 will become more negative, current draw from U1-5 becomes smaller and the gain of U1 decreases. When this occurs, the voltage at U4-7 then is returned to the original value. Note that the gain of U1 is adjusted by the loop to cause dc voltage at U8A-7 to equal the dc voltage on U8A-6. Therefore the voltage of U4A-7 can be of any value desired (within the capabilities of the loop) by changing the dc voltage at U8A-6. Though response of the loop is rapid, there is enough delay to permit compression without causing loss of audio amplitude variations.

(4) Compressor Regulation. In theory, if the RT is keyed and no audio signal is present, in order that the voltage at U8 pins 6 and 7 be equal, compressor action could attempt to increase the gain of U1 to an extremely high level. Voltage at U8-9 would rise to +12.0 Vdc and delay would be encountered when audio is reapplied

while the voltage at U8-9 declined to the normal point of operation (-7.0 Vdc). Q15 prevents this condition and holds the output at -5.0 Vdc with no audio present. With the voltage at U8-9 more negative than -6.0 Vdc, the -5.0 Vdc on the emitter of Q15 keeps it cut off. With the voltage at U8-9 less negative than -6.0 Vdc, Q15 will conduct and maintain a constant negative potential until audio is reapplied.

h. Filtering and Summing Amplifier. U4B is an active high pass filter with 250 Hz at the 3 dB bandpass point. Signals above 600 Hz are passed at unity. The output of the filter is applied to U4C which has unity gain to the plain mode audio signal. U4C feeds the symmetrical peak clipper Q1.

i. Peak Clipper. For the purposes of this description, consider Q1 as a constant current source, and the magnitude of its output current through R102 a function of the value of R100. In the absence of an audio signal, the output of U4C-14 can be considered dc ground and as such, the current supplied by Q1 through R102 divides evenly between the two paths; CR23 and R101, CR24 and R104. The voltage from the junction of R104, CR24 and C50 to ground is the output voltage of the clipper. With no audio input, it is equal to the voltage drop across R101, or +0.75 Vdc. When an audio signal is present at the output of U4C, during the positive half cycle, as the voltage at U4C rises, the voltage drop across R101 decreases and less current flows through R101. Since the current flowing through R102 is constant, more current flows through R104, and the voltage drop across R104 increases. The signal appearing across R104 is exactly like that appearing at U4C-14, except the amplitude is reduced by approximately one half. A point is reached when the positive voltage at U4C-14 is of a magnitude to reverse bias CR23. When this occurs, no current flows through R101 and all the current supplied by Q1 through R102 flows through R104. This causes the voltage across R104 to be twice the original magnitude, or +1.5 Volts. Should the voltage at U4C-14 continue to rise even as high as +10.0 Volts, voltage across R104 remains at +1.5 Volts. During the negative half cycle, a similar action occurs, except CR23 remains forward biased and CR24 ultimately becomes reverse biased. This causes current to cease to flow through R104 and the clipper output is 0.0 Volts though audio at U14C could decline to as much as -10.0 Volt. Neglecting diode voltage drops, any signal appearing at U4C-14 of less than 3 volt peak-to-peak will pass through the clipper stage unaffected except for an amplitude reduction of one-half. Any signal greater than this is limited to 1.5 Volts peak-to-peak. During plain text operation, R77 of the compressor circuit (value selected during test) sets the compressor operating point so that with a normal audio level input, clipping is barely noticeable at J4-4. The compressor amplifier maintains this audio level over a wide range of input voltages with minimum distortion due to limiting. Sudden transients are positively limited and overmodulation of the carrier is prevented. To reduce harmonic distortion that could result from clipping action, the output of the clipper is routed to two active filter circuits. The plain mode filter is U5B and the cipher mode filter is U10.

j. Plain Mode Premodulation Filter and Amplifier. During plain text operation U6A is closed and U6B is open and U5B is selected. U5B is a low pass filter with a 3 dB frequency of 4 kHz, unity gain below 2 kHz and 18 dB per octave roll off above 6 kHz. The filtered audio output is routed through U6A to buffer amplifier U5D. U5D provides approximately 6 dB of gain and isolates the filter output from the modulation level adjustment, R139. The wiper of R139 supplies audio signals to the ALC loop through R3 to modulate the carrier as previously discussed. Normal adjustment of R139 sets a level of 88% negative modulation in the plain mode of operation.

k. External Audio Output. Amplifier U7A provides a sample of the modulation audio to J3-29 (LPA XMIT AUDIO) for use by external equipment. When J3-29 is loaded by 5 Kilo-Ohms to ground, the output is measured at 0.8 Vrms. U7A is linear over a wide range of frequencies and is used as a test point to sample the modulating audio prior to the modulation process.

l. DF Tone Generation. U5A is a Wien-bridge audio oscillator circuit. C42, R76, C41 and R75 determine the frequency of the oscillation. CR16 and CR17 limit the oscillator loop gain as a function of peak-to-peak output voltage, and provides a means of turning the oscillator on and off. With the DF tone control line low, R83 is effectively connected to ground. The two diodes, CR16 and CR17 are reverse biased through voltage dividers R82, R83, R84 and R85. With the output at U5A high enough, one of the two diodes begins to conduct, limiting the magnitude of positive feedback to make overall gain of the system unity. With the DF tone control signal high, CR16 is forward biased putting a positive potential on U5A-3. This drives the output to approximately +8 Vdc and the oscillator is turned off.

m. Cipher Operation. Cipher mode does not require the precise amplitude control of plain mode since the intelligence is transmitted by a series of ones and zeros. However, cipher mode requires a wider bandwidth (10 Hertz to 11 kHz). During cipher operation, U2C is closed which connects -5 Vdc to U4-5. This drives its output into the negative power supply rail and prevents any audio signal from passing through the amplifier. The cipher path gain is set so that the smallest input signal from the external device causes clipping as discussed previously in paragraph i. Cipher mode uses the low pass filter U10. Switch U6B is closed, and switch U6A is open. This filter has unity gain (within 1 dB) from dc to about 7 kHz. The 3 db frequency is at about 11 kHz, and theoretical roll off continues to -66 dB at 50 kHz. The filter has near linear phase shift with frequency. At 10 kHz, the phase shift from input to output of the filter is about 180 degrees with 0 degrees at dc.

4-10. TRANSMITTER ASSEMBLY A1A1A2. Figure 4-5 provides a block diagram of the transmitter assembly. The schematic diagram for the transmitter and reflectometer is contained in FO-7 at the rear of this manual. The transmitter assembly consists of transmitter circuit card assembly A1, reflectometer A1A1 and a mounting bracket for RF power amplifiers Q1, Q3 and Q4. The transmitter A1 contains RF switching networks, output low pass filters and a temperature sensor circuit. The reflectometer A1A1 contains circuits to develop sidetone signals, forward and reflected power samples and transmit-receive (T-R) antenna switching. The following sub-paragraphs present a description of the theory of operation of the transmitter.

a. Driver Amplifier Circuits. The driver amplifier circuit amplifies the modulated RF signal (approximately 25 mW) from the modulator to the two watt level. This power gain is accomplished with two broadband RF power amplifiers, Q1 and Q3. The modulated RF signal is applied to J1 (RF IN) and routed to Q1 through impedance matching transformer A1T1. The RF gain of Q1 is 10 dB. The RF output from Q1 is applied to Q3 input through a low pass filter and impedance matching transformer A1T2. The gain of Q3 is 10 dB. Base bias voltage for both Q1 and Q3 is established with diode A1CR1. The bias voltage is derived from the current used to switch the 2 watt or 10 watt select pin diodes (CR5, CR6, CR7 or CR8). The collector supply for both Q1 and Q3 (switched +24 Vdc) is routed from J4-8/10. The RF output from Q3 is applied to the power selection circuit through impedance matching network L7, L8, L9, L11, C16, C17 and C19. During VHF transmissions, Q2 provides a shunt current

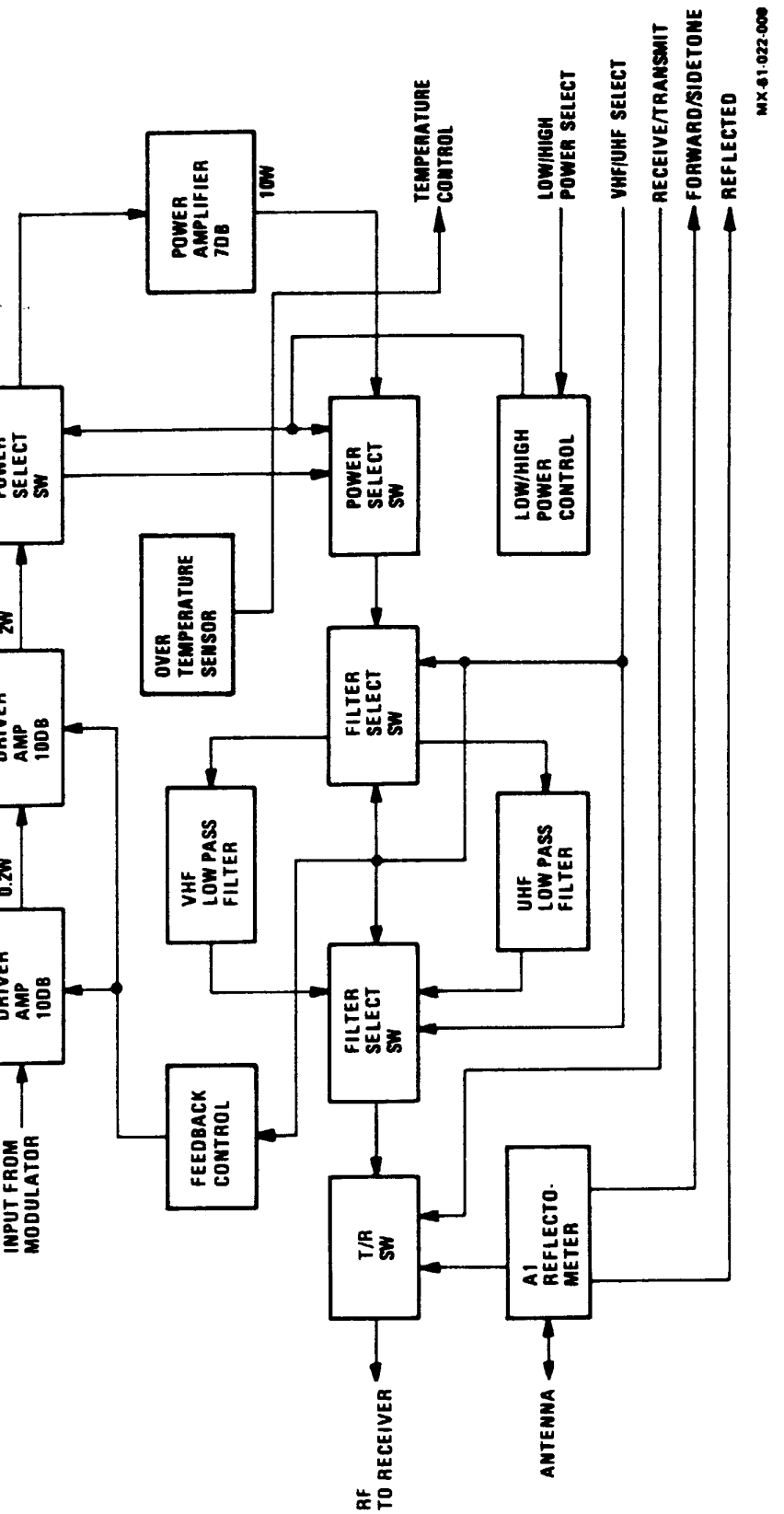


Figure 4-5. Transmitter Assembly A2 Block Diagram

path to forward bias pin diodes CR2 and CR3. This provides negative feedback to Q1 and Q3 bases and maintains a constant RF power gain in VHF mode. To accomplish this, the modulator applies a high control signal (+6.3 Vdc) to J4-5 (VHF PIN DRIVE). This forward biases diode CR4 which provides turn on bias for Q2.

b. Power Level Selection. The selection of low (2 watt) or high (10 watt) modes of operation at the front panel and the status of the transmitter temperature sensor circuit determine the low/high power signal state at J4-3 (-10.0 Vdc for 2 watt mode or +6.3 Vdc for 10 watt mode).

(1) Low Power Mode. During the low power mode, -10.0 Vdc at J4-3 forward biases diode CR22 and switch driver Q5. Collector supply for Q5 (-29.0 Vdc) is routed from J4-16. When Q5 switches on, its collector voltage raises to +3.5 Vdc and forward biases pin diodes CR6 and CR7. This provides a signal path that routes the driver amplifier (Q3) RF output to the filter selection circuitry. Switch driver Q5 emitter is the current sink for the filter selection circuitry.

(2) High Power Mode. During the high power mode, +6.3 Vdc at J4-3 forward biases diode CR23. The voltage developed across resistor R42 (+1.0 Vdc) biases on Q7. Transistor Q7 provides the forward bias current to turn on switch driver Q6. Collector supply for Q6 (-29 Vdc) is routed from J4-16. When Q6 switches on, its collector voltage raises to +3.5 Vdc and forward biases pin diodes CR5 and CR8. Pin diode CR5 provides a signal path that routes the driver amplifier RF output through balancing transformer T3 and an impedance matching network of power amplifier Q4. The output of Q4 passes through an impedance matching network, balance transformer T4 and pin diode CR8 to the filter selection circuit. Transistor Q4 is a broadband amplifier having a gain of 7 dB. Collector supply for Q4 (switched +24 Vdc) is routed from J4-8/10. Transistor Q4 operates without base bias voltage and inductors L20, L21, L48 and L77 are base current return paths. Switch driver Q6 emitter is the current sink for the filter selection circuit.

c. Filter Selection Circuit. Table 4-3 lists the pin diode drive signals. Pin diode drive circuits in the modulator control the selection of the UHF/VHF low pass filters in the transmitter T-R switch position. This is accomplished with high/low control signals (+6.3 Vdc or -29.0 Vdc) applied to pin diode switches in the transmitter. The UHF low pass filter comprises inductors L57 through L65 and capacitors C62 through C65. The VHF low pass filter comprises inductors L66 through L73 and capacitors C66 through C69.

Table 4-3. Pin Drive Control Signals

Operating mode	Control signals*		
	VHF pin drive (J4-5)	UHF pin drive (J4-7)	RCV pin drive (J4-1)
VHF Transmit	High	Low	Low
UHF Transmit	Low	High	Low
Receive	Low	Low	High

*Low = -29 Vdc, High = +6.3 Vdc.

(1) UHF Low Pass Filter Selection. During UHF transmit mode, J4-7 (UHF PIN DRIVE) is driven high and J4-5 (VHF PIN DRIVE) is driven low. The high on J4-7 forward biases pin diodes CR9, CR12, CR14 and CR15. Pin diode CR9 routes the RF signal from driver amplifier Q3 (low power) or from power amplifier Q4 (high power) through the UHF low pass filter. The RF signal is then routed through diode CR15 and coupling capacitor C81 to the reflectometer. Pin diodes CR10 and CR16 switch out the VHF low pass filter. Pin diodes CR11 and CR13 are reverse biased by -29 Vdc from J4-5.

(2) VHF Low Pass Filter Selection. During VHF transmit mode, J4-5 (VHF PIN DRIVE) is driven high and J4-7 (UHF PIN DRIVE) is driven low. The high on J4-5 forward biases pin diodes CR10, CR11, CR13, CR28 and CR16. Pin diode CR10 routes the RF signal from driver amplifier Q3 (low power) or from power amplifier Q4 (high power) through the VHF low pass filter. After filtering the signal is routed through CR16 and coupling capacitor C81 to the reflectometer/antenna. Pin diodes CR9 and CR15 switch out the UHF low pass filter.

d. Reflectometer and T-R Switch Circuits. The T-R switch connects either the receiver or transmitter circuits to the antenna circuits. The reflectometer samples both the forward and reflected power outputs levels. The samples are rectified, filtered and sent to the modulator where they control the modulator output level to the transmitter. The main line output from the reflectometer is applied to the antenna.

(1) Receive Mode. In the receive mode, J4-1 (RCV PIN DRIVE) is driven high (+6.3 Vdc) by the modulator assembly. This forward biases pin diode switch A1CR20. Incoming signals can now pass from J2 (ANTENNA) through A1CR20 and J3 (RCV RF) to the input of the guard receiver. The high RCV PIN DRIVE also switches on CR27 and CR14 to shunt out the VHF low pass filter and switches CR26 and CR13 to shunt out the UHF low pass filter. Diode CR24 and CR25 and their shunt resistor R23 and R27 respectively, prevent the RCV PIN DRIVE from setting the VHF and UHF PIN DRIVE signals high.

(2) Transmit Mode. In the transmit mode, J4-1 (RCV PIN DRIVE) is driven low (-29.0 Vdc) by the modulator assembly. This reverse biases A1CR20 prevents transmit signals from passing to the guard receiver. In effect, the antenna connection is removed from J3 (RCV RF). The low RCV PIN DRIVE signals also switches off diodes CR26 and CR27. At the same time, a high signal (+4.0 Vdc) from the filter selection current summing point of Q5 and Q6 emitters forward biases pin diode A1CR21. This puts A1CR21 in a low resistance state which protects the input stage of the guard receiver.

(3) Forward and Reflected Power. Forward and reflected power samples are sent to the modulator to maintain a constant power carrier level and a constant percent of modulation level and to develop sidetone signals. Electrical energy pickup off the RF output line is accomplished by inductors A1L42 and A1L43. Diode A1CR18 is the forward power detector. Capacitor A1C83 filters the detected RF voltage which is routed through J4-11 (FORWARD POWER) to the modulator. Diode A1CR17 is the reference and bias diode of A2CR18. The bias voltage is derived from one of the power switch drivers, Q5 or Q6 (dependent on power level selection). Reflected power is detected with diode A1CR19 through coupling capacitor A1C85. The reflected power sample is routed through J4-13 (REF PWR) to the modulator.

4-11. CONTROL/DATA CONVERTER ASSEMBLY A1A1A1. Figure 4-6 is the overall functional block diagram of the four CCA's contained in the Control/Data Converter Assembly (Data converter). Additional figures are provided with the description of the individual CCA. FO-1 through FO-6 at the rear of this manual contain the detailed schematic diagrams for the data converter assembly. The data converter assembly consists of four separate circuit card assemblies (CCA's); the A1 interface board, the A4 LCD board, the A2 memory I/O board and the A3 central processing unit (CPU) board. The following description is in this order since it most closely approximates the data sequence from basic keyboard inputs.

a. Data Converter Interface CCA A1A1. Refer to figure 4-7 and FO-3. Interface board A1 provides signal interface between the front panel mounted keyboard, memory I/O board A2 and LCD board A4. Interface board A1 includes the following circuits; a keyboard encoder, a display output port, an electroluminescent (EL) panel lighting control, and a LCD heater control.

(1) Keyboard Encoder Circuit. The keyboard encoder circuit consists of keyboard encoder U2, D-type flip-flop (FF) U3A and transistor Q1. The keyboard is a matrix of four rows and three columns. With a key depressed on the keyboard, a single row is shorted to a single column that corresponds to the position of the key. The keyboard is interfaced to interface board A1 via J3 (pins 4 through 10). The keyboard entries are fed to U2 which converts the keystroke inputs into a binary keycode. Once a keystroke is detected by U2, it toggles its data available line to clock the local/remote data available FF (U3A). The remote and local data available lines are combined by diodes CR1 and CR2 so that either source will cause FF U3A to be clocked. The output at U3A-1 flags the microprocessor (A1A3U14) that a keystroke is waiting for processing. The microprocessor will wait until it reaches the input portion of the program before it processes the keystroke. This may take as long as 120 milliseconds. Once the input portion of the program is reached, the microprocessor controlled chip select (CS1) signal at P1-24 goes high, Q1 conducts, and U2-13 (output enable) is forced low. This enables the output lines of U2 and keycode data is then sent on the data bus (P1-16, -18, -20, -22) for processing. Once the microprocessor has processed a keycode input, it sends eight lines (DB0 - DB7) of display and control data along the data bus to the display output port.

(2) Display Output Port. The display output port circuitry consists of octal D-type flip-flop U1 and comparator U4. The display output port receives eight lines of display and control data from the microprocessor. Six of the eight data lines (DB1-DB6) provide the necessary clock and data information to the displays. The remote lines (DB4-DB6) also double as outputs to a radio communication system when one of the appropriate modes is selected via the remote select lines of the front panel REMOTE connector. All clock and data lines (DB1-DB6) are active high and are kept in the low state when not in use. The two remaining lines (DB0 and DB7) are control lines. DB0 shuts off the keyboard/display backlighting regardless of the position of the dimmer control on the RT front panel. DB7 to resets the keyboard data available latch (U3A) after a keystroke has been processed. Data is latched into U1 by a low to high transition of the chip select input (P1-23) from the MNOS port decoder (A1A2U10). The effect of serial data streams is achieved by toggling only the desired bits in the 8 bit data word. The data converter is interfaced to the LCD drivers and compatible remote control units. Interfacing of data for the local display is accomplished via quad voltage comparator U4. U4 transforms the

TO 31R2-2URC-63

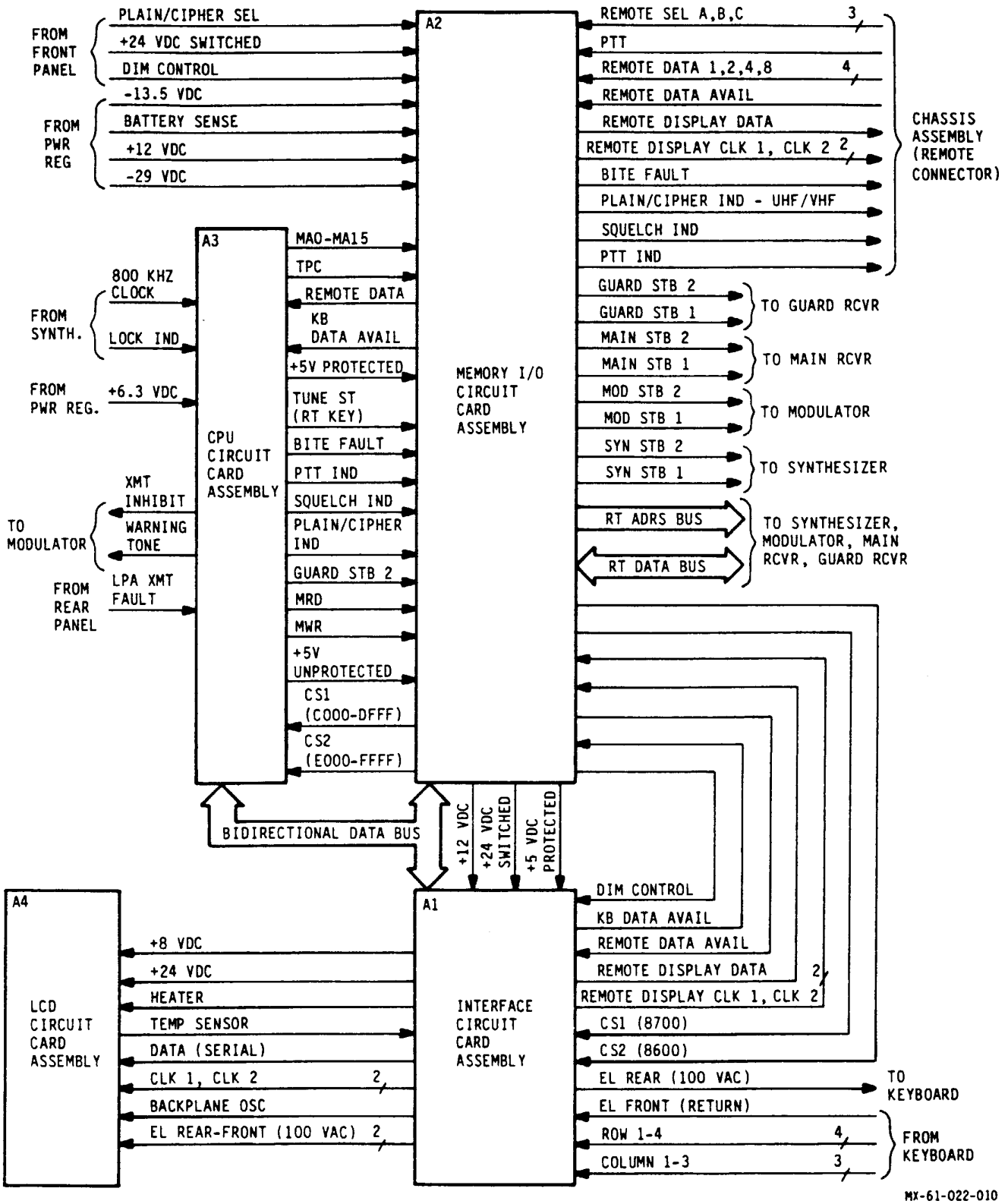


Figure 4-6. Data Converter Assembly A1 Block Diagram

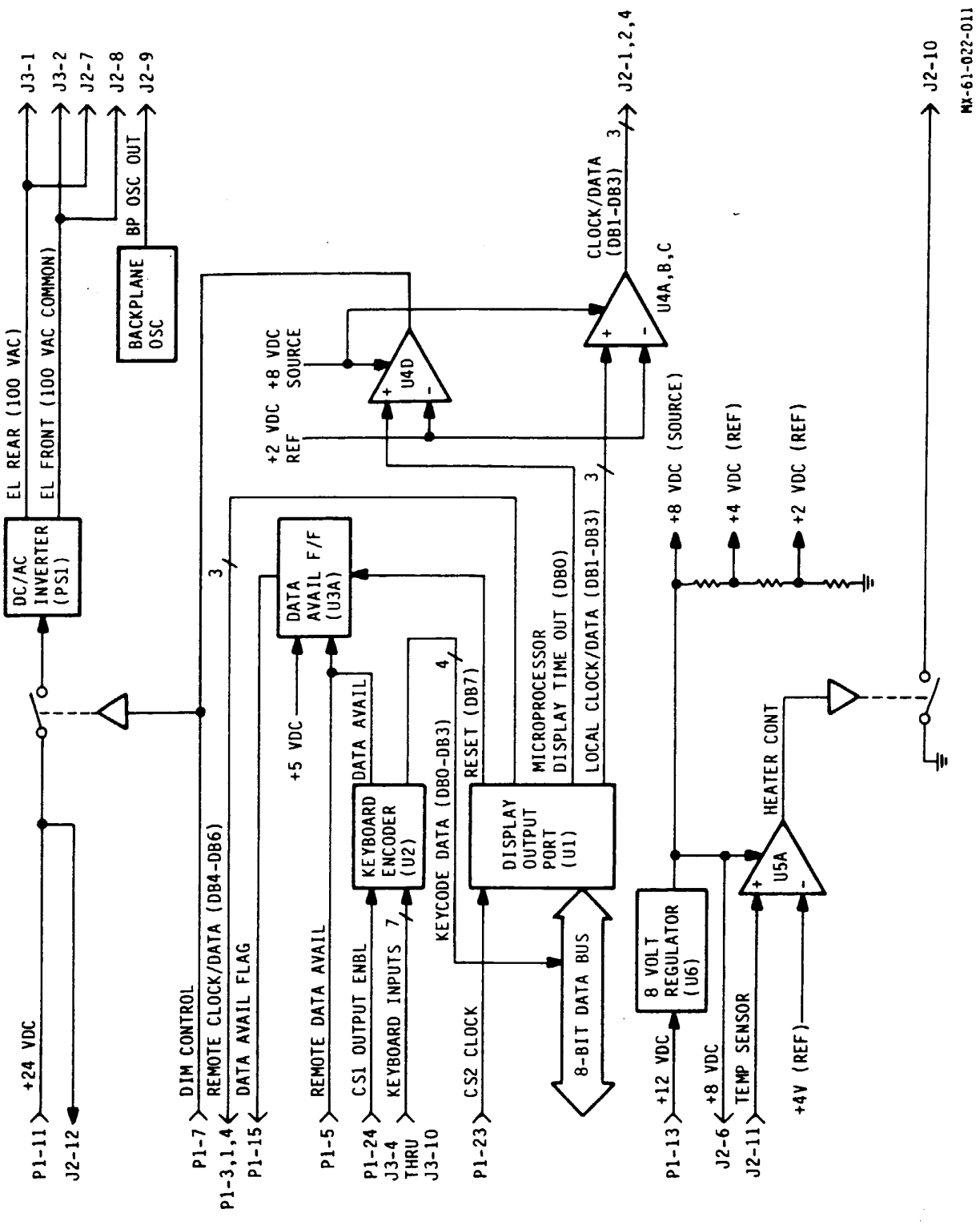


Figure 4-7. Interface CCA A1A1 Block Diagram

zero to +5.0 Vdc logic to zero to +8.0 Vdc logic. The +8.0 Vdc applied to the A4 board display drivers permits maximum resolution and viewing angles without overstressing the display drivers.

(3) Lamp Control Circuit. The lamp control circuit consists of dc/ac inverter PS1, series pass transistor Q3 and comparator U4D. PS1 is a dc/ac power supply operating with dc input voltages ranging from +17.5 to +30.0 Vdc. Output voltages range from 50.0 to 150.0 Vrms and is totally dependent on the input voltage. This voltage is supplied to the keyboard lighting circuit via J3 (pins 1 and 2) and to the LCD EL panel via J2 (pins 7 and 8). PS1 is controlled by the front panel DIM control and the power saver portion of the microprocessor program. The DIM control input (P1-7) establishes biasing for Q3 while the microprocessor controls when power is enabled to PS1. The microprocessor enables power to PS1 during the following conditions: an initial power up (RT turned on); a keyboard key is depressed; or 30 seconds has not elapsed since the last keyboard entry. When the microprocessor enables power to PS1, the output of comparator U4D provides a path to ground. This causes R10 and R11 to become a voltage divider. As the front panel DIM control resistance is varied, the base drive of Q3 is varied. As the base drive is varied, the current to PS1 is also varied, thus controlling input voltage to PS1. When the microprocessor disables power to PS1, the output of U4D is approximately +8.0 Vdc (ground path removed from voltage divider). This ceases current flow through the resistors and forces the base of Q3 to be at the same potential as the emitter. This causes current flow to be zero and PS1 is turned off.

(4) Heater Control Circuit. The heater control circuit consists of a resistive bridge network, voltage comparator U5A and transistor Q2. The circuit is controlled by the temperature sensor signal (J2-11) routed from the A4 LCD board. With the ambient temperature below -22 degrees F(-30 degrees C), the temperature sensor input at U5A-5 becomes positive with respect to the reference voltage (approximately +4.0 Vdc) at U5A-4. This forces the output voltage at U5A-2 positive and transistor Q2 into conduction. With Q2 conducting, current flows from the heater circuit (HR1) on the A4 LCD board. As the LCD display warms up (or if the ambient temperature is sufficiently warm) the temperature sensor input at U5A-5 is less positive. With the input at U5A-5 is less positive (lower) than the reference voltage at U5A-4, the output at U5A-2 is forced to ground (negative rail). This turns Q2 off, and current flow through HR1 on the A4 LCD board stops. Power for the heater control circuit is a regulated +8.0 Vdc supplied by U6.

b. Data Converter LCD CCA A1A4. Refer to Figure 4-8 and FO-6. LCD board A4 consists of a LCD display, two LCD drivers, an EL panel, and a temperature sensor/heater circuit.

(1) Electroluminescent (EL) Panel. EL panel DS2 backlights the LCD display. With a high voltage (approximately 100 Vrms, 400 Hz) applied to P1-7 and P1-8, the EL panel produces light. Power supplied to the EL panel is switched on or off by the lamp control circuit of interface board A1. The EL panel is connected to the input power via a short zebra elastomeric layer connector (zebra connector) located between the EL panel and the A4 PCB. The zebra connector is attached by pressure to two pads located on the A4 PCB. The pads are attached to traces that connect to connector P1 (pins 7 and 8) on the A4 board.

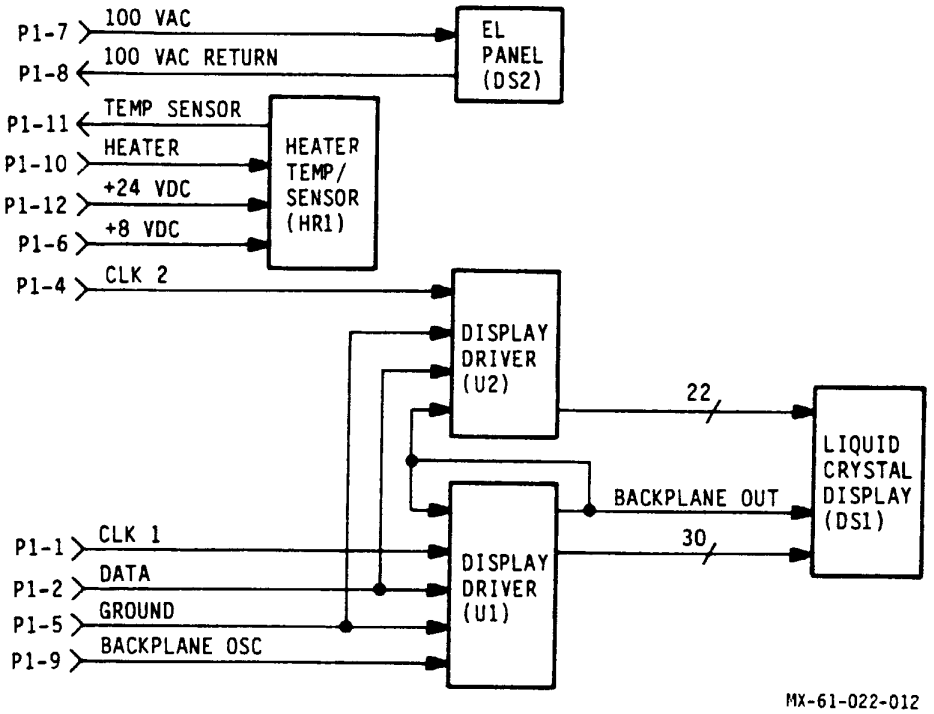


Figure 4-8. LCD CCA A1A4 Block Diagram

(2) Temperature Sensor/Heater Circuit. Heating for the LCD display is provided by resistive heater HR1. HR1 includes a thermistor with positive temperature coefficient. As the display warms (or if the ambient temperature is sufficiently warm) the heater power is reduced to conserve energy. The +8.0 Vdc supply (P1-6) is derived from the fixed 8.0 volt regulator (U6) on the A1 interface board. The switched +24.0 Vdc supply (P1-12) is supplied to HR1 via the front panel OFF/VOLUME control and is derived from the +24.0 Vdc input at the rear of the RT. The temperature sensor (P1-11) output level is determined by the temperature/resistance of HR1 (thermistor) in series with R1. When P1-11 becomes positive with respect to the reference voltage at U5-4 on the A1 board, a ground path is provided at P1-10. This enables HR1 and current is flows through the heater element of HR1. When the temperature of the display rises above -22 degrees F (-30 degrees C), the voltage at P1-11 is negative with respect to the reference voltage at U5-4. This removes the ground path at P1-10 and HR1 is disabled.

(3) LCD Display Drivers. Display drivers U1 and U2 provides interface between the data source and the LCD display. Each driver can drive 32 segments of the LCD. Synchronization between U1, U2 and the LCD display is accomplished via the backplane (common) connection. The RC elements (R12 and C11) on the A1 board, along with an oscillator and divide-by-16 circuit internal to U1, establishes the backplane/ display frequency. The backplane output at U1-23 is a square wave signal between 35 and 100 Hz. Serial data transfer from the data source to the display driver is accomplished with two signals, data and clock. The input data format consists of a logic one (1) start bit, followed by 32 bits of data. Internal to U1/U2 a load and reset signal is generated at the 36th clock pulse. The load signal is generated

ynchronously with the high state of the 36th clock pulse and latches the 32 data its. At the low state of the clock, the reset signal is generated which clears all the internal shift registers for the next set of input data. U1/U2 outputs change only if the serial data bits differ from the previous data input. The clock inputs at P1 (pins 1 and 4) are derived from the microprocessor on the A3 board.

(4) Liquid Crystal Display. LCD display DS1 is a transflective liquid crystal display consisting of seven-segment digits and enunciators. The method used to activate a liquid crystal segment is to apply a square wave drive signal which is out of phase (180 degrees) with the square wave applied to the common backplane. When the segment drive signal is in phase with the square wave, the segment is not activated.

c. Data Converter Memory I/O CCA A1A2. Refer to Figure 4-9 and FO-4. Memory I/O board A2 contains the memory mapping decoder network for the data converter. The term memory mapping refers to a technique where I/O devices appear to be a block of memory to the microprocessor. This technique permits the microprocessor to access any device in the same manner as it accesses the main memory. All I/O devices in this system are memory mapped. This includes the RT data and address bus (RT DB and RT ADRS), and all memory devices both volatile and nonvolatile.

(1) Master Memory Mapping Decoder. Table 4-4 lists the primary memory address mapping scheme. Master memory mapping decoder U18 is a dual binary 1-of-8 decoder/demultiplexer. When a memory read (J3-12) or a memory write (J3-10) signal is sent by the microprocessor, the signal is combined with TPC (J3-8) and memory address line MA15 and applied to U18. This signal is the main enable signal for the master memory mapping decoder (U18). With U18 enabled, the binary combination of memory address lines MA13 and MA14 causes the decoder (U18) to turn on a single block of memory. The master decoder divides the available 64K address locations into 8K byte blocks.

(2) Erasable Programmable Read Only Memories (EPROM). There are three EPROM devices (U7, U8 and U9) on the memory I/O board, however, only U7 is used in receiver-transmitter type RT-1319/URC. U7 is a 65,536 bit EPROM organized as 8192 words by 8 bits each. U7 contains the program for operating the RT. U7 is configured to operate in two modes, read or standby. The read mode is selected when pin 4 of memory mapping decoder U18A goes low. In this mode, data in a memory location designed by the memory address lines (A0 - A12) is sent onto the data bus and routed under microprocessor control. With pin 4 of decoder U18A high, the standby mode is selected. This mode forces all outputs (00 to 07) of the device to the high impedance state and provides an 80% reduction in power.

(3) Random Access Memory (RAM). The memory I/O board uses two 1024 by 4 bit static RAM devices (U19 and U20) in parallel to create the effect of one 1 K by 8 bit RAM. The RAM memory location where data is to be read from or written into is designated by the microprocessor and fed to U19/U20 via memory address lines A0 - A9. Data is read from memory with the MWR signal present at U19/U20-10 high and the chip enable (CE) signal at U19/U20-8 low. Data is written into the RAM with a low logic level present at pins 8 and 10 of U19/U20.

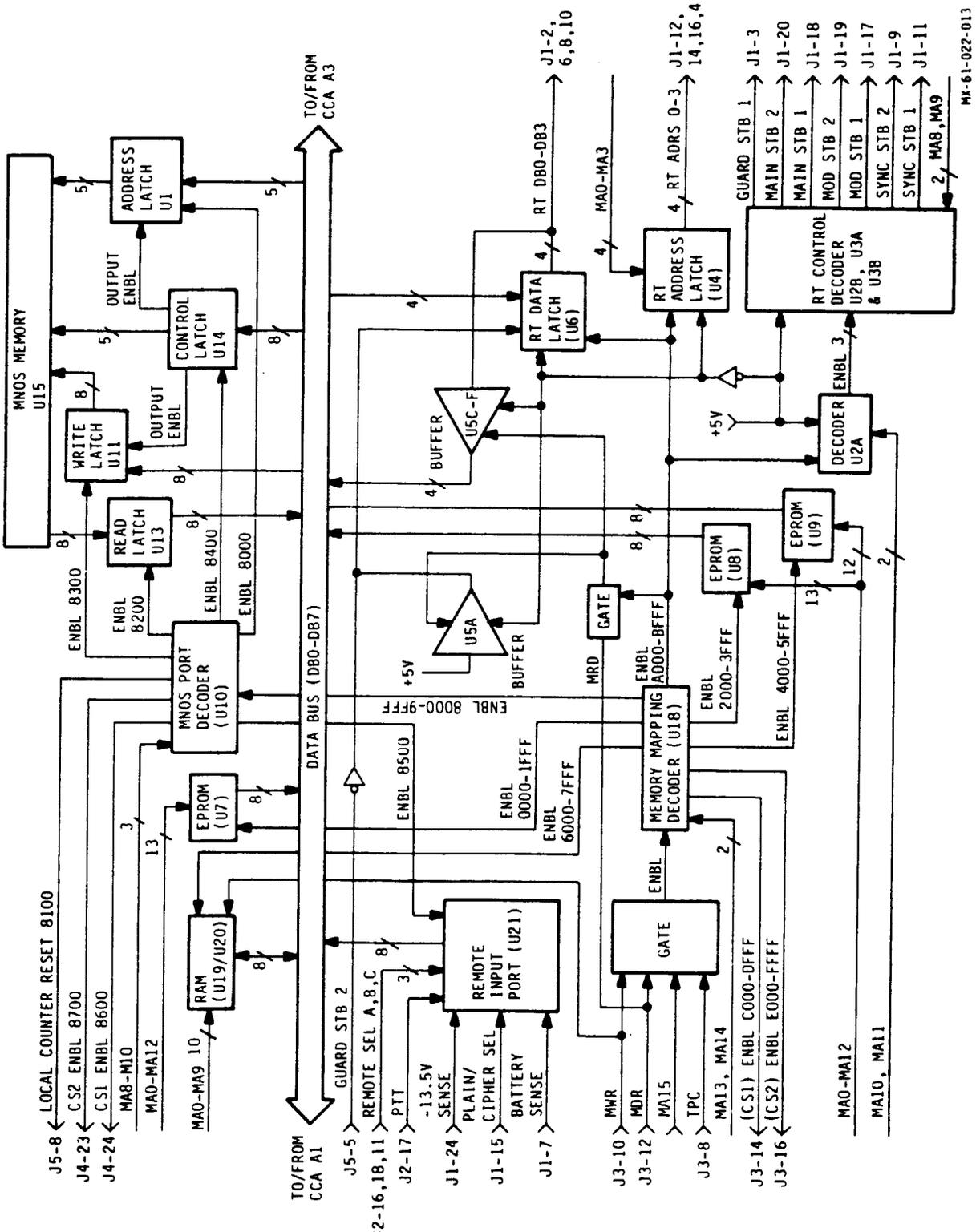


Figure 4-9. Memory I/O CCA A1A2 Block Diagram

Table 4-4. Primary Memory Address Mapping Scheme

Memory address block	Used for	Device	Data converter board
0000 to 1FFF	EPROM 1	U7	A2
2000 to 3FFF	EPROM 2	*U8	A2
4000 to 5FFF	EPROM 3	*U9	A2
6000 to 7FFF	RAM	U19, U20	A2
8000 to 9FFF	MNOS CONTROL PORT	U10	A2
A000 to BFFF	RT CONTROL BUS	U4, U6, U2A	A2
C000 to DFFF	RT KEY CONTROL	U8	A3
E000 to FFFF	Remote I/O	U19, U21	A3

*Device not used on RT-1319/URC

To insure compatability with "on-board" programming equipment, U7 on Memory I/O data converter Board CCA A1A1A1A2 PN 914871-XXX must be the same basic part number. Assembly 914871-805 contains devices which require +21 Vdc programming voltage (V p-p), while assembly 914871-807 requires +12.5 Vdc programming voltage (V p-p). If an assembly is to have U7 replaced, the replacement part must be the identical part number. If this part is not available, U7 must be replaced and the assembly dash number changed accordingly in order to properly identify the assembly.

(4) Metallic-Nitride-Oxide Semiconductor (MNOS) Memory. Refer to Table 4-5 for the associated input signal conditions required to select the MNOS memory operating modes. The MNOS memory device (U15) is the nonvolatile storage medium used to hold all user changeable information that is desired to be maintained when the RT is off. This information includes the preset channels, the last manually entered frequency, and the last selected operating modes. U15 is a 512-bit electrically alterable ROM organized as 64 words by 8 bits each. U15 is a tri-state device with four operating modes; disabled (or standby), write, erase and read.

(5) MNOS Control Port. Table 4-6 lists the secondary memory address mapping scheme. Refer to Table 4-7 for the associated input signal conditions required to select the MNOS control port (U10) operating modes. The MNOS control port (U10) is an eight-bit serial-input, parallel output storage register which fuctions as a 1-of-8 demultiplexer. U10 is a secondary decoder network that decodes the individual memory address locations between 8000 and 8007 so that each address will access a different I/O device. The MNOS control port provides the necessary chip enables so that the read (U13), write (U11), control (U14) and address (U1) latches will operate. U10 also supplies the remote input port (U21) with the chip select signal. Refer to Table 4-7 for the associated input siganl conditions required to select the NOS control port (U10) operating modes.

Table 4-5. MNOS Memory (A2U15) Control Logic Input Levels

Chip select*		Control*		Clock	Selected mode	Function
CS1	CS2	C1	C2			
L	H	X	X	X	DISABLED	Data lines (D0-D7) are open circuited
H	L	L	L	X	WRITE	Input data is written into selected address
H	L	L	H	X	ERASE	Data at selected address is erased
H	L	H	X		READ	Addressed data is read after negative transition of clock pulse

*L= Low (< +0.4 Vdc), H=High (> +4.0 Vdc), X= DON'T CARE

Table 4-6. Secondary Memory Address Mapping Scheme

Memory address block	Used for	Device	Board
8000	Address Latch	U1	A2
8100	Local Counter Reset	*U12A	A3
8200	Read Latch	U13	A2
8300	Write Latch	U11	A2
8400	Control Latch	U14	A2
8500	Remote Input Port Latch	U21	A2
8600	Display Port	U1	A1
8700	Keyboard Encoder	U2	A1

*Device not used on RT-1319/URC

Table 4-7. MNOS Port Decoder (A2U10) Control Logic Input Levels*

Latch output	Address state A2	A1	A0	Interfaced device/signal	
Pin 9	Low	Low	Low	U1	Clock Input
Pin 10	Low	Low	High	A3U12A	Local Counter Reset (Not used RT-1319/URC)
Pin 11	Low	High	Low	U13	Clock Input
Pin 12	Low	High	High	U11	Clock Input
Pin 13	High	Low	Low	U14	Clock Input
Pin 14	High	Low	High	U12D	Output Enable Signal (U21)
Pin 15	High	High	Low	A1U1	Chip Select (CS2)
Pin 1	High	High	High	A1U2	Output Enable (CS1)

* 1. With the write disable input (U10-4) low the addressed latch follows the data input (U10-3); unaddressed latches are reset to zero.

2. With U10-4 high, all latches are reset to zero.

(6) Read, Write, Control and Address Latches. The MNOS memory (U15) requires the input signal conditions necessary to enable various operating modes be as long as 120 milliseconds. Since the microprocessor must continue to cycle through the program, it is impossible to maintain any input signal condition for U15 directly from the microprocessor. Therefore, read latch U13, control latch U14, write latch U11 and address latch U1 maintain the necessary signal lengths required for the operation of U15.

(a) Read latch. The read latch (U13) to latches data from the MNOS memory data port for output onto the microprocessor data bus. The device is selected by the microprocessor via the MNOS control port (U10-11). Input data is transferred to the output on the low-to-high transition of the signal applied to the clock input (U13-11). The outputs of U13 are isolated (open circuited) from the microprocessor data bus whenever the device is not selected (U13-1, high).

(b) Write latch. The write latch (U11) latches data from the microprocessor data bus for input to the MNOS memory data port. The device is selected by a high logic state supplied by the MNOS control port (U10-12). The state of the output enable input (U11-1) from control latch U14, determines when the outputs of U11 are available to the MNOS memory data port. The outputs are available to MNOS memory with the output enable signal low. With the output enable signal is high, the outputs of U11 are open circuited, eliminating contention between the read and write latches for the MNOS memory data port.

(c) Address latch. The address latch (U1) latches address information from the microprocessor data bus for input to the MNOS memory address port. The device is selected by a high logic state supplied by the MNOS control port (U10-9). U1 latches the five bit address code which designates which MNOS memory location data is to be read from or written into. The five bit address code is available to the MNOS memory address port with the output enable signal from the control latch (U14-12) low.

(d) Control latch. The control latch (U14) supplies the control inputs required for various MNOS memory operations. It is accessed by the microprocessor to control the signal lengths of data supplied to MNOS memory by the address and write latches. The device is selected by a high logic state supplied by the MNOS control port (U10-13). The device is configured with its output enable input tied low. This permits the input data to be transferred to the outputs of U14 each time the device is selected. The control data latched by U14 is always available to MNOS memory (U15), write latch U11 and address latch U1. Refer to table 4-5 for the input signal conditions applied to MNOS memory via control latch U14.

(7) Remote Input Port. The remote input port (U21) latches RT configuration and status information onto the microprocessor data bus. Data applied to U21 is from the power regulator CCA (A7) and the front panel REMOTE connector of the RT. The outputs of U21 are available to the microprocessor data bus the output enable signal supplied by the MNOS control port (U10-14) high. With the output enable signal supplied by U10 low, all outputs of U21 are open circuited. A description of the input signals applied to the remote input port is as follows:

(a) Remote select inputs. The REMOTE SEL A,B and C inputs (J2-16, -18, and -11, respectively) provide a digital code which informs the microprocessor of the active RT configuration. With the RT configured for full function local control, the state of these inputs are pulled high through 100 Kilo-Ohm resistors (R27, R28, R29) and protected against high input current by 1 Kilo-ohm resistors (R45, R46, R47).

(b) Push-to-talk input. The PUSH-TO-TALK (PTT) input informs the microprocessor of the active receive or transmit state of the RT. The PTT input is routed from the front panel AUDIO connector and is also supplied to the front panel REMOTE connector. This input is held at a high state during reception and forced low during transmission.

(c) Battery sense. The BATTERY SENSE input (J1-7) is an input voltage sense line supplied from the power regulator CCA (A7). This input is zener regulated by CR2 which converts the battery sense input to CMOS compatible 5.0 volt logic. The input state to U21-4 is high unless the input voltage drops below +18.0 Vdc. If the input voltage drops below +18.0 Vdc, the normally high output at U21-5 goes low. The microprocessor then causes the decimal point in the frequency display to blink.

(d) Negative 13.5 Vdc sense. The data converter does not use the -13.5 Vdc supply for operation, however, it does monitor the supply for a minimum tolerable level. If the supply does not meet the minimum tolerable level of -5.0 Vdc, the microprocessor will not allow the RT to enter the transmit mode. This inhibit function is required because the -13.5 Vdc supply is used by the modulator to control the power out of the RT. The -13.5 Vdc supply is sensed by the combination of R56, R25, R43, CR6 and the input of U21-18.

(e) Plain/cipher select. The PLAIN/CIPHER SEL input (J1-15) informs the microprocessor of the active clear or secure configuration of the RT. The state of this input (U21-7) is high for clear communication and low for secure communication.

(8) RT Control Bus. The RT control bus provides the digital interface between the microprocessor address and data bus, and the RT address and data bus resident in other RT assemblies. In addition, the RT control bus circuitry generates seven strobe signals to facilitate address and data transfer.

(a) Address and data interface. The RT control bus circuitry for address/-data interface includes; two 4-bit d-type registers (U4, U6), a hex noninverting buffer (U5), two Schmitt trigger inverters (U12E,F) and OR gate U17C. Input data is applied to 4-bit registers U4 and U6 directly from the microprocessor address and data bus. This data is transferred to the Q outputs of the registers on the positive transition of the clock input (U4/U6-7) only if all inputs to the OUT ENBL and DATA ENBL inputs (pins 1, 2, 9 and 10) are low. With either OUT ENBL input (pins 1 or 2) high, the Q outputs present a high impedance state to the bus. With either DATA ENBL input (pins 9 or 10) high, data entry is inhibited and the Q outputs remain unchanged. Conditions that will inhibit communication between U4/U6 and requiring RT assemblies includes; the device is not selected by the microprocessor (U18-11 is high), or the unprotected +5 Vdc supply is loss due to a low input power condition. The GD STB 2 input (J2-5) controls data transfer between requiring RT assemblies and the microprocessor. With (J2-5) high, data transfer is allowed from the microprocessor via U6 to requiring RT assemblies. Data transfer from RT assemblies to the microprocessor is accomplished when the GD STB 2 input is low and the microprocessor is in the memory read mode (MDR is low). This permits data from RT assemblies to be routed onto the microprocessor data bus via four sections of noninverting buffer U5 (U5C,D,E,F). Hex-buffer U5 is a tri-state device with two independent disable inputs (pins 1 and 15). With the voltage at either disable input high, all outputs go to the high impedance state. With the microprocessor in any mode other than the read mode, U5 is disabled eliminating contention for the data bus.

(b) Strobe generation. Dual 1-of-8 decoders U2 and U3 are used to generate strobe signals to enable various RT functions maintained by other RT assemblies. Primary decoder U2A enables/disables secondary decoders U2B, U3A and U3B. U2A is enabled when the logic state applied to its enable input (U2-1) is low. The selected output line of U2A is active low, and is determined by the binary combination of memory address lines MA10 and MA11 from the microprocessor. The active output of U2A enables one of the three secondary decoders. The selected output of either secondary decoder is determined by the binary combination of memory address lines MA8 and MA9. The selected output of decoders U2B, U3A or U3B enables latch circuits resident in the modulator, synthesizer, main receiver or guard receiver assembly. U2 and U3 are powered by the unprotected +5.0 Vdc supply and is disabled if the supply is loss due to low input voltage conditions.

d. Data Converter CPU CCA A1A3. Refer to Figure 4-10 and FO-5. CPU board A3 contains the system timing generators, the remote I/O port, and the microprocessor which provides data processing and control of the data converter.

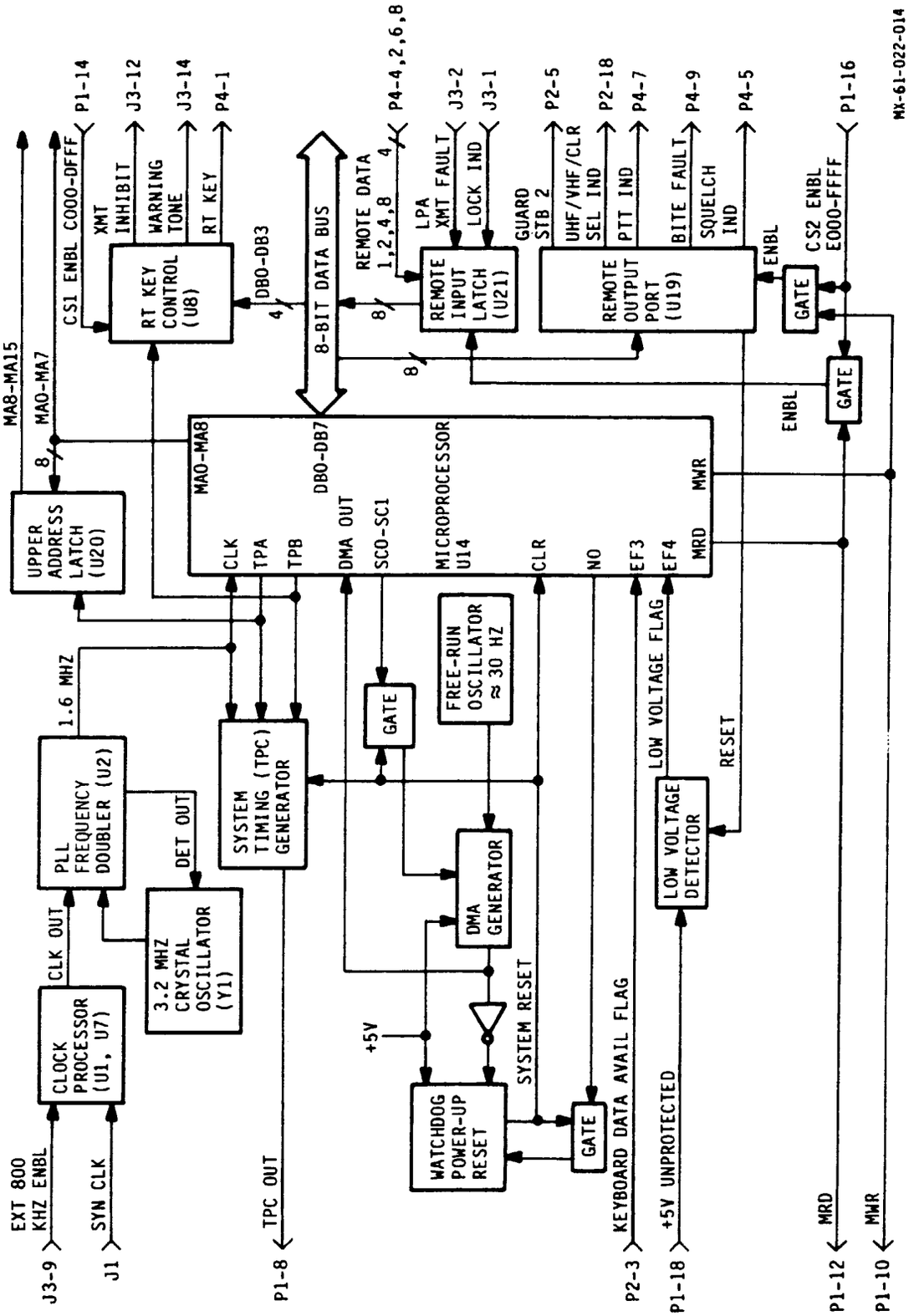


Figure 4-10. CPU CCA A1A3 Block Diagram

(1) Clock Processing Circuit. The clock processing circuit consists of multiplexer U1 and Schmitt trigger inverter U7A. The 800 kHz clock source from the synthesizer enters the CPU board at J1 and is applied to Schmitt trigger inverter U7A which provides an output waveform with sharp transitions. The output of the inverter is routed through multiplexer U1 and applied to a phase-locked-loop (PLL) frequency doubler circuit. In RT-1319/URC, the synthesizer clock source is always selected by multiplexer U1. This is due to the low or default condition (J3-9 left open) of the EXT 800 KHZ ENBL line at J3-9.

(2) Frequency Doubler Circuit. The frequency doubler circuit consists of phase-locked-loop (PLL) frequency synthesizer U2 with a voltage controlled crystal oscillator. With the input frequency from multiplexer U1 applied to the PLL frequency synthesizer (U2-2), the output of the voltage-controlled crystal oscillator is forced to maintain the same frequency. However, with no input frequency applied to U2-2, or the input frequency is outside the capture range of the PLL, the oscillator will free run. This permits the data converter to operate even if no input frequency is applied to the PLL frequency synthesizer. The output frequency (U2-5) maintained by the frequency doubler circuit is 1.6 MHz and is supplied to the microprocessor clock input (U14-1). U2 contains three internal divide circuits; a divide-by-two circuit, a selectable 29 or 210 reference divide circuit and a programmable divide-by-N counter. The divide-by-two circuit receives the 3.2 MHz input (U2-3) and supplies 1.6 MHz to the reference divide circuit, the TPC generator and to the microprocessor (U14-1). The selectable reference divider divides the reference frequency (1.6 MHz) by 29 or 210 and applies it to the phase detector. The reference divider is controlled by the state of the frequency select (FS) input (U2-6). A high level at this input selects 3.125 kHz as the reference frequency and a low level selects 1.5625 kHz. The programmable divider circuit receives the selected input frequency (U2-2) and performs a divide-by-N function determined by the binary inputs (U2-9 through U2-17, U2-9 MSB input). The divider performs a divide-by-256 and applies a 3.125 kHz input frequency to the phase detector. The phase detector output (U2-7) is high when the input frequency is less than the 3.125 kHz reference frequency, and is low when the input frequency is greater than the reference frequency. This output signal (U2-7) controls the bias for varactors CR9 and CR10. A resistive-capacitive (RC) network (consisting of R90, R91, R95 and C32) insures that only a slow varying voltage is applied to the varactors. A coupling capacitor (C20) insures that no signal voltages are applied to the varactors.

(3) Main Processor. Data processing for the data converter is provided by microprocessor U14. U14 uses an 8-bit bidirectional data bus and a 16-bit multiplexed address bus. The microprocessor generates timing signals which control most of the signal processing within the RT. The most important of these timing signals are the TPA, TPB, MRD, MWR, NO, SC0 and SC1. The TPA signal latches the upper address into an external latch (U20) and therefore, defines when the upper address (MA8-MA15) is valid. The latched upper address is held until the next occurence of the TPA signal. The TPB signal sets the timing for data transfer to or from the microprocessor. Therefore, this signal defines when the data and the lower address is valid. The MRD signal provides the clock timing to read data from the data bus. The MWR signal provides the clock timing to write data onto the data bus. The SC0 and SC1 signals indicate the active operating state (fetch, execute, DMA or interrupt) of the microprocessor. When a DMA request is being processed, the condition of these lines force the DMA generator (U6A) to be reset. The NO signal resets the watchdog circuit which monitors operation of the system software.

(4) TPC Generator. The TPC generator consists of D-type flip-flops (FF) U10 and U6B, Schmitt trigger inverting buffers U7C and U7D, and OR gates U16B and U16C. The TPC generator sets up the required timing for the data converters memory and I/O devices. The TPC generator uses the 1.6 MHz clock signal (U2-2) in conjunction with the TPA and TPB timing pulses from the microprocessor to develop the TPC pulse. The TPC timing pulse establishes the number of clock cycles within each machine cycle (eight clock cycles) that the memory and I/O devices are available to the microprocessor. The TPA and TPB pulses are routed through waveshaping inverters (U7C,D) and applied to the clock inputs of a dual D-type FF (U10). The Q output of the FF (U10-1) is ORed with the system reset signal (U16-8) from the watchdog circuit. The OR gate (U16B) permits the low-to-high transition of the TPC pulse to be initiated by the TPC generator or by the watchdog circuit if it detects a software malfunction. The output of the OR gate is applied to the reset pin (U6-10) of the TPC generator output FF. The output FF (U6B) is clocked by the ORed output of U16C which receives the 1.6 MHz clock and the Q output of U6B as inputs. The output of U16C initiates the high-to-low transition of the TPC timing pulse if the TPC generator is not held in reset by the watchdog circuit. During normal operation, the TPC timing pulse is high for approximately three clock cycles after the TPB signal occurs at the microprocessor (U14-33).

(5) DMA Generator. The DMA generator consists of D-type U6A and several gates (U13D, U15F and U16A) that gate together the microprocessor SC0 and SC1 lines with the system reset. The clock input for U6A is supplied by a free-running oscillator made from inverters U15A and U15B. The output frequency is approximately 30 Hz and is set by the values of R80 and C19. During normal operation, U6A is clocked by a rising edge at its clock input which causes the inverted Q line (U6A-2) to go to a logic zero state. This logic zero state is applied to the microprocessor DMA OUT input (U14-37) which flags the microprocessor of a pending DMA request. With the DMA request enabled, the microprocessor finishes the current instruction, then responds by setting SC1 (U14-5) high and SC0 (U14-6) low. The logic state of SC1 and SC0 is applied to U15F and U13D, respectively, causing a high state to be applied to the reset input (U6-4) of the DMA FF. With the DMA FF reset, the DMA request is disabled permitting normal program operation to continue. The microprocessor is forced to increment its program counter every time the DMA request occurs. By inserting idle instructions in the program and allowing the DMA generator to force the microprocessor past them, the system timing can be established. This type of timing is used to set the time out period of the display as well as other display timers. The DMA generator also supplies the clock signal to the watchdog circuit.

(6) Watchdog Power Up Reset Circuit. The watchdog/power up reset circuit consists of dual D-type FF U9 and several gates (U12C, U13A, and U16A). The clock input for U9 is supplied from the Q output of DMA generator U6A. It should be noted that the Q output applied to U9 (U9-3, -11) is the inverse of the DMA pulse (U6A-2) applied to the microprocessor. This permits the watchdog circuit to clock/count each DMA pulse applied to the microprocessor. The watchdog circuit is configured to reset the system if two consecutive DMA pulses occur without the microprocessor performing a watchdog circuit reset. A watchdog circuit reset is performed by the microprocessor toggling its N0 line (U14-19) when it executes an output instruction. Output instructions have been placed in the software such that in normal operation no more than one DMA pulse will occur per watchdog reset. When the N0 line (U14-19) is not toggled after each output instruction, U9-13 goes high on the next positive

transition at the clock input. This high logic level at U9-13 will reset the system. The system reset includes watchdog circuit U9, DMA generator U6A, TPC generator U6B, and the microprocessor. When a system reset is performed, the watchdog circuit will hold the microprocessor in the reset condition for approximately 30 milliseconds. The watchdog circuit then begins to count from zero again. The watchdog circuit permits the microprocessor to monitor the function of the software and reset itself if the software is not functioning normally.

(7) Low Power Detector Circuit. The low power detector circuit consists of inverting buffers U15C-D-E, NOR gate U13B, Schmitt trigger U7E, and AND gates U11C-D. The primary function of the circuit is to monitor temporary low input voltage conditions of the RT when it is configured in radio sets/systems powered by a vehicle power generating system. The circuit monitors the unprotected +5.0 Vdc supply which powers the circuitry that interfaces the data converter to other RT assemblies. It should be noted that the +6.3 Vdc (J3-10) and the unprotected +5.0 Vdc supply (P1-18) is the same voltage. This voltage is supplied by power regulator CCA A7, and is derived from the +24.0 Vdc input at the rear panel. During low input voltage conditions, the unprotected supply is not available to the data converter. The unprotected +5.0 Vdc is input to a low voltage trigger circuit consisting of U15C, C17, U13B and U7E. The output of the trigger circuit (U7E-10) is a constant high as long as the unprotected supply is present. When the unprotected supply is lost, the circuit generates a momentary low pulse which forces the normally high output (U15E-4) of the detector circuit low. The output of U15E is connected to the microprocessor external flag (EF-4) input (U14-21), which is sampled at the beginning of each instruction execute cycle. If the state of EF-4 is low, I/O controllers internal to U14 are enabled to transfer status information to the microprocessor. Included in this status information is the state of the BATTERY SENSE line from the remote input port latch (A2U21-5). When the state of A2U21-5 is low, the front panel display low voltage indicator (blinking decimal point) is enabled by the microprocessor. When normal input power is restored, the low voltage indicator is disabled (A2U21-5 goes high) and the low voltage detector circuit is reset (U15E-4 goes high). This is accomplished by logic states supplied by the microprocessor to output port U19 (pin 13). The low power detector circuit is reset by a low state applied to U11D-6. Once the circuit is reset, a high state is applied to U11D-6 which permits the circuit to again monitor the unprotected supply.

(8) Remote I/O Latch. The control signals applied to U21 are described in table 4-8. The remote I/O latch (U21) is an octal (8-bit) D-type latch. The latch interfaces remote data from an external unit onto the data bus. The outputs of U21 are available to the data bus when the state of the input (U21-1) is low. The state of the output enable line is controlled by OR gate U16D. U16D receives the MRD signal (U14-7) from the microprocessor and the CS2 signal (P1-16) from U18 on the A2 board. The state of the output enable line (U21-1) is high unless the microprocessor is in the memory read cycle (MRD signal low) and the remote I/O latch is selected by the microprocessor via A2U18.

(9) RT Key Control Circuit. The RT key control circuit consists of 4-bit D-type register U8, AND gate U11B, and transistor Q1 and Q2. U8 is clocked by the TPB timing pulse supplied by the microprocessor. Data transfer is controlled by the CS1 input (P1-14) supplied by memory mapping decoder U18 on the A2 board. When the CS1 input (P1-14) is low, the outputs of U8 follow the data inputs at the next positive

Table 4-8. Remote I/O Latch (U21) Input Signals

Input signal	Function
Remote data (1,2,4 and 8)	Supplies data from a remote controller to the data converter for processing.
LPA XMIT FAULT	Fault indication derived from the AM-7176/VRC-83 when the RT is configured in the AN/VRC-83(V) Radio Set.
Lock Ind	Signal from the synthesizer to indicate when the phase-locked loop is locked on frequency.

transition of the TPB pulse. When the CS1 input is high, data entry is inhibited and the state of the outputs will remain unchanged. The outputs of U8 control the states of the WARNING TONE, TUNE ST and XMIT INHIBIT lines from the data converter. The WARNING TONE signal (J3-14) is always held in the low state by U11B. This signal is used to disable the warning tone circuit of the guard receiver assembly. The TUNE ST (also referenced as the RT Key) output (P4-1) is high when in receive and low when the RT is in the transmit mode. This signal indicates to requiring RT assemblies that the transmit mode has been entered. One of the functions of the RT key line is to select the correct output on the synthesizer module (i.e., remove the injection signal from the main receiver and apply it to the modulator). When the RT key is in the transmit state and the synthesizer should lose lock, the RT key line will return to the receive state. The XMIT INHIBIT output (J3-12) is similar to the RT key signal in that it is high in receive and low when in transmit. Its primary function is to permit the B+ supply to be applied to the modulator at the proper moment. This permits the synthesizer to settle on a frequency before power is applied to the transmitter by the modulator. When the data converter detects the -13.5 volt supply line (A2J1-14) is out of the desired limits, it returns the XMIT INHIBIT line to the receive state.

(10) Remote I/O Port. The remote I/O port consists of octal D-type FF U19 and NOR gate U13C. U19 receives status information from the data bus for output to an external unit. Data is transferred to the Q outputs of U19 on the positive going transition of the clock input (U19-11). This clock input is the NORed output of U13C which receives a MWR signal from the microprocessor (U14-35) and a CS2 signal (P1-16) from memory mapping decoder A2U18B. The Q outputs of U19 controls the state of the SQUELCH IND, BITE FAULT, PTT IND, UHF/VHF CLR/SEC IND and GUARD STB 2 lines from the data converter. The SQUELCH IND signal (P4-5) provides the means to inform an external unit that incoming traffic is present. It is also used in the retransmit mode to key the repeater. The BITE FAULT signal (P4-9) indicates the status of the radio amplifier. With this line low, a fault has been detected by the microprocessor on the LPA XMIT FAULT line and the data converter has switched the RT into the stand alone mode. When the RT is in the AN/PRC-113(V) configuration, this line will indicate a fault due to the default condition. The default condition of the LPA XMIT FAULT line is to indicate a fault whenever the radio amplifier is not connected to the RT. The UHF/VHF CLR/SEC IND signal (P2-18) is assigned as a dual function line. The first function is the UHF/VHF selection. This function is designated for use in systems where both the UHF and VHF capability of a single RT is being used regularly. By attaching this output to an antenna selector, the RT can

select the required antenna automatically. At present, this function is not included in the software. The remaining function is to indicate if the RT has been put into the secure mode by a secure speech device. A low on this line (P2-18) indicates that the RT has been put into the secure mode. The GUARD STB 2 signal (P2-5) strobes the guard receiver. When this line is low, the output latch on the guard receiver is enabled. This line is also used on memory I/O board A2 to disable the RT control bus circuit (A2U6) when the guard receiver is enabled. In addition, one section of U19 outputs an internal control signal (U19-12) for the low power detector circuit. It resets the low power detector circuit after normal power has been restored.

(11) Power Supply Voltages. The following subparagraphs describe the supply voltages used or monitored by the data converter.

(a) Positive 6.3 Vdc protected. The +6.3 Vdc protected supply is also reference as the EXT 5 VDC power supply. It enters the A3 board at J3-11. It powers the circuitry needed to keep the data converter running during low input power conditions without powering the other modules of the RT. The protected power supply enters the RT through the REMOTE connector on the front panel.

(b) Positive 6.3 Vdc unprotected. The unprotected +6.3 Vdc power supply is supplied to the data converter by power regulator CCA A7. It is derived from the +24.0 Vdc input on the rear of the RT and enters the A3 board at J3-10. The unprotected power supply powers the circuitry that interfaces the data converter to other RT modules. During a low input power condition, the unprotected supply is not available to the data converter. The unprotected supply is monitored by the low power detector circuit on the A3 board.

(c) Negative 13.5 Vdc and sensing. The data converter does not use the -13.5 Vdc supply for operation. However, the data converter does monitor this supply. The -13.5 Vdc enters the A2 board at J1-24 and is sensed by the combination of R56, R25, R43, CR6 and U21-18. When the supply does not meet the minimum tolerable level of -5.0 Vdc, the data converter will not allow the RT KEY line to go low. This prevents the RT from entering the transmit mode. This feature is included because the -13.5 Vdc supply is required by the modulator to control the power out of the RT.

(d) Negative 29.0 Vdc. The -29.0 Vdc supply enters the A2 board at J1-1. It is required by the nonvolatile memory (U15) in order to perform a read or write function. When the supply is not present, the data converter will not be able to read or store presets or modes of operation. When this condition occurs, the data converter will still be capable of operating the RT in the manual mode with no damage to the RT.

(e) Positive 12.0 Vdc. The +12.0 Vdc supply enters the A2 Board at J1-22 and is routed to P1-13 on the A1 Board. This +12.0 Vdc supply is the source to 8.0 volt regulator U6. The +12.0 Vdc supply is not used on any other board in the data converter.

(f) Switched +24.0 Vdc. The switched +24.0 Vdc supply enters the A2 board at J1-28 and is routed to P1-11 on the A1 board. On the A1 board, the +24.0 Vdc

supply powers the dc-to-ac converter and its associated control circuit. The +24.0 Vdc supply is also routed to P1-12 on the A4 board where it powers the LCD heater circuit.

(g) Positive 8.0 Vdc. The +8.0 Vdc power source is derived from the +12.0 Vdc source. An 8.0 Volt fixed regulator on the A1 board performs this conversion. The supply is used to power the display drivers and interface for the LCD display. It is also used by the heater control and heater circuits.

4-12. SYNTHESIZER ASSEMBLY A1A1A6. Refer to Figure 4-11 for a block diagram of the synthesizer assembly. Refer to FO-11 for the synthesizer schematic diagram. The synthesizer assembly consists of a bracket assembly and synthesizer CCA A1. The synthesizer CCA is a digital phase-locked-loop, indirect synthesizer which permits all channel frequencies to be derived from a single crystal. The loop consists of a charge-pump-phase-detector, a loop filter, a voltage controlled oscillator (VCO), and a programmable digital divider. In the transmit mode, the synthesizer supplies a coherent, on-channel frequency to the modulator assembly. In the receive mode, it supplies an injection frequency to the main receiver which is offset from the desired operating channel by an amount equal to the receivers first IF (30.1 MHz). In addition, the synthesizer also establishes the basic frequency accuracy and warmup characteristics of the RT.

a. RT Data Latches. Table 4-9 lists the initial power up routine data input sequence. Table 4-10 lists the sequential order in which data is input to the synthesizer. The synthesizer receives all its frequency select information over a 4-bit data bus (P1-11,-13,-15, and -17). This information is stored in addressable data registers/latches (internal to U1, U2 and U4) accessed via a 4-bit address bus (P1-19,-21,-23, and -28) and two strobe lines (P1-6 and -8). All data and address information is supplied under microprocessor control by the data converter. The data stored in four of the latches (internal to U4) is independent of the operating frequency; thus, it never changes and is sent to the synthesizer only once after the RT power is turned on. This data sets the reference (R) counter to divide-by-32, and sets the two LSB digits of the main counter to zero. This data must be present before the synthesizer will operate and therefore, must be sent during the power up initialization routine. The data words stored in the D/A converter (U1) and the main and swallow counters (internal to U4) are dependent on the operating frequency and must be updated each time a new frequency is selected. D/A converter U1 stores/converts the binary coarse and fine tune words supplied by the microprocessor, into an analog tune voltage for the main receiver. All data words are sent via the 4-bit data bus and therefore, must be broken down into 4-bit nibbles and sent sequentially to the synthesizer. The main, swallow, and coarse tune words are each 8-bit numbers and divided such that the four MSBs represent a nibble and the four LSB's represent another. The fine tune word is only a 4-bit number and is represented by a single nibble. The microprocessor also supplies the binary address code which accesses specific registers/latches internal to U1, U2, and U4. One of the binary address codes applied to U1 initiates a parallel load function internal to U1. When this address code is input to U1, the contents of its internal latches (12-bit coarse-fine tune word) is transferred in parallel to a 12-bit DAC register for digital-to-analog conversion.

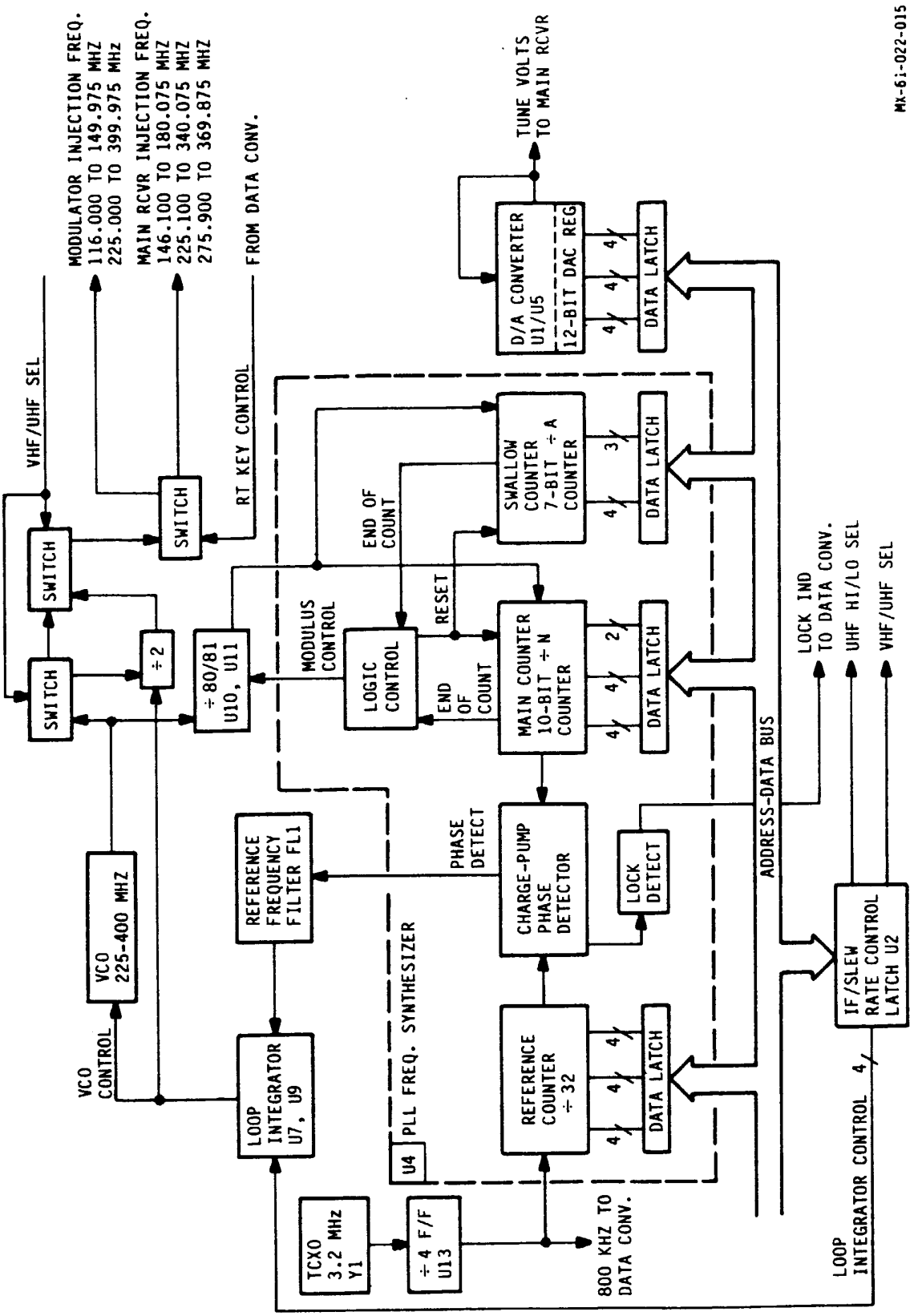


Figure 4-11. Synthesizer Assembly A6 Block Diagram

Table 4-9. Power Up Routine Data Input*

Data D3	D2	D1	D0	RT address A3	A2	A1	A0	Function	Purpose
L	L	L	L	H	H	H	L	Loads divide-by N Bits 8 and 9	Sets the two LSB's of main counter to zero.
L	L	L	L	H	H	L	H	Loads divide-by R Bits 0 through 3	Sets the reference (R) counter to a divide-by 32 event count.
L	L	H	L	H	H	H	L	Loads divide-by R Bits 4 through 7	
L	L	L	L	H	H	H	H	Loads divide-by R Bits 8 through 11	

* 1. L=Low (<0.4 Vdc) H=High (>4.0 Vdc)

2. Information at the data inputs (Do-D3) is entered into U4 when the SYN STB 1 signal (J1-8) is low, and is latched when the SYN STB 1 signal is high.

3. The high state of RT address 3 (A3) inhibits data entries to U1 while U4 is being accessed.

b. Reference Oscillator and Divider. The reference oscillator/divider circuit consists of a temperature compensated crystal oscillator (Y1), a dual D-type FF (U13), and a p-channel FET (Q5). The temperature compensated crystal oscillator (TCXO) supplies a 3.2 MHz output frequency to the clock input of U13A. U13 is configured to divide the 3.2 MHz output from the TCXO by four; thus, generating an 800 kHz reference frequency. The 800 kHz reference frequency is sent to the data converter via J4 and to the PLL frequency synthesizer oscillator input (U4-7). The fast switching p-channel FET (Q5) insures a synchronized output waveform is maintained between U13-2 and J4.

c. PLL Frequency Synthesizer. The PLL frequency synthesizer (U4) generates and maintains the minimum spacing (25.0 kHz) between frequency channels of the RT. It accomplishes this function via the following inputs: binary information from the microprocessor; the fixed reference frequency (800 kHz) from the TCXO/divider circuit; and the variable frequency input which is derived from the feedback loop. From these inputs, U4 generates the primary output signals to maintain the 25 kHz channel spacing via associated circuits within the synthesizer. U4-5 is the output line from an internal digital charge-pump phase detector which responds only to positive transitions on the divided-down reference and variable frequency inputs. When a phase error is detected the charge-pump phase detector acts as a discriminator and tunes the VCO toward a lock condition. The signal at U4-5 is negative when the variable frequency is greater than or leading the reference frequency, and positive when the variable frequency is less than or lagging the variable frequency. During a lock condition (phase coincidence) U4-5 is open circuited. The modulus control output at U4-14 controls the divide function of a two-modulus prescaler (U10

and U11). This output is low until the event count of the swallow counter is complete, then is high until the event count of the of the main counter (main plus swallow counter additional counts) is complete. When the preselected number of events (cycles of VCO output) is counted, the main counter provides an end-of-count signal which resets the counters, and the counting cycle is repeated. The lock detect signal at U4-13 is high during a lock condition, and low for any condition other than lock. This signal is sent to the data converter via J1-4. Refer to the RT data latch description for additional information on U4 internal logic.

Table 4-10. Synthesizer Address/Data Input Sequence

	Data received via SYN STB 1 signal				
Order	Data* D3 D2 D1 D0	Address* A3 A2 A1 A0	Selected device	Nibble name	Function
1	DATA INPUTS FREQUENCY DEPENDENT	L L H L	U1	4 MSB of coarse word	12-bit coarse-fine word tune from which the analog voltage for the main receiver is derived.
2		L L L H	U1	4 LSB of coarse word	
3		L L L L	U1	Fine word	
4		H L H H	U4	4 MSB of main word	Sets main counter to appropriate divide-by-N event count.
5		H L H L	U4	4 LSB of main word	
6		L L H H	U1	D/A converter parallel load	Initiates parallel load of 12 bit coarse-fine word contained in the three intermediate registers of U1. Data present on the databus during this address state is not used.
7		H L L H	U4	4 MSB of swallow word	Set swallow counter to appropriate divide-by-A event count.
8		H L L L	U4	4 LSB of swallow word	

Table 4-10. Synthesizer Address/Data Input Sequence-Continued

Order	Data received via SYN STB 1 signal: Data* D3 D2 D1 D0	Address* A3 A2 A1 A0	Selected device	Nibble name	Function
9	X X X L	X L L L	U2-9	Slew rate control	
10	X X X L	X L L H	U2-10	If main word >= 140 and main word <190	
	X X X H	X L L H	U2-10	If main word <140 or main word >=190	
11	X X X L	X L H L	U2-11	If main word >= 190	
	X X X H	X L H L	U2-11	If main word < 190	
12	X X X L	X L H H	U2-12	If UHF selected	
	X X X H	X L H H	U2-12	If VHF selected	
13	X X X L	X H L L	U2-13	If UHF and channel frequency >= 310.000 MHz	
	X X X H	X H L L	U2-13	All other VHF/UHF frequencies	
14	X X X L	X H L H	U2-14	If FM and XMIT (This condition not used)	
	X X X H	X H L H	U2-14	All other conditions	
15	X X X H	X L L L	U2-9	Slew rate control	

* 1. L=Low (<0.4 Vdc) H=High (>4.0 Vdc) X=DON'T CARE.

2. A high state at RT Address 3 (A3) inhibits data entries to D/A converter U1 while U4 is being accessed.

3. Data latches addressed via SYN STB 2 each store only a single bit (D0) of information.

4. Information present at U2 DATA input is transferred to the addressed latch when SYN STB 2 signal is low, and inhibited when SYN STB 2 is high.

d. Loop Integrator Circuit. The phase error signal is output from U4-5 and applied to low pass reference frequency filter FL1. The filter attenuates the reference frequency signal and harmonics that appear at the phase detector output (U4-5). This attenuation (approximately 123 dB) prevents spurious signals on the VCO output frequency by attenuating the magnitude of the 25 kHz component before it is applied to the VCO control line. The signal from the reference filter is applied to the loop integrator. The loop integrator consists of a RC (resistive-capacitive) network used in conjunction with

operational amplifier U9. The loop integrator provides the RC time constants necessary to control fundamental loop characteristics such as loop bandwidth, capture time, open-loop gain verses frequency, and transient response (damping ratio). The gain and slew rate adjustments for U9 is controlled by the microprocessor via control latch U2 and quad SPST analog switch U7 (see table 4-10 for input/output logic functions of U2). The control inputs of U7 (pins 1,8,9,16) are active low, and are held in the high state when its corresponding switch is not selected. The loop integrator in conjunction with the reference frequency filter provides approximately 3 dB damping coefficient to provide open and closed loop stability. Resistor R69 is a select component insuring the incidental frequency modulation (IFM) peaks from the synthesizer are maintained between 400 to 600 Hz.

e. VCO Circuit. The VCO is a varactor-tuned LC (inductor - capacitor) oscillator. The VCO control voltage is derived from the PLL frequency synthesizer phase detect output signal (U4-5). This signal is filtered and applied to an integrator whose output tunes the VCO to the desired operating frequency. Inductor L5 provides the mechanical adjustment necessary to insure the VCO control voltage (VCO end-point tune voltage at TP3) is set to the proper level. In the transmit mode, this control voltage varies from approximately +2.0 Vdc at 255.000 MHz to +20.0 Vdc at 399.975 MHz. The control voltage varies the reverse-bias on the hyperabrupt junction varactor diodes which electrically tunes the VCO to the desired operating frequency. Variable components T1, C30, C31 and T2 establish VCO tracking across the frequency range of 225.000 MHz to 399.975 MHz. The output of the VCO circuit is the desired UHF operating frequency or a frequency which is twice the desired VHF operating frequency. When the RT is operating in the UHF band, the VCO output is routed via pin diodes directly to the input of RF amplifier Q6. When the RT is operating in the VHF band, the VCO circuit continues to operate at UHF frequencies, but the VCO output is switched to a high-speed divide-by-two circuit. In addition, the VCO supplies the operating frequency feedback for the closed loop. This signal clocks a two-modulus prescaler which performs a divide-by-80/81 function on the frequency applied to its clock input (U11-12). The output frequency of the divide-by-80/81 counter is the variable closed loop feedback frequency input which is applied to PLL frequency synthesizer U4 via pin 3.

f. Two Modulus Prescaler Circuit. The two modulus prescaler circuit consists of; divide-by-8 counter/controller U10, variable (divide-by-10/11) modulus driver U11, buffer amplifier Q11, and transformers T4 and T5. The loop feedback frequency from the VCO is RC coupled to the base of Q11. Q11 is forward biased for class A operation via resistive network R23 and R24, and compensated for temperature and degeneration by emitter elements R36 and C42. The output of Q11 is the inverted loop feedback frequency which is transformer coupled to the clock input of U11. The divide-by-10/11 function of U11 is controlled by the state of the input signal at pin 14. U11 divides the input clock frequency by ten when U11-14 is high, and performs a divide-by-11 function when pin 14 is low. The divided-down loop feedback frequency from U11 is supplied to controller U10 in complementary form. U10 performs a divide-by-eight event count on the frequency applied to its CLK inputs. U10 control input signal (pin 6) is routed from U4-14, and is low until the event count of the swallow counter is complete, then high until the event count of the main counter is complete (main plus swallow counter additional counts). The signal at U10-6 is totally dependent on the count loaded into the programmable divider (main and swallow counters) of U4. The control input at U10-6 is logicly ORed to the control output at U10-2, such that if pin 6 is high the output of pin 2 is high;

thus, controlling the the divide-by-10/11 function of U11. The divided-down loop feedback frequency is output at U10-3 and transformer coupled (and inverted) to the variable frequency input at U4-3. The frequency of this input is applied to the programmable divider main and swallow counters, and completes the feedback loop.

g. UHF/VHF Select Switching. The UHF/VHF switching circuit switches the path of the RF signal from the VCO to the circuitry associated with UHF/VHF operations. UHF/VHF switching is provided by Q4 and Q13 which are turned on or off by the state of the UHF/VHF SEL line from U2-12. The output state of U2-12 is low for UHF operations, and high for VHF. When the RT is operated in the UHF band, Q13 is off and Q4 is on. This condition forward biases pin diodes CR21 and CR23, thus, permitting the VCO output to be coupled directly to the base of RF amplifier Q6 via C34. When the RT is operated in the VHF band, Q4 is cutoff and Q13 conducts. This condition reverse biases CR21 and CR23. CR22 is forward biased which forces the VCO output via this branch to ground. The VCO output path associated with VHF operations is via R104 and the VHF divide-by-two tracking circuit. The VHF divide-by-tracking is provided by mixer Z1, buffer amplifier Q12, and a LC oscillator consisting of T3, CR4, CR5, C24, C40, C57 and R42. The VCO output is input at Z1-1 and mixed with the desired VHF operating frequency present at the secondary of T3. Electrical tuning for the buffer amplifier is supplied from the loop integrator and mechanical tuning is via C24 and T3. The output at Z1-2 is an IF signal which is one half the VCO output frequency (e.g., the VHF operating frequency). The IF output is applied to the base of Q12 which is biased on when Q13 conducts. The output of Q12 is the desired VHF operating frequency, and is transformer coupled to Z1 and R106. Resistor R106 is a select component used in conjunction with C24 and T3 to insure the RF output power level across the VHF band is greater than +9.0 dBm. It is also used in conjunction with C44 to couple the RF signal to the base of RF amplifier Q6.

h. RF Output Stage. The selected RF signal from the VCO or VHF divide-by-two tracking circuit is RC coupled to the base of wideband RF amplifier Q6. Q6 is operated class A and is forward biased via R43, R108 and R109. Emitter resistors R101 and R110, in conjunction with CR25, provide temperature stabilization. Resistor R108 is a select component used in conjunction with bypass capacitors C25 and C45 to prevent degeneration and sets the emitter voltage of Q6 between +0.23 to +0.28 Vdc. Mechanical tuning components L11, L12, and L13 determine the transmit RF output power across the frequency range of 116.000 to 399.975 MHz. The adjustment of L11 affects the lower frequencies, L12 the higher frequencies, and L13 is the adjustment which controls the second harmonic output frequency. The minimum RF output power level across the UHF frequency range (225.000 to 399.975 MHz) is greater than +10.0 dBm in the transmit mode, and is established by the value of select component R112. Transmit output power to the modulator via J2 is +8.0 to +12.0 dBm for VHF operation, and +9.0 to +13.0 dBm for UHF. Receive output power to the main receiver via J3 is +7.0 to +12 dBm for VHF operation, and +9.0 to +13.0 dBm for UHF. The RF injection signal is switched to the appropriate output connector (J2/J3) via the receive/transmit switching circuit controlled by the state of the R/T KEY line (J1-26).

i. Receive/Transmit Switch. The receive/transmit switch controls routing of the RF injection signal to the modulator and main receiver. The switch uses Q7, CR26 and R119 to control the XMIT RF injection to the modulator; while Q8, CR27 and R121 controls the injection path to the main receiver. The circuit is controlled by the state of the R/T KEY line at J1-26. In the receive mode, the R/T KEY line is high

and Q7 is biased off permitting Q8 to be biased on by the -12.0 Vdc source applied to resistive network R116 through R119. The negative voltage across the resistive network also reverse biases CR26 which is used to attenuate the RF injection signal to J2 during receive operations. With Q8 on, reverse bias is removed from CR27 permitting the receiver RF injection to be routed to the main receiver via J3. It should be noted that the R/T KEY line will also be in the receive state (high) during low input power conditions or if the synthesizer should lose lock. In the transmit mode, the R/T KEY line is low, Q7 is biased on and the reverse bias is removed from CR27. This condition permits the XMIT RF injection signal to be routed to the modulator via J2. With Q8 biased off, CR27 attenuates the RF injection signal to the main receiver.

4-13. POWER SWITCHING ASSEMBLY A1A1A9. Refer to block diagram figure 4-12 and the foldout FO-14 at the rear of this manual. The nominal +24.0 Vdc input from each of the battery connectors enters the power switch through isolation diodes CR2 and CR3. The two input diodes provide isolation of the sources and prevents a discharged battery from placing a current drain on a fully charged battery. This input voltage is then applied to the source terminal of a series pass p-channel MOSFET Q1. When the front panel OFF/VOLUME switch is in the on position, ground is applied from P1-2 through MOSFET Q3 forward biasing Q1. This causes Q1 to turn on which permits the +24.0 Vdc to pass from Q1 drain to the power regulator, remote connector and the transmitter RF power stages. SCR Q2 is connected across the gate of Q1 to cause turnoff during gamma radiation and is a part of the nuclear hardening for the RT. Gamma radiation would result in gating the SCR and turning off Q1.

4-14. POWER REGULATOR ASSEMBLY A1A1A7. Refer to figure 4-13 for a block diagram of the power regulator and to the foldout FO-12 at the rear of this manual. The power regulator assembly consists of a single circuit card assembly. Power regulator circuits comprise input/output filters, two independent switching mode regulators and an input voltage comparator which provides a low battery visual alarm.

a. Regulated +6.3 and -29.0 Vdc Supplies. The +24.0 Vdc switched input from J1 pins 1 and 2 is applied through a low pass filter to the input series switch Q2 and to the bias input of switching mode regulator U1. A square wave drive signal from U1-16 controls the on-off cycle of series pass switch Q1 and CR1. The switched output of Q1 is filtered to produce the +6.3 Vdc source and applied to J2-1. A voltage comparator within U1 monitors a sample of the +6.3 Vdc reference. The comparator output determines the on-time pulse duration of Q1 drive signal to maintain +6.3 Vdc regulation. A current limiting circuit within U1 limits the duty factor base drive current to Q1. When Q1 switches off, shunt diode CR1 is biased on and electrical energy is induced from the flyback winding of transformer T1. This produces a -29.0 Vdc source which is applied through blocking diode CR3 and an output filter to J2-7.

b. Regulated +12.0 Vdc and -13.5 Vdc Supplies. The +24.0 Vdc switched input from J1 pins 1 and 2 is applied through a low pass filter to the input of series switch Q2 and to the bias input of switching mode regulator U2. A square wave drive signal from U2-16 controls the on/off cycle of series switch Q2 and CR2. The switched output of Q2 is filtered to produce the +12.0 Vdc output and compares it to an internal +1.3 Vdc reference. The comparator output determines the on-time pulse duration of the Q2 drive signal to maintain +12.0 Vdc regulation. A current limiting circuit within U2 limits the duty factor base drive current of Q2. When Q2

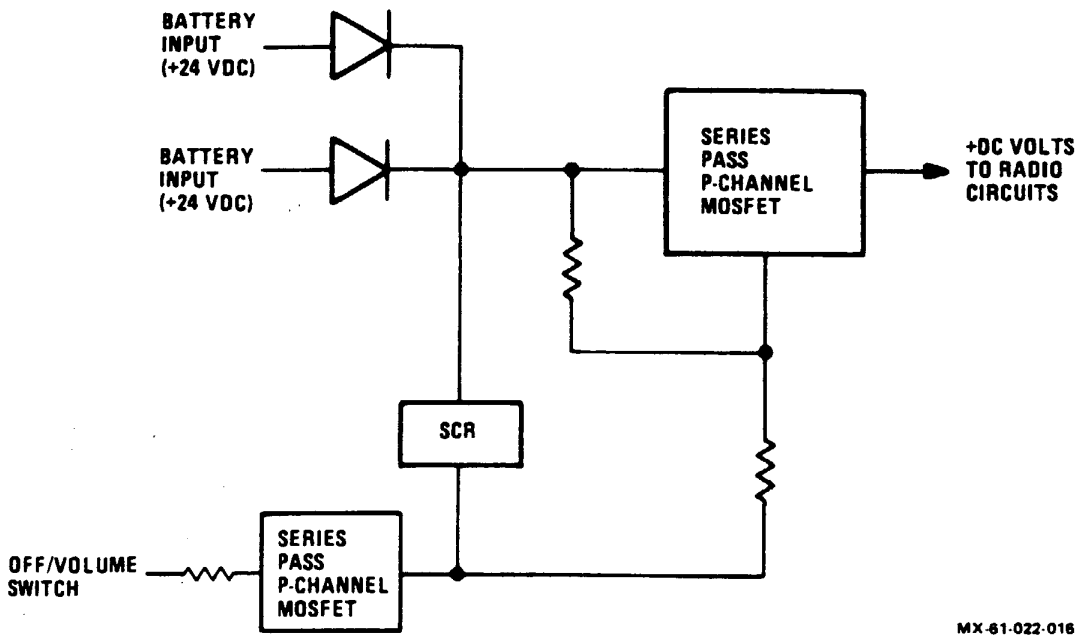


Figure 4-12. Power Switching CCA A9 Block Diagram

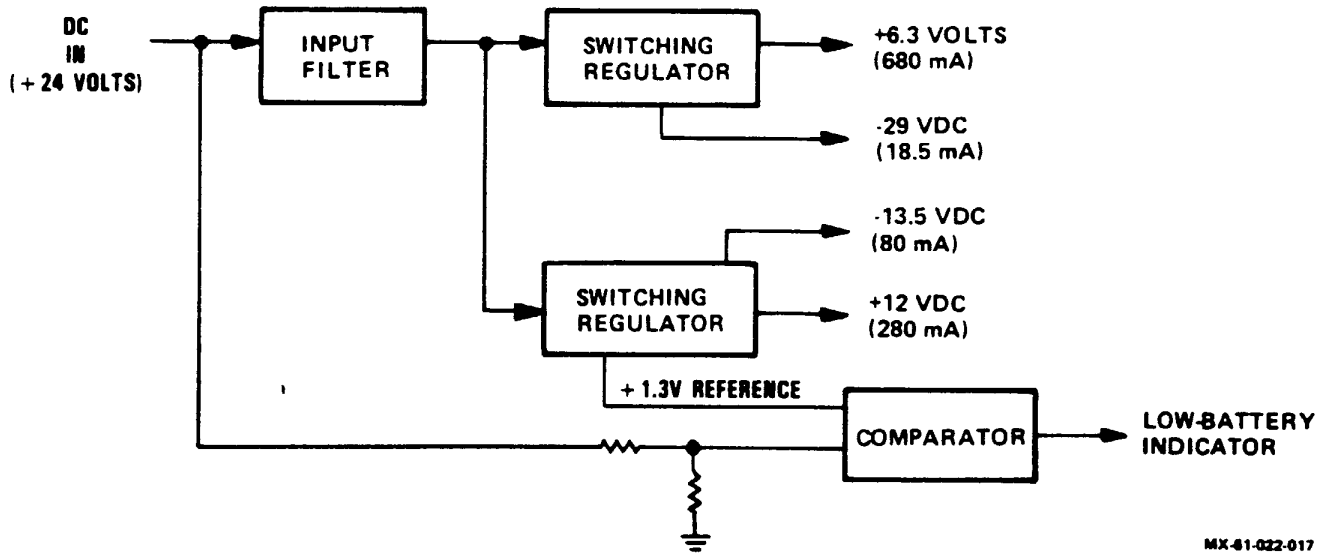


Figure 4-13. Power Regulator CCA A7 Block Diagram

switches off, shunt diode CR2 is biased on and electrical energy is induced across the flyback winding of transformer T2. This produces a -13.5 Vdc source which is applied through blocking diode CR4 and an output filter to J2-5. Transistor Q3 is a synchronous rectifier for the -13.5 Vdc supply.

c. Battery Sensing Circuit. A comparator circuit within switching mode regulator U2 monitors the input voltage and compares a portion of it against a +1.3 Vdc reference voltage. The comparator output (U2-4) provides a battery status signal that is routed to the data converter. When the comparator senses input voltages below +18.0 Vdc, the signal to the data converter LCD causes the decimal in the frequency display to blink.

CHAPTER 5

MAINTENANCE

Section I. ORGANIZATIONAL AND INTERMEDIATE MAINTENANCE

5-1. MAINTENANCE CONCEPT. Detailed organizational and intermediate level maintenance of the Receiver-Transmitter RT-1319/URC is not contained within this manual. Organizational and intermediate maintenance consists of fault isolation to the failed assembly, removal and replacement of failed assemblies, repair and replacement of connecting hardware, shipment of failed assemblies to a depot repair facility. Maintenance instructions for operator/organizational maintenance are contained in TO 31R2-2PRC113-1. Intermediate level maintenance instructions are contained in TO 31R2-2URC-62.

Section II. SPECIAL MAINTENANCE

5-2. GENERAL. Special maintenance consists of maintenance performed at the depot level. Maintenance instructions within this manual concern testing and repair of assemblies contained in the RT-1319/URC. These instructions include testing of removed assemblies, isolation to failed components, instructions for replacement of components which require special techniques, determining component values for components which are selected by test, and testing of repaired assemblies. For the purposes of this manual, it is assumed that the failed assembly has been removed at lower levels of maintenance and will be installed intermediate level. If removal or installation instructions for the assemblies are required, refer to TO 31R2-2URC-62. Schematic diagrams of the RT and for each assembly are furnished as foldout illustrations at the rear of this manual. Bench test setups, illustrations of component and test point location, and performance test tables are provided for each assembly repaired at the depot level. The instructions are presented in reference designation order, i.e., assembly A1A1A1, followed by A1A1A2 through A1A1A9. The test equipment required to perform special maintenance on the RT-1319/URC is listed in table 1-4. The trouble analysis diagrams are included as foldouts after the schematic diagrams. A trouble analysis diagram is provided for each assembly or CCA. These trouble analysis diagrams are based on symptoms that could occur during performance testing of the assembly or CCA. Use the applicable diagrams to determine the required corrective action. The trouble analysis diagrams do not cover all possible discrepancies or symptoms, but are provided as a guide for systematic troubleshooting.

5-3. NUCLEAR SURVIVABILITY MAINTENANCE. The following components are critical in maintaining the nuclear survivability of the RT-1319 in a nuclear environment.

a. Silicon Controlled Rectifier. The SCR, reference designation A1A1A9-Q1 (part number 646158-901) located on the Power Switch Assembly number 811963-801 circumvents the power supply when triggered by an ionizing pulse.

b. External Cables. All external cables are shielded to provide EMP protection and are not repairable.

c. Series Resistors. Microcircuits susceptible to EMP have series resistors on the inputs to prevent burn-out. Power supply pins of microcircuits also have series resistors to prevent burn-out during transient radiation.

5-4. DATA CONVERTER ASSEMBLY A1A1A1 TEST AND MAINTENANCE. The test and maintenance of data converter assembly A1A1A1 is accomplished using automatic test equipment (ATE).

NOTE

To insure compatability with "on-board" programming equipment, U7 on Memory I/O data converter Board CCA A1A1A1A2 PN 914871-XXX must be the same basic part number. Assembly 914871-805 contains devices which require +21 Vdc programming voltage (Vpp), while assembly 914871-807 requires +12.5 Vdc programming voltage (Vpp). If an assembly is to have U7 replaced, the replacement part must be the identical part number. If this part is not available, U7 must be replaced and the assembly dash number changed accordingly in order to properly identify the assembly.

5-5. TRANSMITTER ASSEMBLY A1A1A2 TEST AND MAINTENANCE. Initial test setup does not require further disassembly of the transmitter assembly. Transmitter Test Set TS-4093/URC (PN 812542-801) is required to perform test and alignment of the transmitter assembly. Detailed description of this test fixture is contained in TO 33D7-33-191-1. During RF output power test, the transmitter assembly must be mounted on the holding fixture so it can be cooled with airflow. All parts subject to failure are top accessible. An insulator is mounted between the board and the heat sink to electrically isolate the board component junctions. Inspect the suspect components in the failed stage visually under magnification for physical evidence of failure such as cracked capacitors, open inductors, overheated diodes or resistors. Table 5-1 contains the transmitter performance test procedures. Refer to FO-15 for the trouble analysis diagrams for fault locations listed under the performance standards column. Table 5-2 contains the transmitter alignment procedures. The transmitter must be aligned in the following order:

a. VHF filter
b. UHF filter
c. two watt filter selection
d. ten watt filter selection
e. directional coupler.

Figure 5-1 shows the transmitter performance test connections. Figure 5-2 shows the transmitter alignment connections. Figure 5-3 shows the component and test point locations.

5-6. MODULATOR ASSEMBLY A1A1A3 TEST AND MAINTENANCE. Initial test setup does not require further disassembly of the modulator assembly. Modulator Test Set TS-4092/URC (PN 812544-801) is required to perform test and alignment of the modulator assembly. Detailed description of this test set is contained in TO 33DA48-25-1. Table 5-3 contains the modulator latch states for standard test modes. Table 5-4

provides the preliminary calibration set up procedure for the modulator test set. This procedure need only be done the first time the test set is used, provided the same test set, attenuator, and 2 W amplifier are used for each subsequent test. Performance tests are contained in Table 5-5. Refer to FO-16 for the trouble analysis diagrams for fault locations listed under the performance standards column. Performance test connection setup is shown in figure 5-4. Test connections for modulator alignment setup are shown in figure 5-5. Component and test point locations are shown in figure 5-6. The modulator alignment procedures are contained in table 5-6.

5-7. MAIN RECEIVER ASSEMBLY A1A1A4 TEST AND MAINTENANCE. Initial test setup does not require further disassembly of the main receiver assembly. Receiver Test Set TS-4091/URC (PN 812539-801) is required to perform test and alignment of the main receiver. Detailed description of this test fixture is contained in TO 33D7-36-51-1. Table 5-7 contains the main receiver linear tune volts and lists the corresponding UHF frequency and J2 injection frequency. Table 5-8 lists the main receiver mode select switch settings. Table 5-9 contains the main receiver performance test procedures. Refer to FO-17 for the trouble analysis diagrams for fault locations listed under the performance standards column. Table 5-10 contains the main receiver alignment procedures. Figure 5-7 shows the equipment connections required for main receiver performance test. Figure 5-8 shows the equipment connections required for main receiver alignment. Figure 5-9 shows the main receiver component and test point locations.

5-8. GUARD RECEIVER ASSEMBLY A1A1A5 TEST AND MAINTENANCE. Initial test setup does not require further disassembly of the guard receiver assembly. Receiver Test Set TS-4091/URC (PN 812539-801) is required to perform test and alignment of the guard receiver. Detailed description of this test fixture is contained in TO 33D7-36-51-1. Table 5-11 contains the guard receiver performance test procedure. Refer to FO-18 for the trouble analysis diagrams for fault locations listed under the performance standards column. Table 5-12 contains the guard receiver alignment procedures. Figure 5-10 shows the equipment connections required for guard receiver performance test. Figure 5-11 shows the equipment connections required for guard receiver alignment. Figure 5-12 shows the guard receiver component and test point locations.

5-9. SYNTHESIZER ASSEMBLY A1A1A6 TEST AND MAINTENANCE. Initial test setup does not require further disassembly of the synthesizer assembly. Synthesizer Test Set TS-4141/URC (PN 815155-801) is required to perform test and alignment of the synthesizer assembly. Detailed description of this test set is contained in TO33A1-5-497-1. Table 5-13 contains the synthesizer performance test procedure. Refer to FO-19 for the trouble analysis diagrams for fault locations listed under the performance standards column. Figure 5-13 is the synthesizer performance test and alignment connection diagram. Table 5-14 contains the synthesizer alignment procedures. Figure 5-14 shows the synthesizer component and test point locations.

5-10. POWER REGULATOR ASSEMBLY A1A1A7 TEST AND MAINTENANCE. Initial test setup does not require further disassembly of the power regulator assembly. Power Converter Test Set TS-4090/GRC-206(V) (PN 812540-801) is required to perform test and alignment of the power regulator. Detailed description of this test fixture is contained in TO 33DA7-17-1. Table 5-15 contains the power regulator performance

test procedure. Refer to FO-20 for the trouble analysis diagrams for fault locations listed under the performance standards column. Figure 5-15 shows the power regulator performance test connections. Figure 5-16 shows the power regulator component and test point locations.

5-11. CHASSIS ASSEMBLY A1A1A8 TEST AND MAINTENANCE. Initial test setup does not require further disassembly of the chassis assembly. All testing is done with an Ohmmeter. Table 5-17 contains the chassis assembly performance test procedure. Figure 5-17 shows the chassis assembly component and test point locations.

5-12. POWER SWITCHING ASSEMBLY A1A1A9 TEST AND MAINTENANCE. Initial test setup does not require further disassembly of the power switching assembly. Special test fixture TS-4094/URC (PN 812541-801) is required to test the power switching assembly. Detailed description of this test fixture is contained in TO 33D7-33-190-1. Test and maintenance instructions are contained in table 5-17. Refer to FO-21 for the trouble analysis diagrams for fault locations listed under the performance standards column. Figure 5-18 shows the power switching assembly performance test connection diagram. Figure 5-19 shows the power switching assembly component and test point locations.

Section III. PERFORMANCE TEST CHECKS

5-13. PERFORMANCE TEST CHECKS. Performance test checks to measure the overall performance of Receiver-Transmitter RT-1319/URC are accomplished at intermediate maintenance level. Refer to TO 31R2-2URC-62. Refer to the trouble analysis diagrams in this chapter and the fold out schematics provided at the back of this manual as needed.

Table 5-1. Transmitter CCA A1A1A2 Performance Test Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			Thermistor Resistance	
1.	Mount transmitter in holding fixture as shown in figure 5-3.			(See figure 5-20 for trouble analysis)
2.	Connect equipment as shown in Figure 5-1. Connect -29 Vdc red terminal to + and black to -. The test set inverts polarity internally. Do not use ground jumper from (-) terminal to ground on power supply.			
			TEST PRESETS Preset test set controls as follows:	
			Control — Position	
3.			S5 AMPLIFIER/BIAS — AMPLIFIER	
4.			S4 TRANSMITTER/DRIVER/PA — TRANSMITTER	
5.			S2 VHF/RCV/UHF — VHF	
6.			S3 10W/2W — 2W	
			NOTE Chassis must be at or near room temperature for next measurement.	

Table 5-1. Transmitter CCA A1A1A2 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
7.	Connect DMM	Test set TP-10, TP-14	Set multimeter for resistance measurement.	6 to 10 kOhms (L50,R44,RT1, C101,C94)
8.	Disconnect DMM			
			RF Power Input	
			CAUTION Do not allow transmitter to become too hot to comfortably touch during tests.	
9.	Connect power meter between input and output coaxial transfer switches as shown in Figure 5-2 as needed in following steps.		Turn on power supplies. Adjust 22.5/24 V power supply to 24 V. Set test set POWER ON/OFF switch S1 to ON. Set transmitter holding assembly ON/OFF switch S1 to ON. Turn on RF power amplifier.	
			NOTE Be sure to take into account the attenuation losses for transmitter inputs and outputs for following tests.	
10.	Signal generator		Adjust signal generator to 116 mHz.	
11.	Power meter	J2	Increase signal generator RF power until transmitter output at J2 is 38.2 dBm.	
12.	Power meter	J1	Read RF power input.	$\leq$ +19 dBm
13.	Power meter	J2	Decrease signal generator to obtain 32 dBm RF power output at J2.	

Table 5-1. Transmitter CCA A1A1A2 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
14.	Test set	M1	Read 24 Vdc current. **NOTE** dbc = decibels under carrier; i.e. as read on spectrum analyzer, this reading is measurement of a harmonic with respect to carrier frequency amplitude.	$\leq$ 0.60 A
15.	Spectrum analyzer	J2	Read second harmonic of 116 MHz.	$\geq$ -60 dbc
16.	Spectrum analyzer	J2	Read third harmonic of 116 MHz.	$\geq$ -60 dbc
17.	Test set	TP11	Read FWD PWR voltage.	0.45 $\pm$ 0.10 Vdc
18.	Signal generator		Reduce signal generator output.	
19.			Repeat steps 9-17 for 120, 130, 140, and 150 MHz. Omit harmonic measurements at 120, 130 and 140 MHz.	
20.			Set test set VHF/RCV/UHF switch S2 to UHF.	
21.			Repeat steps 9-17 for 225, 260, 300, 350 and 400 MHz. Omit harmonic measurements at 225, 350 and 400 MHz.	
22.			Set test set 10W/2W switch S3 to 10W.	
23.			Set test set VHF/RCV/UHF switch S2 to VHF	

Table 5-1. Transmitter CCA A1A1A2 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
24.	Signal generator	J1	Adjust signal generator to 116 mHz.	
25.	Power meter	J2	Increase signal generator RF power until transmitter output at J2 is 44.4 dBm.	
26.	Power meter	J1	Read RF power input.	≤ 20 dBm
27.	Power meter	J2	Decrease signal generator RF power output to obtain 39 dBm at J2.	
28.	Test set	M1	Read 24 Vdc current.	≤ 2.2 A
			NOTE dbc = decibels under carrier; i.e. as read on spectrum analyzer, this reading is measurement of a harmonic with respect to carrier frequency amplitude.	
29.	Spectrum analyzer	J2	Read second harmonic of 116 MHz.	≥ -60 dBc
30.	Spectrum analyzer	J2	Read third harmonic of 116 MHz.	≥ -60 dBc
31.	Test Set and DMM	TP11 FWD PWR	Read voltage at FWD PWR terminal	1.32 ± 0.10 Vdc
32.	Test Set and DMM	TP12 REF PWR	Increase signal generator RF power until transmitter output at J2 is 44.4 dBm RF output.	≤ 0.10 Vdc
33.	Signal generator		Reduce signal generator output.	

Table 5-1. Transmitter CCA A1A1A2 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
34.			Repeat steps 22-31 for 120, 130, 140, 150 MHz. Omit harmonic measurements at 150 MHz. Omit step 30.	
35.			Set test set VHF/RCV/UHF switch to UHF.	
36.			Repeat steps 22-31 for 225, 250, 275, 300, 325, 350, and 375 MHz. Omit harmonic measurements at 250 and 300 MHz. Omit step 30.	
37.			Repeat steps 22-31 for 400 MHz. Omit harmonic measurements at 400 MHz.	
38.	Connect DMM to Test set TP12. Disconnect cable from J2.	TP12	While performing 400 MHz tests for steps 25-29, read DC voltage at REF PWR test point with J2 disconnected.	$\geq$ 0.2 Vdc
			Receive-Transmit Diode Switch Test	
39.	Connect power meter directly to signal generator as shown in figure 5-1 sheet 2.		Calibrate signal generator output to 0 dBm at 116 MHz.	
40.			Set test set VHF/RCV/UHF switch S2 to REC.	

Table 5-1. Transmitter CCA A1A1A2 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
41.	Connect signal generator to J2.			
42.	Connect power meter to J3.	J3	Read receive switch loss on power meter.	$\leq$ 1.5 dB
43.			Repeat steps 39 to 42 for 400 MHz.	
44.	End of test. Deenergize and remove test set and test equipment from UUT.			

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			VHF Filter Alignment	
1.	Connect equipment as shown in Figure 5-2			
2.			Ensure that minimum of two pounds per minute of airflow is directed onto transmitter CCA during RF power output tests.	
3.	Connect signal generator to spectrum analyzer.		Adjust signal generator to 0 dBm output at 232 MHz.	
4.			Adjust spectrum analyzer for 50 MHz per centimeter display and 400 MHz center.	
5.			Adjust 232 MHz signal display for -10 dB from full scale on spectrum analyzer.	
6.	Remove C27 and install 470 pf capacitor at junction of L29, CR9 and CR 10. Attach length of small coax cable to input side of C27 to allow connection of test equipment. (see figure 5-2.)			

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
7.	Connect signal generator to coax cable soldered to C27.			
8.	Connect spectrum analyzer to J2.			
9.			Set test set POWER ON/OFF switch S1 to ON. Set transmitter holding assembly ON/OFF switch S1 to ON.	
10.			Set test set VHF/RCV/UHF switch to VHF.	
			NOTE It is permissible to use a solder fillet on an inductor turn to decrease inductance if spreading turns does not provide adequate range.	
11.	Spectrum analyzer	J2	Adjust L72 for minimum display of spectrum analyzer 232 MHz signal. Remove 10 dB of RF attenuation from spectrum analyzer to obtain range of at least 70 dB.	$\geq$ -60 dB lower than full scale.
12.			Set signal generator to 256 MHz.	
	Spectrum analyzer	J2	Adjust L71 for minimum display of 256 MHz signal.	$\geq$ -60 dB rejection
13.				

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
14.			Set signal generator to 329 MHz.	
15.	Spectrum analyzer	J2	Adjust L73 for minimum display of 329 MHz signal.	≥ -55 dB rejection.
16.	Connect signal generator to C27.			
17.	Connect spectrum analyzer to J2.	J2	Measure rejection of filter from 232 to 350 MHz.	≥ -55 dB rejection.
18.	Spectrum analyzer	J2	Measure rejection of filter from 351 to 450 MHz.	≥ -50 dB rejection.
19.			Calibrate RHO-Tector, oscilloscope and sweep generator so that 1.50:1 VSWR provides 3 centimeter display on oscilloscope over 100 MHz to 200 MHz frequency range.	
20.	Connect RHO-Tector Z1 to C27.			
21.	Connect 50 Ohm load to J2.			
			NOTE The 232, 256 and 329 MHz traps may be adjusted slightly if required to meet 1.5 CM display. Moving trap frequency will affect following rejection test.	

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
22.	Oscilloscope	C27	Adjust L66, 67, 68, 69 and 70.until display of 1.5 centimeters or less is obtained on oscilloscope over 116 to 150 MHz frequency range; or VSWR of 1.33:1 or less may be used as limit.	$\leq$ 1.5 cm scope display over 116 to 150 MHz range; or 1.33:1 VSWR.
			UHF Filter Section Alignment	
23.			Set test set POWER ON/OFF switch to OFF.	
24.	Connect signal generator to spectrum analyzer.		Adjust signal generator to 0 dBm output at 453 MHz.	
25.			Adjust spectrum analyzer for 50 MHz per centimeter display and 600 MHz center.	
26.			Adjust 453 MHz signal display for -10 dB from full scale on spectrum analyzer.	
27.	Connect signal generator to coax cable soldered to C27.	C27		
28.	Connect spectrum analyzer to J2.	J2		
29.			Set test set POWER ON/OFF switch S1 to ON.	

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
30.			Set test set VHF/RCV/UHF switch to UHF. **NOTE** It is permissible to use a solder fillet on an inductor turn to decrease inductance if spreading turns does not provide adequate range.	
31.	Spectrum analyzer	J2	Adjust L61 and L63 equally for minimum display of spectrum analyzer 453 MHz signal. Remove 10 dB of RF attenuation from spectrum analyzer to obtain range of at least 70 dB.	$\geq$ 55 dB lower than full scale
32.			Set signal generator to 480 MHz.	
33.	Spectrum analyzer	J2	Adjust L59 for minimum 453 MHz display.	$\geq$ -50 dB rejection
34.			Set signal generator to 577 MHz.	
35.	Spectrum analyzer	J2	Adjust L64 for minimun 577 MHz display. **NOTE** It is permissible to use a solder fillet on an inductor turn to decrease inductance if spreading turns does not provide adequate range.	$\geq$ -55 dB rejection

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			NOTE The 452, 480 and 577 MHz traps may be adjusted slightly if required to meet 1.5 cm display. Moving trap frequency will affect following rejection test.	
36.			Calibrate RHO-Tector, oscilloscope and sweep generator so that 1:50 VSWR provides 3 centimeter display on oscilloscope over 200 MHz to 400 MHz frequency range.	
37.	Connect RHO -Tector to C27.			
38.	Connect 50 Ohm load to J2.			
39.	Oscilloscope	J1	Adjust L57, 58, 60, 62 and 65 until display of 1.5 centimeters or less is obtained on oscilloscope over 225 to 400 MHz frequency range, or VSWR of 1.33:1 or less may be used as limit.	$\leq$ 1.33:1 VSWR
40.	Connect signal generator to C27.			
41.	Connect spectrum analyzer to J2.	J2	Measure rejection of filter from 452 to 500 MHz.	$\geq$ -48 dB rejection

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
42.		J2	Measure rejection of filter from 500 to 600 MHz.	≥ -47 dB rejection
43.			Turn test set POWER ON/OFF switch S1 to OFF.	
44.	Disconnect and normalize test equipment.			
45.	Solder original C27 in place.			
			Two Watt Power Section	
			NOTE	
			This section is aligned to provide 38.2 dBm RF power output with 19 dBm RF input maximum from 116 to 150 MHz and 225 to 400 MHz. Maximum 24 Vdc current of 0.60 A at 32 dBm RF output is allowed.	
46.	Connect equipment as shown in Figure 5-1 sheet 1 Connect power meter to UUT J2 via 30 dB attenuator and coaxial transfer switch.			
47.			Set test set AMPLIFIER/ BIAS switch S5 to AMPLIFIER.	

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
48.			Set test set TRANSMITTER-DRIVER/PA switch S4 to TRANSMITTER.	
49.			Set test set VHF/RCV/UHF switch S2 to UHF	
50.			Set test set 10W/2W switch to 2W.	
51.			Set test set POWER ON/OFF switch S1 to ON. CAUTION Do not allow 24 VDC current to exceed 1.4 A during alignment of this section to avoid damaging Q1 and Q3. CAUTION Do not allow transmitter chassis to become too hot to comfortably touch during alignment.	
52.			Adjust signal generator to 400 MHz.	
53.	Signal generator	J1	Adjust signal generator output to obtain approximately 13 dBm RF input power to transmitter.	

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
54.	Power meter	J2	Adjust L2, L3, L8 and L9 to obtain maximum output power. Spread or compress inductor turns to decrease or increase their inductance respectively. CAUTION Do not allow 24 VDC current to exceed 1.4 A during alignment of this section to avoid damaging Q1 and Q3. NOTE If spreading inductor turns does not provide sufficient range, it is permissible to put solder fillets in inductor turns. NOTE Capacitors C3 and C4 on Q1 base and C14 and C15 on Q3 base may require repositioning during alignment to obtain proper power output across 225 to 400 MHz frequency range.	
55.	Power meter	J2	Increase RF input until output power =38.2 dBm. Do not exceed 19 dBm RF input.	38.2 dBm RF output
56.	Test set	M1	Read 24 Vdc current.	$\leq$ 0.60 A
57.	Power meter	J2	Measure RF input return loss. (Capacitor C3 and C4 positioning affects return loss.)	> -5 db @400 MHz

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
58.			Reduce RF input.	
59.			Set test set VHF/RCV/UHF switch S2 to VHF.	
60.	Power meter	J1, J2	Adjust signal generator to 125 MHz.	Adjust for approximately 13 dBm of RF input power or until output power is 25 dBm, whichever occurs first.
61.	Power meter	J2	Adjust L1, L6 and L11 for maximum RF output. Spread or compress turns for adjustment as needed.	
62.	Power meter	J2, J1	Adjust RF input to obtain 38.2 dBm output power. Do not exceed 19 dBm input power.	38.2 dBm RF output power. RF input return loss >5 dB.
63.			Repeat step 62 for 116 to 150 MHz range. Some compromise of L1, L6 and L11 adjustments are required to obtain best overall range.	
64.	Test set	M1	Measure 24 Vdc current at 32 dBm RF output.	<0.60 A at all frequencies.
65.			Set test set VHF/RCV/UHF switch S2 to UHF.	

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
66.			Adjust signal generator to 400 MHz.	
67.			Repeat step 62 for 225 to 400 MHz range. Some compromise of L1, L6 and L11 adjustments performed in steps 54 thru 57 are required to obtain best overall range.	
68.			Repeat step 64 over 225 to 400 MHz range.	
69.			Repeat steps 59 to 62 for 116 to 150 MHz range if major adjustments were made in UHF range.	
			Ten Watt Power Section	
			NOTE This section is aligned to provide 44.4 dBm RF power output with 20 dBm RF input maximum from 116 to 150 MHz and 225 to 400 MHz. Maximum 24 Vdc current of 2.2 A at 39 dBm RF output is allowed.	
70.	Connect equipment as shown in Figure 5-1 sheet 1. Connect power meter to UUT J2 via coaxial transfer switch.			

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
71.			Set test set AMPLIFIER/ BIAS switch S5 to AMPLIFIER.	
72.			Set test set TRANSMITTER-DRIVER/PA switch S4 to TRANSMITTER.	
73.			Set test set VHF/RCV/UHF switch S2 to UHF	
74.			Set test set 10W/2W switch to 10W. **CAUTION** Do not allow 24 VDC current to exceed 5.5 A during alignment of this section to avoid damaging Q1, Q3 or Q4. **CAUTION** Do not allow transmitter chassis to become too hot to comfortably touch during alignment.	
75.			Set test set power switch S1 to ON.	
76.			Adjust signal generator to 400 MHz. **CAUTION** Use less RF input power if output power is over 15 Watts during alignment.	

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
77.	Signal generator	J1	Adjust signal generator output to obtain approximately 13 dBm RF input power to transmitter.	
78.		J2	Adjust L18, L19, L75, L76, L79, L80, L25, L82, L26 and L84 to obtain maximum output power. With metal end of tuning tool, short out portion of a coil loop to decrease inductance respectively. **CAUTION** Remove RF input power and turn off power supplies before soldering circuitry. **NOTE** If spreading inductor turns does not provide sufficient range, it is permissible to put solder fillets in inductor turns. **NOTE** Capacitors C37 and C38 on Q4 base may require repositioning during alignment to obtain proper power output across 225 to 400 MHz frequency range.	$\leq$ 15 W
79.	Power meter Test set	J2 M1	Increase RF input. Do not exceed 20 dBm RF input.	44.4 dBm RF output Approx. 3.5 A (24 Vdc current).

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
80.			Set test set VHF/RCV/UHF switch S2 to VHF	
81.	Signal generator	J1	Adjust signal generator to 125 MHz and for approximately 13 dBm of RF input power.	
82.	Power meter	J2	Adjust L52, and L83 for maximum RF output. Spread or compress turns for adjustment as needed. **NOTE** These inductors affect UHF band so that some compromises are necessary.	
83.	Power meter	J2	Adjust RF input to obtain 44.4 dBm output power.	RF input power < 20 dBm.
84.	Power meter	J2	Repeat step 83 for 116 to 150 MHz range. Some compromise of inductor adjustments are required to obtain best overall range.	
85.	Test set	M1	Measure 24 Vdc current at 39 dBm RF output.	< 2.2 A at all frequencies.
86.			Set test set VHF/RCV/UHF switch S2 to UHF.	
87.			Adjust signal generator to 400 MHz.	

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
88.			Repeat step 83 for 225 to 400 MHz range. Some compromise of inductor adjustments performed in step 78 is required to obtain best overall range.	
89.			Repeat step 83 over 225 to 400 MHz range.	
90.			Repeat steps 80, 83 and 84 for 115 to 150 MHz range if major adjustments were made in UHF range.	
			Directional Coupler Alignment	
			NOTE This section is aligned to provide directional coupler output of 1.0 ± 0.10 Vdc with 0.10 Vdc maximum delta at 39 dBm RF output level across 116 to 150 MHz and 225 to 400 MHz frequency bands.	
91.	Connect equipment as shown in Figure 5-1 sheet 1. Connect power meter to UUT J2 via 30 dB coupler and coaxial transfer switch.			

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
92.			Set test set AMPLIFIER/ BIAS switch S5 to AMPLIFIER.	
93.			Set test set TRANSMITTER-DRIVER/PA switch S4 to TRANSMITTER.	
94.			Set test set 10W/2W switch to 10W.	
95.			Set test set VHF/RCV/UHF switch S2 to UHF	
96.			Set test set POWER ON/OFF switch to ON.	
97.			Adjust signal generator to 400 MHz.	
98.	Power meter	J2	Increase signal generator output. **NOTE** Covers should be on filters and coupler for reading.	Approximately 39 dBm RF output power from transmitter.
99.	Test set	TP11 FWD PWR	Measure voltage at FWD PWR terminal. If voltage reading is not close to required value, change R20 to one of the values on parts list. To increase voltage, use lower value and vice versa.	Approximately 1.0 Vdc.

Table 5-2. Transmitter CCA A1A1A2 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
100.	Test set	TP12 REF PWR	Measure voltage at REF PWR terminal with 44.4 dBm RF output level. If voltage is higher than required value, go to step 101. If voltage is ok, go to step 103.	<0.10 Vdc
101.			Reduce RF output power. **NOTE** The next step may require several attempts; also FWD PWR reading will be affected.	
102.			Adjust turns of L42 or L43 (one only) closer together and repeat steps 98, 99, 100.	
103.			Reduce RF output power.	
104.			Repeat steps 97, 98, 99 and 100 at several UHF and VHF frequencies.	
105.	End of test. Deenergize and remove test set and test equipment from UUT.			

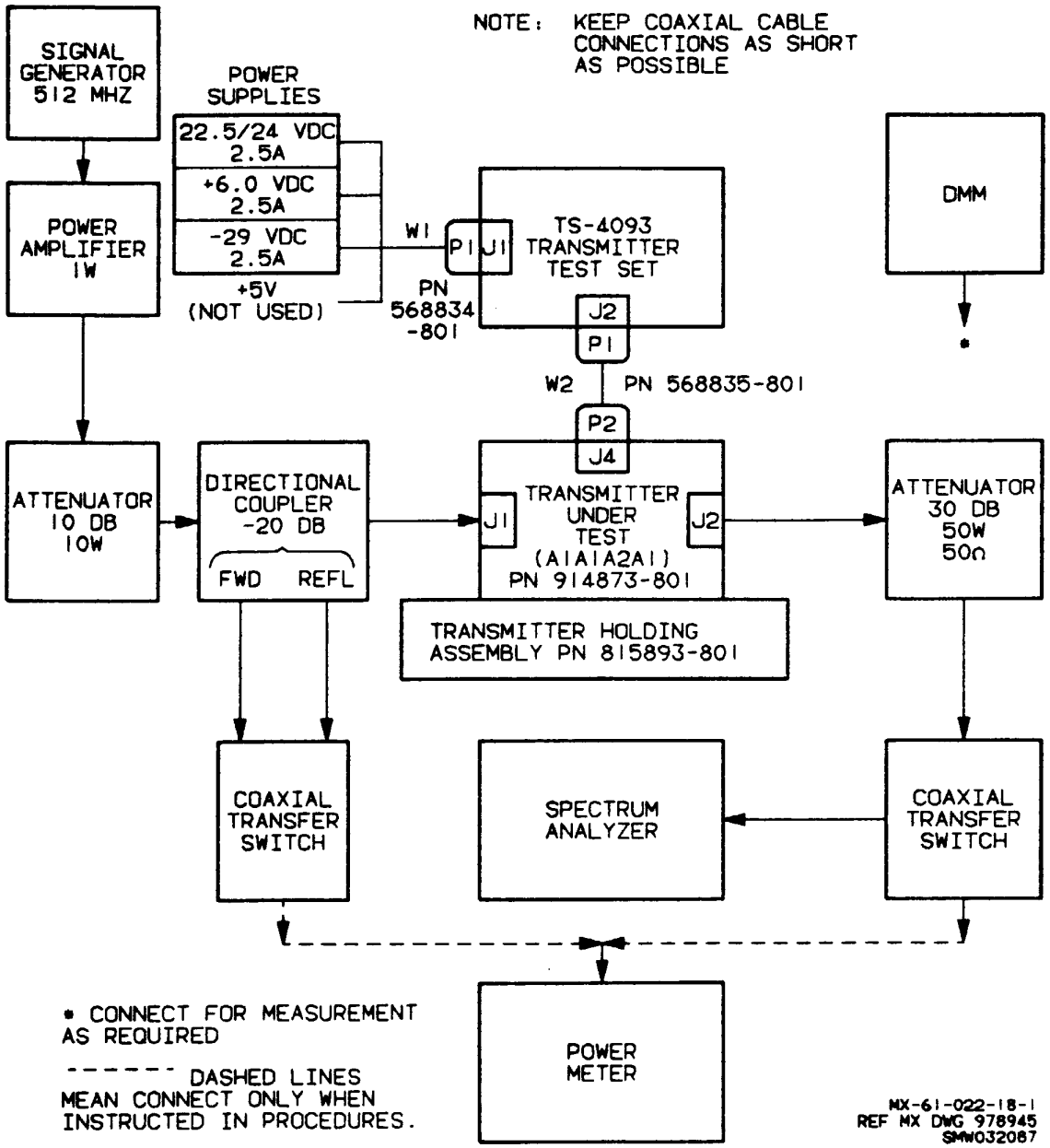


Figure 5-1. Transmitter CCA A1A1A2 Performance Test/Alignment Connection Diagram (Sheet 1 of 2)

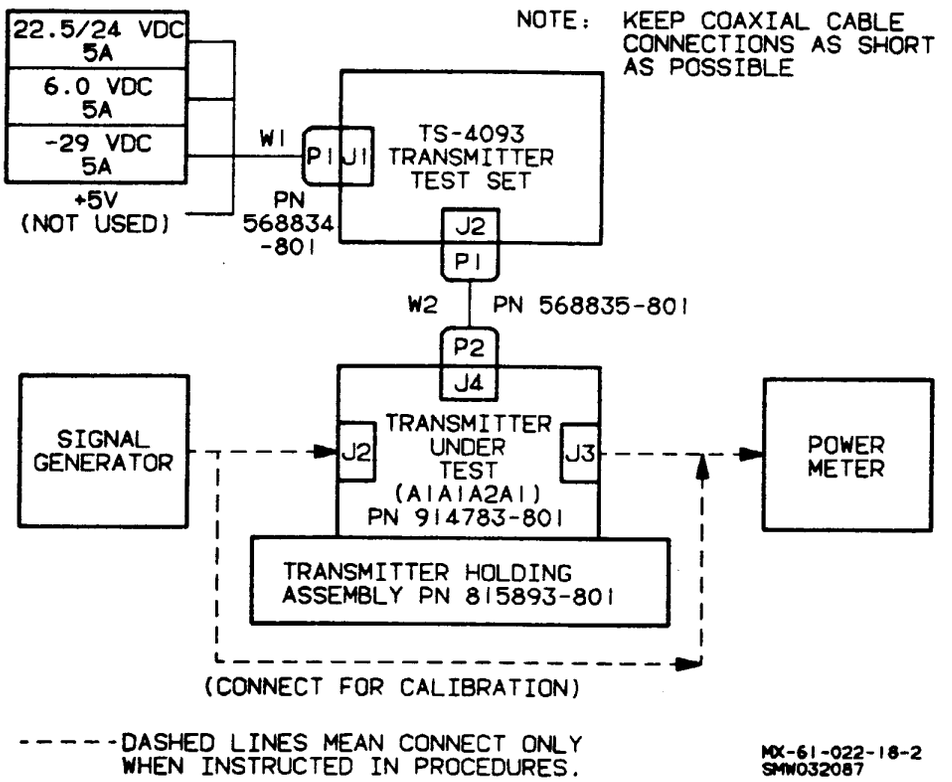


Figure 5-1. Transmitter CCA A1A1A2 Performance Test/Alignment Connection Diagram (Sheet 2 of 2)

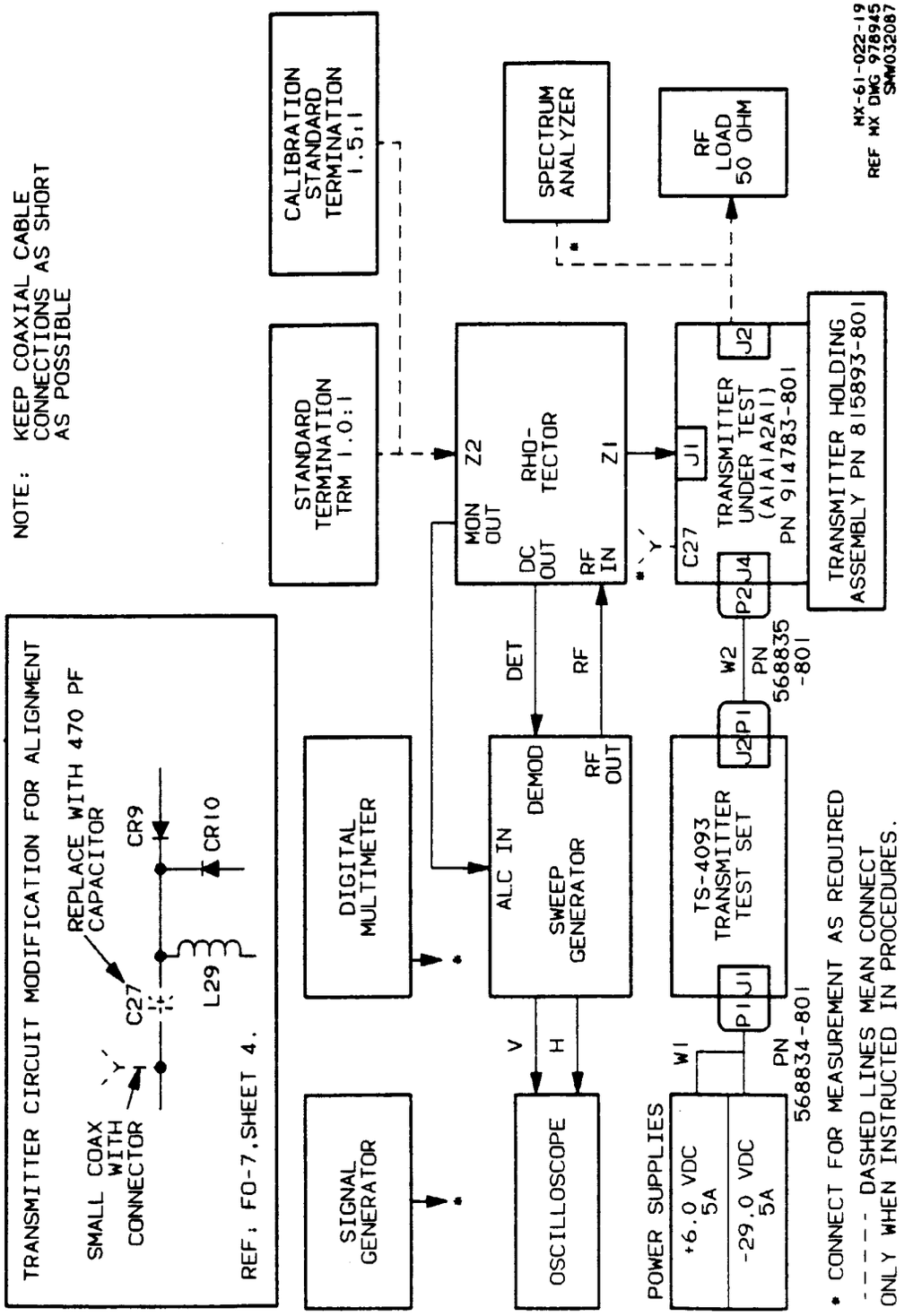


Figure 5-2. Transmitter CCA A1A1A2 Alignment Connection Diagram

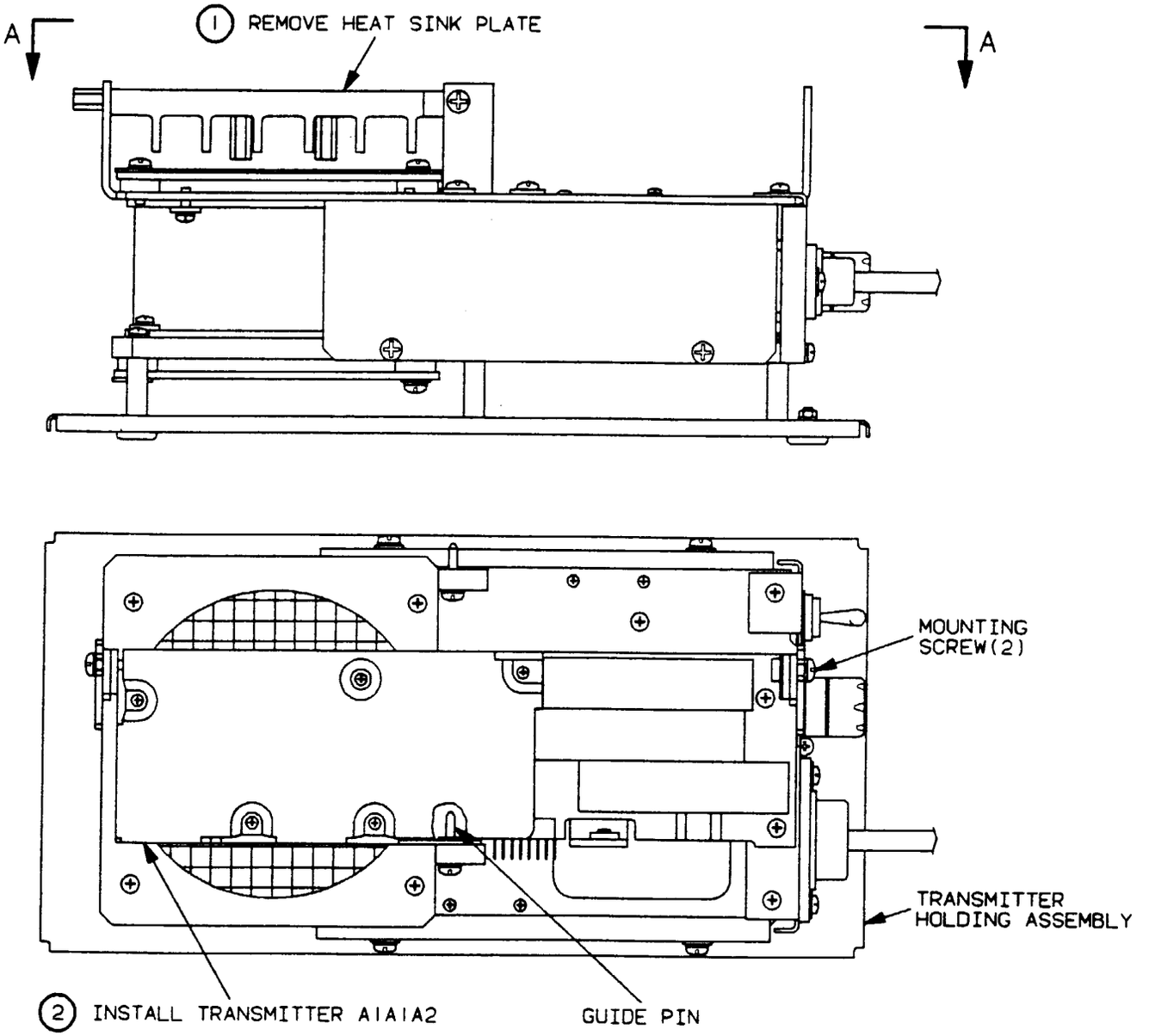


Figure 5-3. Transmitter CCA A1A1A2
Component and Test Point Location Diagram (Sheet 1 of 6)

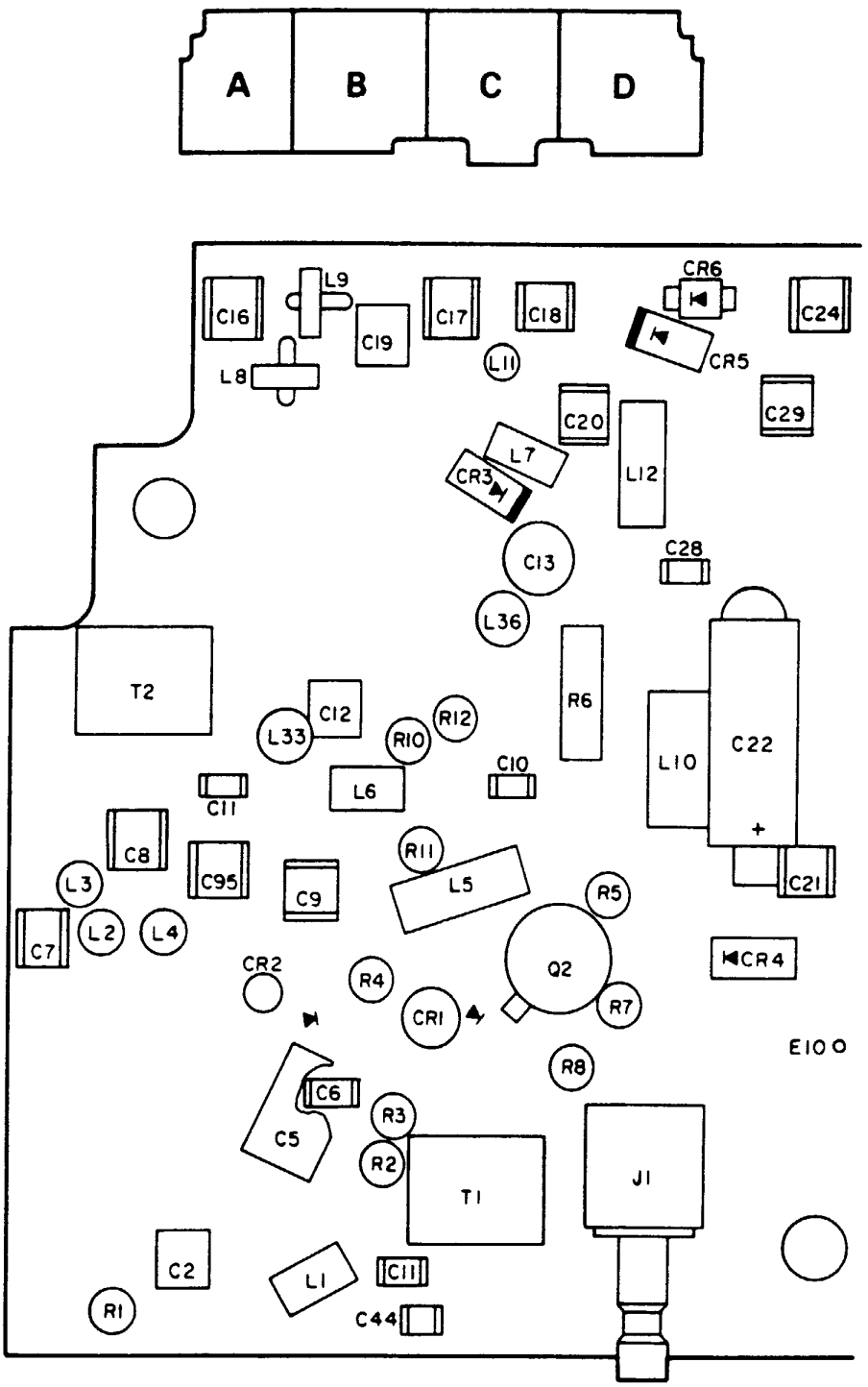


Figure 5-3. Transmitter CCA A1A1A2
Component and Test Point Location Diagram (Sheet 2 of 6)

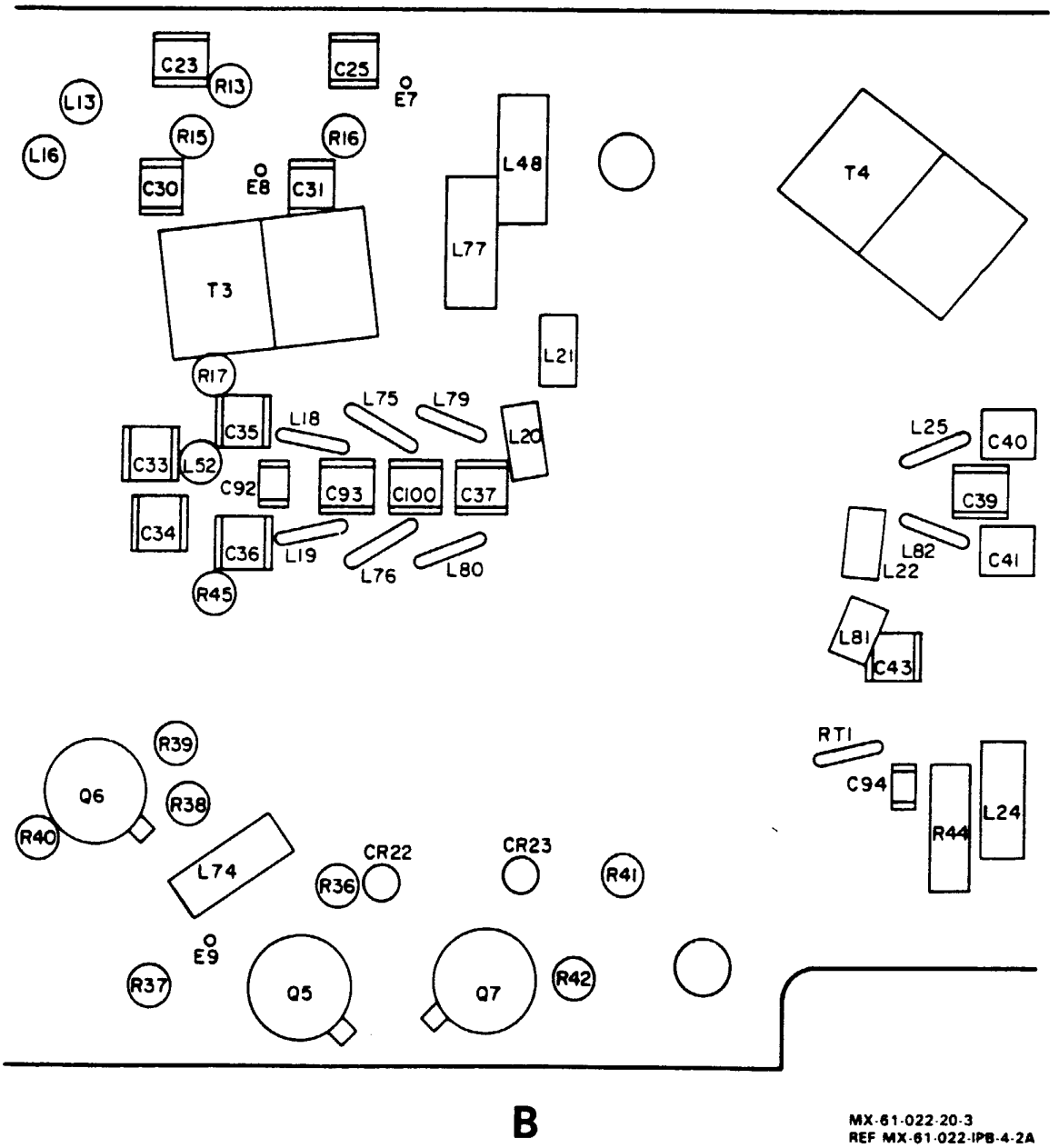


Figure 5-3. Transmitter CCA A1A1A2
Component and Test Point Location Diagram (Sheet 3 of 6)

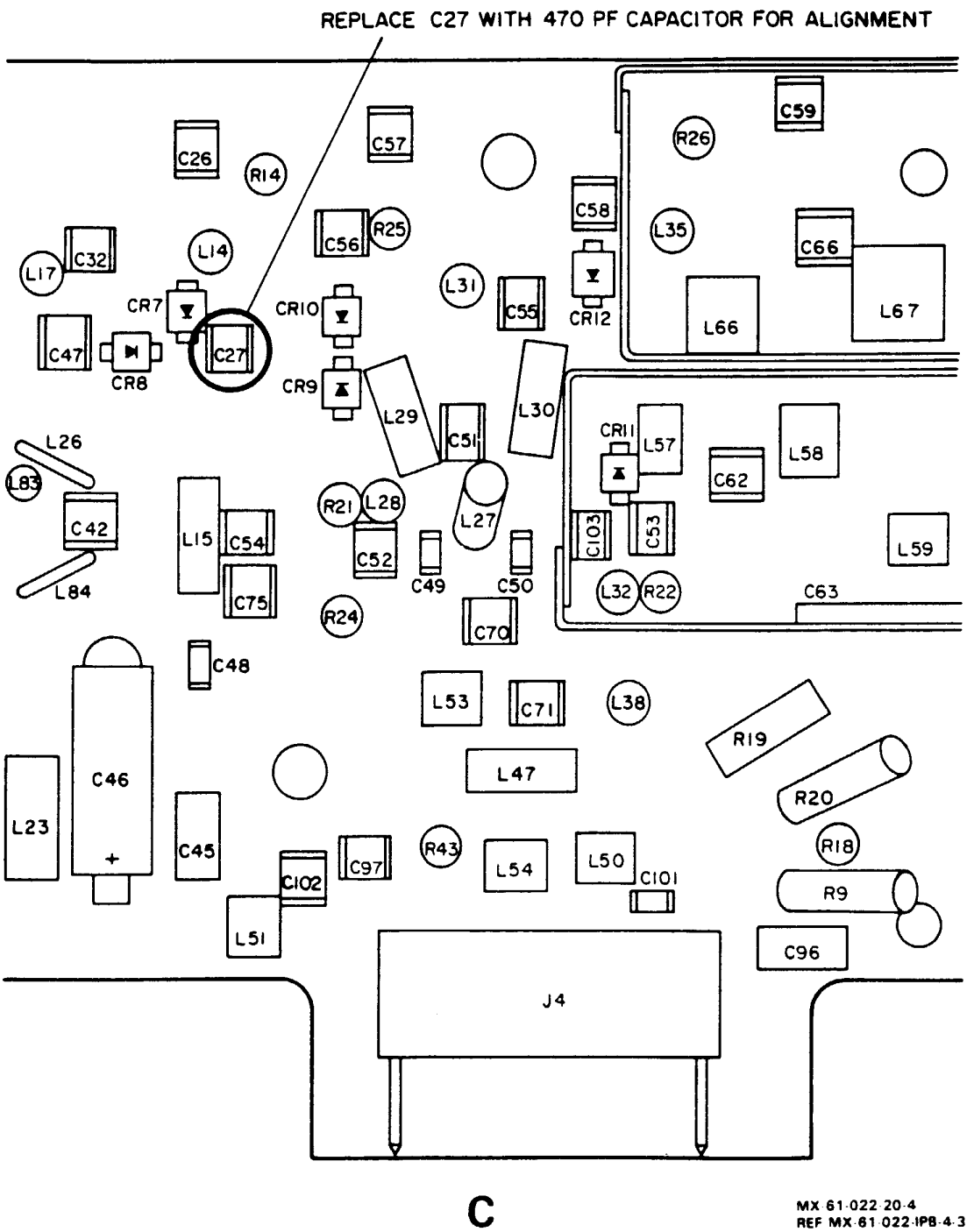


Figure 5-3. Transmitter CCA A1A1A2
Component and Test Point Location Diagram (Sheet 4 of 6)

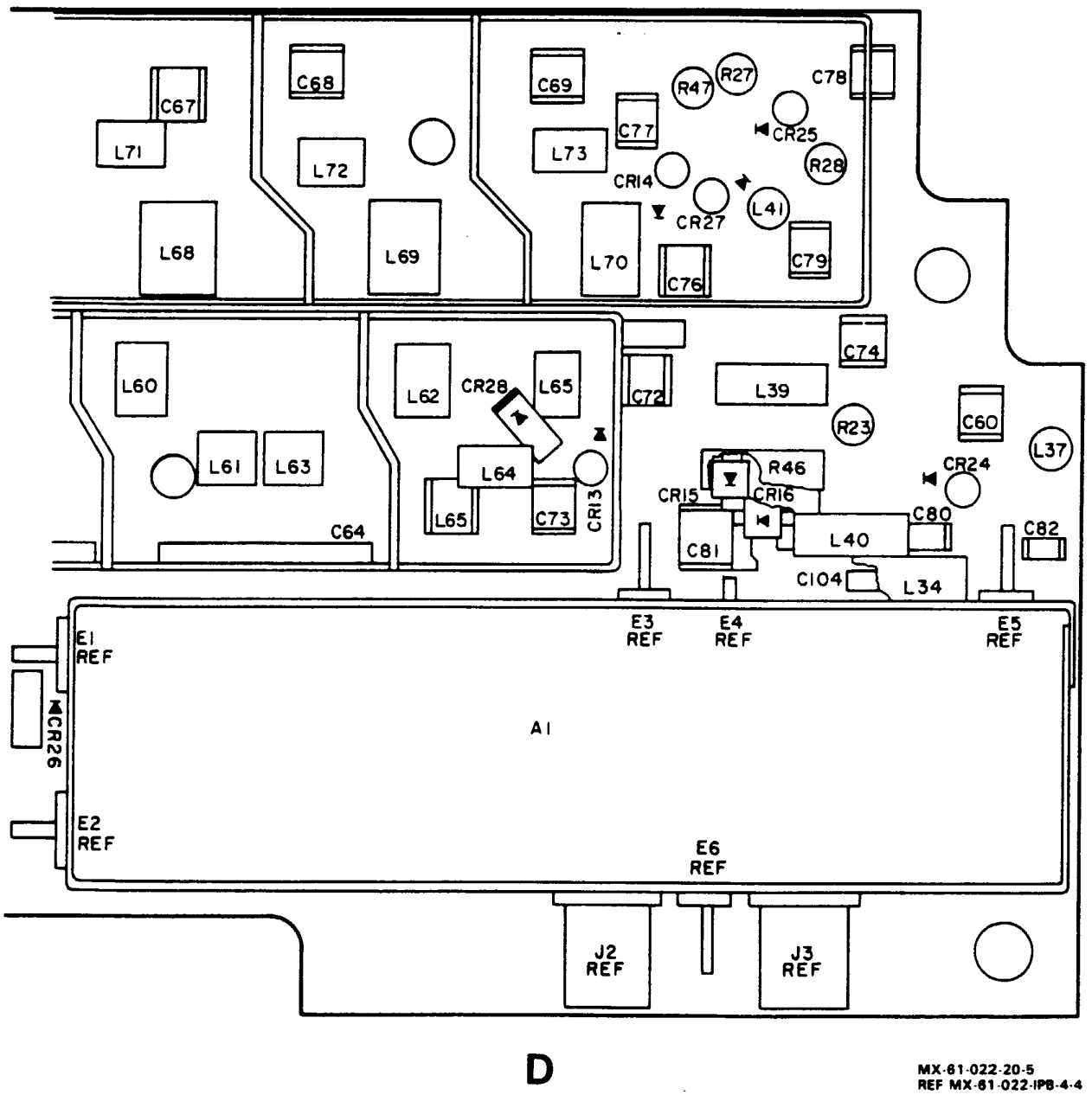


Figure 5-3. Transmitter CCA A1A1A2
Component and Test Point Location Diagram (Sheet 5 of 6)

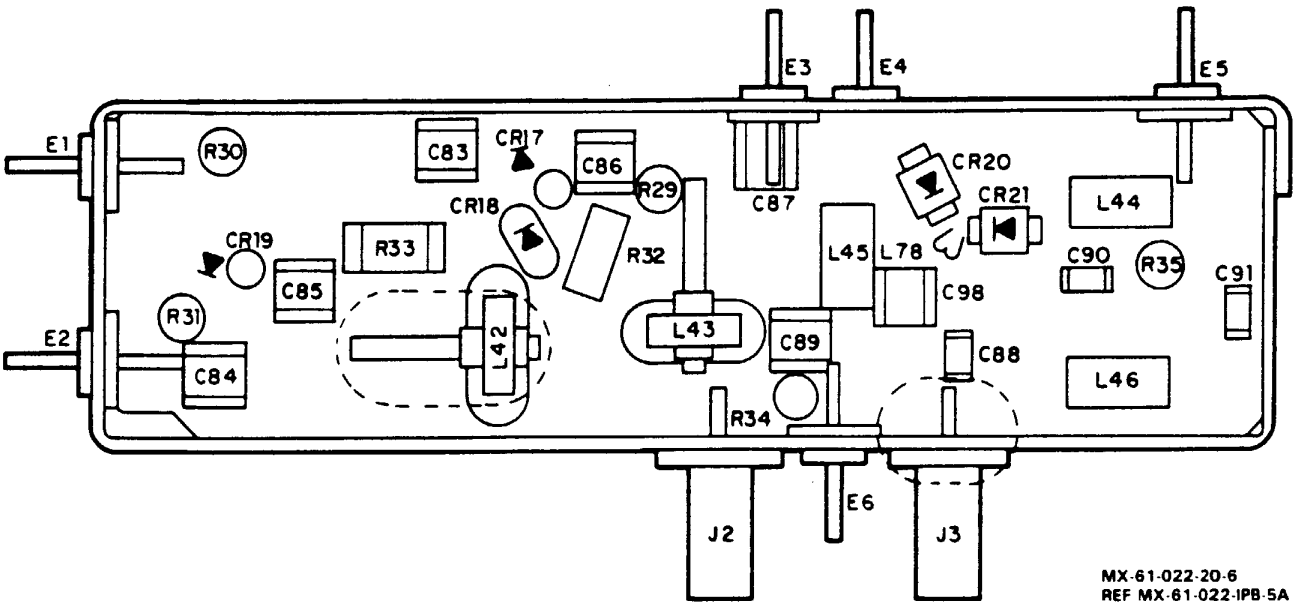


Figure 5-3. Transmitter CCA A1A1A2
Component and Test Point Location Diagram (Sheet 6 of 6)

Table 5-3. Modulator CCA A1A1A3 Latch States for Standard Test Modes

Mode	U11 pin no's								U12 pin no's							
	1	9	10	11	12	13	14	15	1	9	10	11	12	13	14	15
RECEIVE	X	L	L	L	L	L	L	L	H	L	H	X	H	H	X	X
PLAIN TRANSMIT LOW	X	H	L	H	L	H	H	L	H	L	H	X	H	L	H	H
PLAIN TRANSMIT HIGH	X	L	H	H	L	H	H	L	H	H	H	X	H	L	H (VHF)	H
CIPHER TRANSMIT	X	H	L	H	H	L	H	L	H	H	H	X	H	H	L	L
DF TONE TRANSMIT	X	H	L	H	L	H	H	L	H	H	H	X	L	L	H	L
CONFERENCE TRANSMIT	X	H	L	H	L	H	H	L	H	H	L	X	H	H	H	H
TOD TRANSMIT	X	H	L	H	H	L	H	L	L	H	H	X	H	L	H	L

Table 5-4 Modulator Test Set Preliminary Setup Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment		Performance standards
			NOTE Use known good modulator to perform the following calibration. Remove modulator cover if installed.		
1.	Connect power supplies as shown in Figure 5-4, sheet 1. Do not connect any other equipment at this time. For negative voltages, connect red terminal to (+) and black to (-). Test set inverts polarity internally. Do not use ground jumper from (-) terminal to ground on power supply.				(See figure 5-21 trouble analysis.)
2.	System presets Test set		Switch	Position	
			S1 POWER-ON	off (down)	
			S2 PTT-ON/OFF/ MOM ON	OFF	
			S3 CIPHER/PLAIN	PLAIN	
			S4 FAULT/ACTUATE	ACTUATE	
			S5 REFLECTED POWER-TEST/OFF	OFF	
			S7 NORM/CONF ON/ CONF OFF/ TOD AUD OFF/ TOD AUD ON	NORM	
			R1 REFLECTED POWER ADJUST	FULL CCW	
			R2 OVERTEMP CONTROL	FULL CCW	

Table 5-4 Modulator Test Set Preliminary Setup Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
3.	Connect known good modulator to test set.			
4.	Connect RF generator to modulator as shown in figure 5-4, sheet 1. Test Set	Mod. J1	Adjust RF generator for 250 MHz at +9 dBm +0,-1 dBm and enter 250.000 on test set keypad.	LCD displays 250.000
5.	Connect directional coupler, variable attenuator, 2 Watt amplifier, 10 dB and 3 dB pads as shown in Figure 5-4, sheet 1.			
6.	Connect distortion analyzer audio generator output to test set XMIT AUDIO-PLAIN.	Test set +J6 -J7	Input 1 kHz signal at 200 mV.	
7.			Turn on power supplies and set test set POWER switch S1 to ON.	
8.	Connect DMM to FWD PWR and power meter to directional coupler 20 dB out port as shown in Figure 5-4, sheet 1.	Test set +TP21 -TP20	Set test set S2 to ON. Adjust modulator carrier power pot R11 for 1.06 $\pm$ 0.01 Vdc. Adjust variable attenuator for -6 dBm $\pm$ 1 dB RF power out. Set S2 to OFF.	1.06 $\pm$ 0.01 Vdc

Table 5-4 Modulator Test Set Preliminary Setup Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
9.			Modulator test setup is now calibrated. This attenuation value will remain the same for all future modulator tests if the same test set, attenuator, and 2 watt amplifier is used.	
10.	Disconnect distortion analyzer audio out from test set J6.			
11.	Remove known good modulator from test setup and install unit to be tested or aligned.			
12.	Leave all other connections as is, and proceed to performance test or alignment procedures as applicable.			

Table 5-5. Modulator CCA A1A1A3 Performance Test Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			NOTE The modulator test set preliminary setup procedure in table 5-4 must be done before starting the performance test procedure.	
1.	Connect power supplies as shown in Figure 5-4, sheet 2. Do not connect any other equipment at this time. For negative voltages, connect red terminal to (+) and black to (-). Test set inverts polarity internally Do not use ground jumper from (-) terminal to ground on power supply.			
2.	System presets Test set		Switch — Position S1 POWER-ON — off (down) S2 PTT-ON/OFF/MOM ON — OFF S3 CIPHER/PLAIN — PLAIN S4 FAULT/ACTUATE — ACTUATE S5 REFLECTED POWER-TEST/OFF — OFF S7 NORM/CONF ON/CONF OFF/TOD AUD OFF/TOD AUD ON — NORM R1 REFLECTED POWER-ADJUST — FULL CCW R2 OVERTEMP CONTROL — FULL CCW	

Table 5-5. Modulator CCA A1A1A3 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
3.	Connect modulator to test set as shown in figure 5-4, sheet 1.			
4.			Turn on power supplies and set test set POWER switch S1 to ON.	
			Power Reference Setting	
5.	Test set		Set test set CIPHER/PLAIN switch S3 to CIPHER.	LCD displays; PT not lit.
			Set test set CIPHER/PLAIN switch S3 to PLAIN.	PT lit.
6.	Connect RF signal generator to UUT.	UUT J1	Set RF input to 250.000 MHz at +9 dBm, +0 -1 dBm.	-6 dBm, +0 -1 dB
7.	Connect power meter directly to UUT J2 as in Figure 5-4, sheet 2.	UUT J2	Set test set S2 to PTT-ON and adjust UUT R11.	
8.			Set test set S2 to PTT-OFF.	
9.			Maintain this power level throughout this procedure.	

Table 5-6. Modulator CCA A1A1A3 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			Audio Circuits Sidetone Audio	
			NOTE Power level established in step 16 must be maintained for the following step.	
42.	Distortion analyzer audio out.	Test set +J6 -J7	Operate in Plain transmit high mode with 1 kHz 2 mV signal applied to XMIT AUDIO. Value of R211 controls sidetone level.	Sidetone level of 0.8 ± 0.15 Vrms.
			Audio Circuits LPA Transmit Audio	
43.	Distortion analyzer	Test set +J6 -J7	Operate in Plain transmit high mode with 1 kHz 2 mV signal applied to XMIT AUDIO. Value of R142 controls LPA audio level.	Sidetone level of 0.8 ± 0.1 Vrms.
44.	End of test. Deenergize and remove test set and test equipment from UUT.			

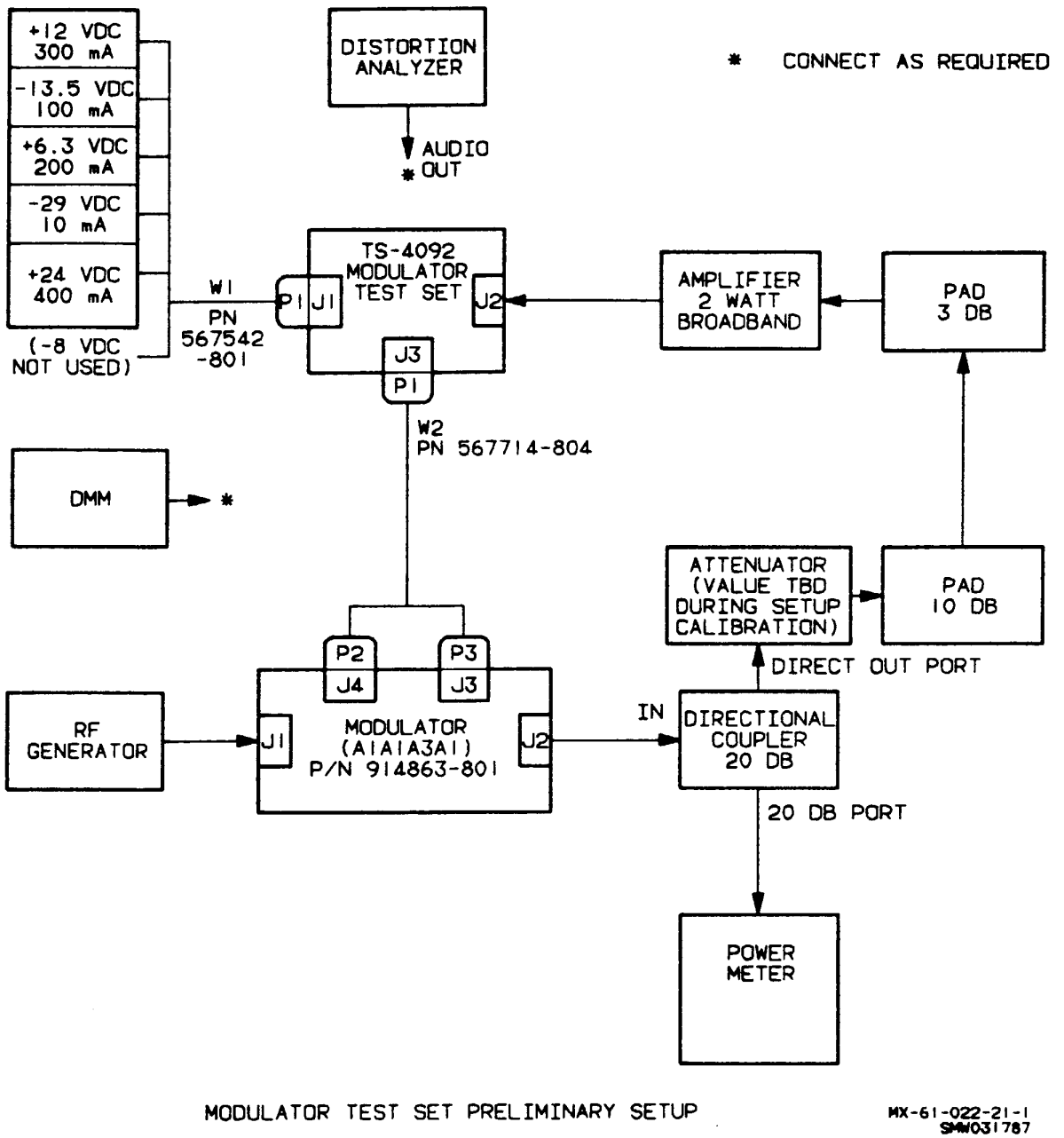


Figure 5-4. Modulator Assembly A1A1A3 Performance Test Connection Diagram (Sheet 1 of 7)

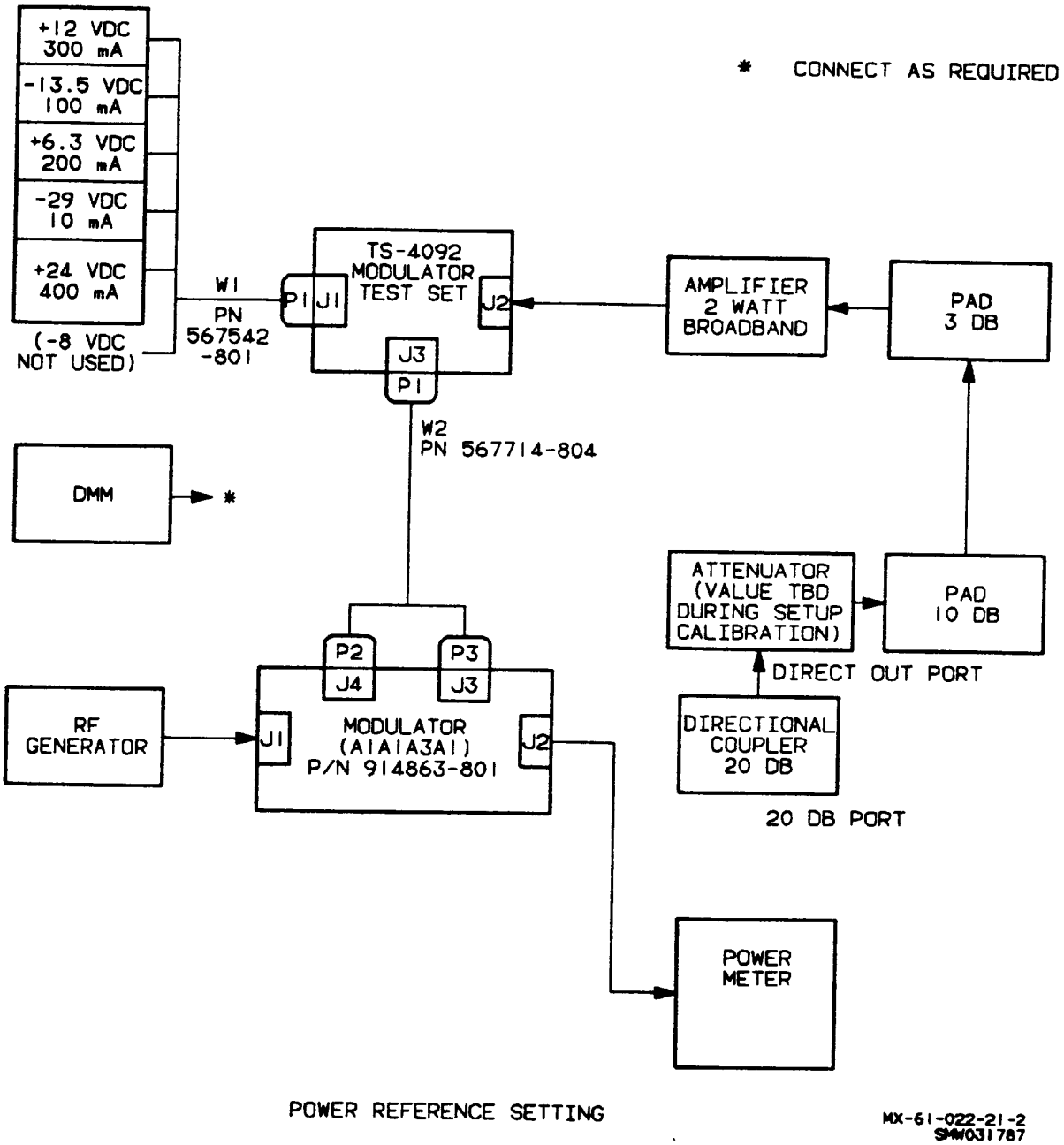


Figure 5-4. Modulator Assembly A1A1A3 Performance Test Connection Diagram (Sheet 2 of 7)

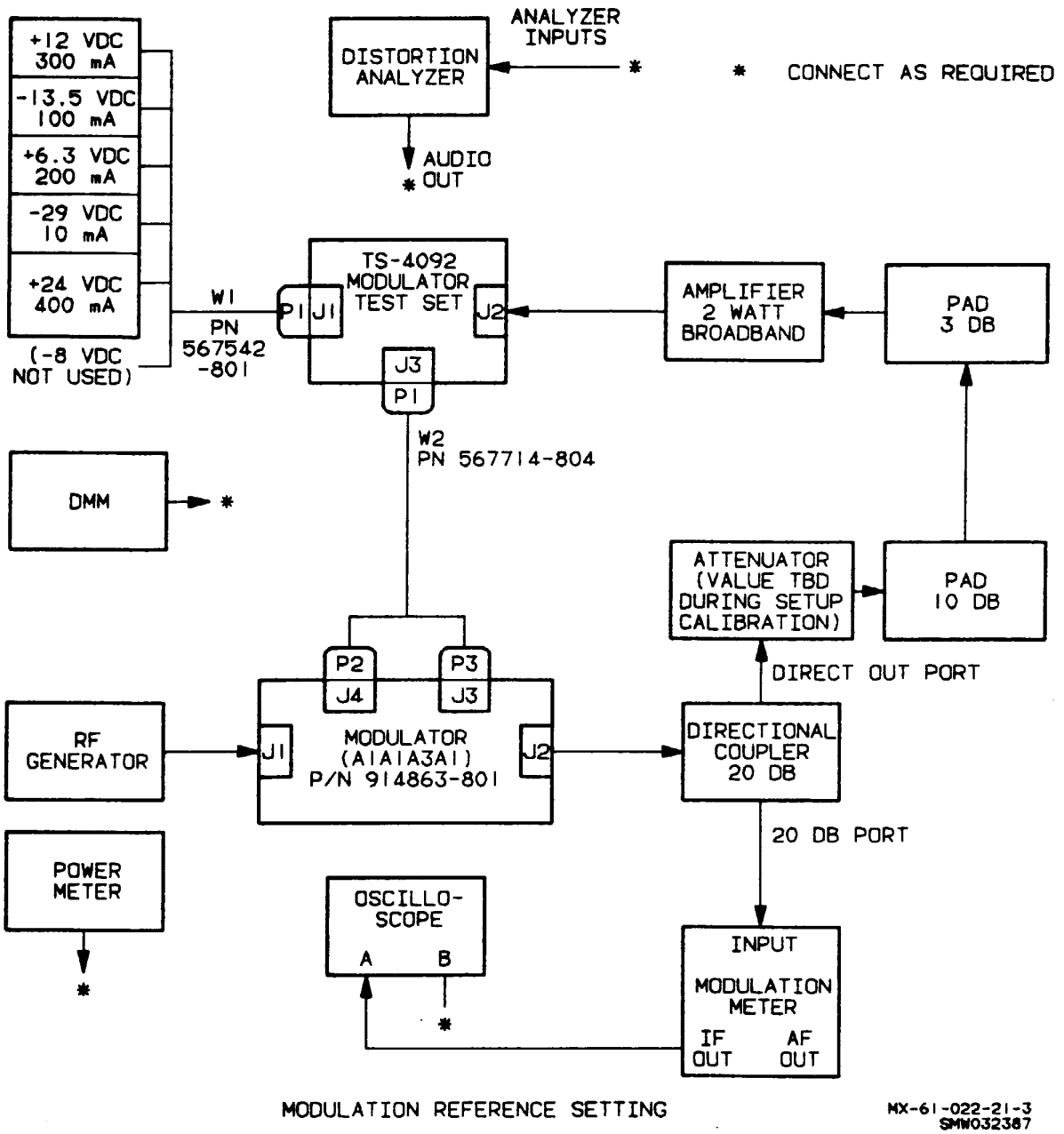


Figure 5-4. Modulator Assembly A1A1A3 Performance Test Connection Diagram (Sheet 3 of 7)

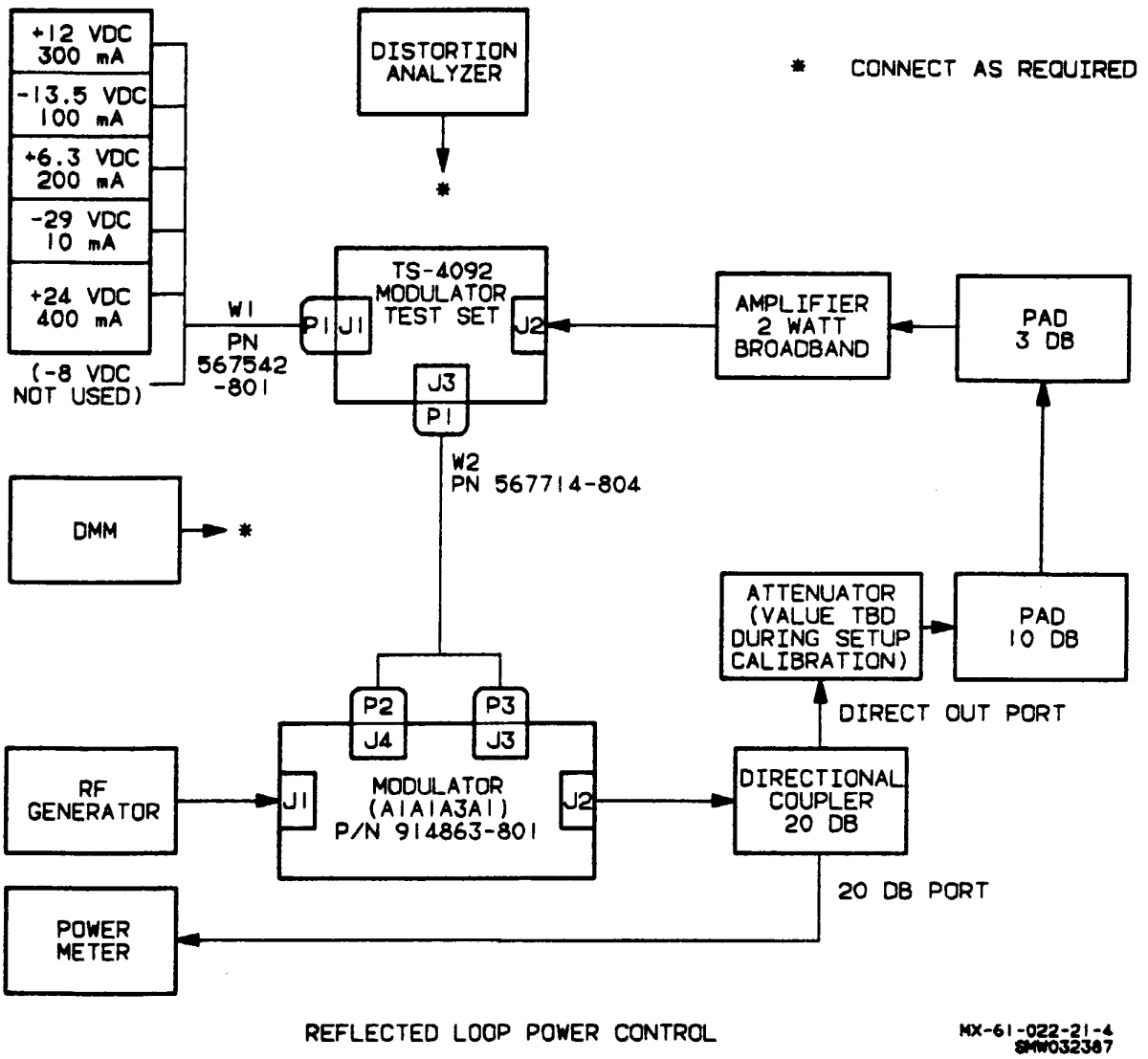


Figure 5-4. Modulator Assembly A1A1A3 Performance Test Connection Diagram (Sheet 4 of 7)

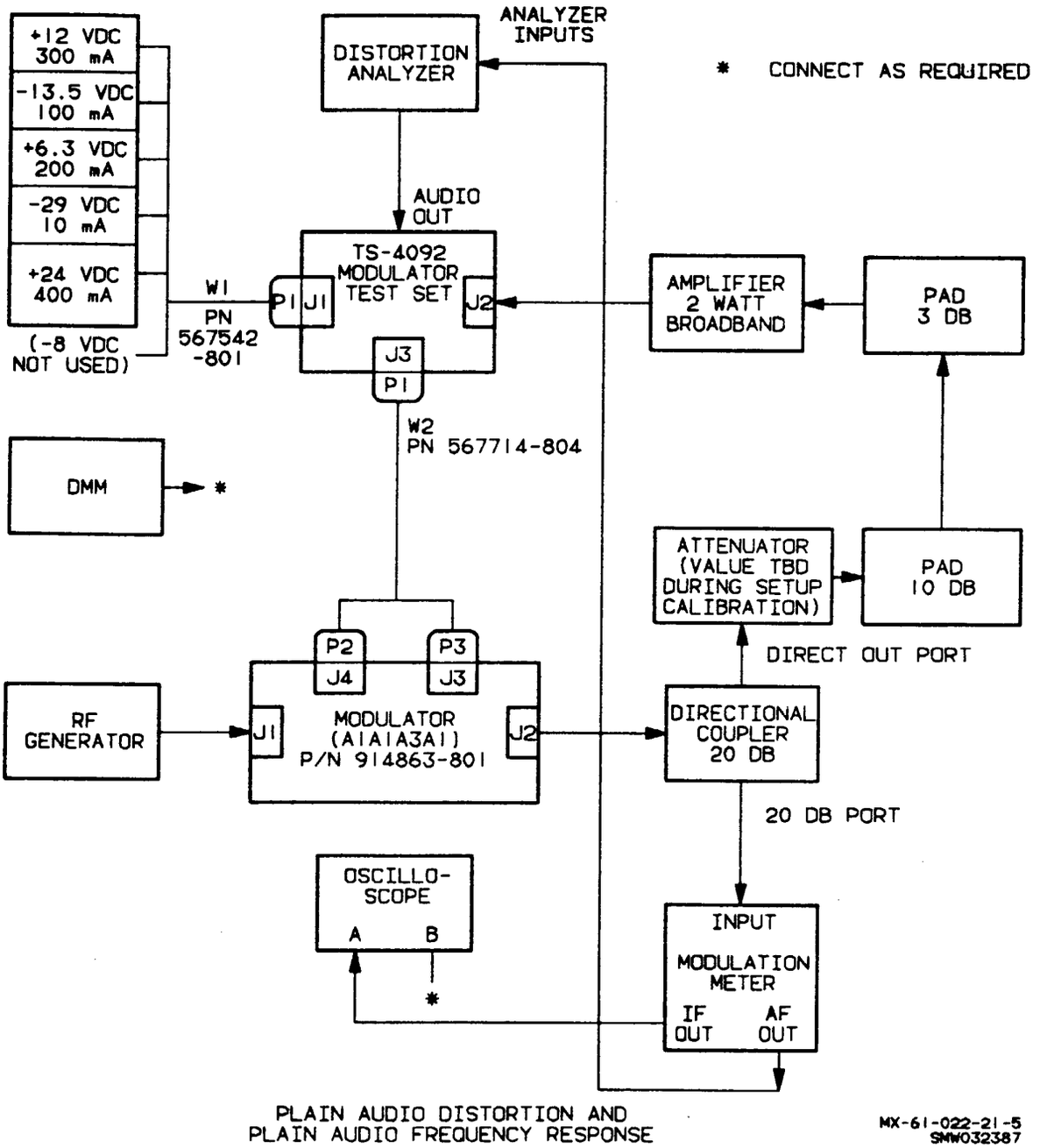


Figure 5-4. Modulator Assembly A1A1A3 Performance Test Connection Diagram (Sheet 5 of 7)

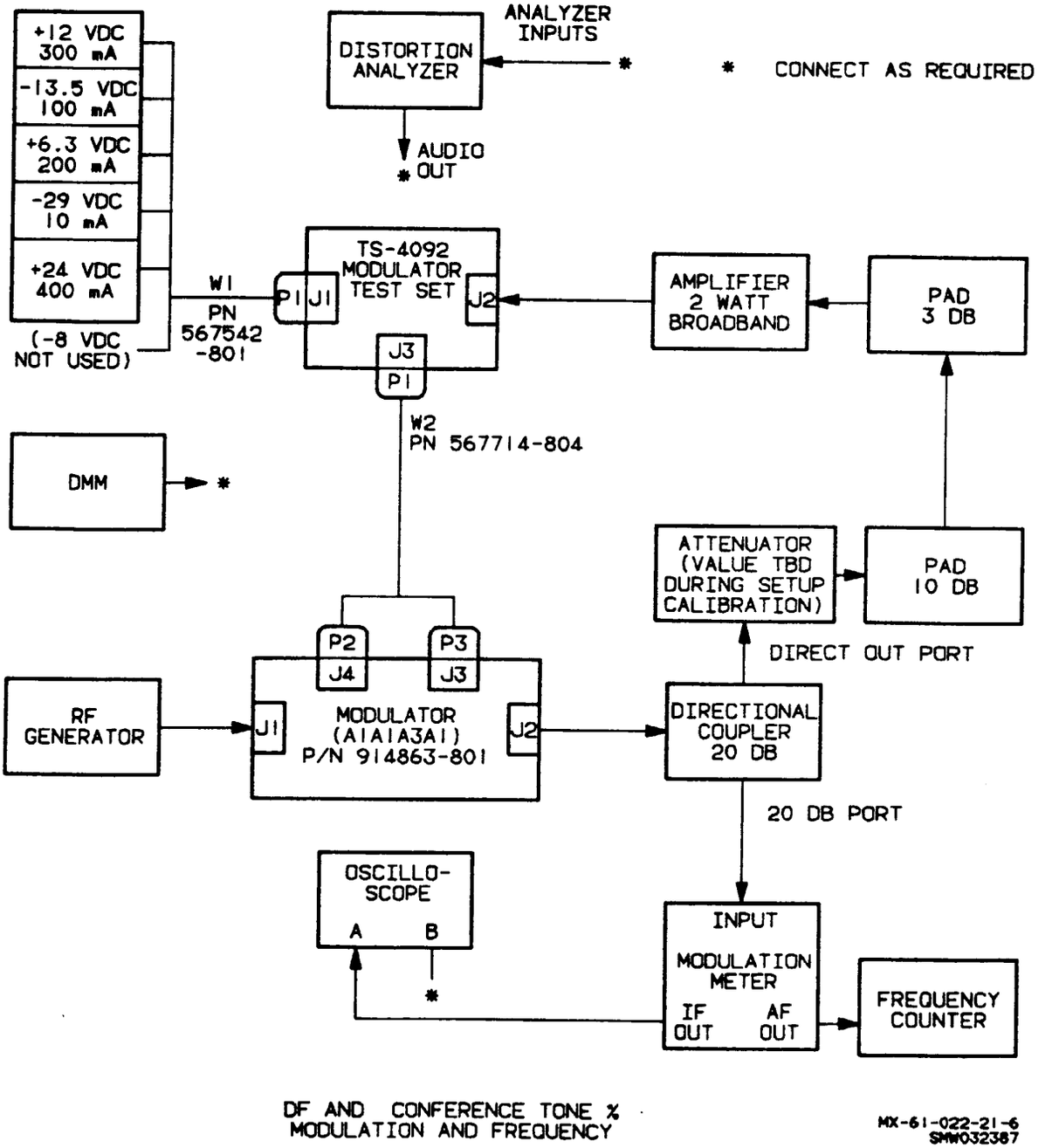


Figure 5-4. Modulator Assembly A1A1A3 Performance Test Connection Diagram (Sheet 6 of 7)

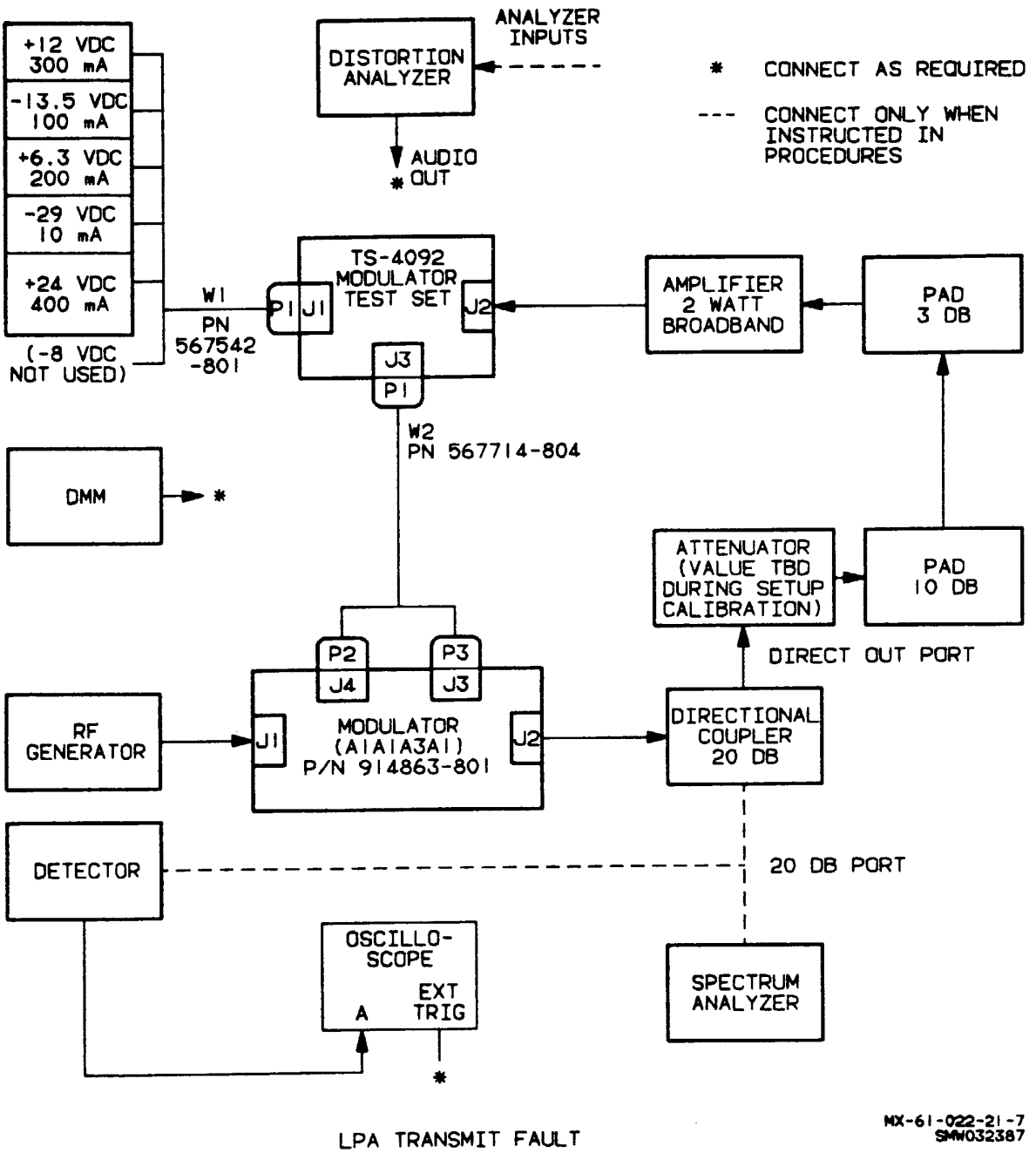


Figure 5-4. Modulator Assembly A1A1A3 Performance Test Connection Diagram (Sheet 7 of 7)

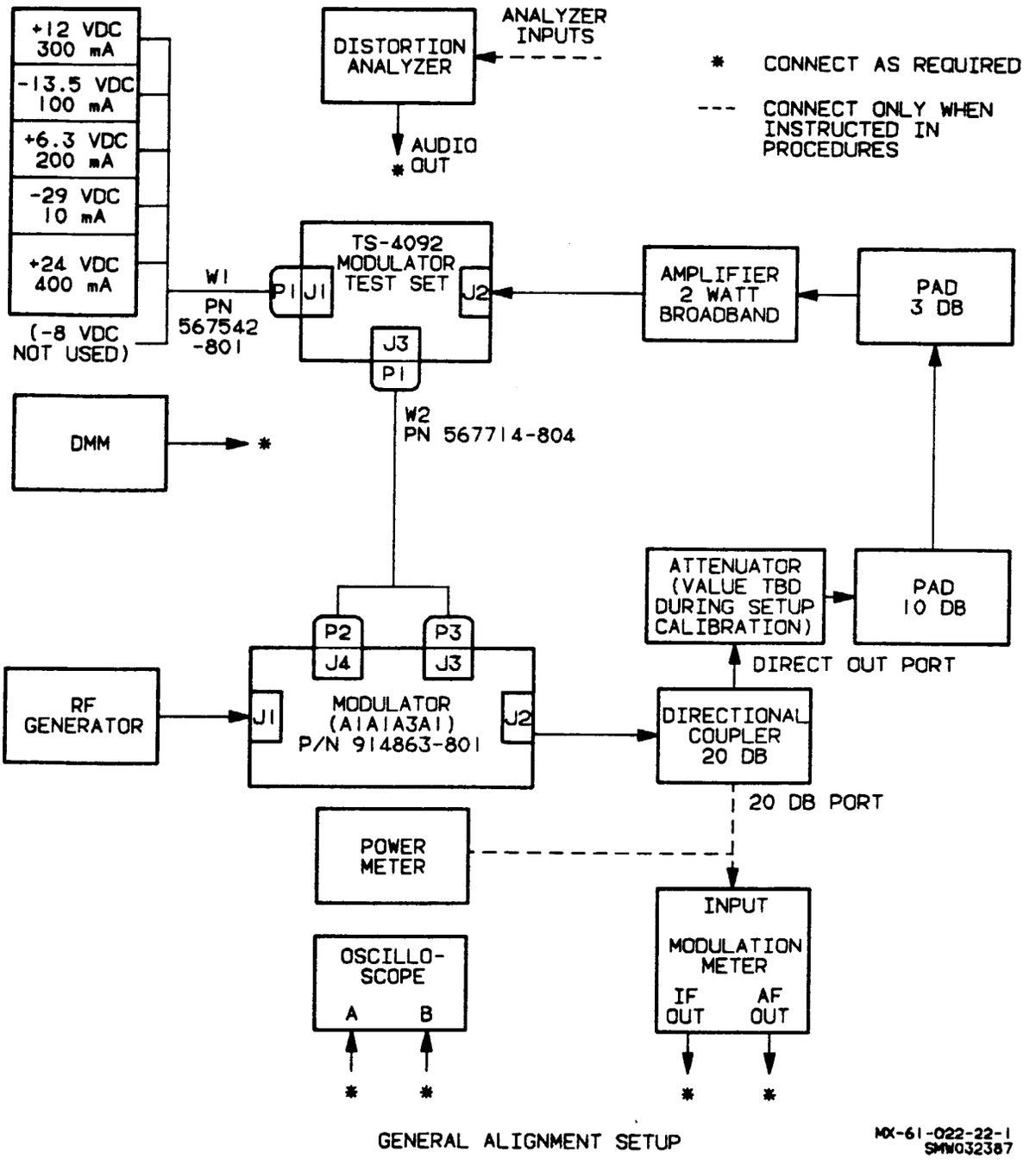


Figure 5-5. Modulator Assembly A1A1A3 Alignment Connection Diagram (Sheet 1 of 2)

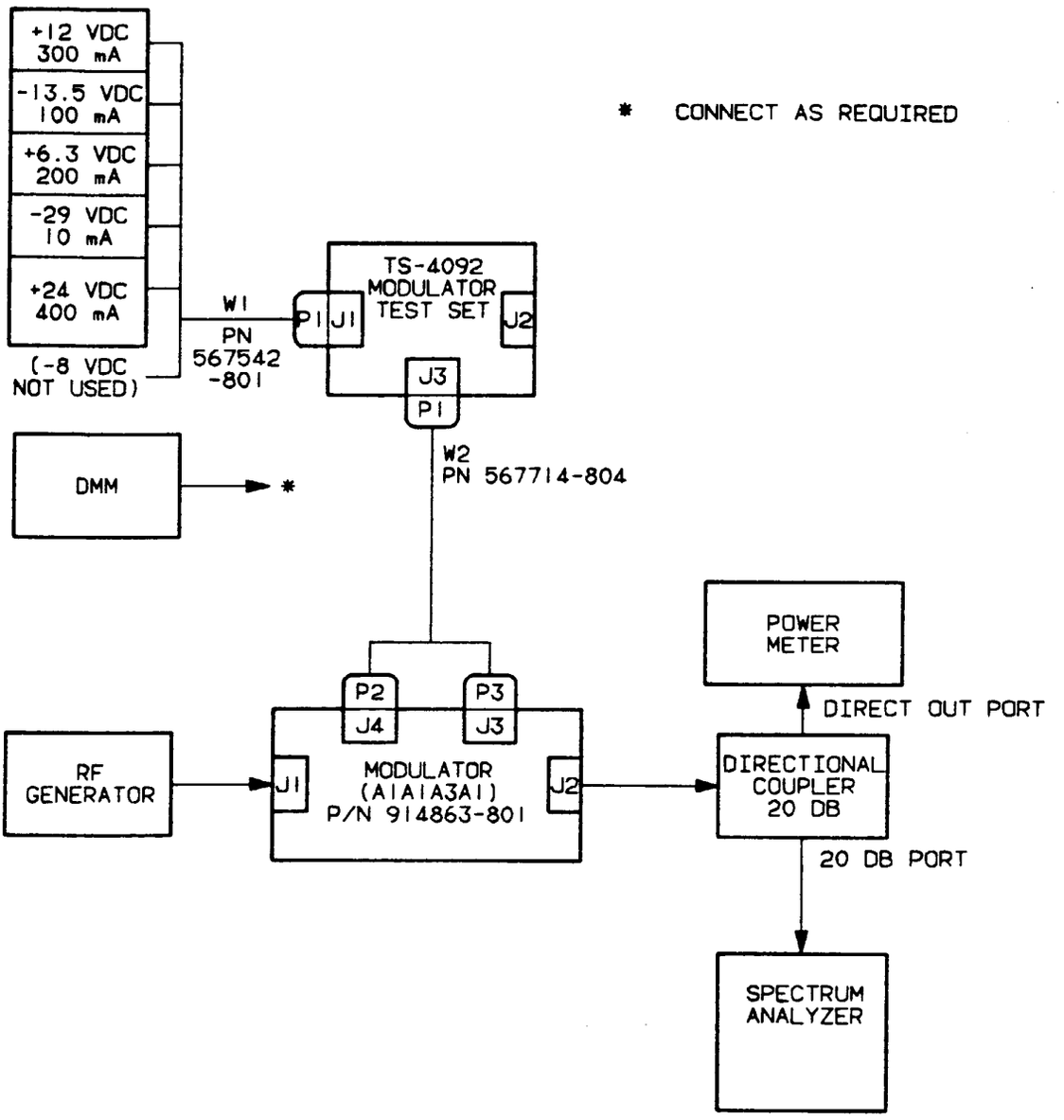
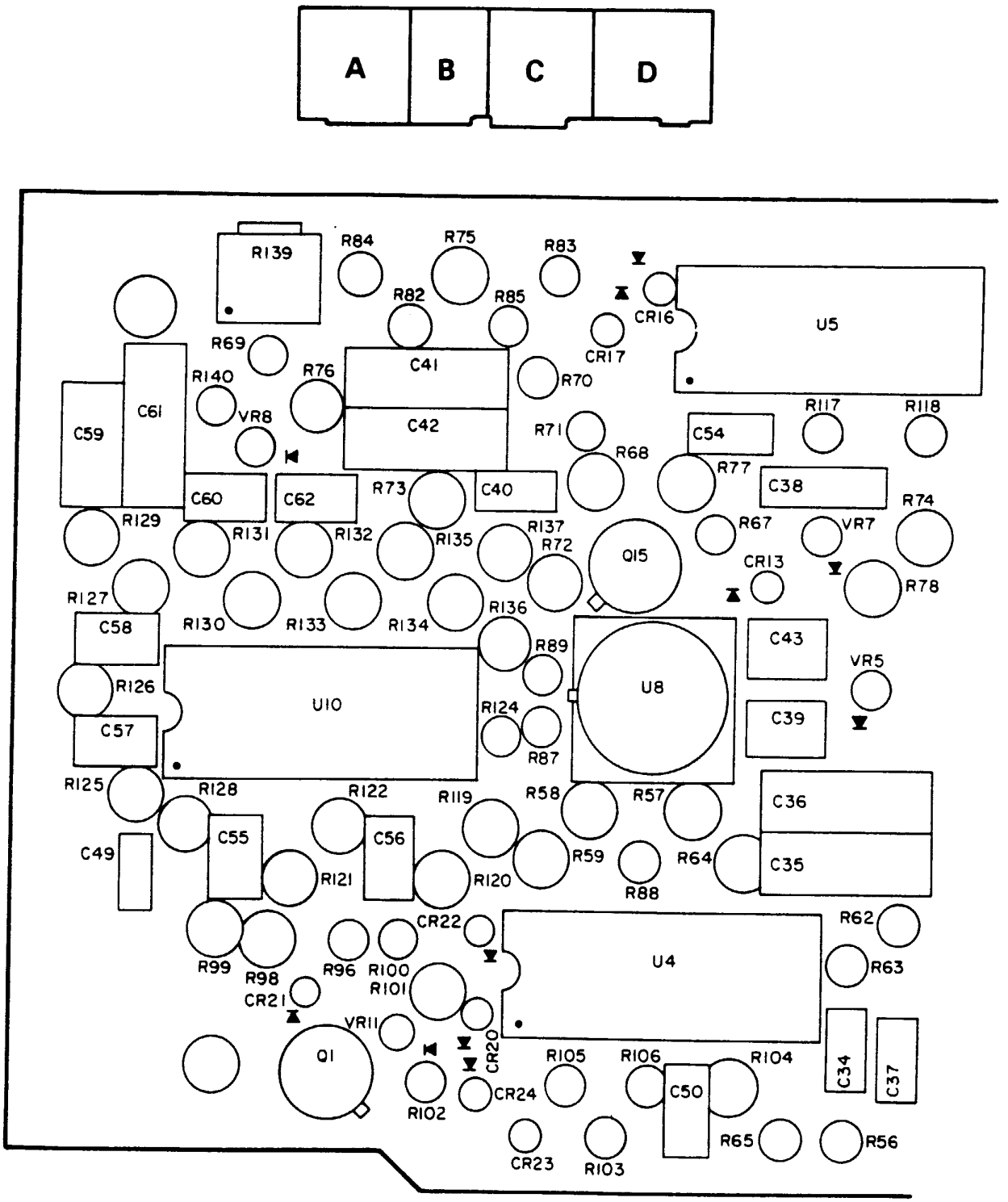


Figure 5-5. Modulator Assembly A1A1A3 Alignment Connection Diagram (Sheet 2 of 2)



REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX WITH A1A1A3A1.

A

MX-61-022-23-1
REF MX-61 022-IPB-13-1

Figure 5-6. Modulator Assembly A1A1A3
Component and Test Point Location Diagram (Sheet 1 of 4)

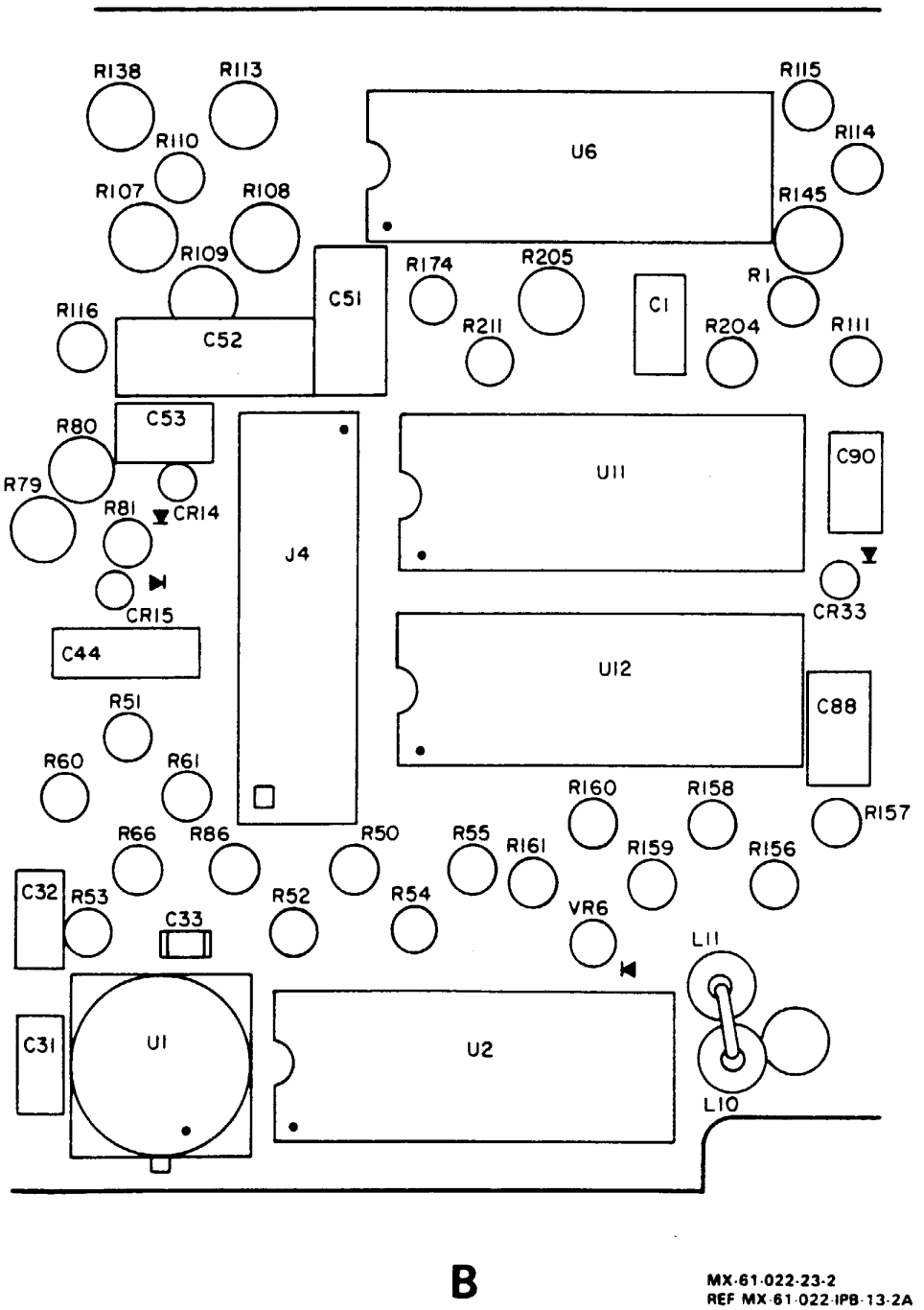


Figure 5-6. Modulator Assembly A1A1A3
Component and Test Point Location Diagram (Sheet 2 of 4)

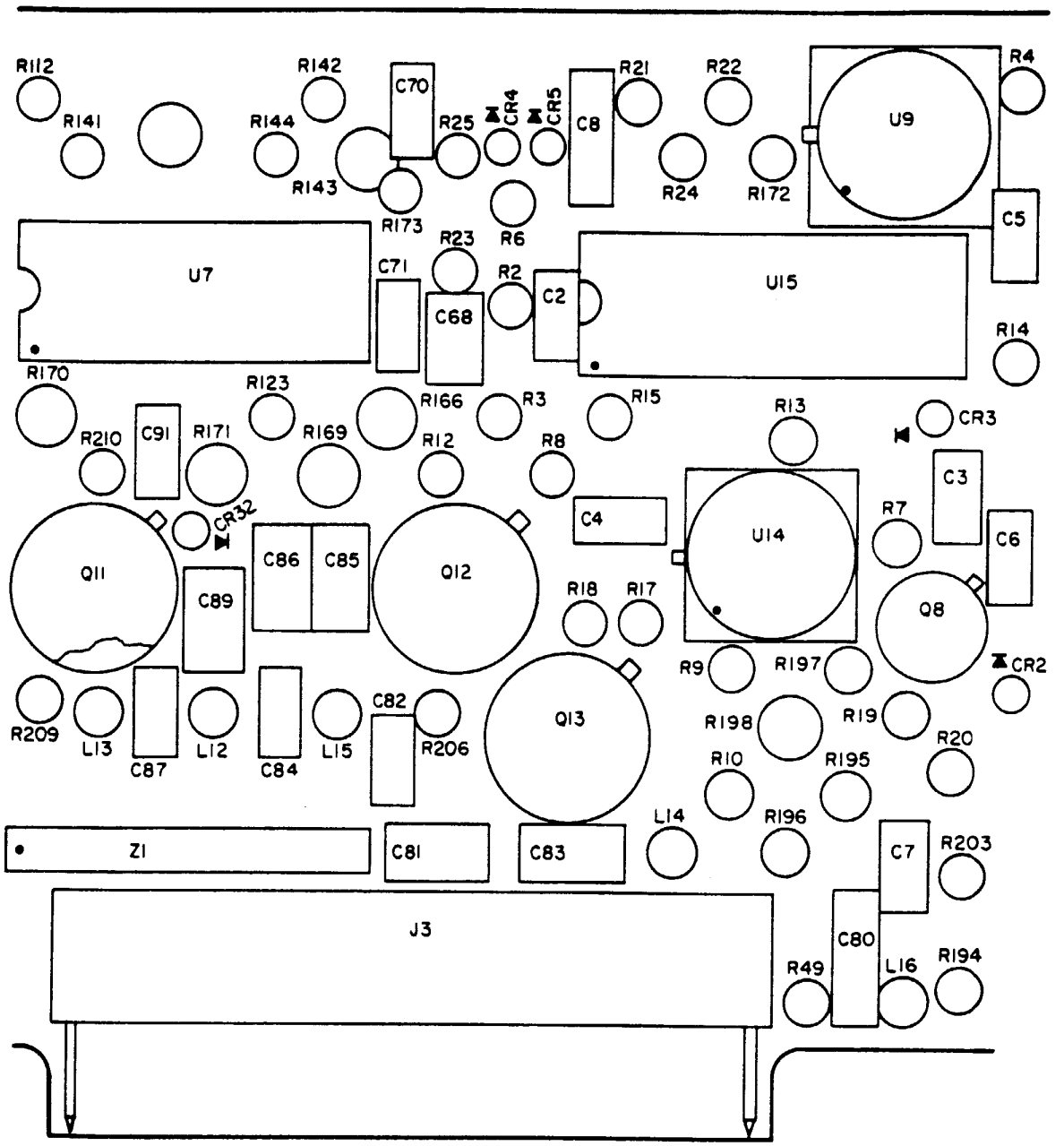


Figure 5-6. Modulator Assembly A1A1A3
Component and Test Point Location Diagram (Sheet 3 of 4)

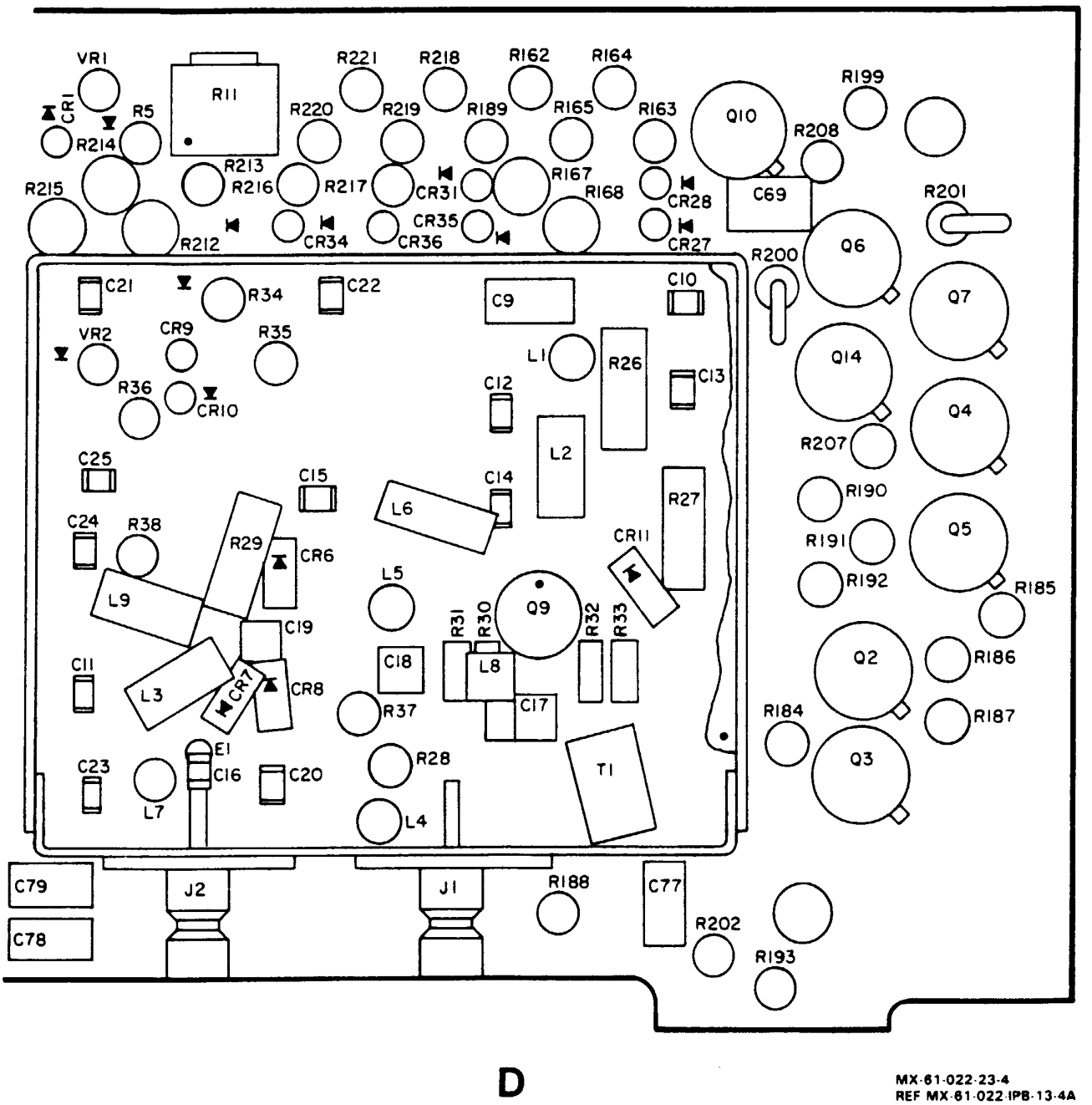


Figure 5-6. Modulator Assembly A1A1A3
Component and Test Point Location Diagram (Sheet 4 of 4)

Table 5-7. Main Receiver CCA A1A1A4 Linear Tune Volts

Sig gen A input to receiver J1	Tune volts (Vdc)	Sig gen B inject to receiver J2
UHF Frequency (MHz)		J2 Injection Frequency (+7 dBm) (MHz)
225.000	1.719	255.100
230.000	1.875	260.100
270.000	3.125	300.100
312.500	4.453	282.400
360.000	5.937	329.900
399.975	7.188	369.875
VHF Frequency (MHz)		
116.000	2.468	146.100
125.000	3.031	155.100
130.000	3.343	160.100
134.000	3.593	164.100
149.975	4.591	180.075

Table 5-8. Main Receiver CCA A1A1A4 Mode Select Switch Settings

Mode	Switch setting					Indicators lighted
To select mode, set the following switches in the order specified.						
MODE 1	S2	S3	S4	S5	S6	
	1	0	0	1	press	UHF ON
	0	0	0	0	press	VHF OFF
	0	1	1	1	press	UHF BAND
	0	1	0	1	press	SQUELCH ENABLE
	1	0	1	0	press	NB IF
	1	1	0	0	press	AM ON
	0	0	1	1	press	FM OFF
MODE 2	S2	S3	S4	S5	S6	
	1	0	0	0	press	UHF OFF
	0	0	0	1	press	VHF ON
	0	1	1	0	press	VHF BAND
	0	1	0	1	press	SQUELCH ENABLE
	1	0	1	0	press	NB IF
	1	1	0	0	press	AM ON
	0	0	1	1	press	FM OFF
MODE 3	S2	S3	S4	S5	S6	
	1	0	0	1	press	UHF ON
	0	0	0	0	press	VHF OFF
	0	1	1	1	press	UHF BAND
	0	1	0	1	press	SQUELCH ENABLE
	1	0	1	1	press	WB IF
	1	1	0	0	press	AM ON
	0	0	1	1	press	FM OFF
MODE 4	S2	S3	S4	S5	S6	
	1	0	0	1	press	UHF ON
	0	0	0	0	press	VHF OFF
	0	1	1	1	press	UHF BAND
	0	1	0	0	press	SQUELCH DISABLE
	1	0	1	1	press	WB IF
	1	1	0	0	press	AM ON
	0	0	1	1	press	FM OFF
MODE 5	S2	S3	S4	S5	S6	
	1	0	0	1	press	UHF ON
	0	0	0	0	press	VHF OFF
	0	1	1	1	press	UHF BAND
	0	1	0	0	press	SQUELCH DISABLE
	1	0	1	0	press	NB IF
	1	1	0	0	press	AM ON
	0	0	1	1	press	FM OFF

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			NOTE All RF input signals referred to are open circuit levels. (6 dB pad at receiver input.)	
			Test Presets	
1.			Preset test set controls as follows:	(See figure 5-22 for trouble analysis.)
			Control — Position	
			S1 — off (down position)	
			STATUS INPUTS section:	
			S2 RT ADDR 0 — 0 S3 RT ADDR 1 — 0 S4 RT ADDR 2 — 0 S5 RT DB — 0	
			MAIN RECEIVER section:	
			R1 SQUELCH — max ccw R2 TUNE VOLTAGE — max ccw	
			GUARD RECEIVER section:	
			R3 VOL — max ccw R4 SPEAKER VOLUME — max ccw S8 SQUELCH-DISABLE/ENABLE — ENABLE S9 GUARD STB/ACT — STB S7 MODULE SELECT -MAIN/GUARD — MAIN	

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
2.	Connect equipment as shown in fig. 5-7. For negative voltages, connect red terminal to (+) and black to (-). Test set inverts polarity internally. Do not use ground jumper from (-) terminal to ground on power supply.		Adjust input power supplies to indicated voltage and current levels. Set test set S1 to ON. Measure voltage drop across following test set test points and calculate current for each using resistance factor listed.	
		Test set Pos Neg	Resistance factor / Maximum current	
	DMM	7 13	2 Ohms / 7 mA	
		8 14	1 Ohm / 17 mA	
		9 15	2 Ohms / 5 mA	
		10 16	not used / not used	
		11 17	1 Ohm / 16 mA	
		12 18	1 Ohm / 40 mA	
			NOTE Refer to table 5-8 to setup Modes 1-5 in following steps.	
			UHF Sensitivity	
3.	Test set		STATUS INPUT section select Mode 1.	
4.	Signal generator B		Set signal generator B for output of +7dBm (500 mV) at 255.100 MHz (no modulation).	

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
5.	DMM	Test set +TP23 -TP20	Set TUNE VOLTAGE (R2) to +1.719 Vdc.	+1.719 Vdc
6.	Signal generator A	UUT J2	Set signal generator A for output of 6 µV at 225.000 MHz amplitude modulated 30% at 1000 Hz.	
7.	Distortion analyzer RMS voltmeter	Test set MAIN J7 GND J8	Establish reference level on distortion analyzer.	
8.	Distortion analyzer RMS voltmeter	Test set MAIN J7 GND J8	Remove modulation and read quiescent noise.	≥ 12 dB below reference
9.			Repeat Steps 4 thru 8 using following frequency and tune voltage settings. Sig Gen A 270.000 MHz Sig Gen B 300.100 MHz Tune voltage +3.125 Vdc	
10.			Repeat Steps 4 thru 8 using following frequency and tune voltage settings. Sig Gen A 312.500 MHz Sig Gen B 282.400 MHz Tune voltage +4.453 Vdc	
11.	Distortion analyzer RMS voltmeter	Test set MAIN J7 GND J8	Increase rf input to 1 mV and measure S + N/N	30 dB min.

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
12.			Repeat Steps 4 thru 8 using following frequency and tune voltage settings. Sig Gen A 360.000 MHz. Sig Gen B 329.900 MHz. Tune voltage +5.937 Vdc.	
13.			Repeat Steps 4 thru 8 using following frequency and tune voltage settings. Sig Gen A 399.975 MHz. Sig Gen B 369.875 MHz. Tune voltage +7.188 Vdc.	
			VHF Sensitivity	
14.		Test set	STATUS INPUT section, Select Mode 2.	
15.	Signal generator B		Set signal generator B for output of +7dBm (500 mV) at 146.100 MHz.	
16.	DMM	Test Set +TP23 -TP20	Set TUNE VOLTAGE (R2) to +2.468 Vdc as measured with DMM.	+2.468 Vdc
17.	Signal generator A		Set signal generator A for output of 6 µV at 116.000 MHz modulated 30% at 1000 Hz.	
18.	Distortion analyzer RMS voltmeter	Test set MAIN J7 GND J8	Establish reference level.	
19.			Remove modulation and read quiescent noise.	≥ 12 dB below reference

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
20.			Repeat Steps 15 thru 19 using following frequency and tune voltage settings. Sig Gen A 125.000 MHz Sig Gen B 155.100 MHz tune voltage +3.031 Vdc	
21.			Repeat Steps 15 thru 19 using following frequency and tune voltage settings. Sig Gen A 134.000 MHz Sig Gen B 164.100 MHz tune voltage +3.593 Vdc	
22.			Repeat Steps 15 thru 19 using following frequency and tune voltage settings. Sig Gen A 149.975 MHz Sig Gen B 180.070 MHz tune voltage +4.591 Vdc AGC Response	
23.		Test Set	STATUS INPUT section select Mode 1.	
24.	Signal generator B	UUT J1	Set signal generator B for output of +7 dBm (500 mV) at 282.400 MHz.	
25.	DMM	Test Set +TP23 -TP20	Set TUNE VOLTAGE (R2) to +4.453 Vdc as measured with DMM.	

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
26.	Signal generator A		Set signal generator A for output of -47 dBm (1 mV) at 312.500 MHz modulated 90% at 1000 Hz.	
27.	Distortion analyzer RMS voltmeter	Test set MAIN J7 GND J8	Establish reference level.	
28.	Signal generator A		Set signal generator A for output of -97.5 dBm (3 µV) at 312.500 MHz modulated 90% at 1000 Hz.	
29.	Distortion analyzer RMS voltmeter	Test Set MAIN J7 GND J8	Measure audio level at AUDIO OUTPUTS MAIN. CAUTION The following input is considerably above normal input levels. Use only as long as required to observe audio output measurements.	+4 dB or -3 dB with respect to reference in step 27.
30.	Signal generator A		Set signal generator A for output of 7 dBm (500 mV) at 312.500 MHz modulated 90% at 1000 Hz.	
31.	Distortion analyzer RMS voltmeter	Test Set MAIN J7 GND J8	Measure audio level at AUDIO OUTPUTS MAIN.	+5 dB or -3 dB with respect to reference in step 27.
32.	Signal generator A		Set signal generator A to +13 dBm.	

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
33.	Distortion analyzer RMS voltmeter	Test set MAIN J7 GND J8	Measure audio level at AUDIO OUTPUTS MAIN.	Audio present.
34.	Test set		STATUS INPUT section, select Mode 2.	
35.			Repeat steps 25 thru 32 using following frequency and tune voltage settings. Sig Gen A 134.000 MHz Sig Gen B 164.100 MHz tune voltage +3.593 Vdc Receive Audio Level	
36.	Test set		STATUS INPUT section select Mode 1.	
37.	Signal generator B		Set signal generator B for output of +7dBm (500 mV) at 282.400 MHz.	
38.	DMM	Test Set +TP23 -TP20	Set TUNE VOLTAGE (R2) to +4.453 Vdc as measured with DMM.	+4.453 Vdc
39.	Signal generator A		Set signal generator A for output of -47 dBm (1 mV) at 312.500 MHz modulated 30% at 1000 Hz.	
40.	Distortion analyzer RMS voltmeter	Test set J3 GND J4	Connect distortion analyzer to AUDIO OUTPUTS MODULE and measure output level.	360 mV ± 20 mV
41.	Test set		STATUS INPUT section select Mode 2.	

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
42.			Repeat Steps 37 thru 40 using following frequency and tune voltage settings. Sig Gen A 134.000 MHz Sig Gen B 164.100 MHz tune voltage +3.593 Vdc Main Audio Frequency Response And Distortion	
43.	Test set		STATUS INPUT section, select Mode 1.	
44.	Signal generator B		Set signal generator B for output of +7 dBm (500 mV) at 282.400 MHz.	
45.	DMM	Test set +TP23 -TP20	Set TUNE VOLTAGE (R2) to +4.453 Vdc as measured with DMM.	+4.453 Vdc
46.	Signal generator A RMS voltmeter	 Test set MAIN J7 GND J8	Set signal generator A for output of -47 dBm (1 mV) at 312.500 MHz modulated 50% at 1000 Hz. Measure and record audio level reference.	 Record level (dBm)
47.	Signal generator A RMS voltmeter	UUT J2 Test set MAIN J7 GND J8	Vary modulation frequency from 300 Hz to 3500 Hz.	Verify audio level does not vary more that ± 3 dB from audio reference.

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
48.	Signal generator A Distortion Analyzer	UUT J2 Test set MAIN J7 GND J8	Set signal generator A for output of -47 dBm (1 mV) at 312.500 MHz modulated 50% at 1000 Hz. Measure audio distortion at AUDIO OUTPUTS MAIN.	< 10% Audio distortion
49.	Signal generator A Distortion Analyzer	UUT J2 Test set MAIN J7 GND J8	Set modulation frequency to 300 Hz then 3500 Hz.	Verify distortion is less than 10 % for each frequency.
			Wideband Audio Level and Frequency Response	
50.	Test set		STATUS INPUT section select Mode 4.	
51.	Signal generator B		Set signal generator B for output of +7dBm (500 mV) at 282.400 MHz.	
52.	DMM	Test set +TP23 -TP20	Set TUNE VOLTAGE (R2) to +4.453 Vdc as measured with DMM.	+4.453 Vdc
53.	Signal generator		Set signal generator A for output of -47 dBm (1 mV) at 312.500 MHz modulated 50% at 1000 Hz.	
54.	Distortion analyzer	Test set CIPHER J5 GND J6	Measure and record audio reference in dB using AUDIO OUTPUTS-CIPHER.	Record level (dBm) (audio reference)

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
55.	Signal generator A RMS voltmeter	Test set CIPHER J5 GND J6	Set modulation frequency to 40 Hz and slowly increase to 10 kHz.	Verify audio level does not vary more than ± 3 dB from audio reference.
56.	Sig Gen A Distortion analyzer		Set modulation to 90%	
	RMS voltmeter	Test set CIPHER J5 GND J6	Measure audio level at AUDIO OUTPUTS-CIPHER.	1.42 Vrms min.
57.	RMS voltmeter	Test set MAIN J7 GND J8	Verify no audio output from AUDIO OUTPUTS-MAIN.	0.0 Vrms
			Narrow Band Selectivity and Passband Ripple	
58.	Test set		STATUS INPUT section select Mode 1.	
59.	Signal generator B		Set Signal Generator B for output of +7dBm (500 mV) at 282.400 MHz.	
60.	DMM	Test set +TP23 -TP20	Set TUNE VOLTAGE (R2) to +4.453 Vdc as measured with DMM.	+4.453 Vdc
61.	Signal generator A		Set signal generator A for output of -93 dBm (5.0 µV) (unmodulated) at 312.500 MHz.	
62.	DMM	Test set +TP 22 -TP 20	Measure AGC voltage at MAIN RECEIVER section AGC TP 22 on test set and record value as AGC reference voltage (AGC reference).	Record AGC reference voltage.

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
63.	Signal generator A		Set signal generator A for output of -87dBm (10 µV) at 312.489 MHz. Measure AGC voltage	
	DMM	Test set +TP 22 -TP 20		< AGC reference
64.			Repeat step 63 with a frequency setting of 312.511 MHz at signal generator A.	< AGC reference
65.	Signal generator A		Set signal generator A for output of -33 dBm (5 mV) at 312.475 MHz. Measure AGC voltage.	
	DMM	Test set +TP 22 -TP 20		> AGC reference
66.			Repeat step 65 with a frequency setting of 312.525 MHz at signal generator A.	> AGC reference
67.	Signal generator A		Set signal generator A for output of -87 dBm (10 µV) unmodulated at 312.500 MHz. Tune signal generator A to 312.508 MHz and slowly decrease generator A frequency to 312.492 MHz. Measure AGC voltage.	Record highest and lowest AGC voltages and frequencies where occurred.
	DMM	Test set +TP 22 -TP 20		Record AGC voltage.

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
68.	Signal generator A		Set signal generator A to frequencies of highest AGC voltages as recorded in step 67 Increase signal generator A output to provide lowest AGC voltages as recorded in step 67.	
	DMM Signal generator	Test set +TP 22 -TP 20		Lowest AGC levels recorded in step 67. Change in dB of generator A output level (peak to valley ratio) shall not exceed 3 dB.
			Squelch Operation	
69.	Test set		STATUS INPUT section select Mode 1.	
70.	Signal generator B		Set signal generator B for output of +7dBm (500 mV) at 282.400 MHz	
71.	DMM	Test set +TP23 -TP20	Set TUNE VOLTAGE (R2) to +4.453 Vdc as measured with DMM.	+4.453 Vdc
72.	Signal generator A		Set signal generator A for minimum output at 312.500 MHz modulated 30% at 1000 Hz and set RF output switch to OFF position.	

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			NOTE If R1 is turned too far ccw, erroneous reqdings may result in steps 74, 75 and 76. If this occurs, repeat step 73 being careful not to overshoot the point where receiver just squelches.	
73.	DMM	Test set +TP 21 -TP 20	Rotate R1 to max cw while measuring SQUELCH IND (TP 21) with DMM turn SQUELCH (R1) slowly ccw until receiver squelches.	TP21 $\leq$ +0.4 Vdc
74.	Signal generator A DMM	UUT J2 Test set +TP 21 -TP 20	Turn RF output switch to on position and slowly increase RF level until receiver squelch breaks.	RF level < -99 dBm (2.5 µV). Record this level. TP21 $\geq$ +5.0 Vdc
75.	DMM	Test set +TP 21 -TP 20	Verify SQUELCH IND reads greater than +5 Vdc with receiver unsquelched.	TP21 $\geq$ +5.0 Vdc
76.	Signal generator A DMM		Decrease RF level until receiver squelches.	Difference is 2 to 8 dBm from level in step 74.
77.	Test set		Set SQUELCH (R1) control to full ccw position.	TP21 $\leq$ +0.4 Vdc
78.	Signal generator A DMM	Test set TP21	Increase RF level and verify that receiver squelch breaks between -91 dBm and -81 dBm	-91 to -81 dBm (TP21 > 5.0 Vdc)
79.	Signal generator A		Set RF output switch to off position.	

Table 5-9. Main Receiver CCA A1A1A4 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
80.	Test set DMM		Select mode 5 on STATUS INPUTS section and verify receiver squelch breaks.	Receiver squelch breaks. (TP21 < 0.4 Vdc)
81.	Test set		Select Mode 2 at STATUS INPUT section and set SQUELCH (R1) max cw.	
82.	Signal generator B		Set signal generator B for output of +7 dBm (500 mV) at 164.100 MHz	
83.	DMM	Test set +TP23 -TP20	Set TUNE VOLTAGE (R2) to +3.593 Vdc as measured with DMM.	+3.593 Vdc
84.	Signal generator A		Set signal generator A for minimum output at 134.000 MHz modulated 30% at 1000 Hz.	
85.	Test set DMM		Turn SQUELCH (R1) control ccw until receiver squelches.	(TP21 < 0.4 Vdc)
86.	Signal generator A		Set RF OUTPUT switch ON and slowly increase RF level until receiver squelch breaks.	< -99 dBm (2.5 μV) (TP21 > 5.0 Vdc)
87.	Test set		Set SQUELCH (R1) control max ccw.	
88.	Signal generator A DMM	Test set TP 21	Slowly increase RF level until receiver squelch breaks and verify RF level.	RF level between -91 dBm and -81 dBm when receiver squelch break breaks. (TP21 < 0.4 Vdc)
89.	End of test. De-energize and remove test set and test equipment from UUT.			

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			NOTE Prior to performing alignment procedure, capacitor C37 must be lifted on the Z1-1 side and a short piece of coax soldered to C37 (see figure 5-9).	
			NOTE All RF input signals referred to are open circuit levels with 6 dB pad at receiver input.	
1.	Connect equipment as shown in figure 5-8 sheet 1.		Preset equipment controls as follows: Receiver Test Set Control — Position S1 — off (down position) S7 MODULE SELECT-MAIN/GUARD — MAIN R1 MAIN RECEIVER-SQUELCH — max ccw R2 TUNE VOLTAGE — max ccw (ten turns) R4 SPKR VOL — max ccw.	
2.			Energize all test equipment and proceed with UUT alignment.	

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
3.		Test set	Set S1 to ON. Select Mode 1 at STATUS INPUTS section (see table 5-8).	
4.	DMM	Test set + TP 23 - TP 20	Adjust TUNE VOLTAGE R2 for 1.719 Vdc as measured by DMM.	
5.	DMM	UUT TP3 and GND	Measure tune voltage.	-2.200 Vdc ± 20 mVdc measured with DMM
6.		UUT TP 1 TP 2 R100 (see figure 5-9)	If tune voltage is not within tolerance, select replacement resistor from list of selected resistors. Lift R100 lead from TP 1 junction, insert selected resistor between TP 1 and TP 2 and repeat step 5. If tune voltage at TP3 is within tolerance proceed to step 7, if all selected resistors do not yield a tune voltage within tolerance, proceed to troubleshooting UUT in tune voltage section (refer to FO-9). Selected Resistors	
7.	Network analyzer	UUT J1	Adjust analyzer for center frequency of 225.000 MHz at 0 dBm and sweep width to 20 MHZ with 20 dB attenuation on transmission/reflection test set.	
8.	Network Analyzer	UUT Z1-1 (see figure FO-9)	With HI-Z probe attached to B input of Network Analyzer, measure output gain at UUT receiver front end, 37. Adjust L3, L8, L13, L15 and L17 in UUT for maximum gain and symmetrical response as monitored on network analyzer crt display.	

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			NOTE Capacitors and Coils are marked on bottom of board all adjustments are to be made from bottom.	
9.		UUT (see FO-9)	Adjust L3 for maximum return loss dip as monitored through channel 1 at network analyzer (lower display on crt).	
10.	Network analyzer		AdjustRF output for 399.975 MHz.	
11.	Network analyzer		Place frequency marker at 400 MHz at screen center.	
12.	DMM	Test set + TP 23 - TP 20	Adjust TUNE VOLTAGE (R2) for 188 ± 0.005 Vdc as measured on DMM.	
13.	Network analyzer	UUT	Adjust C9, C28, C31, C44, and C49 for maximum gain and symmetrical response at channel 2 (upper scale on crt). Adjust C9 for maximum return loss dip at channel 1 (lower scale on crt).	
14.	Network analyzer		Adjust RF output for 225.000 MHz.	
15.	Network analyzer		Place frequency marker at 225 MHz at screen center.	
16.	DMM	Test set + TP 23 - TP 20	Adjust TUNE VOLTAGE (R2) for 1.719 Vdc as measured by DMM.	
17.			Repeat steps 8 and 9.	

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
18.			Repeat steps 10 through 13 until response tracks at both 225 MHz and 399.975 MHz.	
19.	Network analyzer		Adjust RF output for 225.000 MHz.	
20.	Network analyzer		Set up network analyzer to sweep frequency range from 225 to 399.75 MHz.	
			NOTE	
			Network analyzer is now sweeping from 225 MHz to 399.975 MHz.	
21.	Network analyzer	Test set	Adjust TUNE VOLTAGE R2 slowly clockwise while observing network analyzer display.	GAIN across band 10 dB to 20 dB
			NOTE	
			TUNE VOLTAGE R2 Adjustment rotation may be both clockwise then counterclockwise as required to observe display for limits as stated.	
			If gain is above 20 dB refer to main receiver front end troubleshooting. INPUT RETURN LOSS must be minimum of 10 dB at 225 MHz and minimum of 8 dB at 399.975 MHz.	Figure 5-23.
			If input return loss is less than limits, refer to main receiver front end trouble-shooting.	Figure 5-23.
22.	Network analyzer		Set RF output to 230.000 MHz.	

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
23.	Network analyzer		Set Network Analyzer controls as required to position top of bell curve at screen center.	
24.	DMM	Test set + TP 23 - TP 20	Adjust test set TUNE VOLTAGE R2 to voltage listed in the following chart for applicable frequency input as measured by DMM.	
25.	Network analyzer			Verify marker is maximum of 1 dB down from level at center of passband.
			NOTE Between 340 and 380 MHz marker may be down 2 dB. Above 380 MHz, marker may be down 1.5 dB.	
			NOTE If requirement of step 30 is not met, reselect R90, 92, 94, 107, 108 and 109 as necessary in warping network.	
			LINEAR TUNE VOLTS	
			UHF Frequency (MHz) / Tune Volts (Vdc) 225.000 / 1.719 230.000 / 1.875 240.000 / 2.188 250.000 / 2.500 260.000 / 2.813 270.000 / 3.125	Tolerance (dB) 1 dB 1 dB 1 dB 1 dB 1 dB 1 dB

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			LINEAR TUNE VOLTS-cont.	
			UHF Frequency (MHz) / Tune Volts (Vdc)	Tolerance (dB)
			280.000 / 3.438	1 dB
			290.000 / 3.750	1 dB
			300.000 / 4.063	1 dB
			310.000 / 4.375	1 dB
			320.000 / 4.688	1 dB
			330.000 / 5.000	1 dB
			340.000 / 5.313	2 dB
			350.000 / 5.625	2 dB
			360.000 / 5.938	2 dB
			370.000 / 6.250	2 dB
			380.000 / 6.563	2 dB
			390.000 / 6.875	1.5 dB
			400.000 / 7.188	1.5 dB
26.	Network analyzer		Increase network analyzer frequency control settings by 10 MHz and repeat steps 24 and 25. Adjust network analyzer FINE TUNING and CHANNEL 1 thumbwheels as necessary to position bell curve at display center.	
27.	Network analyzer		Repeat step 26 at 10 MHz steps to 399.975 MHz inclusive.	
			VHF Alignment	
28.	Network analyzer		Set RF output for 116.000 MHz.	
29.	Network analyzer		Set up network analyzer to sweep frequency range over 50 MHz bandwidth from 116 MHz to 150 MHz.	

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
30.	Test set		Select mode 2 at STATUS INPUTS section. (Refer to Table 5-8.)	
31.	DMM	Test set + TP23 - TP20	Adjust TUNE VOLTAGE R2 for 2.468 Vdc ± 5 mVdc as measured by DMM.	
32.	Network analyzer	UUT Z1-1	With HI-Z probe connected at B input of analyzer measure output gain at UUT C37. Adjust L5, L7, and L12 for maximum gain and symmetrical response.	
33.	Network analyzer	UUT Z1-1	Adjust L5 for maximum return loss dip.	
34.			Repeat Step 32 and 33 as required for maximum gain and symmetrical response of output, and maximum return loss dip.	
35.	Network analyzer		Adjust RF output frequency to 150.00 MHz.	
36.	Digital multimeter	Test set + TP 23 - TP 20	Adjust TUNE VOLTAGE (R2) for 4.591 Vdc ± 5 mVdc as measured on DMM.	
37.	Network analyzer		Adjust analyzer tuning until frequency marker is at screen center (approximately 150.000 MHz).	
38.	Network analyzer	UUT	Adjust C4, C23, and C30 for maximum gain figure and symmetrical response.	
39.			Adjust C4 for maximum return loss dip.	
40.			Repeat steps 38 and 39 as required for maximum readings at channel 1 (lower scale on CRT) and channel 2 (upper scale on CRT).	

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
41.			Repeat steps 29 through 33.	
42.			Repeat steps 35 through 39.	
43.			Repeat steps 41 and 42 until no further peaking results from adjustment of components.	
44.	Network analyzer		Adjust RF output for 130.000 MHz.	
45.	Network analyzer		Adjust tuning until frequency marker is at center of screen (approximately 130.000 MHz).	
46.	Digital multimeter	Test set + TP 23 - TP 20	Adjust TUNE VOLTAGE (R2) for 3.343 Vdc $\pm$ 5 mVdc as measured on DMM or until return loss dip is centered on network analyzer display marker.	
47.	Network analyzer		Measure and record input return loss dip.	Reading should be minimum 15 dB down from center line.
48.	Network analyzer	UUT	Remove connector from ANT IN (J2) and connect to coax cable soldered to 37. Measure and record output return loss dip.	$\geq$ 15 dB down from return loss dip record-record in step 47.
49.	Network analyzer		Adjust output frequency to 116.000 MHz.	
50.	Network analyzer		Set up network analyzer to sweep frequency range from 116.000 MHz to 149.975 MHz.	
51.	Network analyzer		Adjust trace until marker appears at right side graticule of screen.	

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			NOTE Network Analyzer is now sweeping from 116 MHz to 149.975 MHz.	
52.	Digital multimeter	Test set + TP 23 - TP 20	Adjust test set TUNE VOLTAGE R2 for 2.468 Vdc as measured on DMM.	
53.	Network analyzer		Slowly increase TUNE VOLTAGE R2 CW while observing trace.	Output return loss shall be minimum of 15 dB down from center line as R2 is adjusted from 116 MHz to 149.975 MHz.
			NOTE CCW and CW rotation may be required to observe display for limits listed.	
54.	Reconnect Trans/Ref1 to J2 as shown in Figure 5-8.	UUT J2		
55.	DMM	Test set	Adjust TUNE VOLTAGE R2 for 2.468 Vdc as measured on DMM.	
56.	Network analyzer	UUT Z1-1	Observe trace on analyzer as receiver test set TUNE VOLTAGE R2 is adjusted slowly clockwise.	Verify minimum of 10 dB gain above reference across band and min. of 12 dB gain above reference at 149.975 MHz.

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
57.			Repeat step 55 while observing trace for maximum input return loss dip.	Return loss dip shall be minmum 15 dB down from reference across band.
58.	Digital multimeter	Test set + TP 23 - TP 20	Adjust TUNE VOLTAGE R2 to voltage listed for each applicable frequency input as measured by DMM. **NOTE** Adjust Network Analyzer as necessary to position top of bell curve on screen center. LINEAR TUNE VOLTS VHF Frequency (MHz) — Tune Volts (Vdc) 116.000 — 2.468 120.000 — 2.718 130.000 — 3.343 140.000 — 3.968 149.975 — 4.593	Verify marker is maximum of 1 dB down from level at center of passband for each frequency.
59.			Set test set S1 OFF.	
60.	Disconnect network analyzer and test set.			
61.	Reinstall C37.			

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			I. F. Alignment	
			NOTE Prior to IF alignment procedure, C37 must be reinstalled. (prior alignment procedure instructed to remove capacitor C37).	
62.	Test set		Set S1 to ON and select Mode 1 at STATUS INPUTS section (see table 5-8).	
63.	Connect Signal generator A as shown in figure 5-7.	UUT J2	Set signal generator A to 225.000 Mhz, -87 dBm,30 % modulated at 1000 Hz.	
64.	Connect Signal general B as shown in figure 5-7.	UUT J1	Set signal generator B to 255.100 MHz, +7 dBm.	
65.	DMM	Test set TP23 TP20	Adjust TUNE VOLTAGE R2 to +1.719 Vdc (see table 5-7).	
			NOTE The following adjustment of L28 is critical.	
66.	UUT DMM	Test set TP22 TP20	Adjust C47,C58 and L28 for minimum AGC voltage.	
67.			Set test set S1 OFF.	
68.			Remove R41 and C64. Install coax at C64/R41 junction.	

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
69.	Connect network analyzer as shown in figure 5-8 sheet 2.			
70.	Test set		Select Mode 3 at STATUS INPUTS section (see tabel 5-8).	
71.	Network analyzer	UUT J1	Set network analyzer for 30.1 MHz at 0 dBM. Set sweep width for 1 MHz. Adjust C58 for maximum gain.	
72.			Perform steps 71 with Mode 1 selected (see table 5-8). Continue steps 70-72 until both crystal filters exhibit maximum gain.	
73.	Reconnect signal generator A to UUT J2.			
74.	Signal generator A.	UUT J2	Select Mode 1 (see table 5-8) at STATUS INPUTS section and set signal generator A to 225.000 MHz, -67 dBm modulated 90 % at 1000 Hz.	
75.	Reconnect Signal generator B to J1.			
76.	Signal generater B.	UUT J1 Test set TP23 TP20	Set signal generator B to 255.100 MHz. +7 dBm, and tune voltage to +1.719 Vdc.	
77.	Put oscilloscope probe on UUT U2-9	UUT U2-9	Adjust C92 to center noise spikes equidistant on both sides of baseline.	
78.	Turn off equipment and reinstall R41 and C64.			

Table 5-10. Main Receiver CCA A1A1A4 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
79.	Sig gen A		Set sig gen A to -47 dBm modulated 30 % at 1000 Hz.	
80.			Turn on test set and SELECT MODE 1. (see table 5-8).	
81.	Connect distortion analyzer to test set.	Test set J3 J4	Select value for R63 which will give 340 to 380 mV at test set J3 and J4.	340 to 380 mV
82.	Signal generator A Signal generator B DMM	Test set TP23 TP20	Set sig gen A to 312.500 MHz with minimum output. Set sig gen B to 282.400 MHz, +7 dBm and adjust tune voltage to 4.453 Vdc.	
83.		Test set	Adjust SQUELCH R1 max ccw.	
84.	DMM	Test set TP21 TP20	Select value for R123 which will allow squelch to break at RF level of -89 to -82 dBm.	TP21 >5.0 Vdc
85.	Connect network analyzer as shown in figure 5-8 sheet 3.	UUT J1	Adjust for 30.1 MHz.	
86.		Test set	Select Mode 3 at STATUS INPUTS section. (see table 5-8)	
87.	Signal generator		Inject a 30.1 MHz external marker into network analyzer.	
88.	Network analyzer	UUT C46	Adjust C46 for max return loss (highest signal) at 30.1 MHz.	
89.	End of test. Deenergize and remove test set and test equipment from UUT.			

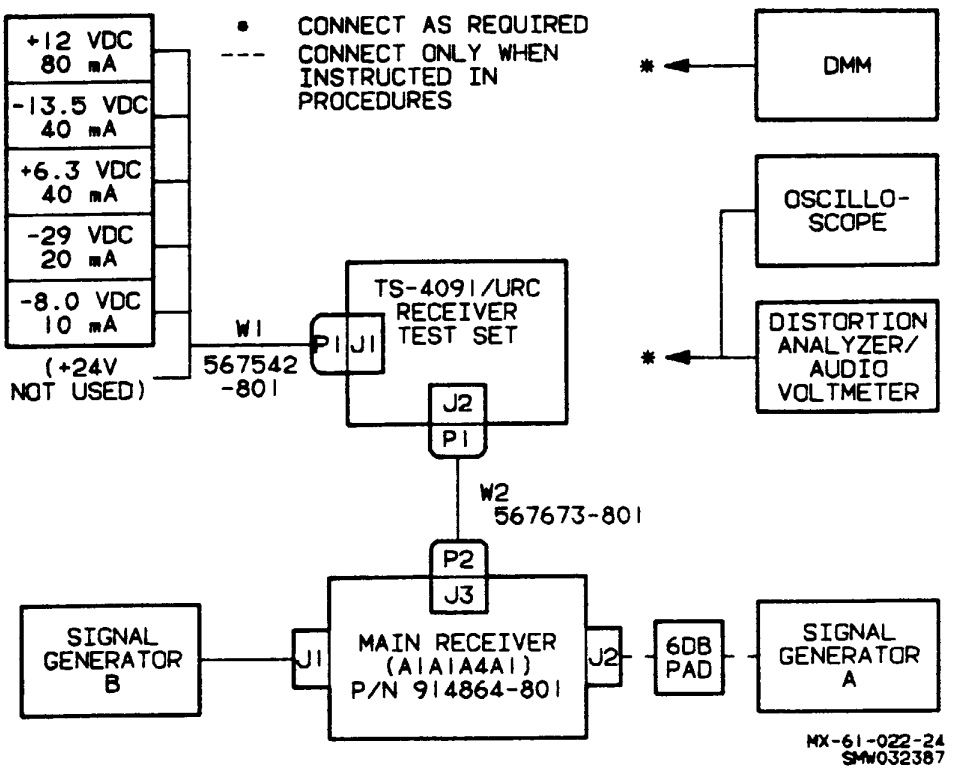


Figure 5-7. Main Receiver Assembly A1A1A4 Performance Test/Alignment Connection Diagram

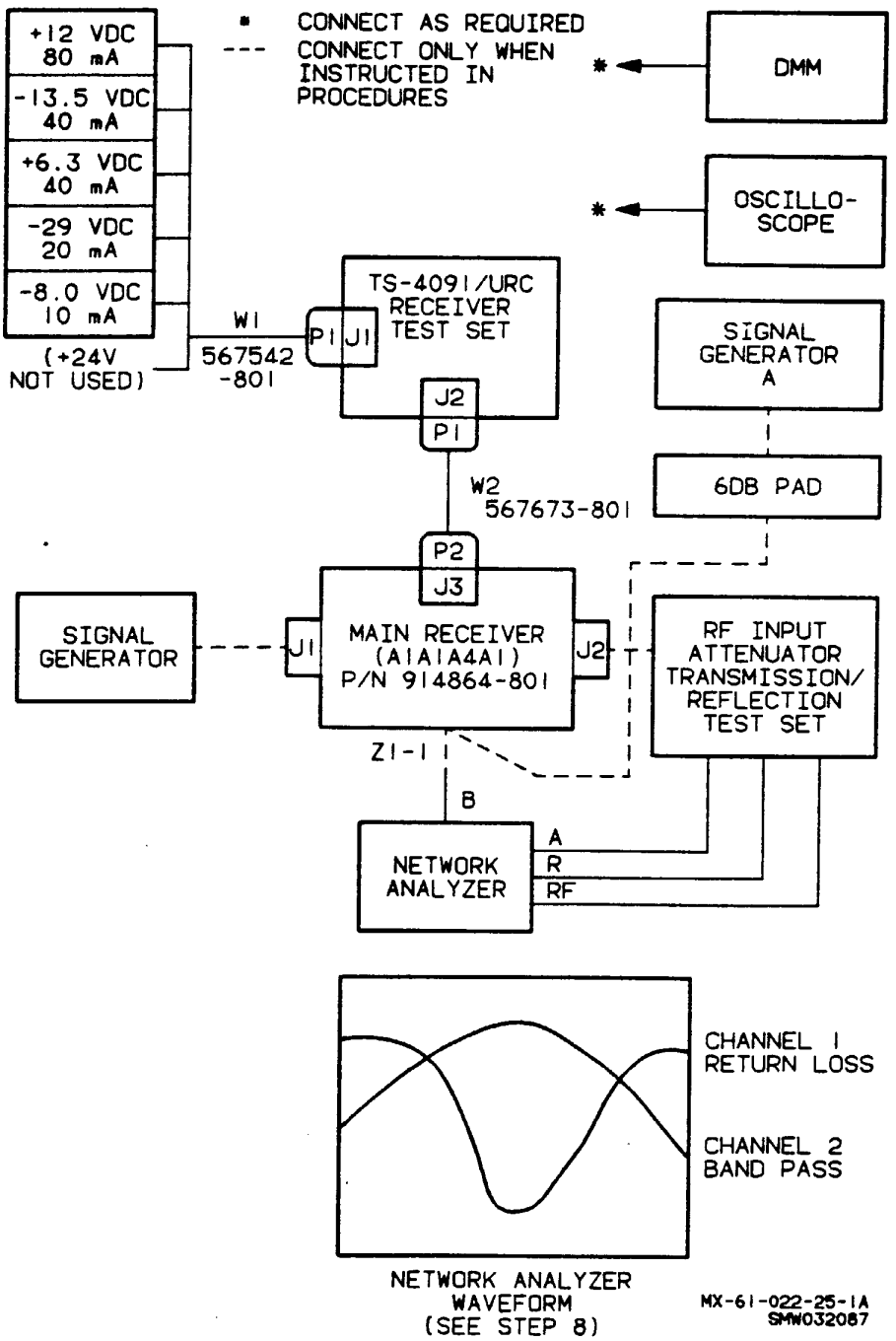


Figure 5-8. Main Receiver Assembly A1A1A4 Alignment Connection Diagram (Sheet 1 of 3)

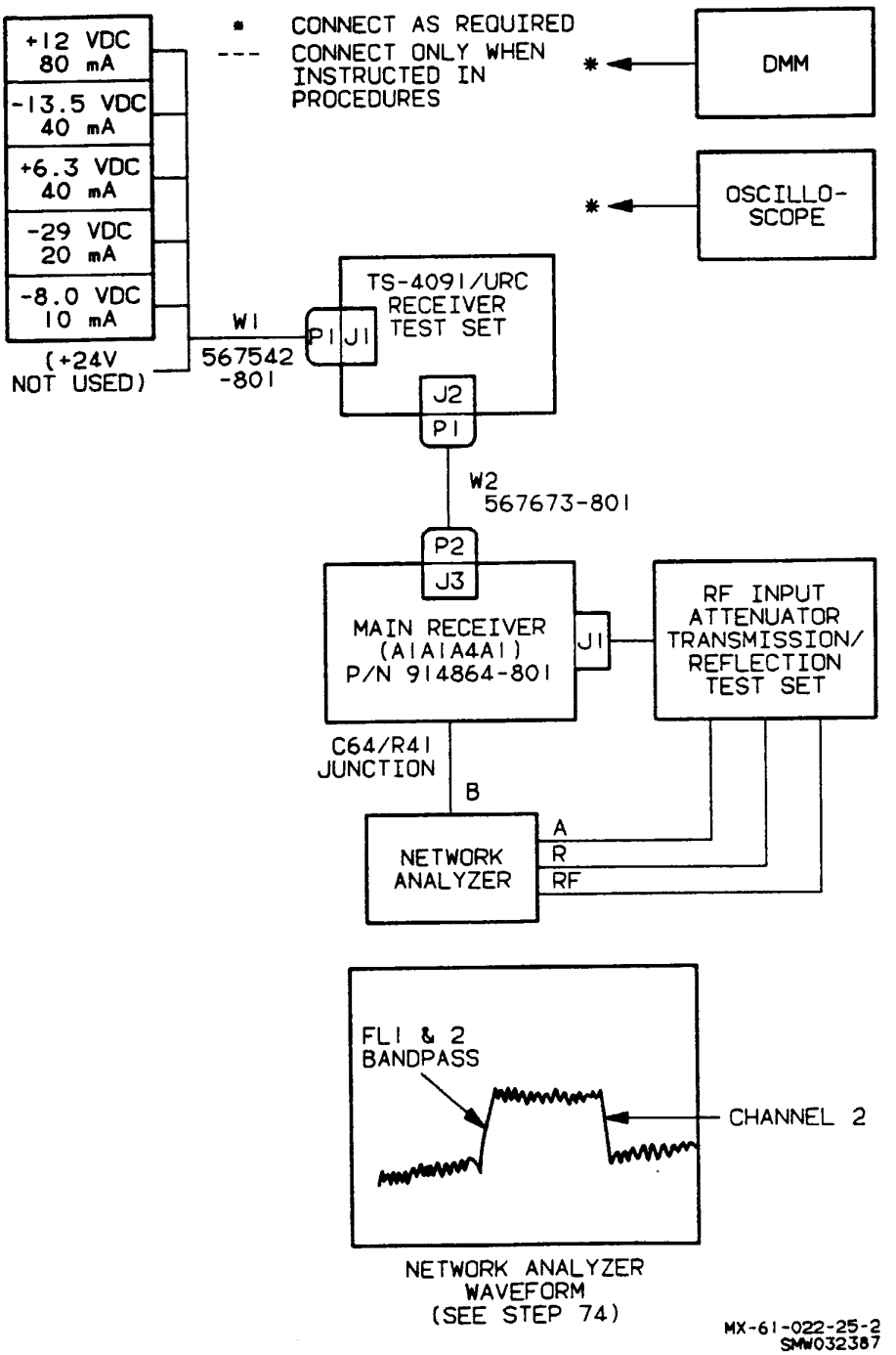


Figure 5-8. Main Receiver Assembly A1A1A4 Alignment Connection Diagram (Sheet 2 of 3)

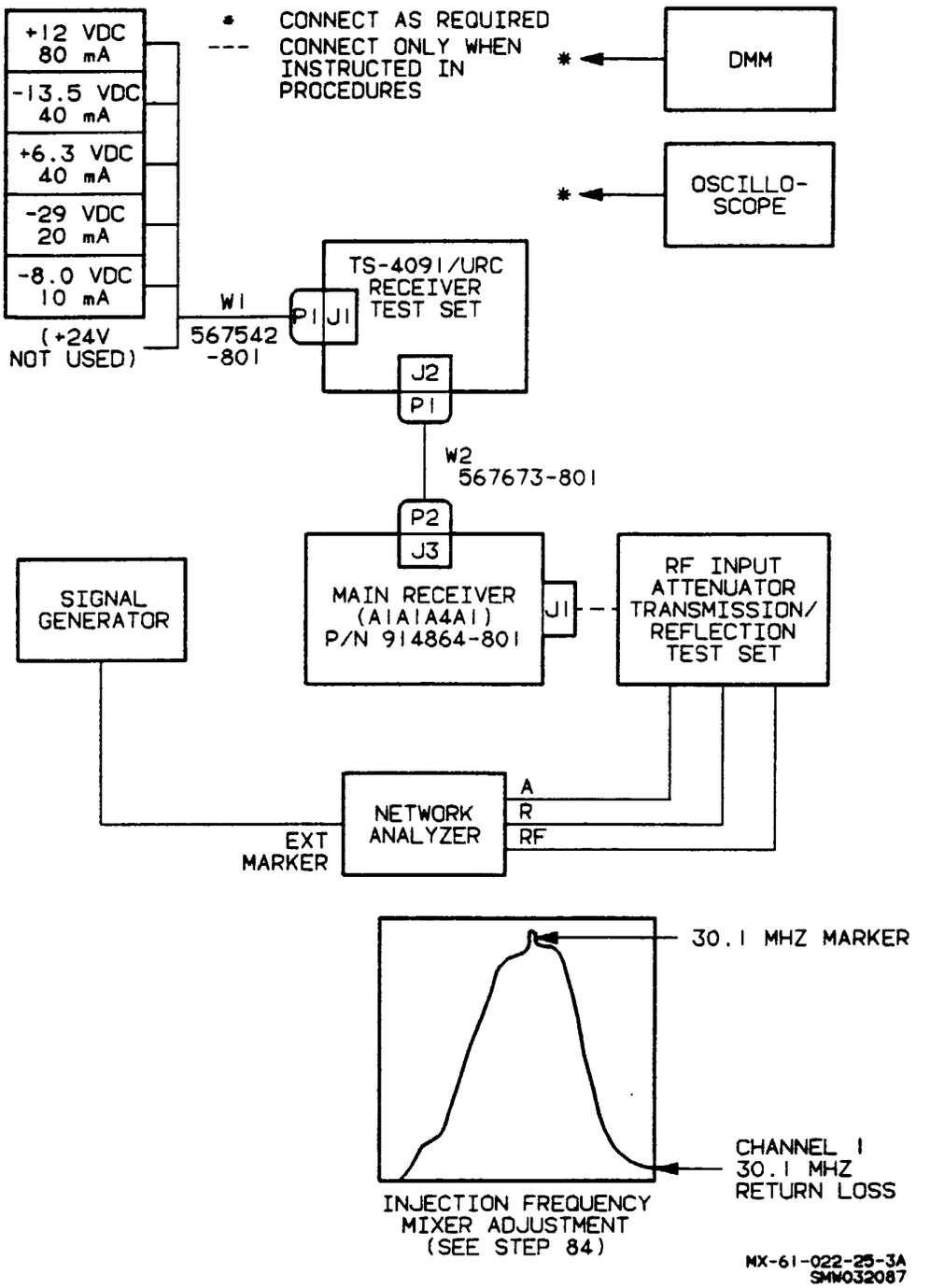


Figure 5-8. Main Receiver Assembly A1A1A4 Alignment Connection Diagram (Sheet 3 of 3)

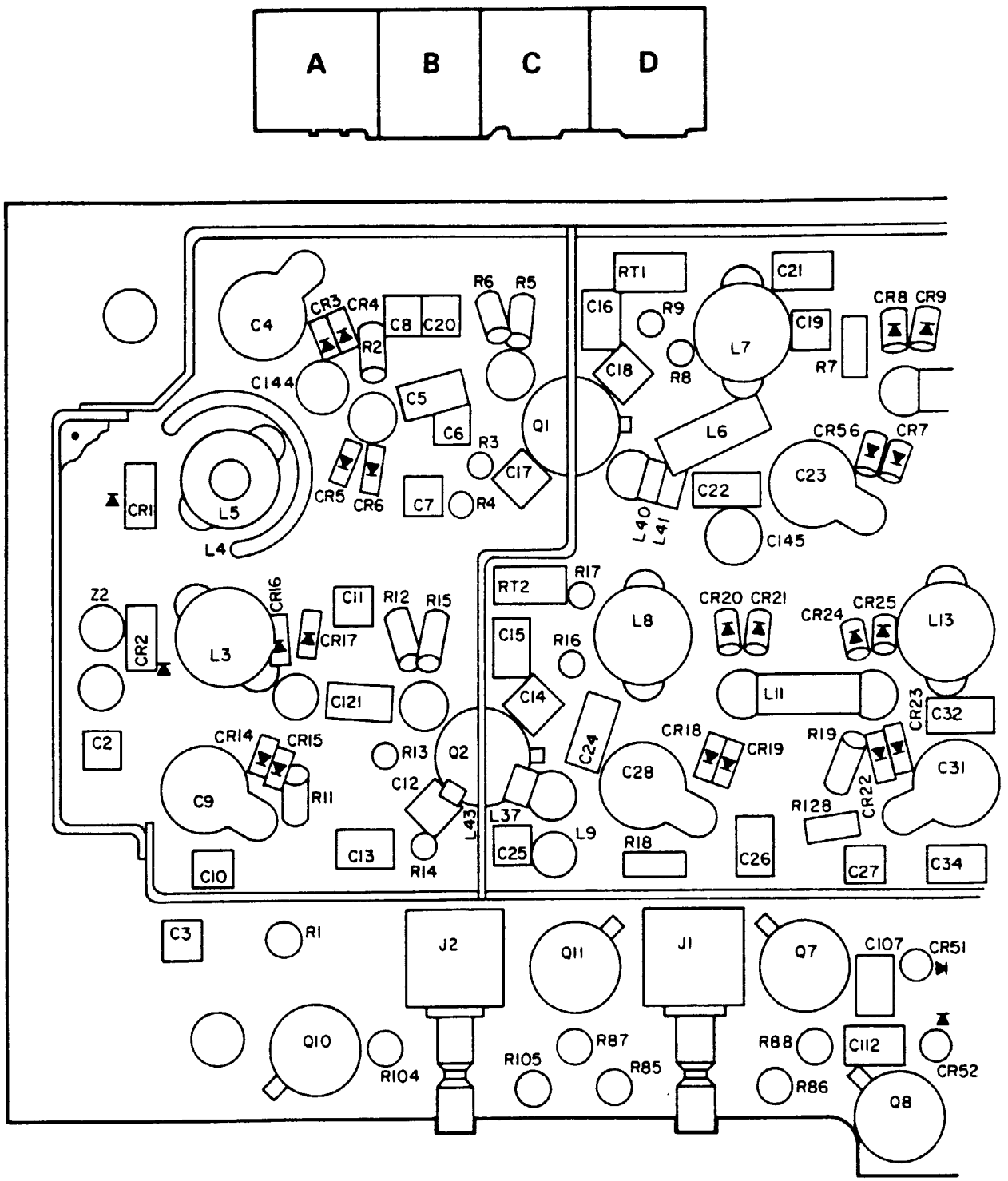
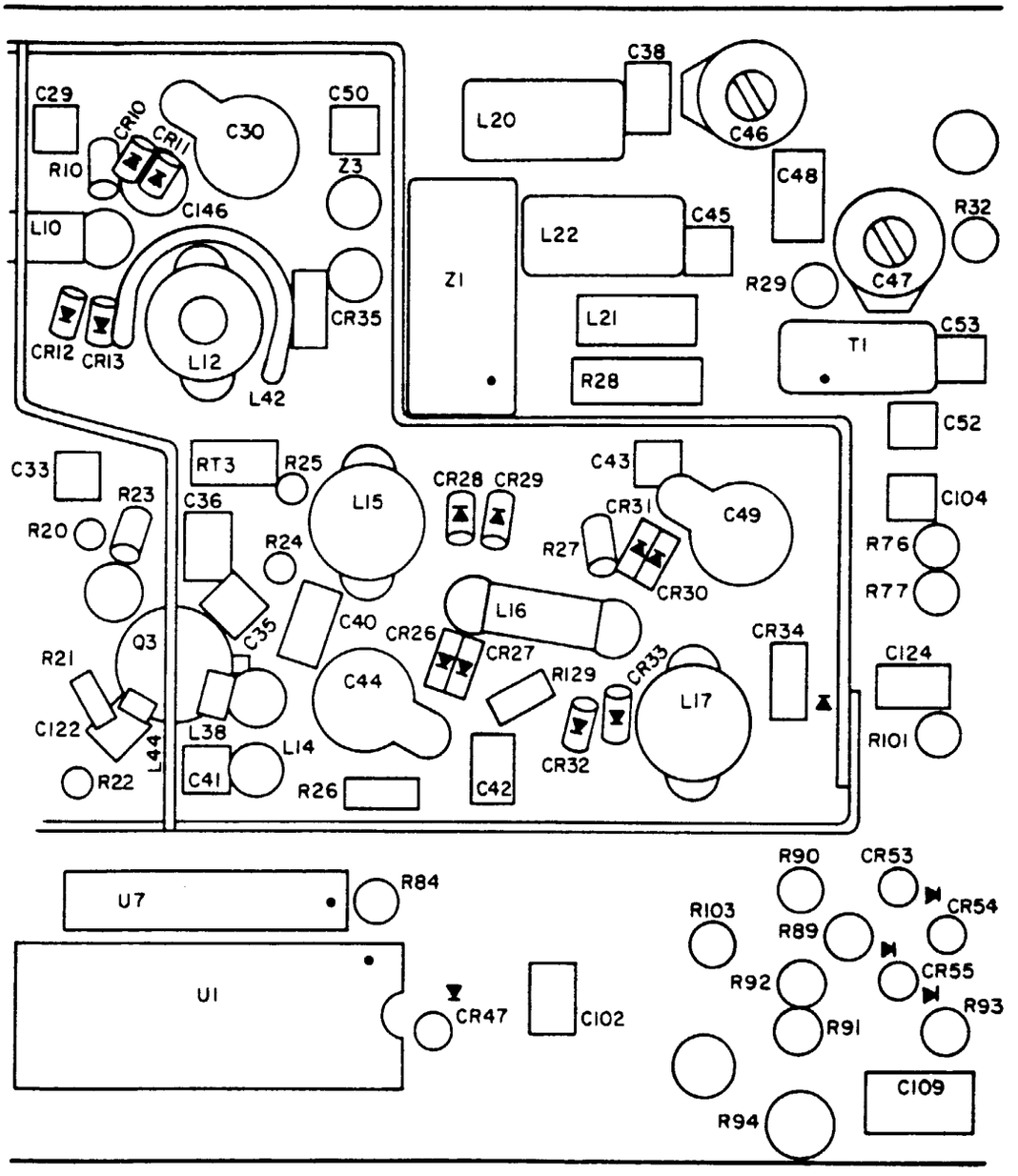


Figure 5-9. Main Receiver Assembly A1A1A4 Component and Test Point Location Diagram (Sheet 1 of 5)



B

MX-022-26-2
REF MX-61-022-IPB-11-2A

Figure 5-9. Main Receiver Assembly A1A1A4 Component and Test Point Location Diagram (Sheet 2 of 5)

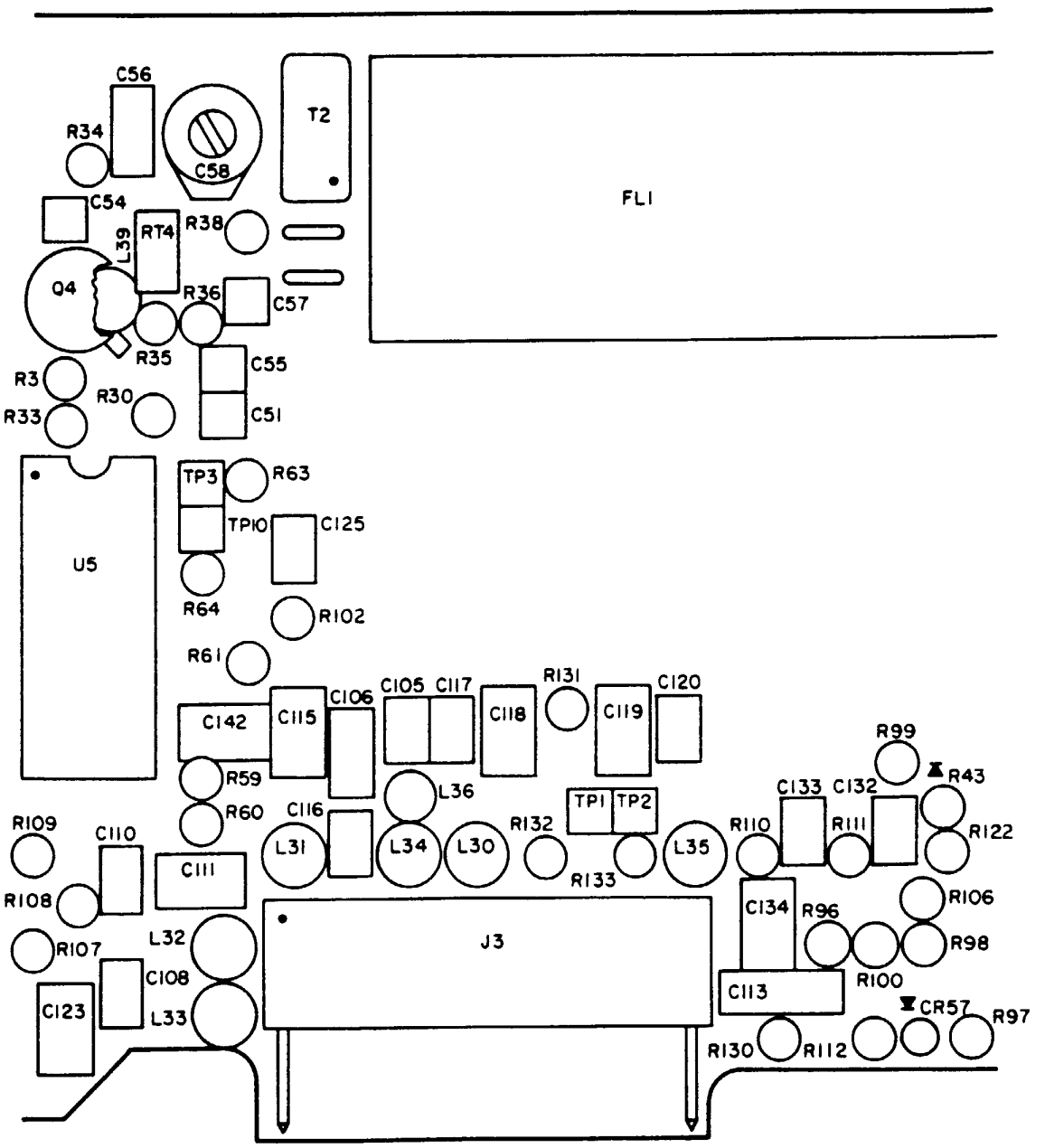
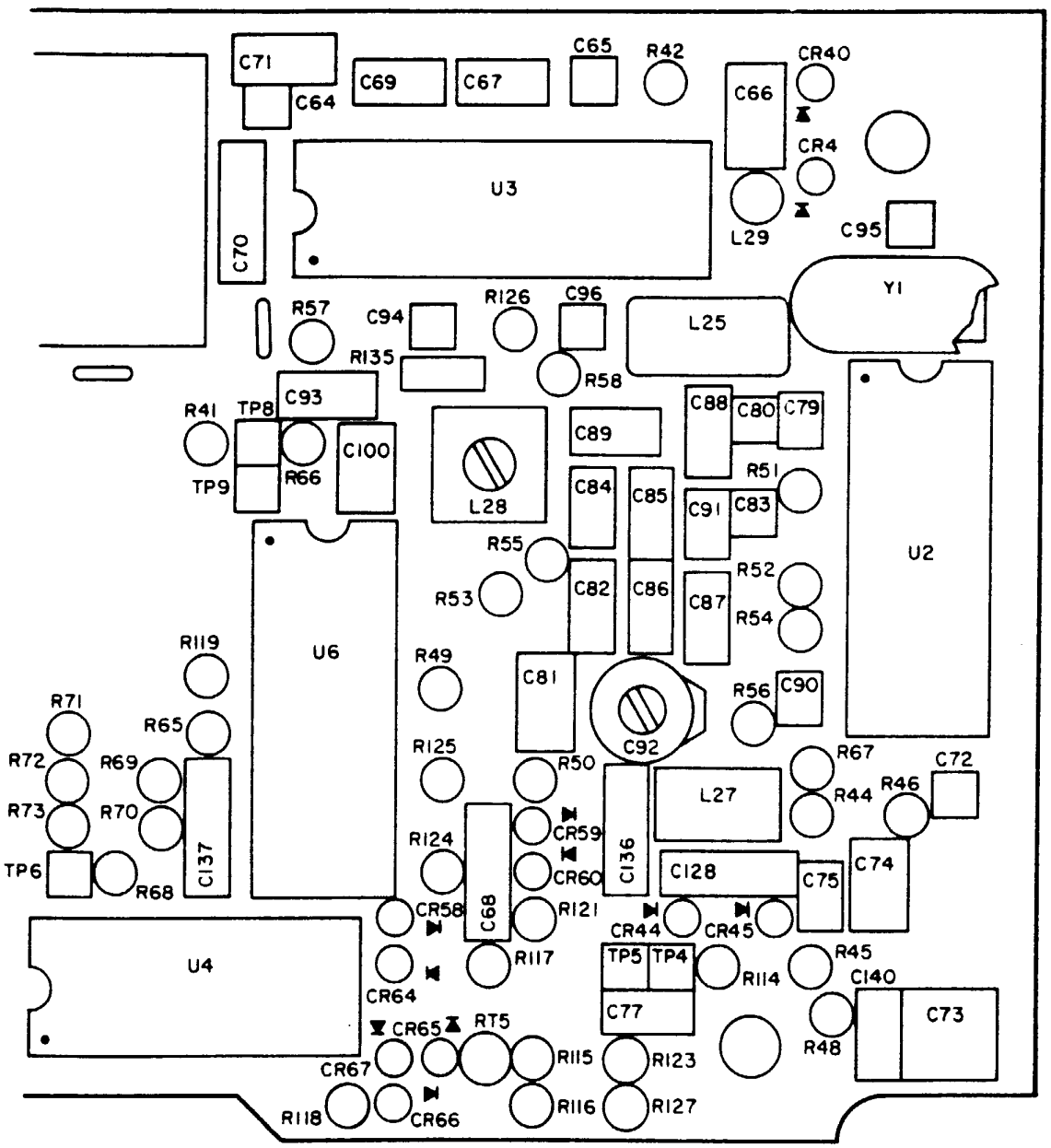


Figure 5-9. Main Receiver Assembly A1A1A4 Component and Test Point Location Diagram (Sheet 3 of 5)



D

MX-022-26-4
REF MX-61-022-IP8-11-4A

Figure 5-9. Main Receiver Assembly A1A1A4 Component and Test Point Location Diagram (Sheet 4 of 5)

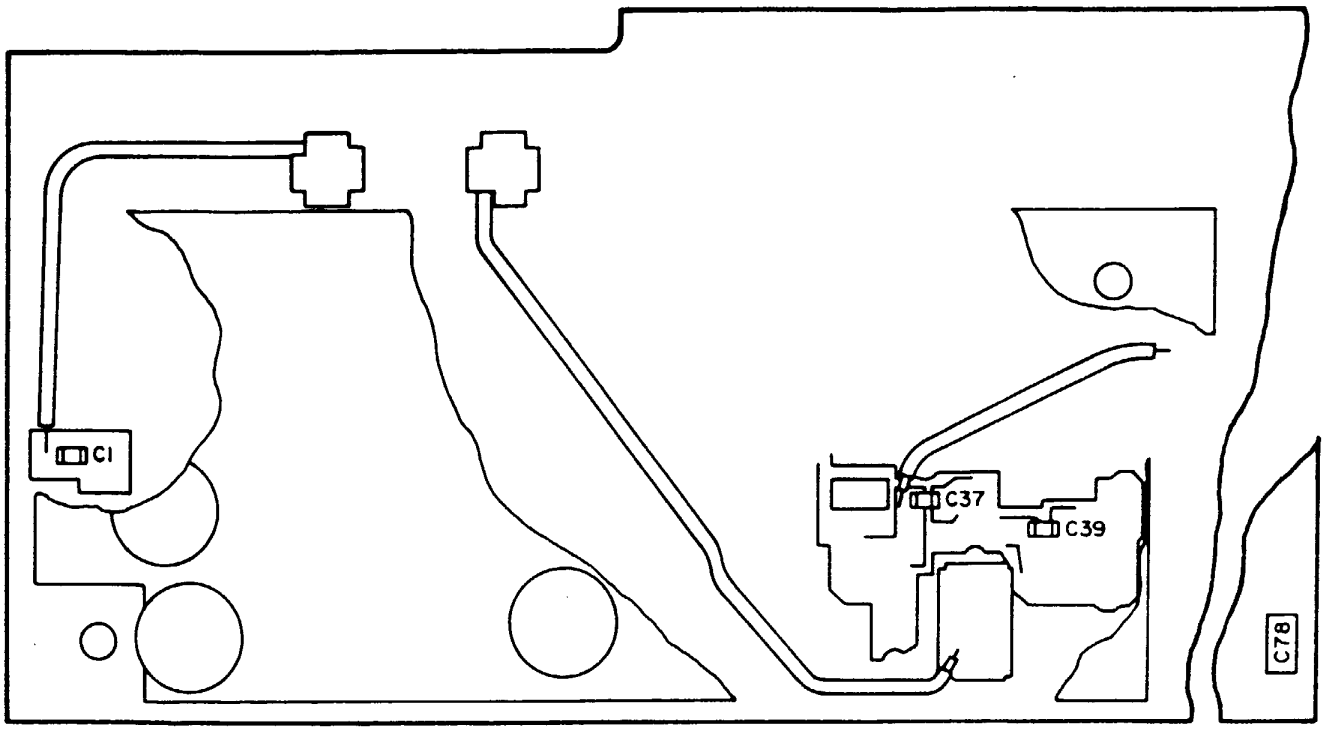


Figure 5-9. Main Receiver Assembly A1A1A4 Component and Test Point Location Diagram (Sheet 5 of 5)

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			NOTE All RF input signals referred to are open circuit levels. (6 dB pad at receiver input.)	
1.			Preset test set controls as follows:	(See figure 5-23 for trouble analysis.)
			Control — Position	
			S1 DC POWER-ON/(off) — off (down position)	
			STATUS INPUTS section:	
			S2 RT ADDR 0 — 0 S3 RT ADDR 1 — 0 S4 RT ADDR 2 — 0 S5 RT DB — 0	
			MAIN RECEIVER section:	
			R1 SQUELCH — max ccw	
			R2 TUNE VOLTAGE — max ccw	
			GUARD RECEIVER section:	
			R3 VOL — max ccw	
			S8 SQUELCH-DISABLE/ENABLE — ENABLE	
			S9 GUARD STB/ACT — STB	
			S7 MODULE SELECT-MAIN/GUARD — GUARD	
			R4 SPEAKER VOLUME — max ccw	

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
1. Cont			Assure that RF and audio inputs are not connected to UUT. Preset R72 (refer to figure 5-12) on UUT to max cw (squelch ON).	
2.	Connect equipment as shown in Figure 5-10. For negative voltages, connect red terminal to (+) and black to (-). Test set inverts polarity internally. Do not use ground jumper from (-) terminal to ground on power supply.		Adjust input power supplies to indicated levels. Set test set DC POWER S1 to ON.	
3.	DMM		Measure voltage drop across following test set test points and calculate current for each using resistance factor listed. Test set TP / Gnd / Resistance factor / Maximum current 7 / 13 / not used / not used 8 / 14 / 1 Ohm / 9.5 mA 9 / 15 / not used / not used 10 / 16 / not used / not used 11 / 17 / 1 Ohm / 18 mA 12 / 18 / 1 Ohm / 35 mA After completion of power supply input current measurements set R72 on UUT to max ccw position.	

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			Sensitivity	
4.	Test set		STATUS INPUTS section, select the following:	
			Address S2 S3 S4 DATA S5 STB ACT S6	Indicators lit
			0 1 0 1 press (mom)	GUARD ON
			1 0 0 0 press (mom)	LOCAL
			0 0 0 1 press (mom)	H/Q OFF
5.	Signal generator	UUT J1	Set Signal Generator for output 3 µV at 243.000 MHz amplitude modulated 30% at 1000 Hz.	
6.	Distortion analyzer RMS voltmeter	Test set PLAIN J19 GND J20	Set reference level on distortion analyzer.	
7.	Signal generator		Remove AM modulation.	
8.	Distortion analyzer RMS voltmeter	Test set PLAIN J19 GND J20	Measure signal plus noise to noise to noise (S + N/N) at test set OUTPUTS-RCV PLAIN.	> = 12 dB below reference.
			AGC Response	
9.	Signal generator	UUT J1	Set Signal Generator for output 1 mV modulated 90% at 1000 Hz.	
10.	Distortion analyzer RMS voltmeter	Test set J19 J20	Measure audio level at OUTPUTS-RCV PLAIN and record output level as audio level reference (A ref).	Record level (dBm) (A ref)
11.	Signal generator	UUT J1	Set signal generator for output of -97.5 dBm (3 uV) modulated 90% at 1000 Hz.	

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
12.	Distortion analyzer RMS voltmeter	Test set J19 J20	Measure audio level at OUTPUTS-RCV PLAIN. **CAUTION** The following inputs are considerably above normal input levels. Use only as long as required to observe audio output measurements.	A ref value +4 or -3 dB with respect to reference A.
13.	Signal generator	UUT J1	Increase RF level of signal generator to +7 dBm (500 mV).	
14.	Distortion analyzer RMS voltmeter Oscilloscope	Test set J19 J20	Measure audio level at RCV PLAIN. Increase RF level of signal generator to +13 dBm (1.0 V) and verify audio is present at J19 and J20. Audio Output Level	A ref +4 or -3 dB with respect to reference A.
15.	Signal generator		Set signal generator for output of 1 mV modulate 90% at 1000 Hz.	
16.	Distortion analyzer RMS voltmeter	Test set FIXED J21 GND J22	Measure audio level at OUTPUTS-AUDIO FIXED.	1.0 Vrms min.
17.	Distortion analyzer RMS voltmeter	Test set PLAIN 19 GND J20	Set VOL (R3) max cw. Measure audio level at OUTPUTS-RCV PLAIN.	3.16 Vrms min.

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			Audio Frequency Response	
18.	Signal generator		Set signal generator for output of -47 dBm (1 mV) modulated 50% at 1000 Hz.	
19.	Distortion analyzer RMS voltmeter.	Test set J19 J20	Measure audio level and establish audio reference.	Record level dBm (reference).
20.	Signal generator Distortion analyzer RMS voltmeter.	Test set J19 J20	Set modulation frequency to 530 Hz and slowly increase to 3050 Hz.	Audio level varies less than ± 2 dB from reference.
21.	Signal. generator Distortion analyzer RMS voltmeter.	Test set J19 J20	Set modulation frequency to 350 Hz and slowly increase to 530 Hz.	Audio level varies less than ± 3 dB from reference.

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
22.	Signal generator Distortion analyzer RMS voltmeter	Test set J19 J20	Set modulation frequency to 3050 Hz and slowly increase to 3500 Hz. **NOTE** If roll off at 3500 Hz is greater than 2.9 dB remove C112 and repeat steps 18 through 22.	Audio level varies less than ± 3 dB from reference.
23.	Signal generator RMS voltmeter	Test set J19 J20	Set modulation frequency to 100 Hz.	Audio level varies more than 9 dB from reference.
24.	Signal generator Distortion analyzer	Test set J19 J20	Set modulation frequency to 7000 Hz. Audio Distortion	Audio level varies more than 13 dB from reference.
25.	Signal generator Distortion analyzer	Test set J19 J20	Set signal generator for output of -47 dBM (1 mV). Set modulation to 50% at 1000 Hz and measure audio distortion.	Does not exceed 10%
26.	Signal generator Distortion Analyzer	Test set J19 J20	Set modulation frequency to 300 Hz and slowly increase to 3500 Hz and measure audio distortion.	Does not exceed 10%

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			Selectivity and Passband Ripple	
27.	Signal generator		Set signal generator for output of -97 dBm (3.0 uV) at 243.000 MHz unmodulated.	
28.	DMM	Test set +TP 29 -TP 32	Measure AGC voltage at GUARD RECEIVER section AGC TP 29 on test set and record value as AGC reference voltage (AGC ref).	Record AGC voltage reference.
29.	Signal generator DMM		Set signal generator for output of -91dBm (6.0 uV) at 242.970 MHz and measure AGC voltage.	Less than AGC reference
30.			Repeat step 29 with a frequency setting of 243.030 MHz at signal generator	Less than AGC reference
31.	Signal generator DMM	Test set +TP29 -TP32	Set signal generator for output of -31 dBm (6 mV) at 242.925 MHz. Measure AGC voltage	Greater than AGC reference
32.			Repeat step 31 with a frequency setting of 243.075 MHz.	Greater than AGC reference
33.	Signal generator DMM	Test set +TP29 -TP32	Set signal generator for output of -91 dBm (6.0 uV) unmodulated at 243.000 MHz. Measure GUARD AGC and record AGC reference.	Record AGC voltage (reference)

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
34.	Signal generator DMM	Test set +TP29 -TP32	Set RF input frequency to 243.029 MHz and slowly decrease to 242.971 MHz while measuring AGC voltage.	Record highest and lowest AGC voltages and frequencies where occurred.
35.	Signal generator DMM	Test set +TP22 -TP20	At the frequencies of the highest AGC voltage, increase the signal generator output to provide the lowest AGC voltage of step 34.	The change in signal generator output level is the peak to valley ratio and shall not shall not exceed 3.
			Squelch Operation	
36.	Signal generator		Set RF output to off. Tune to 243.000 MHz 30 % modulation at 1000 Hz.	
37.	DMM	Test set SQUELCH TP28 GND TP32	Set R72 (squelch adjust) max ccw.	Guard receive is unsquelched (TP28 < 5.0 Vdc)
38.	DMM	Test set SQUELCH TP28 GND TP32	Set R72 max cw.	Guard receiver is squelched with no RF input. (TP28 < 0.4 Vdc)
39.	DMM	Test set SQUELCH TP28 GND TP32	Set RF output switch to ON and slowly increase RF output.	Verify receiver unsquelches between -91 dBm and -81 dBm. (TP28) 5.0 Vdc).

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
40.	Signal generator DMM	Test set SQUELCH TP28 GND TP32	Set RF output to -102 dBm (1.5 uV) and set RF	Guard receiver is squelched. (TP28 > 0.1 Vdc)
41.	Signal generator DMM	Test set SQUELCH TP28 GND TP32	Slowly increase RF output level until guard receiver squelch breaks.	Guard receiver squelch breaks between -91 dBm and -84 dBm (TP28 > 5.0 Vdc).
42.	Signal generator		Set signal generator for output of -102 dBm (1.8 uV) at 243.000 MHz modulated 30% at 1000 Hz.	
43.	UUT DMM	Test set SQUELCH TP28 GND TP32	Set R72 so squelch breaks at -102 dBm of RF input.	TP28 > 5.0 Vdc.
44.	Signal generator	Test set SQUELCH TP28 GND TP32	Slowly decrease RF output until guard receiver squelches.	Guard receiver squelches between -104 dBm and -109 dBm RF input TP28 < 0.4 Vdc.
			Audio Output Levels	
45.	Signal generator		Set RF output to off.	
46.	UUT		Adjust R100 to max cw position.	
	Test set		Set VOL (R3) on test set max cw.	

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
48.	Distortion analyzer	Test set J19 J20	Measure audio level at RCV PLAIN output.	2.25 Vrms min.
49.	Oscillator	Test set J15 J16	Inject signal of 1000 Hz at 0.8 Vrms into INPUTS-MAIN AUDIO.	
50.	Dstorton analyzer	Test set J21 GND J22	Measure audio level at AUDIO FIXED output.	1.20 Vrms min.
51.	Oscillator	Test set J11 GND J12	Inject signal of 3000 Hz at 1.75 Vrms at INPUTS-WARNING TONE	
52.	Distortion analyzer	Test set J19 GND J20	Measure audio level at OUTPUTS-RCV PLAIN. Main Squelch Indicator In/Out	2.5 Vrms min.
53.	DMM	Test set TP26 TP32	Set DMM to function as ohmmeter. Verify RT DB 2 is in high impedance state.	HI-Z state > 10 megohm
54.	DMM	Test set TP26 TP32	Set DMM to function as dc voltmeter. Measure RT DB 2 and verify logic 0 condition when SQUELCH DISABLE/ENABLE S8 is in ENABLE position and GUARD STB S9 is set to in ACT position position (spring loaded).	< +0.4 Vdc
55.	DMM	Test set TP26 TP32	Measure RT DB 2 and verify logic 1 condition when SQUELCH DISABLE/ENABLE (S8) is in DISABLE position and GUARD STB is set to ACT position (spring loaded).	< +5.0 Vdc

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			Local/Remote Operation	
56.	Test set		Adjust VOL R3 control max cw.	
57.	Signal generator		Turn RF output on and adjust signal generator for -47 dBm (1.0 mV) 243.000 MHz modulated 90% at 1000 Hz.	
58.	Distortion analyzer	Test set J19 J20	Measure and record RCV PLAIN output audio level for reference audio.	Record level (dBm) (reference)
59.	Test set		Adjust VOL (R3) control max ccw and select S2-5 to 1 0 0 1 (STATUS INPUTS section). Press and release S6.	MODULE STATUS REMOTE led lighted
60.	Distortion analyzer	Test set J19 J20	Measure RCV PLAIN audio level and compare with audio level reference recorded in step 58.	< 0.5 dB lower than audio level reference
61.	Test set		Set S2-5 to 1 0 0 0 and press and release S6.	MODULE STATUS LOCAL led led lighted
			Guard On/Off	
62.	Test set		Set S2-5 to 0 1 0 0 and press and release S6.	MODULE STATUS GUARD OFF lighted
63.	DMM	Test set TP31 TP32	Measure and verify GUARD ON/OFF voltage is logic 0.	< +0.4 Vdc
64.	Test set		Set S2-5 to 0 1 0 1 and press and release S6.	MODULE STATUS GUARD ON lighted

Table 5-11. Guard Receiver CCA A1A1A5 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			Rcv Audio (CIPHER) In/Out	
65.	Test set		Set S1 to off (down position) and remove all inputs from test set.	
66.	DMM	Test set J17 J9	With DMM set to function as ohmmeter, measure resistance across WB AUDIO input and RCV CIPHER output.	100 ± 5 Ohms
67.	End of test. De-energize and remove test set and test equip-ment from UUT.			

Table 5-12. Guard Receiver CCA A1A1A5 Alignment Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
1.			Preset test set controls as follows: Control — Position DC POWER section: S1 DC POWER-ON/(off) — off (down position) MAIN RECEIVER/GUARD RECEIVER section: S7 MODULE SELECT-MAIN/GUARD — GUARD GUARD RECEIVER section: R3 GUARD RECEIVER-VOL — max ccw S8 SQUELCH-DISABLE/ENABLE — DISABLE **NOTE** All RF input signals referred to are open circuit levels. (6 dB pad at receiver input.) Adjust input power supplies to indicated levels. Set test set DC POWER S1 to ON.	

Table 5-12. Guard Receiver CCA A1A1A5 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
2.	Connect equipment as shown in Figure 5-11. For negative voltages, connect red terminal to (+) and black to (-). Test set inverts polarity internally. Do not use ground jumper from (-) terminal to ground on power supply.			
	DMM		Prior to complete set up of Guard Receiver UUT for alignment procedure, connect and monitor individual power supply currents to UUT. Measure voltage drop across the following test set test points and calculate current for each using resistance factor listed.	
			Test set TP: 7, 13 — Resistance factor: not used	Maximum current: not used
			8, 14 — 1 Ohm	9.5 mA
			9, 15 — not used	not used
			10, 16 — not used	not used
			11, 17 — 1 Ohm	18 mA
			12, 18 — 1 Ohm	35 mA
3.	Test set		STATUS INPUTS section, select the following:	
			Address S2 S3 S4: 0 1 0 — DATA S5: 1 — STB ACT S6: press (mom)	Indicators lit: GUARD ON
			1 0 0 — 0 — press (mom)	LOCAL
			0 0 0 — 1 — press (mom)	H/Q OFF

Table 5-12. Guard Receiver CCA A1A1A5 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
4.	Connect equipment as shown in figure 5-11.		Adjust tracking generator to 243.000 MHz at -38 dBm (2.9 mV)	
5.	Tracking generator Spectrum analyzer	UUT J1 UUT TP3 GND	Inject Tracking Generator signal at UUT ANT IN (J1). Adjust L3, L6, L7, and L10 for symmetrical response about center frequency of 243.000 MHz.	Adjust for symmetrical response.
6.	Spectrum Analyzer	UUT TP9 GND	Adjust L11 for maximum amplitude and verify frequency is 212.900 MHz ± 3.0 kHz.	Maximum amplitude at 212.900 MHz on on Spectrum analyzer
7.	Signal Generator	UUT J1	Set signal generator for output of -98 dBm (2.9 mV) at 243.000 MHz and inject at UUT ANT IN J1.	
8.	Digital Multimeter	Test Set TP29	Monitor GUARD AGC voltage at Test Set and adjust C29, C60, L12, and L21 on UUT for minimum AGC voltage. **NOTE** Adjustment of L21 is critical.	Minimum AGC voltage
9.	Tracking Generator	UUT Q3-3	Inject tracking generator signal of -38 dBm (2.9 mV) at 243.000 MHz to Q3-3.	
10.	Spectrum analyzer	UUT TP4	Using HI-Z probe at TP4 monitor spectrum analyzer while adjusting C29 and C60 on UUT for minimum crystal filter passband ripple.	Minimum passband ripple

Table 5-12. Guard Receiver CCA A1A1A5 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
11.	Signal generator	UUT J1	Inject signal generator -98 dBm at 243.000 MHz modulated 90% at 1000 Hz at UUT ANT IN (J1).	
12.	Oscilloscope	UUT TP10	Monitor UUT TP10 with oscilloscope and adjust C93 to center noise spikes about baseline of frequency on oscilloscope display.	Center noise spikes about baseline
13.	Signal generator		Adjust output level on signal generator for -47 dBm (1 mVrms) modulated 30% at 1000 Hz.	
14.	Distortion analyzer RMS voltmeter	TP6	UUT Select resistor R64 to provide 360 ± 20 mVrms at TP6 as measured on RMS voltmeter.	
15.	Test set		Set SQUELCH DISABLE/ENABLE (S8) to ENABLE.	
16.	Signal generator		Set signal generator for rf output of -98 dBm (2.9 µVrms) at 243.000 MHz modulated 30% with 1000 Hz.	
17.		UUT R72	Adjust squelch potentiometer to max cw position.	
18.	DMM	Test set TP21 TP20	Increase RF output until squelch breaks.	TP21 >5.0 Vdc
19.	Signal generator	UUT R105 Test set TP21 TP20	Select resistor R105 to provide squelch break between -89 dBm and -86 dBm.	TP21 >5.0 Vdc
20.	End of test. Deenergize and remove test set and test equipment from UUT.			

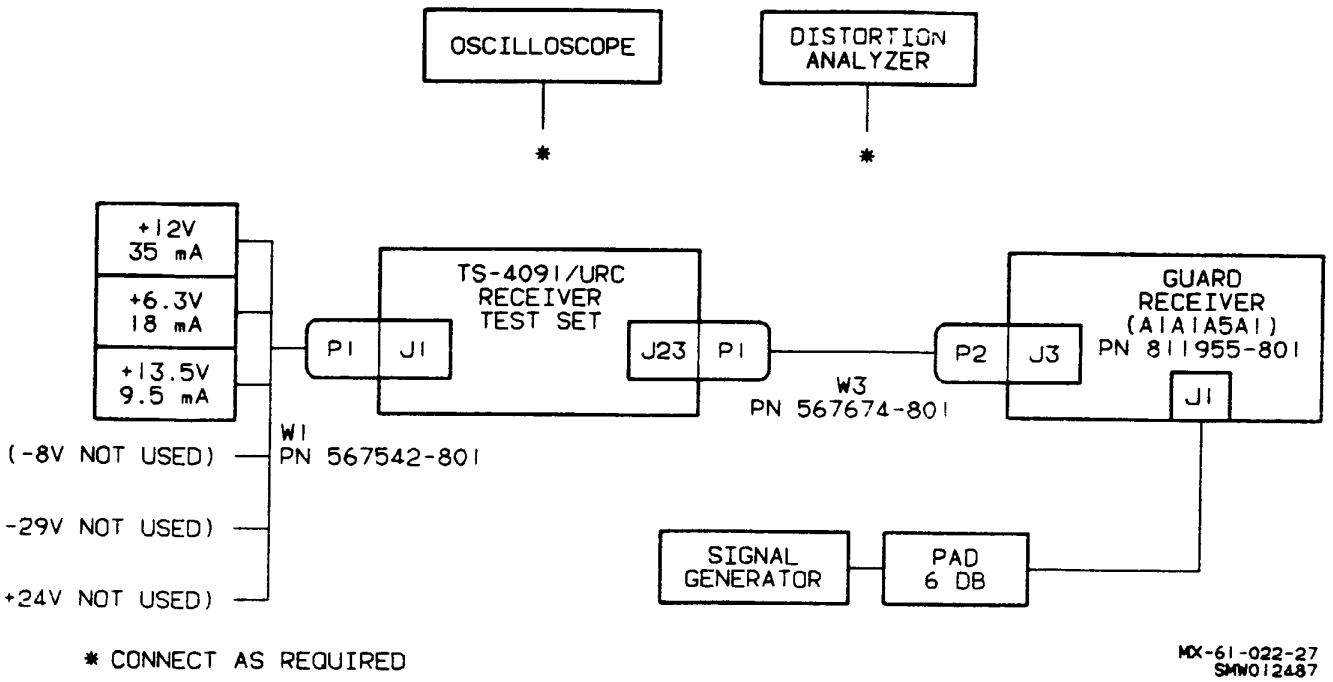


Figure 5-10. Guard Receiver Assembly A1A1A5 Performance Test Connection Diagram

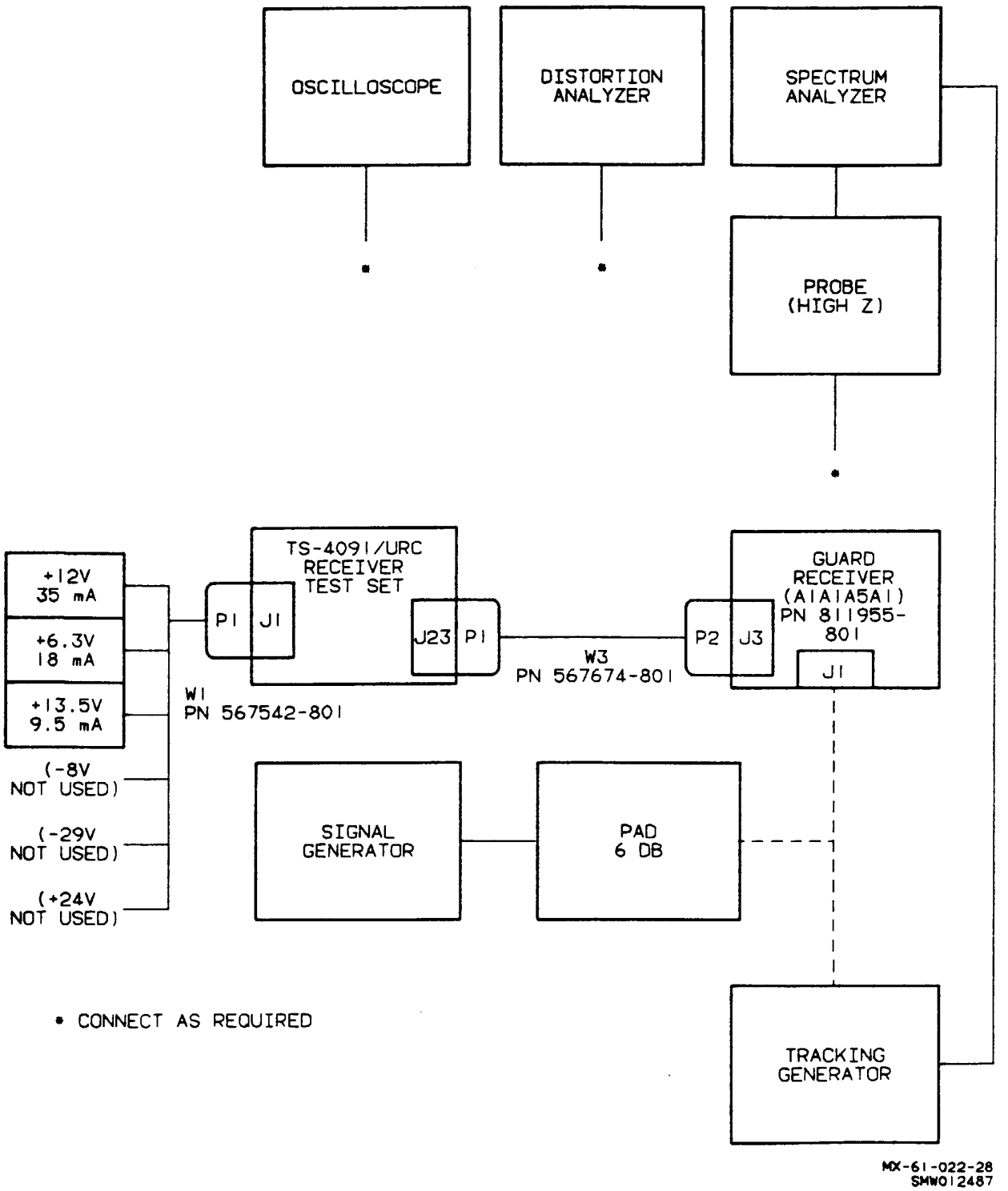
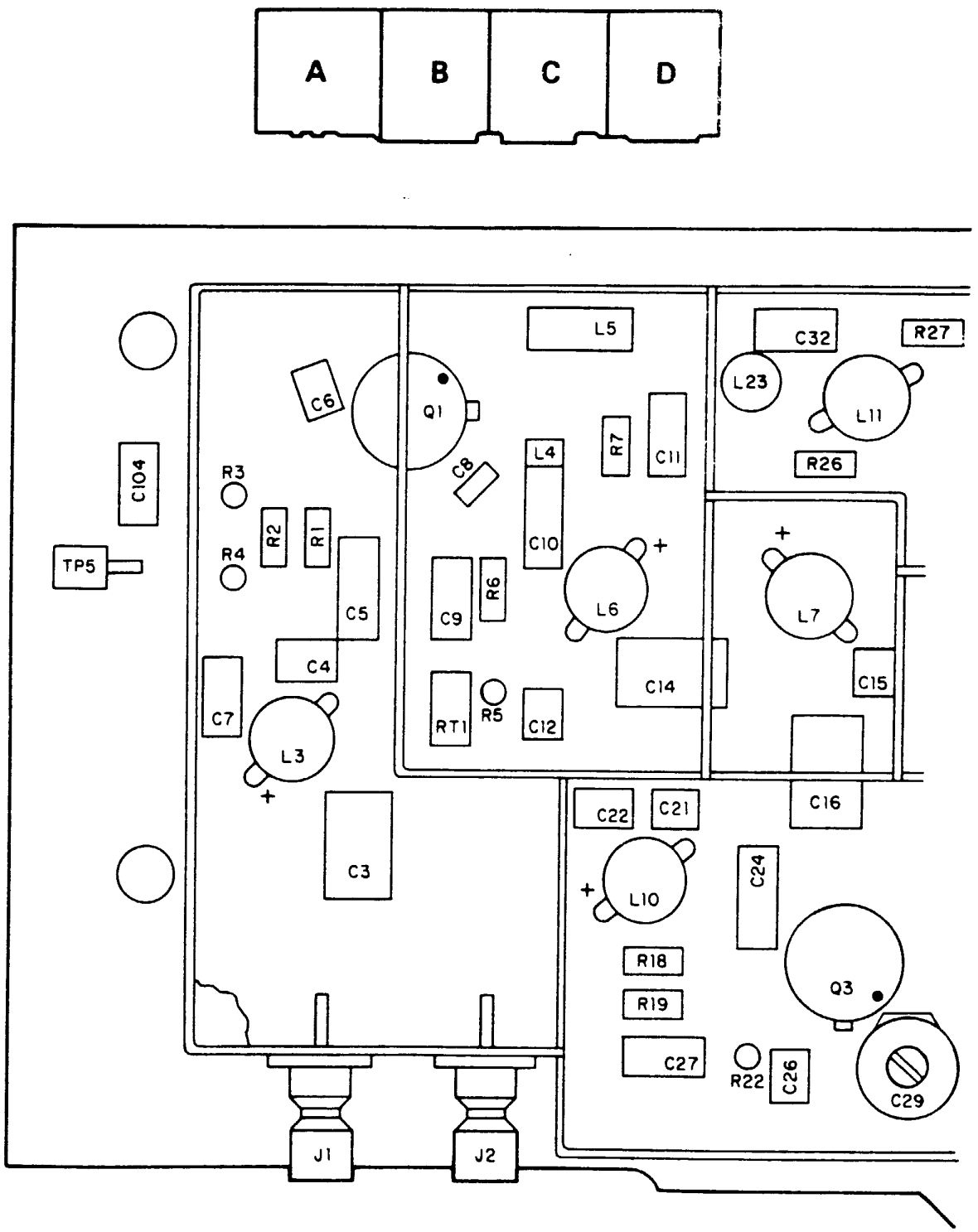


Figure 5-11. Guard Receiver Assembly A1A1A5 Alignment Connection Diagram



REFERENCE DESIGNATIONS ARE ABBREVIATED.
PREFIX WITH A1A1A5A1.

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REF MX-61-022-IP8-7-1A

Figure 5-12. Guard Receiver Assembly A1A1A5 Component and Test Point Location Diagram (Sheet 1 of 5)

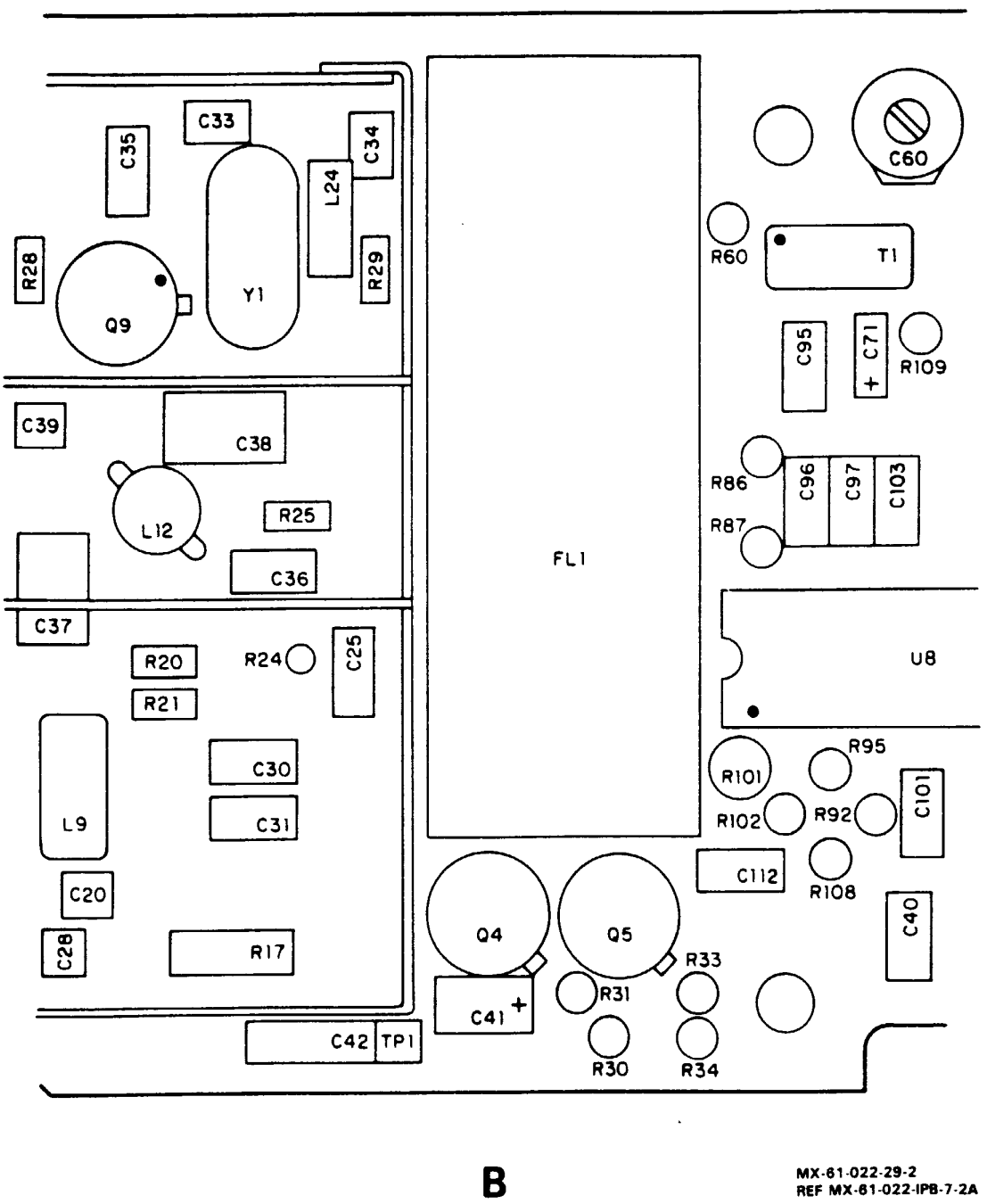
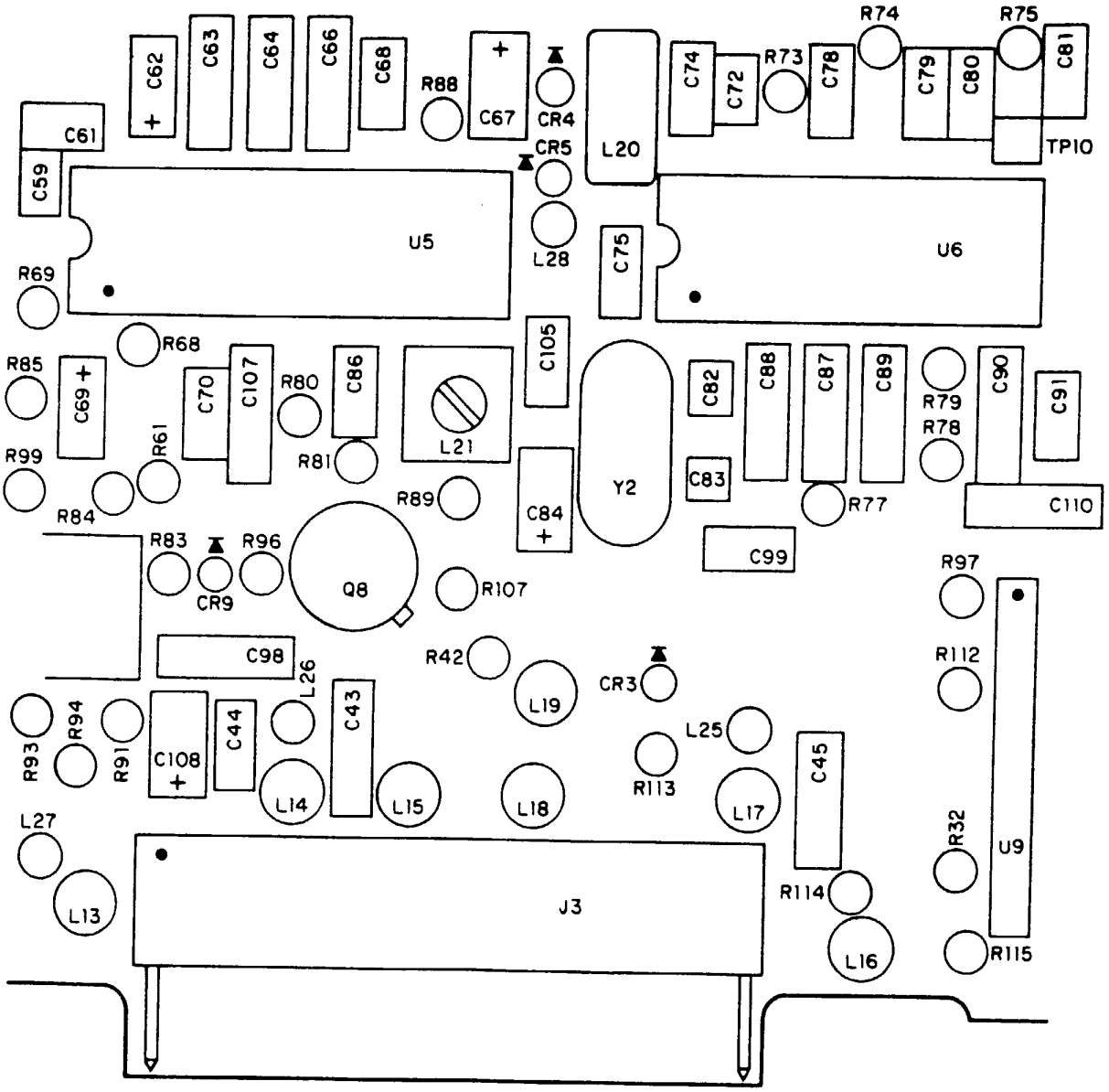


Figure 5-12. Guard Receiver Assembly A1A1A5 Component and Test Point Location Diagram (Sheet 2 of 5)



C

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REF MX-61-022-IPB-7-3A

Figure 5-12. Guard Receiver Assembly A1A1A5 Component and Test Point Location Diagram (Sheet 3 of 5)

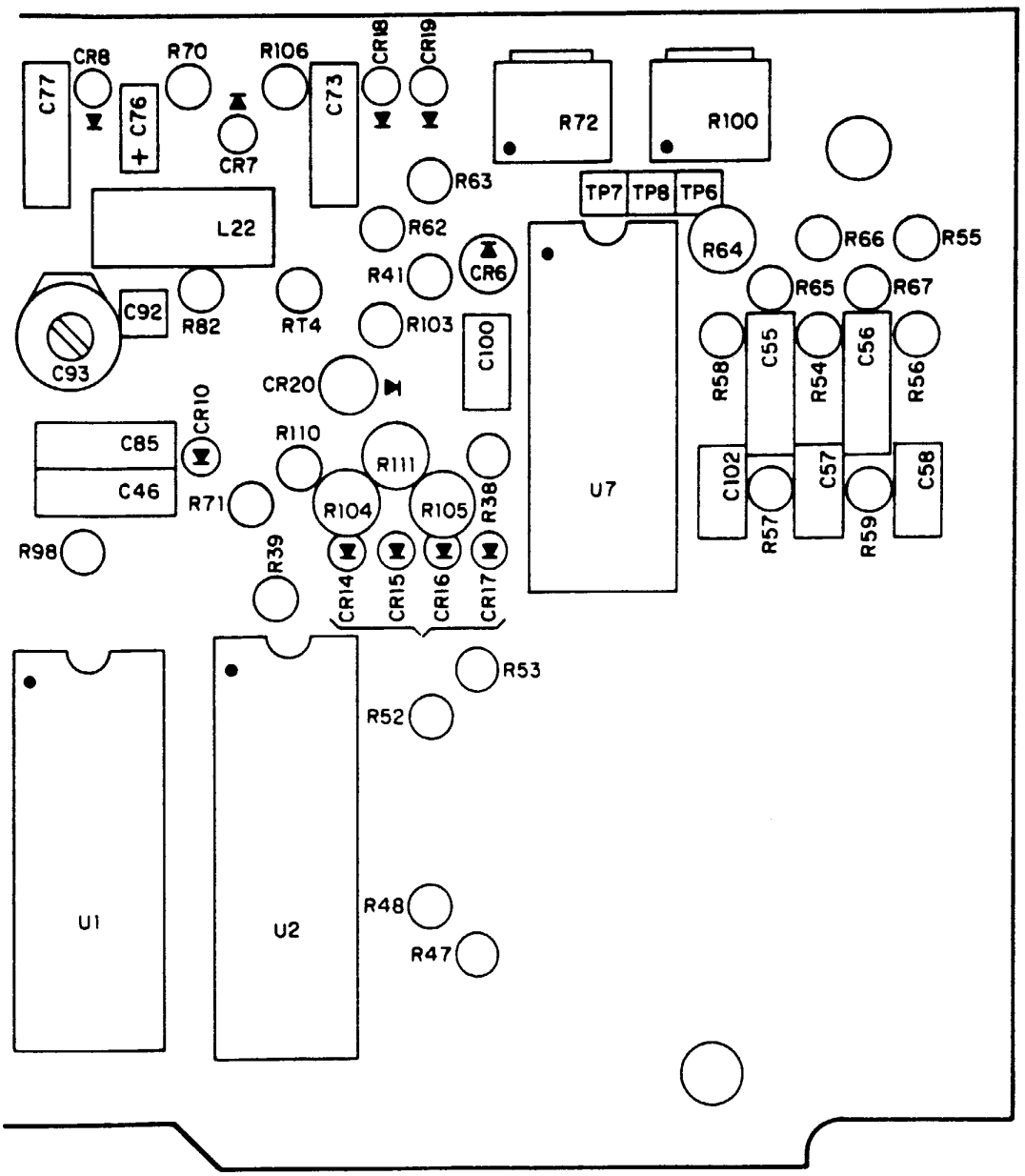


Figure 5-12. Guard Receiver Assembly A1A1A5 Component and Test Point Location Diagram (Sheet 4 of 5)

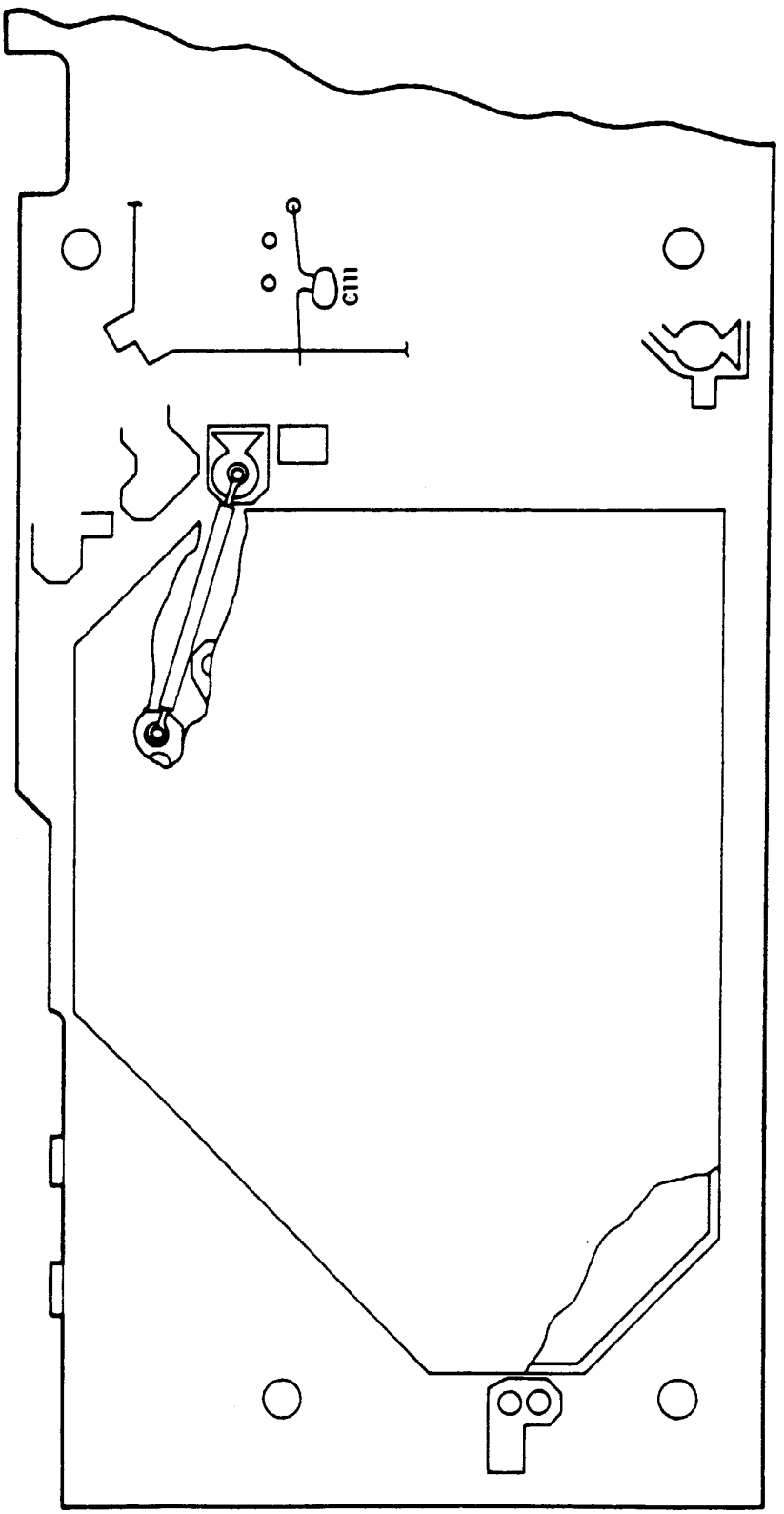


Figure 5-12. Guard Receiver Assembly A1A1A5 Component and Test Point Location Diagram (Sheet 5 of 5)

Table 5-13. Synthesizer CCA A1A1A6 Performance Test Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
1.			Set Synthesizer Test Set controls as follows: S1 to OFF S2 to RECEIVE	(See figure 5-24 for trouble analysis.)
2.	Connect equipment as shown in Figure 5-13 sheet 1 For negative voltages, connect red terminal to (+) and black to (-). Test set inverts polarity internally. Do not use ground jumper from (-) terminal to ground on power supply.		Adjust input power supplies to indicated levels.	
3.			Set test set S1 to ON.	
4.	DMM		Measure voltage drop across following test set test points and calculate current for each. For TP 1 and 2 use 10 ohms as resistance factor for all others use 1 ohm.	

Test Set TP	Nominal Value		Lower (mA)	Upper (mA)
1, 2	-29.00	Vdc	0.5	2.75
3, 4	-13.50	Vdc	15	25
5, 6	+6.30	Vdc	103	140
7, 8	+12.00	Vdc	30	50

Table 5-13. Synthesizer CCA A1A1A6 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
5.	DMM		Measure tune voltage at following frequencies.	
				Tune Voltage (Vdc)
		Test Set GND POS	Test Set frequency;	
		TP18, 15	116.000	2.468 ± .025
			132.000	3.468 ± .025
			149.000	4.537 ± .025
			225.000	1.719 ± .025
			300.000	4.063 ± .025
			399.000	7.172 ± .025
6.	DMM		Tune to any valid frequency, verify reference voltage.	
		Test Set GND POS	Ref. Voltage	Limit
		TP16, 14	J1-14 (+8Vdc)	+8.00 ± 0.40 Vdc
		TP16, 11	J1-7 (-8Vdc)	-8.00 ± 0.02 Vdc
7.	DMM		Tune to any valid VHF frequency.	
		Test Set GND POS		
		TP22, 19	(116 to 149.975)	+5.0 ± .4 Vdc
		TP22, 20	Verify logic high.	CR6, CR7, CR8 ON.
8.	DMM	Test Set GND POS TP22, 19 TP22, 20	Tune to any valid UHF frequency greater than 310.000 MHz.	Logic low < .4 Vdc
9.	DMM	Test Set GND POS TP22, 21	Tune to any valid UHF or VHF frequency.	4.0 to 5.6 Vdc

Table 5-13. Synthesizer CCA A1A1A6 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
10.	Connect frequency counter to UUT J4.	UUT J4	Tune to any valid frequency, verify proper frequency.	Frequency: 800 kHz ± 100 Hz
11.	Move output probe to oscilloscope.	J4	Verify voltage levels.	High Level: +2.8 Vdc minimum Low Level: +0.4 Vdc maximum
			NOTE All RF shield covers must be installed on UUT prior to performing the following steps.	
			NOTE Remember to account for IF offset in the following two steps. For frequencies less than 310 MHz, FO +30.1 MHz. For frequencies more than 310 MHz, FO -30.1 MHz. (FO=Frequency Offset).	
			NOTE dbc = decibels under carrier; i.e. as read on spectrum analyzer, reading is measurement of a harmonic with respect to carrier frequency amplitude.	

Table 5-13. Synthesizer CCA A1A1A6 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
12.			Verify Test Set S2 is in RECEIVE. Verify limits for the following VHF frequencies: 116, 132, 149 MHz.	
	Power meter	J3	Measure RF output power.	+ 7.0 dBm to + 12.0 dBm
	Spectrum Analyzer	J3	Measure 2nd harmonic.	≥ 15.0 dBc
		J3	Set reference level for fundamental frequency.	
		J2	Measure difference in RF output levels from J3 to J2.	≥ 20.0 dBc
13.		UUT	Verify indicated limits for following frequencies in UHF band: 225, 300, 399 MHz.	
	Power meter	J3	Measure RF output power.	+ 9.0 dBm to + 13.0 dBm
	Spectrum Analyzer	J3	Measure 2nd harmonic.	≥ 15.0 dBc
		J3	Set reference level for fundamental frequency.	
		J2	Measure difference in RF output levels from J3 to J2.	≥ 20.0 dBc
14.	Test set		Set test set S2 to XMIT. Verify indicated limits for following frequencies in VHF band: 116, 132, and 149 MHz.	CR9 lighted
	Power meter	J3	Measure RF output power.	+ 8.0 dBm to + 12.0 dBm
	Spectrum Analyzer	J3	Measure 2nd harmonic.	≥ 15.0 dBc
		J3	Set reference level for fundamental frequency.	

Table 5-13. Synthesizer CCA A1A1A6 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
		J2	Measure difference in RF output levels from J2 to J3.	≥ 20.0 dBc
	Modulation meter	J2	Measure Incidental Frequency Modulation (IFM).	≤ 700 Hz (in 300 to 3500 Hz bandwidth)
15.			Verify indicated limits for following frequencies in UHF band: 225, 300, 399 MHz.	
	Power meter	J2	Measure RF output power.	+ 9.0 dBm to + 13.0 dBm
	Spectrum Analyzer	J2	Measure 2nd harmonic.	≥ 15.0 dBc
		J2	Set reference level for fundamental frequency.	
		J3	Measure difference in RF output levels from J3 to J2.	≥ 20.0 dBc
	Modulation meter	J2	Measure Incidental Frequency Modulation (IFM).	≤ 700 Hz (in a 300 to 3500 Hz bandwidth)
16.	Frequency counter	UUT J2	Set test set to 399.975 MHz and verify output frequency.	399.975 MHz ± 200 Hz
17.	Connect equipment as shown in figure 5-13 sheet 2.		Set spectrum analyzer bandwidth to 3 kHz and scan width to 0. Set oscilloscope sweep rate to 2ms/division.	
18.	Test Set		Load 225.000 MHz in preset channel 1 and 399.975 MHz in preset channel 2.	

Table 5-13. Synthesizer CCA A1A1A6 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
19.	Spectrum analyzer		Set test set S2 to TRANSMIT and preset channel 1, tune spectrum analyzer to 225 MHz and maximum vertical deflection.	
20.	Test Set		Select preset channel 2. **NOTE** The following steps may require several attempts to view the settling time on the scope.	
21.	Oscilloscope	Test set J4	Change from preset channel 2 to 1 and measure settling time for 225 MHz.	$\leq$ 7.5 ms
22.			Tune spectrum analyzer to 399.975 MHz and maximum vertical deflection. Select preset channel 1.	
23.	Oscilloscope	Test set	Change from preset channel 1 to 2 and measure settling time for 399.975 MHz.	$\leq$ 7.5 ms
22.	End of test. Deenergize and remove test set and test equipment from UUT.			

Table 5-14. Synthesizer CCA A1A1A6 Alignment Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
1.			Set Synthesizer Test Set controls as follows: S1 to OFF S2 to RECEIVE	
2.	Connect equipment as shown in Figure 5-13. For negative voltages, connect red terminal to (+) and black to (-). Test set inverts polarity internally. Do not use ground jumper from (-) terminal to ground on to ground on power supply.		Adjust input power supplies to indicated levels.	
3.			Set test set S1 to ON.	
4.	DMM	TP4 (cathode of CR28)	Select following values for R145 and measure voltage at TP4.	
			Value selected 6.04K ohms 5.36K ohms 4.64K ohms 4.12K ohms	Voltage at TP4 6.35 to 6.51 Vdc 6.20 to 6.35 Vdc 6.05 to 6.20 Vdc 5.97 to 6.05 Vdc
5.	DMM	Test set TP12	Select value for R130 so that voltage measured is same as listed.	+5.10 ± 0.05 Vdc
6.	DMM	Test set TP13	Select value for R136 so that voltage measured is same as listed.	+5.10 ± 0.05 Vdc
7.	DMM	Test set TP11	Select value for R129 so that voltage measured is same as listed.	-8.00 ± 0.015 Vdc

Table 5-14. Synthesizer CCA A1A1A6 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
8.	DMM	Test set TP12	Select value for R130 so that voltage measured is same as listed.	+5.10 ± 0.05 Vdc
9.	DMM	Q6 (top of C25)	Measure voltage, select new value for R108.	+0.23 and +0.28 Vdc
			VCO End-Point Tune Voltages	
10.	DMM	UUT TP3	Set test set S2 to TRANSMIT. Tune test set to 225.000 MHz. Adjust L5 and measure voltage.	2.1 ± 0.1 Vdc
11.	DMM	UUT TP3	Tune UUT to 399.975 MHz and measure voltage. Adjust L5 if necessary and repeat step 7.	20.0 ± 1.0 Vdc
			RF Alignment, VCO Buffer	
12.	Oscilloscope	Q3 (UUT E4)	With test set S2 in TRANSMIT, adjust T1, T2, C30 and C31 to track buffer amplifier Q3 to the VCO across frequency range of 225.000 to 399.975 MHz.	Maximize RF output.
			RF Alignment, VHF Divide-by-Two-Tracking	
13.	Oscilloscope	R106	Temporarily install part number RCR05G101JS to mounting holes of R106. With test set S2 in TRANSMIT, adjust C24 and T3 to maximize RF output across frequency range of 116.000 to 149.975 MHz.	

Table 5-14. Synthesizer CCA A1A1A6 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			NOTE C24 affects higher frequencies, T3 affects lower frequencies.	
			Output Buffer	
14.	Oscilloscope	L13	Tune UUT to 230 MHz TRANSMIT, adjust L13 for minimum second harmonic output (460 MHz). Adjust L11 and L12 to maximize RF output across frequency range of 116 to 399.975 MHz.	
15.			**NOTE** L11 affects lower frequencies, L12 affects higher frequencies.	
16.			Output Power Level With test set S2 in TRANSMIT, select value for R112 so that minimum RF output power across frequency range of 225 to 399.975 MHz is greater than +10 dBm. **NOTE** Worst case will usually be at 399.975 MHz.	

Table 5-14. Synthesizer CCA A1A1A6 Alignment Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
17.			Select value for R106 so that minimum RF output power across frequency range of 116 to 149.975 MHz is greater than +9 dBm. **NOTE** Worst case will usually be at 149.975 MHz. **NOTE** Setting RF output too high will cause excessive harmonic levels at lower band edges.	
18.			Select value for R69 so that IFM peaks will not be greater that 600 Hz and so that minimum will not be lower than 300 Hz.	
19.	End of test. Deenergize and remove test set and test equipment from UUT.			

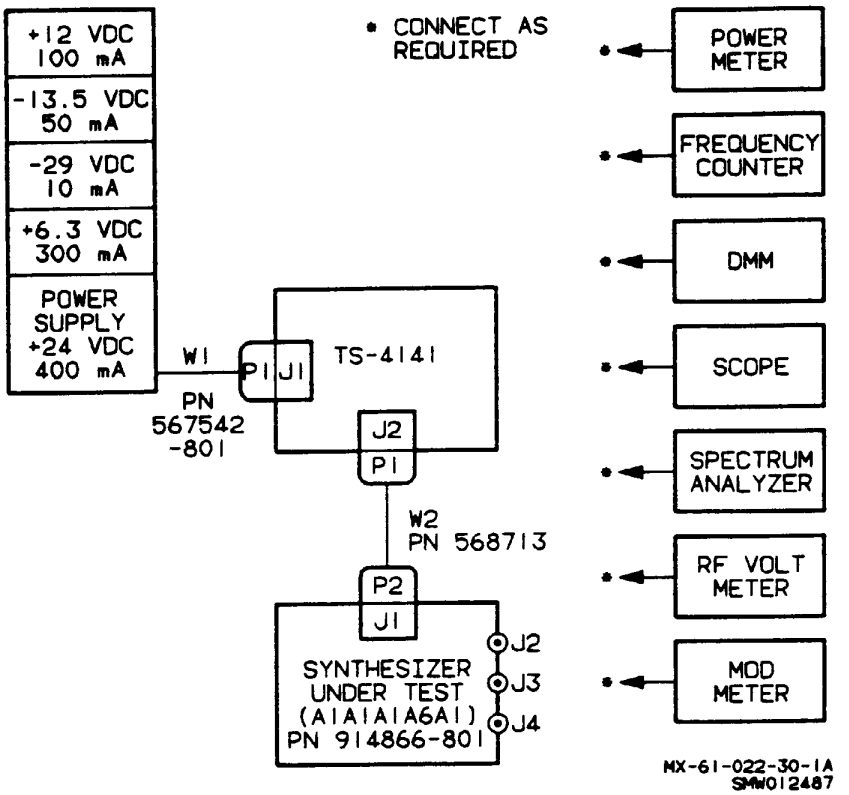


Figure 5-13. Synthesizer Assembly A1A1A6A1 Performance Test Connection Diagram (Sheet 1 of 2)

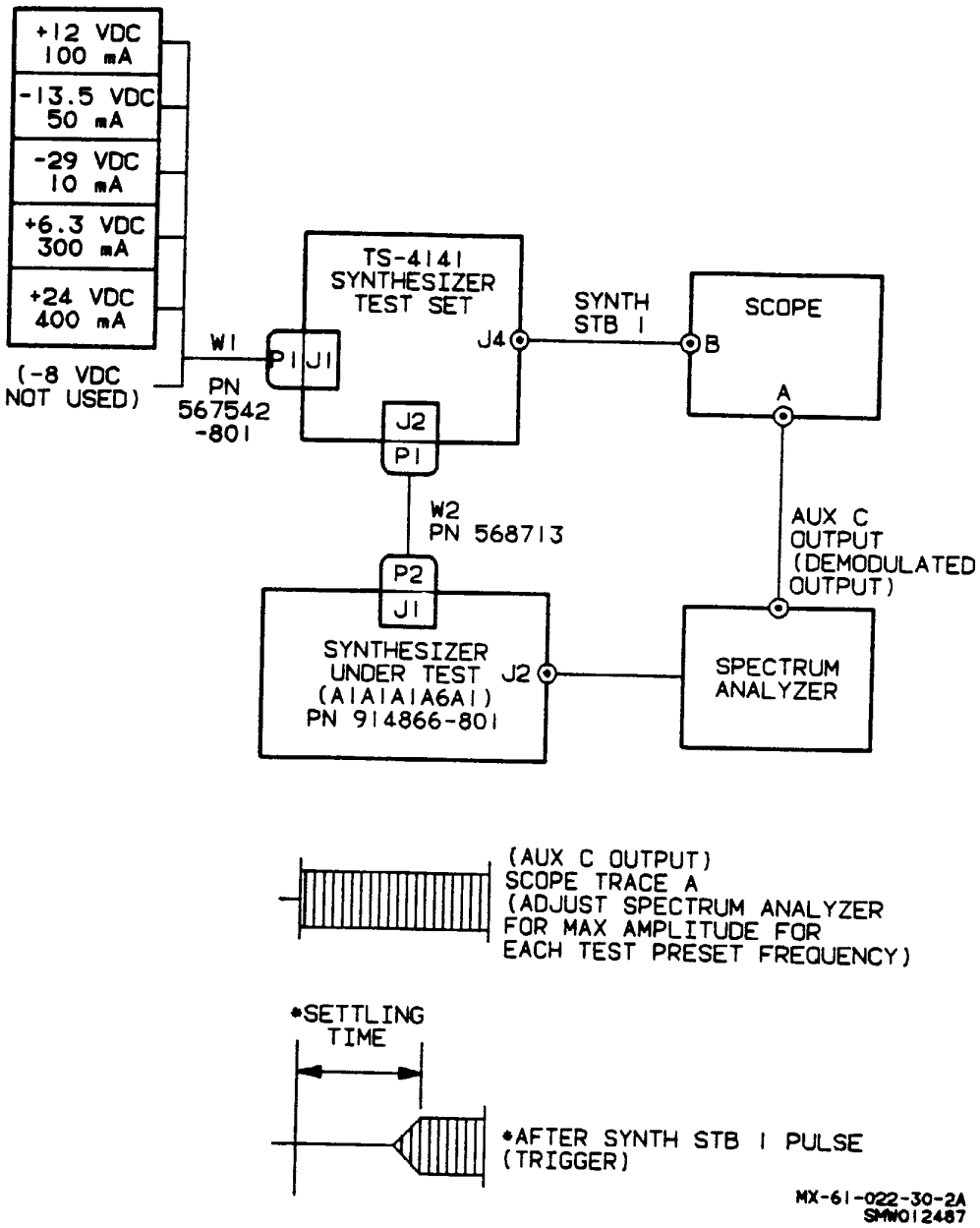
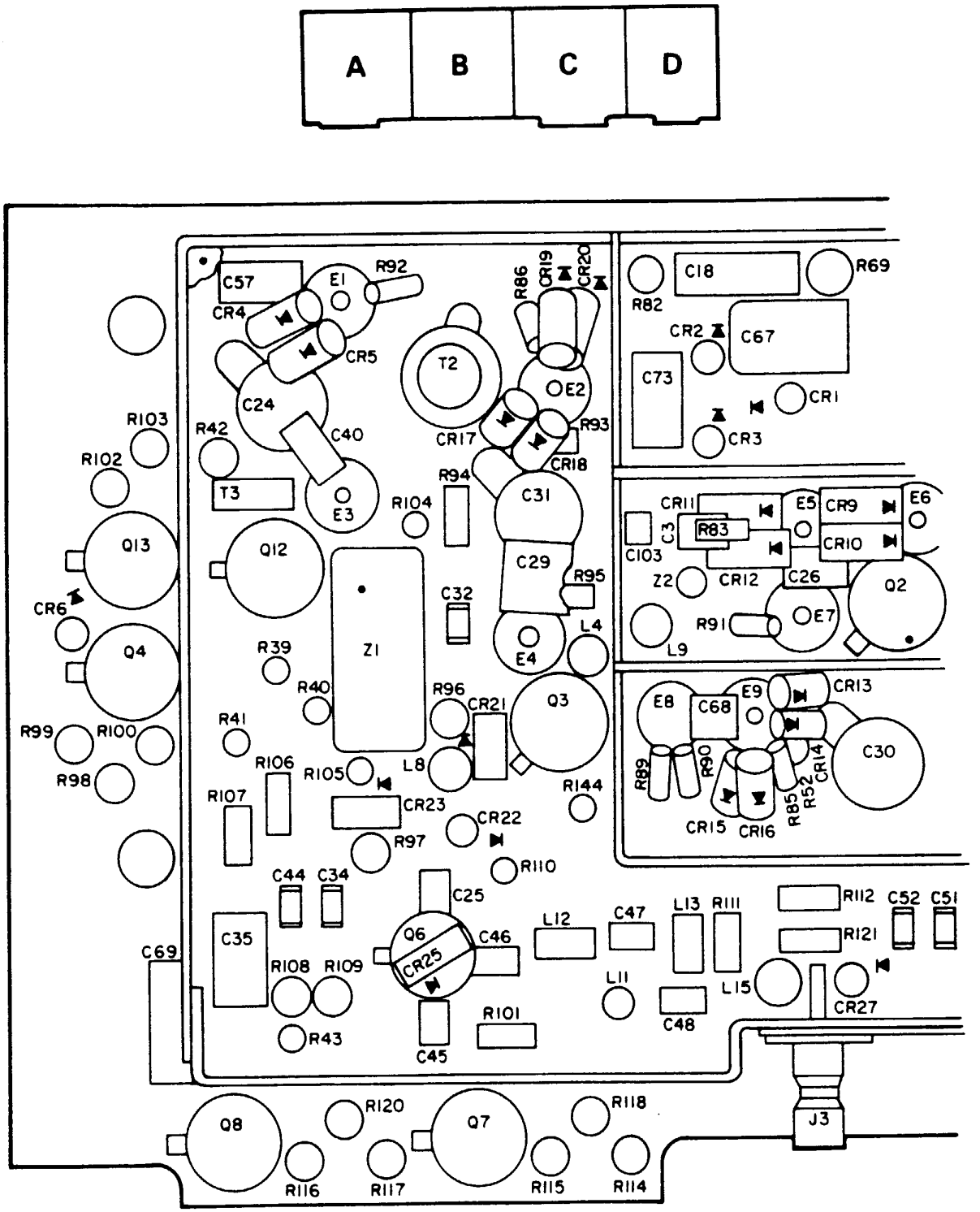


Figure 5-13. Synthesizer Assembly A1A1A6A1 Performance Test Connection Diagram (Sheet 2 of 2)



REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX WITH A1A1A1A6A1

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REF MX-61-022-IPB-9-1A

Figure 5-14. Synthesizer Assembly A1A1A6A1 Component and Test Point Location Diagram (Sheet 1 of 4)

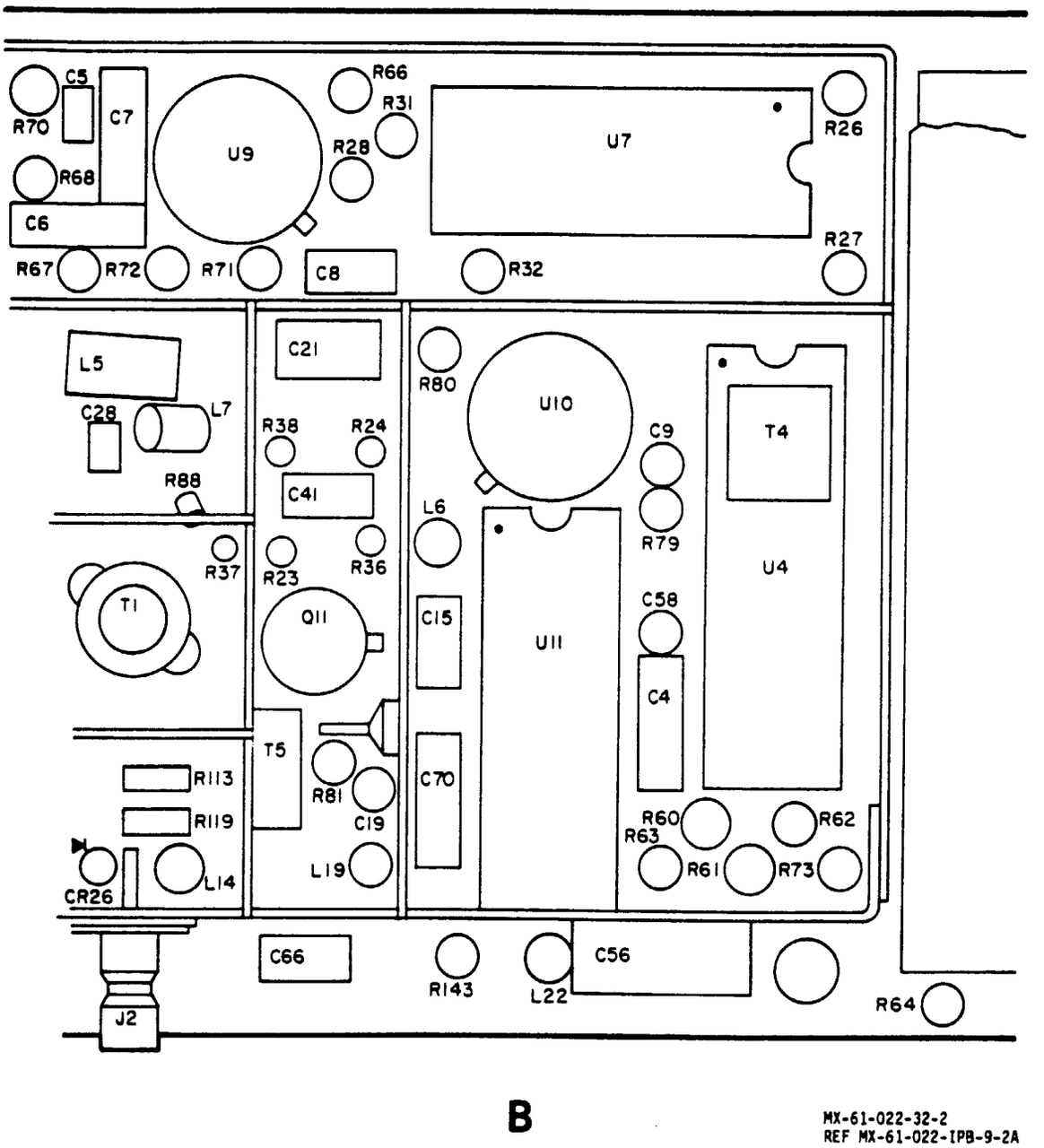
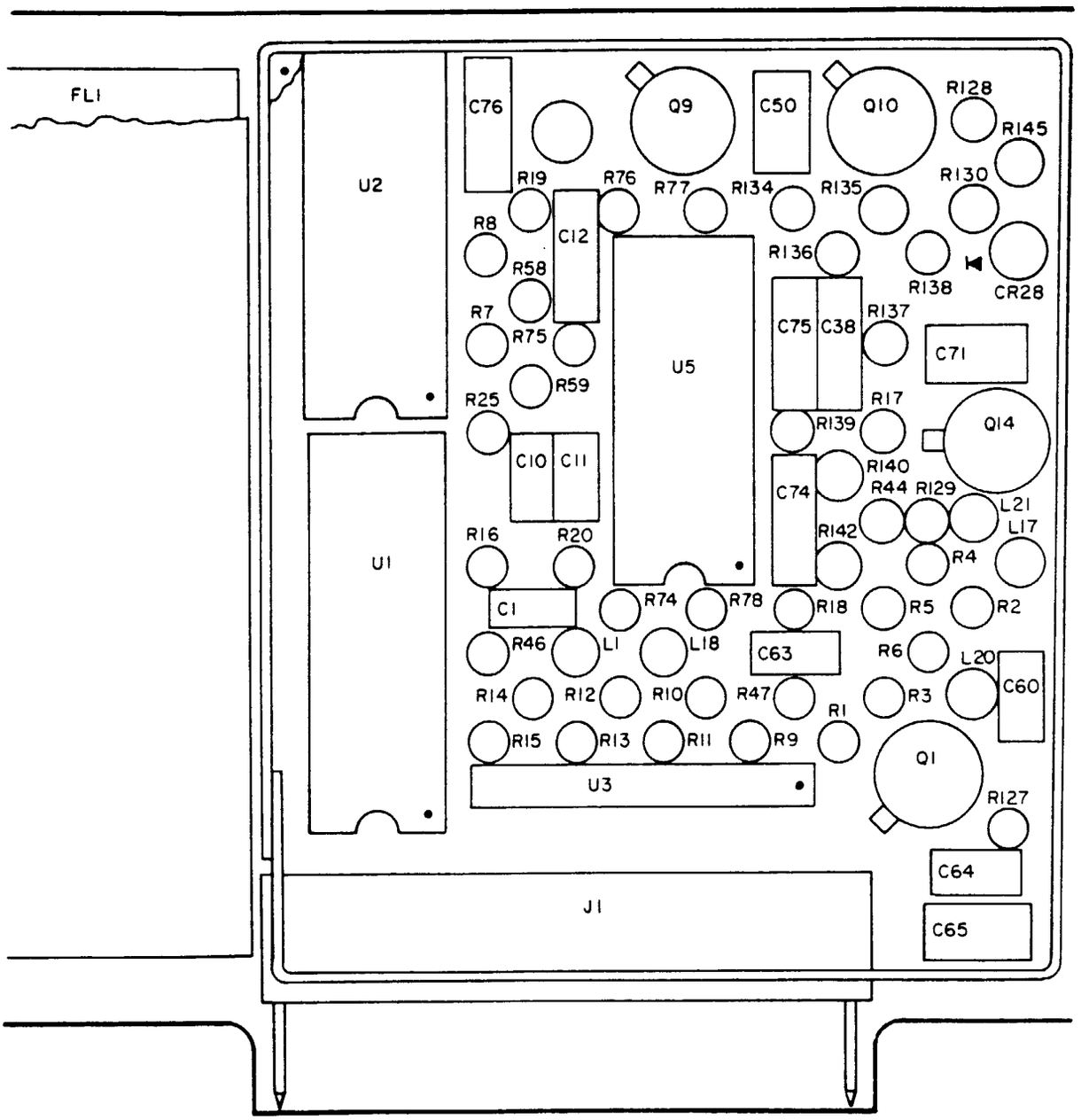


Figure 5-14. Synthesizer Assembly A1A1A6A1 Component and Test Point Location Diagram (Sheet 2 of 4)



C

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REF MX-61-022-IPB-9-3A

Figure 5-14. Synthesizer Assembly A1A1A6A1 Component and Test Point Location Diagram (Sheet 3 of 4)

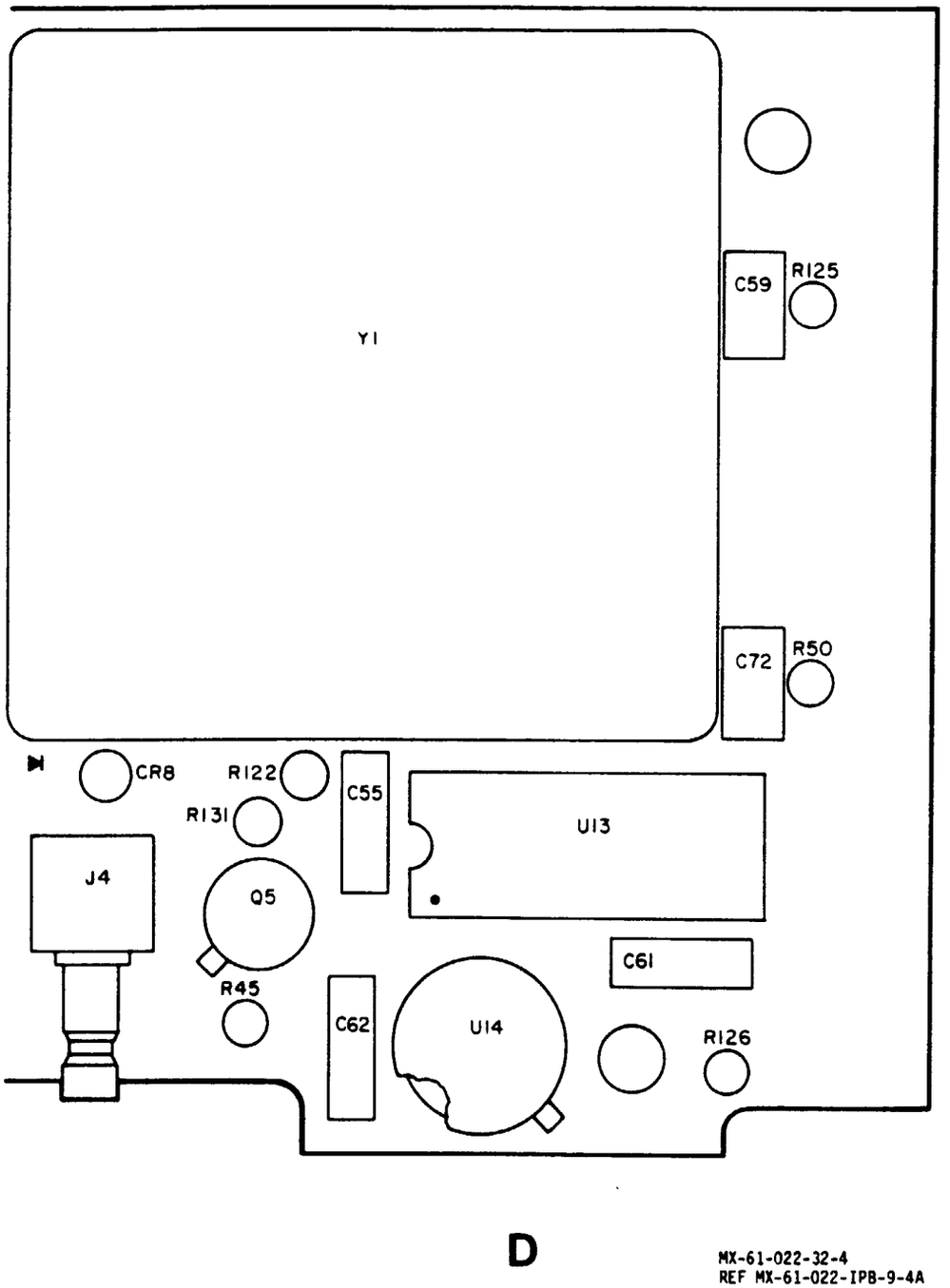


Figure 5-14. Synthesizer Assembly A1A1A6A1 Component and Test Point Location Diagram (Sheet 4 of 4)

Table 5-15. Power Regulator CCA A1A1A7 Performance Test Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
1.			Set test set controls as follows: PWR-CB1 to off (down position) PRC-113 section LOAD S22 - MIN	(See figure 5-25 for trouble analysis.)
2.	Connect equipment as shown on Figure 5-16.		Turn power supply on and adjust for minimum voltage. Set test set PWR CB1 to ON. Regulation	
3.	Ammeter		Increase power supply voltage to + 18 Vdc. Observe input current.	≤ 0.050 Amps
4.	Digital multimeter	Test POS TP / Set NEG TP	Measure UUT output voltages.	
		32 34		+6.0 to +6.8 Vdc
		33 34		+11.6 to +12.4 Vdc
		35 34		-10.0 to -13.9 Vdc
		36 34		-25 to -32 Vdc
5.	Ammeter		Set LOAD S22 to HIGH. Observe input current.	≤ 0.475 Amps
6.	Digital multimeter	Test POS / Set NEG	Measure UUT output voltages.	
		32 34		+6.1 to +6.5 Vdc
		33 34		+11.6 to +12.4 Vdc
		35 34		-8.0 to -13.9 Vdc
		36 34		-27.0 to -31.0 Vdc
7.	Ammeter		Set LOAD S22 to LOW Observe input current.	≤ 0.225 Amps

Table 5-15. Power Regulator CCA A1A1A7 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
8.	Digital multimeter	Test Set POS NEG 32 34 33 34 35 34 36 34	Measure UUT output voltages.	 +6.1 to +6.5 Vdc +11.6 to +12.4 Vdc -10.0 to -13.9 Vdc -27 to -31 Vdc
9.	Ammeter		Increase power supply voltage to + 30 Vdc. Observe input current.	≤ 0.150 Amps
10.	Digital multimeter	Test Set POS NEG 32 34 33 34 35 34 36 34	Measure UUT output voltages.	 +6.1 to +6.5 Vdc +11.6 to +12.4 Vdc -13.0 to -13.9 Vdc -27 to -31 Vdc
11.	Ammeter		Set LOAD S22 to HIGH. Observe input current.	≤ 0.280 Amps
12.	Digital multimeter	Test Set POS NEG 32 34 33 34 35 34 36 34	Measure UUT output voltages.	 +6.1 to +6.5 Vdc +11.6 to +12.4 Vdc -13.0 to -13.9 Vdc -27 to -31 Vdc
13.			Set LOAD S22 to MED.	
14.			Lower power supply voltage to +25Vdc.	
15.	Ammeter		Observe input current.	≤ 0.235 Amps

Table 5-15. Power Regulator CCA A1A1A7 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
16.	Digital multimeter, oscilloscope	Test POS TP / Set NEG TP 32 34 33 34 35 34 36 34	Measure UUT output voltages with DMM. Measure AC ripple with oscilloscope.	+6.1 to +6.5 Vdc 0.25 V p-p max +11.6 to +12.4 Vdc 0.15 V p-p max -13.0 to -13.9 Vdc 0.20 V p-p max -27 to -31 Vdc 0.50 V p-p max
			Short Circuit and Recovery	
17.	Ammeter		Set SHORT CIRCUIT 6.3VDC S23 to down position and release. Observe input current	≤ 0.250 Amps
18.	Digital multimeter	Test POS TP / Set NEG TP 32 34	Measure UUT output voltages.	+6.1 to +6.5 Vdc
19.	Ammeter		Set SHORT CIRCUIT 12VDC S24 to down position and release. Observe input current.	≤ 0.250 Amps
20.	Digital multimeter	Test POS TP / Set NEG TP 33 34	Measure UUT output voltages.	+11.6 to +12.4Vdc
21.	Ammeter		Set SHORT CIRCUIT -13.5VDC S25 to down position and release. Observe input current.	≤ 0.250 Amps

Table 5-15. Power Regulator CCA A1A1A7 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
22.	Digital multimeter	Test Set POS NEG TP TP 35 34	Measure UUT output voltages.	-13.0 to -13.9Vdc
23.	Ammeter		Set SHORT CIRCUIT -29VDC S26 to down position and release. Observe input current.	0.250 Amps maximum
24.	Digital multimeter	Test Set POS NEG TP TP 36 34	Measure UUT output voltages. Low Battery Indicator Voltage	-27 to -31 Vdc
25.	Digital multimeter	Test Set POS NEG TP TP 31 34	Set Power Supply voltage to +21.5 Vdc and measure LOW BAT output.	≥ +11 Vdc min
26.	Digital multimeter	Test Set POS NEG TP TP 31 34	Set Power Supply voltage to +18 Vdc and measure LOW BAT output.	≤ +1 Vdc max
27.	Test Set		Set LOAD switch S22 to MIN.	
28.			Set POWER-ON CB1 to off, (down position).	
29.	End of test. Deenergize and remove test set and test equipment from UUT.			

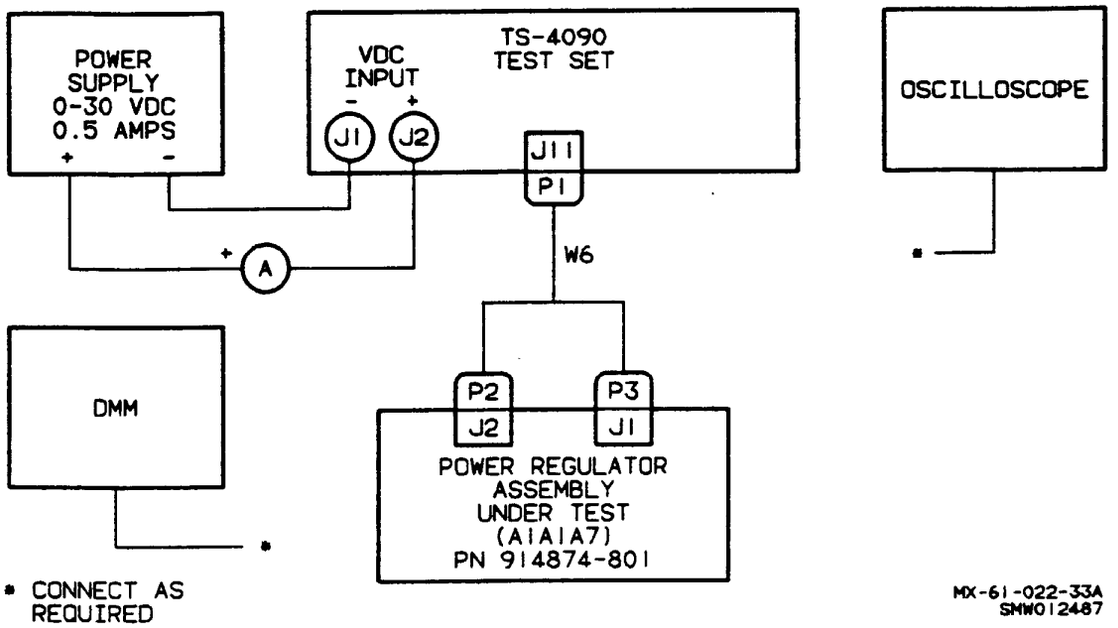


Figure 5-15. Power Regulator Assembly A1A1A7 Test Connection Diagram

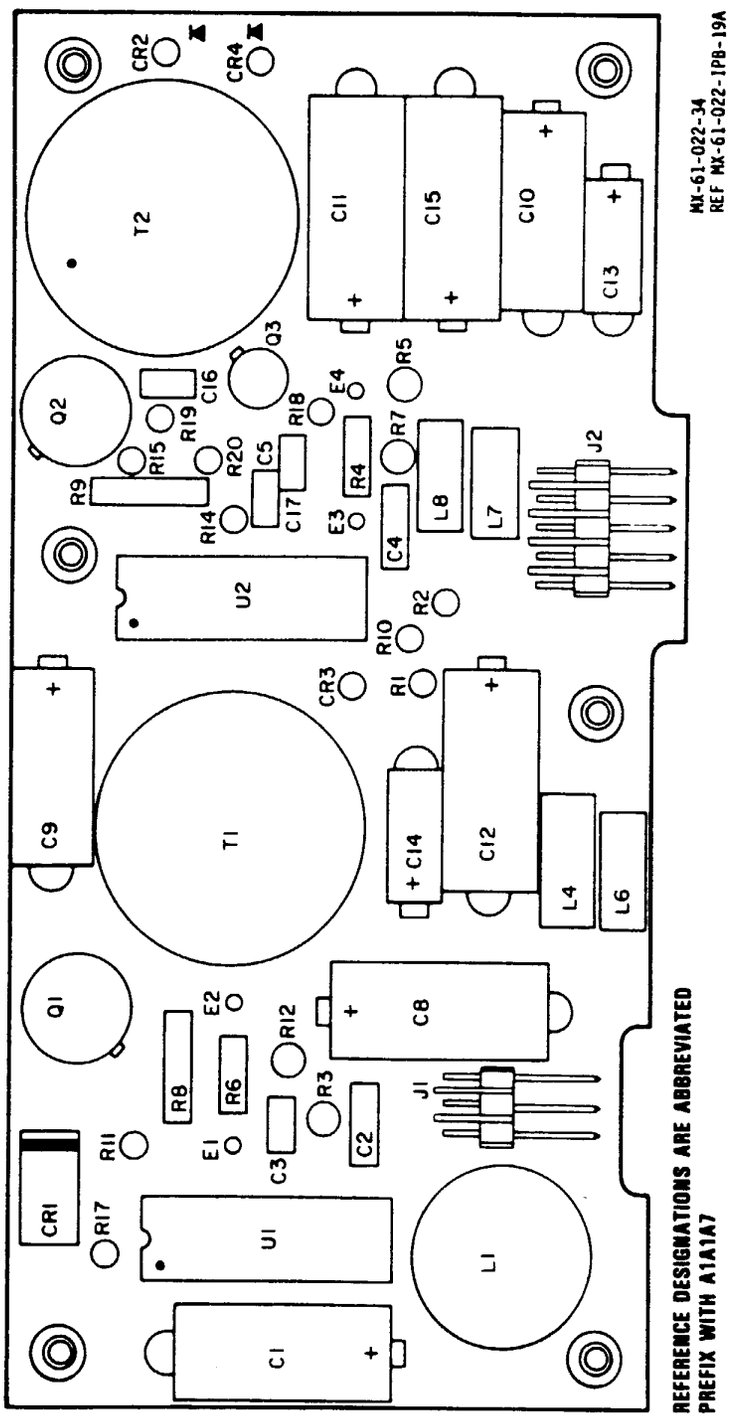


Figure 5-16. Power Regulator Assembly A1A1A7 Component and Test Point Location Diagram

Table 5-16. Chassis Assembly A1A1A8 Continuity Check

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
1.	DMM	UUT J2 / P7 24 13 1 9 8 8 19 7 18 15 7 6 23 10 13 16 14 18 15 11 20 5 34 3 35 1 36 2 37 4 30 17 6 12	Measure continuity between pins listed.	< 1 Ohm
2.	DMM	UUT J2 / J8 21 20 31 16 32 18 10 22 25 14 22 7 28 19	Measure continuity between pins listed.	< 1 Ohm
3.	DMM	UUT J8 / J3 21 B 23 F 10 D 12 A 11 E	Measure continuity between pins listed.	< 1 Ohm

Table 5-16. Chassis Assembly A1A1A8 Continuity Check-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
4.	DMM	UUT J10 J5 2 2 2 4 5 3 3 6	Measure continuity between pins listed.	< 1 Ohm
5.	DMM	UUT J10 J4 6 6 7 3 1 4 1 2	Measure continuity between pins listed.	< 1 Ohm
6.	DMM	UUT P9 J6 1 8 6 6 5 1	Measure continuity between pins listed.	< 1 Ohm
7.	DMM	UUT J2 J3 30 C	Measure continuity between pins listed.	< 1 Ohm
8.	DMM	UUT J2 J5 9 6	Measure continuity between pins listed.	< 1 Ohm
9.		UUT J2 P6 17 2 29 5 12 2	Measure continuity between pins listed.	< 1 Ohm

Table 5-16. Chassis Assembly A1A1A8 Continuity Check-Continued

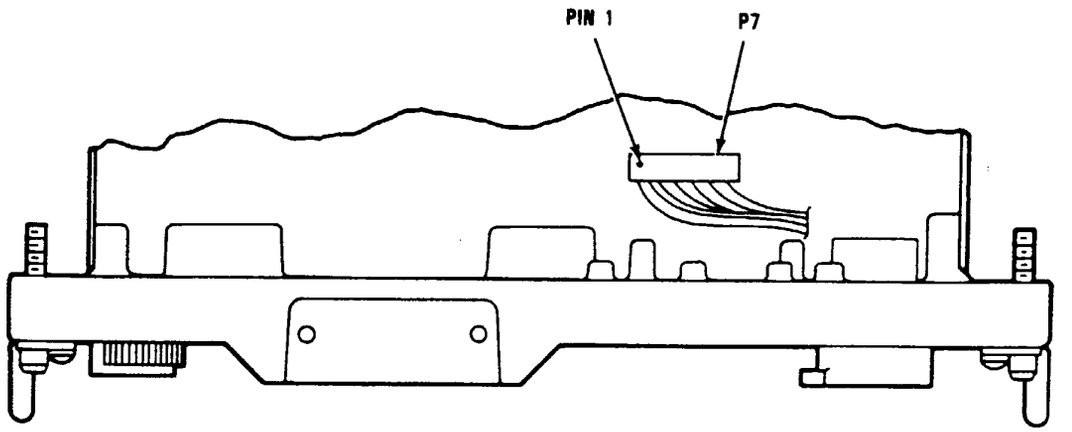
Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
10.	DMM	UUT J2 16 GND 26 GND 27 GND 33 GND 2 GND 11 GND	Measure continuity between pins listed.	< 1 Ohm
11.	DMM	UUT P9 6 GND 5 GND	Measure continuity between pins listed.	< 1 Ohm
12.	DMM	UUT J8 12 GND 17 GND 8 GND 6 GND	Measure continuity between pins listed.	< 1 Ohm
13.	DMM	UUT P6 J8 7 2	Measure continuity between pins listed.	< 1 Ohm
14.	DMM	UUT J5 P6 5 4 5 3	Measure continuity between pins listed.	< 1 Ohm
15.	DMM	UUT J4 P6 5 9 5 10	Measure continuity between pins listed.	< 1 Ohm
16.	DMM	UUT J4 1 GND	Measure continuity between pins listed.	< 1 Ohm

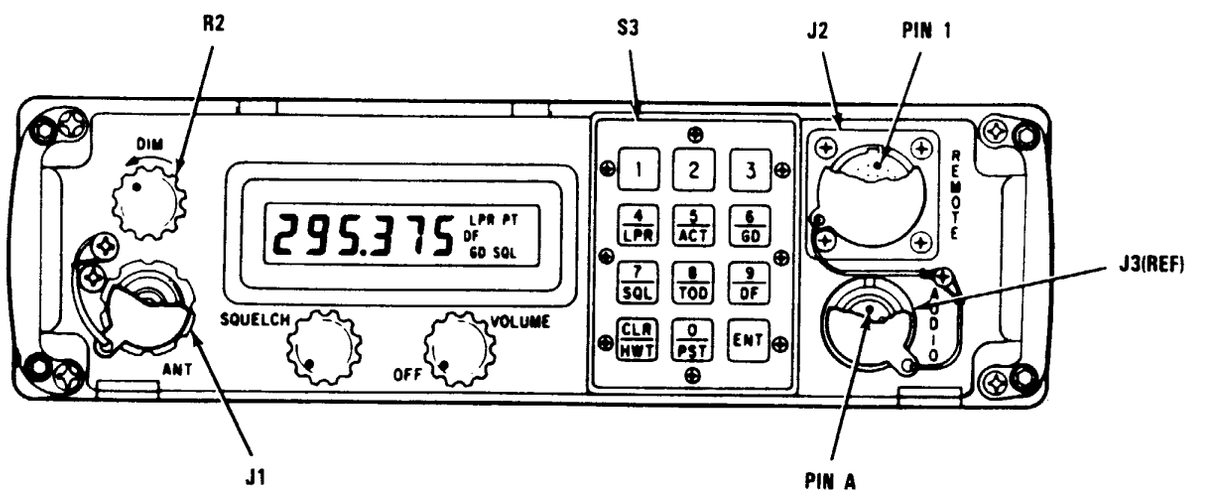
Table 5-16. Chassis Assembly A1A1A8 Continuity Check-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
17.	DMM	UUT J5 1 GND	Measure continuity between pins listed.	< 1 Ohm
18.	DMM	UUT J2 12 GND	With S2 set to OFF, check for no continuity.	> 20 MegOhm
19.	DMM	UUT P6 2 GND	With S2 set to OFF, check for no continuity.	> 20 MegOhm
20.	DMM	UUT J2 12 GND	With S2 set to ON, check continuity.	< 1 Ohm
21.	DMM	UUT P6 2 GND	With S2 set to ON, check continuity.	< 1 Ohm
22.	DMM	UUT J8 J8 24 15	Measure resistance of R3.	25k Ohms
23.	DMM	UUT J8 J8 9 15 9 24	Set R3 fully ccw, measure continuity at following points.	 < 1 Ohm 25 kOhms
24.	DMM	UUT J8 J8 1 4	Set R2 fully ccw, measure continuity at following points while varying R2 to full cw.	0 - 1 kOhms

Table 5-16. Chassis Assembly A1A1A8 Continuity Check-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
25.	DMM	UUT J8 P9 1 2	Set R2 fully ccw, measure continuity at following points.	< 1 Ohm
26.	DMM	UUT J8 5 GND	Set R1 fully ccw, measure continuity at following points while varying R1.	2000 Ohms
27.	DMM	UUT J8 J8 P1 1 2	Vary R1 from fully ccw to fully cw and measure continuity.	0-2 kOhms
28.	DMM	W1P1 W1J1	Measure continuity of W1 cable.	< 1 Ohm
29.	Test complete. Disconnect and normalize test equipment.			





REFERENCE DESIGNATIONS ARE ABBREVIATED.
PREFIX WITH A1A8.

MX-81-022-51-1
REF MX DWG 914880-801 REV P
PL 914880-801 REV AE

Figure 5-17. Chassis Assembly A1A1A8 Component and Test Point Location Diagram (Sheet 1 of 3)

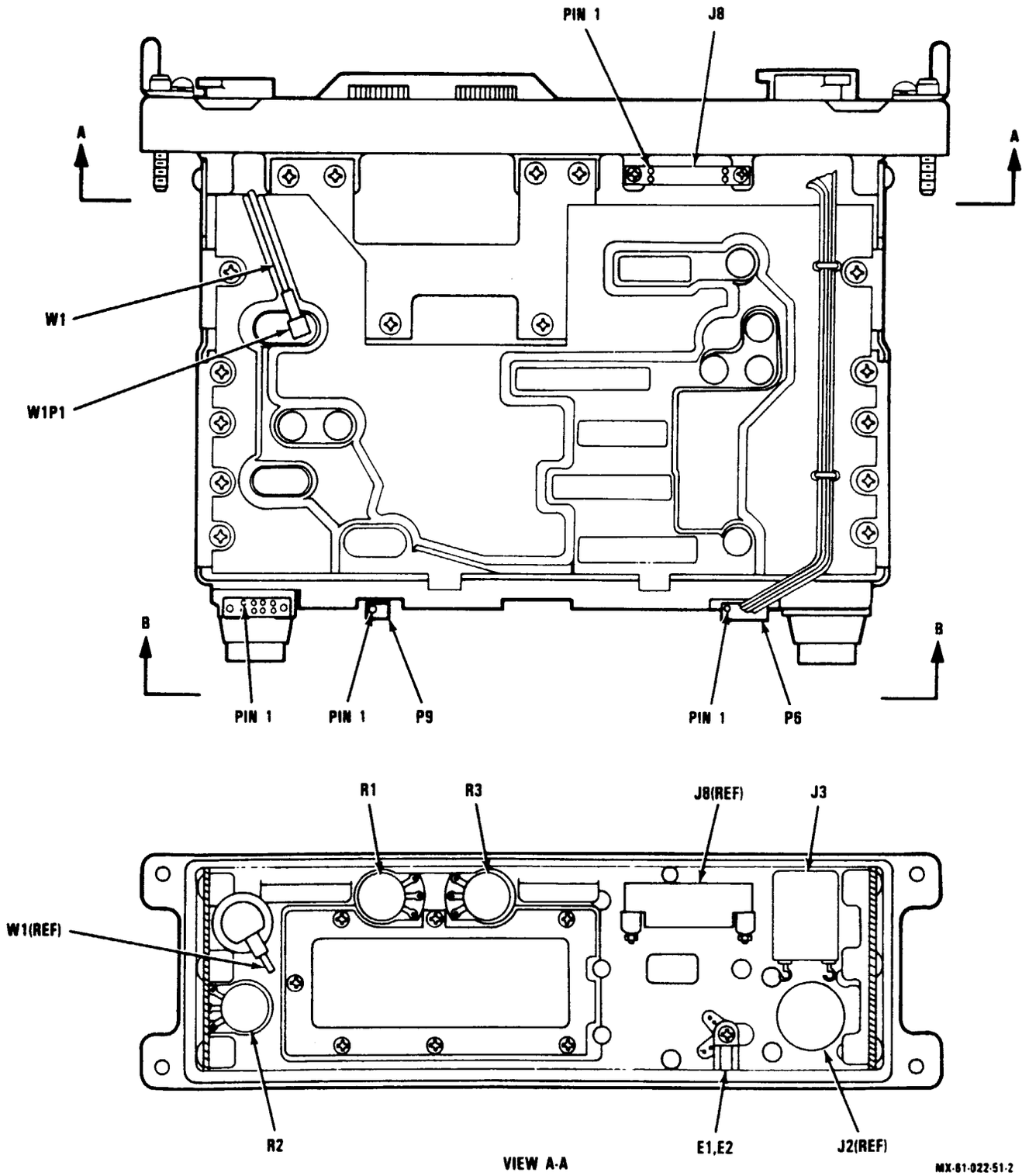


Figure 5-17. Chassis Assembly A1A1A8 Component and Test Point Location Diagram (Sheet 2 of 3)

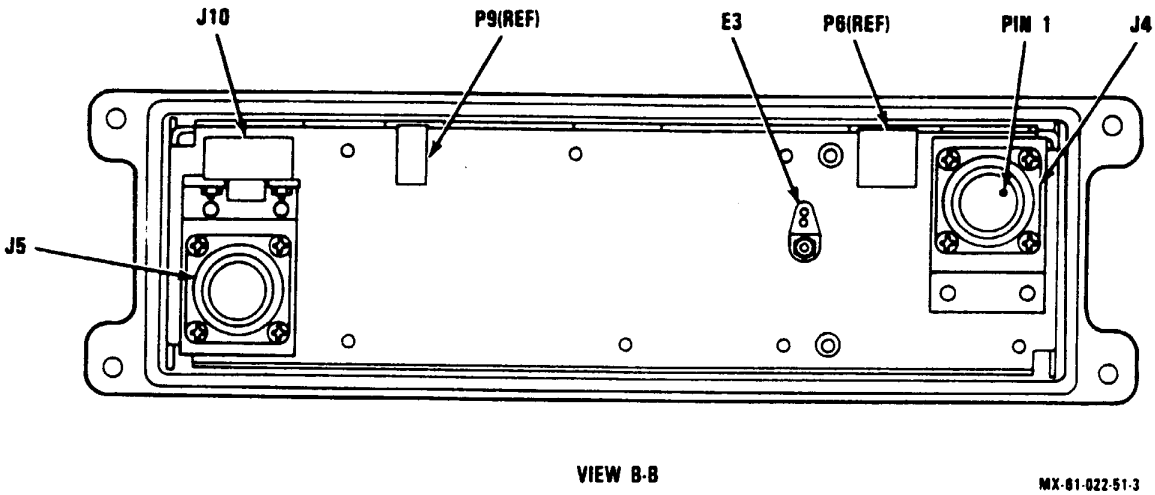


Figure 5-17. Chassis Assembly A1A1A8 Component and Test Point Location Diagram (Sheet 3 of 3)

Table 5-17. Power Switching CCA A1A1A9 Performance Test Procedure

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
1.			Make following adjustments to test set: S4 to OFF S5 to BATTERY 1, and S6 to LOW.	(See figure 526 for trouble analysis.)
2.	Connect equipment as shown in figure 5-19.		Set Power Supply to ON and adjust for 24 Vdc input.	
3.			Set Test Set S1 DC POWER switch to on.	CR5 and CR7 ON
			Battery 1 Test	
4.		Test Set TP13 GND TP9 POS TP12 POS	Alternately measure DC voltage.	< .05 Vdc
5.	DMM		Set S4 to ON.	CR6 ON
6.	DMM	Test Set TP13 GND TP9 POS TP12 POS	Alternately measure DC voltage.	≥ 23 Vdc
7.			Set S6 to HIGH and insure input power is still 24 Vdc.	
9.	DMM	Test Set TP13 GND TP9 POS TP12 POS	Alternately measure DC voltage.	≥ 22.75 Vdc

Table 5-17. Power Switching CCA A1A1A9 Performance Test Procedure-Continued

Step	Connection of test equipment	Point of test	Control settings and operation of equipment	Performance standards
			Battery 2 Test	
10.			Set S4 to OFF, S5 to BATTERY 2, and S6 to LOW.	CR6 OFF
11.		Test Set TP13 GND TP9 POS TP12 POS	Alternately measure DC voltage.	< .05 Vdc
12.			Set S4 to ON.	CR6 ON
13.	DMM	Test Set TP13 GND TP9 POS TP12 POS	Alternately measure DC voltage.	≥ 23 Vdc
14.			Set S6 to HIGH and insure input power is still 24 Vdc.	
15.	DMM	Test Set TP13 GND TP9 POS TP12 POS	Alternately measure DC voltage.	≥ 23 Vdc
16.	End of test. Deenergize and remove test set and test equipment from UUT.			

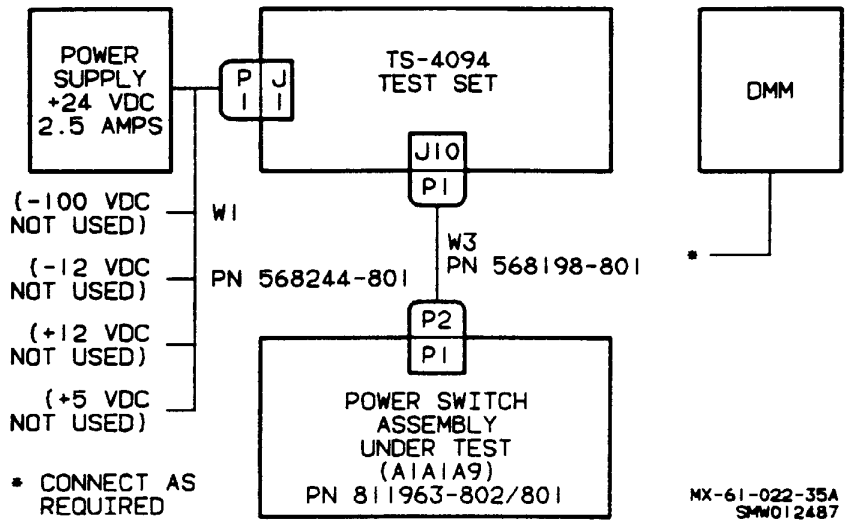


Figure 5-18. Power Switching CCA A1A1A9 Performance Test Connection Diagram

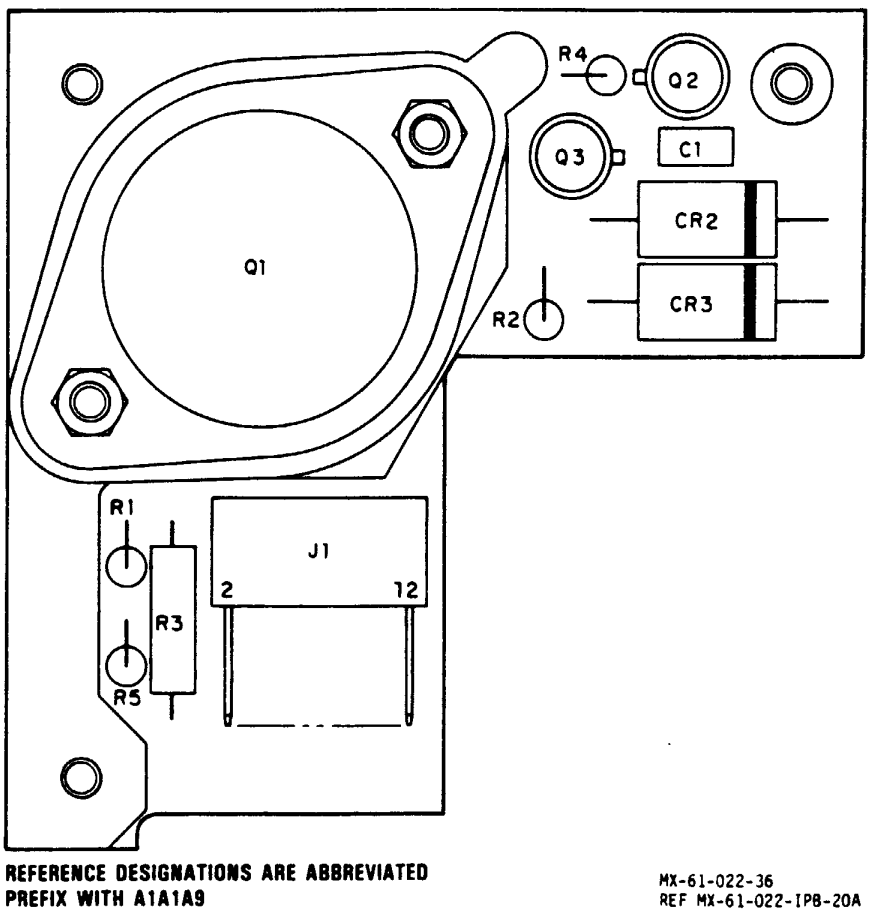
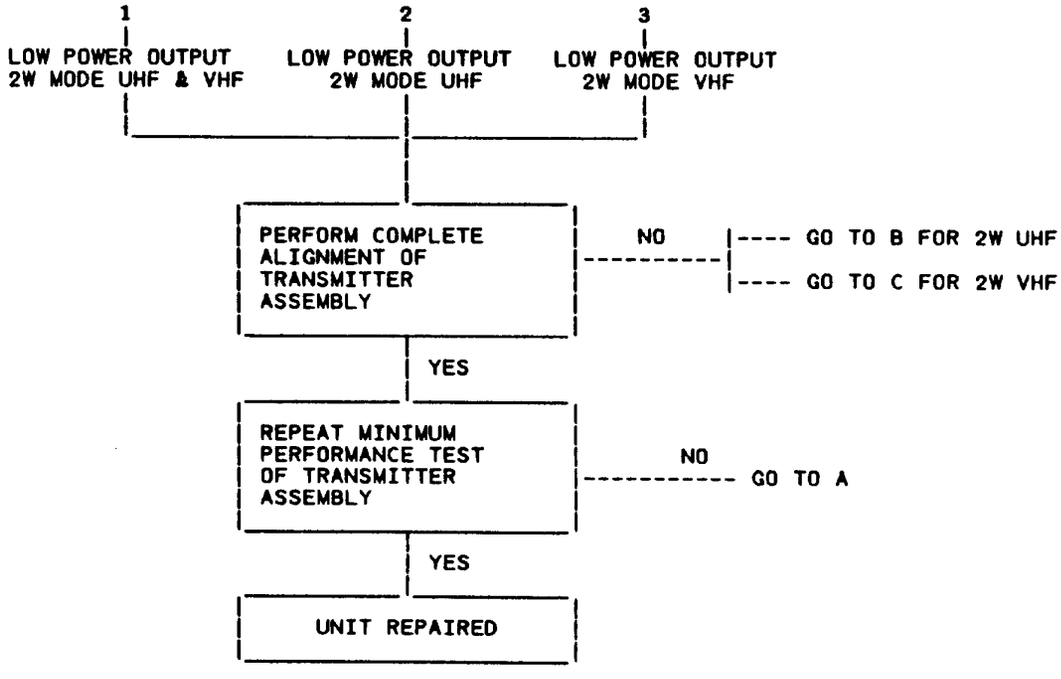
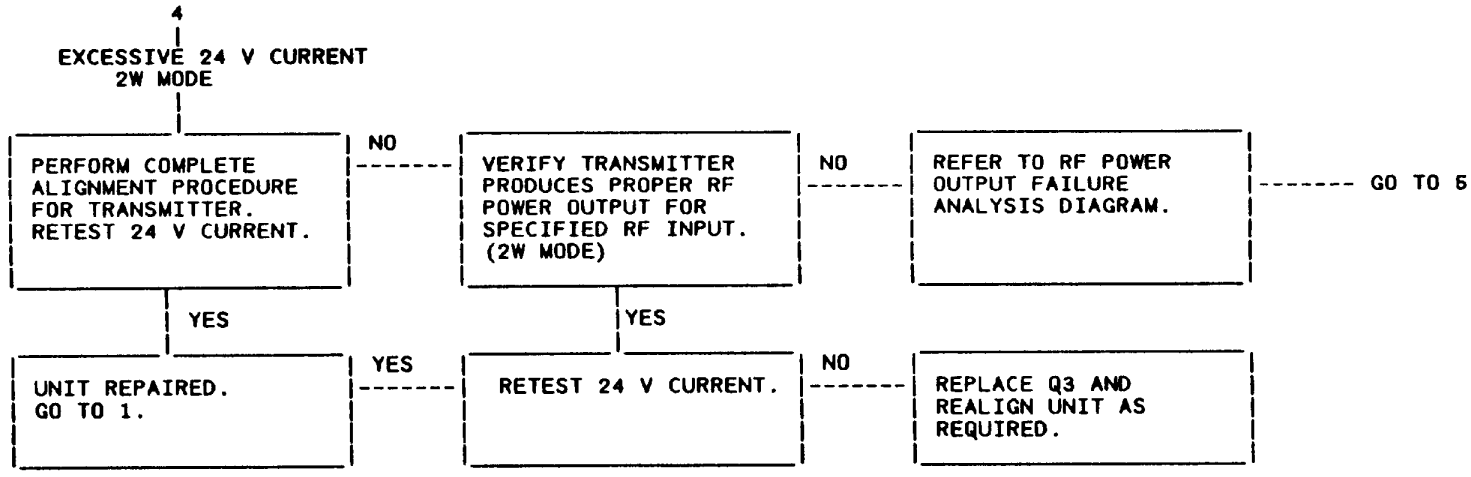


Figure 5-19. Power Switching CCA A1A1A9 Component and Test Point Location Diagram



VAX-MX-81-022-82-1

Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram
(Sheet 1 of 11)



NOTES: 1. All DC VOLTAGES ARE TO BE +/- 10% UNLESS OTHERWISE SPECIFIED.

2. All TESTS ARE PERFORMED WITH UUT IN THE TRANSMIT MODE UNLESS OTHERWISE SPECIFIED.

VAX-MX-81-022-52-2

Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram
(Sheet 2 of 11)

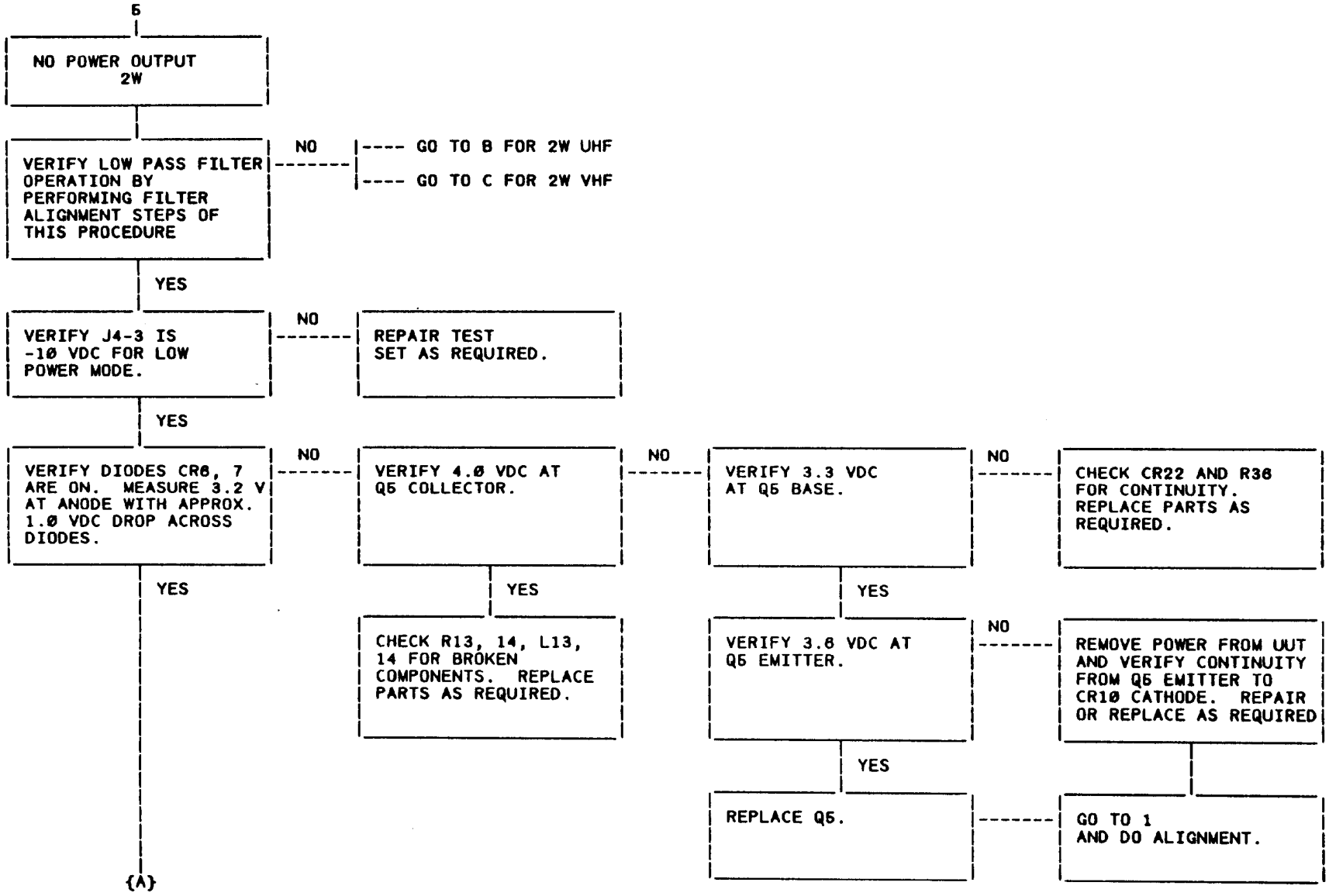
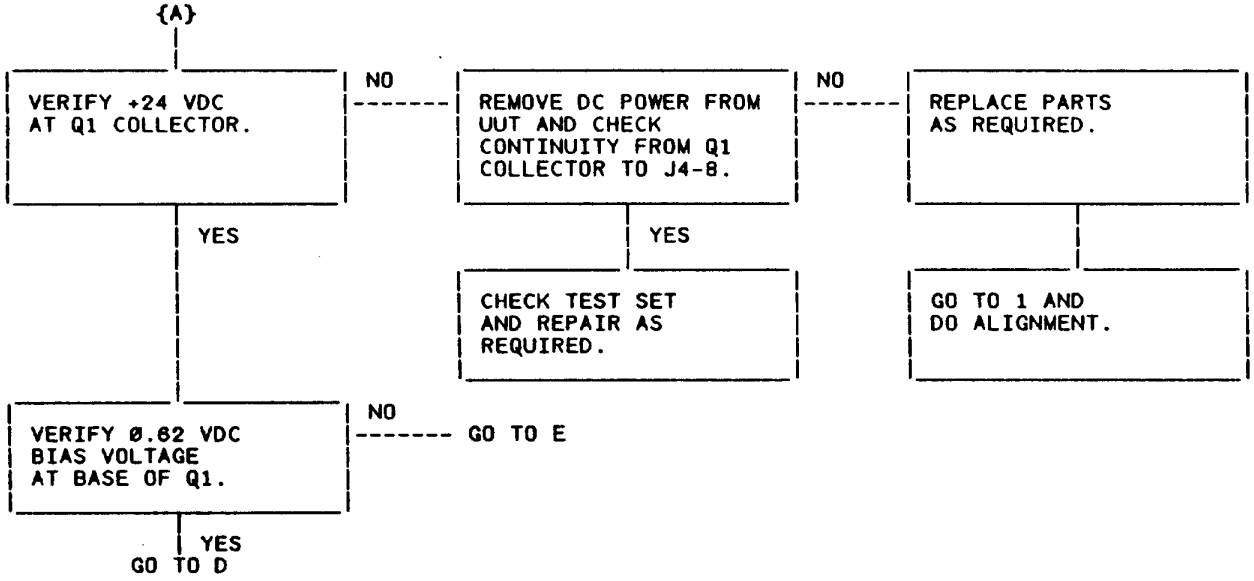
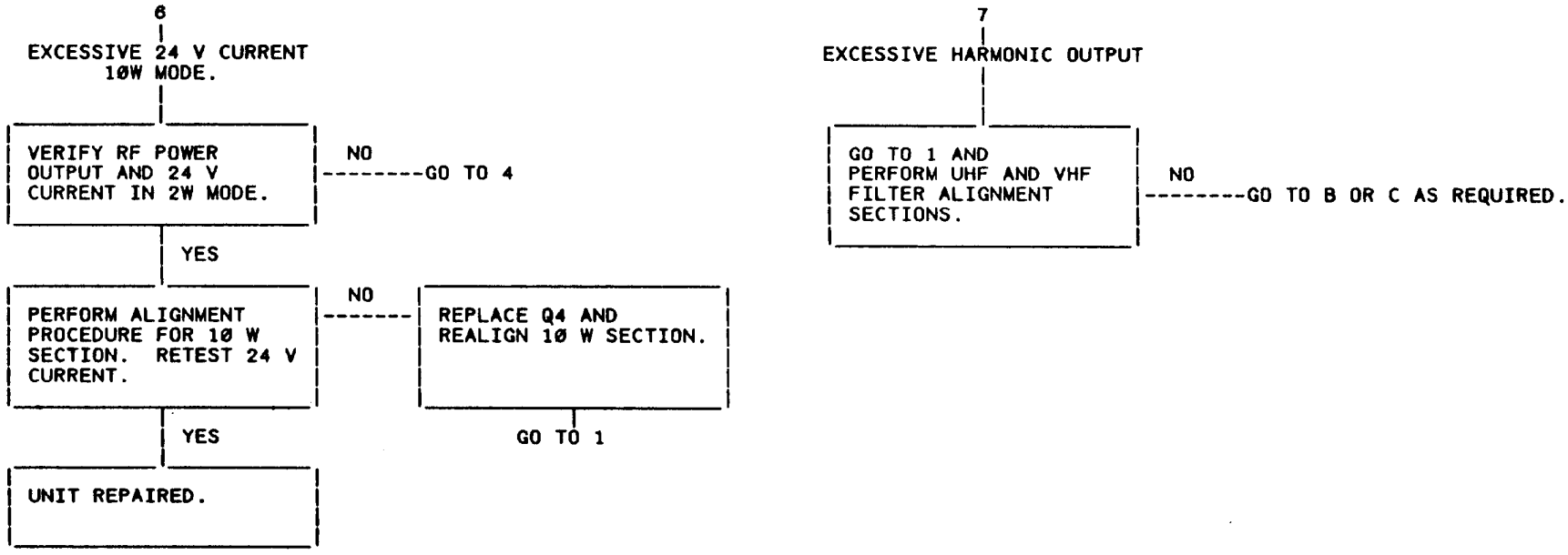


Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram
(Sheet 3 of 11)



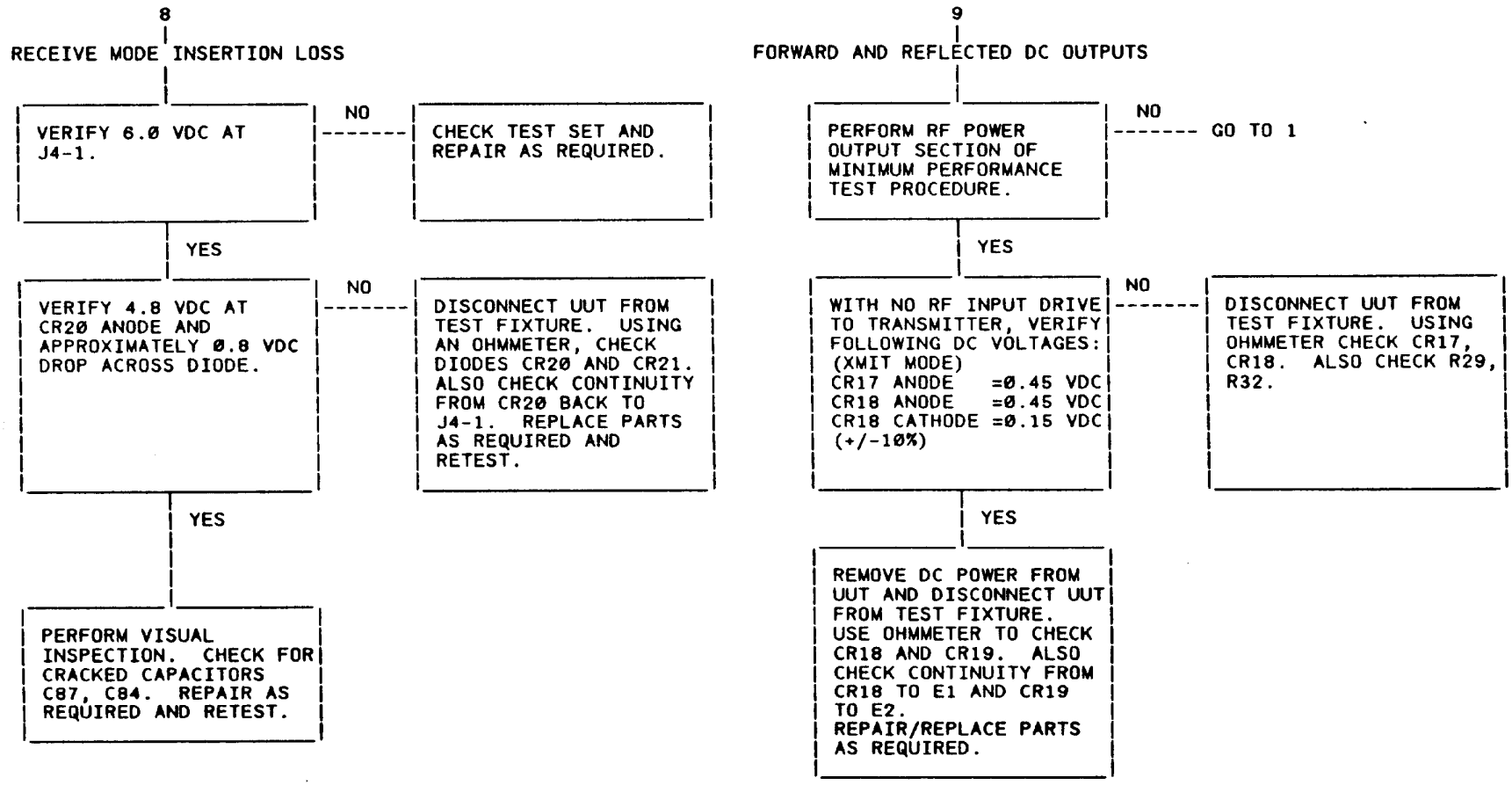
VAX-MX-81-022-52-4

Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram
(Sheet 4 of 11)



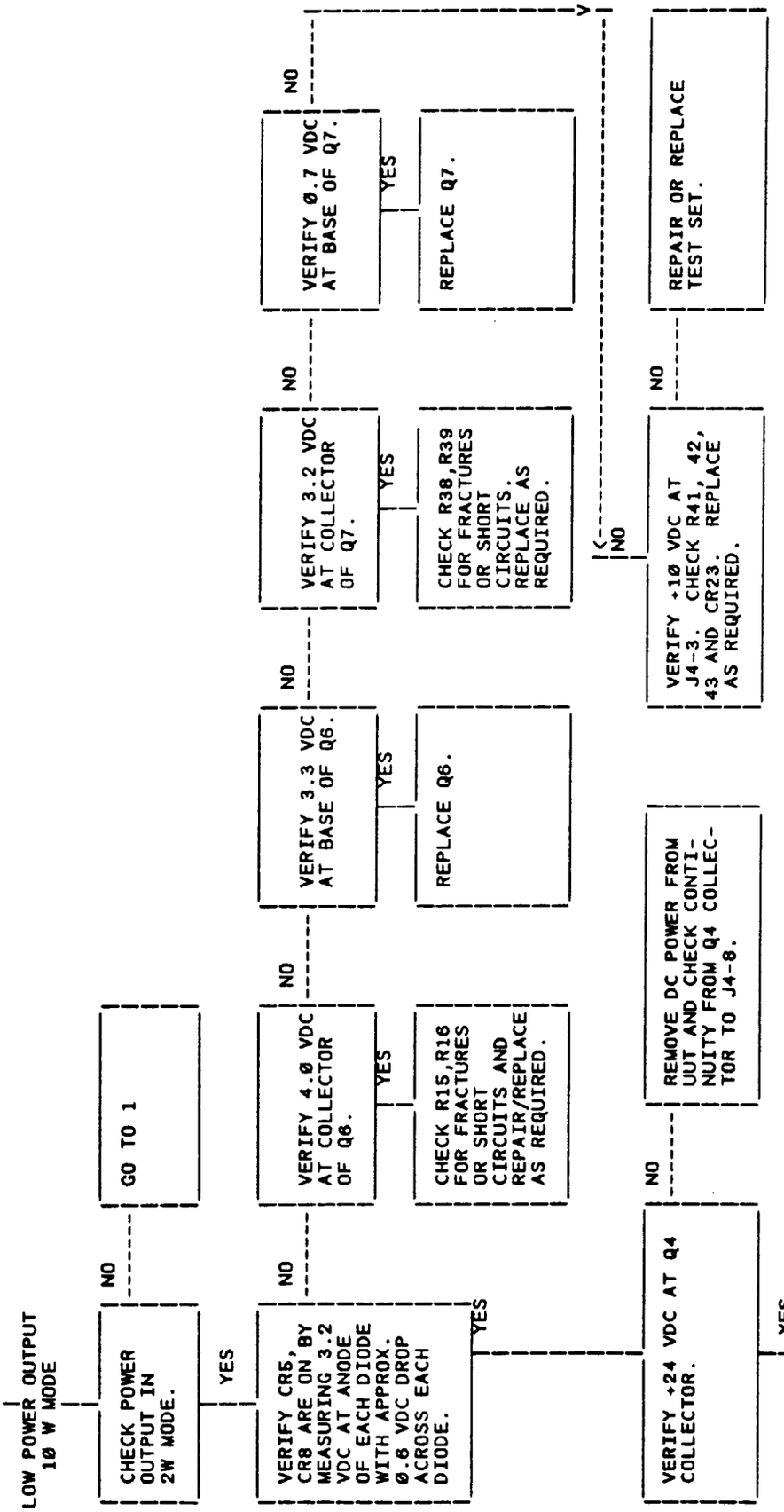
VAX-MX-61-022-52-5

Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram
(Sheet 5 of 11)



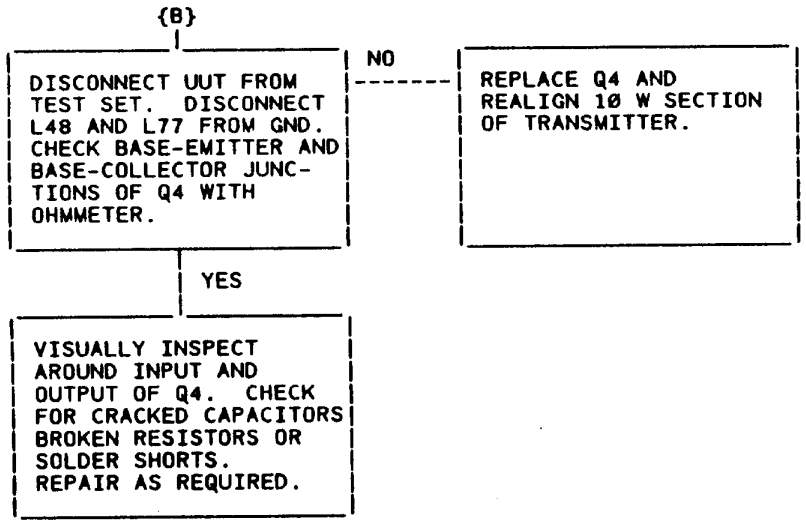
VAX-MX-81-022-52-8

Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram
(Sheet 6 of 11)



VAX-MX-81-022-52-7

Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram
(Sheet 7 of 11)



VAX-MX-81-022-52-8

Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram
(Sheet 8 of 11)

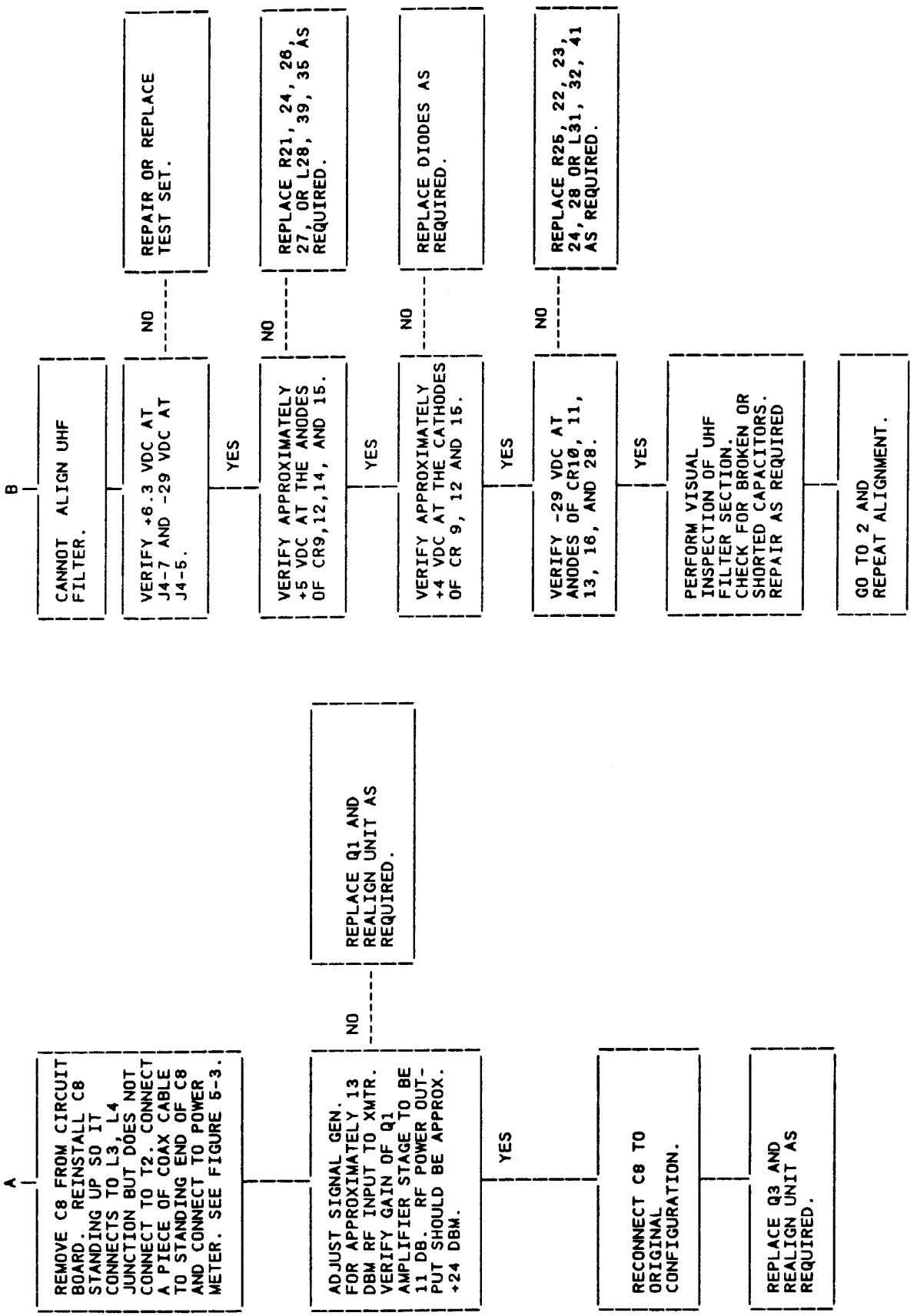


Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram (Sheet 9 of 11)

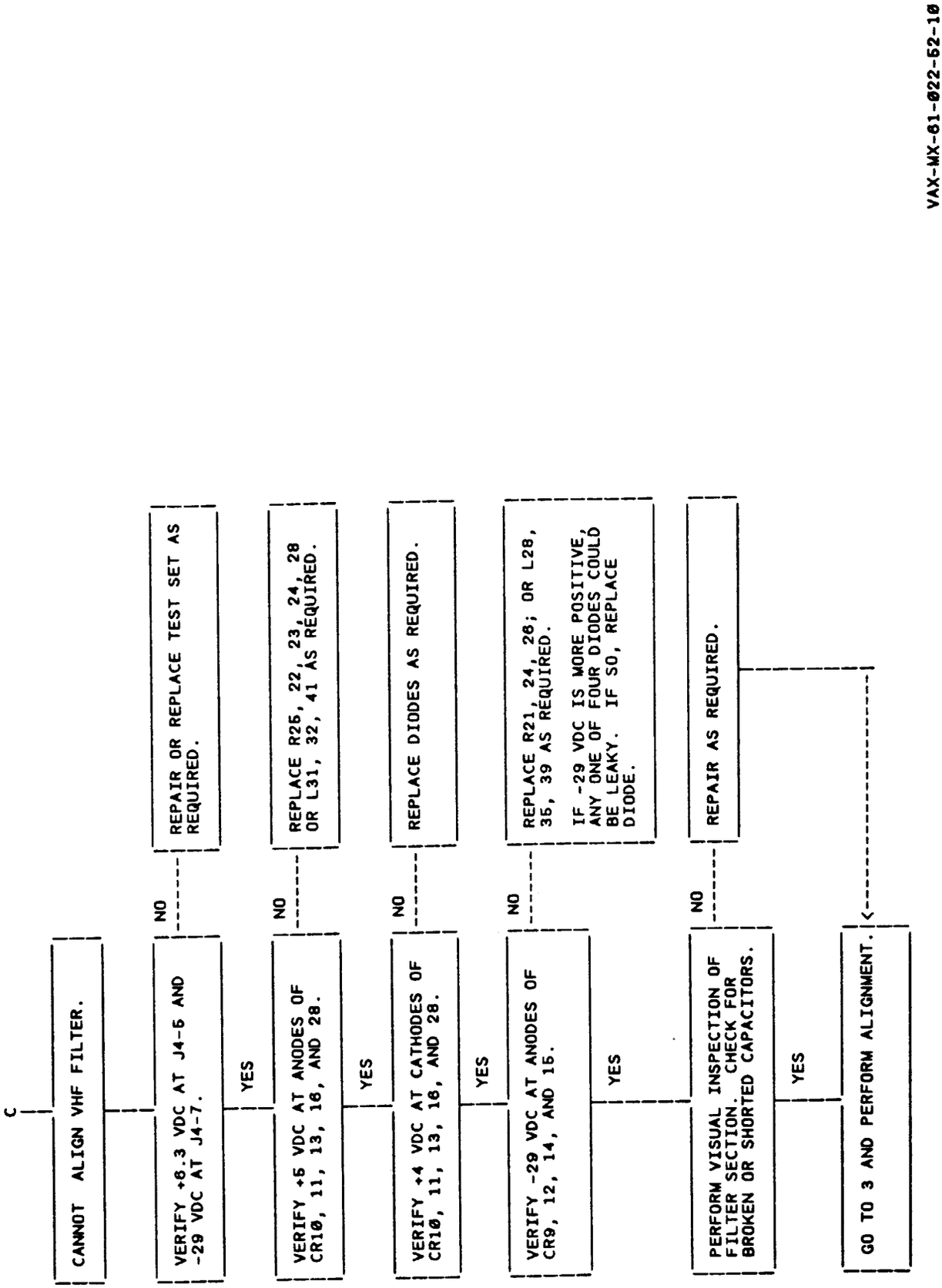
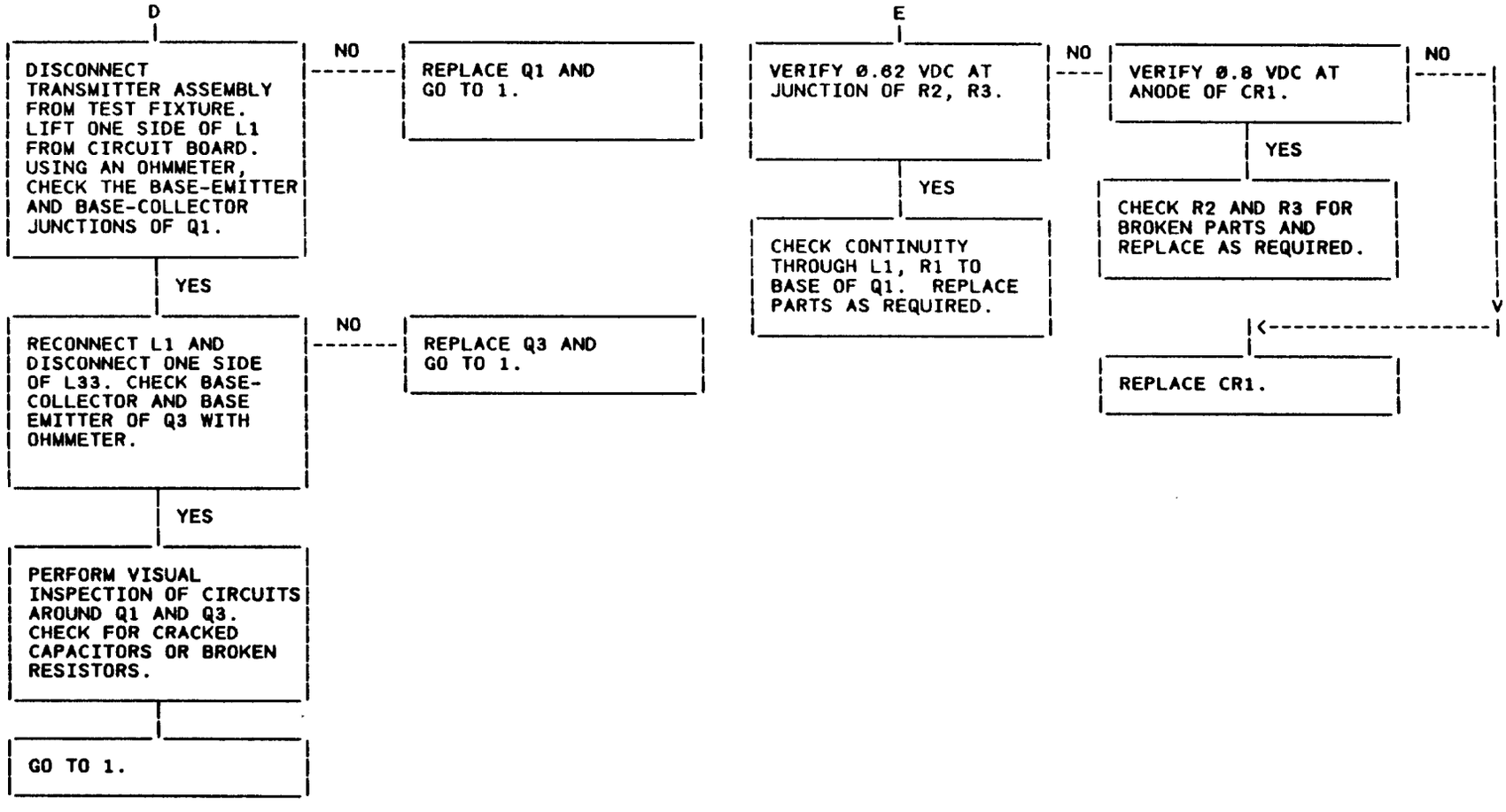


Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram
(Sheet 10 of 11)



VAX-MX-61-022-52-11

Figure 5-20. Transmitter Assembly A1A1A2 Trouble Analysis Diagram
(Sheet 11 of 11)

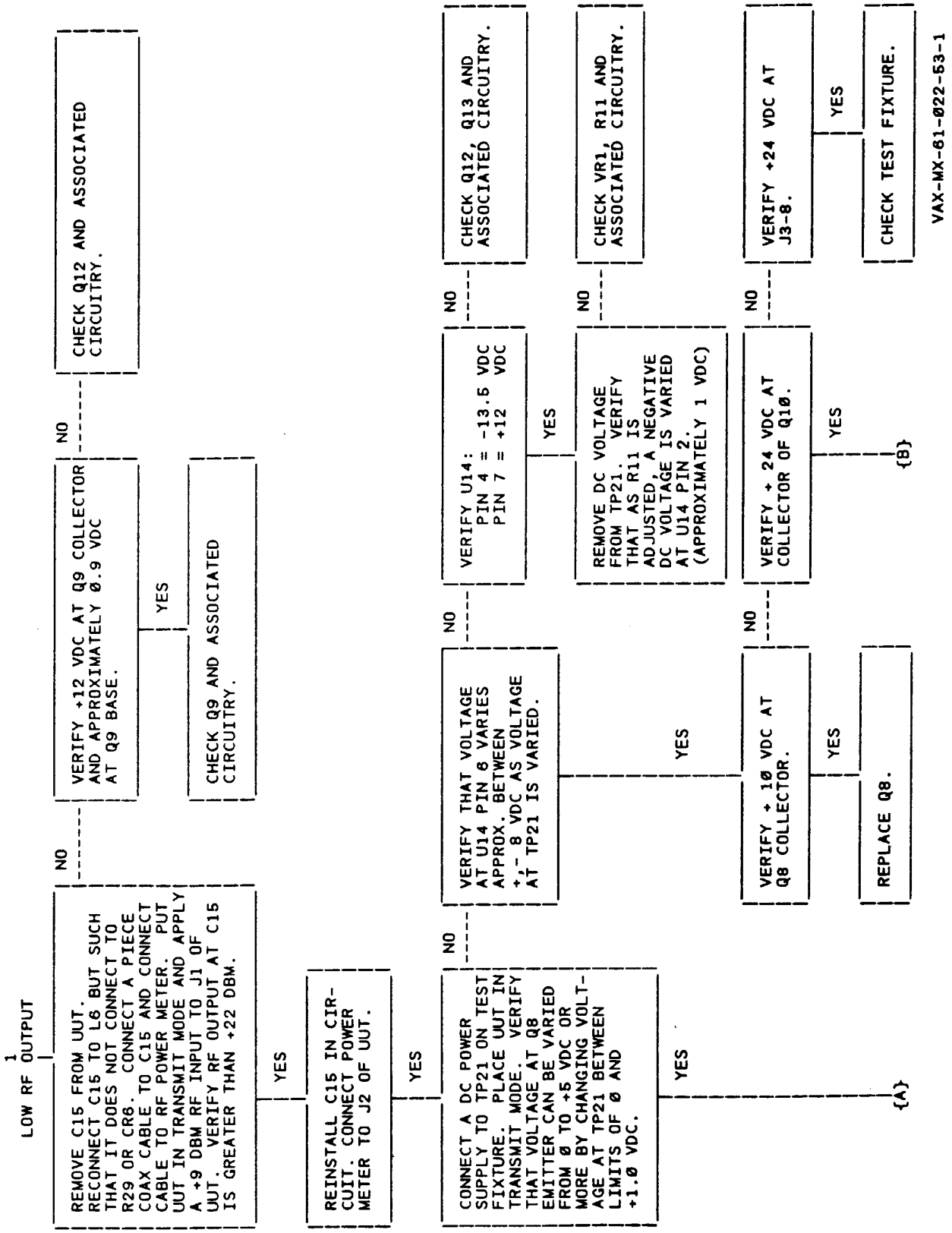
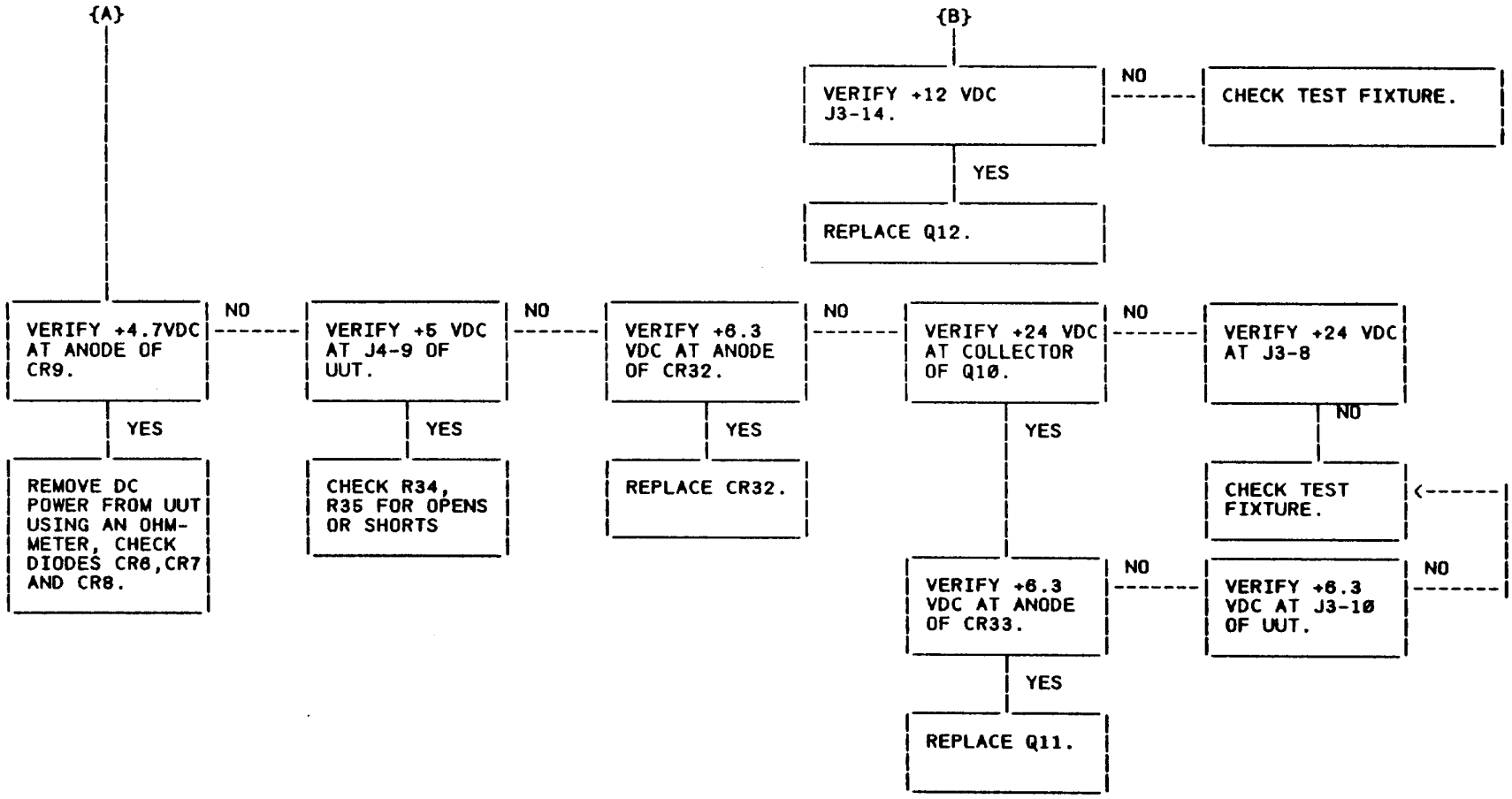


Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 1 of 14)



VAX-MX-61-022-53-2

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 2 of 14)

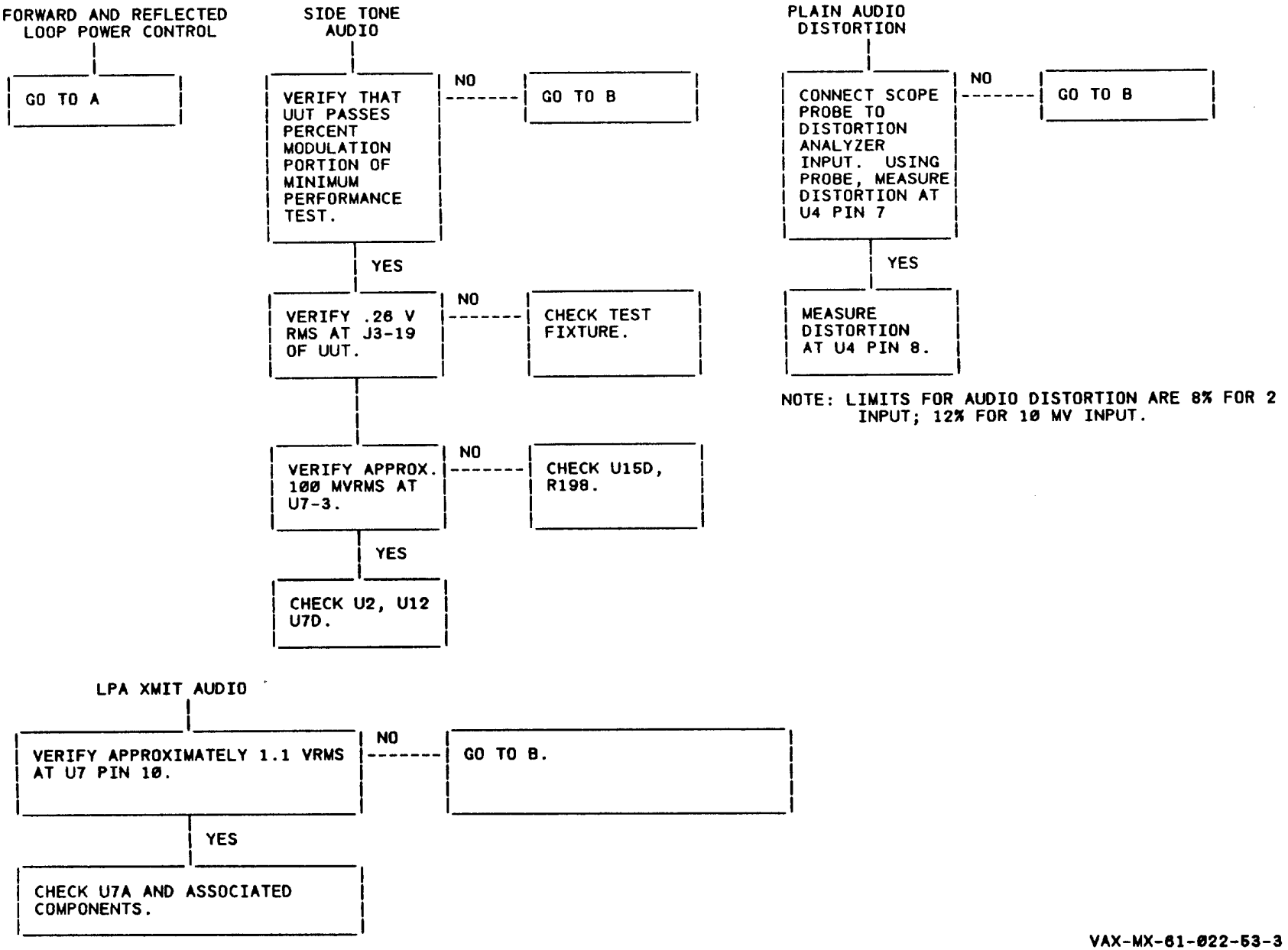
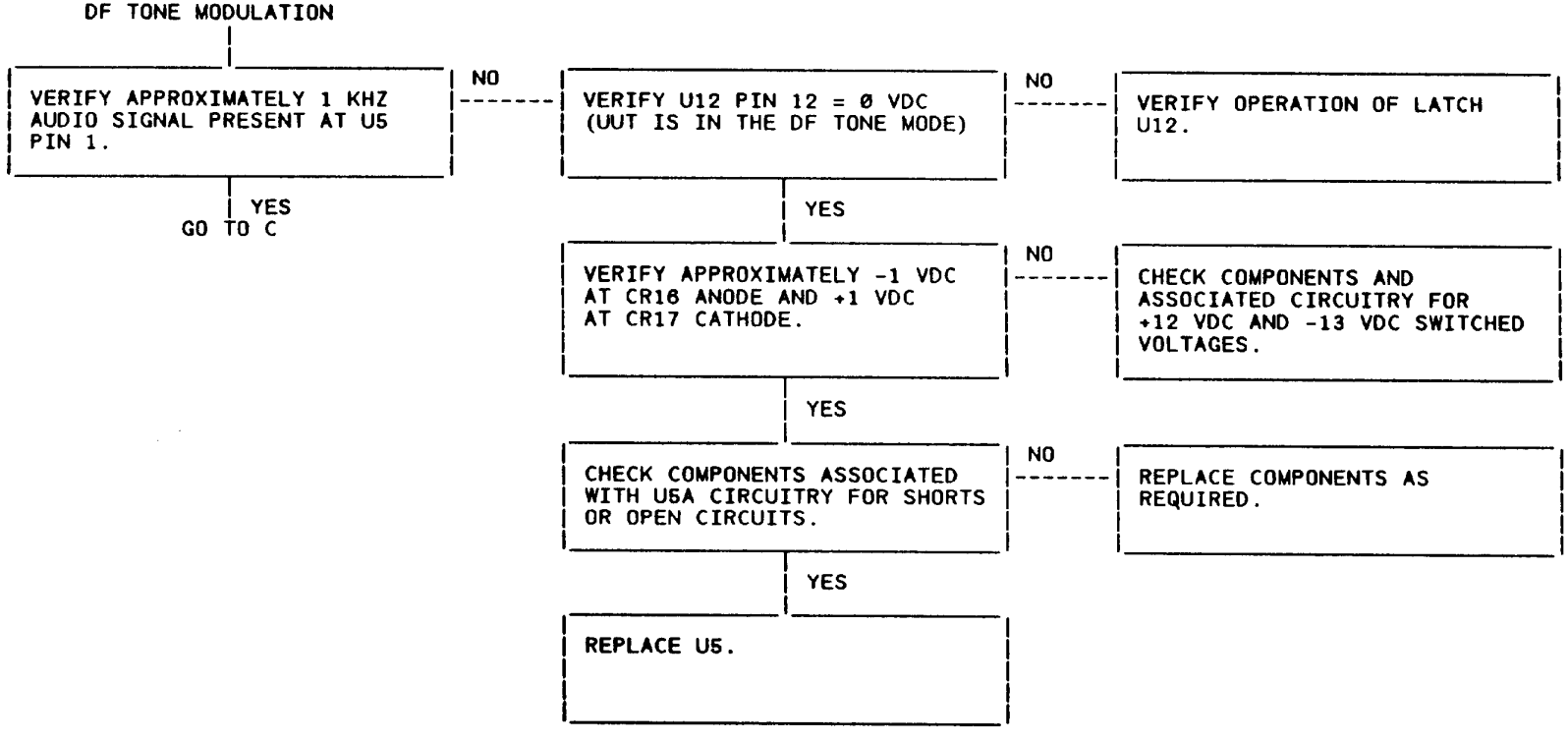
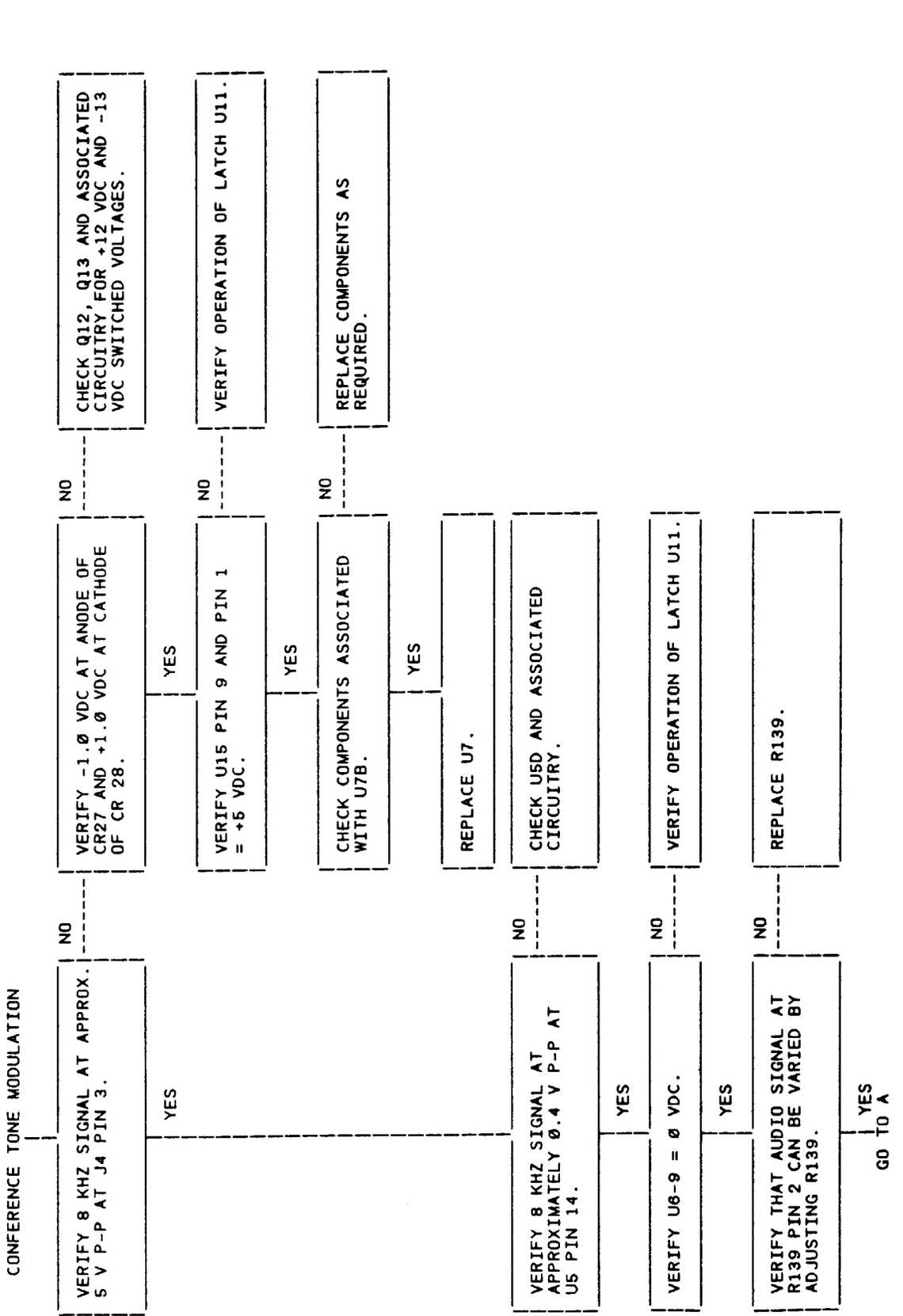


Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 3 of 14)



VAX-MX-61-022-53-4

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram (Sheet 4 of 14)



VAX-MX-81-022-53-5

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 5 of 14)

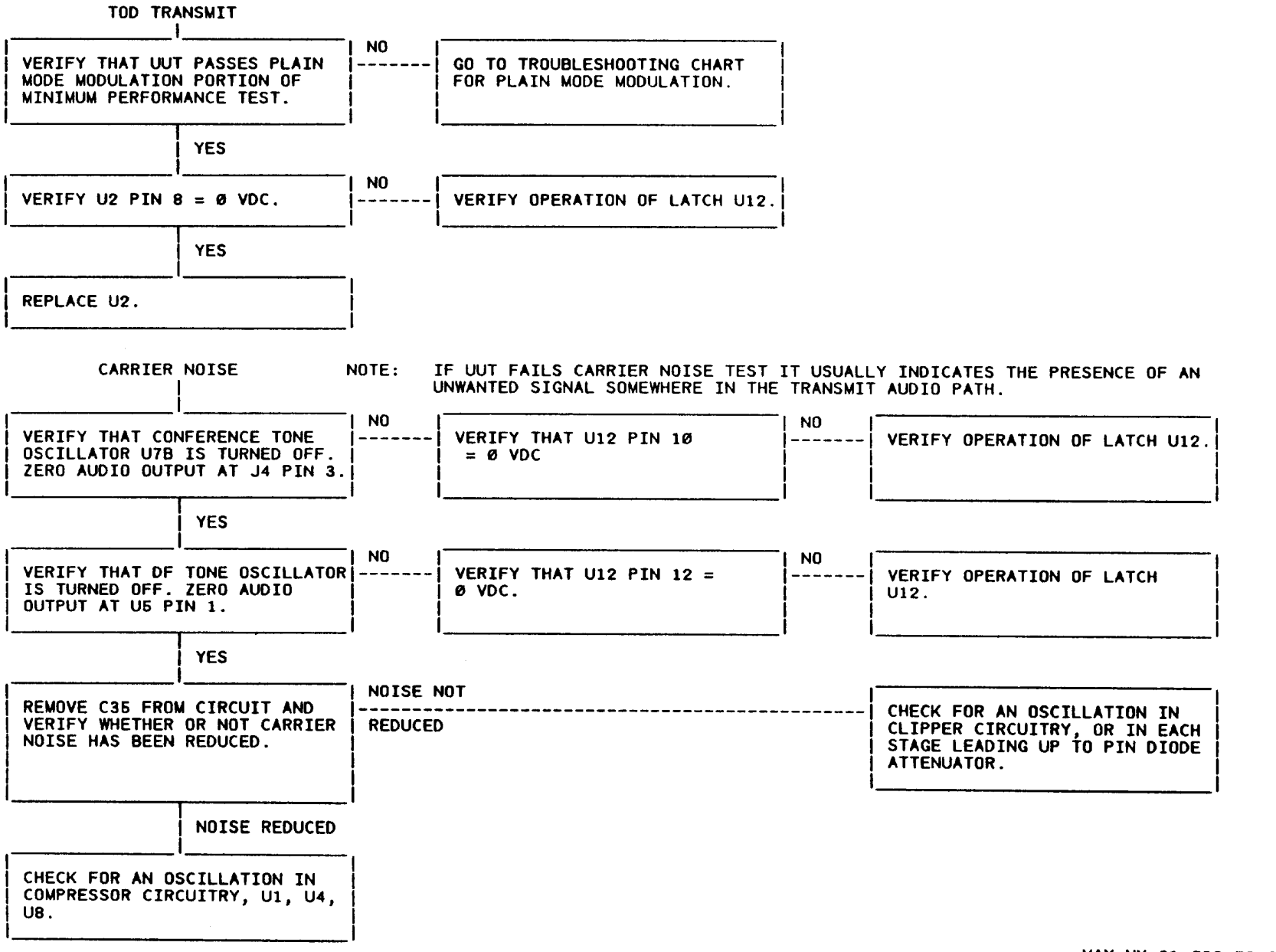
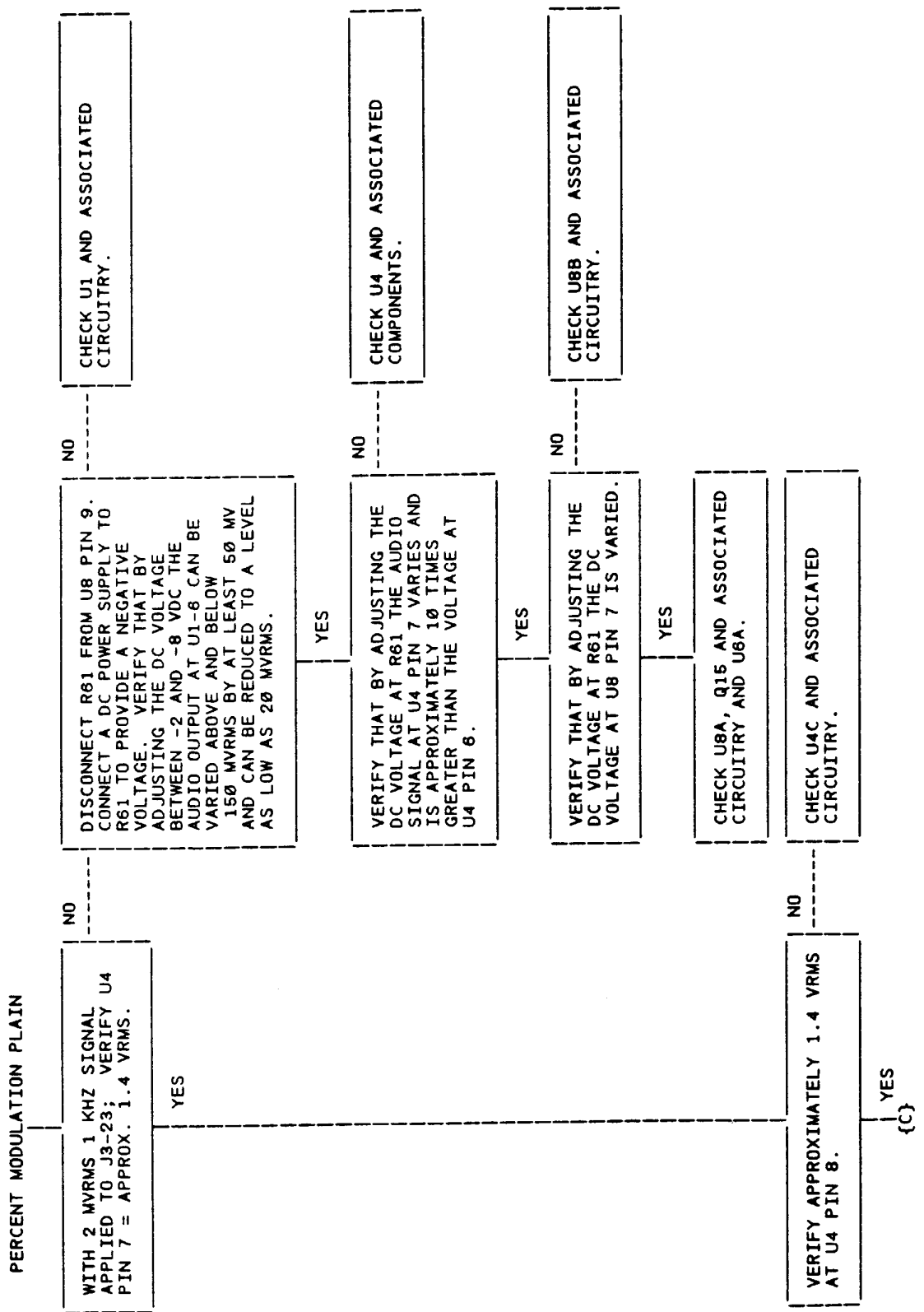
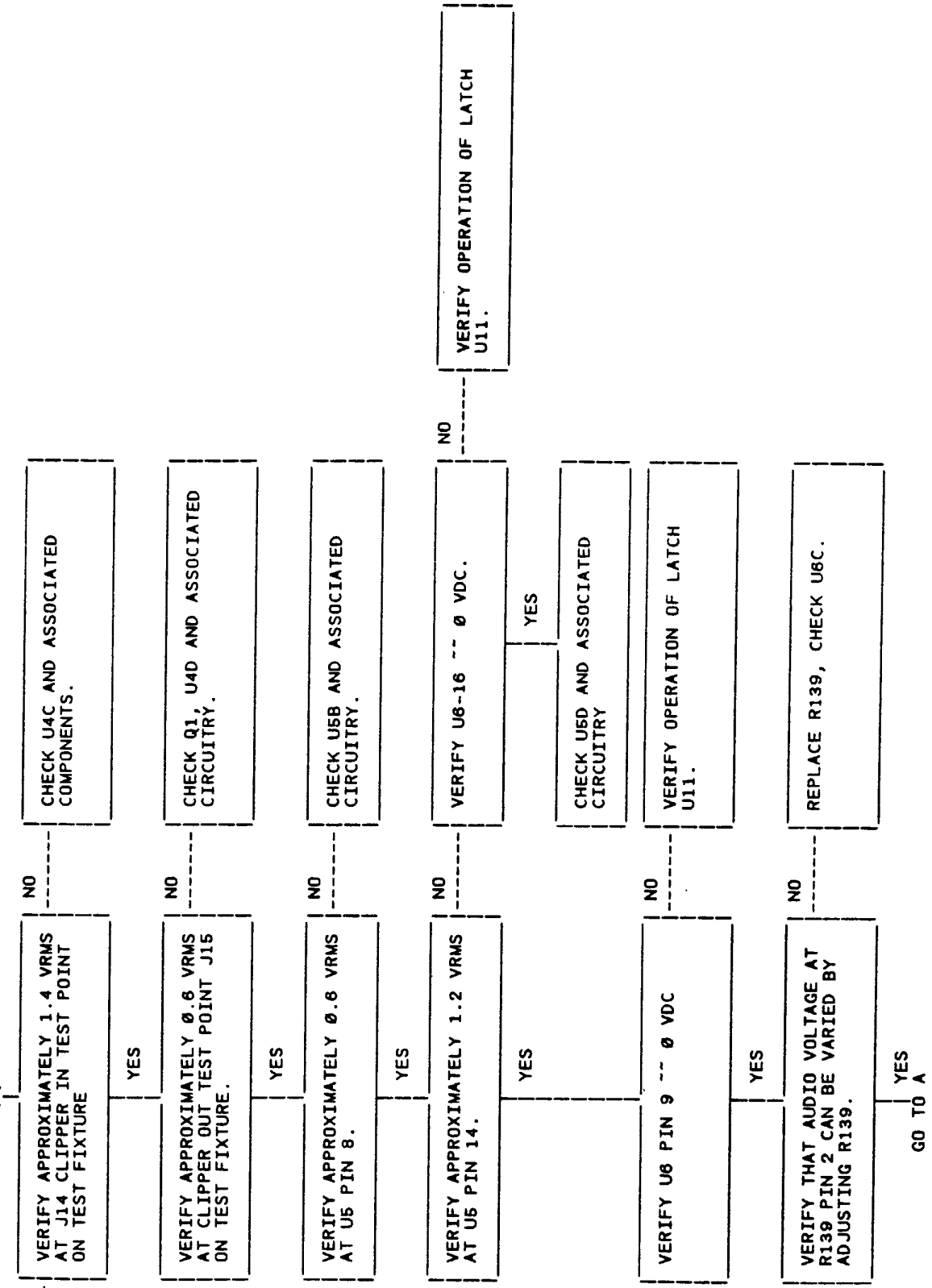


Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 6 of 14)



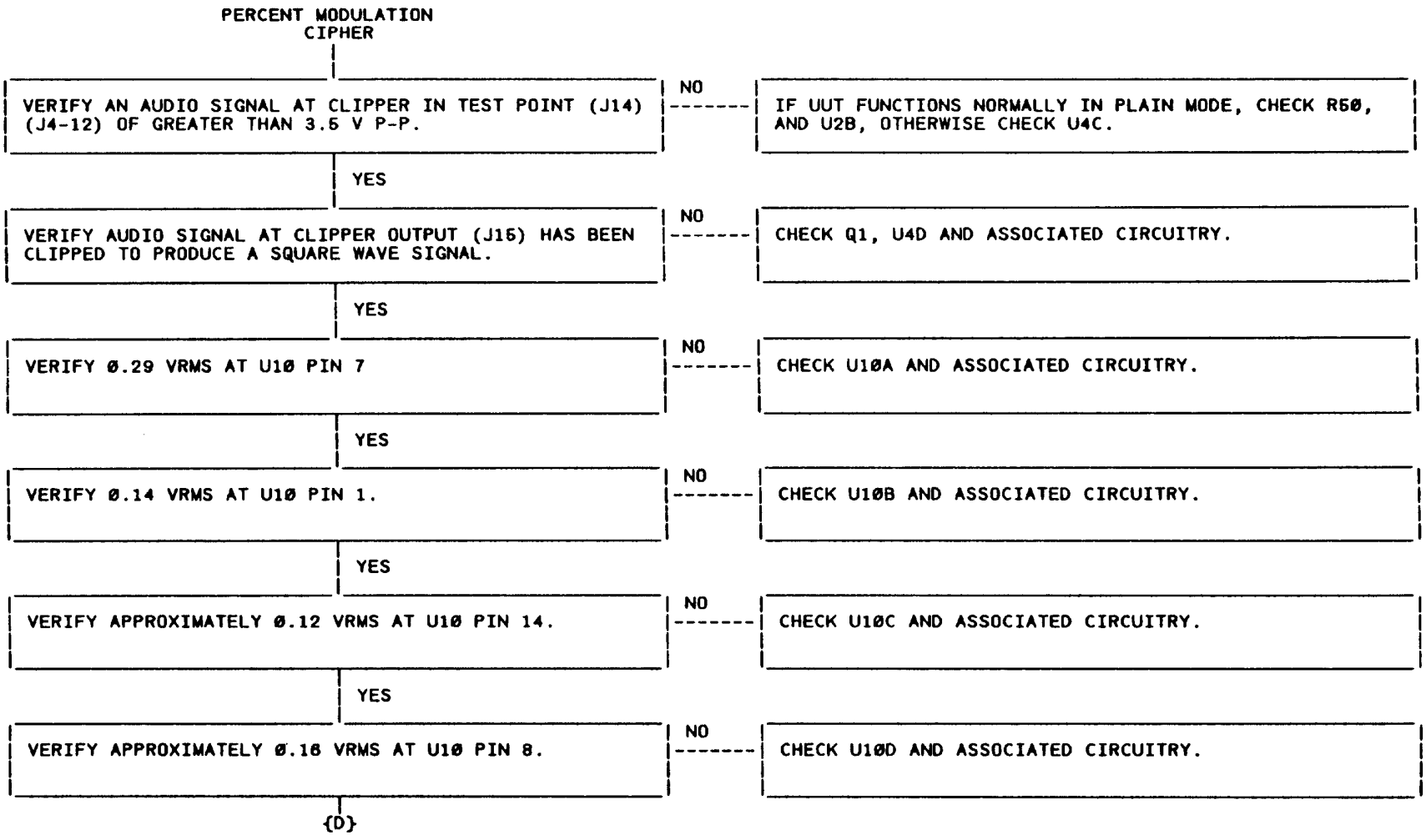
VAX-WX-01-022-53-7

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram (Sheet 7 of 14)



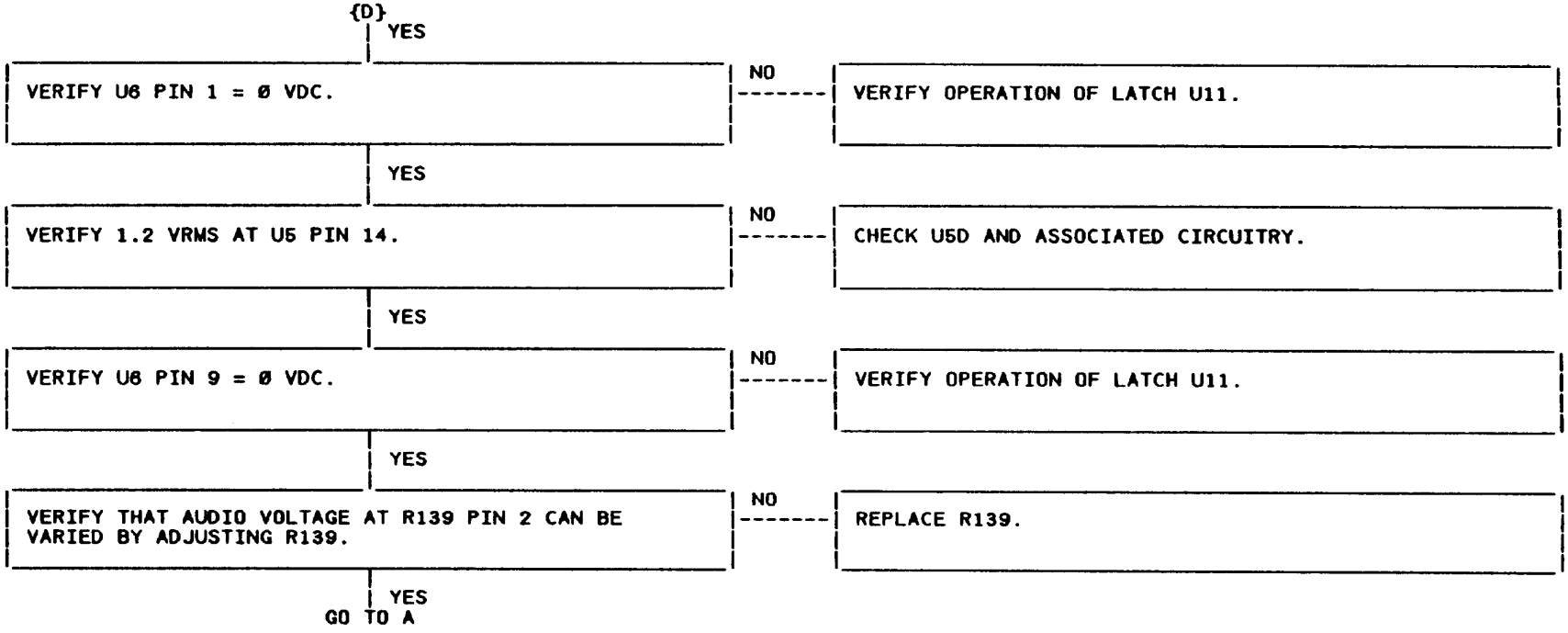
VAX-MX-81-022-53-8

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram (Sheet 8 of 14)



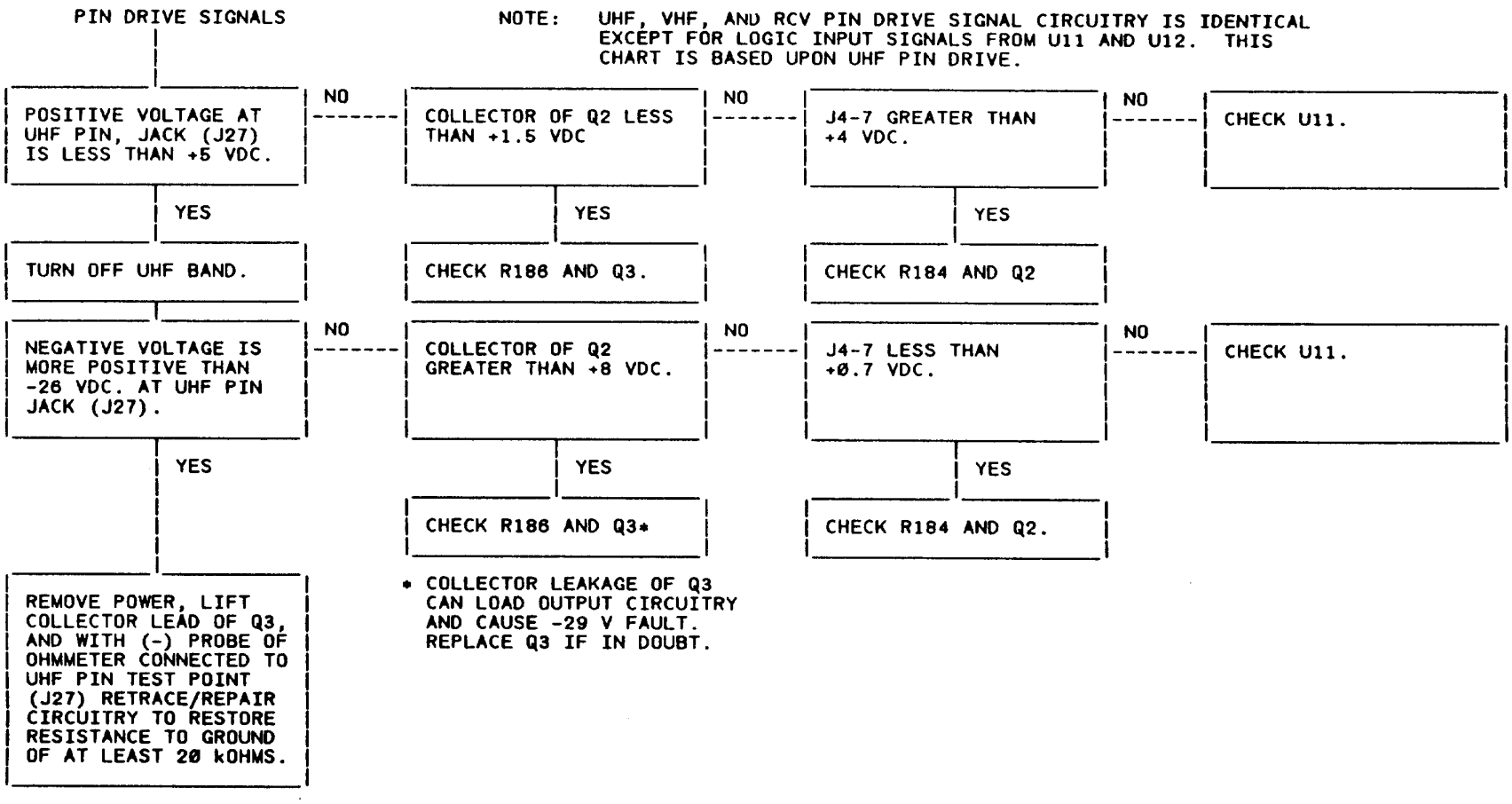
VAX-MX-61-022-53-9

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 9 of 14)



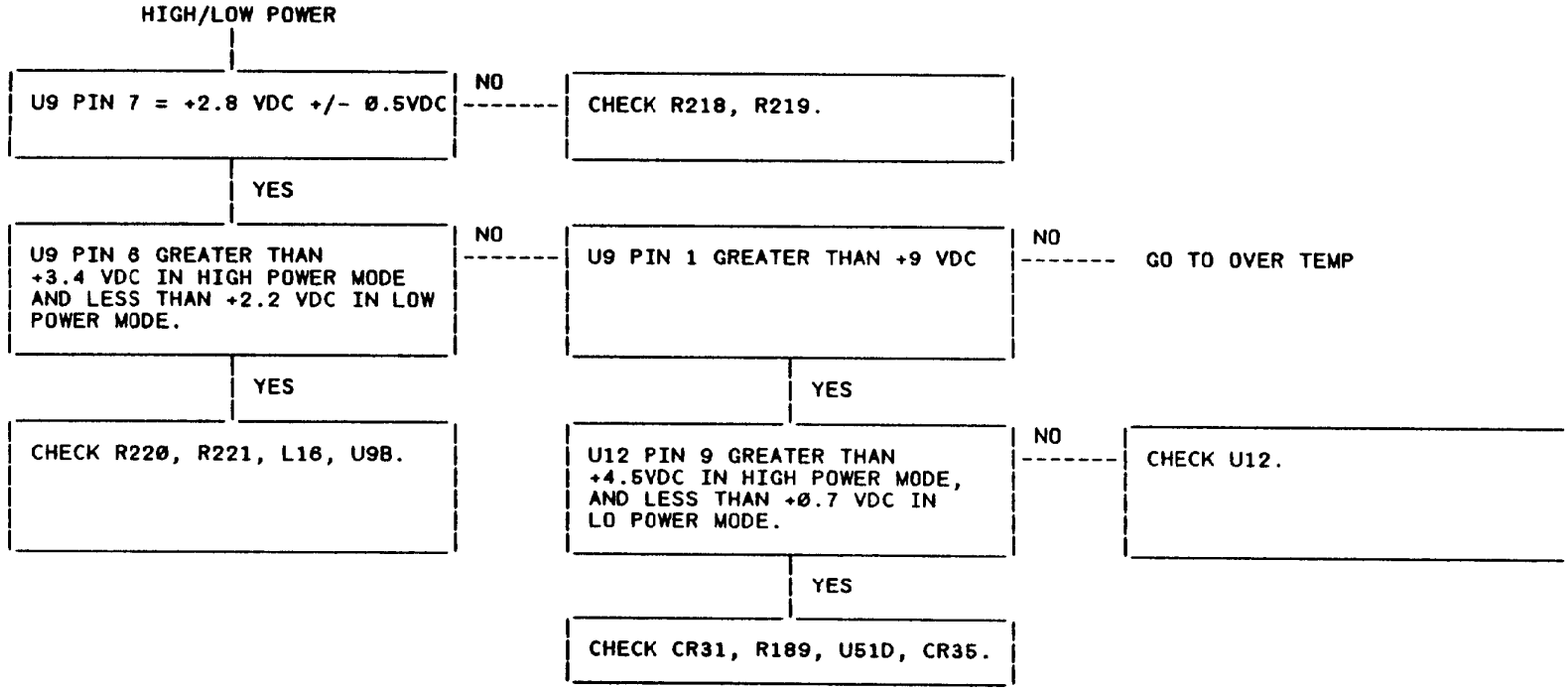
VAX-MX-61-022-53-10

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 10 of 14)



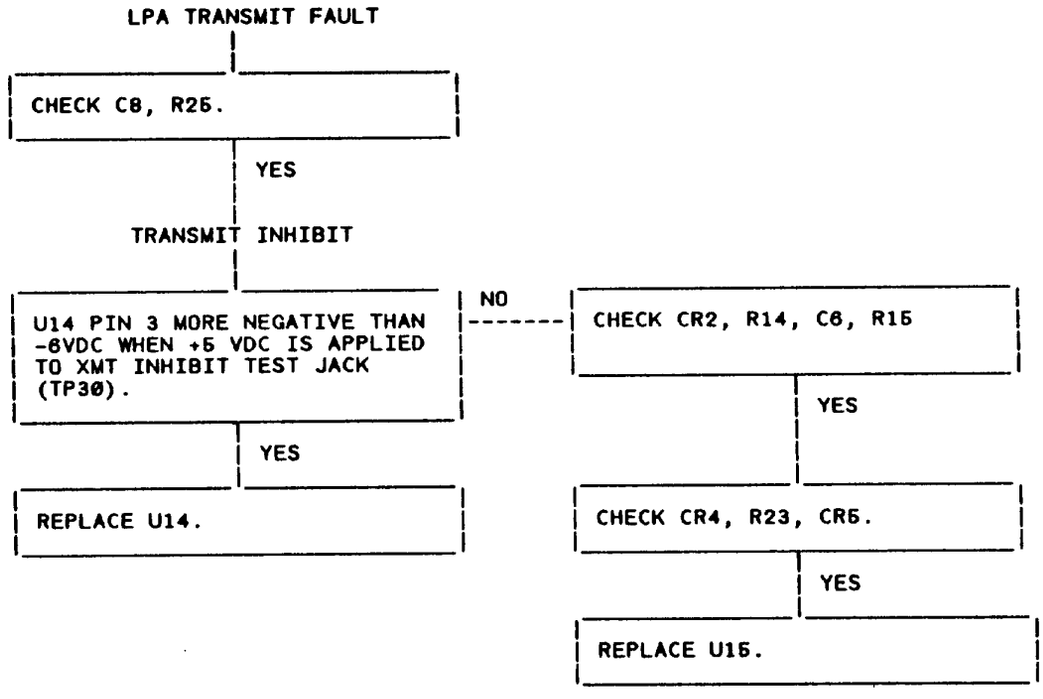
VAX-MX-81-022-53-11

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 11 of 14)



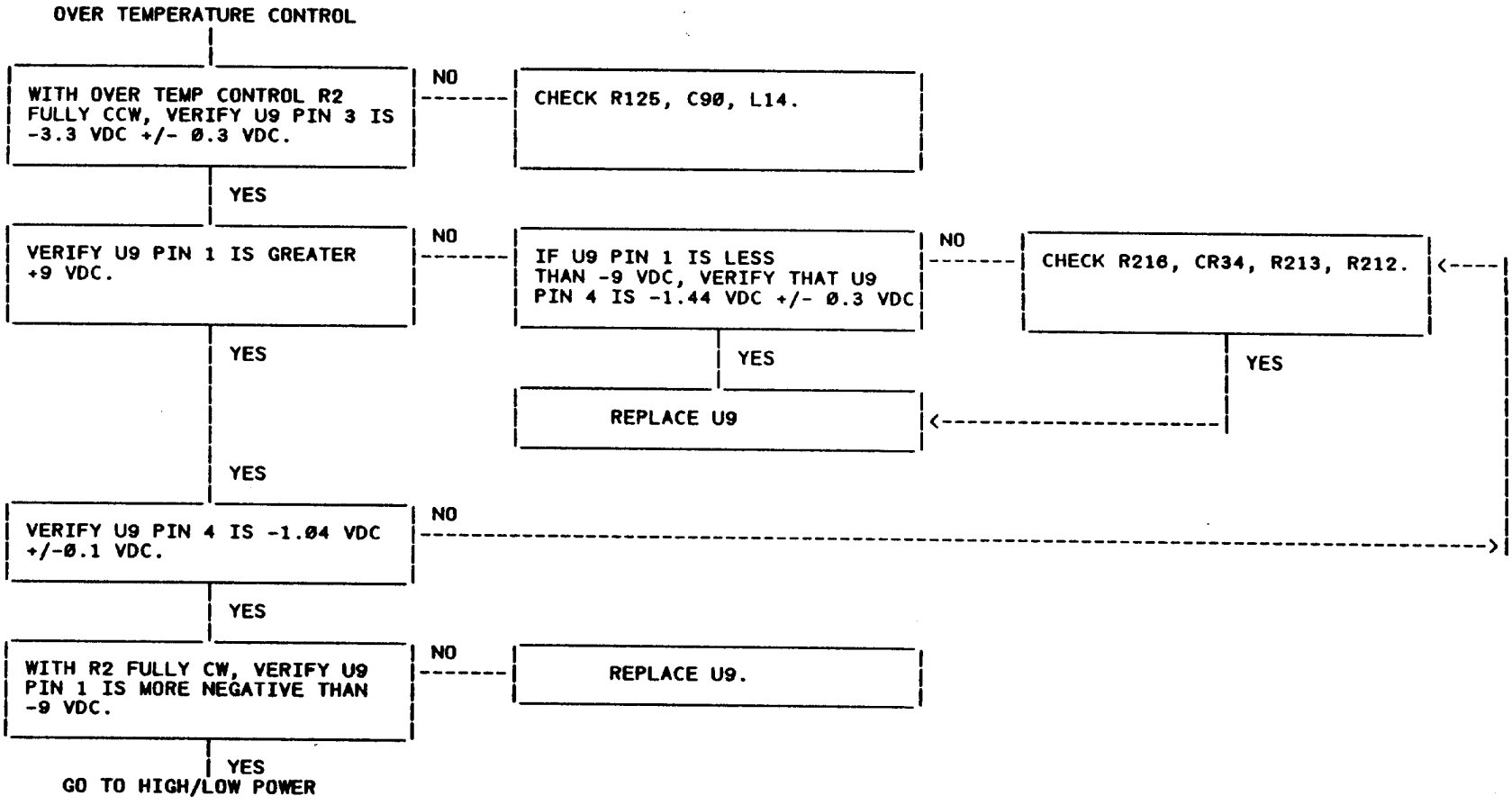
VAX-MX-81-Ø22-53-12

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 12 of 14)



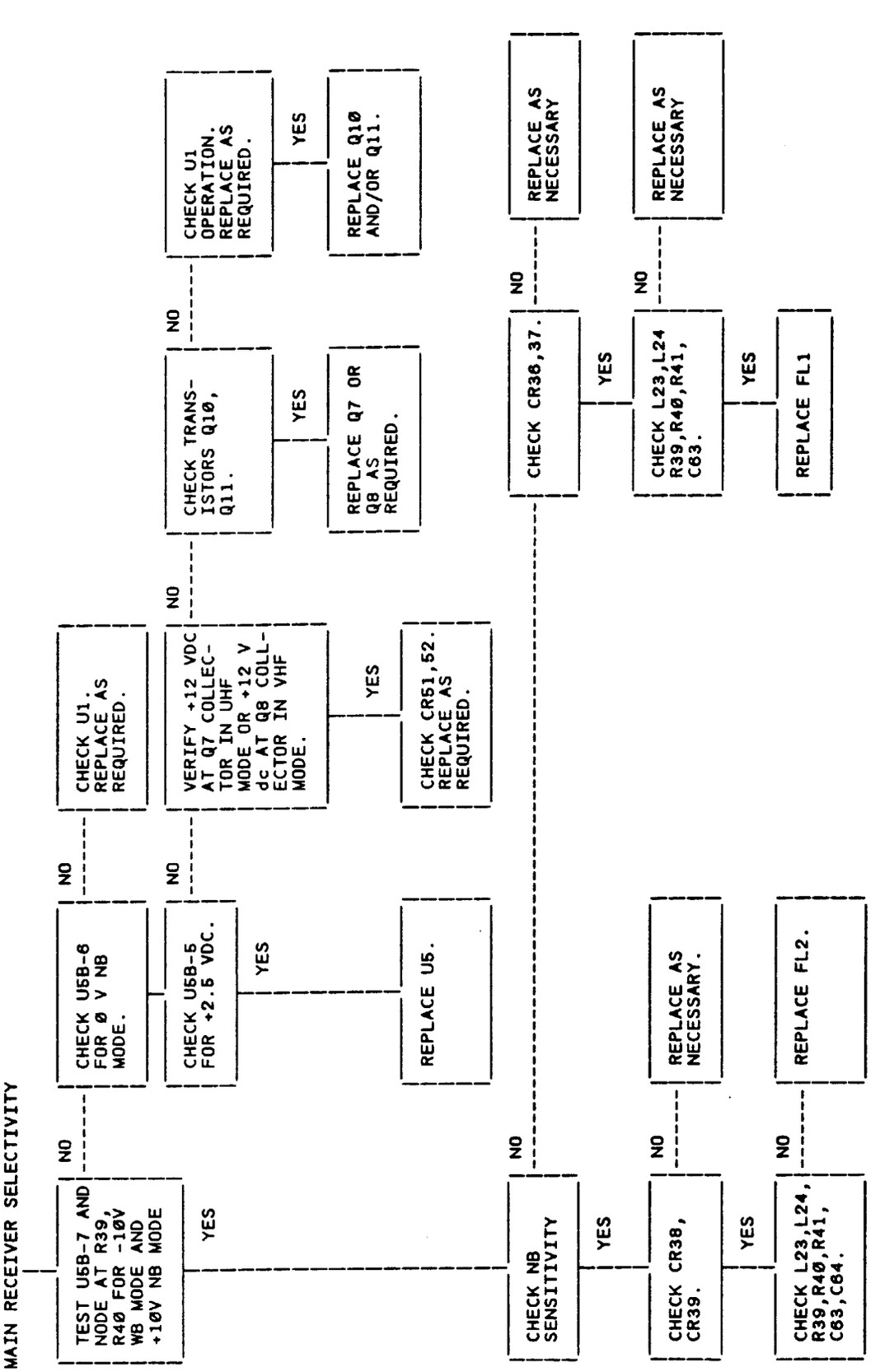
VAX-MX-61-022-53-13

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 13 of 14)



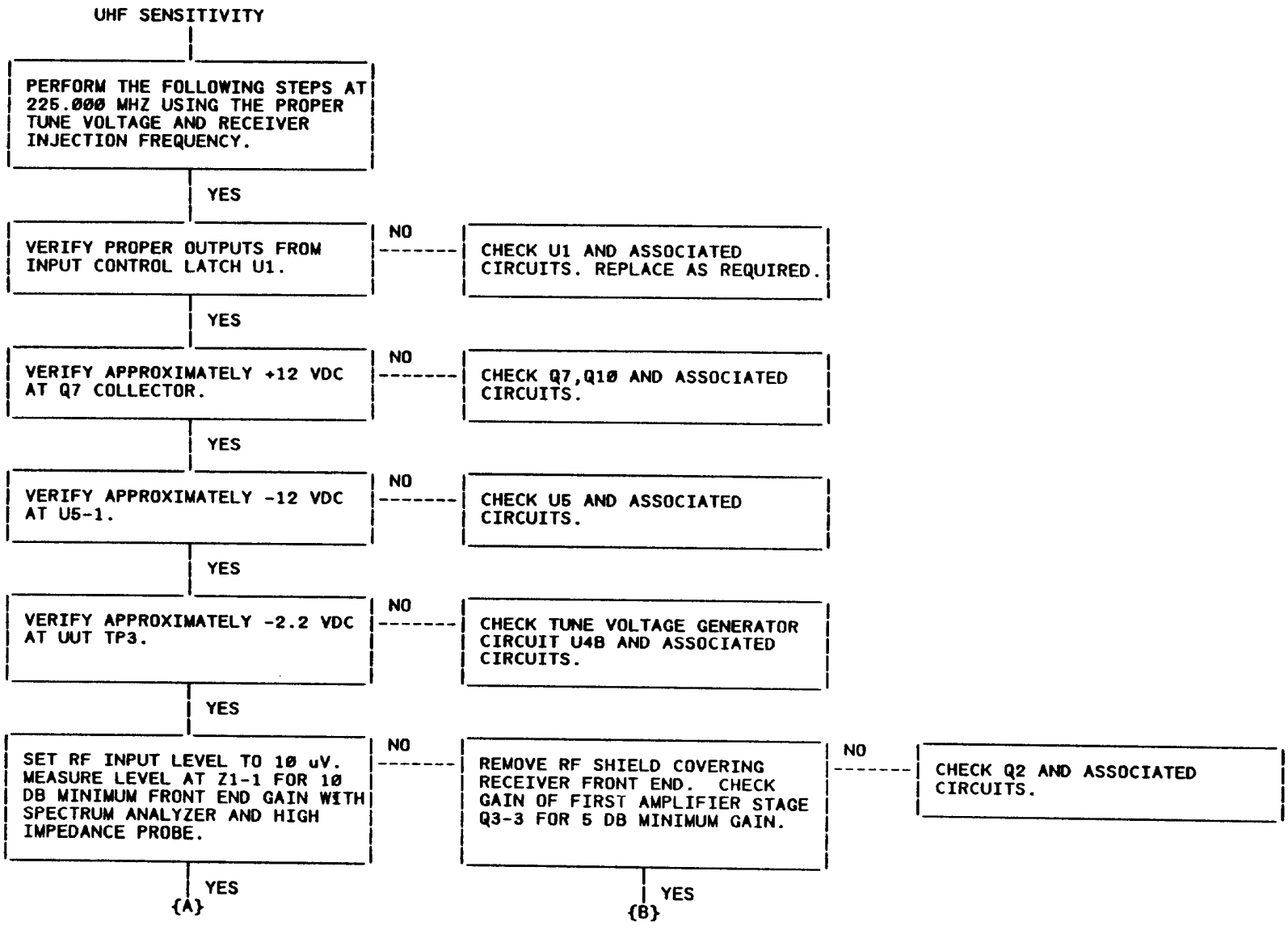
VAX-MX-61-022-53-14

Figure 5-21. Modulator Assembly A1A1A3 Trouble Analysis Diagram
(Sheet 14 of 14)



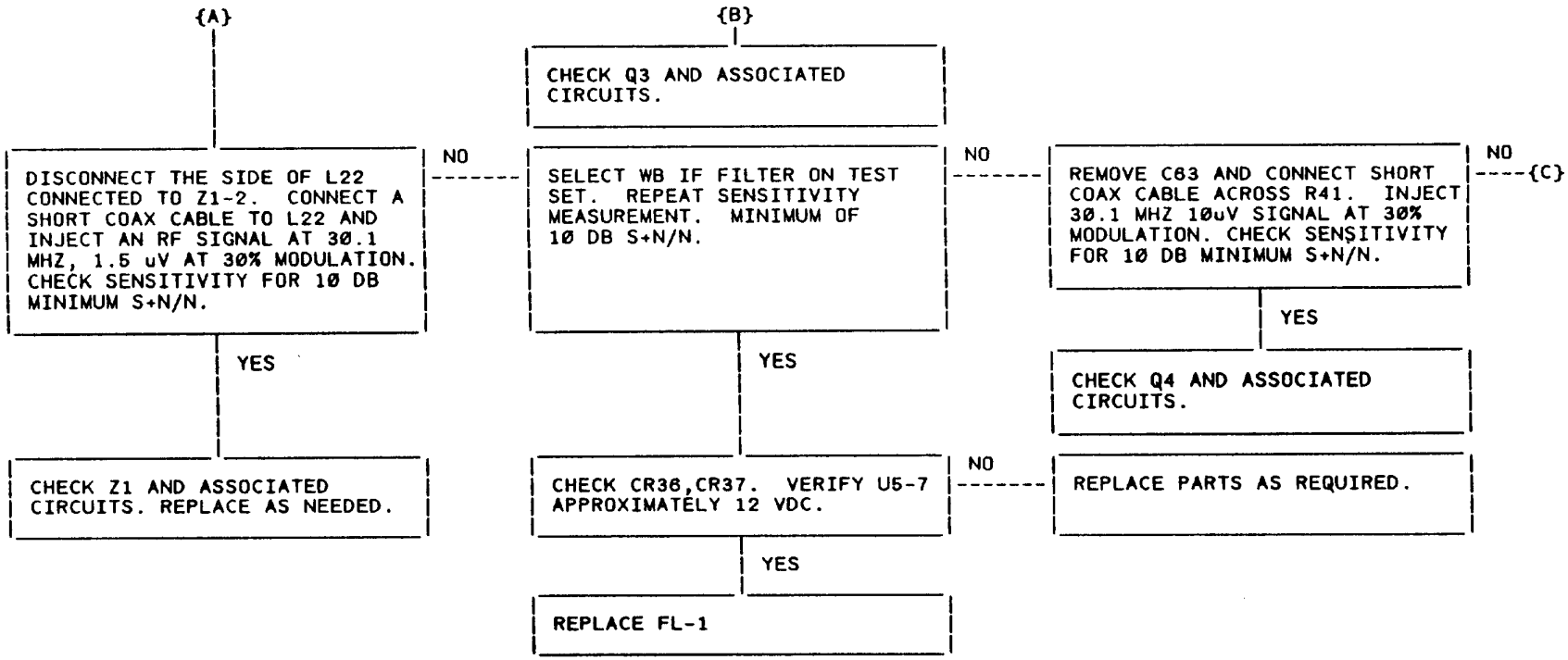
VAX-MX-81-022-54-1

Figure 5-22. Main Receiver Assembly A1A1A4 Trouble Analysis Diagram
(Sheet 1 of 9)



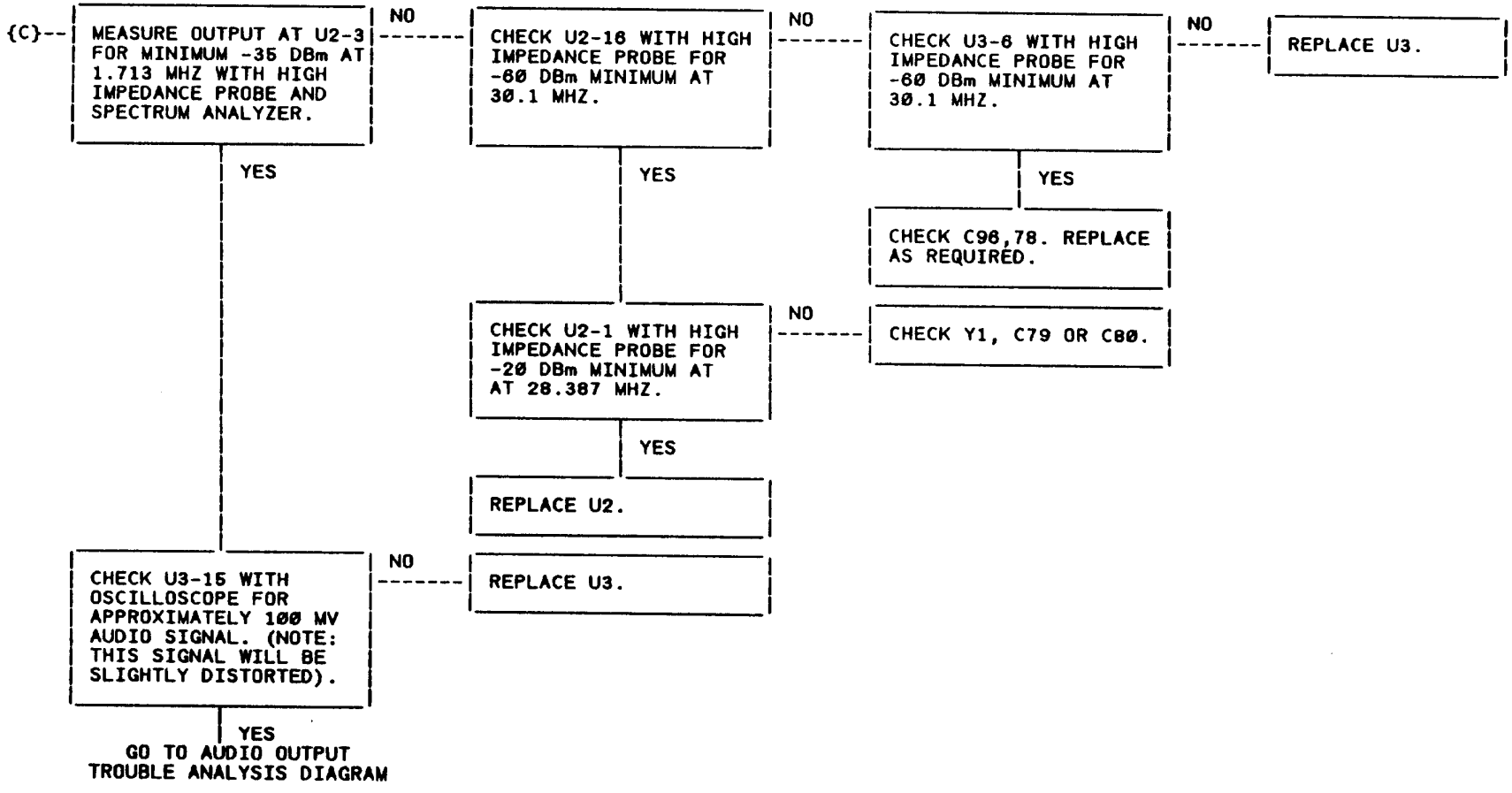
VAX-MX-61-022-54-2

Figure 5-22. Main Receiver Assembly A1A1A4 Trouble Analysis Diagram
(Sheet 2 of 9)



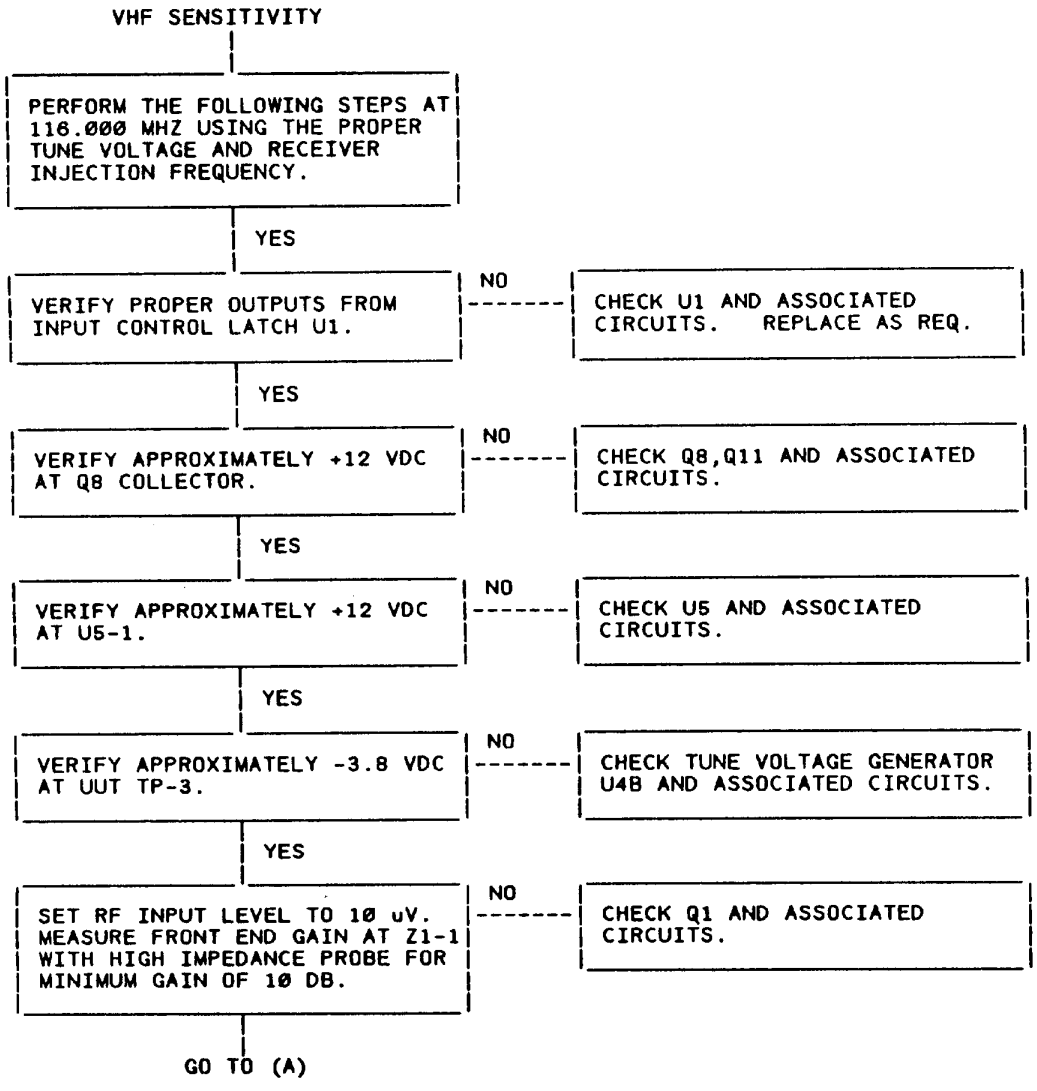
VAX-MX-81-022-54-3

Figure 5-22. Main Receiver Assembly A1A1A4 Trouble Analysis Diagram
(Sheet 3 of 9)



VAX-MX-61-022-54-4

Figure 5-22. Main Receiver Assembly A1A1A4 Trouble Analysis Diagram (Sheet 4 of 9)



VAX-MX-81-022-54-5

Figure 5-22. Main Receiver Assembly A1A1A4 Trouble Analysis Diagram
(Sheet 5 of 9)

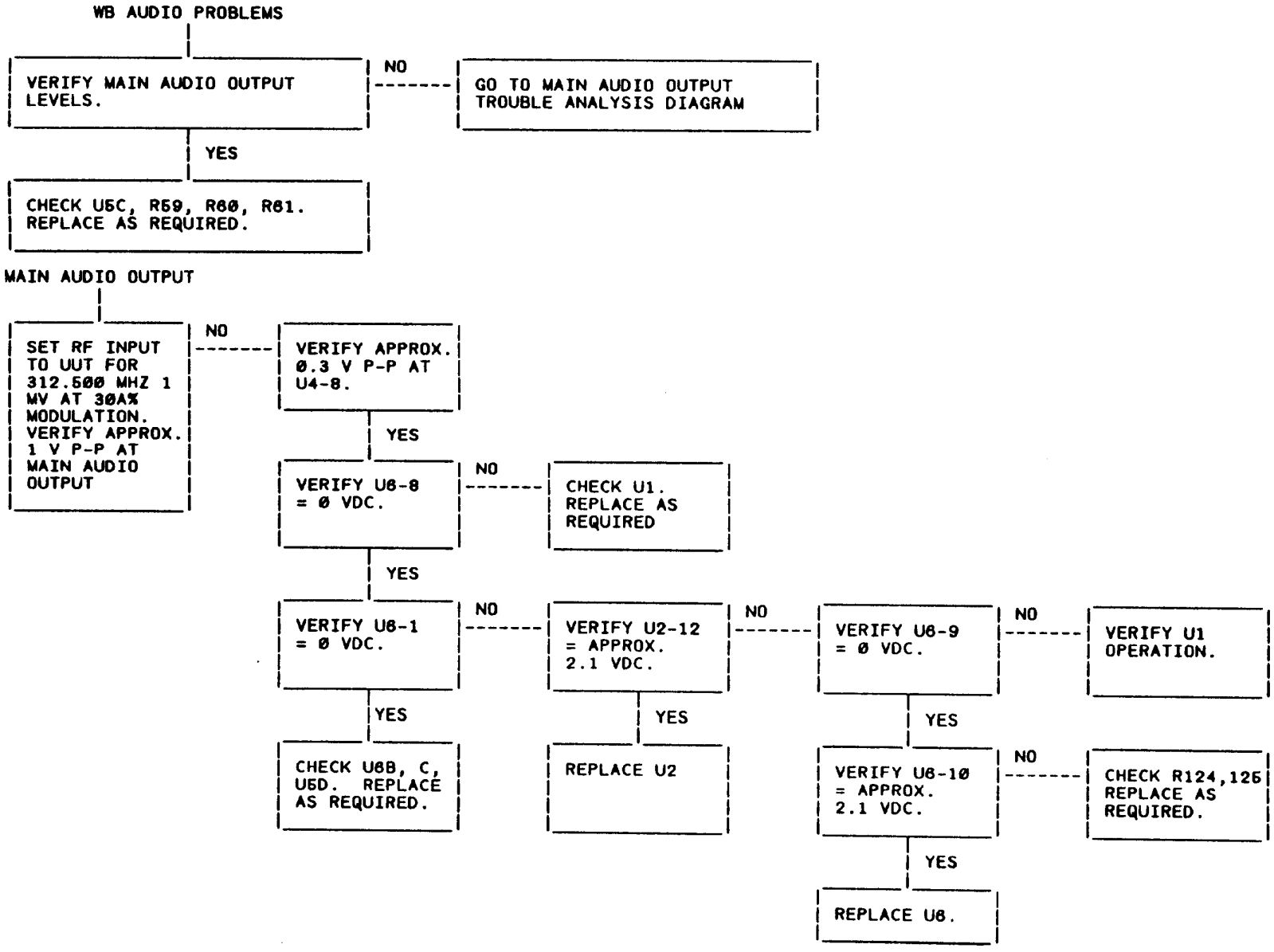
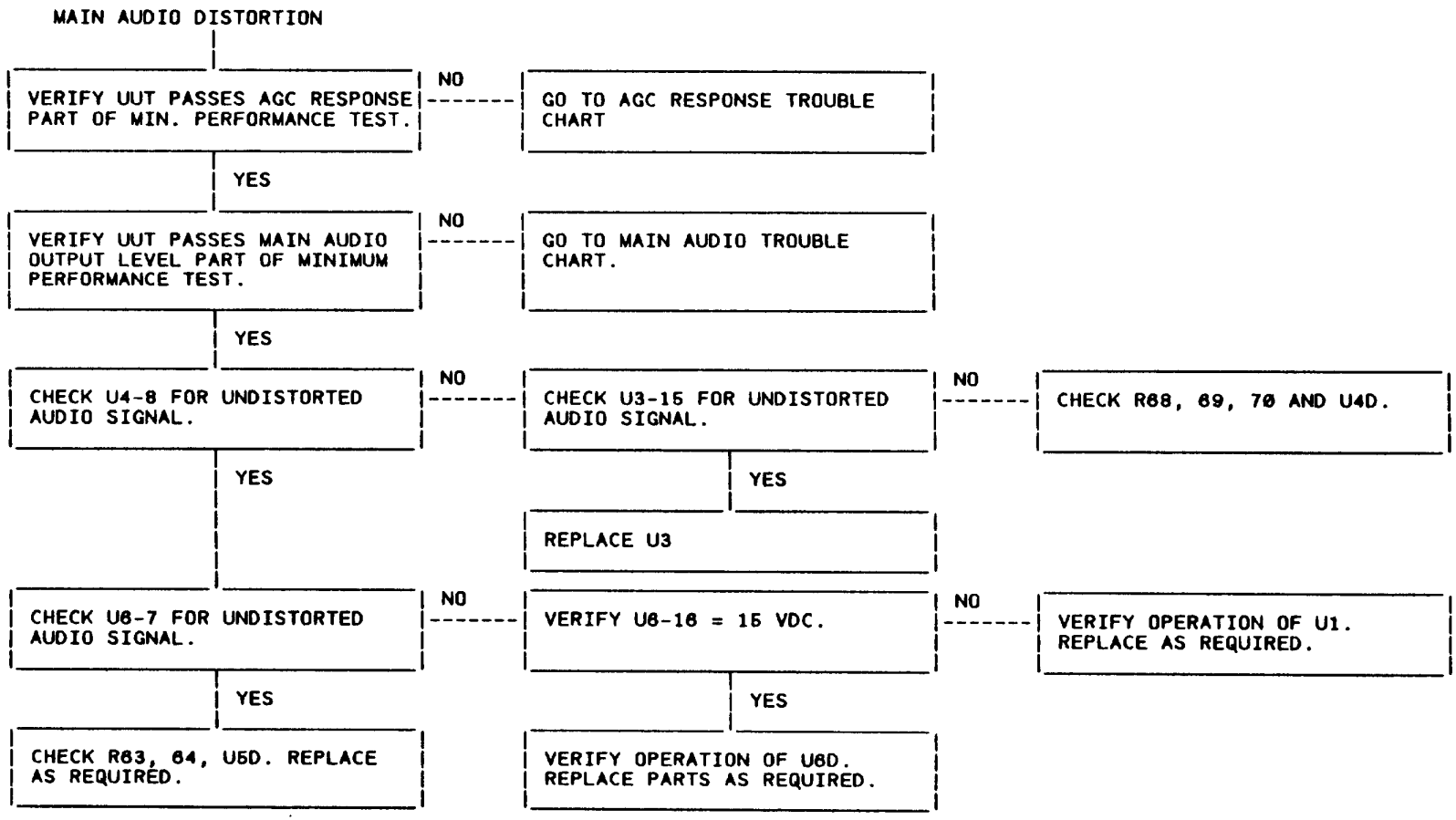
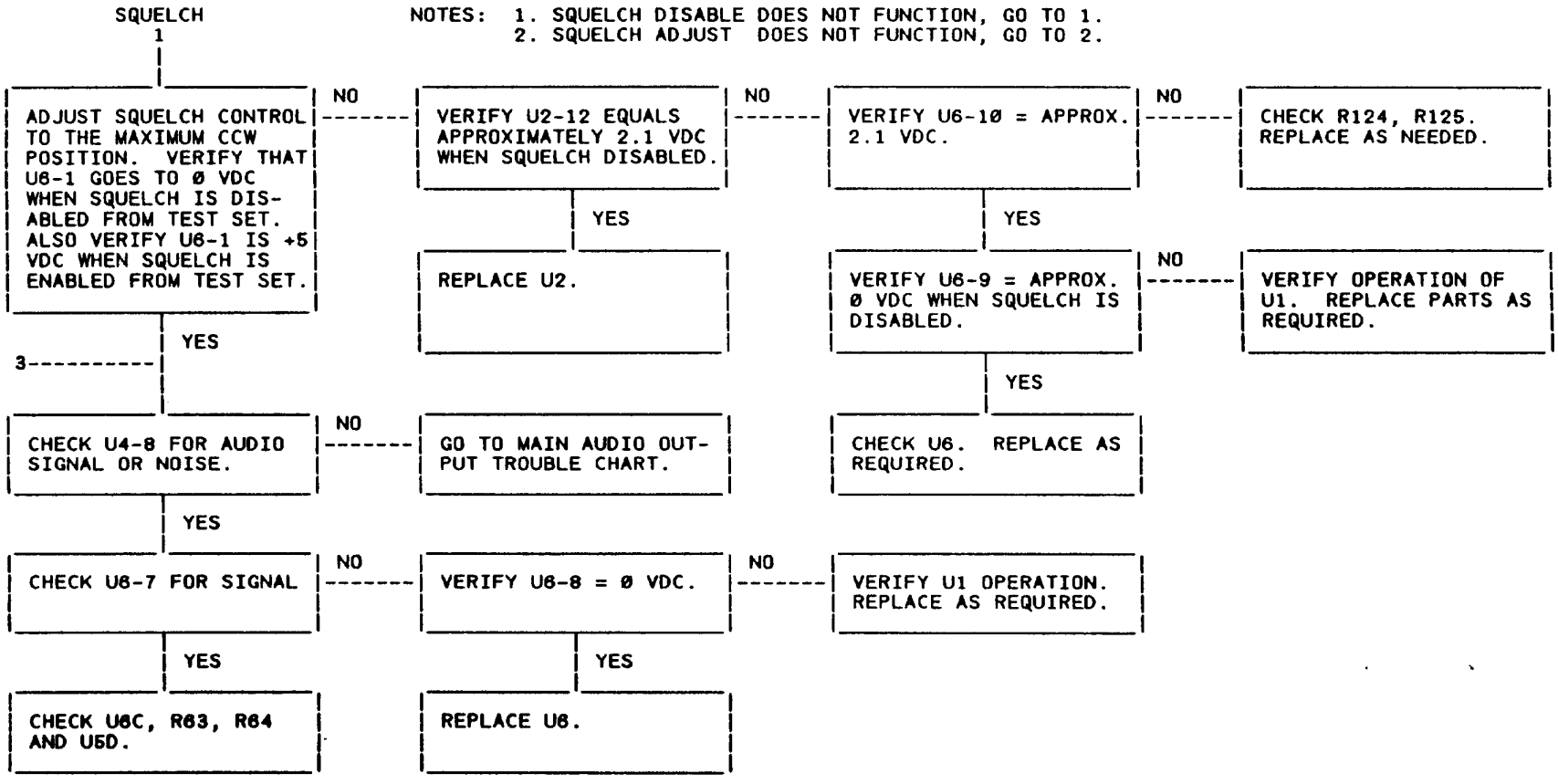


Figure 5-22. Main Receiver Assembly A1A1A4 Trouble Analysis Diagram
(Sheet 6 of 9)



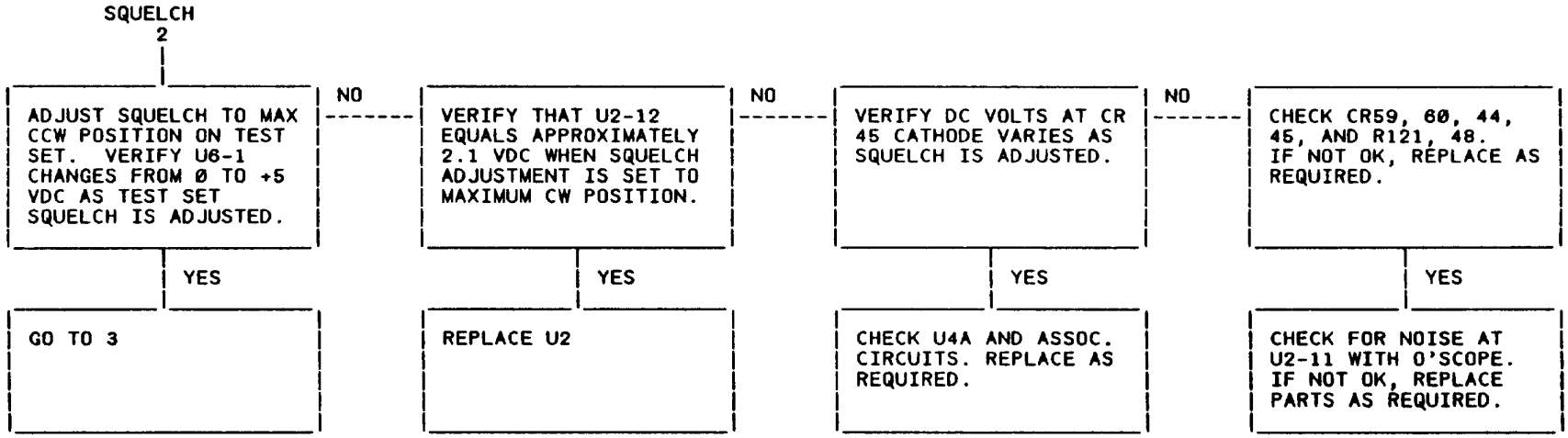
VAX-MX-61-022-64-7

Figure 5-22. Main Receiver Assembly A1A1A4 Trouble Analysis Diagram
(Sheet 7 of 9)



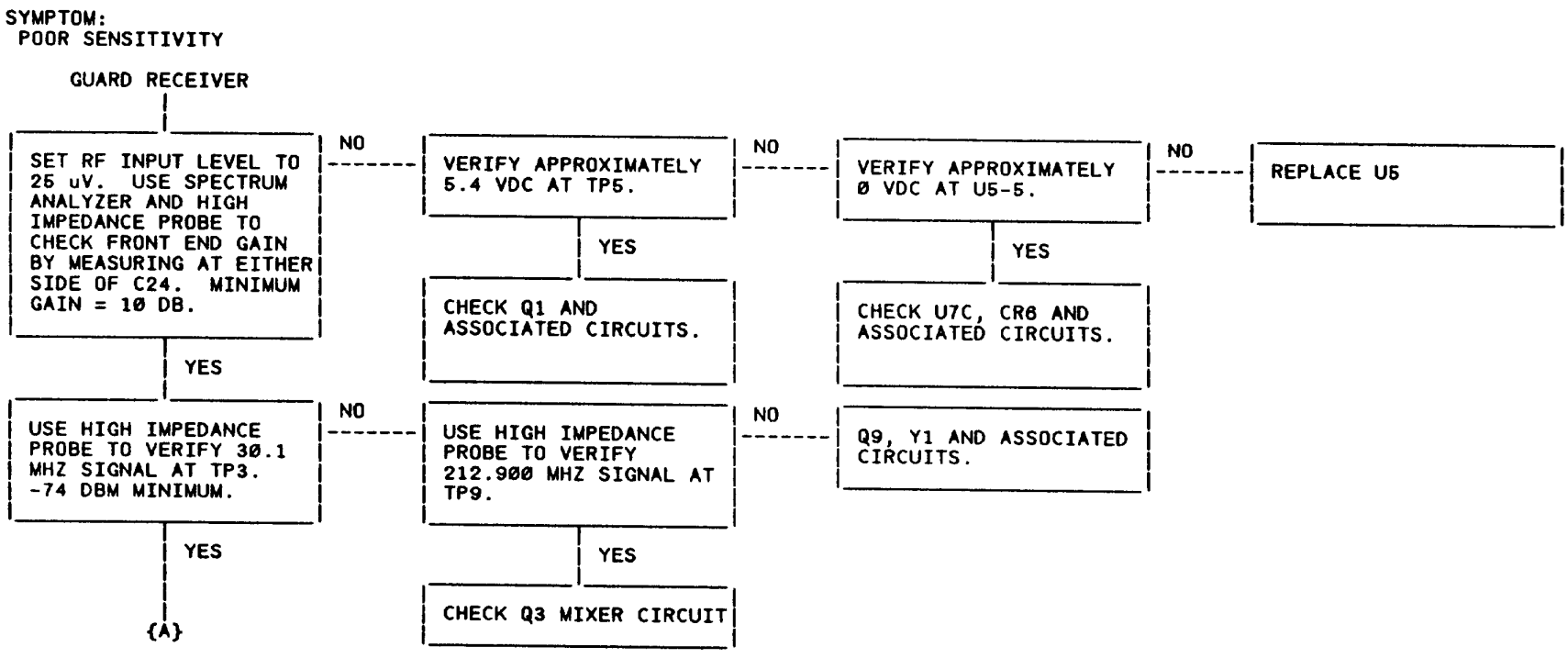
VAX-MX-81-022-54-8

Figure 5-22. Main Receiver Assembly A1A1A4 Trouble Analysis Diagram
(Sheet 8 of 9)



VAX-MX-81-022-54-9

Figure 5-22. Main Receiver Assembly A1A1A4 Trouble Analysis Diagram
(Sheet 9 of 9)



VAX-MX-61-022-55-1

Figure 5-23. Guard Receiver Assembly A1A1A5 Trouble Analysis Diagram
(Sheet 1 of 7)

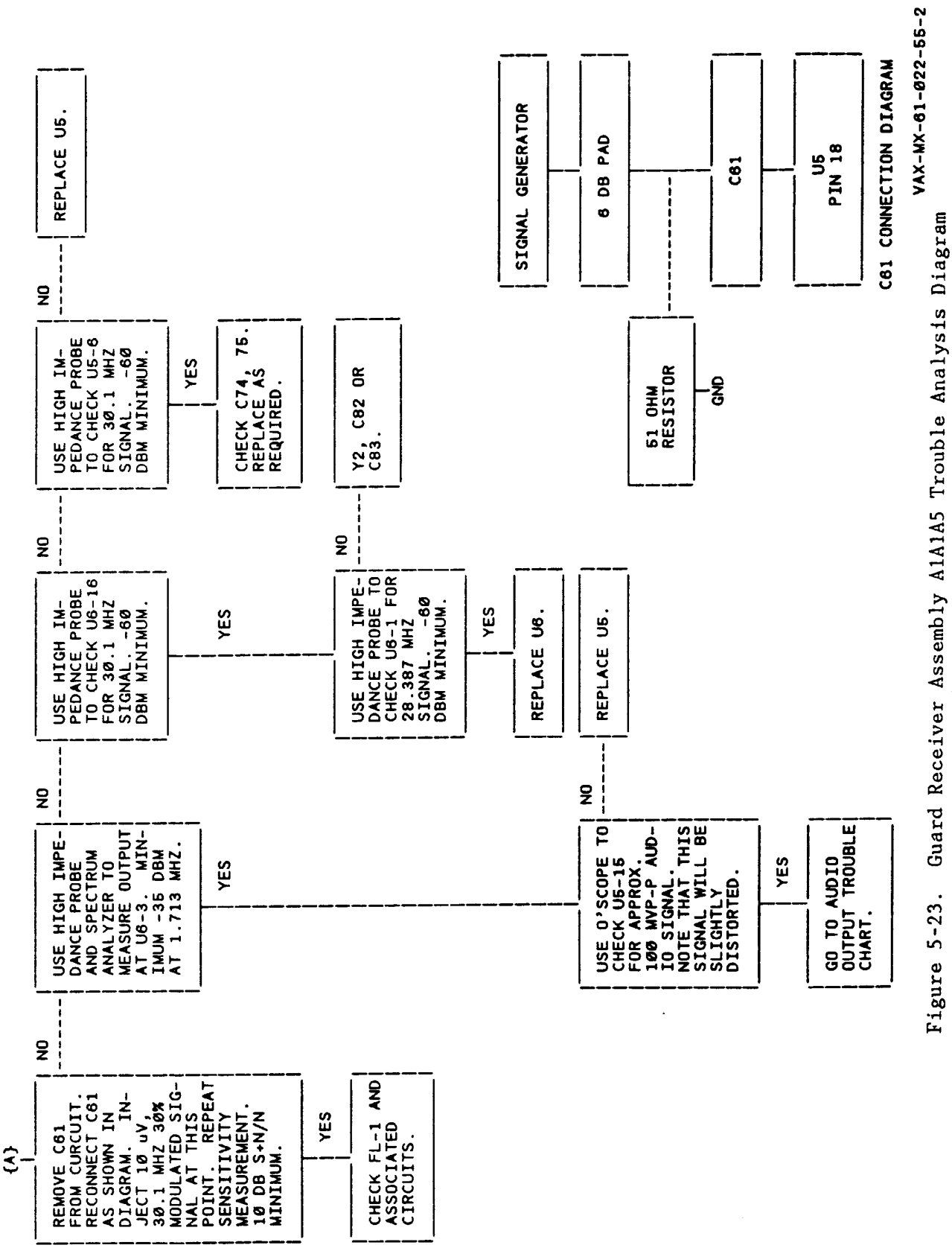
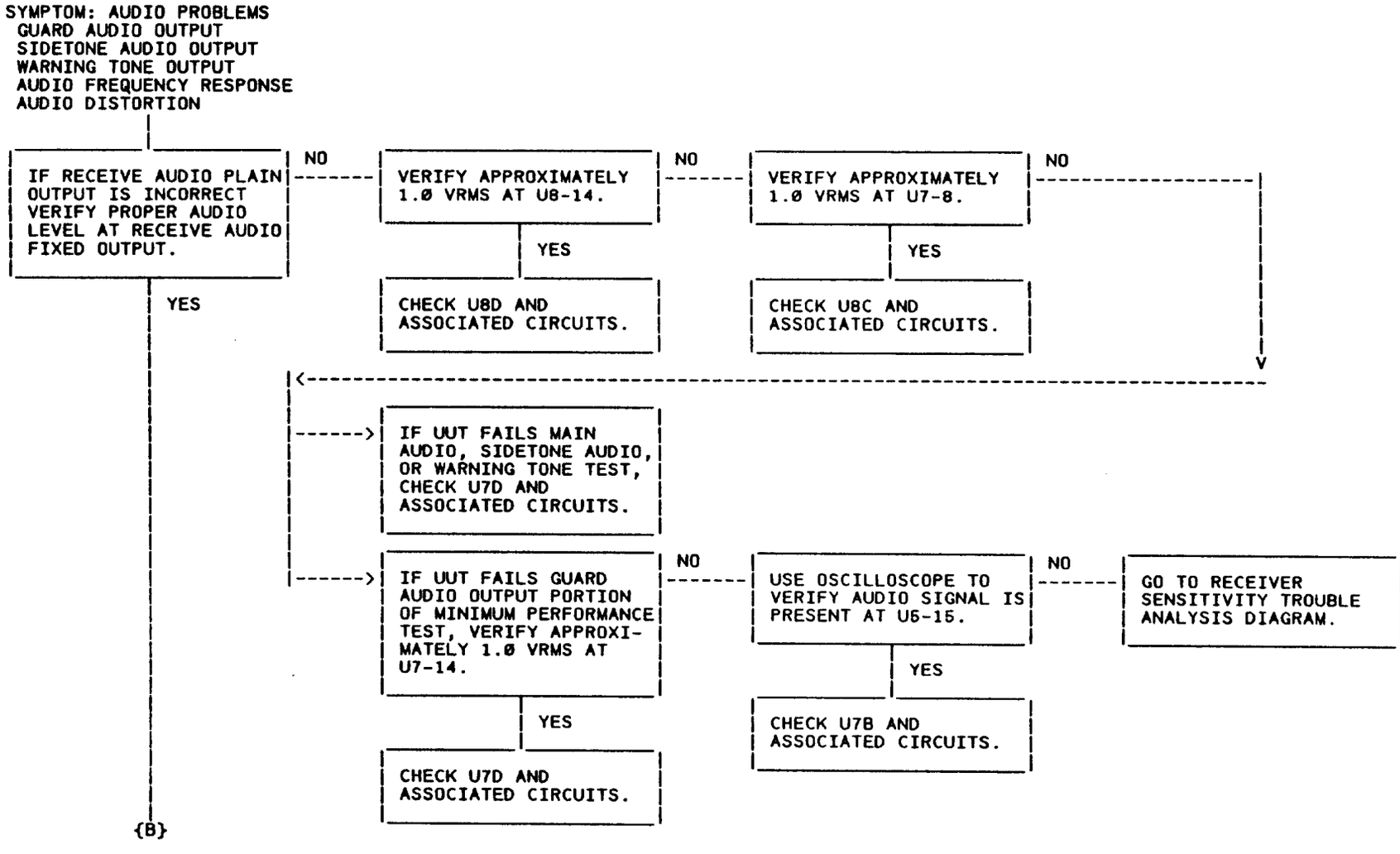


Figure 5-23. Guard Receiver Assembly A1A1A5 Trouble Analysis Diagram (Sheet 2 of 7)



VAX-MX-61-022-55-3

Figure 5-23. Guard Receiver Assembly A1A1A5 Trouble Analysis Diagram
(Sheet 3 of 7)

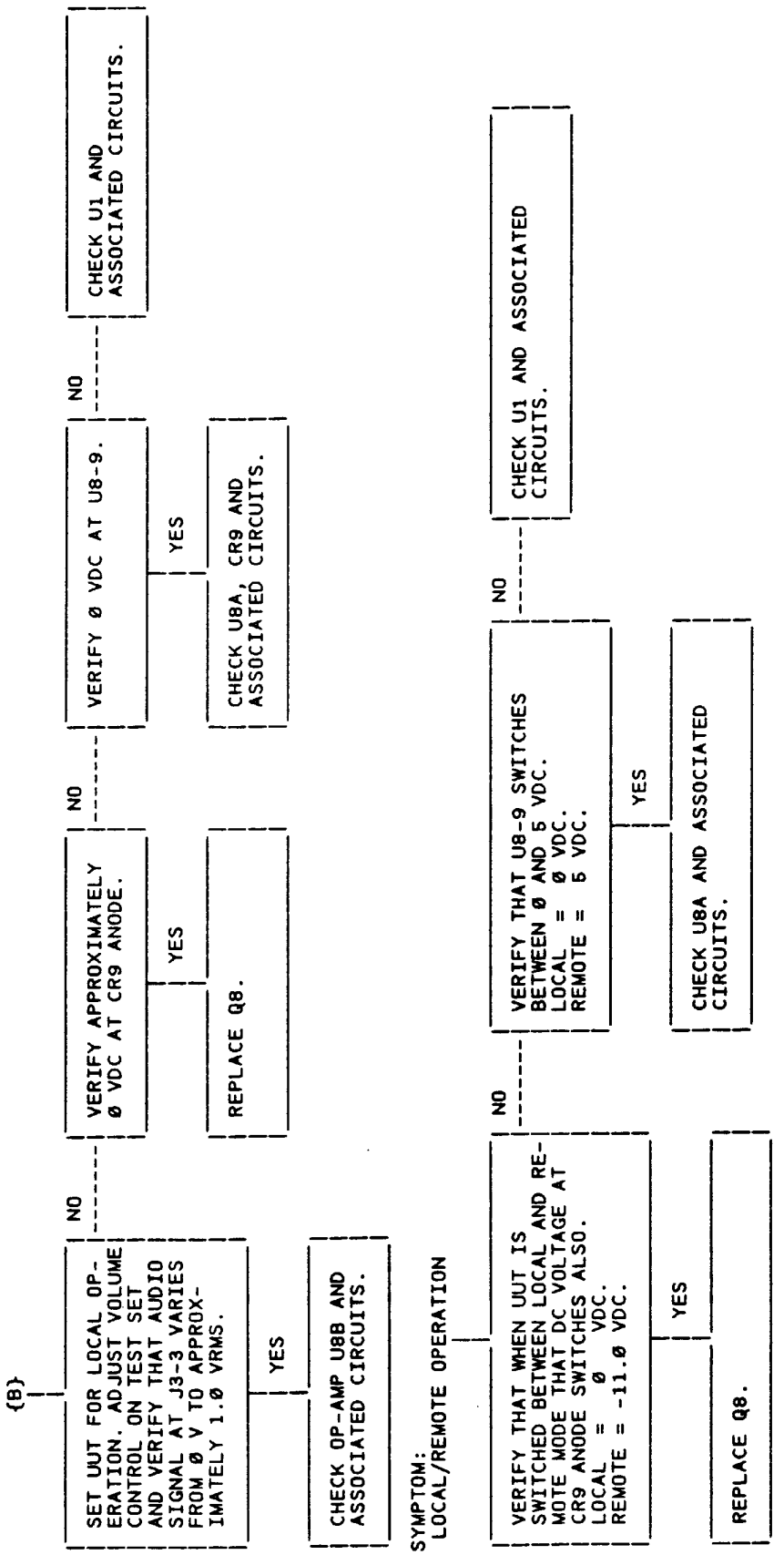
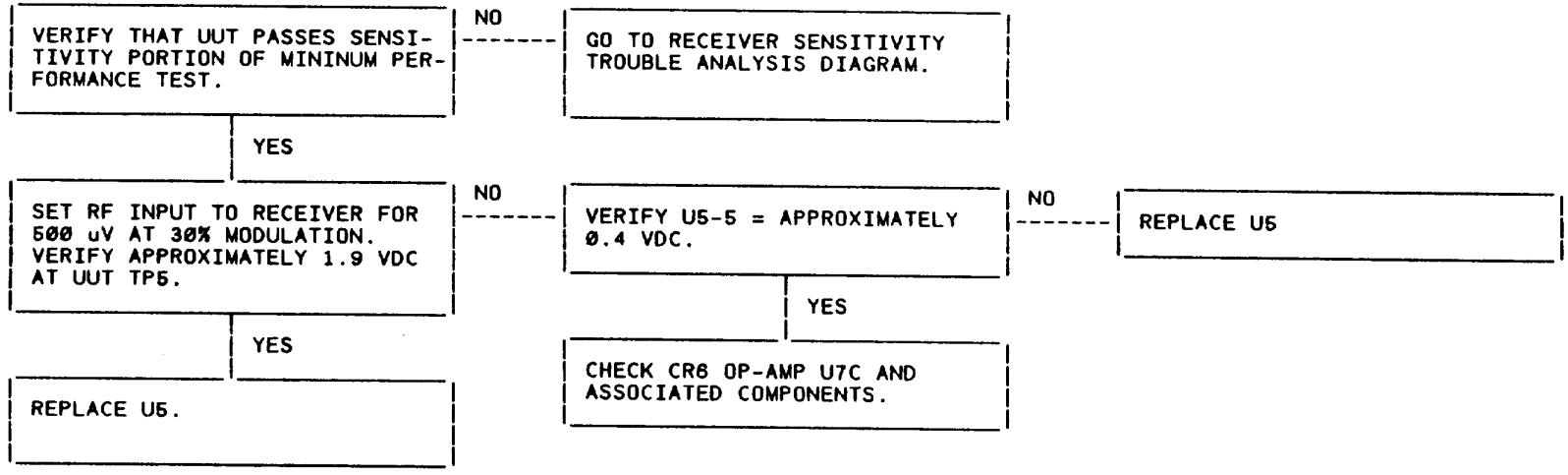


Figure 5-23. Guard Receiver Assembly A1A1A5 Trouble Analysis Diagram (Sheet 4 of 7)

SYMPTOMS:
AGC PROBLEMS



SYMPTOM:
SELECTIVITY

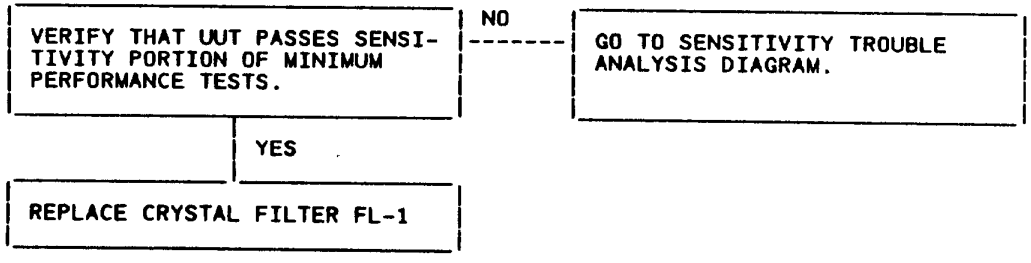
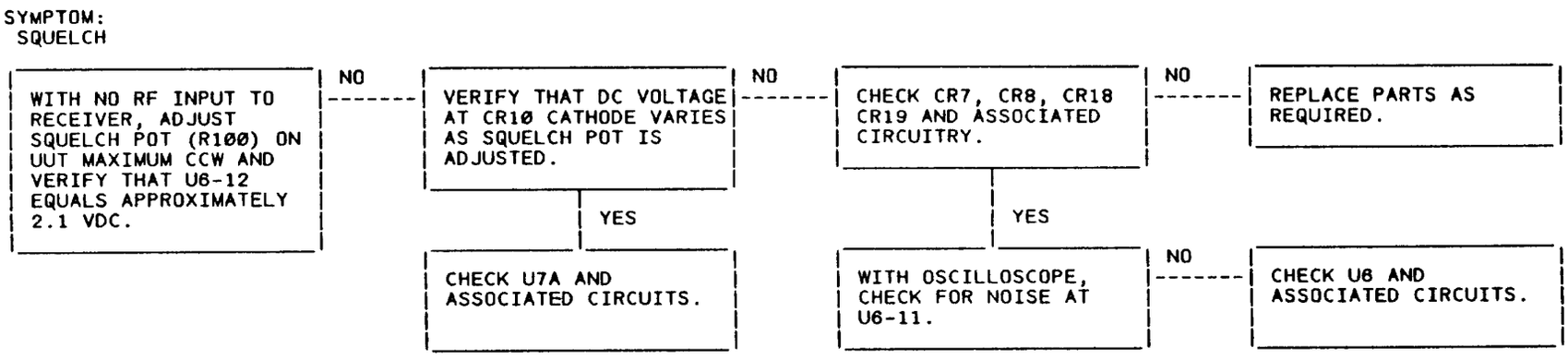


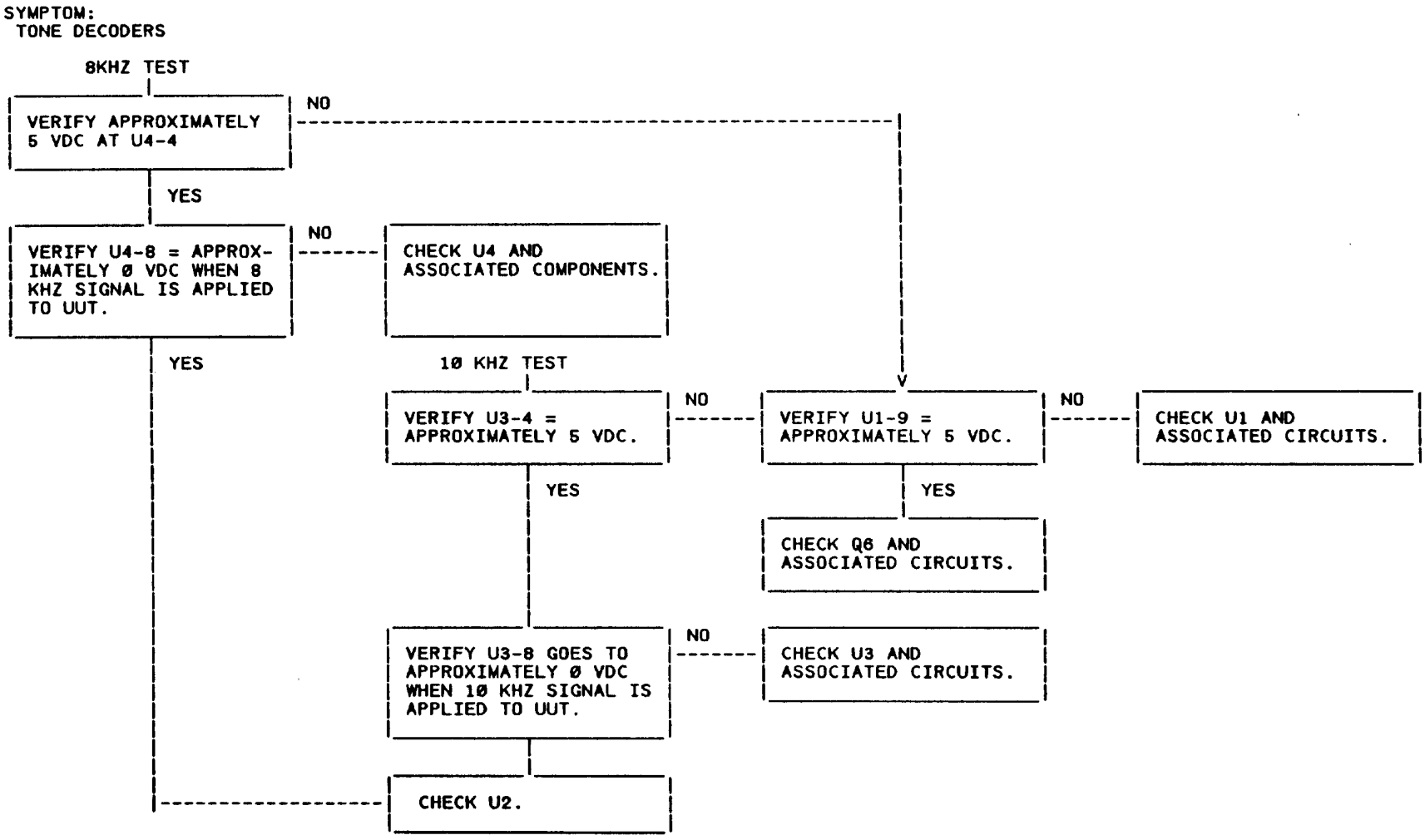
Figure 5-23. Guard Receiver Assembly A1A1A5 Trouble Analysis Diagram (Sheet 5 of 7)

VAX-MX-81-022-55-5



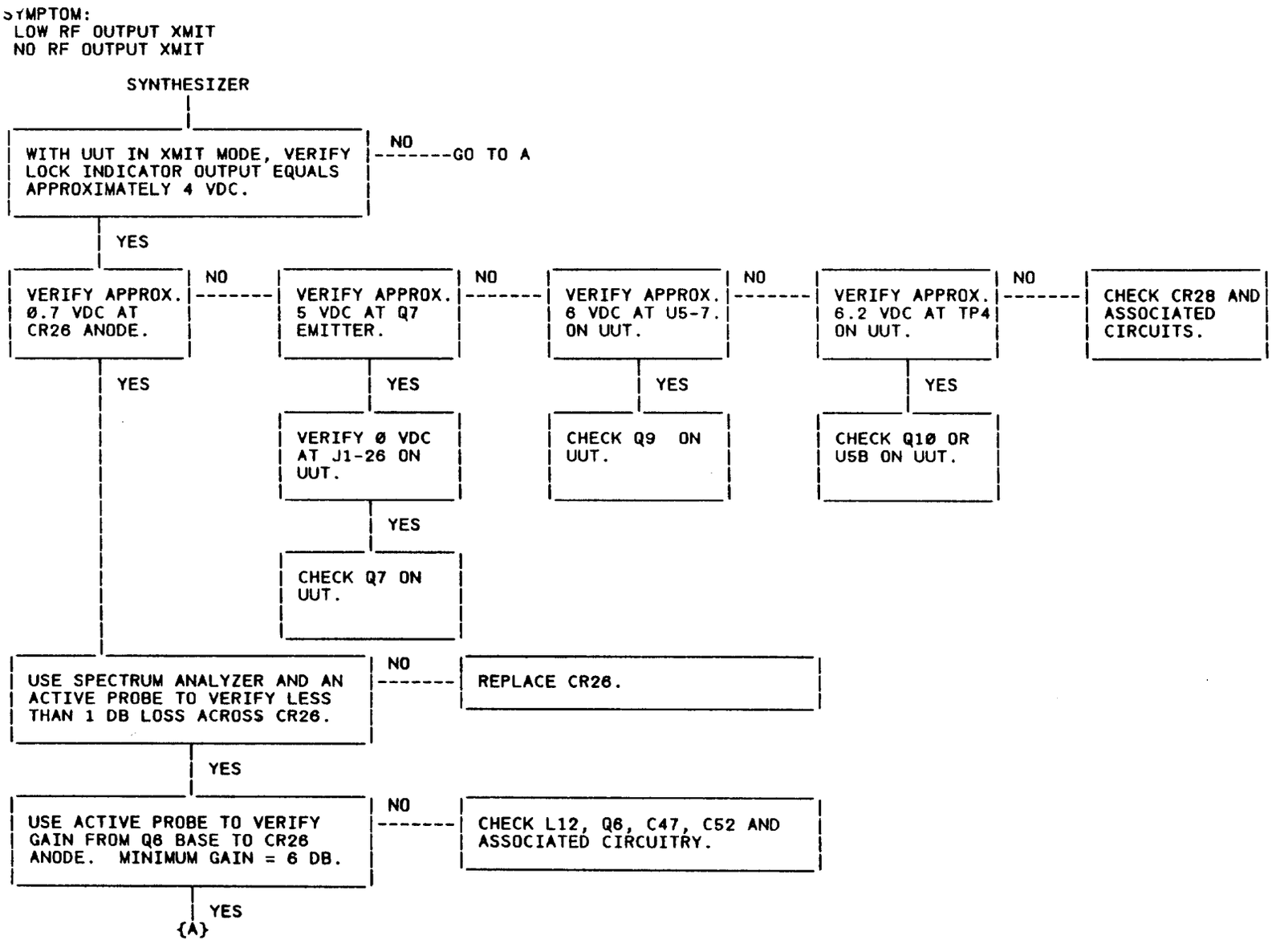
VAX-MX-61-022-55-6

Figure 5-23. Guard Receiver Assembly A1A1A5 Trouble Analysis Diagram
(Sheet 6 of 7)



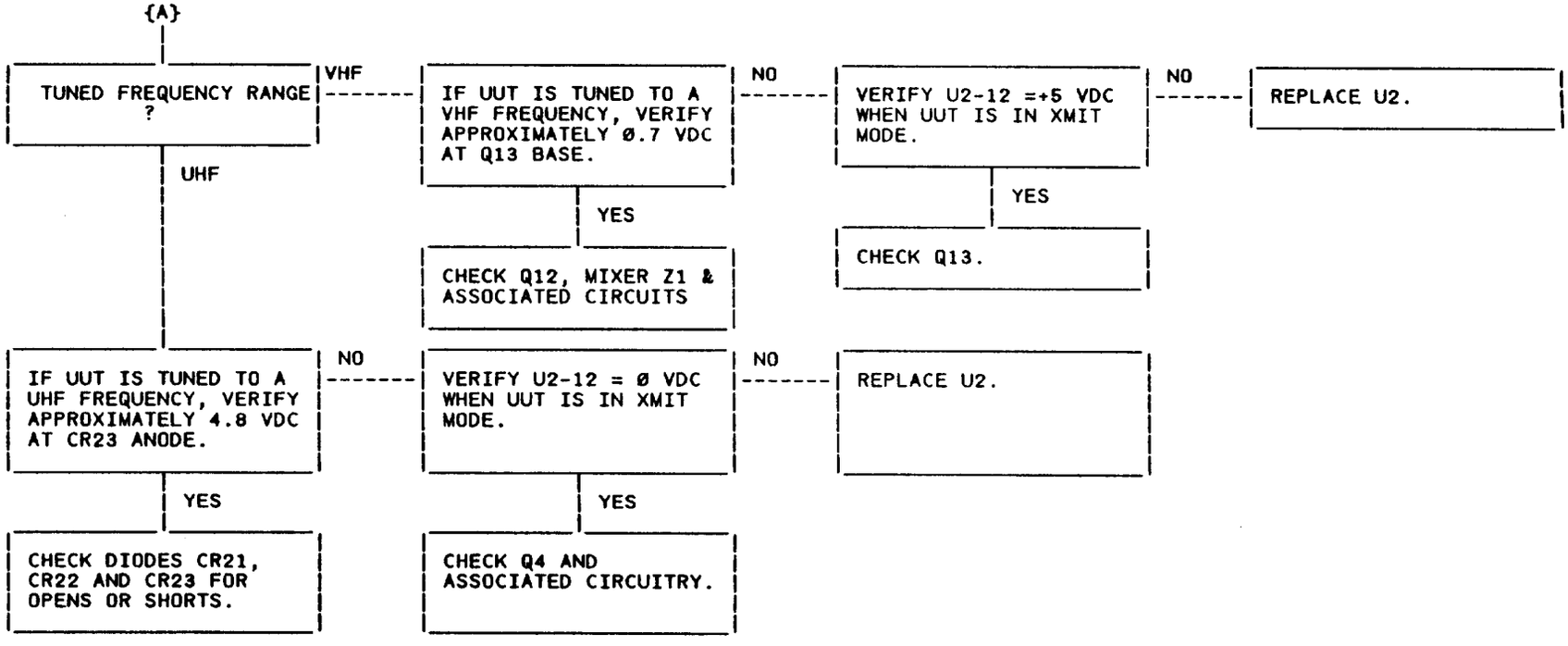
VAX-MX-61-022-55-7

Figure 5-23. Guard Receiver Assembly A1A1A5 Trouble Analysis Diagram
(Sheet 7 of 7)



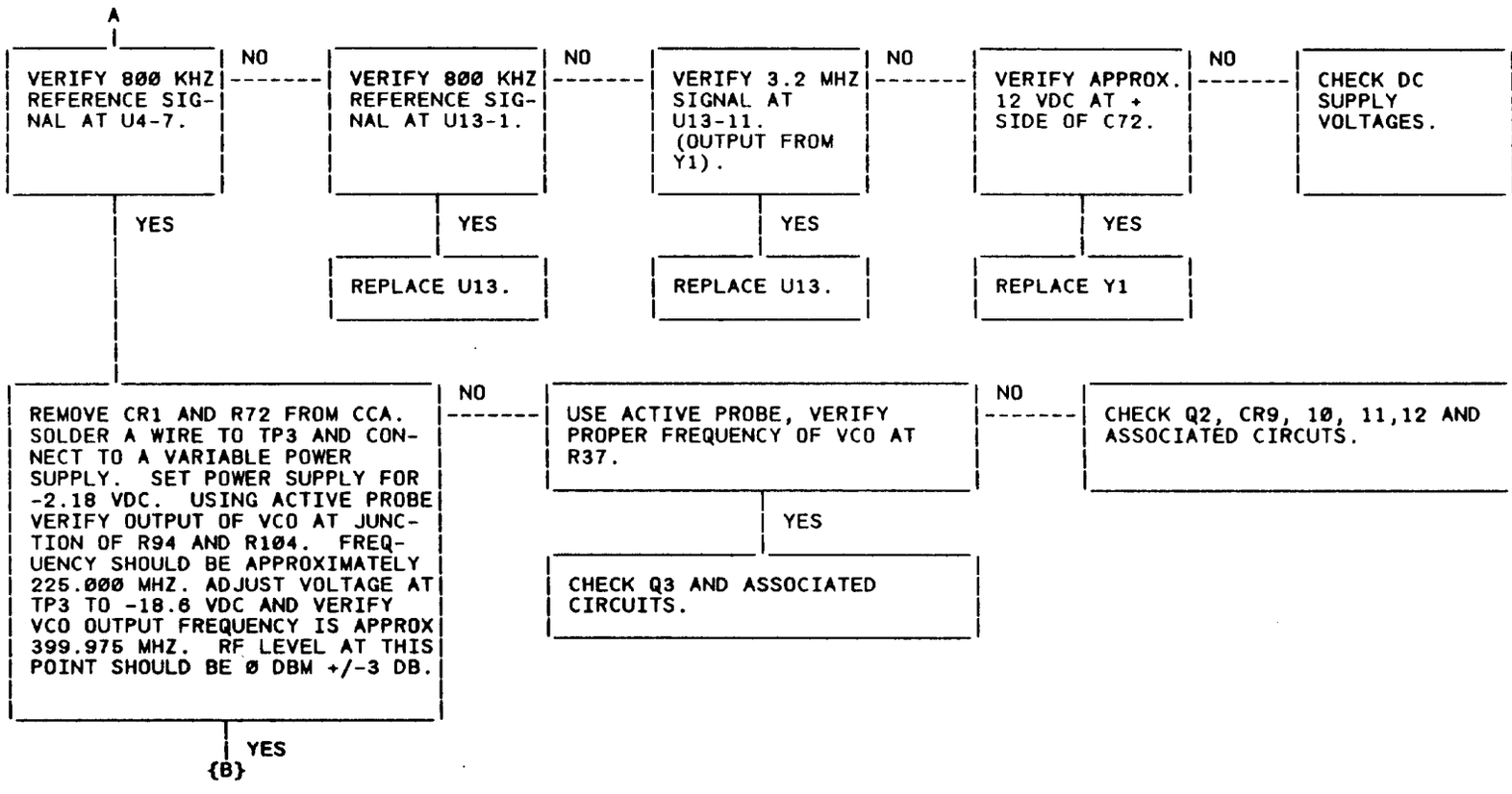
VAX-MX-81-022-56-1

Figure 5-24. Synthesizer Assembly A1A1A6 Trouble Analysis Diagram
(Sheet 1 of 5)



VAX-MX-61-022-56-2

Figure 5-24. Synthesizer Assembly A1A1A6 Trouble Analysis Diagram
(Sheet 2 of 5)



VAX-MX-81-022-56-3

Figure 5-24. Synthesizer Assembly A1A1A6 Trouble Analysis Diagram
(Sheet 3 of 5)

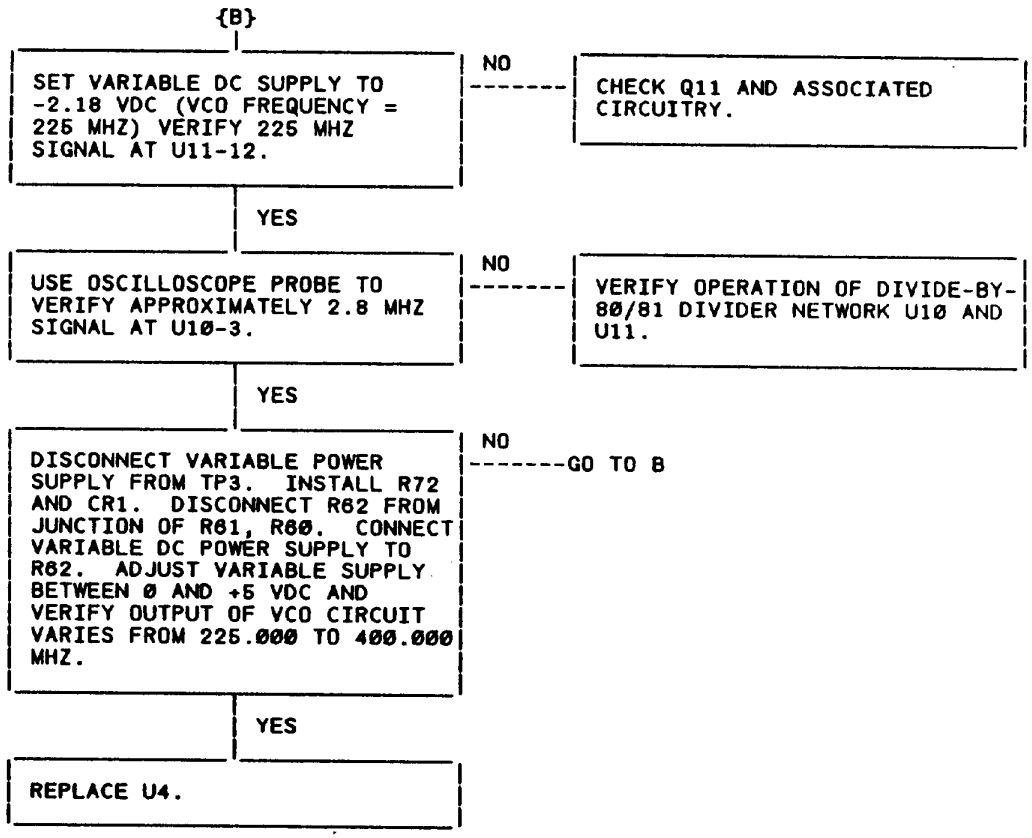
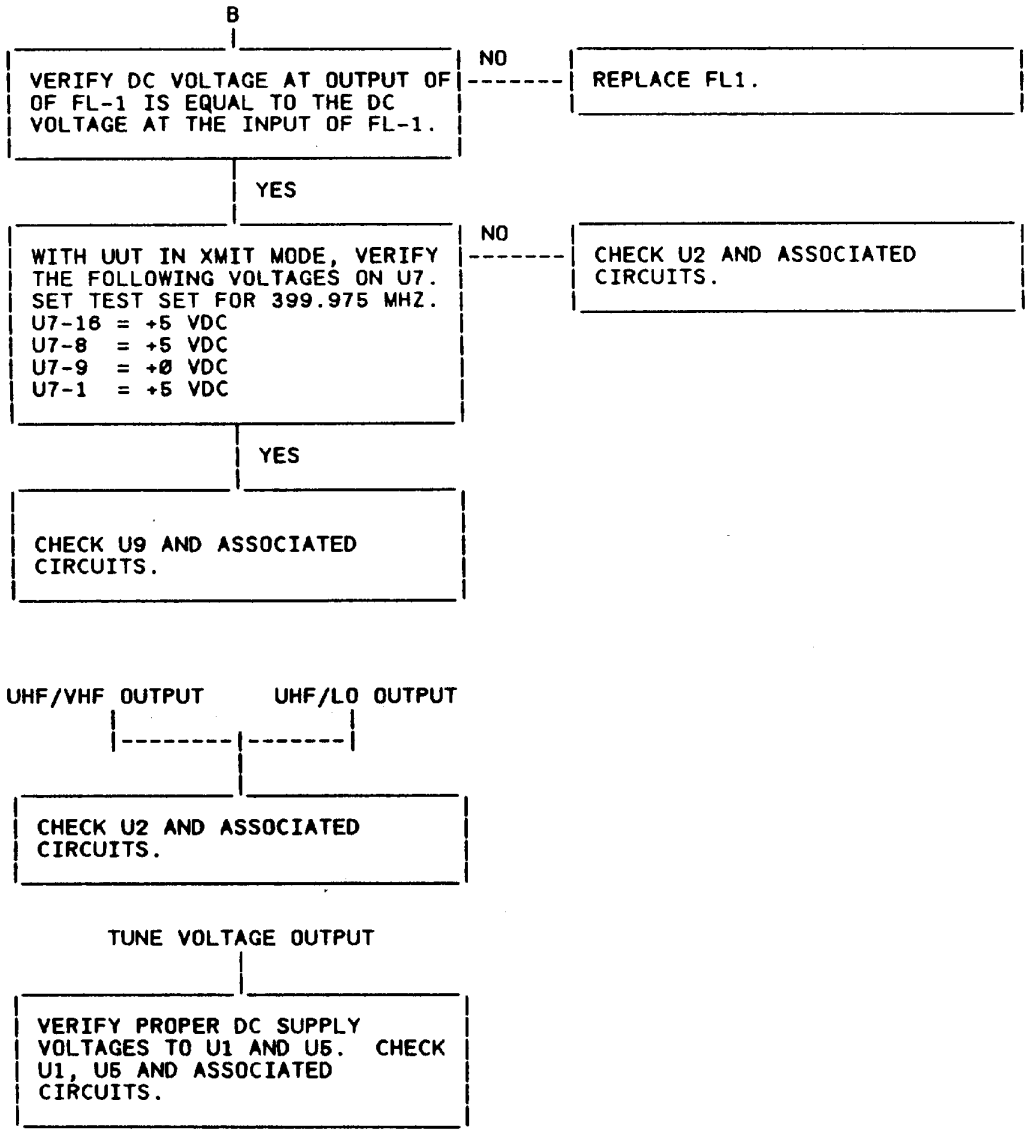


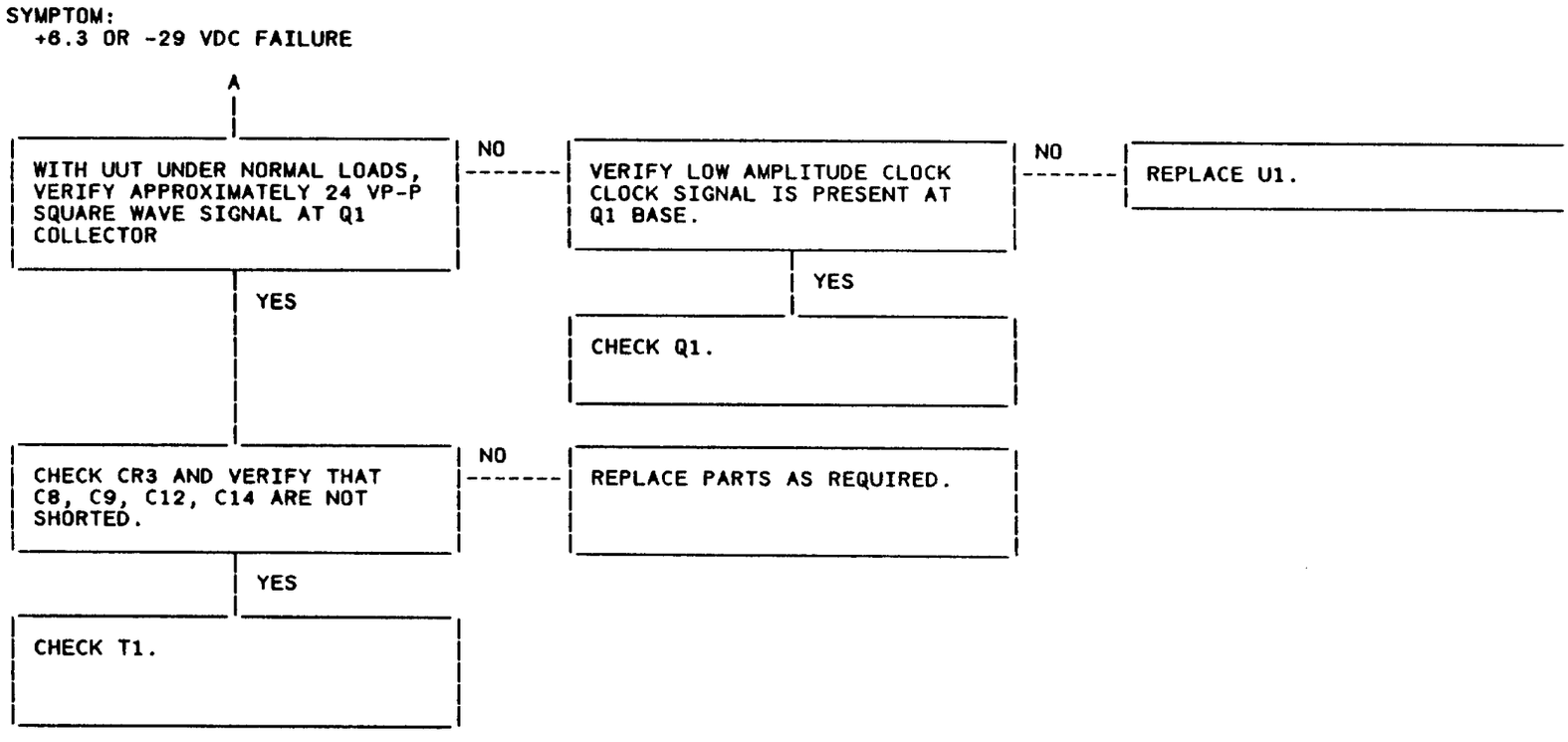
Figure 5-24. Synthesizer Assembly A1A1A6 Trouble Analysis Diagram (Sheet 4 of 5)

VAX-MX-81-022-56-4



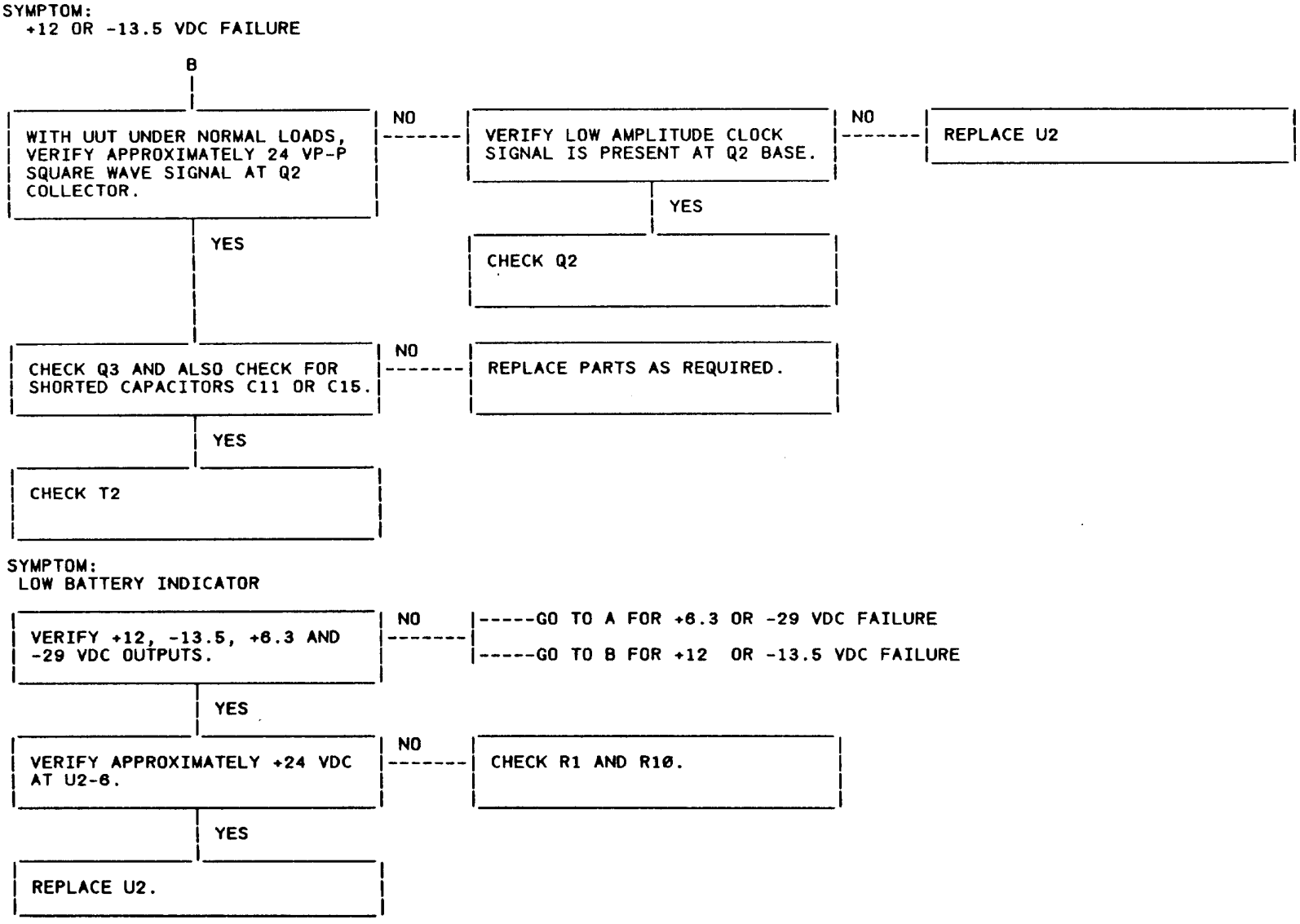
VAX-MX-61-022-56-5

Figure 5-24. Synthesizer Assembly A1A1A6 Trouble Analysis Diagram
(Sheet 5 of 5)



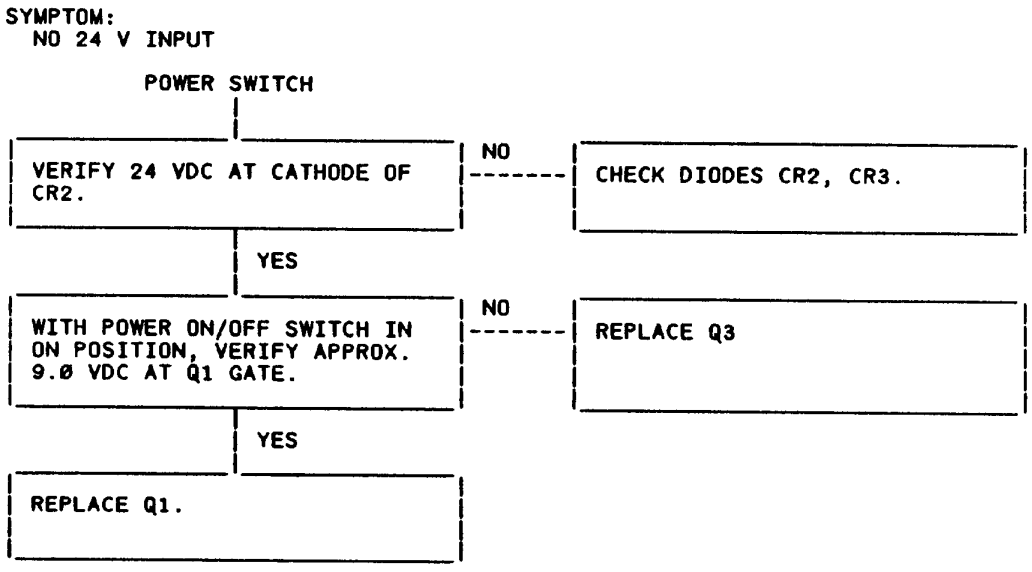
VAX-MX-81-022-57-1

Figure 5-25. Power Regulator Assembly A1A1A7 Trouble Analysis Diagram
(Sheet 1 of 2)



VAX-MX-81-022-57-2

Figure 5-25. Power Regulator Assembly A1A1A7 Trouble Analysis Diagram
(Sheet 2 of 2)



VAX-MX-61-022-58

Figure 5-26. Power Switching Assembly A1A1A9 Trouble Analysis Diagram

CHAPTER 6

CIRCUIT DIAGRAMS

6-1. GENERAL. This chapter contains the circuit and cable assembly diagrams necessary to aid technicians understanding information presented in previous chapters. The diagrams are arranged in the same order as that portion of text to which they pertain. Oversized diagrams are contained in foldout figures located at the rear of this manual.

6-2. INDEX OF DIAGRAMS. Table 6-1 lists oversize foldout figures located at the back of this manual.

Table 6-1. Index of Diagrams

Figure no.	Title
FO-1	RT-1319/URC Receiver-Transmitter A1 Schematic Diagram
FO-2	Data/Converter CCA A1A1A1 Schematic Diagram
FO-3	Interface Data Converter CCA A1A1A1A1 Schematic Diagram
FO-4	Memory I/O Data Converter CCA A1A1A1A2 Schematic Diagram
FO-5	Data Converter-CPU CCA A1A1A1A3 Schematic Diagram
FO-6	Data Converter CCA (LCD) A1A1A1A4 Schematic Diagram
FO-7	Transmitter CCA A1A1A2 Schematic Diagram
FO-8	Modulator CCA A1A1A3A1 Schematic Diagram
FO-9	Main Receiver CCA A1A1A4A1 Schematic Diagram
FO-10	Guard Receiver CCA A1A1A5A1 Schematic Diagram
FO-11	Synthesizer CCA A1A1A1A6A1 Schematic Diagram
FO-12	Power Regulator CCA A1A1A7 Schematic Diagram
FO-13	Electrical Chassis Assembly A1A8 Schematic Diagram
FO-14	Power Switching CCA A1A1A9 Schematic Diagram

CHAPTER 7

SECTION A
INTRODUCTION

7-1. GENERAL. This illustrated Parts Breakdown lists, illustrates and describes the parts used in Receiver-Transmitter RT-1319/URC manufactured by the Magnavox Government and Industrial Electronics Company Fort Wayne, Indiana.

7-2. MAINTENANCE PARTS LIST. The Maintenance Parts List (MPL), (Chapter 7 Section B), consists of the complete Receiver-Transmitter RT-1319/URC divided into main groups. The main groups are broken down into assemblies, subassemblies and details. Each item is arranged to indicate its relationship to its next higher assembly. Each of the assemblies and subassemblies listed is followed immediately by its component parts. The relationship of the first item of each separately illustrated assembly or subassembly to its next higher assembly is indicated followed by the nomenclature of the first item. In general, the assemblies and parts installed at the time the end item was manufactured are listed and identified in the manual. When an assembly or part (including vendor items) which is different from the original was installed during manufacture of the later items, series, or blocks, all assemblies and parts are listed (and "Usable on" coded). However, when the original assembly or part does not have continued application (no spares of the original were procured or such spares are no longer authorized for replacement), only the preferred assembly or part is listed. Also, when an assembly or part was installed during modification, and the original does not have continued application, only the preferred item is listed. Interchangeable and substitute assemblies and parts, subsequently authorized by the Government, are not listed in this manual; such items are identified by information available through the Interchangeable and Substitute (I & S) Data Systems. Refer to T.O. 00-25-184. When a standard size part can be replaced with an oversize or undersize part, the latter parts, showing sizes, are also listed. Repair Parts Kits and Quick Change Units are listed when they are available for replacement.

a. Figure and Index Number Column. This column lists the figure and index number of each part illustrated in the corresponding figure. The index numbers are in numerical sequence and indicate the order of disassembly except where the order of disassembly does not apply. Index numbers identify each part shown in the corresponding figure, with the exception of subassemblies and attaching parts which are not illustrated separately. In these cases they are listed, but not indexed. The component parts of the subassemblies are both listed and indexed. When a group of parts (bolt, washer, nut) is used at a specific location for attachment purposes, one index number assigned to the group is sufficient. The index number appears on the same line as the first part composing the group.

b. Part Number Column. This column lists the contractor's drawing number (Part Number) including dash numbers, assigned to each part and vendor part numbers of parts used by the contractor exactly as produced by the respective vendor. Those parts which have Government Standards numbers assigned to them have the Government Standards number listed. Parts altered or selected for special fit, tolerance, etc., from vendor, commercial or government standard items have contractor part numbers. The vendor, commercial or Government Standards part number of the altered or selected part follow the part description in the Description column. Alternate

vendor items, installed during manufacturing or modification, will be listed and identified as alternate by an (=) sign preceding the part number one space to the left.

Item(s) of supply part number(s) and FSCM that is stocked; stored and issued by the Government as identified by the Government during the initial provisioning process shall be identified by an (*) sign preceding the part number one space to the left. Select at test items installed during manufacturing or modification, will be listed and identified as selected by an (+) sign preceding the part number one space to the left. Government Furnished Equipment (GFE) and Contractor Furnished Equipment (CFE), covered by separate manuals will be listed and identified by a number sign (#) inserted flush right following the part number. Decalcomania, metalcals, and vinyl film marking. The part number for each marking appears in the part number column (flush right and is identified by an asterisk (*) sign and this symbol means "requestion the marking in accordance with the requirements of ARF6-1."

c. FSCM Column. This column list a 5-digit code number denoting the vendor from whom the part may be procured is shown following the part number. The source of vendor code numbers is the Federal Supply Code for Manufacturers (FSCM) Cataloging Handbook H4-1 H4-2 and H4-3.

d. Description Column. This column contains the description of all item appearing on the Maintenance Parts List. The indentation headed "1" through "7", in this column shows the relationship of parts and subassemblies to assemblies. The description consists of the approved item name, as found in the Federal Item Identification Guide for Supply Cataloging Handbook H6-1, or are in accordance with the contractor's drawing title, plus modifiers that are necessary to identify the particular item. Additional information may follow the item description and list of alternate part numbers, as required to give stock ordering information, exceptions to the Usable On Code for the item, references to preceding subsequent figures concerning assemblies and subassemblies, etc. These data are to be considered an integral part of the item description to assure the correctness of repair maintenance procedures. Item(s) identified as a Hardness Critical Item (HCI), the marking HCI (reference DOD-STD-100) shall precede the first word in the Description column.

e. Attaching Parts. These are items used to attach parts or assemblies to each other and are listed immediately after the part to be attached. The attaching parts have the same indentation code as the parts attached. The code (AP) appears on the same line with and immediately following the item identified as an attaching part.

f. Units Per Assembly. This column contains the number of units required per assembly and/or subassembly. If more than one assembly is required, the total number of assemblies is listed. When an assembly or subassembly is listed more than once, the total number of units per assembly or subassembly appears the first time and REF for subsequent listings.

g. Usable On Code. This column shows the Usable On Codes for systems, assemblies and parts to indicate specific usability by part number. Explanations of the usable on codes are provided at the bottom of the applicable page. The codes A, B, C etc., when shown within a group relate the part back to the same coded part within the next higher assembly. When this column is left blank, an assembly or part is common to all part number variations of the next higher assembly.

h. Source, Maintenance and Recoverability SMR Codes. This manual contains Joint Military Services Uniform SMR Codes. Detailed coding criteria may be obtained from T.O. 00-25-195.

7-3. NUMERICAL INDEX. The Numerical Index (Chapter 7 Section C) is compiled in accordance with the numerical part number filing system described in paragraph a.

a. Part Number Column. This column contains all the part numbers that appear in the Maintenance Parts List and part numbers that have been assigned to detail parts assembled into the end article. The order of procedure establishing the sequence in which the part numbers are listed is explained below. The order of precedence in the first position of each part number is Letters A through Z, Numerals 0 through 9.

NOTE

Alphabetical 0's are considered as numerical zeroes in all positions in each part number.

The order of precedence in the second and succeeding positions in each part number is as follows:

(1) Space (blank column).
(2) Diagonal (/).
(3) Period (.).
(4) Dash (-).
(5) Letters A through Z.
(6) Numerals 0 through 9.

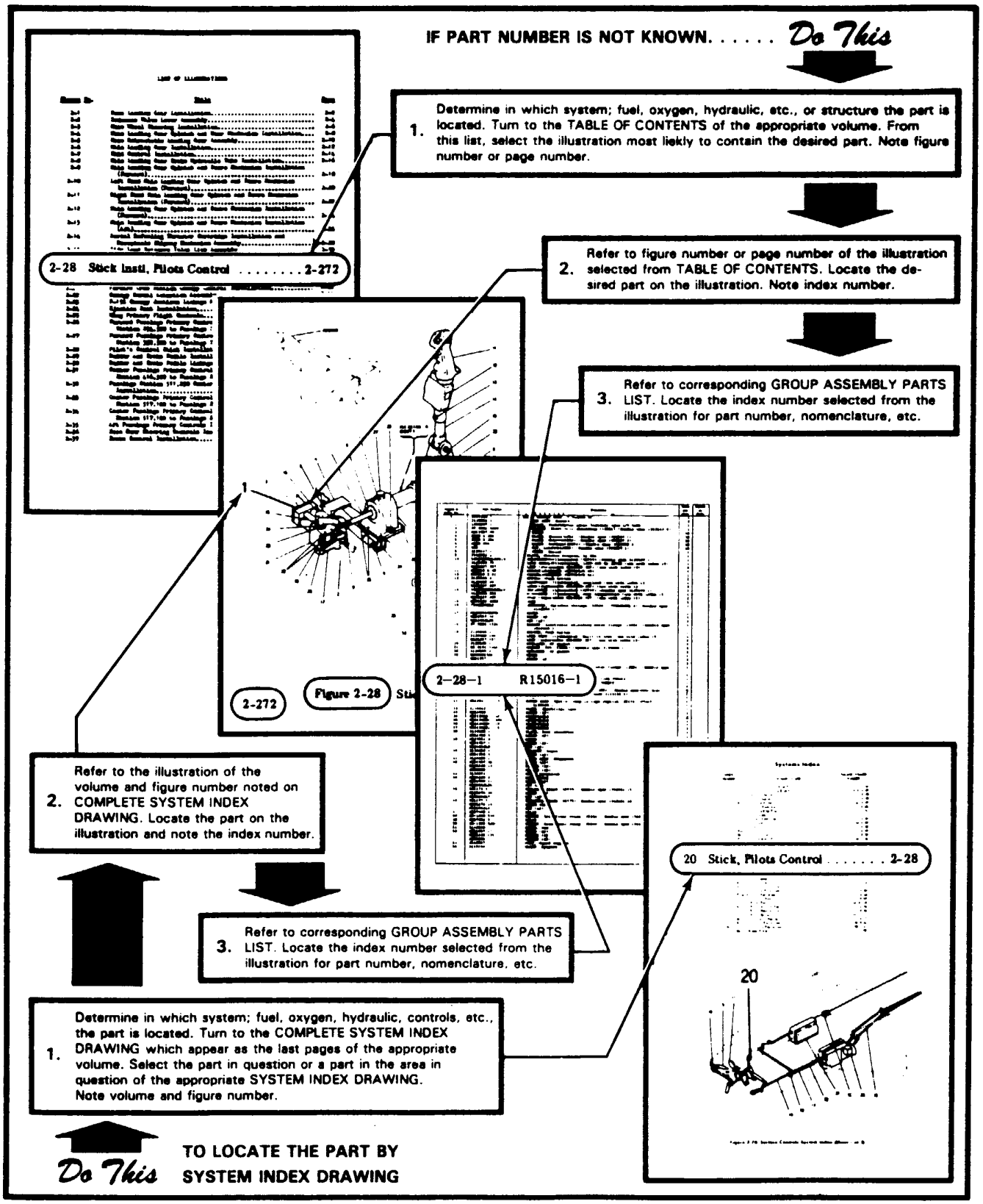
The following is a sample of part numbers arranged in sequence used in the Numerical Index.

AN931-4-13	B2	16.W2
A2460	S/1	16W060
A317	1140	32P010-1
A32	121873	32P0101
B12	128	39A45

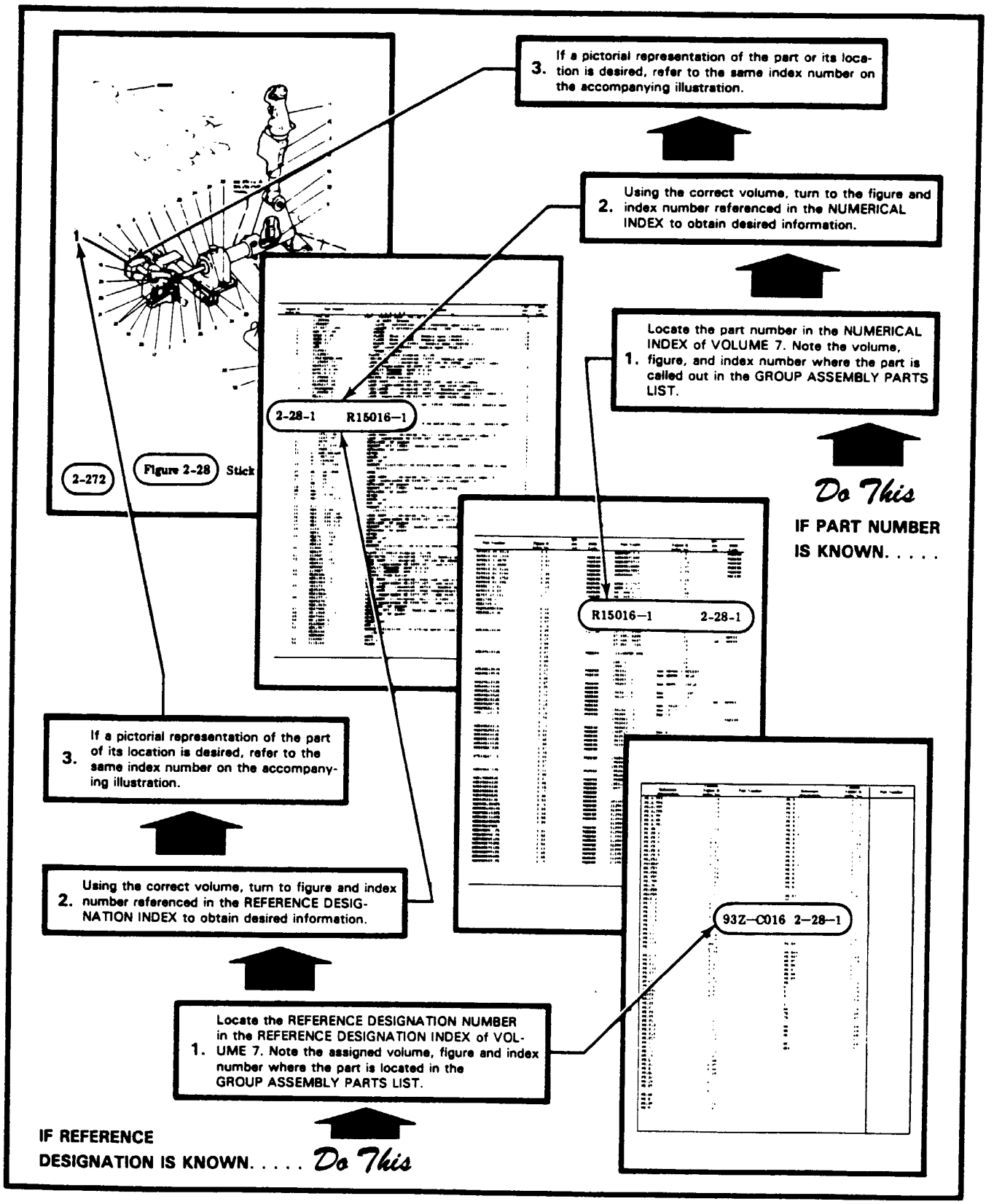
b. Figure and Index Number Column. For each part number, the figure or figure and index number refers to the Maintenance Parts List where parts relationship is shown. For government standard parts and contractor standard parts only, the first figure and index number that occurs will be listed. When an assembly or part has not been assigned in index number, the figure and index number of the preceding part in the Maintenance Parts List is used with the letter "F" before the figure number, such as F7-6. The letter "F" denotes "follows".

7-4. REFERENCE DESIGNATION INDEX. The Reference Designation Index (Chapter 7 Section D) lists, in alphabetical-numerical order, the reference designations used in schematic diagrams and instruction books. Opposite the reference designation is listed the figure index number as shown in the Maintenance Parts List.

HOW TO USE THIS ILLUSTRATED PARTS BREAKDOWN



HOW TO USE THIS ILLUSTRATED PARTS BREAKDOWN



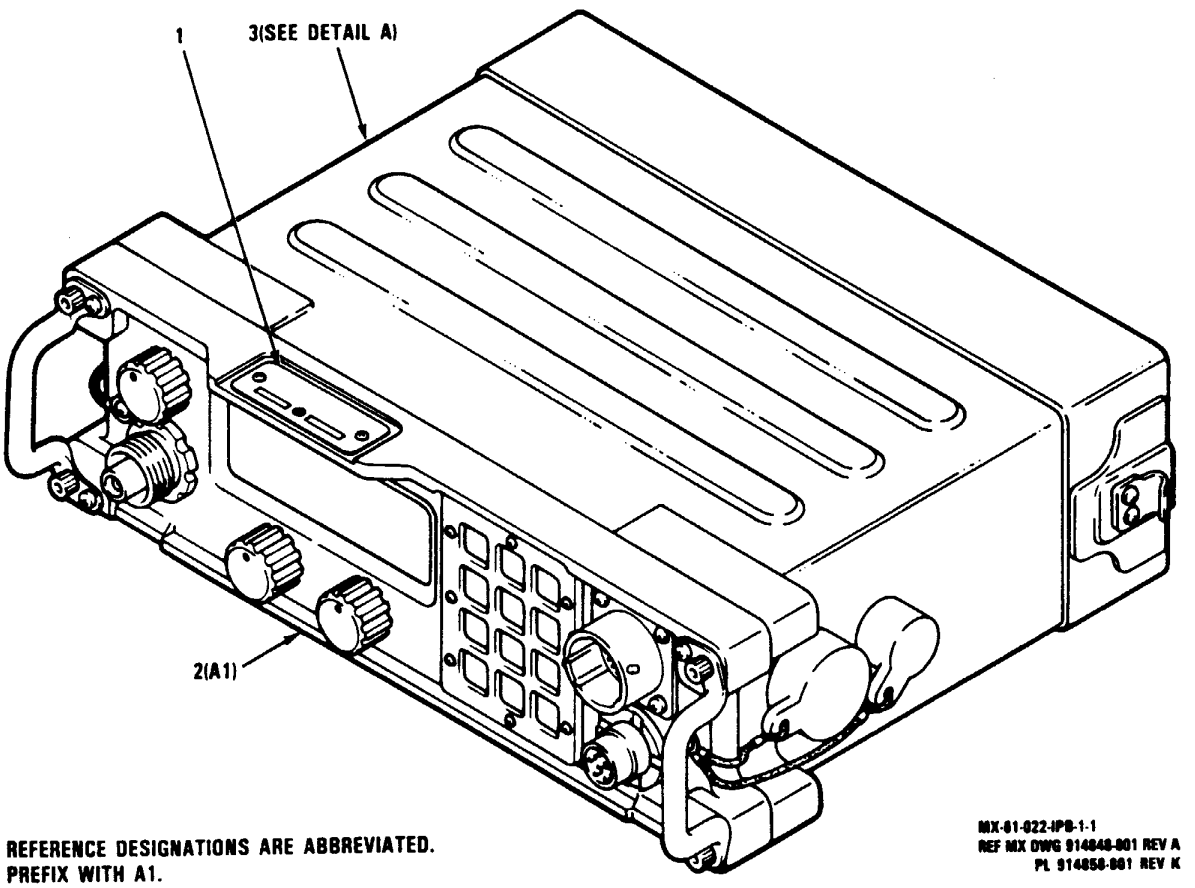


Figure 7-1. RT-1319/URC Receiver-Transmitter (Sheet 1 of 2)

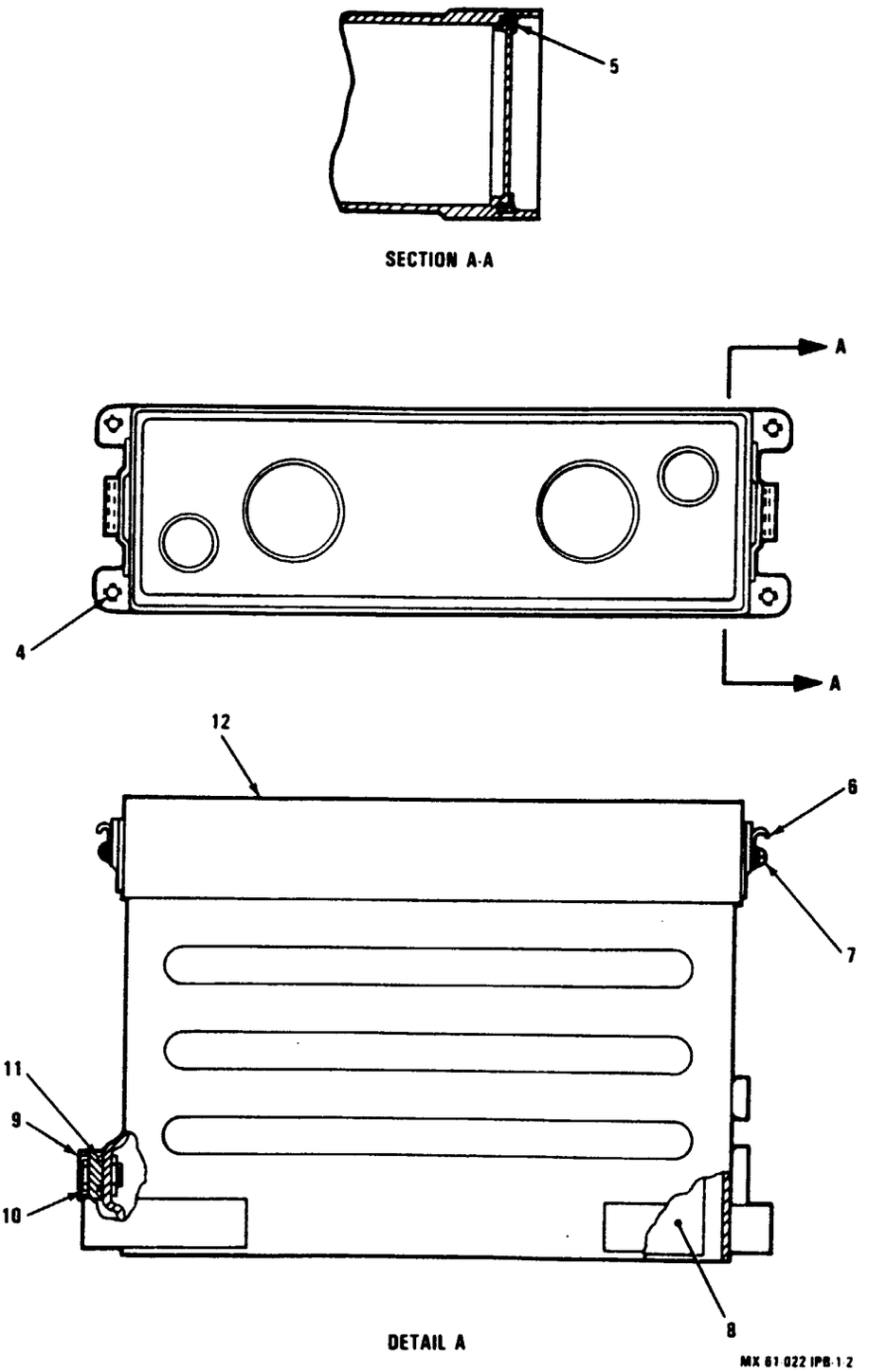


Figure 7-1. RT-1319/URC Receiver-Transmitter (Sheet 2 of 2)

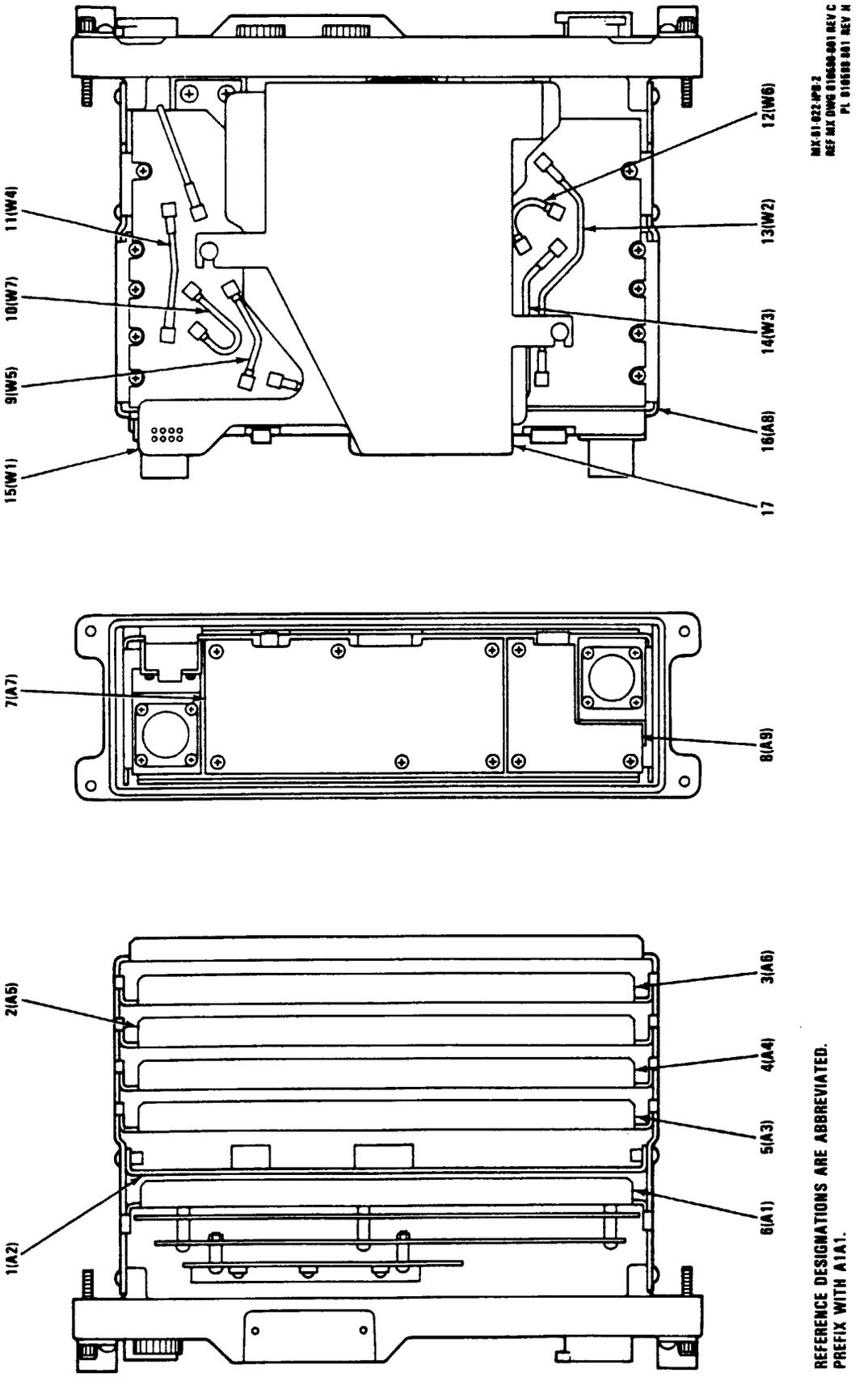


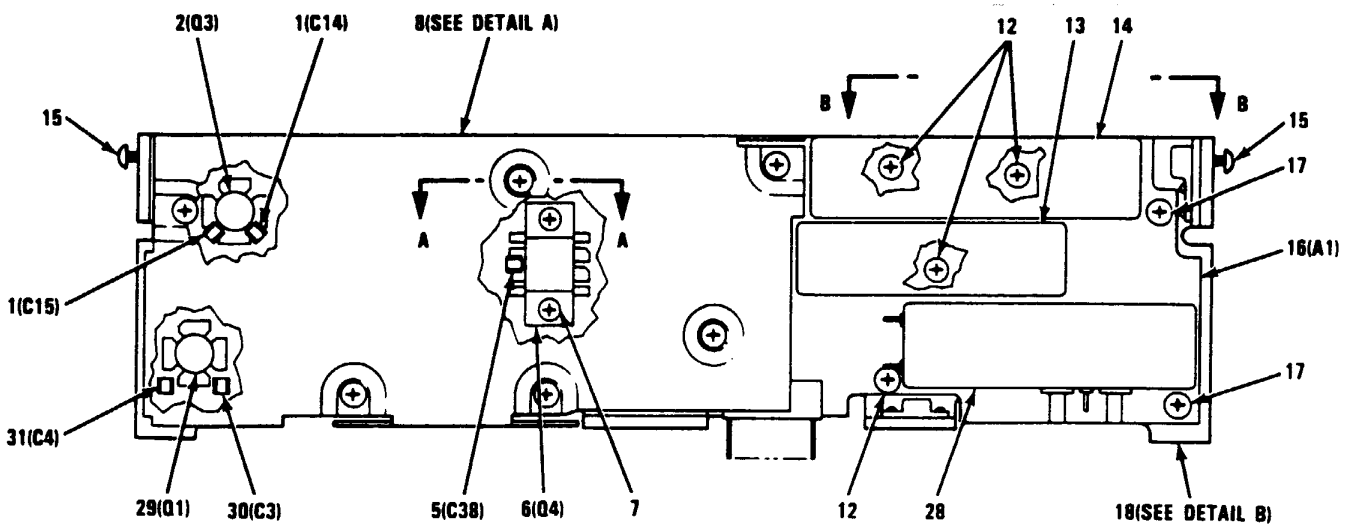
Figure 7-2. Radio Assembly

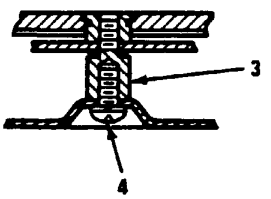
CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN
SECTION B
MAINTENANCE PARTS LIST

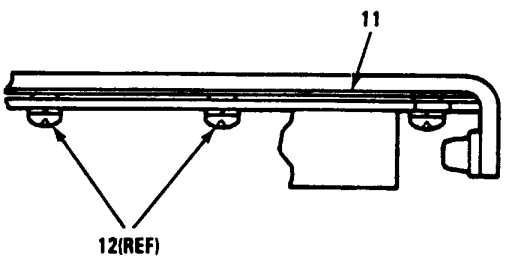
FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 1-	914858-801	37695	RECEIVER/TRANSMITTER, ... RT-1319/URC	1		PAODD
- 1	155896- *	37695	. PLATE, Identification	1		MD
	MS51957-11B	96906	. SCREW (AP)	2		PAFZZ
- 2	810598-801	37695	. RADIO ASSEMBLY ..... (See fig. 2 for bkdn)	1		XA
- 3	914868-801	37695	. CASE, Radio assembly	1		XB
- 4	MS21209F1-20L	96906	. . INSERT	4		PAFZZ
- 6	125249-102	37695	. . LATCH ASSEMBLY	2		PAFZZ
- 7	MS51957-26B	96906	. . SCREW (AP)	2		PAFZZ
	MS35338-136B	96906	. . WASHER (AP)	2		PAFZZ
- 8	348918-1	37695	. . INSULATOR, Flex ..... circuit	2		PAFZZ
- 9	515032-1	37695	. . BUSHING	1		PAFZZ
- 10	MS3213-31	96906	. . SCREW (AP)	1		PAFZZ
	MS25082C20	96906	. . NUT (AP)	1		PAFZZ
- 11	MS9068-013	96906	. . PACKING	1		PAFZZ
- 12	936698-1	37695	. . CASE, Radio	1		XB
7- 2-	810598-801	37695	RADIO ASSEMBLY ..... (See fig. 1 for nha)	REF		XA
- 1	914862-801	37695	. TRANSMITTER ASSEMBLY ..... (See fig. 3 for bkdn)	1		PAFLD
- 2	811955-801	37695	. RECEIVER ASSEMBLY, Guard . (See fig. 6 for bkdn)	1		PAFLD
- 3	811829-801	37695	. SYNTHESIZER ASSEMBLY ..... (See fig. 8 for bkdn)	1		PAFLD
- 4	811826-801	37695	. RECEIVER ASSEMBLY ..... (See fig. 10 for bkdn)	1		PAFLD
- 5	811827-801	37695	. MODULATOR ASSEMBLY ..... (See fig. 12 for bkdn)	1		PAFLD
- 6	914861-801	37695	. CONTROL/DATA CONVERTER ... ASSEMBLY (See fig. 14 for bkdn)	1		PAFLD

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 2- 7	914874-801	37695	. CIRCUIT CARD ASSEMBLY, ... Power regulator (See fig. 19 for bkdn)	1		PAFLD
- 8	811963-802	37695	. CIRCUIT CARD ASSEMBLY, ... Power switching (See fig. 20 for bkdn) (Preferred item)	1		
	811963-801	37695	. CIRCUIT CARD ASSEMBLY, ... Power switching (See fig. 20 for bkdn) (Alternate item)	1		PAFLD
- 9	569342-803	37695	. CABLE ASSEMBLY	1		PAFZZ
- 10	569342-802	37695	. CABLE ASSEMBLY	1		PAFZZ
- 11	565947-803	37695	. CABLE ASSEMBLY	1		PAFZZ
- 12	569342-801	37695	. CABLE ASSEMBLY	1		PAFZZ
- 13	565947-801	37695	. CABLE ASSEMBLY	1		PAFZZ
- 14	565947-802	37695	. CABLE ASSEMBLY	1		PAFZZ
- 15	566102-801	37695	. CABLE ASSEMBLY	1		PAFZZ
- 16	914860-801	37695	. CHASSIS ASSEMBLY, ... Electrical (See fig. 21 for bkdn)	1		XB
- 17	349127-1	37695	. CIRCUIT INSULATOR, Flex ..	1		PAFZZ
7- 3-	914862-801	37695	TRANSMITTER ASSEMBLY ..... (See fig. 2 for nha)	REF		PAFLD
- 1	CDR14BG680EGSM	81349	. CAPACITOR	2		PADZZ
=	ATC-100-B-680-G-P-500-SP	29990	. CAPACITOR, Fixed, glass .. dielectric (Magnavox spec cont dwg 258300-11357)	2		PADZZ
- 2	615467-905	37695	. TRANSISTOR	1		PADZZ
	NAS620C8L	80205	. WASHER (AP)	1		PADZZ
	MS25082C2	96906	. NUT (AP)	1		PADZZ
- 3	515004-1	37695	. POST, Mechanical ..... - electrical	6		XB
- 4	MS51957-12	96906	. SCREW (AP)	1		PADZZ
	MS35338-135	96906	. WASHER (AP)	2		PADZZ
- 5	258300-11351	37695	. CAPACITOR, Fixed, glass .. dielectric	1		
- 6	645512-903	37695	. TRANSISTOR, RF power	1		PADZZ
- 7	MS51957-13	96906	. SCREW (AP)	2		PADZZ
	MS35338-135	96906	. WASHER (AP)	2		PADZZ
	NAS620C4	80205	. WASHER (AP)	2		PADZZ





SECTION A-A

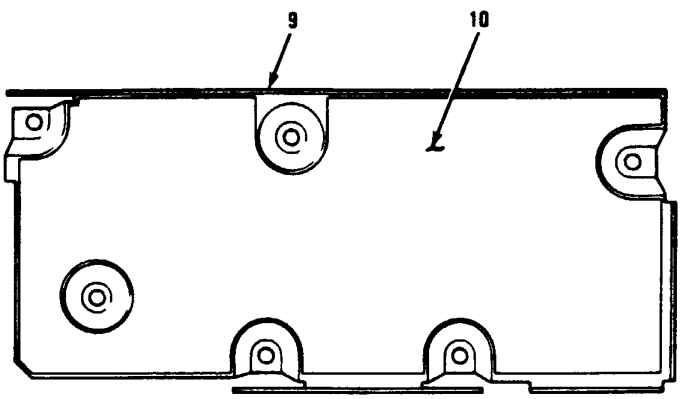


VIEW B-B

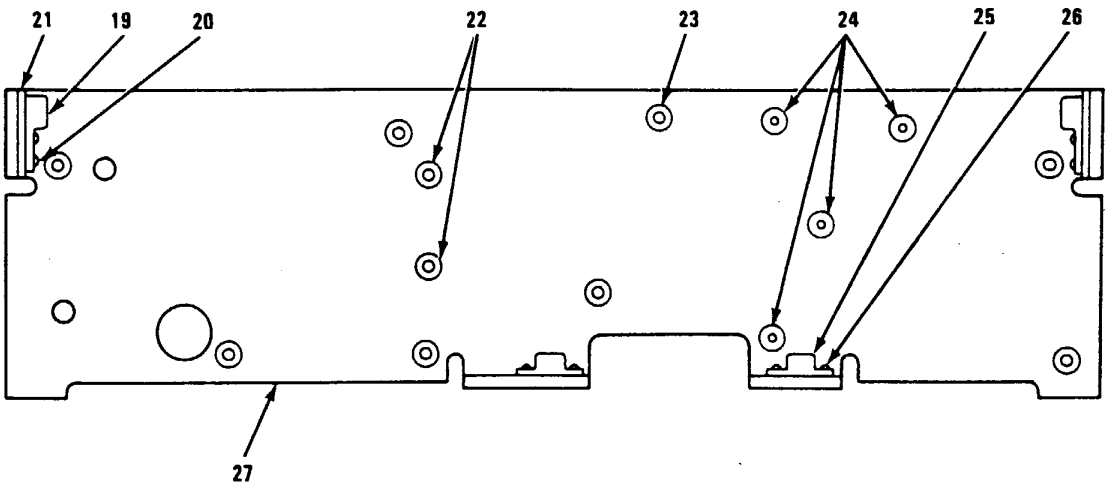
REFERENCE DESIGNATIONS ARE ABBREVIATED.
PREFIX WITH A1A1A2.

MX-81-022-IPB-3-1
REF MX DWG 914882-881 REV F
PL 914882-881 REV W

Figure 7-3. Transmitter Assembly (Sheet 1 of 2)



DETAIL A



DETAIL B

MX-81-022-IPB-3-2

Figure 7-3. Transmitter Assembly (Sheet 2 of 2)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 3- 8	939192-801	37695	. HOUSING ASSEMBLY, ... Shield	1		XB
- 9	939492-1	37695	. . HOUSING, Shield	1		XB
- 10	349034-1	37695	. . INSULATOR, Shield	1		XB
- 11	348500-1	37695	. INSULATOR, Transistor	1		PADZZ
- 12	MS51957-3	96906	. SCREW (AP)	4		PADZZ
	MS35338-134	96906	. WASHER (AP)	4		PADZZ
- 13	939012-2	37695	. HOUSING, Shield	1		XB
- 14	939012-1	37695	. COVER, Shield	1		XB
- 15	MS51957-29B	96906	. SCREW	2		PAFZZ
- 16	914873-801	37695	. CIRCUIT CARD ASSEMBLY, ... Transmitter (See fig. 4 for bkdn)	1		PAFLD
- 17	MS51957-13	96906	. SCREW (AP)	2		PAFZZ
	MS35338-135	96906	. WASHER (AP)	2		PAFZZ
- 18	936695-801	37695	. HEAT SINK ASSEMBLY	1		XB
- 19	NAS696C06M	80205	. . NUT	2		XB
- 20	MS20426AD2-4-5	96906	. . RIVET (AP)	2		XB
- 21	938710-1	37695	. . SPACER	2		XB
- 22	MS3214-6	96906	. . NUT	2		XB
- 23	514527-8	37695	. . INSERT, Screw thread ...	8		XB
- 24	515041-1	37695	. . INSERT, Screw thread ...	4		XB
- 25	NAS1068C06M	80205	. . NUT	2		XB
- 26	MS20426AD2-3	96906	. . RIVET (AP)	2		XB
- 27	936695-1	37695	. . HEAT SINK	1		XB
- 28	939012-3	37695	. HOUSING, Shield	1		XB
- 29	615467-904	37695	. TRANSISTOR	1		PADZZ
	NAS620C8L	80205	. WASHER (AP)	1		PAFZZ
	MS25082C2	96906	. NUT (AP)	1		PAFZZ
- 30	CDR14BG360EGSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG360EFSM	81349	. CAPACITOR	1		PADZZ
=	258300-11350	37695	. CAPACITOR, Fixed, glass .. dielectric	1		PADZZ
- 31	CDR14BG240EGSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG240EFSM	81349	. CAPACITOR	1		PADZZ
=	258300-11346	37695	. CAPACITOR, Fixed, glass .. dielectric	1		PADZZ
7- 4-	914873-801	37695	CIRCUIT CARD ASSEMBLY, ... Transmitter (see fig. 3 for nha)	REF		PAFLD

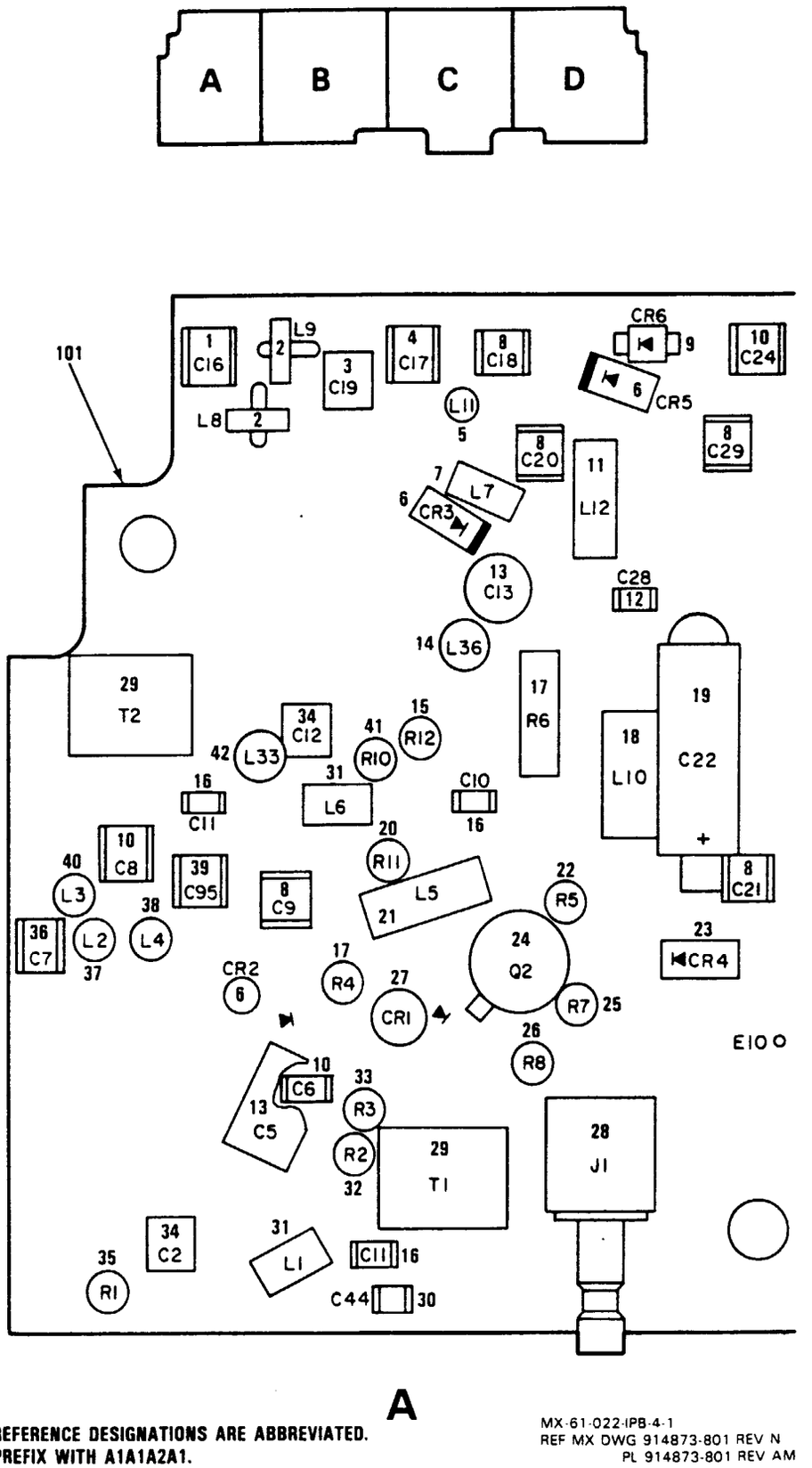


Figure 7-4. Transmitter Circuit Card Assembly (Sheet 1 of 4)

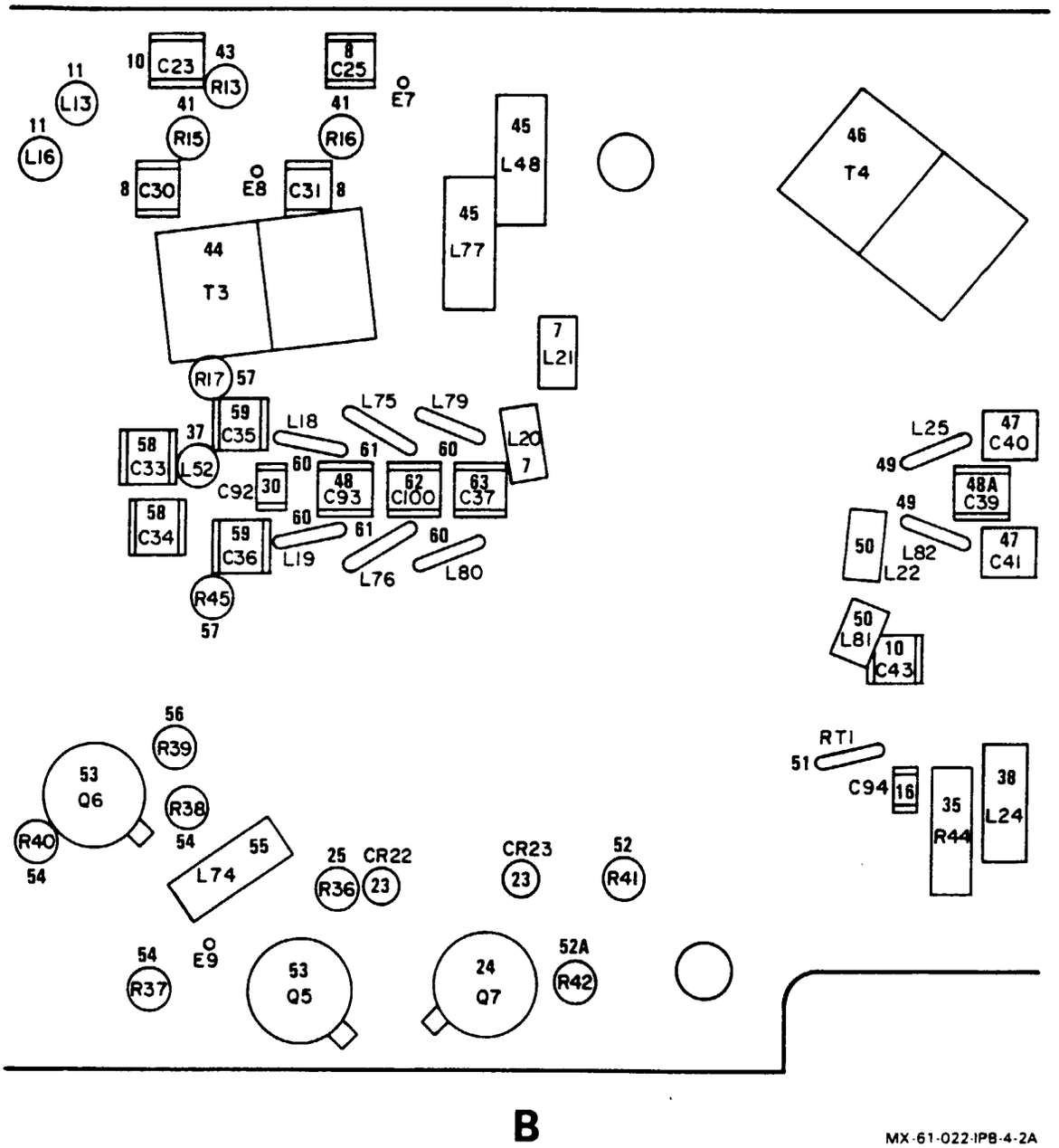


Figure 7-4. Transmitter Circuit Card Assembly (Sheet 2 of 4)

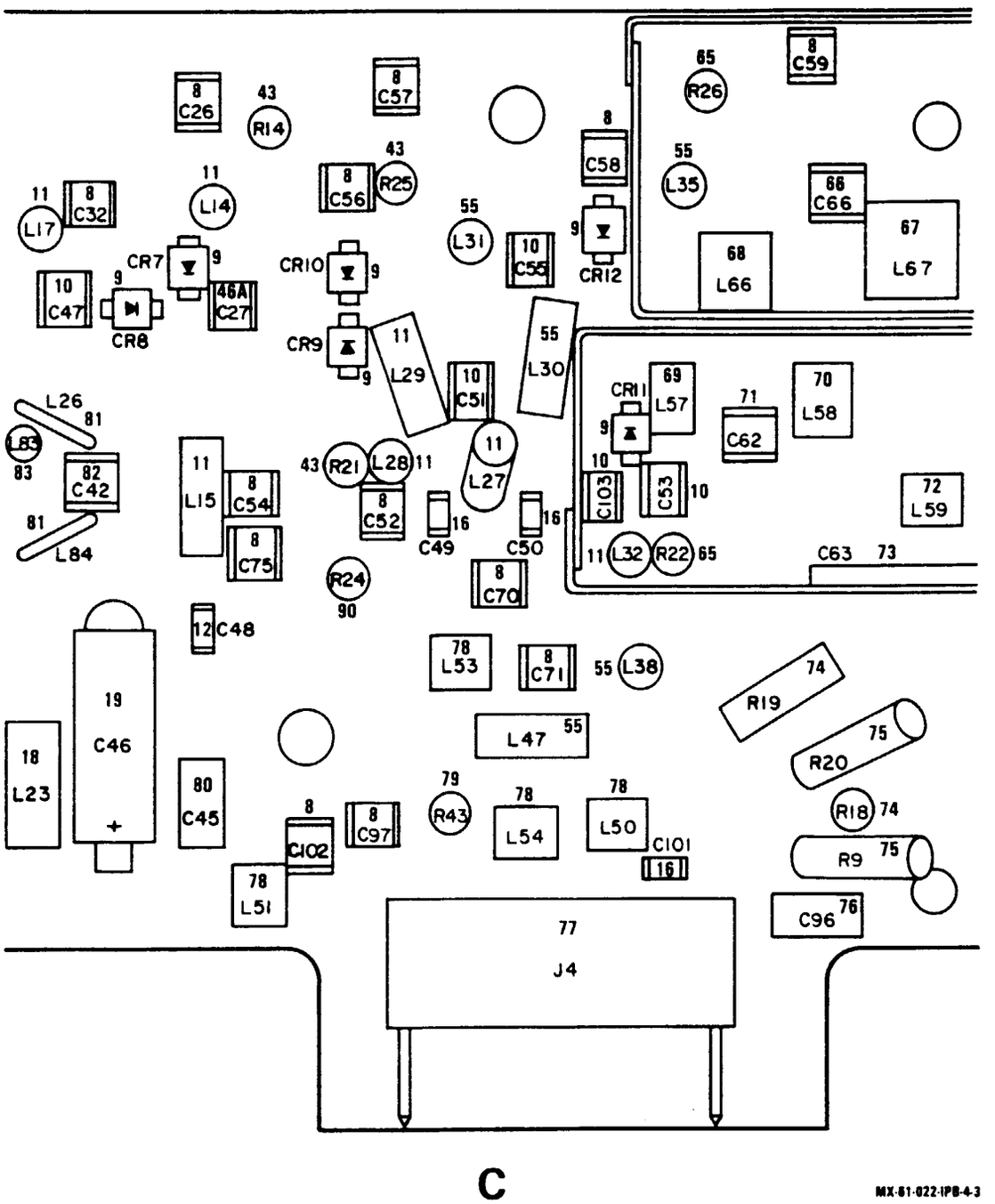


Figure 7-4. Transmitter Circuit Card Assembly (Sheet 3 of 4)

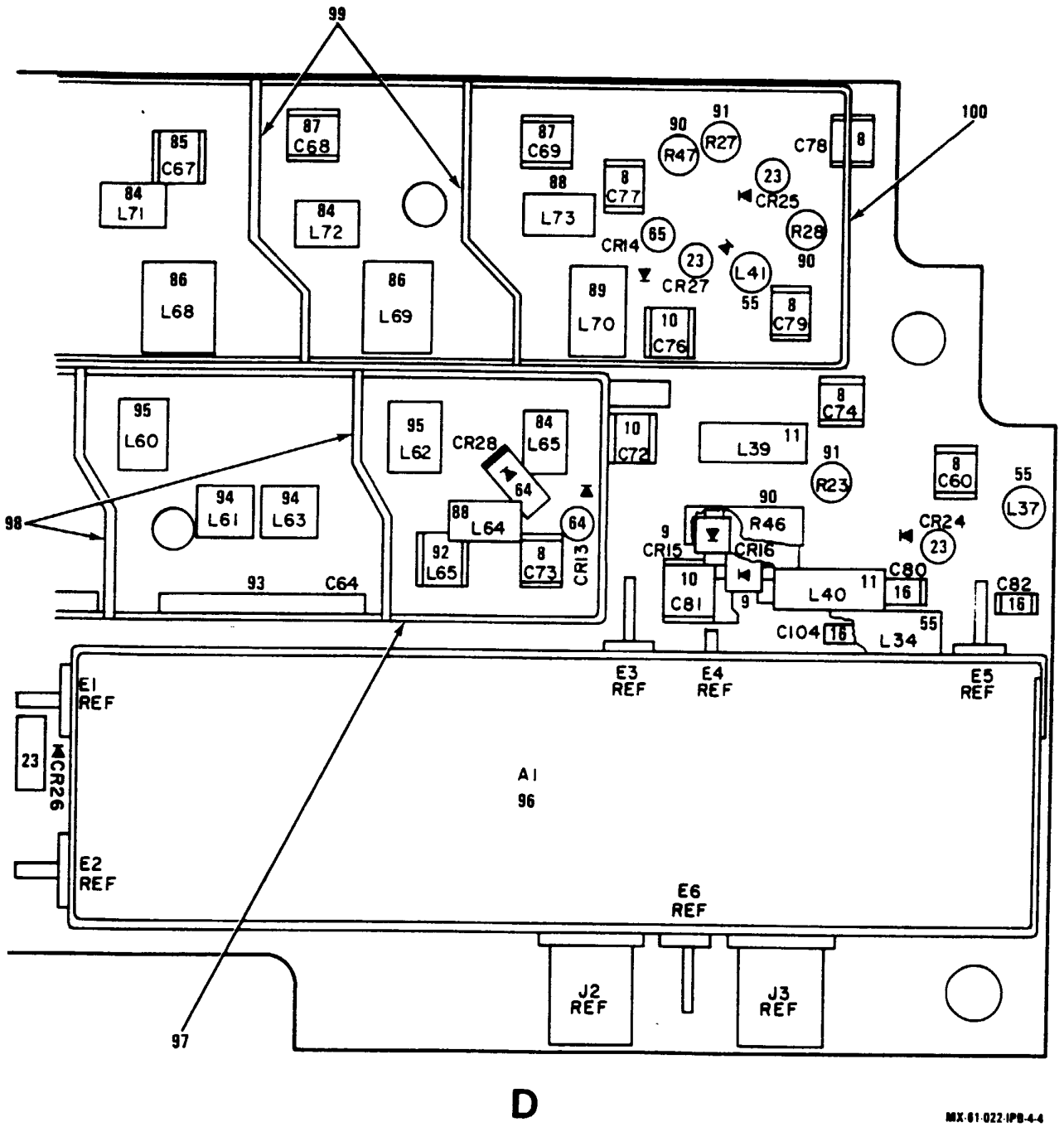


Figure 7-4. Transmitter Circuit Card Assembly (Sheet 4 of 4)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 4- 1	CDR14BG130EGSM	81349	. CAPACITOR	1		PADZZ
=	ATC-100-B-130-G-P-500-SP	29990	. CAPACITOR, Fixed, glass .. dielectric (Magnavox spec cont dwg 258300-11340)	1		PADZZ
- 2	365173-44	37695	. COIL, Radio frequency	2		PADZZ
- 3	258300-11632	37695	. CAPACITOR, Fixed, glass ..	1		
- 4	CDR14BG330EGSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG330EFSM	81349	. CAPACITOR	1		PADZZ
=	258300-11349	37695	. CAPACITOR, Fixed, glass ..	1		PADZZ
- 5	365174-817	37695	. COIL, Radio frequency	1		PADZZ
- 6	619915-902	37695	. SEMICONDUCTOR DEVICE, ... Diode	3		PADZZ
- 7	368863-801	37695	. COIL, Radio frequency	3		PADZZ
- 8	MN50471K	73899	. CAPACITOR, Fixed ..... (Magnavox spec cont dwg 258475-160)	26		PADZZ
- 9	619691-905	37695	. SEMICONDUCTOR DEVICE, ... Diode	9		PADZZ
- 10	CDR14BG471CKSM	81349	. CAPACITOR	13		PADZZ
*	CDR14BG471CFSM	81349	. CAPACITOR	13		PADZZ
=	258300-11177	37695	. CAPACITOR, Fixed, glass ..	13		PADZZ
- 11	MS75083-8	96906	. COIL	12		PADZZ
- 12	UL155C103K	96095	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258268-1220)	2		PADZZ
- 13	QC-3.3UUFPORM 5PCT	95121	. CAPACITOR, Fixed ..... (Magnavox spec cont dwg 257977-21)	2		PADZZ
- 14	365174-816	37695	. COIL, Radio frequency	1		PADZZ
- 15	RCR07G150JS	81349	. RESISTOR	1		PADZZ
- 16	CDR14BG561BKSM	81349	. CAPACITOR	11		PADZZ
=	255096-94	37695	. CAPACITOR, Fixed ceramic .	11		PADZZ
- 17	RCR07G112JS	81349	. RESISTOR	2		PADZZ
- 18	368863-802	37695	. COIL, Radio frequency	2		PADZZ
- 19	M39003/01-2411	81349	. CAPACITOR	2		PADZZ
*	M39003/01-3131	81349	. CAPACITOR	2		PADZZ
- 20	RCR07G5R1JS	81349	. CAPACITOR	1		PADZZ
- 21	368863-803	37695	. COIL, Radio frequency	1		PADZZ
- 22	RW81S8060FR	81349	. RESISTOR	1		PADZZ
- 23	JANTX1N4454-1	81350	. SEMICONDUCTOR DEVICE	7		PADZZ
- 24	JANTX2N2222A	81350	. TRANSISTOR	2		PADZZ
- 25	RCR07G362JS	81349	. RESISTOR	2		PADZZ
- 26	RCR07G154JS	81349	. RESISTOR	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 4- 27	JANTX1N647-1	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
- 28	M39012/96-0001	81349	. CONNECTOR	1		PADZZ
=	16-210-002	19505	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 189175-8)	1		PADZZ
- 29	368883-802	37695	. TRANSFORMER, Balum	2		PADZZ
- 30	CDR14BG3R9ECSM	81349	. CAPACITOR	2		PADZZ
*	CDR14BG3R9EBSM	81349	. CAPACITOR	2		PADZZ
=	258475-462	37695	. CAPACITOR, Fixed, ... ceramic	2		PADZZ
- 31	368766-847	37695	. COIL, Radio frequency	2		PADZZ
- 32	RCR07G910JS	81349	. RESISTOR	1		PADZZ
- 33	RCR07G200JS	81349	. RESISTOR	1		PADZZ
- 34	ATC-100-B-161-G-P-300-SP	29990	. CAPACITOR, Fixed, glass .. (Magnavox spec cont dwg 258300-11633)	2		PADZZ
*	CDR14BG161DGSM	81349	. CAPACITOR	2		PADZZ
- 35	RCR07G100JS	81349	. RESISTOR	2		PADZZ
- 36	CDR14BG6R8ECSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG6R8EBSM	81349	. CAPACITOR	1		PADZZ
=	258300-11633	37695	. CAPACITOR, Fixed, glass ..	1		PADZZ
- 37	368766-848	37695	. COIL, Radio frequency	2		PADZZ
- 38	MS75083-3	96906	. COIL	2		PADZZ
- 39	CDR14BG100EGSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG100EFSM	81349	. CAPACITOR	1		PADZZ
=	258300-11337	37695	. CAPACITOR, Fixed, glass ..	1		PADZZ
- 40	368760-846	37695	. COIL, Radio frequency	1		PADZZ
- 41	RCR07G300JS	81349	. RESISTOR	3		PADZZ
- 42	365174-815	37695	. COIL, Radio frequency	1		PADZZ
- 43	RCR07G330JS	81349	. RESISTOR	4		PADZZ
- 44	368883-803	37695	. TRANSFORMER, Balum	1		PADZZ
- 45	365174-818	37695	. COIL, Radio frequency	2		PADZZ
- 46	368883-804	37695	. TRANSFORMER, Balum	1		PADZZ
*	CDR14BG470EGSM	81349	. CAPACITOR	1		PADZZ
- 46A	CDR14BG470GSM	81349	. CAPACITOR	1		PADZZ
=	258300-11353	37695	. CAPACITOR, Fixed, glass ..	1		PADZZ
- 47	ATC-100-B-131-G-P-300-SP	29990	. CAPACITOR (Magnavox ..... spec cont dwg 258300-11364)	2		PADZZ
*	CED14BG131DGSM	81349	. CAPACITOR	2		PADZZ
- 48	CDR14BG150EGSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG150EFSM	81349	. CAPACITOR	1		PADZZ
=	258300-11341	37695	. CAPACITOR	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 4- 48A	258300-11343	37695	. CAPACITOR	1		
- 49	365173-6	37695	. COIL, Radio frequency	2		PADZZ
- 50	368766-844	37695	. COIL, Radio frequency	2		PADZZ
- 51	1DC802K-EC	15454	. RESISTOR, Thermal ..... (Magnavox spec cont dwg 238283-2)	1		PADZZ
- 52	RCR07G273JS	81349	. RESISTOR	1		PADZZ
- 52A	RCR07G153JS	81349	. RESISTOR	1		
- 53	JANTX2N2907A	81350	. TRANSISTOR	2		PADZZ
- 54	RCR07G683JS	81349	. RESISTOR	3		PADZZ
- 55	MS75083-13	96906	. COIL	9		PADZZ
- 56	RCR07G911JS	81349	. RESISTOR	1		PADZZ
- 57	RCR07G102JS	81349	. RESISTOR	3		PADZZ
- 58	CDR14BG680EGSM	81349	. CAPACITOR	2		PADZZ
=	ATC-100-B-680-G-P-500-SP	29990	. CAPACITOR, Fixed, ... ceramic (Magnavox spec cont dwg 258300-11357)	2		PADZZ
- 59	CDR14BG560EGSM	81349	. CAPACITOR	2		PADZZ
*	CDR14BG560EESM	81349	. CAPACITOR	2		PADZZ
=	258300-11355	37695	. CAPACITOR	2		PADZZ
- 60	365173-4	37695	. COIL, Radio frequency	4		PADZZ
- 61	365173-5	37695	. COIL, Radio frequency	2		PADZZ
- 62	CDR14BG200EGSM	81349	. CAPACITOR	1		PADZZ
=	ATC-100-B-220-G-P-500-SP	29990	. CAPACITOR, Fixed, ... ceramic (Magnavox spec cont dwg 258300-11344)	1		PADZZ
- 63	CDR14BG300EGSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG300EFSM	81349	. CAPACITOR	1		PADZZ
=	258300-11348	37695	. CAPACITOR, Fixed, glass ..	1		PADZZ
- 64	619915-903	37695	. SEMICONDUCTOR DEVICE, ... Diode	3		PADZZ
- 65	RCR07G111JS	81349	. RESISTOR	2		PADZZ
- 66	ATC175B270GP 500	29990	. CAPACITOR, Fixed ..... ceramic(Magnavox spec cont dwg 258388-125)	1		PADZZ
- 67	365173-16	37695	. COIL, Radio frequency	1		PADZZ
- 68	365173-19	37695	. COIL, Radio frequency	1		PADZZ
- 69	365173-9	37695	. COIL, Radio frequency	1		PADZZ
- 70	365173-10	37695	. COIL, Radio frequency	1		PADZZ
- 71	ATC175B110GP 500	29990	. CAPACITOR, Fixed ..... ceramic (Magnavox spec cont dwg 258388-116)	1		PADZZ
- 72	365173-11	37695	. COIL, Radio frequency	1		PADZZ
- 73	258470-2	37695	. CAPACITOR, Fixed, ... ceramic	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 4- 74	RCR07G182JS	81349	. RESISTOR	2		PADZZ
- 75 +	RCR07G681JS	81349	. RESISTOR	1		PADZZ
+	RCR07G561JS	81349	. RESISTOR	1		PADZZ
+	RCR07G821JS	81349	. RESISTOR	1		PADZZ
- 76	M39014/01-1237	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1357	81349	. CAPACITOR	1		PADZZ
- 77	103008-3	00779	. CONNECTOR, Receptacle, ... electrical (Magnavox spec cont dwg 185627-15)	1		PADZZ
- 78	56-590-65/4A	02114	. SHIELDING BEAD, ... Electronic (Magnavox spec cont dwg 657867-4)	4		PADZZ
- 79	RCR07G510JS	81349	. RESISTOR	1		PADZZ
- 80	M39014/01-1455	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1575	81349	. CAPACITOR	1		PADZZ
- 81	365173-8	37695	. COIL, Radio frequency	2		PADZZ
- 82	CDR14BG8R2EJSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG8R2ECSM	81349	. CAPACITOR	1		PADZZ
=	258300-11635	37695	. CAPACITOR	1		PADZZ
- 83	368766-841	37695	. COIL, Radio frequency	1		PADZZ
- 84	365173-15	37695	. COIL, Radio frequency	3		PADZZ
- 85	ATC175B240GP 500	29990	. CAPACITOR, Fixed ..... ceramic (Magnavox spec cont dwg 258388-124)	1		PADZZ
- 86	365173-17	37695	. COIL, Radio frequency	2		PADZZ
- 87	ATC175B220GP 500	29990	. CAPACITOR, Fixed, ... ceramic (Magnavox spec cont dwg 258388-123)	2		PADZZ
- 88	365173-14	37695	. COIL, Radio frequency	2		PADZZ
- 89	365173-18	37695	. COIL, Radio frequency	1		PADZZ
- 90	RCR07G240JS	81349	. RESISTOR	4		PADZZ
- 91	RCR07G204JS	81349	. RESISTOR	2		PADZZ
- 92	ATC175B6R2FP 500	29990	. CAPACITOR, Fixed, ... ceramic (Magnavox spec cont dwg 258388-23)	1		PADZZ
*	ATC175B6R2BP 500	29990	. CAPACITOR	1		PADZZ
- 93	258470-1	37695	. CAPACITOR, Fixed..... ceramic	1		PADZZ
- 94	365173-13	37695	. COIL, Radio frequency	2		PADZZ
- 95	365173-12	37695	. COIL, Radio frequency	2		PADZZ
- 96	810075-801	37695	. CIRCUIT CARD ASSEMBLY, ... Reflectometer (See fig. 5 for bkdn)	1		PADLD

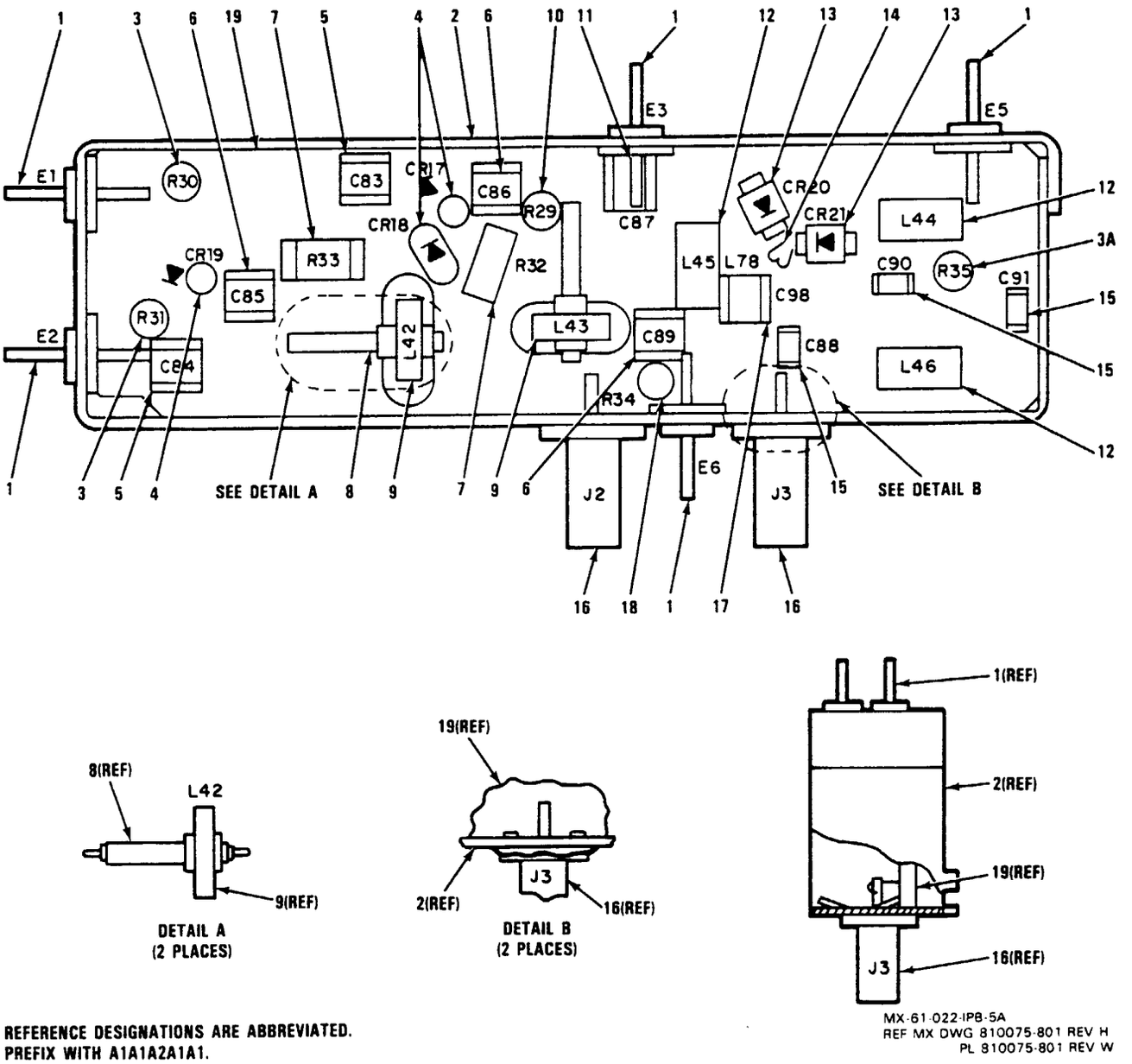


Figure 7-5. Reflectometer Circuit Card Assembly

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 4- 97	939013-1	37695	. HOUSING, Shield	1		XB
- 98	939016-1	37695	. PARTITION, Shield	2		XB
- 99	939017-1	37695	. PARTITION, Shield	2		XB
-100	939015-1	37695	. HOUSING, Shield	1		XB
-101	410906-1	37695	. PRINTED WIRING BOARD	1		XB
7- 5-	810075-801	37695	. CIRCUIT CARD ASSEMBLY, ... Reflectometer (See fig. 4 for nha)	REF		PADLD
- 1	AAA-40T-SS	20093	. TERMINAL, Feedthru, ... insulated (Magnavox spec cont dwg 205034-24)	5		PADZZ
- 2	939014-1	37695	. HOUSING, Shield	1		XB
- 3	RCR05G821JS	81349	. RESISTOR	2		PADZZ
- 3A	RCR05G361JS	81349	. RESISTOR	2		PADZZ
- 4	615485-2	37695	. SEMICONDUCTOR DEVICE, ... Diode	3		PADZZ
- 5	MN40680J	73899	. CAPACITOR, Fixed, ... ceramic dielectric (Magnavox spec cont dwg 258475-229)	2		PADZZ
*	CDR01BP680BJMS	81349	. CAPACITOR	2		PADZZ
- 6	CDR14BG471CKSM	81349	. CAPACITOR	3		PADZZ
*	CDR14BG471CFSM	81349	. CAPACITOR	3		PADZZ
=	258300-11177	37695	. CAPACITOR, Fixed, glass, . dielectric	3		PADZZ
- 7	TRM-18-S	24620	. RESISTOR, Fixed film ..... (Magnavox spec cont dwg 238279-1)	2		PADZZ
- 8	566718-1	37695	. CABLE, Radio frequency ...	2		PADZZ
- 9	365175-801	37695	. COIL, Radio frequency	2		PADZZ
- 10	RCR05G152JS	81349	. RESISTOR	1		PADZZ
- 11	CDR14G560EGSM	81349	. CAPACITOR	1		PADZZ
*	CDR14G560EESM	81349	. CAPACITOR	1		PADZZ
=	258300-11355	37695	. CAPACITOR, Fixed, ... ceramic	1		PADZZ
- 12	MS75083-8	96906	. COIL	3		PADZZ
- 13	619691-905	37695	. SEMICONDUCTOR DEVICE, ... Diode	2		PADZZ
- 14	368766-846	37695	. COIL, Radio frequency	1		PADZZ
- 15	CDR14BG561BKSM	81349	. CAPACITOR	3		PADZZ

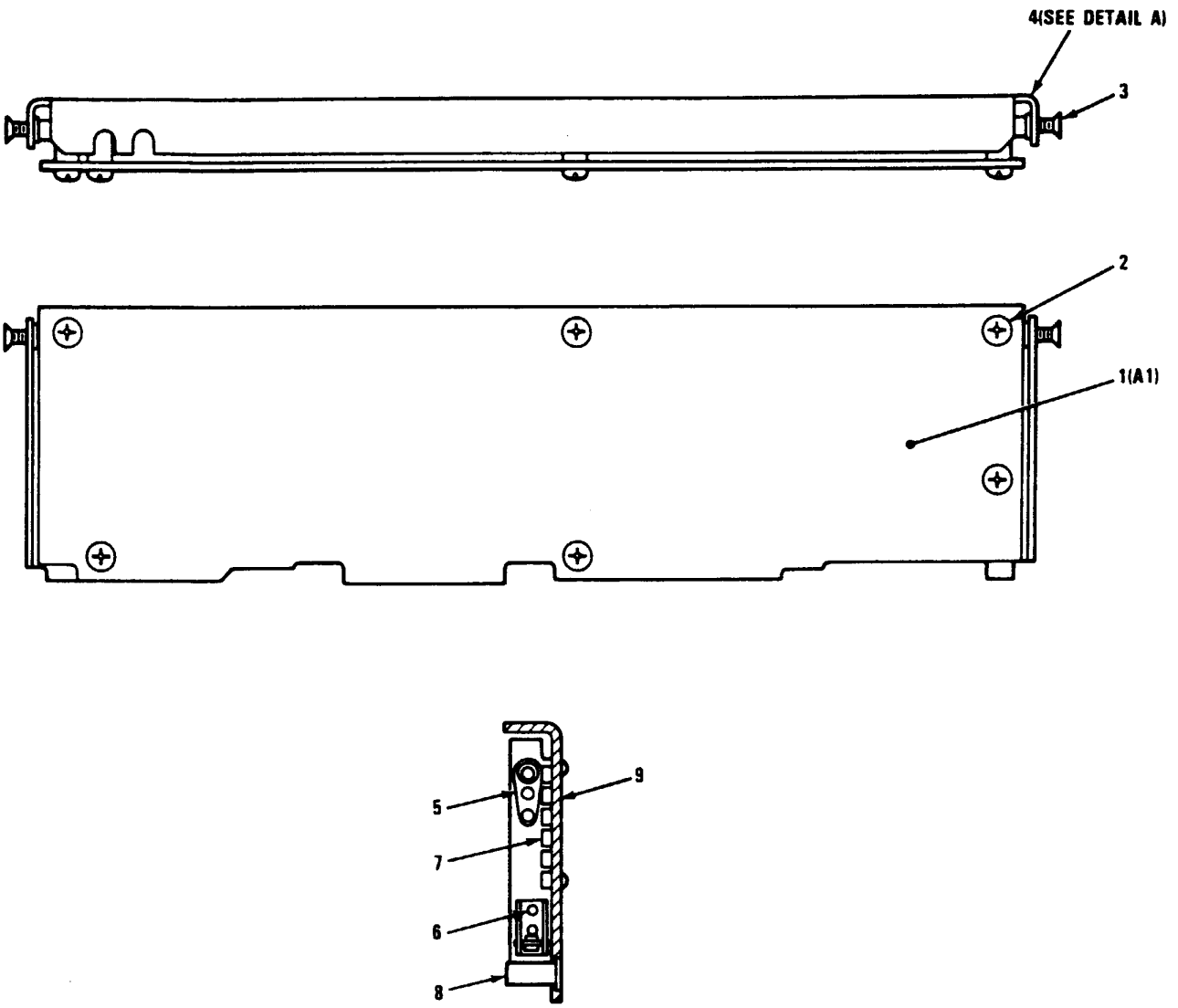


Figure 7-6. Guard Receiver Assembly

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 5-	= 7203A471KF	95275	. CAPACITOR, Fixed ..... ceramic (Magnavox spec cont dwg 255096-94)	3		PADZZ
- 16	M39012/95-0001	81349	. CONNECTOR	2		PADZZ
	= 2009-6511-000	19505	. CONNECTOR, Receptacle, ... electric (Magnavox spec cont dwg 189175-7)	2		PADZZ
- 17	MN403R9D	73899	. CAPACITOR, Fixed, ... ceramic (Magnavox spec cont dwg 258475-462)	1		
- 18	RCR05G111JS	81349	. RESISTOR	1		PADZZ
- 19	410949-1	37695	. PRINTED WIRING BOARD	1		XB
7- 6-	811955-801	37695	RECEIVER ASSEMBLY, Guard ... (See fig. 2 for nha)	REF		PAFLD
- 1	914865-801	37695	. CIRCUIT CARD ASSEMBLY, ... Guard receiver (See fig. 7 for bkdn)	1		PADLD
- 2	MS51957-14	96906	. SCREW (AP)	6		PAFZZ
- 3	MS24693C25	96906	. SCREW (AP)	2		PAFZZ
- 4	938403-801	37695	. BRACKET, Guard receiver ..	1		XB
- 5	NAS696C06M	80205	. . NUT	2		XB
	MS20426AD2-3	96906	. . RIVET (AP)	2		XB
- 6	RMLHA27M2860-62	72962	. . NUT, Self-locking ..... (Magnavox spec cont dwg 107295-2)	2		XB
	MS20426AD2-3	96906	. . RIVET (AP)	2		XB
- 7	165467-1	37695	. . CONTACT STRIP	1		XB
	108747-7	37695	. . RIVET (AP)	2		XB
- 8	514527-101	37695	. . INSERT, Screw thread ...	6		PAFZZ
- 9	938403-1	37695	. . BRACKET, Guard ..... receiver	1		XB
7- 7-	914865-801	37695	CIRCUIT CARD ASSEMBLY, ... Guard receiver (See fig. 6 for nha)	REF		PADLD
- 1	938511-1	37695	. COVER, Shield	1		XB
- 2	186748-1	37695	. CONNECTOR, Strip, ... modified	1		XB

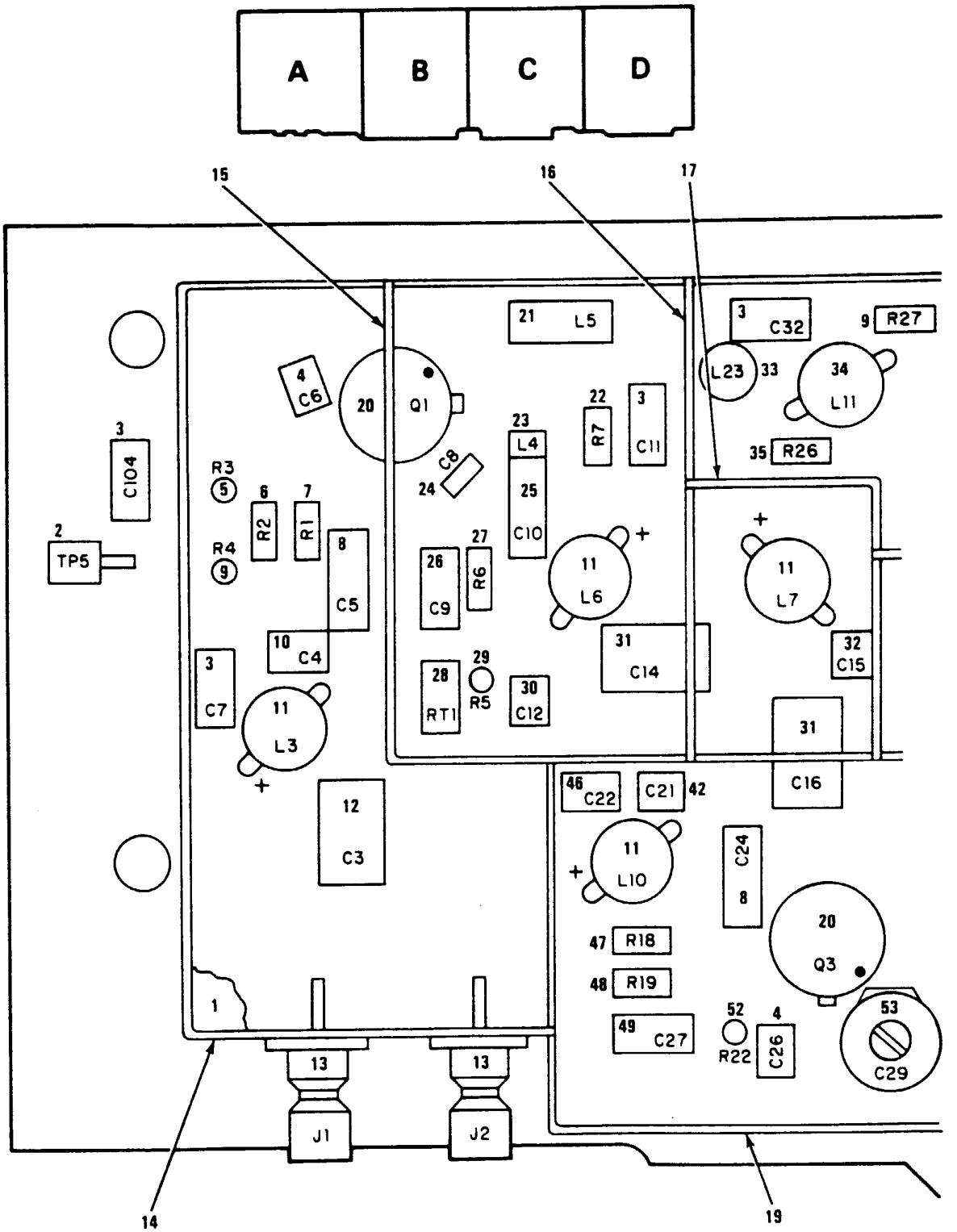


Figure 7-7. Guard Receiver Circuit Card Assembly (Sheet 1 of 5)

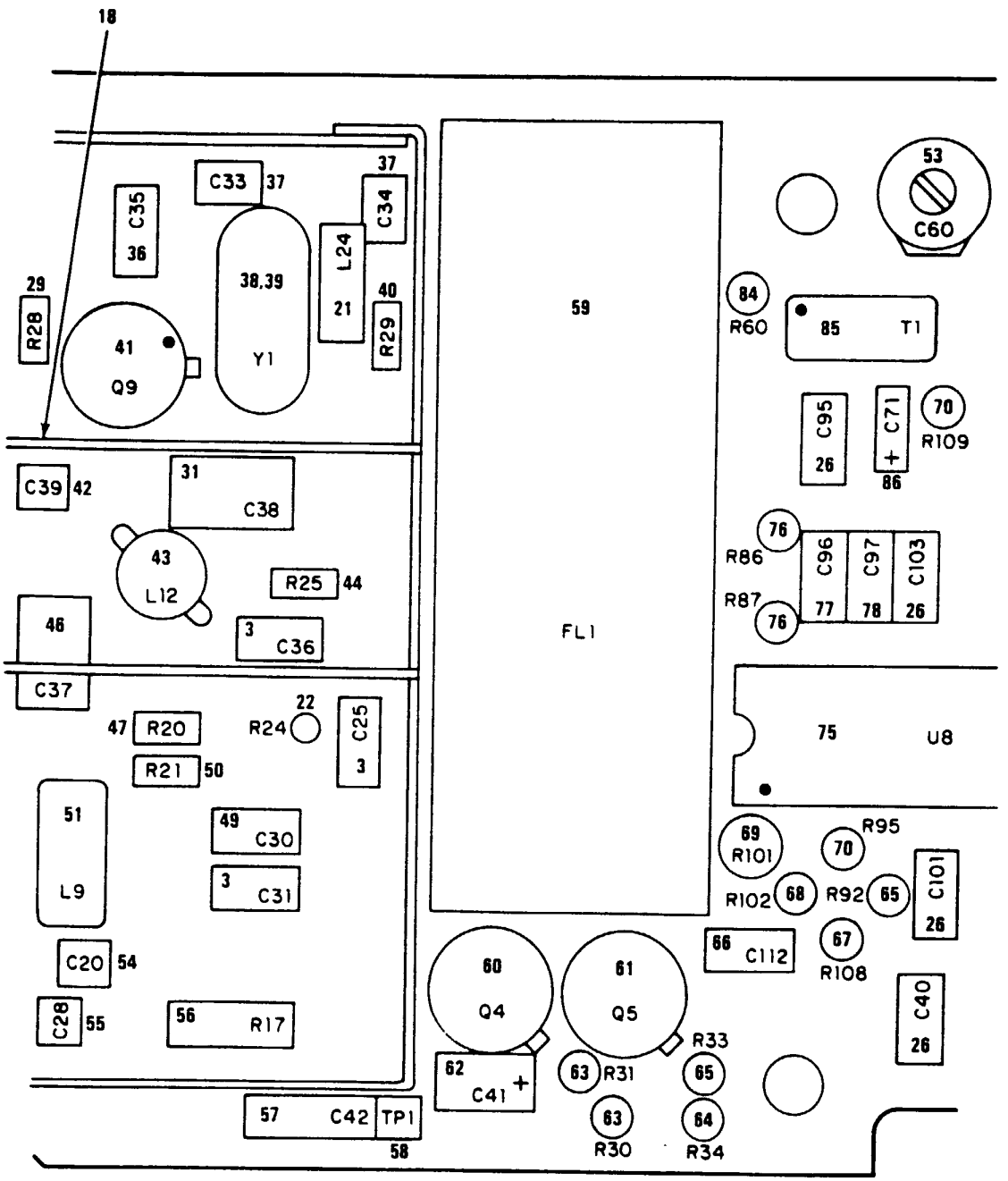


Figure 7-7. Guard Receiver Circuit Card Assembly (Sheet 2 of 5)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 7- 3	M39014/01-1231	81349	. CAPACITOR	7		PADZZ
- 4	CDR14BG102AMSM	81349	. CAPACITOR	2		PADZZ
*	CDR14BG102AGSM	81349	. CAPACITOR	2		PADZZ
=	255096-80	37695	. CAPACITOR, Fixed ceramic . dielectric	2		PADZZ
- 5	RCR05G622JS	81349	. RESISTOR	1		PADZZ
- 6	RCR05G274JS	81349	. RESISTOR	1		PADZZ
- 7	RCR05G563JS	81349	. RESISTOR	1		PADZZ
- 8	C33A8R2J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258236-276)	2		PADZZ
- 9	RCR05G751JS	81349	. RESISTOR	2		PADZZ
- 10 =	CN15A6R8D	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-6193)	1		PADZZ
=	CN15A6R8D	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-26193)	1		PADZZ
*	8101A100C0G 0689C	18796	. CAPACITOR, Fixed ceramic .	1		PADZZ
- 11	041373-RS-1	00779	. COIL, Radio frequency .... (Magnavox spec cont dwg 368839-1)	4		PADZZ
- 12	QC-2.2UUFPORM 5PCT	95121	. CAPACITOR, Fixed, ... composition (Magnavox spec cont dwg 257977-18)	1		PADZZ
- 13	M39012/95-0001	81349	. CONNECTOR	2		PADZZ
=	16-0209-000	19505	. CONNECTOR, Coaxial ..... (Magnavox spec cont dwg 189175-7)	2		PADZZ
- 14	938506-1	37695	. HOUSING, Shield	1		XB
- 15	938507-1	37695	. PARTITION, Shield	1		XB
- 16	938510-1	37695	. PARTITION, Shield	1		XB
- 17	938508-1	37695	. PARTITION, Shield	1		XB
- 18	938509-1	37695	. PARTITION, Shield	1		XB
- 19	938505-1	37695	. HOUSING, Shield	1		XB
- 20	JANTX3N204	81349	. SEMICONDUCTOR DEVICE	2		PADZZ
=	615238-904	37695	. SEMICONDUCTOR DEVICE	2		PADZZ
- 21	MS75083-9	96906	. COIL	2		PADZZ
- 22	RCR05G100JS	81349	. RESISTOR	2		PADZZ
- 23	21-172-J	33062	. SHIELDING BEAD, ... Electric (Magnavox spec cont dwg 657907-1)	1		XB

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 7- 24 =	CDR14BG471CMSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG471CFSM	81349	. CAPACITOR	1		PADZZ
=	255096-94	37695	. CAPACITOR, Fixed ceramic . dielectric	1		PADZZ
- 25	C33A100J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258236-277)	1		PAFZZ
- 26	M39014/01-1455	81349	. CAPACITOR	8		PADZZ
- 27	RCR05G470JS	81349	. RESISTOR	1		PADZZ
- 28	15DC102K-EC-S	15454	. RESISTOR, Thermal ..... (Magnavox spec cont dwg 238283-1)	1		PADZZ
	107240-40		. WASHER, Nonmetalic.....	2		
- 29	RCR05G202JS	81349	. RESISTOR	2		PADZZ
- 30 =	CN15A8R2D	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-26194)	1		
=	CN10C8A2D	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-26004)	1		PADZZ
- 31	QC-0.47UUFPORM 5PCT	95121	. CAPACITOR, Fixed ..... composition (Magnavox spec cont dwg 257977-9)	3		PADZZ
- 32 =	150-100-NPO -471	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22195)	1		PADZZ
=	CN10C100J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22005)	1		PADZZ
*	8101A100C0G 0100B	59660	. CAPACITOR, Fixed ceramic .	1		PADZZ
- 33	56-590-65/4B	02114	. SHIELDING BEAD, ... electrical (Magnavox spec cont dwg 657867-2)	8		XB
- 34	041373-RS-5	00779	. COIL, Radio frequency .... (Magnavox spec cont dwg 368839-5)	1		PADZZ
- 35	RCR05G123JS	81349	. RESISTOR	1		PADZZ
- 36	CCR07CG102JM	81349	. CAPACITOR	1		PADZZ
*	CCR07CG102GR	81349	. CAPACITOR	1		PADZZ
=	258330-22219	37695	. CAPACITOR, Fixed ceramic . dielectric	1		

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 7- 37 =	CN10C270J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2010)	2		PADZZ
=	CN10C270J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22010)	2		PADZZ
- 38	538665-12	37695	. CRYSTAL UNIT, Quartz	1		PADZZ
- 39	345565-1	37695	. INSULATOR	2		PADZZ
- 40	RCR05G121JS	81349	. RESISTOR	1		PADZZ
- 41	JANTX2N2857	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
- 42 =	CN15A6R8D	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-26193)	2		PADZZ
=	CN10C6R8D	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-26003)	2		PADZZ
- 43	041373-RS-6	00779	. COIL, Radio frequency .... (Magnavox spec cont dwg 368839-6)	1		PADZZ
- 44	RCR05G331JS	81349	. RESISTOR	1		PADZZ
- 45	QC-8.2UUFPORM 5PCT	95121	. CAPACITOR, Fixed, ... composition (Magnavox spec cont dwg 257977-26)	1		PADZZ
- 46 =	CN15A820J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2065)	2		PADZZ
=	CN15A820J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22065)	2		PADZZ
*	8101A100CG 0689C	59660	. CAPACITOR, Fixed ceramic .	2		PADZZ
- 47	RCR05G104JS	81349	. RESISTOR	2		PADZZ
- 48	RCR05G223JS	81349	. RESISTOR	1		PADZZ
- 49	M39014/01-1448	81349	. CAPACITOR	9		PADZZ
*	M39014/01-1568	81349	. CAPACITOR	9		PADZZ
- 50	RCR05G333JS	81349	. RESISTOR	1		PADZZ
- 51	365175-804	37695	. COIL, Radio frequency	2		PADZZ
- 52	RCR05G271JS	81349	. RESISTOR	1		PADZZ
- 53 =	518-000-39A	72982	. CAPACITOR, Variable, ... ceramic (Magnavox spec cont dwg 265011-17)	3		PADZZ
=	CV35A250	81349	. CAPACITOR	3		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 7- 54 =	CN10C150J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22007)	1		PADZZ
=	CN15A150D	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22197)	1		
=	100-050-NPO-150J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22007)	1		PADZZ
- 55 =	CN10C620J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2106)	1		PADZZ
=	CN10C620J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22106)	1		PADZZ
- 56	RCR07G201JS	81349	. RESISTOR	1		PADZZ
- 57	M39014/02-1230	81349	. CAPACITOR	14		PADZZ
- 58	186095-1	37695	. CONNECTOR, Strip, ... modified	2		PADZZ
- 59	6207	25120	. FILTER, Bandpass ..... (Magnavox spec cont dwg 328416-10)	1		PADZZ
- 60	JANTX2N2907A	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
- 61	JANTX2N2222A	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
- 62	S106R	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-75)	2		PADZZ
- 63	RCR07G222JS	81349	. RESISTOR	6		PADZZ
- 64	RCR07G332JS	81349	. RESISTOR	2		PADZZ
- 65	RCR07G472JS	81349	. RESISTOR	2		PADZZ
- 66 =	CCR05CG102JM	81349	. CAPACITOR	1		PADZZ
=	W200-100-NP0-102D	51642	. CAPACITOR (Magnavox ..... spec cont dwg 258330-22206)	1		
- 67	RCR07G240JS	81349	. RESISTOR	2		PADZZ
- 68	RCR07G362JS	81349	. RESISTOR	1		PADZZ
- 69	RNC55H1502FR	81349	. RESISTOR	1		PADZZ
*	RNC55H1502FS	81349	. RESISTOR	1		PADZZ
- 70	RCR07G101JS	81349	. RESISTOR	7		PADZZ
- 71	MS75085-7	96906	. COIL	4		PADZZ
- 72	RCR07G123JS	81349	. RESISTOR	2		PADZZ
- 73	RCR07G181JS	81349	. RESISTOR	1		PADZZ
- 74	RCR07G512JS	81349	. RESISTOR	1		PADZZ
- 75	615794-901	37695	. MICROCIRCUIT, Linear	2		PADZZ

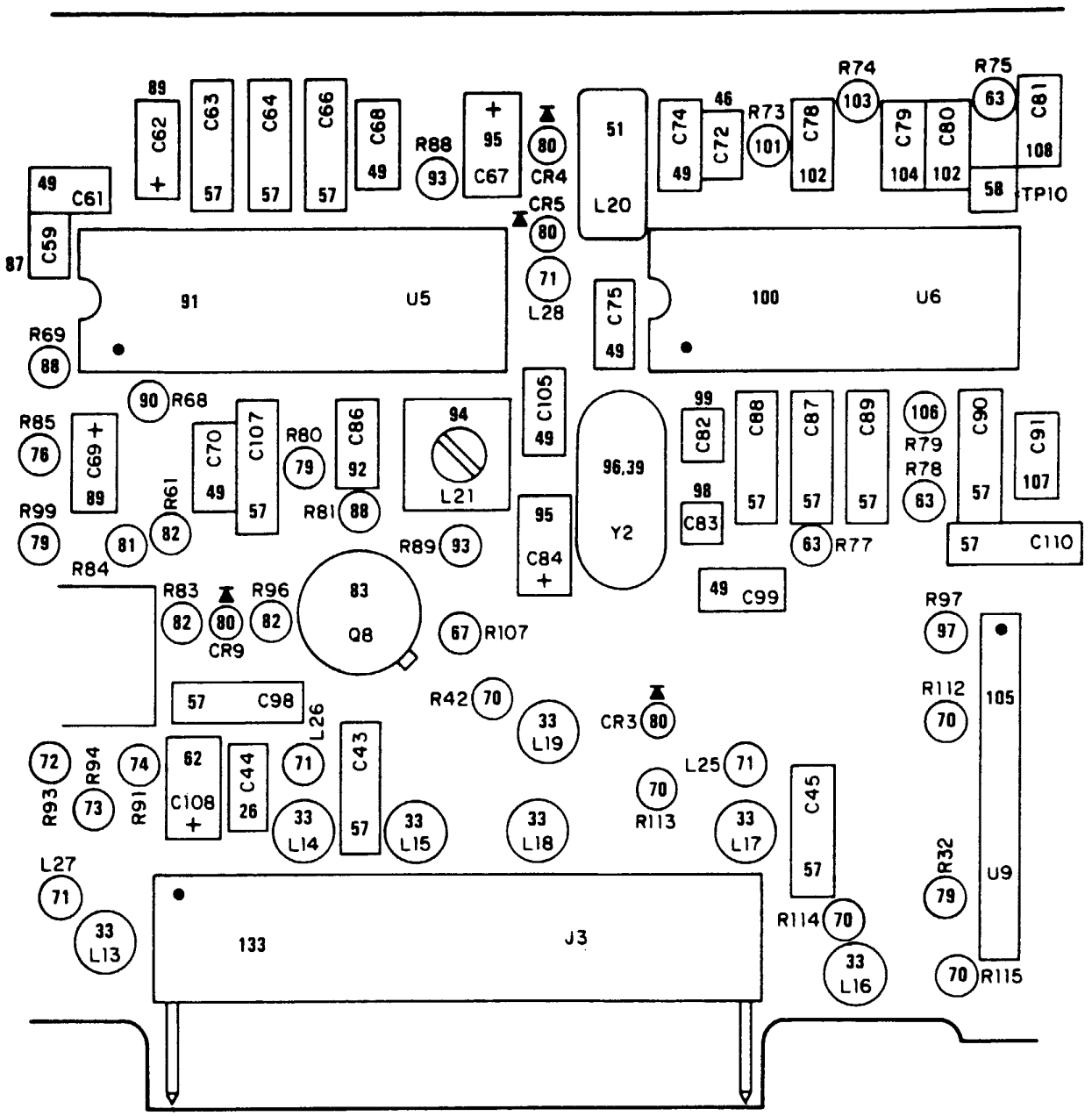


Figure 7-7. Guard Receiver Circuit Card Assembly (Sheet 3 of 5)

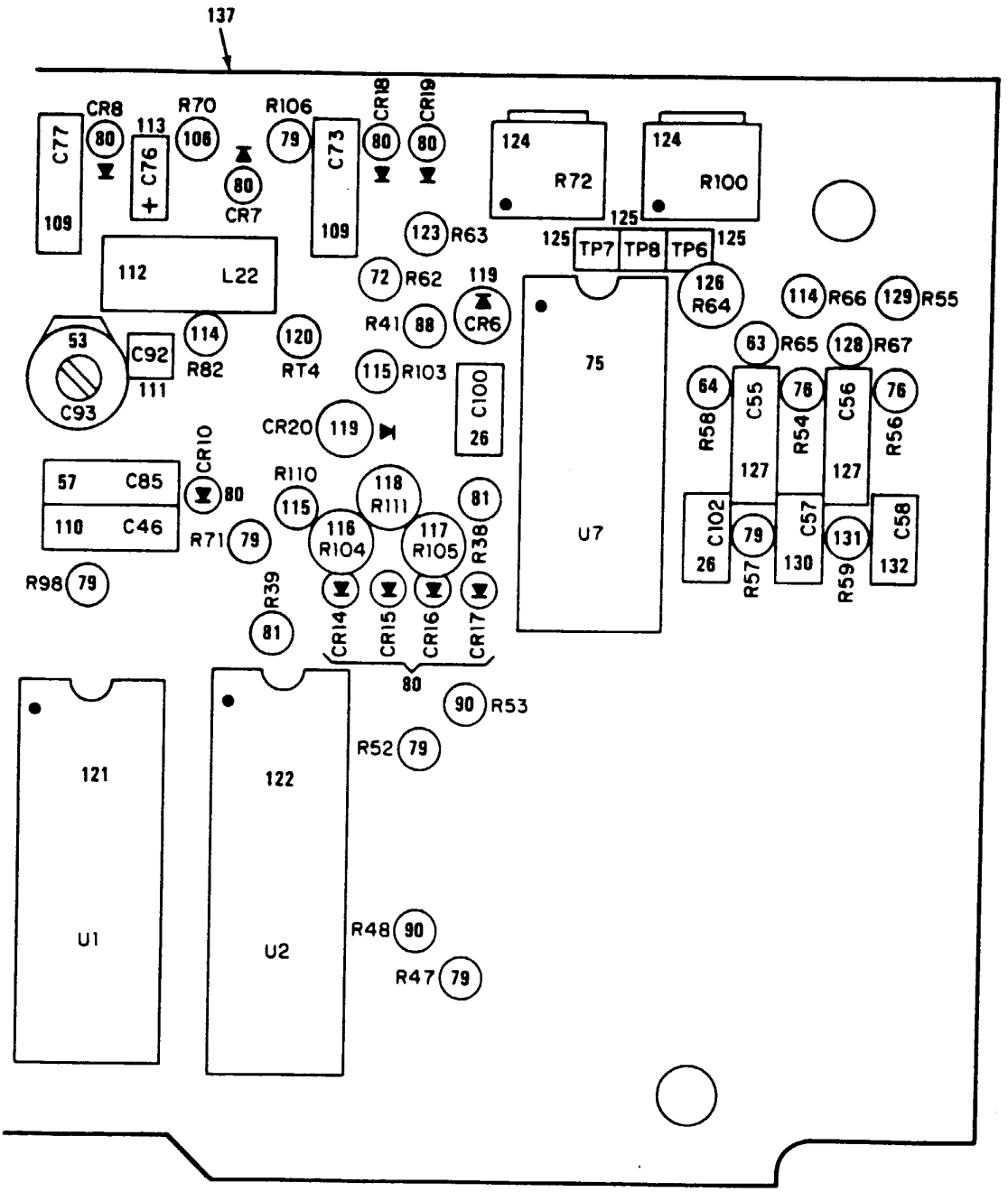


Figure 7-7. Guard Receiver Circuit Card Assembly (Sheet 4 of 5)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 7-	= JM38510/11001 BCX	81350	. MICROCIRCUIT	2		
- 76	RCR07G562JS	81349	. RESISTOR	5		PADZZ
- 77	M39014/01-1240	81349	. CAPACITOR	1		PADZZ
	* M39014/01-1360	81349	. CAPACITOR	1		PADZZ
- 78	M39014/01-1463	81349	. CAPACITOR	1		PADZZ
	* M39014/01-1583	81349	. CAPACITOR	1		PADZZ
- 79	RCR07G103JS	81349	. RESISTOR	9		PADZZ
- 80	JANTX1N4454-1	81350	. SEMICONDUCTOR DEVICE	16		PADZZ
- 81	RCR07G273JS	81349	. RESISTOR	3		PADZZ
- 82	RCR07G104JS	81349	. RESISTOR	3		PADZZ
- 83	JANTX2N4858	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
- 84	RCR07G620JS	81349	. RESISTOR	1		PADZZ
- 85	365175-808	37695	. COIL, Radio frequency	1		PADZZ
- 86	M106R-5	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-438)	1		PADZZ
- 87	CN10C750J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2107)	1		PADZZ
	= CN10C750J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22107)	1		PADZZ
	= 100-050-NPO-750J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2107)	1		PADZZ
	= 100-050-NPO-750J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22107)	1		PADZZ
- 88	RCR07G102JS	81349	. RESISTOR	3		PADZZ
- 89	L156R-5	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-443)	2		PADZZ
- 90	RCR07G471JS	81349	. RESISTOR	3		PADZZ
- 91	617714-902	37695	. MICROCIRCUIT, Linear	1		PADZZ
- 92	CN20C621J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2118)	1		PADZZ
	= CN20C621J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22118)	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 7-	= 200-050-NPO-621J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2118)	1		PADZZ
	= 200-050-NPO-621J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22118)	1		PADZZ
- 93	RCR07G5R6JS	81349	. RESISTOR	2		PADZZ
- 94	MS21381-27	96906	. COIL	1		PADZZ
	= 365189-1	37695	. COIL, Radio frequency	1		PADZZ
- 95	S226R	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-48)	2		PADZZ
- 96	538765-1	37695	. CRYSTAL UNIT, Quartz	1		PADZZ
- 97	RCR07G100JS	81349	. RESISTOR	1		PADZZ
- 98	CN10C430J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2104)	1		PADZZ
	= CN10C430J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22104)	1		PADZZ
	= 100-050-NPO-430J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2104)	1		PADZZ
	= 100-050-NPO-430J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22104)	1		PADZZ
- 99	CN10C180J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 2158330-2008)	1		PADZZ
	= CN10C180J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22008)	1		PADZZ
-100	616594-901	37695	. MICROCIRCUIT, Linear	1		PADZZ
	* CCR13CG180GM	81349	. CAPACITOR	1		PADZZ
-101	RCR07G563JS	81349	. RESISTOR	1		PADZZ
-102	M39014/01-1230	81349	. CAPACITOR	2		PADZZ
-103	RCR07G153JS	81349	. RESISTOR	1		PADZZ
-104	M39014/01-1236	81349	. CAPACITOR	1		PADZZ
	* M39014/01-1356	81349	. CAPACITOR	1		PADZZ
-105	M8340105M4703 JC	81349	. RESISTOR	1		PADZZ
	= M8340105K4703 GC	81349	. RESISTOR	1		PADZZ
-106	RCR07G473JS	81349	. RESISTOR	2		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 7-107	M39014/01-1201	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1321	81349	. CAPACITOR	1		PADZZ
-108	M39014/01-1237	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1357	81349	. CAPACITOR	1		PADZZ
-109	M39014/02-1240	81349	. CAPACITOR	2		PADZZ
*	M39014/02-1360	81349	. CAPACITOR	2		PADZZ
-110	M39014/02-1407	81349	. CAPACITOR	1		PADZZ
*	M39014/02-1419	81349	. CAPACITOR	1		PADZZ
-111	CN10C680J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2015)	1		PADZZ
=	CN10C680J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22015)	1		PADZZ
-112	MS90538-12	96906	. COIL	1		PADZZ
-113	M685R-5	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-437)	1		PADZZ
-114	RCR07G223JS	81349	. RESISTOR	2		PADZZ
-115	RCR07G392JS	81349	. RESISTOR	2		PADZZ
-116	RNC55H9311FR	81349	. RESISTOR	1		PADZZ
*	RNC55H9311FS	81349	. RESISTOR	1		PADZZ
-117 +	RNC55H1053FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1053FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1003FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1003FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1023FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1023FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1073FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1073FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1103FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1103FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1133FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1133FS	81349	. RESISTOR	1		PADZZ
+	RNC55H9762FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H9762FS	81349	. RESISTOR	1		PADZZ
+	RNC55H7872FR	81349	. RESISTOR	1		PADZZ
+	RNC55H8062FR	81349	. RESISTOR	1		PADZZ
+	RNC55H8252FR	81349	. RESISTOR	1		PADZZ
+	RNC55H8452FR	81349	. RESISTOR	1		PADZZ
+	RNC55H8662FR	81349	. RESISTOR	1		PADZZ
+	RNC55H8872FR	81349	. RESISTOR	1		PADZZ
+	RNC55H9092FR	81349	. RESISTOR	1		PADZZ
+	RNC55H9312FR	81349	. RESISTOR	1		PADZZ
+	RNC55H9532FR	81349	. RESISTOR	1		PADZZ
+	RNC55H9762FR	81349	. RESISTOR	1		PADZZ

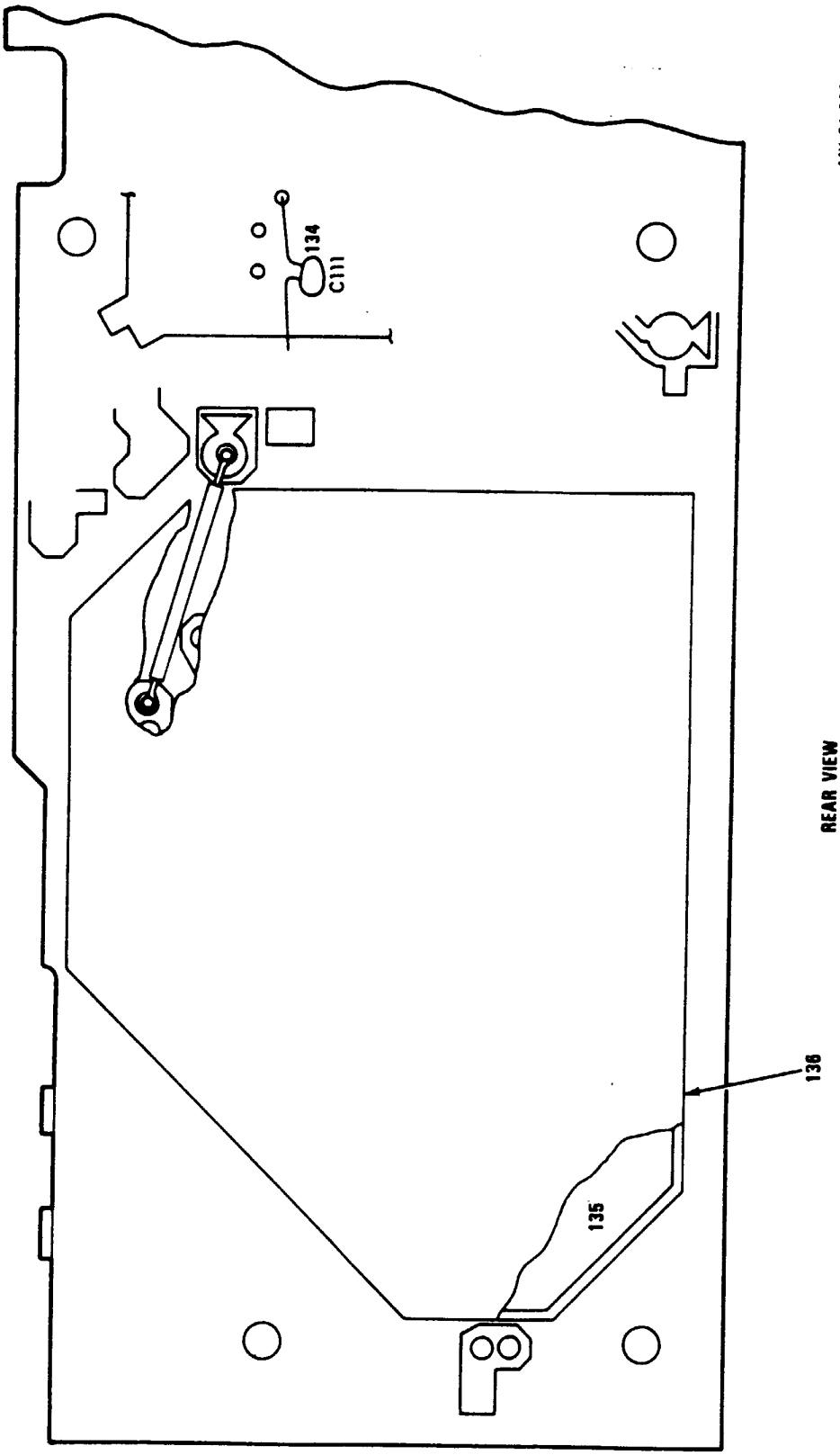
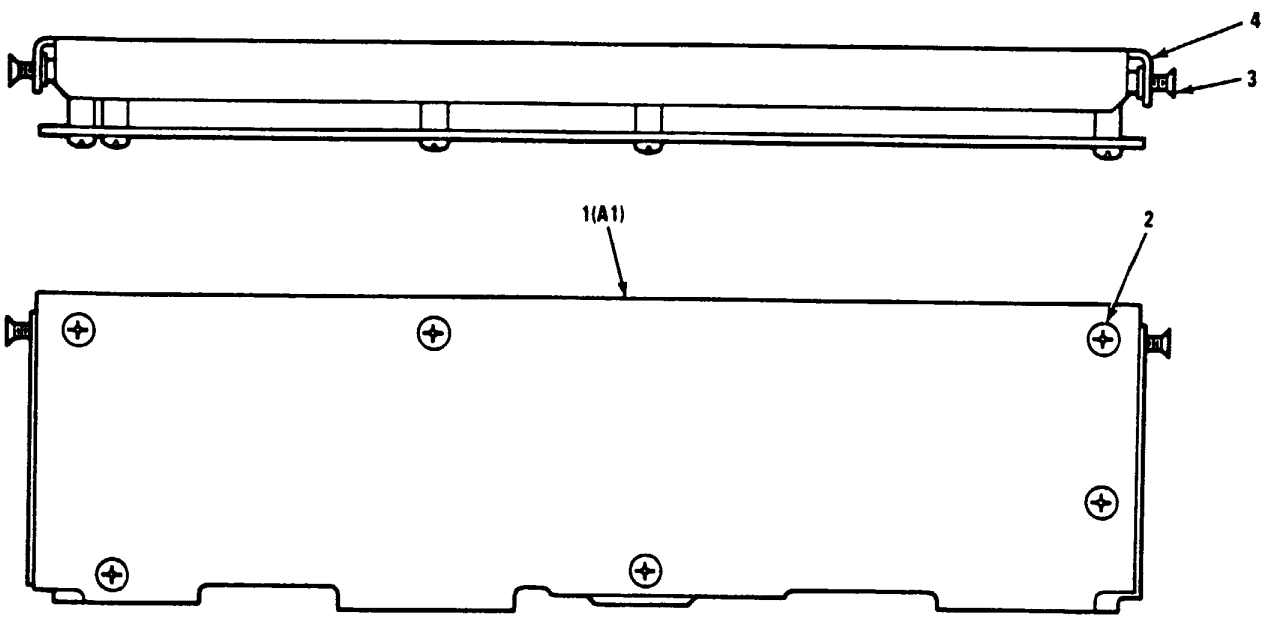


Figure 7-7. Guard Receiver Circuit Card Assembly (Sheet 5 of 5)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 7-118	RNC55H2001FR	81349	. RESISTOR	1		PADZZ
*	RNC55H2001FS	81349	. RESISTOR	1		PADZZ
-119	JANTX1N752A1	81350	. SEMICONDUCTOR DEVICE	2		PADZZ
-120	238099-4	37695	. RESISTOR, Thermal	1		PADZZ
-121 =	JM38510/17601 BEX	81349	. MICROCIRCUIT	1		PADZZ
=	619998-1	37695	. MICROCIRCUIT, Digital	1		PADZZ
*	M38510/17601 BEB	81349	. MICROCIRCUIT	1		PADZZ
-122	615699-903	37695	. MICROCIRCUIT, Digital	1		PADZZ
-123	RCR07G154JS	81349	. RESISTOR	1		PADZZ
-124	8050EKX201GM	30983	. RESISTOR, Variable ..... (Magnavox spec cont dwg 228113-6)	2		PADZZ
-125	186095-3	37695	. CONNECTOR, Strip, ... modified	3		XB
-126 +	RNC55H1502FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1502FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1652FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1652FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1022FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1022FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1072FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1072FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1132FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1132FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1182FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1182FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1242FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1242FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1302FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1302FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1372FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1372FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1432FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1432FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1582FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1582FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1742FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1742FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1822FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1822FS	81349	. RESISTOR	1		PADZZ
+	RNC55H8871FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H8871FS	81349	. RESISTOR	1		PADZZ



REFERENCE DESIGNATIONS ARE ABBREVIATED.
PREFIX WITH A1A1A6.

MX-81-022-IPB-8
REF MX DWG 811829-001 REV C
PL 811829-001 REV F

Figure 7-8. Synthesizer Assembly

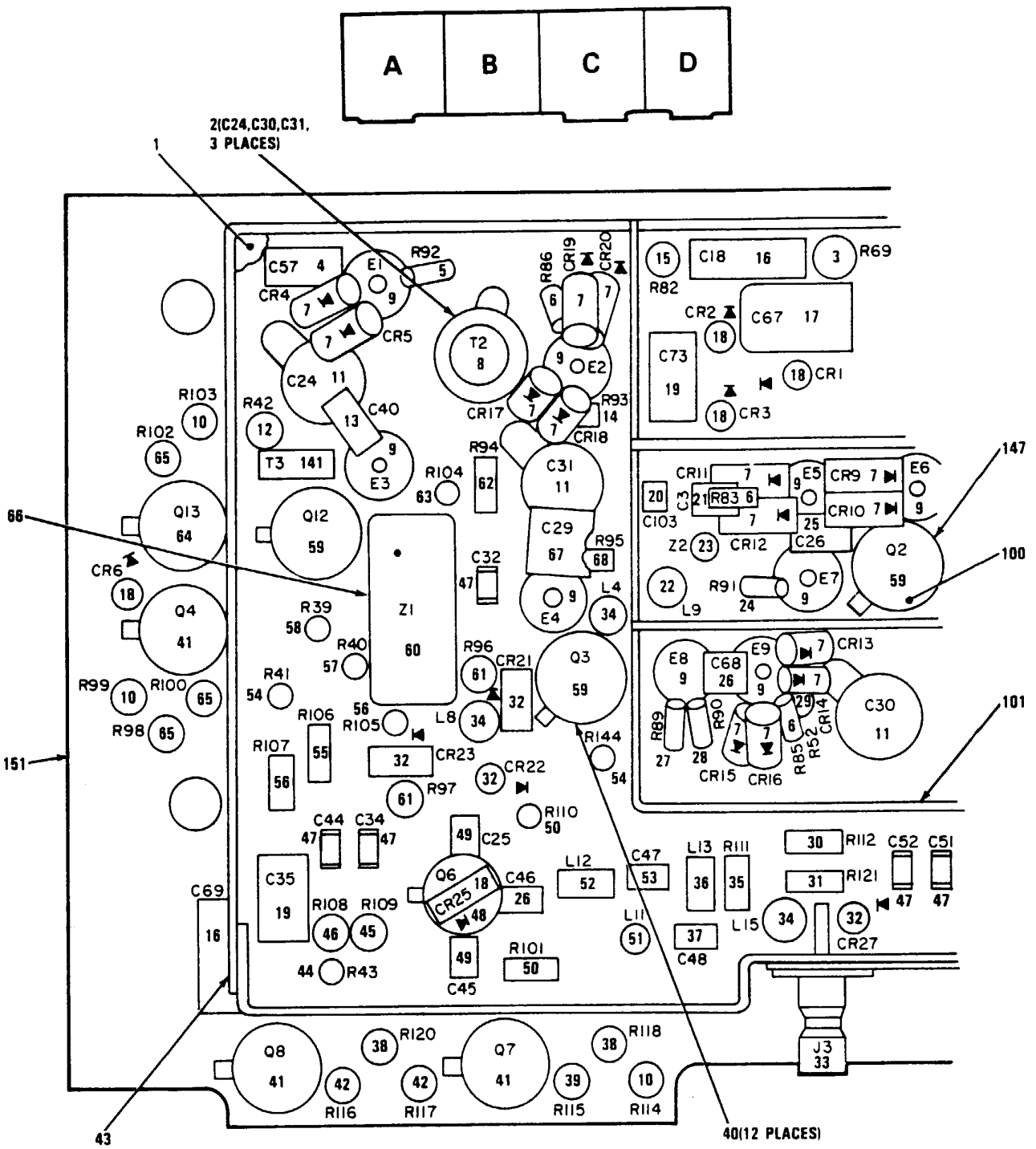


Figure 7-9. Synthesizer Circuit Card Assembly (Sheet 1 of 5)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 7-	+ RNC55H9761FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H9761FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H1872FR	81349	. RESISTOR	1		PADZZ
	+ RNC55H1912FR	81349	. RESISTOR	1		PADZZ
	+ RNC55H1962FR	81349	. RESISTOR	1		PADZZ
	+ RNC55H2002FR	81349	. RESISTOR	1		PADZZ
-127	M39014/02-1234	81349	. CAPACITOR	2		PADZZ
	* M39014/02-1354	81349	. CAPACITOR	2		PADZZ
-128	RCR07G683JS	81349	. RESISTOR	1		PADZZ
-129	RCR05G562JS	81349	. RESISTOR	1		PADZZ
-130	M39014/01-1460	81349	. CAPACITOR	1		PADZZ
-131	RCR07G622JS	81349	. RESISTOR	1		PADZZ
-132	M39014/01-1446	81349	. CAPACITOR	1		PADZZ
	* M39014/01-1566	81349	. CAPACITOR	1		PADZZ
	* M39014/01-1580	81349	. CAPACITOR	1		PADZZ
-133	103008-7	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185627-13)	1		PADZZ
-134	258330-22025	37695	. CAPACITOR, Fixed ceramic .	1		
	258330-2025	37695	. CAPACITOR, Fixed ceramic .	1		
-135	348688-1	37695	. INSULATOR, Shield	1		XB
-136	940485-1	37695	. SHIELD	1		
-137	410900-1	37695	. PRINTED WIRING BOARD	1		XB
7- 8-	811829-801	37695	SYNTHESIZER ASSEMBLY ..... (See fig. 2 for nha)	REF		PAFLD
- 1	914866-801	37695	. CIRCUIT CARD ASSEMBLY, ... Synthesizer (See fig. 9 for bkdn)	1		PADLD
- 2	MS51957-14	96906	. SCREW (AP)	6		PAFZZ
- 3	MS24693C25	96906	. SCREW (AP)	2		PAFZZ
- 4	938404-801	37695	. BRACKET, Synthesizer	1		XB
7- 9-	914866-801	37695	CIRCUIT CARD ASSEMBLY, ... Synthesizer (see fig. 8 for nha)	REF		PADLD
- 1	938648-1	37695	. COVER, Shield	1		XB
- 2	511370-1	37695	. SPACER, Capacitor	3		PADZZ
- 3 +	RNC55H1002FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1002FS	81349	. RESISTOR	1		PADZZ

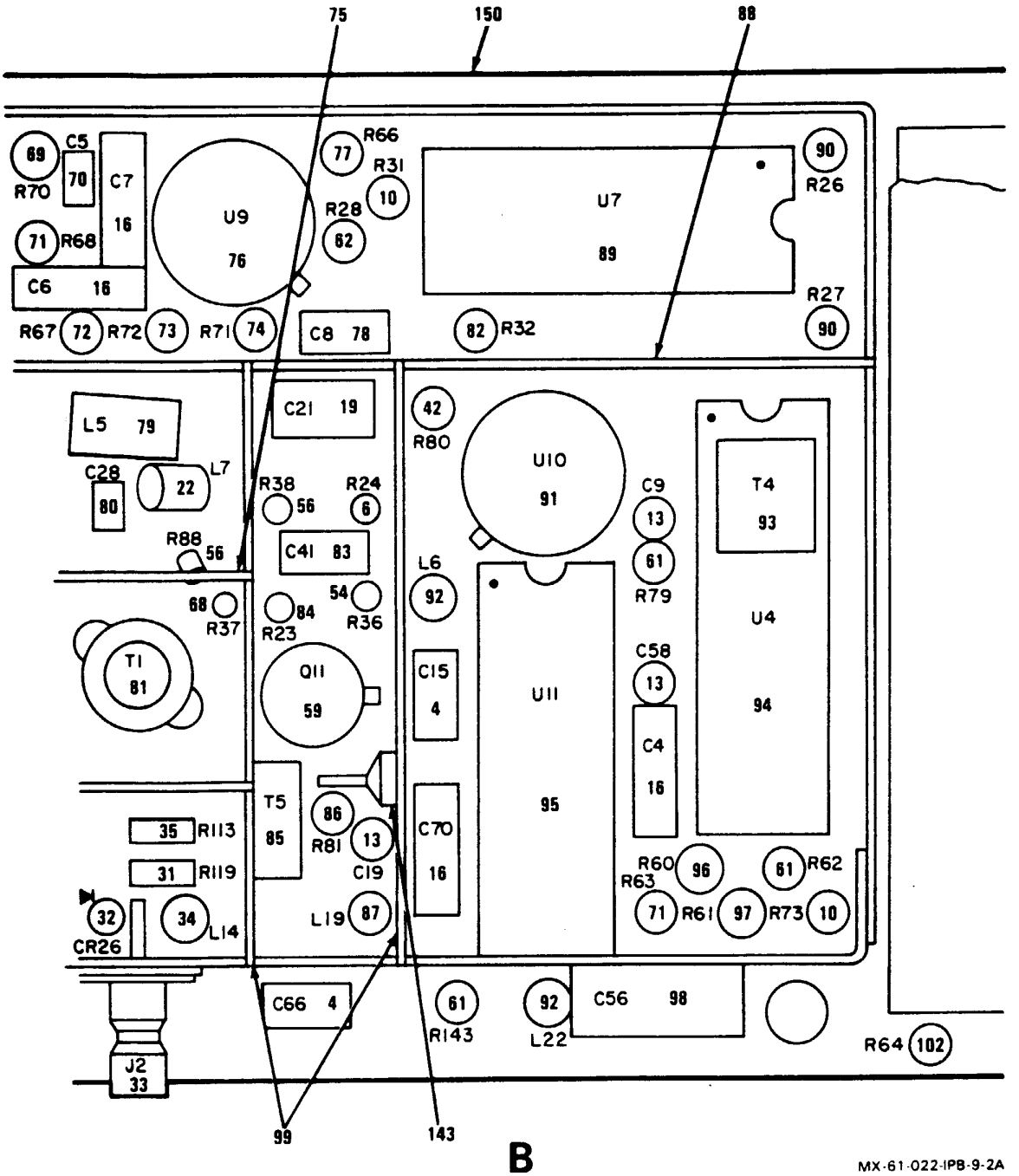
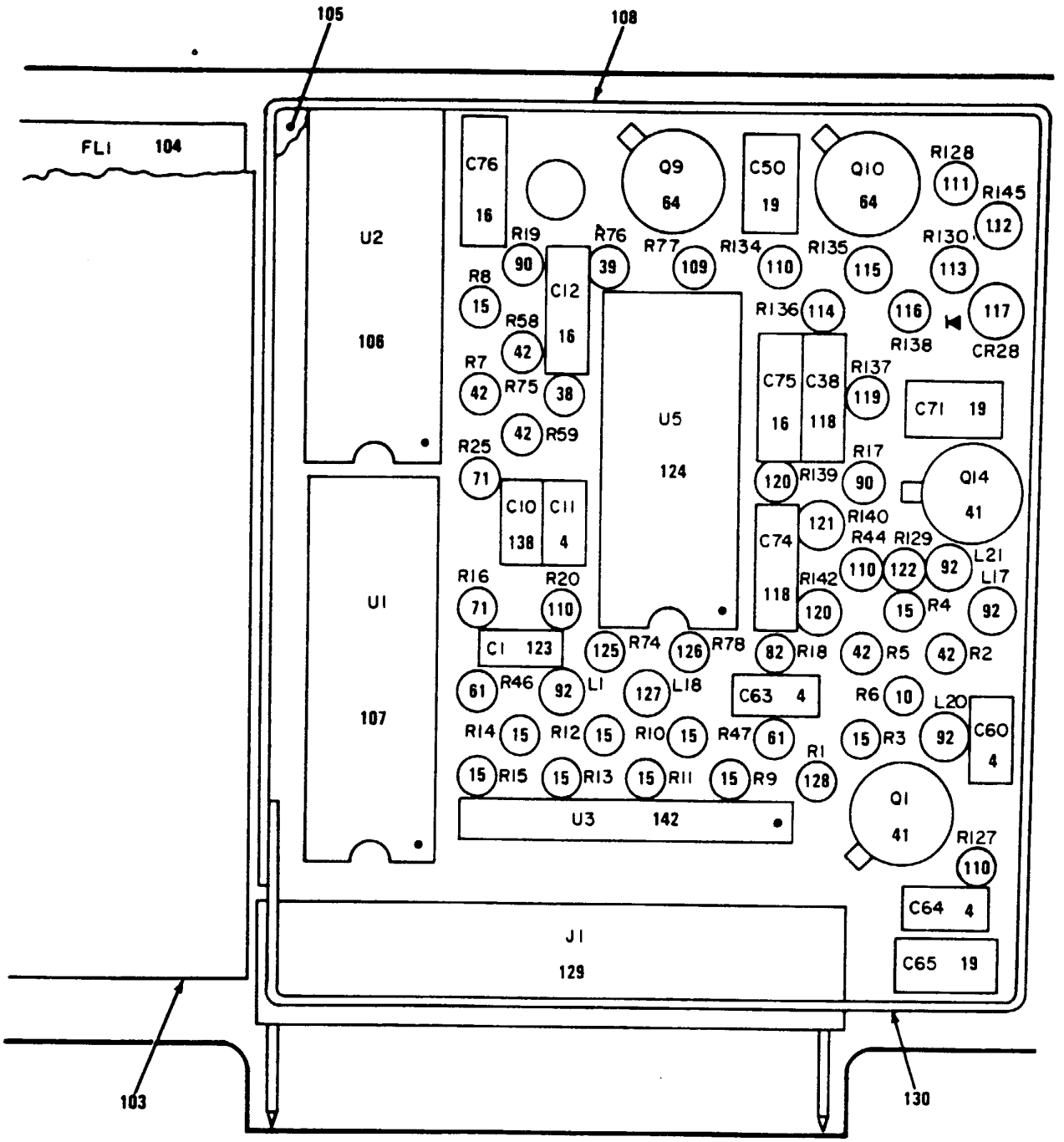


Figure 7-9. Synthesizer Circuit Card Assembly (Sheet 2 of 5)



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MX-61-022-IPB-9-3A

Figure 7-9. Synthesizer Circuit Card Assembly (Sheet 3 of 5)

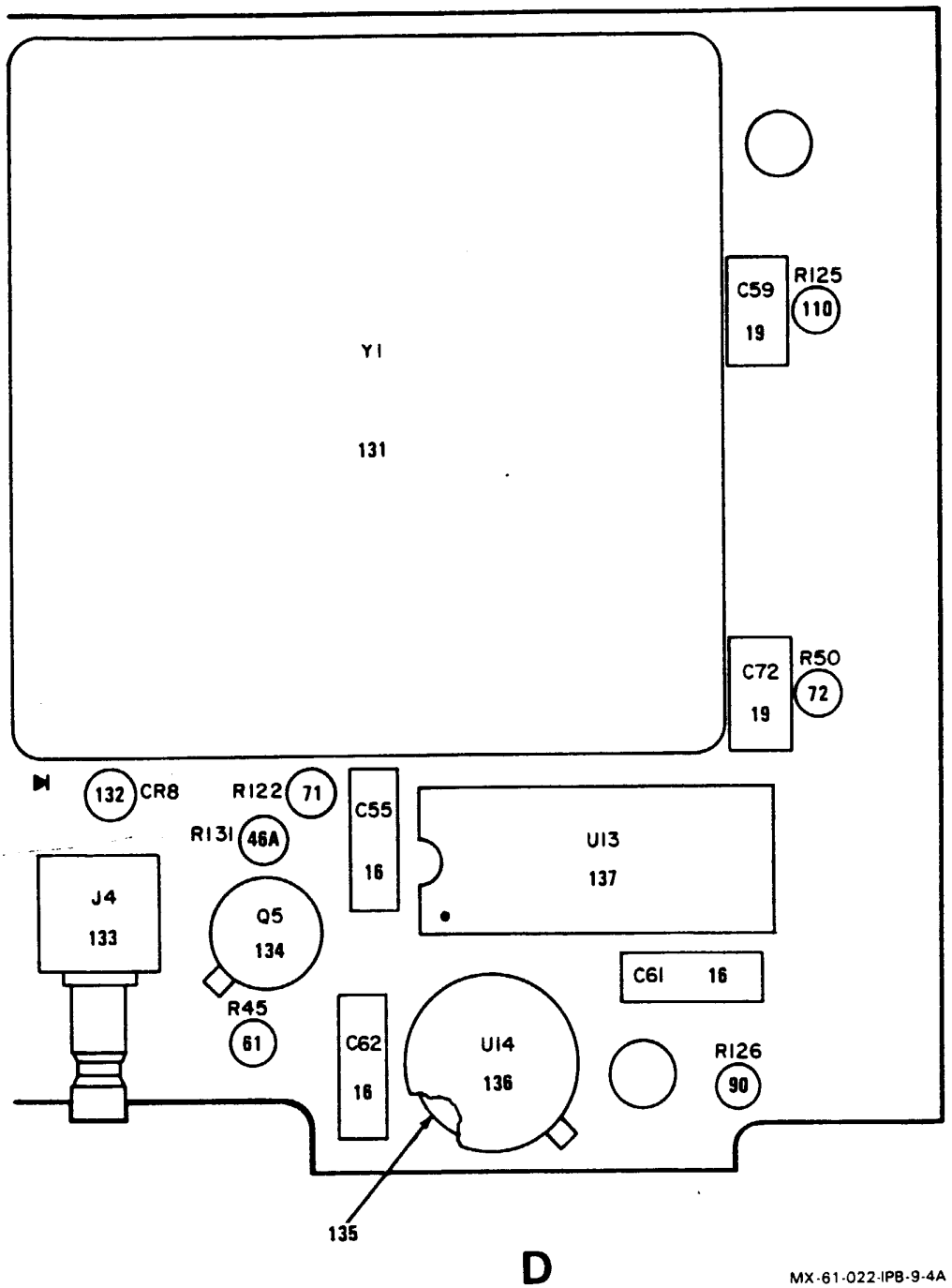


Figure 7-9. Synthesizer Circuit Card Assembly (Sheet 4 of 5)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 9-	+ RNC55H1022FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H1022FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H1052FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H1052FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H1072FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H1072FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H8661FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H8661FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H9531FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H9531FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H9761FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H9761FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H1102FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H1102FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H9091FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H9091FS	81349	. RESISTOR	1		PADZZ
- 4	M39014/01-1237	81349	. CAPACITOR	7		PADZZ
	* M39014/01-1357	81349	. CAPACITOR	7		PADZZ
- 5	RCR05G473JS	81349	. RESISTOR	1		PADZZ
- 6	RCR05G472JS	81349	. RESISTOR	4		PADZZ
- 7	615468-902	37695	. SEMICONDUCTOR DEVICE, ... Diode	14		PADZZ
- 8	368851-4	37695	. COIL, Radio frequency	1		PADZZ
- 9	= AAA-30W-SX-A	20093	. TERMINAL, Feedthru, ... insulated (Magnavox spec cont dwg 205034-10)	9		PADZZ
	= AAA-30W-SX	20093	. TERMINAL, Feedthru, ... insulated (Magnavox spec cont dwg 205034-9)	9		PADZZ
- 10	RCR07G273JS	81349	. RESISTOR	6		PADZZ
- 11	PC25J060	81349	. CAPACITOR	3		PADZZ
	= 5700	91293	. CAPACITOR, Variable ..... (Magnavox spec cont dwg 267933-15)	3		PADZZ
- 12	RCR07G182JS	81349	. RESISTOR	1		PADZZ
- 13	M39014/05-2662	81349	. CAPACITOR	4		PADZZ
	* M39014/05-2661	81349	. CAPACITOR	4		PADZZ
- 14	RCR05G101JS	81349	. RESISTOR	1		PADZZ
- 15	RCR07G103JS	81349	. RESISTOR	11		PADZZ
- 16	M39014/02-1240	81349	. CAPACITOR	12		PADZZ
	* M39014/02-1360	81349	. CAPACITOR	12		PADZZ
- 17	275054-1149	37695	. CAPACITOR, Fixed, ... electrolytic	1		PADZZ
- 18	JANTX1N4454-1	81350	. SEMICONDUCTOR DEVICE	5		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 9- 19	S106R	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-75)	8		PADZZ
- 20	CDR14BG681AGSM	81349	. CAPACITOR	1		PADZZ
=	ATC-100-G-681-B-P-100-SP	29990	. CAPACITOR, Fixed, glass .. (Magnavox spec cont dwg 258300-11181)	1		PADZZ
- 21	QC-1.5UUFPORM 5PCT	95121	. CAPACITOR, Fixed, ... composition (Magnavox spec cont dwg 257977-16)	1		PADZZ
- 22	MS75083-7	96906	. COIL	2		PADZZ
- 23	815016-801	37695	. ELEMENT, Noise filter	1		PADZZ
- 24	RCR05G751JS	81349	. RESISTOR	1		PADZZ
- 25	CDR14BG151DJSM	81349	. CAPACITOR	1		
*	CDR14BG101EGSM	81349	. CAPACITOR	1		PADZZ
=	258300-11265	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
- 26	CDR14BG3R9ECSM	81349	. CAPACITOR	2		PADZZ
*	CDR14BG3R9EBSM	81349	. CAPACITOR	2		PADZZ
=	258300-11627	37695	. CAPACITOR, Fixed ceramic .	2		PADZZ
- 27	RCR05G822JS	81349	. RESISTOR	1		PADZZ
- 28	RCR05G332JS	81349	. RESISTOR	1		PADZZ
- 29	RCR07G162JS	81349	. RESISTOR	1		PADZZ
- 30 +	RCR05G330JS	81349	. RESISTOR	1		PADZZ
+	RCR05G240JS	81349	. RESISTOR	1		PADZZ
+	RCR05G270JS	81349	. RESISTOR	1		PADZZ
+	RCR05G430JS	81349	. RESISTOR	1		PADZZ
+	RCR05G620JS	81349	. RESISTOR	1		PADZZ
+	RCR05G510JS	81349	. RESISTOR	1		PADZZ
+	RCR05G390JS	81349	. RESISTOR	1		PADZZ
- 31	RCR05G102JS	81349	. RESISTOR	2		PADZZ
- 32	619915-901	37695	. SEMICONDUCTOR DEVICE, ... Diode	5		PADZZ
- 33	M39012/95-0001	81349	. CONNECTOR	2		PADZZ
=	16-0209-000	19505	. CONNECTOR, Coaxial ..... (Magnavox spec cont dwg 189175-7)	2		PADZZ
- 34	MS75083-8	96906	. COIL	4		PADZZ
- 35	RCR05G271JS	81349	. RESISTOR	2		PADZZ
- 36	365174-805	37695	. COIL, Radio frequency	1		PADZZ
- 37	CDR14BG2R0ECSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG2R0EBSM	81349	. CAPACITOR	1		PADZZ
=	258300-11620	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
- 38	RCR07G104JS	81349	. RESISTOR	3		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 9- 39	RCR07G223JS	81349	. RESISTOR	2		PADZZ
- 40	7717-7N-WHITE	13103	. INSULATOR, Frequency ..... (Magnavox spec cont dwg 447279-102)	12		PADZZ
- 41	JANTX2N2907A	81349	. TRANSISTOR	5		PADZZ
- 42	RCR07G473JS	81349	. RESISTOR	8		PADZZ
- 43	938652-1	37695	. HOUSING, Shield	1		XB
- 44	RCR05G390JS	81349	. RESISTOR	1		PADZZ
- 45	RCR07G331JS	81349	. RESISTOR	1		PADZZ
- 46 +	RCR07G332JS	81349	. RESISTOR	1		PADZZ
+	RCR07G202JS	81349	. RESISTOR	1		PADZZ
+	RCR07G222JS	81349	. RESISTOR	1		PADZZ
+	RCR07G242JS	81349	. RESISTOR	1		PADZZ
+	RCR07G272JS	81349	. RESISTOR	1		PADZZ
+	RCR07G302JS	81349	. RESISTOR	1		PADZZ
+	RCR07G362JS	81349	. RESISTOR	1		PADZZ
+	RCR07G392JS	81349	. RESISTOR	1		PADZZ
+	RCR07G432JS	81349	. RESISTOR	1		PADZZ
+	RCR07G182JS	81349	. RESISTOR	1		PADZZ
- 46A	RCR07G302JS	81349	. RESISTOR	1		PADZZ
- 47	CDR14BG561BKSM	81349	. CAPACITOR	42		PADZZ
=	7203A471KF	95275	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 255096-94)	42		PADZZ
- 48	645796-901	37695	. TRANSISTOR, NPN	1		PADZZ
- 49	ATC-100-B-101-B-P-500-SP	29990	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258300-11161)	2		PADZZ
- 50	RCR05G180JS	81349	. RESISTOR	2		PADZZ
- 51	365174-806	37695	. COIL, Radio frequency	1		PADZZ
- 52	365174-804	37695	. COIL, Radio frequency	1		PADZZ
- 53	CDR14BG300EGSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG300EFSM	81349	. CAPACITOR	1		PADZZ
=	258300-11348	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
- 54	RCR05G181JS	81349	. RESISTOR	3		PADZZ
- 55 +	RCR05G271JS	81349	. RESISTOR	1		PADZZ
+	RCR05G111JS	81349	. RESISTOR	1		PADZZ
+	RCR05G910JS	81349	. RESISTOR	1		PADZZ
+	RCR05G101JS	81349	. RESISTOR	1		PADZZ
+	RCR05G221JS	81349	. RESISTOR	1		PADZZ
+	RCR05G131JS	81349	. RESISTOR	1		PADZZ
+	RCR05G151JS	81349	. RESISTOR	1		PADZZ
+	RCR05G331JS	81349	. RESISTOR	1		PADZZ
+	RCR05G471JS	81349	. RESISTOR	1		PADZZ
+	RCR05G181JS	81349	. RESISTOR	1		PADZZ

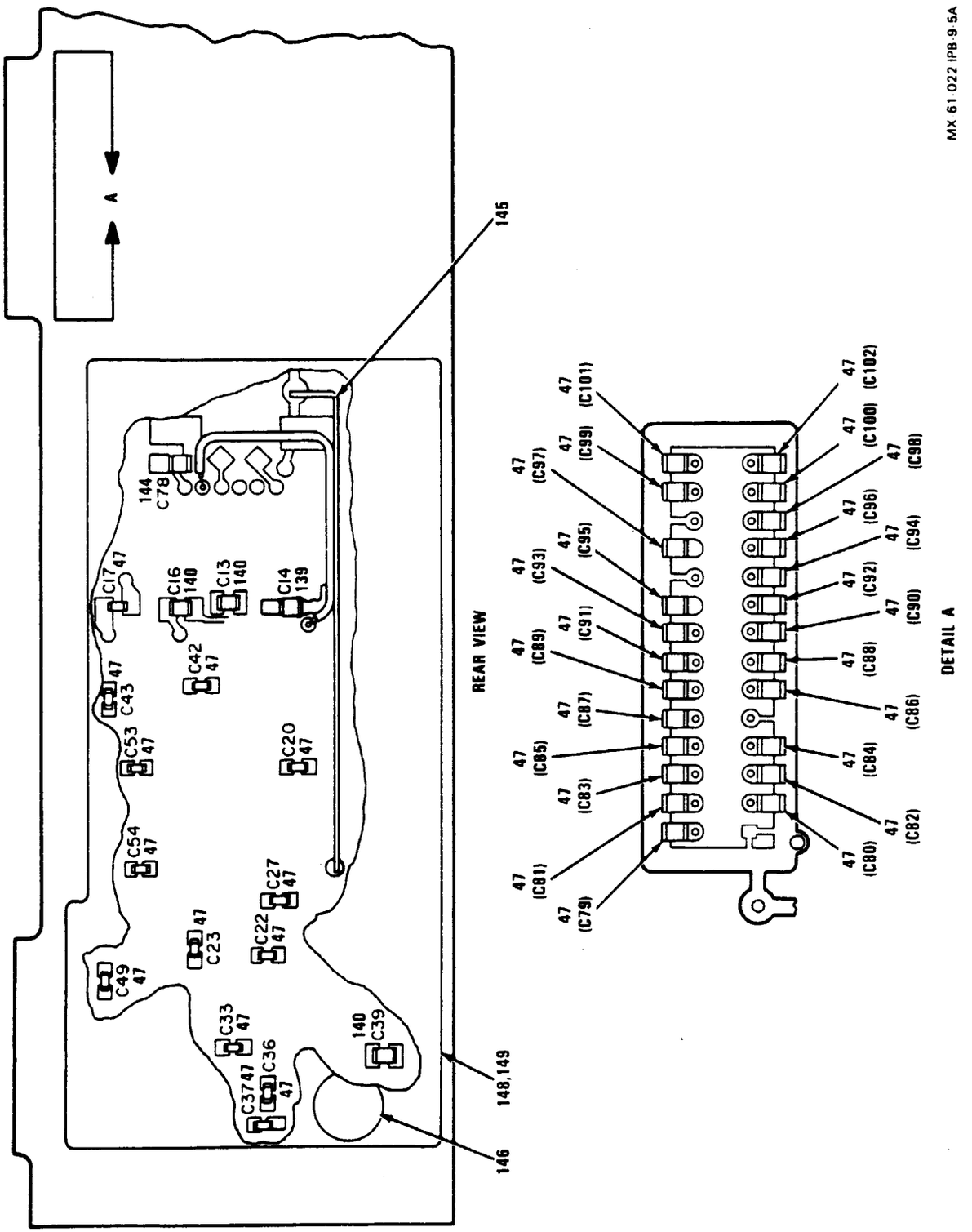


Figure 7-9. Synthesizer Circuit Card Assembly (Sheet 5 of 5)

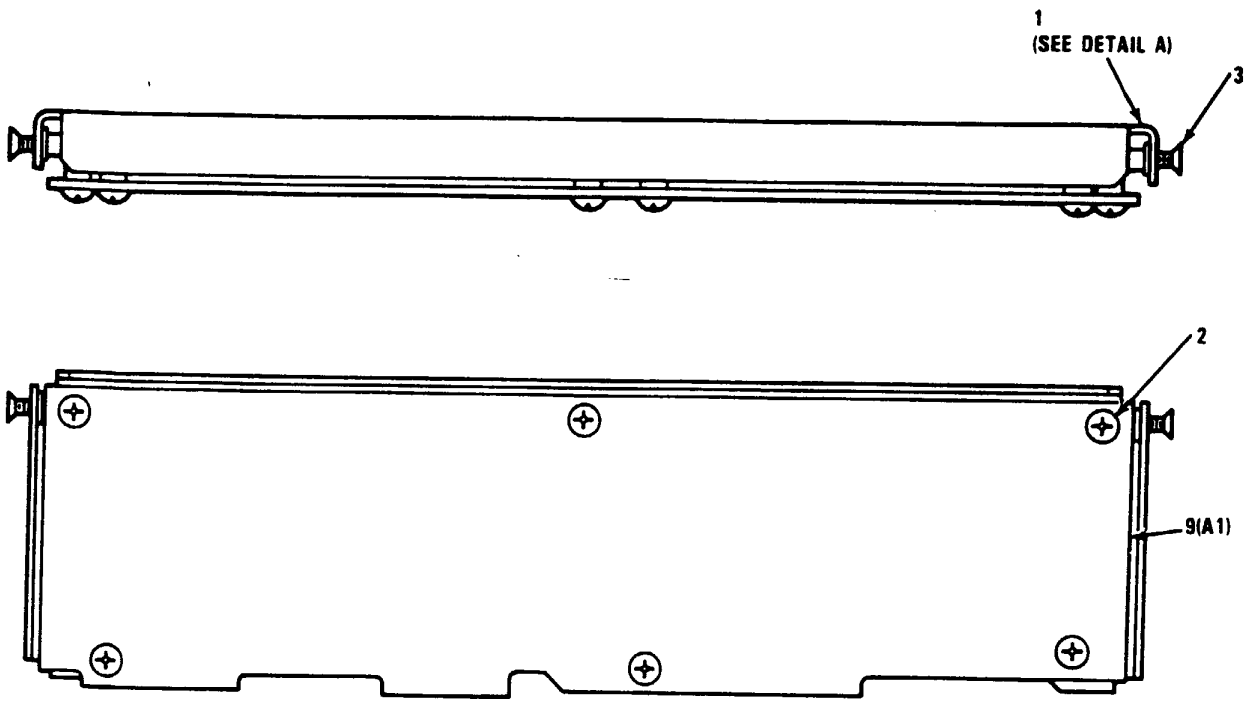
FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 9- 56	RCR05G680JS	81349	. RESISTOR	4		PADZZ
- 57	RCR05G272JS	81349	. RESISTOR	1		PADZZ
- 58	RCR05G682JS	81349	. RESISTOR	1		PADZZ
- 59	616380-901	37695	. TRANSISTOR	4		PADZZ
- 60	TFM-2	15542	. MIXER, Radio frequency ... (Magnavox spec cont dwg 626730-1)	1		PADZZ
- 61	RCR07G102JS	81349	. RESISTOR	8		PADZZ
- 62	RCR05G510JS	81349	. RESISTOR	2		PADZZ
- 63	RCR05G470JS	81349	. RESISTOR	1		PADZZ
- 64	JANTX2N2222A	81350	. TRANSISTOR	3		PADZZ
- 65	RCR07G183JS	81349	. RESISTOR	3		PADZZ
- 66	348755-1	37695	. INSULATOR, RF mixer	1		PADZZ
- 67	UY22111K	73899	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258229-78)	1		PADZZ
- 68	RCR05G221JS	81349	. RESISTOR	2		PADZZ
- 69	RNC55H1102FR	81349	. RESISTOR	1		PADZZ
*	RNC55H1102FS	81349	. RESISTOR	1		PADZZ
- 70	F225R	37695	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-27)	1		PADZZ
- 71	RCR07G100JS	81349	. RESISTOR	5		PADZZ
- 72	RCR07G470JS	81349	. RESISTOR	2		PADZZ
- 73	RCR07G512JS	81349	. RESISTOR	1		PADZZ
- 74	RCR07G303JS	81349	. RESISTOR	1		PADZZ
- 75	939251-1	37695	. PARTITION, Shield	1		XB
- 76	619604-903	37695	. INTEGRATED CIRCUIT	1		PADZZ
- 77	RCR07G393JS	81349	. RESISTOR	1		PADZZ
- 78	CFR06ARA103KM	81349	. CAPACITOR	1		
- 79	365174-814	37695	. COIL, Radio frequency	1		PADZZ
- 80	CDR14BG111EKSM	81349	. CAPACITOR	1		PADZZ
*	CDR14BG111DGSM	81349	. CAPACITOR	1		PADZZ
=	258300-11062	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
- 81	SK651-B	45209	. COIL, Radio frequency .... (Magnavox spec cont dwg 368851-1)	1		PADZZ
- 82	RCR07G752JS	81349	. RESISTOR	2		PADZZ
- 83	M39014/01-1231	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1351	81349	. CAPACITOR	1		PADZZ
- 84	RCR05G752JS	81349	. RESISTOR	1		PADZZ
- 85	365175-812	37695	. COIL, Radio frequency	1		PADZZ
- 86	RCR07G683JS	81349	. RESISTOR	1		PADZZ
- 87	MS75085-11	96906	. COIL	1		PADZZ

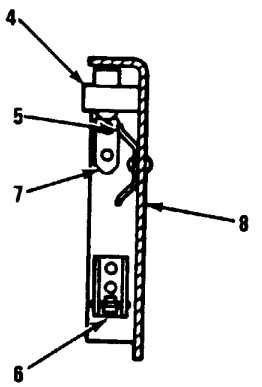
FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 9- 88	939249-1	37695	. PARTITION, Shield	1		PADZZ
- 89	JM38510/12304 BEX	81349	. MICROCIRCUIT	1		PADZZ
	M38510/12304 BEB	81349	. MICROCIRCUIT	1		PADZZ
=	617761-1	37695	. MICROCIRCUIT, Linear	1		PADZZ
- 90	RCR07G220JS	81349	. RESISTOR	5		PADZZ
- 91	616194-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 92	MS75083-13	96906	. COIL	6		PADZZ
- 93	368883-812	37695	. TRANSFORMER, Balum	1		PADZZ
- 94	617763-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 95	616385-1	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 96	RNC55H9091FR	81349	. RESISTOR	1		PADZZ
*	RNC55H9091FS	81349	. RESISTOR	1		PADZZ
- 97	RNC55H1002FR	81349	. RESISTOR	1		PADZZ
*	RNC55H1002FS	81349	. RESISTOR	1		PADZZ
- 98	T330C396010AS	05397	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275054-49)	1		PADZZ
- 99	939250-1	37695	. PARTITION, Shield	2		XB
-100	7717-16N-WHITE	13103	. MOUNTING PAD (Magnavox ... spec cont dwg 445214-102)	1		PADZZ
*	7717-16DAP-WHITE	13193	. MOUNTING PAD	1		PADZZ
-101	738660-1	37695	. PARTITION, Shield	1		XB
-102	RNC55H9090FR	81349	. RESISTOR	1		PADZZ
*	RNC55H9090FS	81349	. RESISTOR	1		PADZZ
-103	940321-1	37695	. SHIELD, Filter	1		XB
-104	45F60	00222	. FILTER, Lowpass ..... (Magnavox spec cont dwg 325274-1)	1		PADZZ
=	MF-532	37695	. FILTER, Lowpass ..... (Magnavox spec cont dwg 325274-1)	1		PADZZ
-105	940233-1	37695	. COVER, Shield	1		XB
-106	JM38510/17601 BEX	81349	. MICROCIRCUIT	1		PADZZ
*	M38510/17601 BEB	81349	. MICROCIRCUIT	1		PADZZ
=	619998-1	37695	. MICROCIRCUIT, Digital	1		PADZZ
-107	645794-901	37695	. MICROCIRCUIT, Linear	1		PADZZ
-108	940231-1	37695	. HOUSING, Shield	1		XB
-109	RCR07G682JS	81349	. RESISTOR	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 9-110	RCR07G101JS	81349	. RESISTOR	5		PADZZ
-111	RCR07G751JS	81349	. RESISTOR	1		PADZZ
-112 +	RNC55H5361FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H5361FS	81349	. RESISTOR	1		PADZZ
+	RNC55H4121FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H4121FS	81349	. RESISTOR	1		PADZZ
+	RNC55H4641FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H4641FS	81349	. RESISTOR	1		PADZZ
+	RNC55H6041FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H6041FS	81349	. RESISTOR	1		PADZZ
-113 +	RNC55H2322FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2322FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2262FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2262FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2372FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2372FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2432FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2432FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2492FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2492FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2552FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2552FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2612FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2612FS	81349	. RESISTOR	1		PADZZ
-114 +	RCR07G103JS	81349	. RESISTOR	1		PADZZ
+	RCR07G183JS	81349	. RESISTOR	1		PADZZ
+	RCR07G123JS	81349	. RESISTOR	1		PADZZ
+	RCR07G153JS	81349	. RESISTOR	1		PADZZ
+	RCR07G203JS	81349	. RESISTOR	1		PADZZ
-115	RCR07G561JS	81349	. RESISTOR	1		PADZZ
-116	RCR07G271JS	81349	. RESISTOR	1		PADZZ
-117	JANTX1N825-1	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
-118	M39014/02-1230	81349	. CAPACITOR	2		PADZZ
*	M39014/02-1350	81349	. CAPACITOR	2		PADZZ
-119	RCR07G472JS	81349	. RESISTOR	1		PADZZ
-120	RNC55H1872BR	81349	. RESISTOR	2		PADZZ
*	RNC55H1872BS	81349	. RESISTOR	2		PADZZ
-121	RNC55H3012FR	81349	. RESISTOR	1		PADZZ
*	RNC55H3012FS	81349	. RESISTOR	1		PADZZ
-122 +	RCR07G201JS	81349	. RESISTOR	1		PADZZ
+	RCR07G221JS	81349	. RESISTOR	1		PADZZ
+	RCR07G241JS	81349	. RESISTOR	1		PADZZ
+	RCR07G301JS	81349	. RESISTOR	1		PADZZ
+	RCR07G431JS	81349	. RESISTOR	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 9-	+ RCR07G511JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G621JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G561JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G361JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G391JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G471JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G681JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G181JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G271JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G331JS	81349	. RESISTOR	1		PADZZ
-123	M39014/01-1213	81349	. CAPACITOR	1		PADZZ
	* M39014/01-1333	81349	. CAPACITOR	1		PADZZ
-124	JM38510/11001 BCX	81349	. MICROCIRCUIT	2		PADZZ
	= 615794-901	37695	. MICROCIRCUIT, Linear	1		
-125	RCR07G275JS	81349	. RESISTOR	1		PADZZ
-126	RCR07G823JS	81349	. RESISTOR	1		PADZZ
-127	MS75084-16	96906	. COIL	1		PADZZ
-128	RCR07G474JS	81349	. RESISTOR	1		PADZZ
-129	103008-07	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185627-13)	1		PADZZ
-130	940232-1	37695	. HOUSING, Shield	1		XB
-131	= 252-4819-4	27802	. OSCILLATOR, Radio ..... frequency (Magnavox spec cont dwg 626164-4)	1		PADZZ
	= 252-4819-6	27802	. OSCILLATOR, Radio ..... frequency (Magnavox spec cont dwg 626164-6)	1		PADZZ
-132	JANTX1N751A1	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
-133	M39012/96-0001	81349	. CONNECTOR	1		PADZZ
	= 16-0210-002	69505	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 189175-8)	1		PADZZ
-134	645733-901	37695	. SEMICONDUCTOR DEVICE	1		
-135	7717-15N	13103	. INSULATOR, Transistor .... (Magnavox spec cont dwg 447173-1)	1		PADZZ
	= 7717-15DAP	13103	. INSULATOR, Transistor	1		PADZZ
-136	616195-910	37695	. MICROCIRCUIT, Linear	1		PADZZ
-137	616501-902	37695	. MICROCIRCUIT, Linear	1		PADZZ
-138	M39014/01-1449	81349	. CAPACITOR	1		PADZZ
	* M39014/01-1569	81349	. CAPACITOR	1		PADZZ

FIGURE AND INDEX NUMBER		PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 9-	+	RCR07G511JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G621JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G561JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G361JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G391JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G471JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G681JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G181JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G271JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G331JS	81349	. RESISTOR	1		PADZZ
-123		M39014/01-1213	81349	. CAPACITOR	1		PADZZ
	*	M39014/01-1333	81349	. CAPACITOR	1		PADZZ
-124		JM38510/11001 BCX	81349	. MICROCIRCUIT	2		PADZZ
	=	615794-901	37695	. MICROCIRCUIT, Linear	1		
-125		RCR07G275JS	81349	. RESISTOR	1		PADZZ
-126		RCR07G823JS	81349	. RESISTOR	1		PADZZ
-127		MS75084-16	96906	. COIL	1		PADZZ
-128		RCR07G474JS	81349	. RESISTOR	1		PADZZ
-129		103008-07	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185627-13)	1		PADZZ
-130		940232-1	37695	. HOUSING, Shield	1		XB
-131	=	252-4819-4	27802	. OSCILLATOR, Radio ..... frequency (Magnavox spec cont dwg 626164-4)	1		PADZZ
	=	252-4819-6	27802	. OSCILLATOR, Radio ..... frequency (Magnavox spec cont dwg 626164-6)	1		PADZZ
-132		JANTX1N751A1	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
-133		M39012/96-0001	81349	. CONNECTOR	1		PADZZ
	=	16-0210-002	69505	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 189175-8)	1		PADZZ
-134		645733-901	37695	. SEMICONDUCTOR DEVICE	1		
-135		7717-15N	13103	. INSULATOR, Transistor .... (Magnavox spec cont dwg 447173-1)	1		PADZZ
	=	7717-15DAP	13103	. INSULATOR, Transistor	1		PADZZ
-136		616195-910	37695	. MICROCIRCUIT, Linear	1		PADZZ
-137		616501-902	37695	. MICROCIRCUIT, Linear	1		PADZZ
-138		M39014/01-1449	81349	. CAPACITOR	1		PADZZ
	*	M39014/01-1569	81349	. CAPACITOR	1		PADZZ





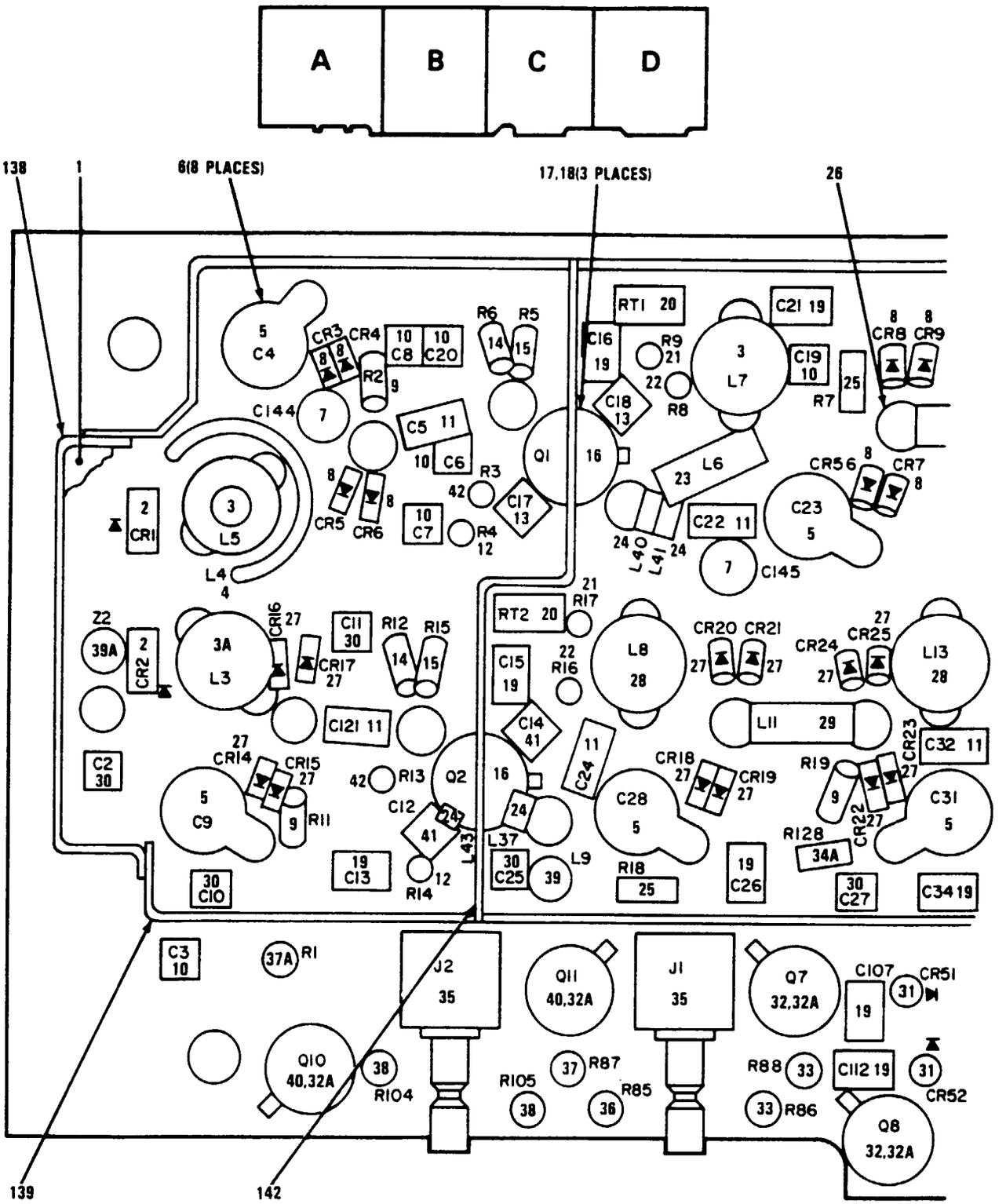
DETAIL A

REFERENCE DESIGNATIONS ARE ABBREVIATED.
PREFIX WITH A1A1A4.

MX-81-022-IPB-10
REF MX DWG 811826-881 REV F
PL 811826-881 REV H

Figure 7-10. Main Receiver Assembly

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7- 9-139	E050U/81K	20932	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258268-1232)	1		PADZZ
-140	CDR14BG102AMSM	81349	. CAPACITOR	3		PADZZ
*	CDR14BG102AGSM	81349	. CAPACITOR	3		PADZZ
=	255096-80	37695	. CAPACITOR, Fixed ceramic .	3		PADZZ
-141	368830-827	37695	. TRANSFORMER, Radio ..... frequency	1		PADZZ
-142	M8340105M4703 JC	81349	. RESISTOR	1		PADZZ
*	M8340105M4703 GC	81349	. RESISTOR	1		PADZZ
-143	205034-6	37695	. TERMINAL, Feedthru	1		XB
-144	VJ1210Y224MF	95275	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258268-1056)	1		PADZZ
=	VJ1210Y224	95275	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258268-1056)	1		PADZZ
-145	940413-1	37695	. SHIELD, Synthesizer	1		XB
-146	513917-2	37695	. COVER	3		XB
-147	346281-1	37695	. SPACER	1		XB
-148	939314-1	37695	. COVER	1		XB
-149	349605-1	37695	. INSULATOR, Cover	1		XB
-150	938653-1	37695	. PARTITION, Shield	1		XB
-151	410901-1	37695	. PRINTED WIRING BOARD	1		XB
7-10-	811826-801	37695	RECEIVER ASSEMBLY, Main .... (See fig. 2 for nha)	REF		PAFLD
- 1	938402-801	37695	. BRACKET, Main receiver ...	1		XB
- 2	MS51957-14	96906	. SCREW (AP)	6		PAFZZ
- 3	MS24693C25	96906	. SCREW (AP)	2		PAFZZ
- 4	514527-101	37695	. . INSERT, Screw thread ...	6		PAFZZ
- 5	165467-1	37695	. . CONTACT STRIP	1		XB
	MS20470AD2-2	96906	. . RIVET (AP)	2		XB
- 6	RMLHA27M2860-62	72962	. . NUT, Self-locking ..... (Magnavox spec cont dwg 107295-2)	2		XB
	MS20426AD2-3	96906	. . RIVET (AP)	2		XB
- 7	NAS696C06M	80205	. . NUT	2		XB
	MS2046AD2-3	96906	. . RIVET (AP)	2		XB
- 8	938402-1	37695	. . BRACKET	1		XB



REFERENCE DESIGNATIONS ARE ABBREVIATED.
PREFIX WITH A1A1A4A1.

A

MX-61-022-IPB-11-1A
REF MX DWG 914864-801 REV P
PL 914864-801 REV AY

Figure 7-11. Main Receiver Circuit Card Assembly (Sheet 1 of 5)

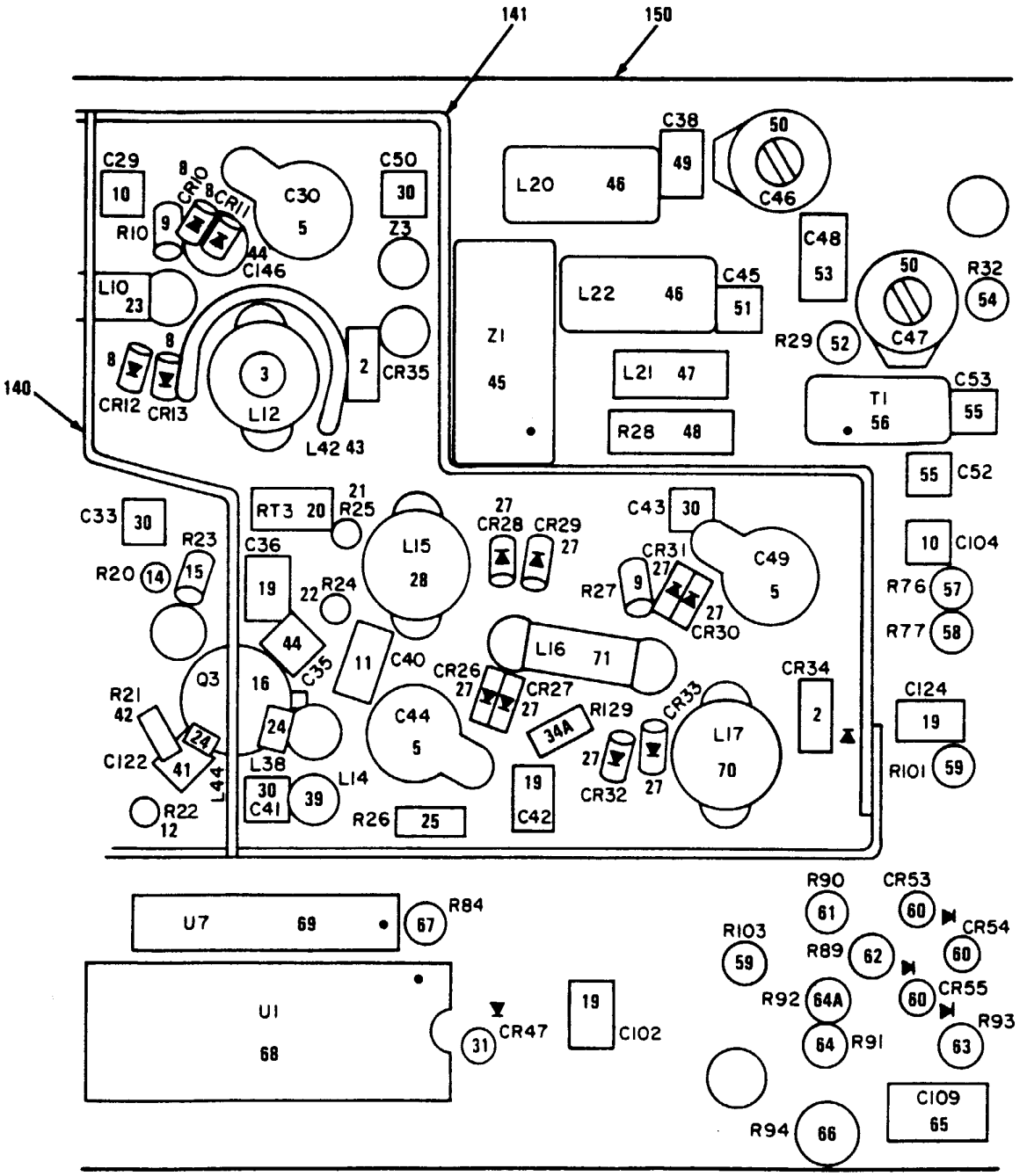
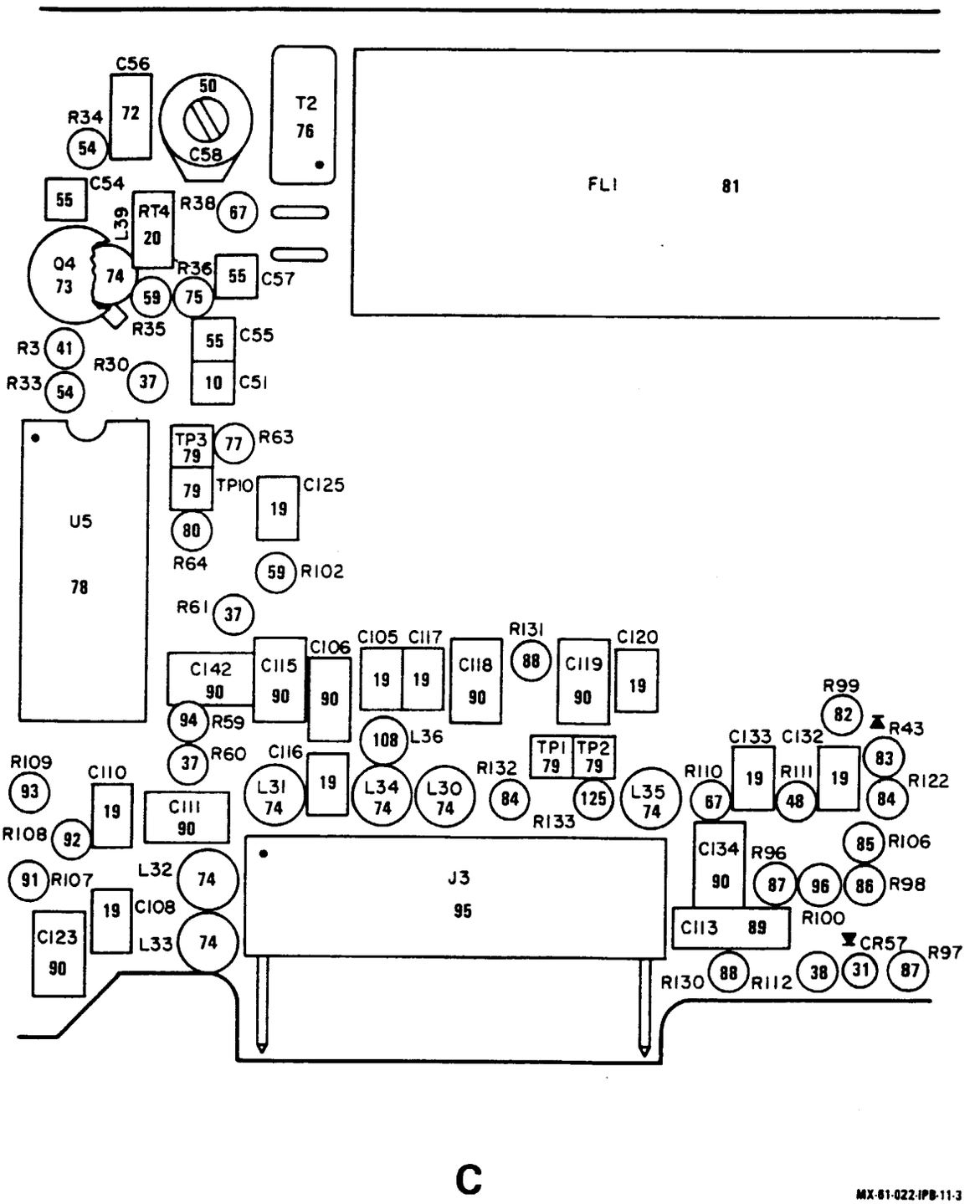


Figure 7-11. Main Receiver Circuit Card Assembly (Sheet 2 of 5)



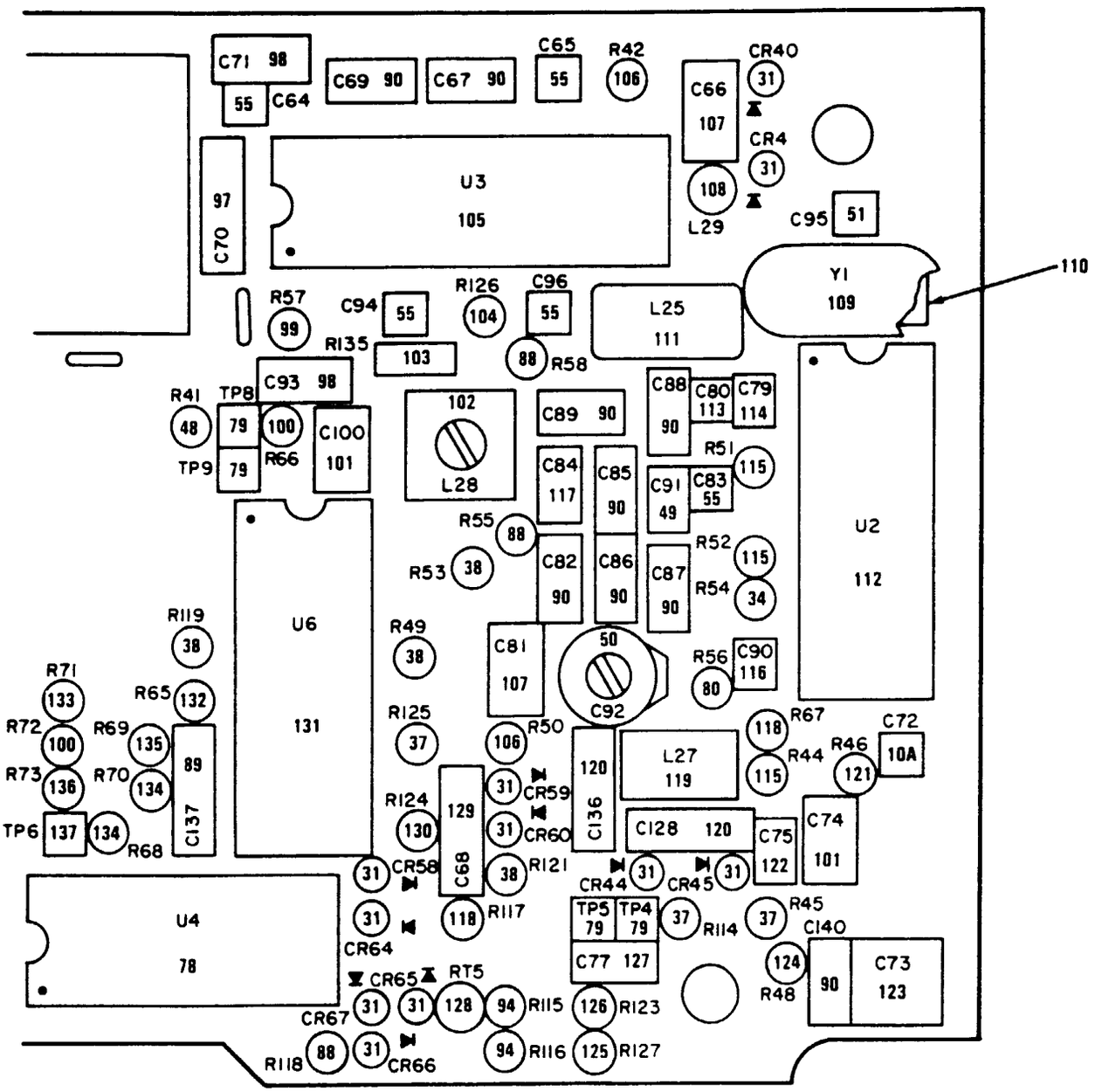
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MX-81-022-IPB-11-3

Figure 7-11. Main Receiver Circuit Card Assembly (Sheet 3 of 5)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-10- 9	914864-801	37695	. CIRCUIT CARD ASSEMBLY, ... Main receiver (See fig. 11 for bkdn)	1		PADLD
7-11-	914864-801	37695	CIRCUIT CARD ASSEMBLY, ... Main receiver (See fig. 10 for nha)	REF		PADLD
- 1	938647-1	37695	. COVER, Shield	1		XB
- 2	619915-901	37695	. SEMICONDUCTOR DEVICE, ... Diode	4		PADZZ
- 3	081976RS1	00779	. COIL, Radio frequency .... (Magnavox spec cont dwg 368851-3)	3		PADZZ
- 3A	368851-5	37695	. COIL, Radio frequency	1		PADZZ
- 4	365190-1	37695	. COIL, Radio frequency	1		PADZZ
- 5	PC25J060	81349	. CAPACITOR	8		PADZZ
=	5700	91293	. CAPACITOR, Variable ..... (Magnavox spec cont dwg 267933-15)	8		PADZZ
- 6	511370-1	37695	. SPACER, Capacitor	8		PADZZ
- 7	QC-2.2UUFPORM 5PCT	95121	. CAPACITOR, Fixed, ... composition (Magnavox spec cont dwg 257977-18)	2		PADZZ
- 8	646264-901	37695	. SEMICONDUCTOR DEVICE, ... Diode	12		PADZZ
- 9	RCR05G104JS	81349	. RESISTOR	5		PADZZ
- 10	CK05BX122K	81349	. CAPACITOR	9		PADZZ
=	C315C102K5R5CA	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258329-21099)	9		PADZZ
- 10A	CDR01BX102BKSP	81349	. CAPACITOR	1		
- 11	UY22111K	73899	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258229-78)	6		PADZZ
- 12	RCR05G332JS	81349	. RESISTOR	3		PADZZ
- 13	CDR14BG102AKSM	81349	. CAPACITOR	2		PADZZ
*	CDR14BG102AGSM	81349	. CAPACITOR	2		PADZZ
=	258300-11085	37695	. CAPACITOR, Fixed ceramic .	2		PADZZ
- 14	RCR05G274JS	81349	. RESISTOR	3		PADZZ
- 15	RCR05G563JS	81349	. RESISTOR	3		PADZZ
- 16	JANTX3N204	81350	. TRANSISTOR	3		PADZZ
=	615238-904	37695	. TRANSISTOR	3		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-11- 17	7717-16N-WHITE	13103	. INSULATOR, Transistor .... (Magnavox spec cont dwg 445214-102)	3		PADZZ
=	7717-16DAP-WHITE	13103	. INSULATOR, Transistor .... (Magnavox spec cont dwg 445214-102)	3		PADZZ
- 18	346281-1	37695	. SPACER	3		XB
- 19	CK51BX103K	81349	. CAPACITOR	21		PADZZ
=	CW15C103K	16546	. CAPACITOR (Magnavox spec . cont dwg 258329-1024)	21		PADZZ
=	CW15C103K	16546	. CAPACITOR (Magnavox spec . cont dwg 258328-21024)	21		PADZZ
=	150-050-W5R-103K	51642	. CAPACITOR (Magnavox spec . cont dwg 258329-1024)	21		PADZZ
=	150-050-W5R-103K	51642	. CAPACITOR (Magnavox spec . cont dwg 258329-21024)	21		PADZZ
- 20	15DC102K-EC-S	15454	. RESISTOR, Thermal ..... (Magnavox spec cont dwg 238283-1)	4		PADZZ
- 21	RCR05G511JS	81349	. RESISTOR	3		PADZZ
- 22	RCR05G270JS	81349	. RESISTOR	3		PADZZ
- 23	MS75083-13	96906	. COIL	2		PADZZ
- 24	21-172-J	33062	. SHIELDING BEAD, ... Electronic (Magnavox spec cont dwg 657907-1)	6		XB
- 25	RCR05G100JS	81349	. RESISTOR	3		PADZZ
- 26	SE089B02	81349	. TERMINAL STUD	14		PADZZ
=	209467-901	37695	. TERMINAL, Feedthru	14		PADZZ
- 27	616543-902	37695	. SEMICONDUCTOR DEVICE, ... Diode	20		PADZZ
- 28	365195-1	37695	. COIL, Radio frequency	3		PADZZ
- 29	MS75083-6	96906	. COIL	1		PADZZ
- 30	CK50BX471K	81349	. CAPACITOR	9		PADZZ
=	C315C471K5R5CA	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258329-21098)	9		
- 31	JANTX1N4454-1	81350	. SEMICONDUCTOR DEVICE	15		PADZZ
- 32	JANTX2N2907A	81350	. TRANSISTOR	2		PADZZ
- 32A	7717-46N-WHITE	13103	. INSULATOR, Transistor .... (Magnavox spec cont. dwg 445214-106)	4		PADZZ
- 33	RCR07G152JS	81349	. RESISTOR	2		PADZZ
- 34	RCR07G473JS	81349	. RESISTOR	1		PADZZ
- 34A=	RCR07G912JS	81349	. RESISTOR	2		PADZZ
=	RCR07G153JS	81349	. RESISTOR	2		PADZZ
=	RCR07G333JS	81349	. RESISTOR	2		PADZZ



D

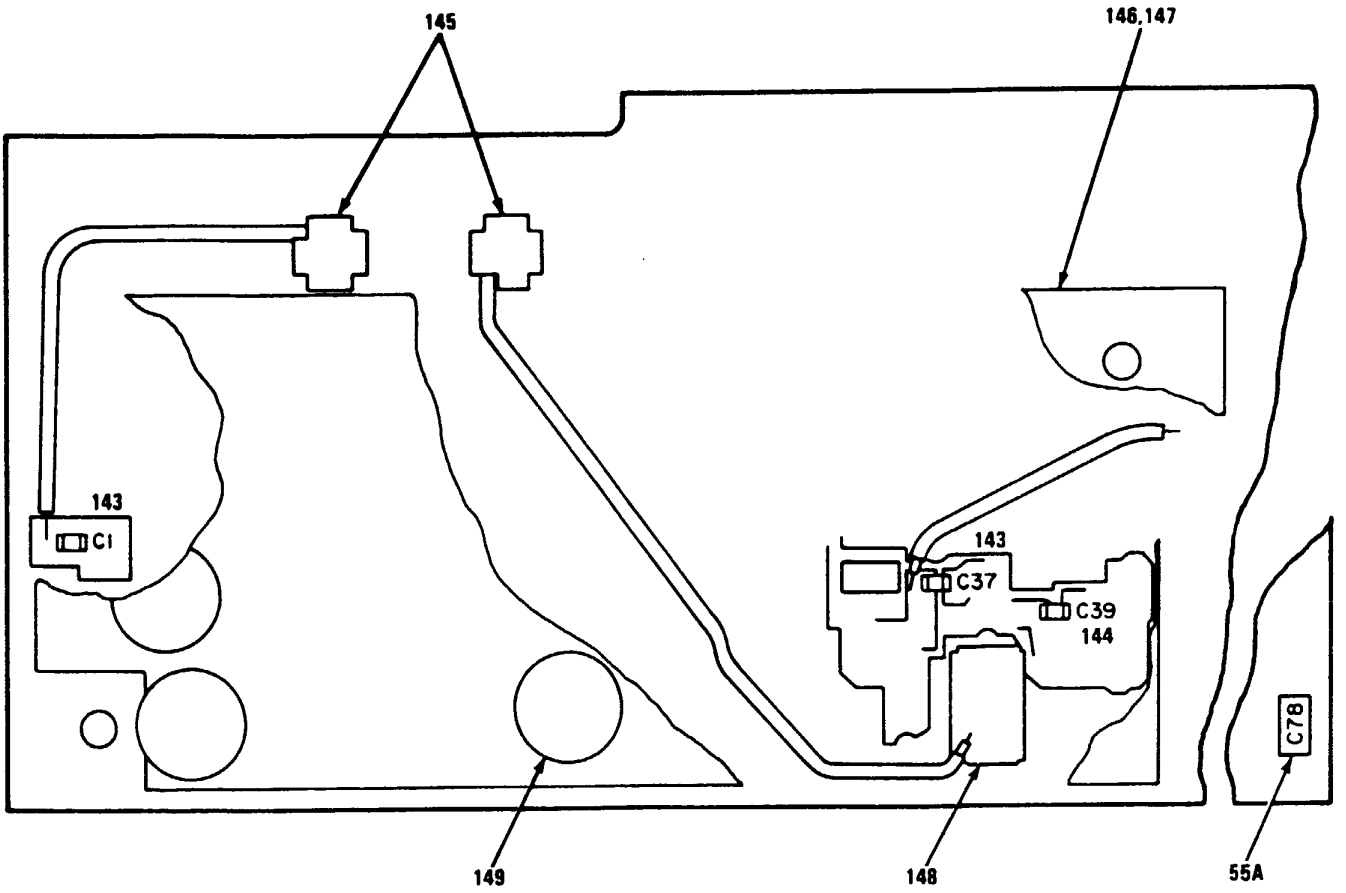
MX-61-022-IPB-11-4A

Figure 7-11. Main Receiver Circuit Card Assembly (Sheet 4 of 5)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-11-	= RCR07G473JS	81349	. RESISTOR	2		PADZZ
	= RCR07G223JS	81349	. RESISTOR	2		PADZZ
- 35	M39012/96-0001	81349	. CONNECTOR	2		PADZZ
	= 16-0210-002	19505	. CONNECTOR, Coaxial ..... (Magnavox spec cont dwg 189175-8)	2		PADZZ
- 36	RCR07G272JS	81349	. RESISTOR	1		PADZZ
- 37	RCR07G332JS	81349	. RESISTOR	7		PADZZ
- 37A	RCR07G162JS	81349	. RESISTOR	1		
- 38	RCR07G103JS	81349	. RESISTOR	7		PADZZ
- 39	MS75083-8	96906	. COIL	2		PADZZ
- 39A	815016-802	37695	. POWER SUPPLY	2		PADZZ
- 40	JANTX2N2222A	81350	. TRANSISTOR	2		PADZZ
- 41	CDR14BG471CMSM	81349	. CAPACITOR	4		PADZZ
	* CDR14BG471CFSM	81349	. CAPACITOR	4		PADZZ
	= 258300-11077	37695	. CAPACITOR, Fixed ceramic .	4		PADZZ
- 42	RCR05G183JS	81349	. RESISTOR	3		PADZZ
- 43	365190-2	37695	. COIL	1		PADZZ
- 44	257977-24	37695	. CAPACITOR, Fixed, ... composition	1		PADZZ
- 45	TFM-2	15542	. MIXER, Radio frequency ... (Magnavox spec cont dwg 626730-1)	1		PADZZ
- 46	365175-803	37695	. COIL, Radio frequency	2		PADZZ
- 47	MS75083-3	96906	. COIL	1		PADZZ
- 48	RCR07G510JS	81349	. RESISTOR	3		PADZZ
- 49	CN10C560J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2014)	2		PADZZ
	= CN10C560J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22014)	2		PADZZ
	= CN10C560G	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2014)	2		PADZZ
	= CN10C560G	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258830-22014)	2		PADZZ
- 50	CV35A250	81349	. CAPACITOR	4		PADZZ
	= 265011-17	37695	. CAPACITOR, Variable, ... ceramic	4		PADZZ
- 51	CN10C750J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2107)	2		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-11-	CN10C750J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22107)	2		PADZZ
=	100-050-NPO-750J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2107)	2		PADZZ
=	100-050-NPO-750J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22107)	2		PADZZ
- 52	RCR07G822JS	81349	. RESISTOR	1		PADZZ
- 53	200-100-N220-820J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 255055-83)	1		PADZZ
=	RPE113R2G820J100V	18796	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 255055-83)	1		PADZZ
- 54	RCR07G563JS	81349	. RESISTOR	3		PADZZ
- 55	CK05BX392K	81349	. CAPACITOR	10		
=	CN10C240D	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258329-21101)	10		PADZZ
- 56A	CDR01BX332BKSP	81349	. CAPACITOR	1		
- 56	365175-806	37695	. COIL, Radio frequency	1		PADZZ
- 56A	RCR07G274JS	81349	. RESISTOR	1		PADZZ
- 57	RCR07G183JS	81349	. RESISTOR	1		PADZZ
- 58	RCR07G683JS	81349	. RESISTOR	1		PADZZ
- 59	RCR07G270JS	81349	. RESISTOR	4		PADZZ
- 60	JANTX1N5712	81349	. SEMICONDUCTOR DEVICE	3		PADZZ
=	615485-1	37695	. SEMICONDUCTOR DEVICE, ... Diode	3		PADZZ
- 61 +	RNC55H2211FR	81349	. RESISTOR	1		PADZZ
+	RNC55H3091FR	81349	. RESISTOR	1		
+	RNC55H1652FR	81349	. RESISTOR	1		PADZZ
*	RNC55H2211FS	81349	. RESISTOR	1		PADZZ
- 62 +	RNC55H5112FR	81349	. RESISTOR	1		PADZZ
+	RNC55H5902FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H5902FS	81349	. RESISTOR	1		PADZZ
- 63	RNC55H7501FR	81349	. RESISTOR	1		PADZZ
*	RNC55H7501FS	81349	. RESISTOR	1		PADZZ
- 64 +	RNC55H3012FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H3012FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2842FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2842FS	81349	. RESISTOR	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-11- 64A	RNC55H7151FR	81349	. RESISTOR	1		PADZZ
+	RNC55H9091FR	81349	. RESISTOR	1		PADZZ
*	RNC55H7151FS	81349	. RESISTOR	1		PADZZ
- 65	S106R	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-75)	1		PADZZ
- 66	RNC55H1542FR	81349	. RESISTOR	1		PADZZ
*	RNC55H1542FS	81349	. RESISTOR	1		PADZZ
- 67	RCR07G100JS	81349	. RESISTOR	3		PADZZ
- 68	JM38510/17601 BEX	81349	. MICROCIRCUIT	1		PADZZ
*	M38510/17601 BEB	81349	. MICROCIRCUIT	1		PADZZ
=	619998-1	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 69	M8340104M4703 JC	81349	. RESISTOR	1		PADZZ
*	M8340104M4703 GC	81349	. RESISTOR	1		PADZZ
- 70	SK651A	00779	. COIL, Radio frequency .... (Magnavox spec cont dwg 368851-2)	1		PADZZ
- 71	MS75083-6	96906	. COIL	1		PADZZ
- 72	200-100-N330-4302J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 255055-82)	1		PADZZ
- 73	615238-905	37695	. TRANSISTOR	1		PADZZ
- 74	56-590-65/4B	02114	. SHIELDING BEAD, ... Electronic (Magnavox spec cont dwg 657867-2)	7		XB
- 75	RCR07G911JS	81349	. RESISTOR	1		PADZZ
- 76	365175-807	37695	. COIL, Radio frequency	1		PADZZ
- 77 +	RNC55H2002FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2002FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1742FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1742FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1822FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1822FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1912FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1912FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2102FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2102FS	81349	. RESISTOR	1		PADZZ
	RNC55H2262FR	81349	. RESISTOR	1		PADZZ
+	RNC55H2322FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2322FS	81349	. RESISTOR	1		PADZZ



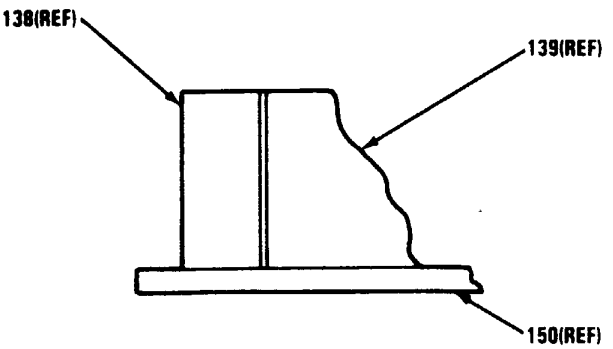


Figure 7-11. Main Receiver Circuit Card Assembly (Sheet 5 of 5)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-11- +	RNC55H2432FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2432FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2552FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2552FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2672FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2672FS	81349	. RESISTOR	1		PADZZ
- 78	JM38510/11001 BCX	81349	. MICROCIRCUIT	2		PADZZ
=	615794-901	37695	. MICROCIRCUIT, Linear	2		PADZZ
- 79	186095-2	37695	. CONNECTOR, Strip	8		PADZZ
- 80	RCR07G223JS	81349	. RESISTOR	2		PADZZ
- 81	6206	25120	. FILTER, Bandpass ..... (Magnavox spec cont dwg 328416-9)	1		PADZZ
- 82	RCR07G104JS	81349	. RESISTOR	1		PADZZ
- 83	JANTX1N752A1	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
- 84	RNC55H1302FR	81349	. RESISTOR	2		PADZZ
*	RNC55H1302FS	81349	. RESISTOR	2		PADZZ
- 85	RNC55H2212FR	81349	. RESISTOR	1		PADZZ
*	RNC55H2212FS	81349	. RESISTOR	1		PADZZ
- 86	RNC55H3922FR	81349	. RESISTOR	1		PADZZ
*	RNC55H3922FS	81349	. RESISTOR	1		PADZZ
- 87	RNC55H3012FR	81349	. RESISTOR	2		PADZZ
*	RNC55H3012FS	81349	. RESISTOR	2		PADZZ
- 88	RCR07G102JS	81349	. RESISTOR	5		PADZZ
- 89	M39014/02-1237	81349	. CAPACITOR	2		PADZZ
- 90	M39014/23-0072	81349	. CAPACITOR	17		PADZZ
*	M39014/23-0372	81349	. CAPACITOR	17		PADZZ
=	258329-1035	37695	. CAPACITOR	17		PADZZ
=	258329-21035	37695	. CAPACITOR	17		PADZZ
- 91	RNC55H5362FR	81349	. RESISTOR	1		PADZZ
*	RNC55H5362FS	81349	. RESISTOR	1		PADZZ
- 92 +	RNC55H1472FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1472FS	81349	. RESISTOR	1		PADZZ
- 93+*	RNC55H7151FS	81349	. RESISTOR	1		PADZZ
+	RNC55H4751FR	81349	. RESISTOR	1		PADZZ
- 94	RCR07G273JS	81349	. RESISTOR	3		PADZZ
- 95	103008-5	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185627-19)	1		PADZZ
- 96 +	RNC55H6492FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H6492FS	81349	. RESISTOR	1		PADZZ
+	RNC55H5232FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H5232FS	81349	. RESISTOR	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-11-	+ RNC55H5492FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H5492FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H5762FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H5762FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H6042FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H6042FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H6192FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H6192FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H6342FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H6342FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H6652FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H6652FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H6812FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H6812FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H6982FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H6982FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H7152FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H7152FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H5902FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H5902FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H5622FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H5622FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H5362FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H5362FS	81349	. RESISTOR	1		PADZZ
- 97	M39014/02-1404	81349	. CAPACITOR	1		PADZZ
	* M39014/02-1416	81349	. CAPACITOR	1		PADZZ
- 98	L156R-5	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-443)	2		PADZZ
- 99	RCR07G331JS	81349	. RESISTOR	1		PADZZ
-100	RCR07G751JS	81349	. RESISTOR	1		PADZZ
-101	CCR09CG152GR	81349	. CAPACITOR	2		PADZZ
	= CN20C152J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2031)	2		PADZZ
	= CN20C152J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22031)	2		PADZZ
-102	MS21381-27	96906	. COIL	1		PADZZ
	= 365189-1	37695	. COIL, Radio frequency	1		PADZZ
-103	M106R-5	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-438)	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-11-104	RCR07G101JS	81349	. RESISTOR	1		PADZZ
-105	617714-902	37695	. MICROCIRCUIT, Linear	1		PADZZ
-106	RCR07G5R6JS	81349	. RESISTOR	2		PADZZ
-107	S226R	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-48)	2		PADZZ
-108	MS75085-9	96906	. COIL	2		PADZZ
-109	538765-1	37695	. CRYSTAL, Unit, quartz	1		PADZZ
-110	345565-1	37695	. INSULATOR	1		PADZZ
-111	365175-804	37695	. COIL, Radio frequency	1		PADZZ
-112	616594-901	37695	. MICROCIRCUIT, Linear	1		PADZZ
-113	CN10C430J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2104)	1		PADZZ
	CN10C430J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22104)	1		PADZZ
	= 100-050-NPO-430J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2104)	1		PADZZ
	= 100-050-NPO-430J	51642	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22104)	1		PADZZ
-114	CCR13CG180GM	81349	. CAPACITOR	1		PADZZ
	= 200-100-NPO-182	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22198)	1		
	= CN10C180J	16546	. CAPACITOR, Fixed,ceramic . (Magnavox spec cont dwg 258330-22008)	1		PADZZ
-115	RCR07G222JS	81349	. RESISTOR	3		PADZZ
-116	CN15A100D	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22195)	1		
	= CN10C100J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22005)	1		PADZZ
-117	CCR09CG152JM	81349	. CAPACITOR	1		PADZZ
	* CCR09CG152GR	81349	. CAPACITOR	1		PADZZ
	= 258330-2026	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
	= 258330-22026	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
-118	RCR07G392JS	81349	. RESISTOR	2		PADZZ
-119	MS21424-13	96906	. COIL	1		PADZZ
-120	M39014/02-1240	81349	. CAPACITOR	2		PADZZ
	* M39014/02-1360	81349	. CAPACITOR	2		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-11-121	RCR07G913JS	81349	. RESISTOR	1		PADZZ
-122	CCR09CG471GR	81349	. CAPACITOR	1		PADZZ
=	CN15C471J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2025)	1		PADZZ
=	CN15C471J	16546	. CAPACITOR, Fixed,ceramic . (Magnavox spec cont dwg 258330-22025)	1		PADZZ
-123	CCR09CG102JM	81349	. CAPACITOR	2		PADZZ
*	CCR09CG102GR	81349	. CAPACITOR	1		PADZZ
=	258330-2029	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
=	258330-22029	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
-124	RCR07G333JS	81349	. RESISTOR	1		PADZZ
-125	RNC55H2001FR	81349	. RESISTOR	2		PADZZ
*	RNC55H2001FS	81349	. RESISTOR	2		PADZZ
-126 +	RNC55H1273FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1273FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1003FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1003FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1023FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1023FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1053FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1053FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1073FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1073FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1103FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1103FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1133FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1133FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1153FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1153FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1183FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1183FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1213FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1213FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1243FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1243FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1303FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1303FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1333FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1333FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1373FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1373FS	81349	. RESISTOR	1		PADZZ
+	RNC55H7872FR	81349	. RESISTOR	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-11-	+ RNC55H8062FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H8062FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H8252FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H8252FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H8452FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H8452FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H8662FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H8662FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H8872FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H8872FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H9092FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H9092FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H9312FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H9312FS	81349	. RESISTOR	1		PADZZ
	+ RNC55H9532FR	81349	. RESISTOR	1		PADZZ
	+* RNC55H9532FS	81349	. RESISTOR	1		PADZZ
-127	M685R-5	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-437)	1		PADZZ
-128	238099-4	37695	. RESISTOR, Thermal	1		PADZZ
-129	M39014/02-1407	81349	. CAPACITOR	1		PADZZ
	* M39014/02-1419	81349	. CAPACITOR	1		PADZZ
-130	RCR07G622JS	81349	. RESISTOR	2		PADZZ
-131	617761-2	37695	. MICROCIRCUIT, Linear	1		PADZZ
	= 617761-1	37695	. MICROCIRCUIT, Linear	1		PADZZ
-132	RCR07G682JS	81349	. RESISTOR	1		PADZZ
-133	RCR07G562JS	81349	. RESISTOR	1		PADZZ
-134	RCR07G124JS	81349	. RESISTOR	2		PADZZ
-135	RCR07G393JS	81349	. RESISTOR	1		PADZZ
-136	RCR07G154JS	81349	. RESISTOR	1		PADZZ
-137	186095-1	37695	. CONNECTOR, Strip, ... modified	1		PADZZ
-138	938651-1	37695	. HOUSING, Shield	1		XB
-139	938650-1	37695	. HOUSING, Shield	1		XB
-140	938655-1	37695	. PARTITION, Shield	1		XB
-141	938649-1	37695	. HOUSING, Shield	1		XB
-142	938656-1	37695	. PARTITION, Shield	1		XB
-143	CDR14BG561BKSM	81349	. CAPACITOR	2		PADZZ
	= 7203A471KF	95275	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 255096-94)	2		PADZZ

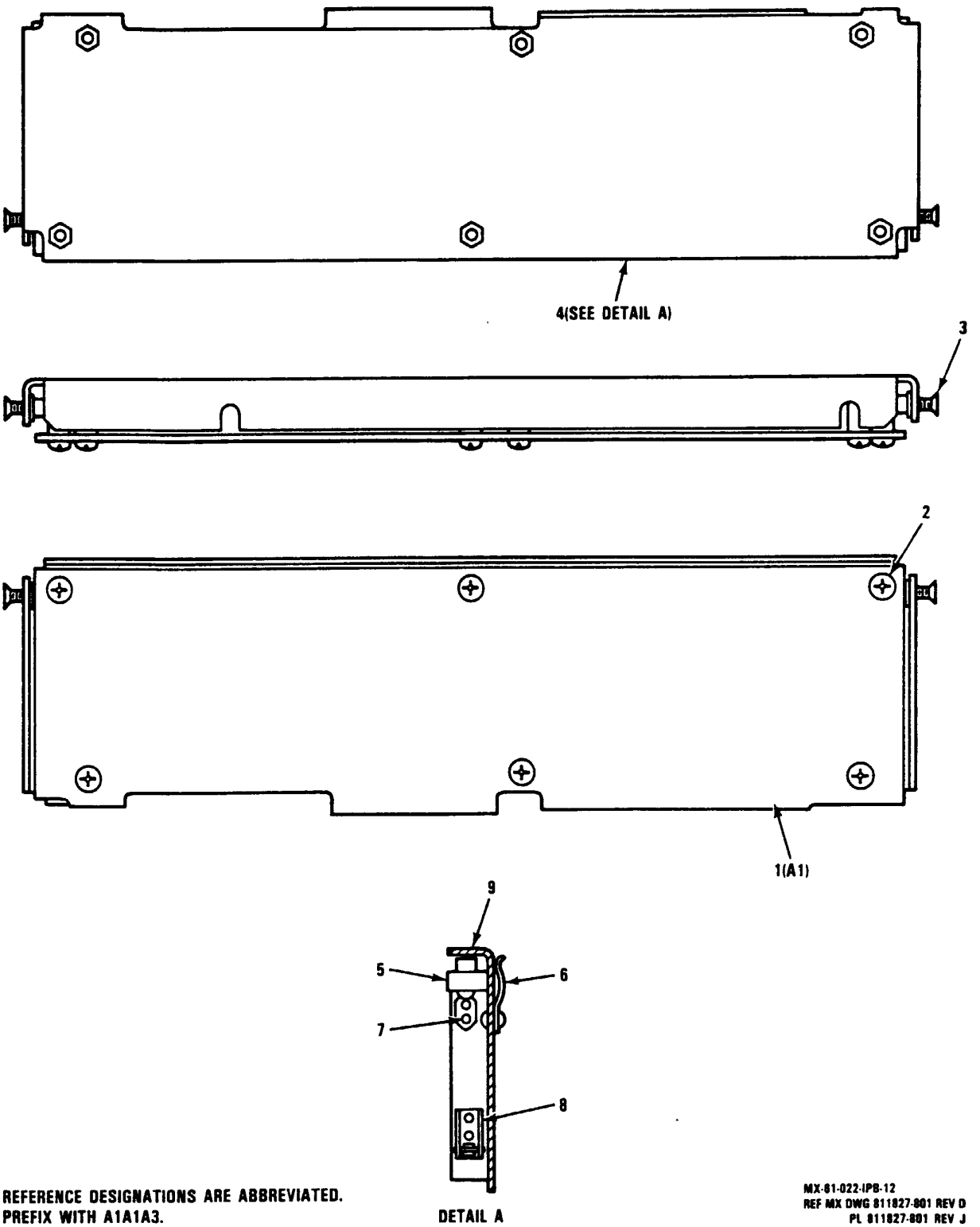
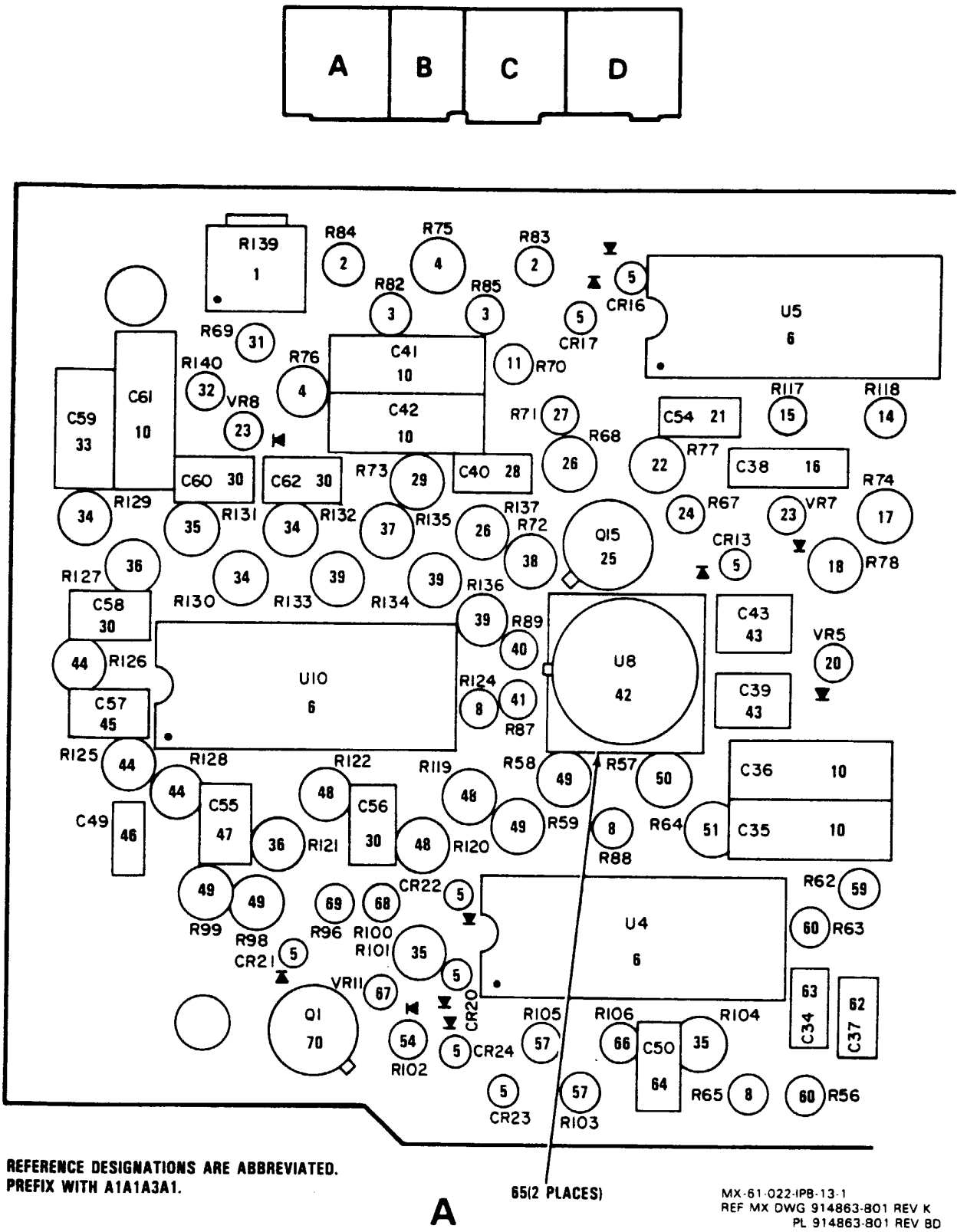


Figure 7-12. Modulator Assembly



REFERENCE DESIGNATIONS ARE ABBREVIATED.
PREFIX WITH A1A1A3A1.

65(2 PLACES)

MX-61-022-IPB-13-1
REF MX DWG 914863-801 REV K
PL 914863-801 REV BD

Figure 7-13. Modulator Circuit Card Assembly (Sheet 1 of 4)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-11-144	CDR01BX181BXSM	81349	. CAPACITOR	1		PADZZ
*	CDR01BX181BKSM	81349	. CAPACITOR	1		PADZZ
=	258475-239	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
-145	940125-1	37695	. SHIELD	2		XB
-146	348984-1	37695	. INSULATOR	1		XB
-147	940821-1	37695	. SHIELD	1		XB
-148	940124-1	37695	. SHIELD	1		XB
-149	513917-2	37695	. COVER, Adjustment hole ...	17		XB
-150	410899-1	37695	. PRINTED WIRING BOARD	1		XB
7-12-	811827-801	37695	MODULATOR ASSEMBLY ..... (See fig. 2 for nha)	REF		PAFLD
- 1	914863-801	37695	. CIRCUIT CARD ASSEMBLY, ... Modulator (See fig. 13 for bkdn)	1		PADLD
- 2	MS51957-14	96906	. SCREW (AP)	6		PAFZZ
- 3	MS24693C25	96906	. SCREW (AP)	2		PAFZZ
- 4	936673-801	37695	. BRACKET, Modulator	1		XB
- 5	514527-101	37695	. . INSERT, Screw thread ...	6		PAFZZ
- 6	165468-1	37695	. . CONTACT STRIP	1		XB
	MS16535-21	96906	. . RIVET (AP)	8		XB
=	MS16534-11	96906	. . RIVET (AP)	8		XB
- 7	NAS696C06M	80205	. . NUT	2		XB
	MS20426AD2-3	96906	. . RIVET (AP)	2		XB
- 8	RMLHA27M2860-62	72962	. . NUT, Self-locking ..... (Magnavox spec cont dwg 107295-2)	2		XB
	MS20426AD2-3	96906	. . RIVET (AP)	2		XB
- 9	936673-1	37695	. . BRACKET, Modulator	1		XB
7-13-	914863-801	37695	CIRCUIT CARD ASSEMBLY, ... Modulator (see fig. 12 for nha)	REF		PADLD
- 1	8050EKX102GM	30983	. RESISTOR, Variable ..... (Magnavox spec cont dwg 228113-3)	2		PADZZ
*	8050JKU102G1	30983	. RESISTOR, Variable	2		PADZZ
- 2	RCR07G302JS	81349	. RESISTOR	4		PADZZ
- 3	RCR07G333JS	81349	. RESISTOR	6		PADZZ
- 4	RNC55H1472FR	81349	. RESISTOR	2		PADZZ
*	RNC55H1472FS	81349	. RESISTOR	2		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-13- 5	JANTX1N4454-1	81350	. SEMICONDUCTOR DEVICE	26		PADZZ
- 6	JM38510/11001 BCX	81349	. MICROCIRCUIT	4		PADZZ
=	615794-901	37695	. MICROCIRCUIT, Linear	4		PADZZ
- 7	RNC55H2742FR	81349	. RESISTOR	1		PADZZ
*	RNC55H2742FS	81349	. RESISTOR	1		PADZZ
- 8	RCR07G240JS	81349	. RESISTOR	19		PADZZ
- 9	RNC66H1212FR	81349	. RESISTOR	2		PADZZ
*	RNC55H1212FS	81349	. RESISTOR	2		PADZZ
- 10	CCR06CG123JM	81349	. CAPACITOR	6		PADZZ
*	CCR06CG123J	81349	. CAPACITOR	6		PADZZ
=	258330-2042	37695	. CAPACITOR, Fixed ceramic .	6		PADZZ
	CCR09CG123JM	81349	. CAPACITOR	6		PADZZ
*	CCR09CG123GR	81349	. CAPACITOR	6		PADZZ
	258330-22228	37695	. CAPACITOR, Fixed ceramic .	6		PADZZ
- 11	RCR07G153JS	81349	. RESISTOR	3		PADZZ
- 12	CCR09CG681JM	81349	. CAPACITOR	3		PADZZ
*	CCR09CG681GR	81349	. CAPACITOR	3		PADZZ
=	CN20C681J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2027)	3		PADZZ
=	CN20C681J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22027)	3		PADZZ
- 13	RNC55H3012FR	81349	. RESISTOR	2		PADZZ
*	RNC55H3012FS	81349	. RESISTOR	2		PADZZ
- 14	RCR07G512JS	81349	. RESISTOR	3		PADZZ
- 15	RCR07G102JS	81349	. RESISTOR	2		PADZZ
- 16	M39014/02-1405	81349	. CAPACITOR	2		PADZZ
*	M39014/02-1417	81349	. CAPACITOR	2		PADZZ
- 17	RNC55H1022FR	81349	. RESISTOR	2		PADZZ
*	RNC55H1022FS	81349	. RESISTOR	2		PADZZ
- 18	RNC55H5111FR	81349	. RESISTOR	2		PADZZ
*	RNC55H5111FS	81349	. RESISTOR	2		PADZZ
- 19	M39014/02-1238	81349	. CAPACITOR	2		PADZZ
*	M39014/02-1358	81349	. CAPACITOR	2		PADZZ
- 20	JANTX1N756A1	81350	. SEMICONDUCTOR DEVICE	2		PADZZ
- 21	M39014/01-1461	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1581	81349	. CAPACITOR	1		PADZZ
- 22 +	RNC55H2261FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2261FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2211FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2211FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1961FR	81349	. RESISTOR	1		PADZZ

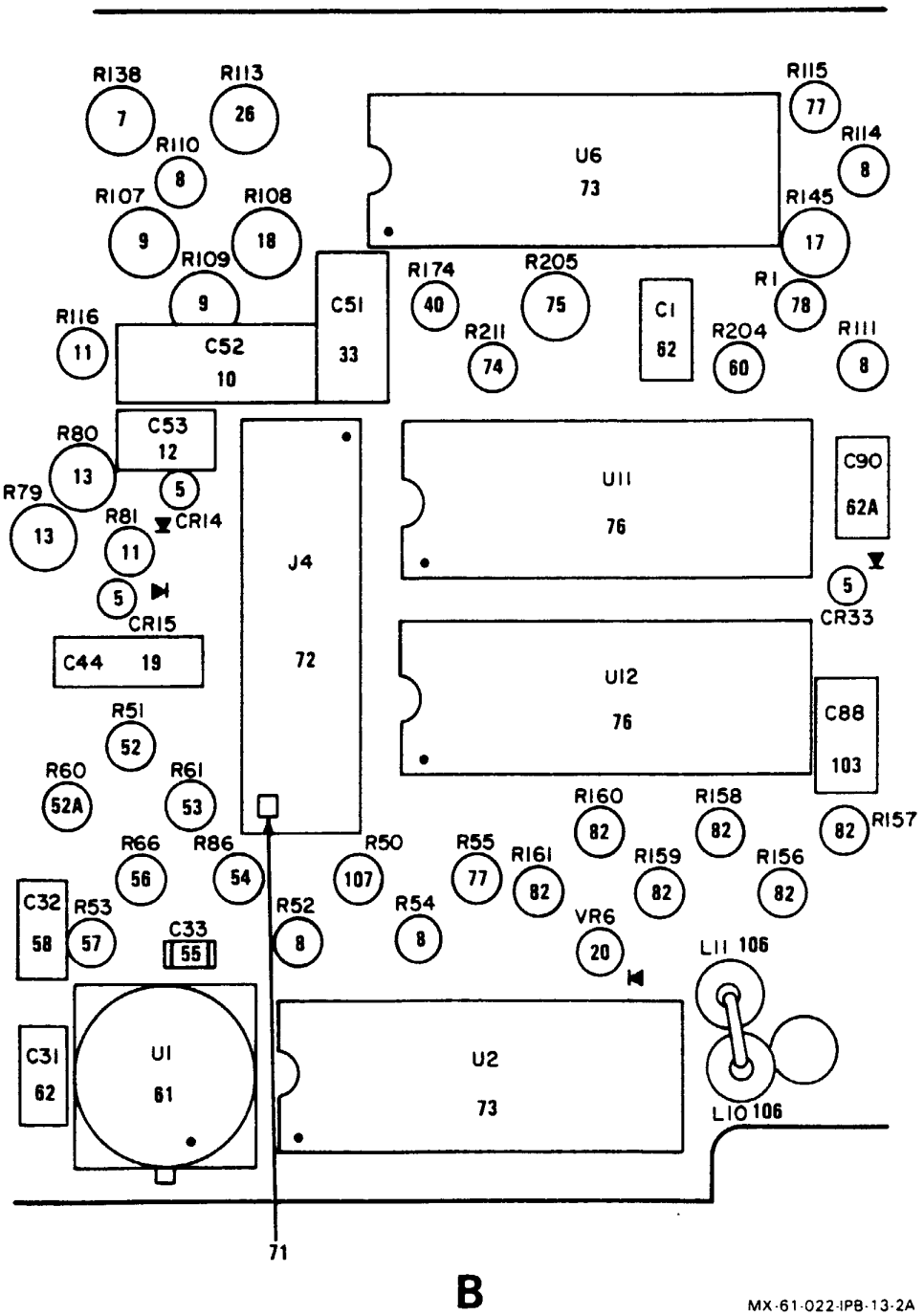


Figure 7-13. Modulator Circuit Card Assembly (Sheet 2 of 4)

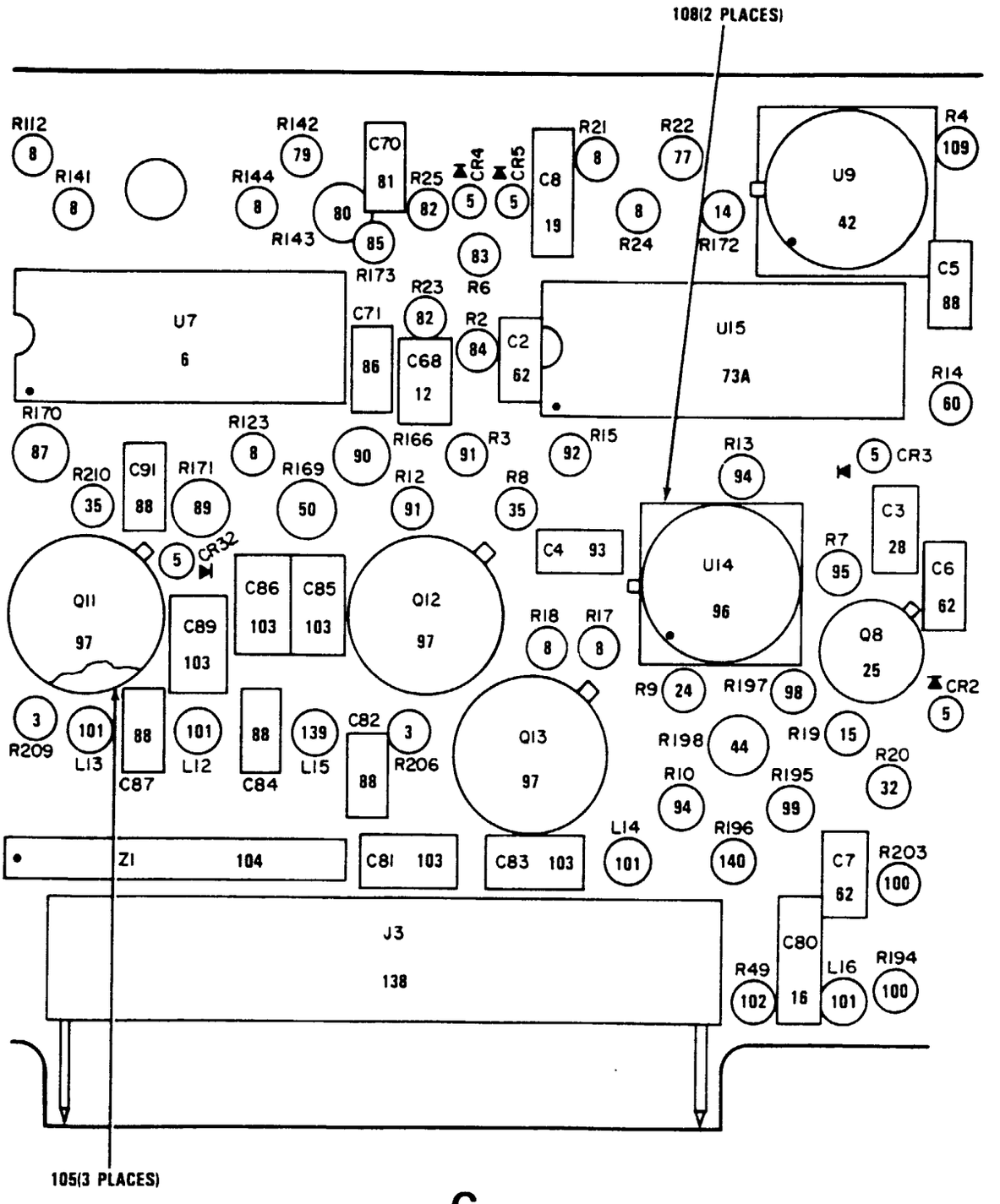


Figure 7-13. Modulator Circuit Card Assembly (Sheet 3 of 4)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-13- +*	RNC55H1961FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2051FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2051FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2151FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2151FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2371FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2371FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2491FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2491FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2611FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2611FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1871FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1871FS	81349	. RESISTOR	1		PADZZ
- 23	JANTX1N751A1	81350	. SEMICONDUCTOR DEVICE	2		PADZZ
- 24	RCR07G432JS	81349	. RESISTOR	2		PADZZ
- 25	JANTX2N2222A	81350	. SEMICONDUCTOR DEVICE	6		PADZZ
- 26	RNC55H1502FR	81349	. RESISTOR	3		PADZZ
*	RNC55H1502FS	81349	. RESISTOR	3		PADZZ
- 27	RCR07G393JS	81349	. RESISTOR	1		PADZZ
- 28	M39014/01-1237	81349	. CAPACITOR	2		PADZZ
*	M39014/01-1357	81349	. CAPACITOR	2		PADZZ
- 29	RNC55H2002FR	81349	. RESISTOR	1		PADZZ
*	RNC55H2002FS	81349	. RESISTOR	1		PADZZ
- 30	CCR09CG102JM	81349	. CAPACITOR	4		PADZZ
*	CCR09CG102GR	81349	. CAPACITOR	4		PADZZ
=	258330-2029	37695	. CAPACITOR, Fixed ceramic .	4		PADZZ
=	258330-22029	37695	. CAPACITOR, Fixed ceramic .	4		PADZZ
- 31	RCR07G242JS	81349	. RESISTOR	4		PADZZ
- 32	RCR07G331JS	81349	. RESISTOR	2		PADZZ
- 33	CCR09CG392JM	81349	. CAPACITOR	2		PADZZ
=	CN30C392J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2036)	2		PADZZ
=	CN30C392J	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22036)	2		PADZZ
=	CN30C392G	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-2036)	2		PADZZ
=	CN30C392G	16546	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258330-22036)	2		PADZZ
- 34	RNC55H5621FR	81349	. RESISTOR	3		PADZZ
*	RNC55H5621FS	81349	. RESISTOR	3		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-13- 35	RNC55H1001FR	81349	. RESISTOR	6		PADZZ
*	RNC55H1001FS	81349	. RESISTOR	6		PADZZ
=	RNC55H1101FR	81349	. RESISTOR	6		PADZZ
*	RNC55H1101FS	81349	. RESISTOR	6		PADZZ
- 36	RNC55H3921FR	81349	. RESISTOR	2		PADZZ
*	RNC55H3921FS	81349	. RESISTOR	2		PADZZ
- 37 +	RNC55H2261FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2261FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1001FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1001FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1101FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1101FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1211FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1211FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1301FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1301FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1401FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1401FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1501FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1501FS	81349	. RESISTOR	1		PADZZ
+	RNC55H1621FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H1621FS	81349	. RESISTOR	1		PADZZ
+	RNC55H2001FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H2001FS	81349	. RESISTOR	1		PADZZ
+	RNC55H6040FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H6040FS	81349	. RESISTOR	1		PADZZ
+	RNC55H7150FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H7150FS	81349	. RESISTOR	1		PADZZ
+	RNC55H8060FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H8060FS	81349	. RESISTOR	1		PADZZ
+	RNC55H9090FR	81349	. RESISTOR	1		PADZZ
+*	RNC55H9090FS	81349	. RESISTOR	1		PADZZ
- 38	RNC55H4221FR	81349	. RESISTOR	1		PADZZ
*	RNC55H4221FS	81349	. RESISTOR	1		PADZZ
- 39	RNC55H2741FR	81349	. RESISTOR	3		PADZZ
*	RNC55H2741FS	81349	. RESISTOR	3		PADZZ
- 40	RCR07G100JS	81349	. RESISTOR	2		PADZZ
- 41 +	RNC55H8661FR	81349	. RESISTOR	1		PADZZ
+	RNC55H1212FR	81349	. RESISTOR	1		PADZZ
+	RNC55H8251FR	81349	. RESISTOR	1		PADZZ
+	RNC55H9091FR	81349	. RESISTOR	1		PADZZ
+	RNC55H9531FR	81349	. RESISTOR	1		PADZZ
+	RNC55H1052FR	81349	. RESISTOR	1		PADZZ
+	RNC55H1102FR	81349	. RESISTOR	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-13-	+ RNC55H1152FR	81349	. RESISTOR	1		PADZZ
	+ RNC55H1272FR	81349	. RESISTOR	1		PADZZ
	+ RNC55H1332FR	81349	. RESISTOR	1		PADZZ
	+ RNC55H1002FR	81349	. RESISTOR	1		PADZZ
	+ RCR07G133JS	81349	. RESISTOR	1		PADZZ
- 42	JM38510/10102 BIX	81349	. MICROCIRCUIT	2		PADZZ
	* M38510/10102 BIC	81349	. MICROCIRCUIT	2		PADZZ
	= 615456-2	37695	. MICROCIRCUIT, Linear	2		PADZZ
- 43	MN335R	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275064-77)	2		PADZZ
- 44	RNC55H7501FR	81349	. RESISTOR	4		PADZZ
	* RNC55H7501FS	81349	. RESISTOR	4		PADZZ
- 45	CCR09CG272JM	81349	. CAPACITOR	1		PADZZ
	* CCR09CG272GR	81349	. CAPACITOR	1		PADZZ
	= 258330-2034	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
	= 258330-22034	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
- 46	M225R-20	17554	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 275056-234)	1		PADZZ
- 47	CCR09CG222JM	81349	. CAPACITOR	1		PADZZ
	* CCR09CG222GR	81349	. CAPACITOR	1		PADZZ
	= 258330-2033	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
	= 258330-22033	37695	. CAPACITOR, Fixed ceramic .	1		PADZZ
- 48	RNC55H8251FR	81349	. RESISTOR	4		PADZZ
	* RNC55H8251FS	81349	. RESISTOR	4		PADZZ
- 49	RNC55H3011FR	81349	. RESISTOR	4		PADZZ
	* RNC55H3011FS	81349	. RESISTOR	4		PADZZ
- 50	RNC55H3922FR	81349	. RESISTOR	2		PADZZ
	* RNC55H3922FS	81349	. RESISTOR	2		PADZZ
- 51	RNC55H7502FR	81349	. RESISTOR	1		PADZZ
	* RNC55H7502FS	81349	. RESISTOR	1		PADZZ
- 52	RCR07G162JS	81349	. RESISTOR	1		PADZZ
- 52A	RCR07G122JS	81349	. RESISTOR	1		PADZZ
- 53	RCR07G622JS	81349	. RESISTOR	1		PADZZ
- 54	RCR07G151JS	81349	. RESISTOR	4		PADZZ
- 55	CDR14BG561BKSM	81349	. CAPACITOR	1		PADZZ
	= 7203A471KF	95275	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 255096-94)	1		PADZZ
- 56	RCR07G821JS	81349	. RESISTOR	1		PADZZ
- 57	RCR07G244JS	81349	. RESISTOR	3		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-13- 58	M39014/01-1218	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1338	81349	. CAPACITOR	1		PADZZ
- 59 +	RCR07G103JS	81349	. RESISTOR	1		PADZZ
+	RCR07G123JS	81349	. RESISTOR	1		PADZZ
+	RCR07G153JS	81349	. RESISTOR	1		PADZZ
+	RCR07G183JS	81349	. RESISTOR	1		PADZZ
+	RCR07G223JS	81349	. RESISTOR	1		PADZZ
+	RCR07G822JS	81349	. RESISTOR	1		PADZZ
+	RCR07G273JS	81349	. RESISTOR	1		PADZZ
- 60	RCR07G104JS	81349	. RESISTOR	5		PADZZ
- 61	615234-901	37695	. INTEGRATED CIRCUIT	1		PADZZ
- 62	M39014/01-1455	81349	. CAPACITOR	10		PADZZ
*	M39014/01-1555	81349	. CAPACITOR	10		PADZZ
- 63	M39014/01-1451	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1574	81349	. CAPACITOR	1		PADZZ
- 63A	M39014/01-1224	81349	. CAPACITOR	1		
- 64	L156R	17554	. CAPACITOR, Fixed, ... (Magnavox spec cont dwg 275056-43)	1		PADZZ
- 65	10318-DAP	07046	. MOUNTING PAD, Electronic . (Magnavox spec cont dwg 447419-4)	2		PADZZ
- 66	RCR07G124JS	81349	. RESISTOR	1		PADZZ
- 67	JANTX1N752A1	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
- 68 +	RNC55H1871FR	81349	. RESISTOR	1		PADZZ
+	RNC55H1961FR	81349	. RESISTOR	1		PADZZ
+	RNC55H2001FR	81349	. RESISTOR	1		PADZZ
+	RNC55H1471FR	81349	. RESISTOR	1		PADZZ
+	RNC55H1541FR	81349	. RESISTOR	1		PADZZ
+	RNC55H1692FR	81349	. RESISTOR	1		PADZZ
+	RNC55H1781FR	81349	. RESISTOR	1		PADZZ
- 69	RCR07G132JS	81349	. RESISTOR	1		PADZZ
- 70	JANTX2N2907A	81349	. TRANSISTOR	5		PADZZ
- 71	M55302/127-00KY	00779	. RECEPTACLE, Guide pin .... (Magnavox spec cont dwg 447514-1)	1		PADZZ
- 72	87518-3	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185626-1)	1		PADZZ
- 73	JM38510/12304 BEX	81349	. MICROCIRCUIT	2		PADZZ
*	M38510/12304 BEB	81349	. MICROCIRCUIT	2		PADZZ
=	617761-1	37695	. MICROCIRCUIT, Linear	2		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-13- 73A=	647025-1	37695	. MICROCIRCUIT, Linear	1		
- 74 +	RCR07G133JS	81349	. RESISTOR	1		PADZZ
+	RCR07G163JS	81349	. RESISTOR	1		PADZZ
+	RCR07G183JS	81349	. RESISTOR	1		PADZZ
+	RCR07G203JS	81349	. RESISTOR	1		PADZZ
+*	RCR07G203JS	81349	. RESISTOR	1		PADZZ
+	RCR07G223JS	81349	. RESISTOR	1		PADZZ
+	RCR07G243JS	81349	. RESISTOR	1		PADZZ
+	RCR07G273JS	81349	. RESISTOR	1		PADZZ
- 75	RNC55H2053FR	81349	. RESISTOR	1		PADZZ
*	RNC55H2053FS	81349	. RESISTOR	1		PADZZ
- 76	JM38510/17601 BEX	81349	. MICROCIRCUIT, Digital	2		PADZZ
*	M38510/17601 BEB	81349	. MICROCIRCUIT, Digital	2		PADZZ
=	619998-1	37695	. MICROCIRCUIT, Digital	2		PADZZ
- 77	RCR07G224JS	81349	. RESISTOR	3		PADZZ
- 78 +	RCR07G224JS	81349	. RESISTOR	1		PADZZ
+	RCR07G244JS	81349	. RESISTOR	1		PADZZ
+	RCR07G274JS	81349	. RESISTOR	1		PADZZ
+	RCR07G304JS	81349	. RESISTOR	1		PADZZ
+	RCR07G184JS	81349	. RESISTOR	1		PADZZ
- 79 +	RCR07G273JS	81349	. RESISTOR	1		PADZZ
+	RCR07G303JS	81349	. RESISTOR	1		PADZZ
+	RCR07G333JS	81349	. RESISTOR	1		PADZZ
+	RCR07G363JS	81349	. RESISTOR	1		PADZZ
+	RCR07G393JS	81349	. RESISTOR	1		PADZZ
+	RCR07G473JS	81349	. RESISTOR	1		PADZZ
+	RCR07G433JS	81349	. RESISTOR	1		PADZZ
- 80	RNC55H5112FR	81349	. RESISTOR	1		PADZZ
- 81	M39014/01-1448	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1568	81349	. CAPACITOR	1		PADZZ
- 82	RCR07G103JS	81349	. RESISTOR	12		PADZZ
- 83	RCR07G134JS	81349	. RESISTOR	1		PADZZ
*	RCR07G134JS	81349	. RESISTOR	1		PADZZ
- 84	RCR07G474JS	81349	. RESISTOR	1		PADZZ
- 85	RCR07G513JS	81349	. RESISTOR	1		PADZZ
- 86	M39014/01-1230	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1350	81349	. CAPACITOR	1		PADZZ
- 87 +	RNC55H2872FR	81349	. RESISTOR	2		PADZZ
+*	RNC55H2872FS	81349	. RESISTOR	2		PADZZ
+	RNC55H2802FR	81349	. RESISTOR	2		PADZZ
+*	RNC55H2802FS	81349	. RESISTOR	2		PADZZ
+	RNC55H2942FR	81349	. RESISTOR	2		PADZZ
+*	RNC55H2942FS	81349	. RESISTOR	2		PADZZ

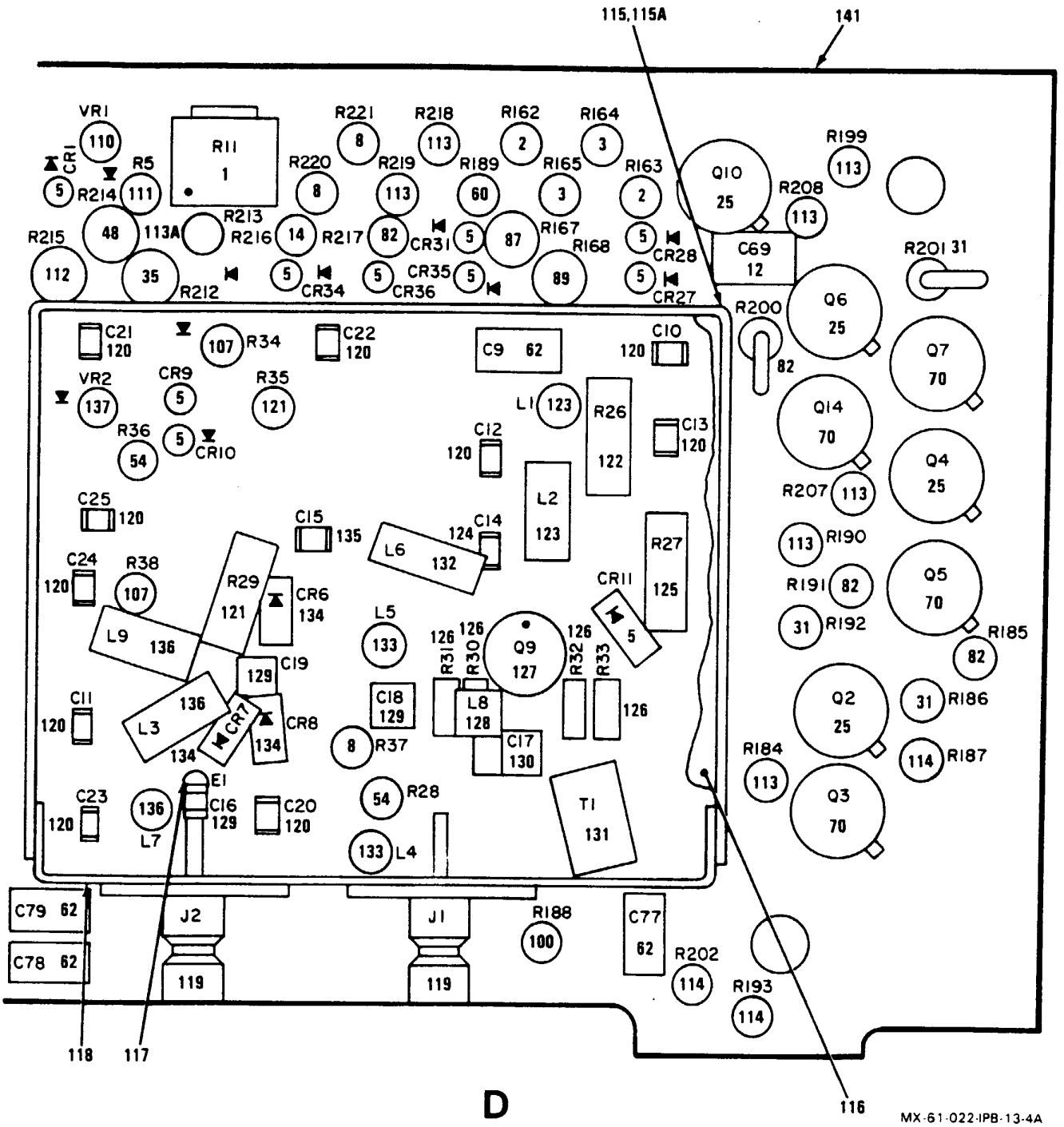
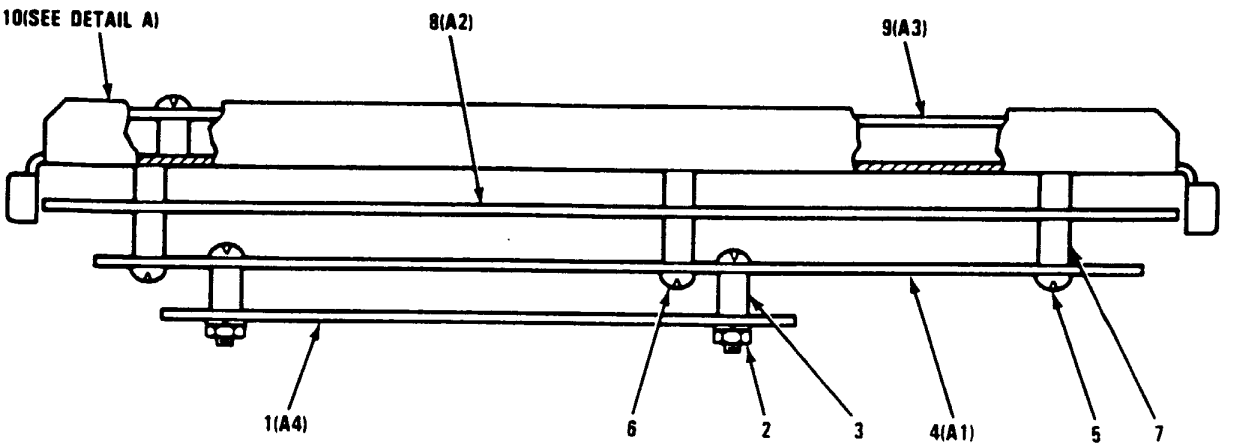


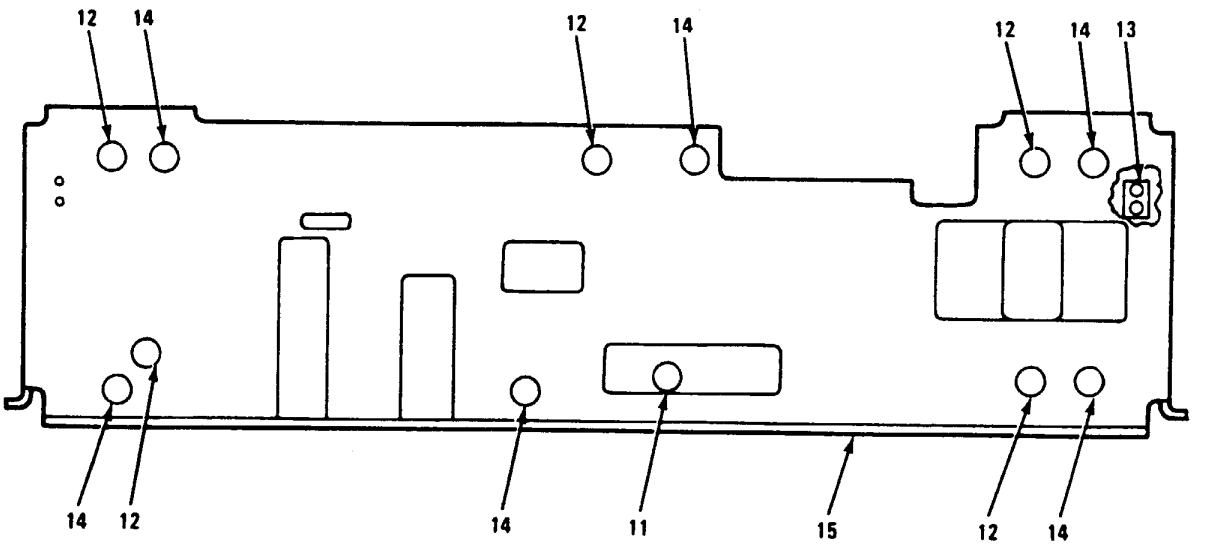
Figure 7-13. Modulator Circuit Card Assembly (Sheet 4 of 4)

FIGURE AND INDEX NUMBER		PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-13- 88		M39014/01-1473	81349	. CAPACITOR	5		PADZZ
	*	M39014/01-1593	81349	. CAPACITOR	5		PADZZ
- 89		RNC55H9092FR	81349	. RESISTOR	2		PADZZ
	*	RNC55H9092FS	81349	. RESISTOR	2		PADZZ
- 90		RNC55H1542FR	81349	. RESISTOR	1		PADZZ
	*	RNC55H1542FS	81349	. RESISTOR	1		PADZZ
- 91		RCR07G752JS	81349	. RESISTOR	2		PADZZ
- 92		RCR07G105JS	81349	. RESISTOR	1		PADZZ
- 93		M39014/01-1216	81349	. CAPACITOR	1		PADZZ
	*	M39014/01-1336	81349	. CAPACITOR	1		PADZZ
- 94		RCR07G202JS	81349	. RESISTOR	2		PADZZ
- 95		RCR07G111JS	81349	. RESISTOR	1		PADZZ
- 96		JM38510/10103 BGX	81349	. MICROCIRCUIT	1		PADZZ
		M38510/10103 BGC	81349	. MICROCIRCUIT	1		PADZZ
	=	615456-3	37695	. MICROCIRCUIT, Linear	1		PADZZ
- 97		617713-902	37695	. TRANSISTOR	3		PADZZ
- 98	+	RCR07G392JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G272JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G332JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G362JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G482JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G472JS	81349	. RESISTOR	1		PADZZ
- 99	+	RCR07G203JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G243JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G273JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G363JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G393JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G473JS	81349	. RESISTOR	1		PADZZ
	+	RCR07G513JS	81349	. RESISTOR	1		PADZZ
-100		RCR07G5R1JS	81349	. RESISTOR	3		PADZZ
-101		MS75083-9	96906	. COIL	4		PADZZ
-102		RCR07G272JS	81349	. RESISTOR	1		PADZZ
-103		S106R	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-75)	6		PADZZ
-104		M8340105M4703 JC	81349	. RESISTOR	1		PADZZ
-105		7717-15N	13103	. MOUNTING PAD, Electronic . (Magnavox spec cont dwg 447173-1)	3		PADZZ
	=	7717-15DAP	13103	. MOUNTING PAD, Electronic .	3		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-13-106	56-590-65/4A	02114	. CORE, Adjust tuning ..... (Magnavox spec cont dwg 657867-4)	2		PADZZ
-107	RCR07G101JS	81349	. RESISTOR	3		PADZZ
-108	10272-DAP	07047	. INSULATOR (Magnavox spec . cont dwg 345158-1)	2		PADZZ
-109	RCR07G621JS	81349	. RESISTOR	1		PADZZ
-110	JANTX1N753A1	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
*	JANTX1N753A	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
-111	RCR07G392JS	81349	. RESISTOR	1		PADZZ
-112	RNC55H9091FR	81349	. RESISTOR	1		PADZZ
*	RNC55H9091FS	81349	. RESISTOR	1		PADZZ
-113	RCR07G473JS	81349	. RESISTOR	7		PADZZ
-113A	RCR07G163JS	81349	. RESISTOR	1		PADZZ
-114	RCR07G273JS	81349	. RESISTOR	3		PADZZ
-115	938589-1	37695	. HOUSING, Shield	1		XB
-115A	349264-1	37695	. INSULATOR, Shield	1		XB
-116	938592-1	37695	. COVER, Shield	1		XB
-117	SE089B02	81349	. TERMINAL	1		PADZZ
=	209467-901	37695	. TERMINAL	1		PADZZ
-118	938590-1	37695	. HOUSING, Shield	1		XB
-119	M39012/95-0001	81349	. CONNECTOR	2		PADZZ
=	16-0209-000	19505	. CONNECTOR, Coaxial ..... (Magnavox spec cont dwg 189175-7)	2		PADZZ
-120	7561A471MFA	95275	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258475-49)	10		PADZZ
-121	RCR07G510JS	81349	. RESISTOR	2		PADZZ
-122	RCR07G182JS	81349	. RESISTOR	1		PADZZ
-123	MS75083-5	96906	. COIL	2		PADZZ
-124 +	MN401R5D	73899	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258475-468)	1		PADZZ
+	MN403R0D	73899	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258475-464)	1		PADZZ
+	MN402R2D	73899	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258475-466)	1		PADZZ
+	MN401R0D	73899	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258475-470)	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-13-125	+ RCR07G150JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G180JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G220JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G240JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G270JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G300JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G330JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G360JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G390JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G430JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G470JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G510JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G513JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G560JS	81349	. RESISTOR	1		PADZZ
	+ RCR07G620JS	81349	. RESISTOR	1		PADZZ
-126	+ RCR05G6R8JS	81349	. RESISTOR	4		PADZZ
-127	645797-901	37695	. TRANSISTOR, NPN	1		PADZZ
-128	365173-2	37695	. COIL, Radio frequency	1		PADZZ
-129	CDR14BG471CMSM	81349	. CAPACITOR	3		PADZZ
	* CDR14BG471CFSM	81349	. CAPACITOR	3		PADZZ
	= 258300-11077	37695	. CAPACITOR	3		PADZZ
-130	CDR14BG680EJSM	81349	. CAPACITOR	1		PADZZ
	ATC-100-B-680-J-P-500-SP	29990	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258300-11257)	1		PADZZ
-131	368883-811	37695	. TRANSFORMER, Balum	1		PADZZ
-132	365174-801	37695	. COIL, Radio frequency	1		PADZZ
-133	MS75083-3	96906	. COIL	2		PADZZ
-134	619915-902	37695	. SEMICONDUCTOR DEVICE, ... Diode	3		PADZZ
-135	CDR14BG130EDSM	81349	. CAPACITOR	1		PADZZ
	= MNH01301	73899	. CAPACITOR, Fixed ceramic . (Magnavox spec cont dwg 258475-212)	1		PADZZ
-136	MS75083-7	96906	. COIL	3		PADZZ
-137	JANTX1N746A1	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
-138	103008-9	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185627-18)	1		PADZZ
-139	MS75085-10	96906	. COIL	1		PADZZ
-140	RNC55H1871FR	81349	. RESISTOR	1		PADZZ
	* RNC55H1871FS	81349	. RESISTOR	1		PADZZ
-141	412277-1	37695	. PRINTED WIRING BOARD	1		XB



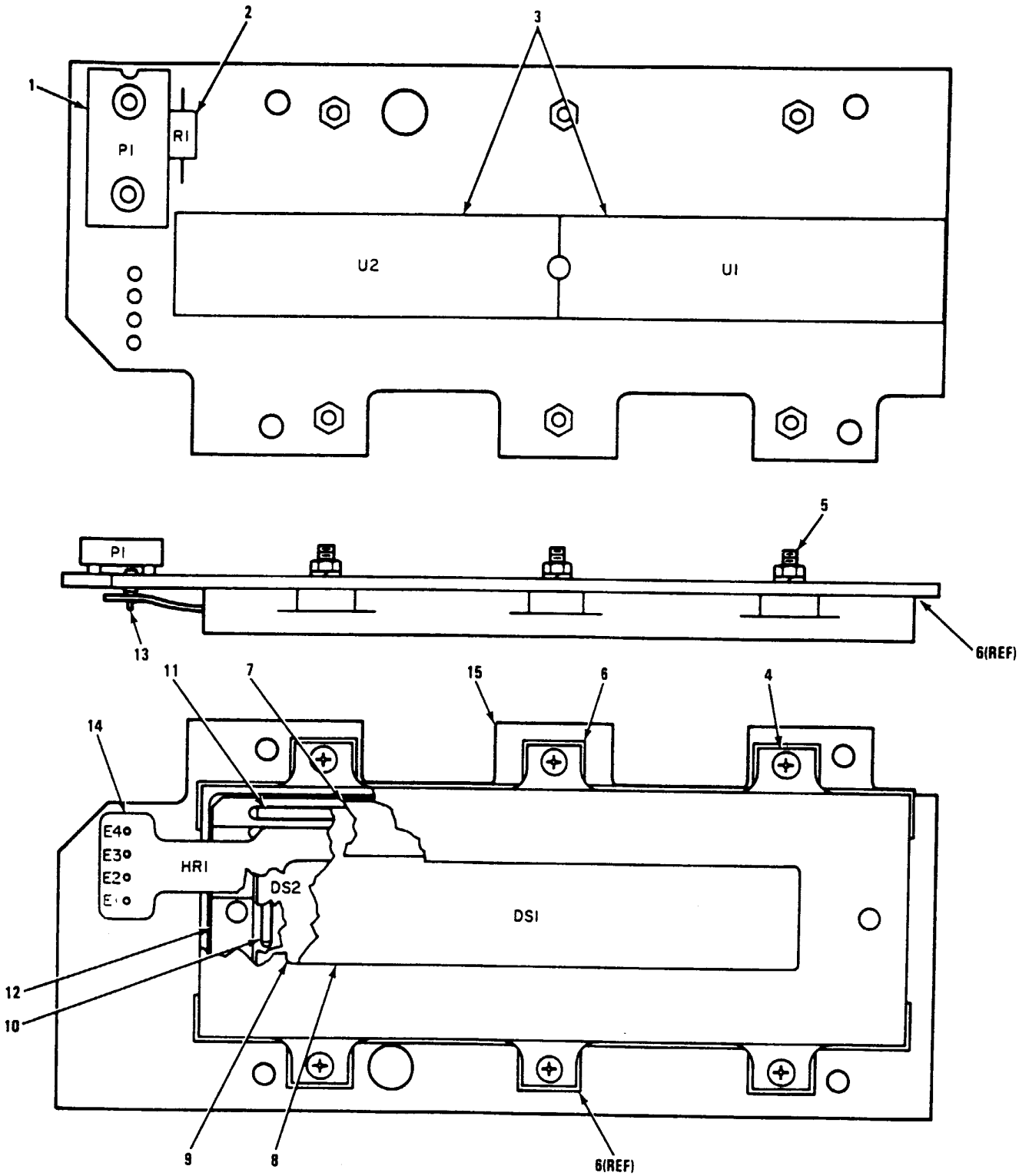


DETAIL A

REFERENCE DESIGNATIONS ARE ABBREVIATED.
PREFIX WITH A1A1A1.

MX 61-022-IPB-14
REF MX DWG 914861-801 REV J
PL 914861-801 REV R

Figure 7-14. Control/Data Converter Assembly



REFERENCE DESIGNATIONS ARE ABBREVIATED.
PREFIX WITH A1A1A1A4.

MX-81-022-IPB-15
REF MX DWG 811947-801 REV B
PL 811947-801 REV N

Figure 7-15. Data Converter Circuit Card Assembly

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-15-	811947-801	37695	CIRCUIT CARD ASSEMBLY, ... LCD data converter (see fig. 14 for nha)	REF		PADLD
- 1	516-AG100	91506	. SOCKET, Plug-in ..... (Magnavox spec cont dwg 189697-2)	1		PADZZ
*	11508735-6	18876	. SOCKET, Plug-in	1		PADZZ
- 2 +	RCR07G101JS	81349	. RESISTOR	1		PADZZ
+	RCR07G111JS	81349	. RESISTOR	1		PADZZ
+	RCR07G121JS	81349	. RESISTOR	1		PADZZ
+	RCR07G131JS	81349	. RESISTOR	1		PADZZ
+	RCR07G151JS	81349	. RESISTOR	1		PADZZ
+	RCR07G560JS	81349	. RESISTOR	1		PADZZ
+	RCR07G620JS	81349	. RESISTOR	1		PADZZ
+	RCR07G680JS	81349	. RESISTOR	1		PADZZ
+	RCR07G820JS	81349	. RESISTOR	1		PADZZ
+	RCR07G910JS	81349	. RESISTOR	1		PADZZ
- 3	645448-901	37695	. MICROCIRCUIT, Digital	2		PADZZ
- 4	513768-1	37695	. BEZEL, LCD	1		PADZZ
- 5	MS51957-3	96906	. SCREW (AP)	6		PAFZZ
	MS35338-134	96906	. WASHER (AP)	6		PAFZZ
	NAS671C2	80205	. NUT (AP)	6		PAFZZ
- 6	348503-1	37695	. INSULATOR, Bezel	2		MD
- 7	345956-1	37695	. GASKET	1		MD
- 8	626482-1	37695	. DISPLAY, Liquid crystal ..	1		PADZZ
- 9	625488-1	37695	. PANEL, ... Electroluminescent	1		XB
- 10	186163-2	37695	. CONNECTOR, Layered, ... elastomeric	1		PADZZ
- 11	186163-1	37695	. CONNECTOR, Layered, ... elastomeric	2		PADZZ
- 12	345955-1	37695	. CARRIER STRIP	1		XB
- 13	229-1064-00-0-590	05009	. TERMINAL, Standoff ..... (Magnavox spec cont dwg 205350-1)	4		PADZZ
- 14	HSK9925	09359	. HEATER, Thin film ..... (Magnavox spec cont dwg 566099-1)	1		PADZZ
- 15	411952-1	37695	. PRINTED WIRING BOARD	1		XB

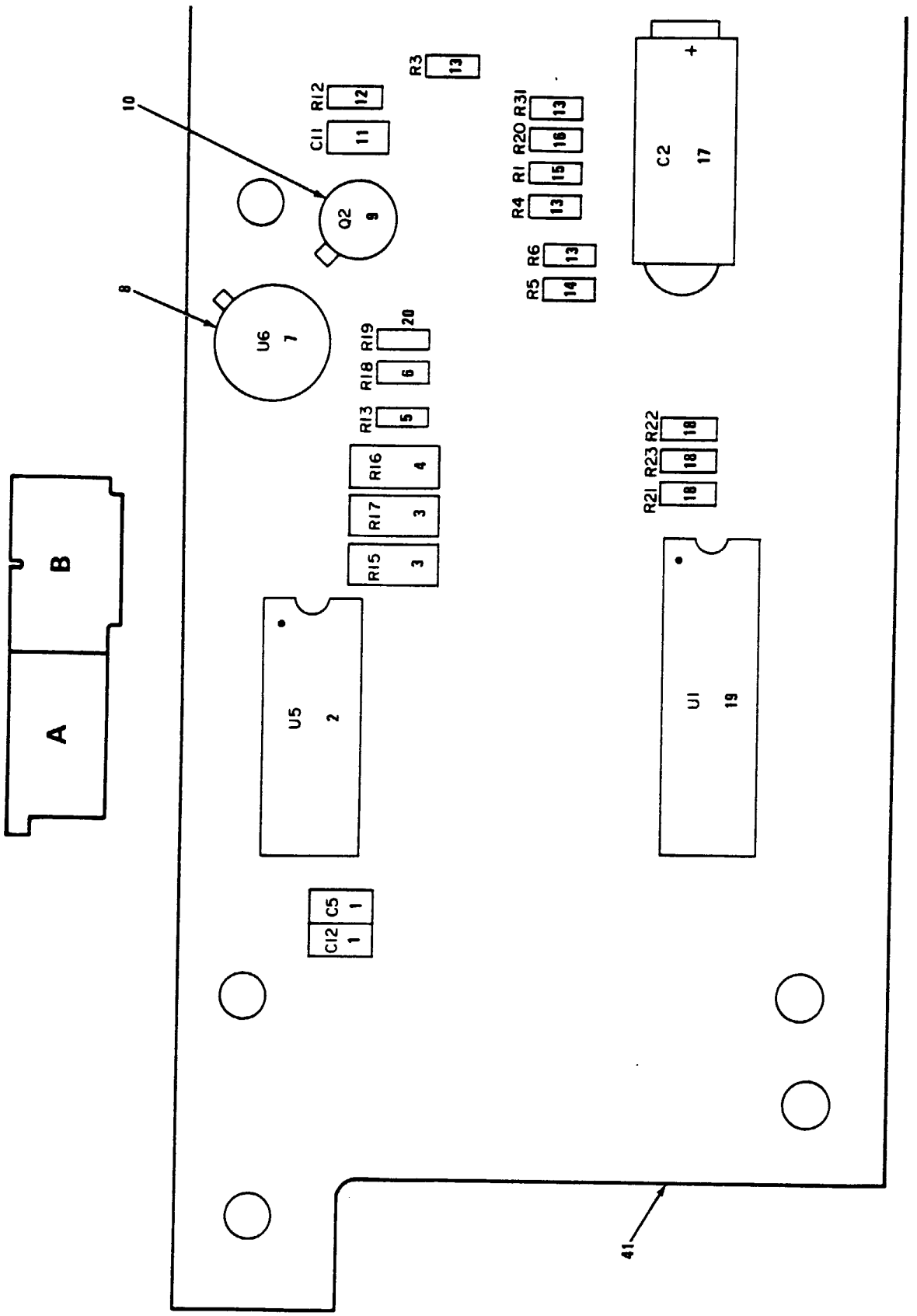


Figure 7-16. Interface Data Converter Circuit Card Assembly (Sheet 1 of 3)

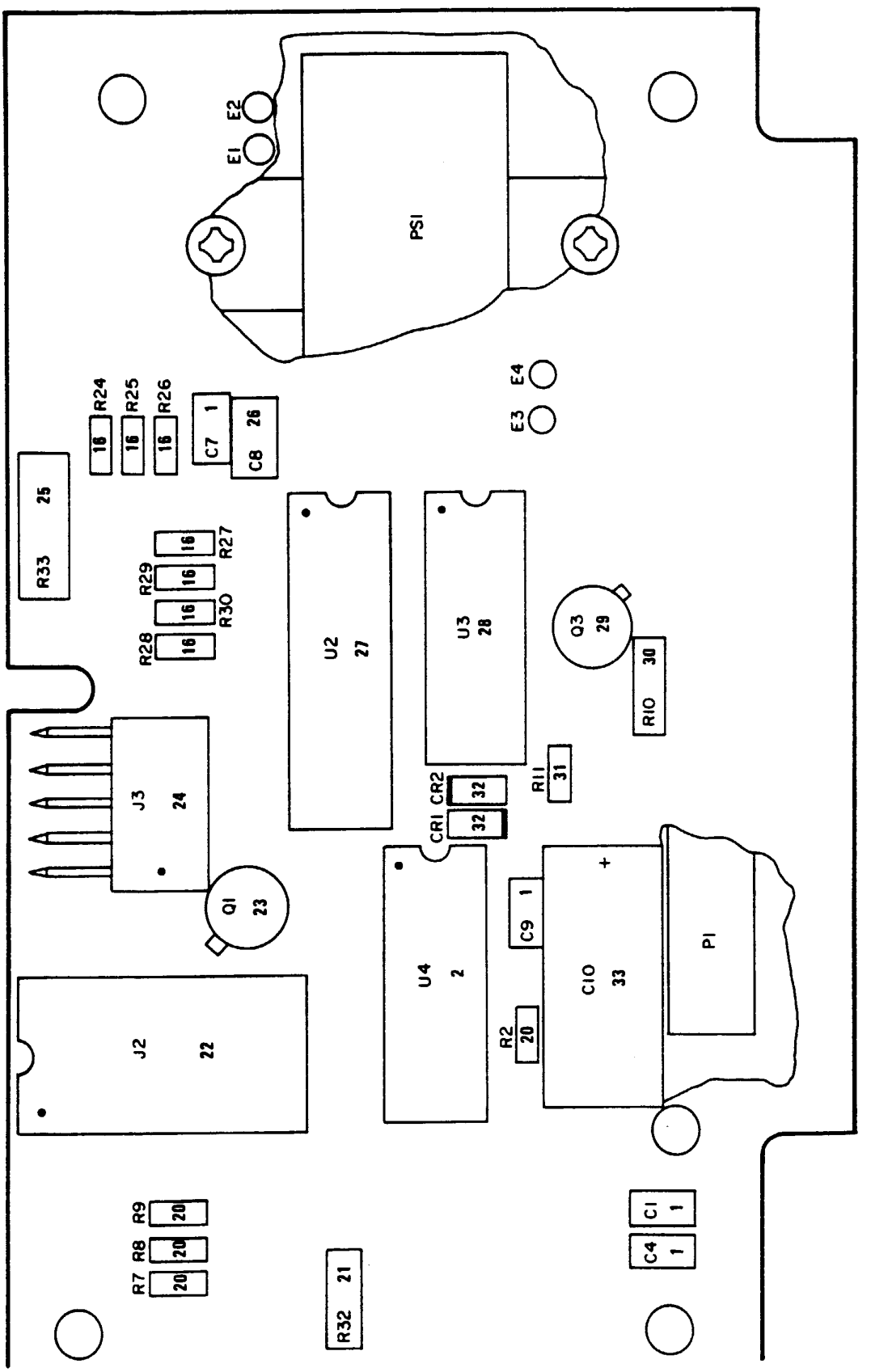


Figure 7-16. Interface Data Converter Circuit Card Assembly (Sheet 2 of 3)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-16-	914870-801	37695	CIRCUIT CARD ASSEMBLY, ... Interface data converter (see fig. 14 for nha)	REF		PADLD
- 1	M39014/01-1473	81349	. CAPACITOR	6		PADZZ
*	M39014/01-1593	81349	. CAPACITOR	6		PADZZ
- 2	JM38510/11201 BCX	81349	. MICROCIRCUIT	2		PADZZ
*	M38510/11201 BCB	81349	. MICROCIRCUIT	2		PADZZ
=	615506-901	37695	. MICROCIRCUIT, Linear	2		PADZZ
- 3	RNC55H3831FR	81349	. RESISTOR	2		PADZZ
*	RNC55H3831FR	81349	. RESISTOR	2		PADZZ
- 4	RCR07G471JS	81349	. RESISTOR	1		PADZZ
- 5 +	RCR05G101JS	81349	. RESISTOR	1		PADZZ
+	RCR05G111JS	81349	. RESISTOR	1		PADZZ
+	RCR05G121JS	81349	. RESISTOR	1		PADZZ
+	RCR05G131JS	81349	. RESISTOR	1		PADZZ
+	RCR05G151JS	81349	. RESISTOR	1		PADZZ
+	RCR05G161JS	81349	. RESISTOR	1		PADZZ
+	RCR05G470JS	81349	. RESISTOR	1		PADZZ
+	RCR05G560JS	81349	. RESISTOR	1		PADZZ
+	RCR05G680JS	81349	. RESISTOR	1		PADZZ
+	RCR05G820JS	81349	. RESISTOR	1		PADZZ
- 6	RCR05G753JS	81349	. RESISTOR	1		PADZZ
- 7	616195-910	37695	. MICROCIRCUIT, Linear	1		PADZZ
- 8	7717-15N-WHITE	13103	. INSULATOR (Magnavox ..... spec cont dwg 447173-2)	1		PADZZ
- 9	617713-902	37695	. TRANSISTOR	1		PADZZ
- 10	7717-15DAP-BLACK	13103	. INSULATOR (Magnavox ..... spec cont dwg 447173-7)	1		PADZZ
- 11	M39014/01-1237	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1357	81349	. CAPACITOR	1		PADZZ
- 12	RCR05G474JS	81349	. RESISTOR	1		PADZZ
- 13	RCR05G104JS	81349	. RESISTOR	4		PADZZ
- 14	RCR05G304JS	81349	. RESISTOR	1		PADZZ
- 15	RCR05G5R1JS	81349	. RESISTOR	1		PADZZ
- 16	RCR05G102JS	81349	. RESISTOR	8		PADZZ
- 17	M39003/01-2373	81349	. CAPACITOR	1		PADZZ
*	M39003/01-3093	81349	. CAPACITOR	1		PADZZ
- 18	RCR05G101JS	81349	. RESISTOR	3		PADZZ
- 19	616391-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 20	RCR05G103JS	81349	. RESISTOR	5		PADZZ
- 21	RCR07G560JS	81349	. RESISTOR	1		PADZZ

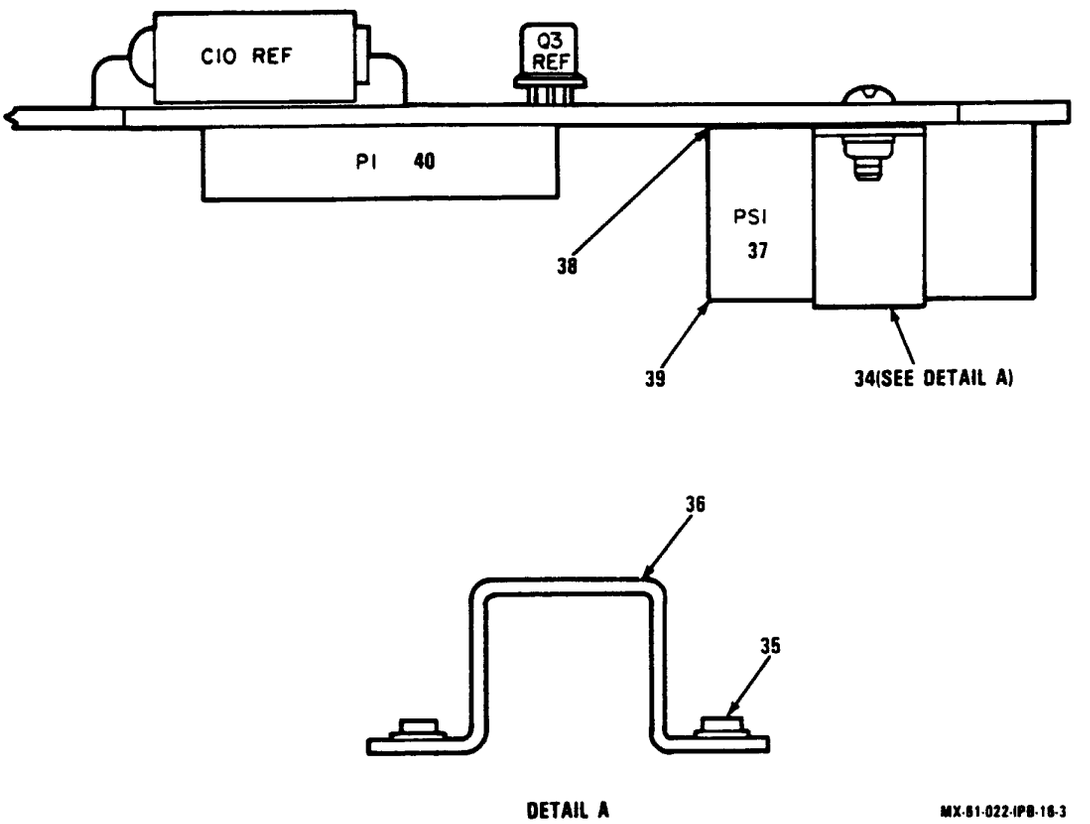


Figure 7-16. Interface Data Converter Circuit Card Assembly (Sheet 3 of 3)

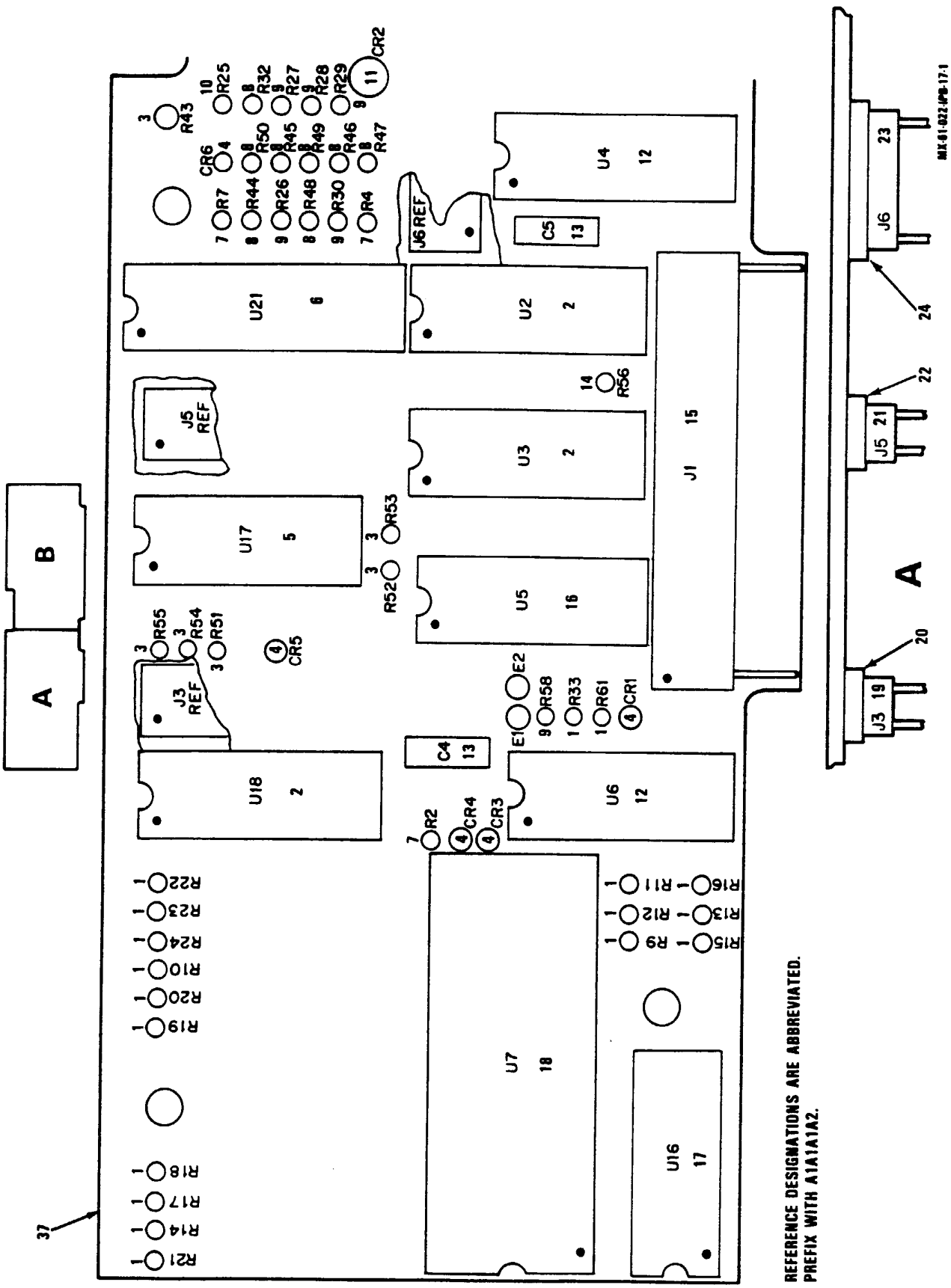


Figure 7-17. Memory I/O Data Converter Board Circuit Card Assembly (Sheet 1 of 2)

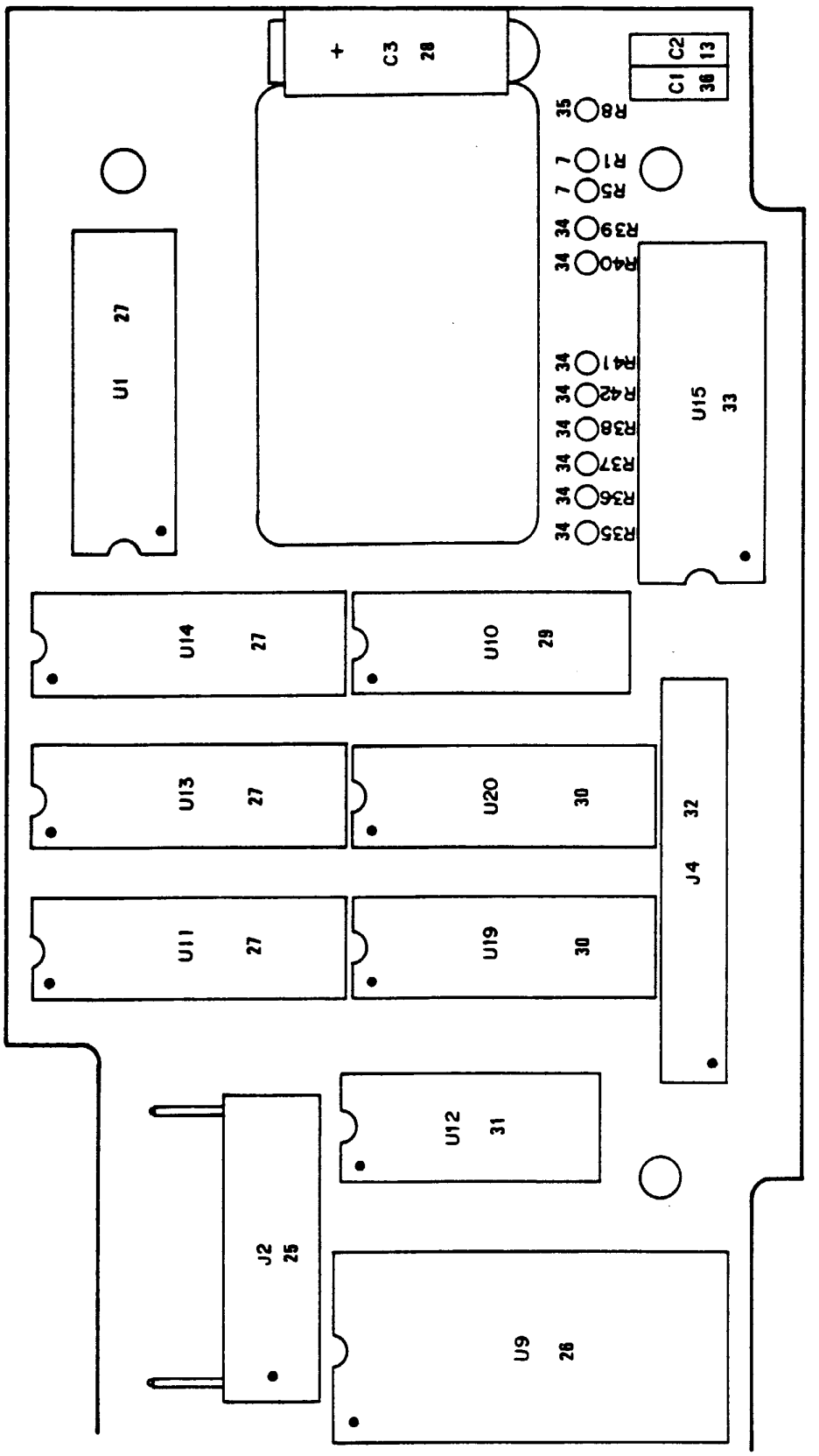


Figure 7-17. Memory I/O Data Converter Board Circuit Card Assembly (Sheet 2 of 2)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-16- 22	616-AG1	91506	. TERMINAL HEADER ..... (Magnavox spec cont dwg 205327-6)	1		PADZZ
*	616AG1	91506	. TERMINAL HEADER	1		PADZZ
- 23	JANTX2N2222A	81350	. TRANSISTOR	1		PADZZ
- 24	103007-2	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185763-212)	1		
- 25	RCR20G513JS	81349	. RESISTOR	1		PADZZ
- 26	S106R	17554	. CAPACITOR, Fixed, ... electrolytic (Magnavox spec cont dwg 275056-75)	1		PADZZ
- 27	616667-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 28	616501-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
=	JM38510/05151 BCX	81349	. MICROCIRCUIT	1		PADZZ
- 29	JANTX2N2907A	81350	. TRANSISTOR	1		PADZZ
- 30	RCR07G390JS	81349	. RESISTOR	1		PADZZ
- 31	RCR05G472JS	81349	. RESISTOR	1		PADZZ
- 32	JANTX1N4454-1	81350	. SEMICONDUCTOR DEVICE	2		PADZZ
- 33	M39006/09-8337	81349	. CAPACITOR	1		PADZZ
*	M39006/09-0588	81349	. CAPACITOR	1		PADZZ
- 34	938734-801	37695	. BRACKET ASSEMBLY, ... Mounting	1		XB
	MS51957-3	96906	. SCREW (AP)	1		PADZZ
- 35	M45938/5-1C	81349	. . NUT	2		PADZZ
- 36	938734-1	37695	. . BRACKET, Mounting	1		XB
- 37	81-0317-02	57026	. POWER SUPPLY (Magnavox ... spec cont dwg 535340-1)	1		PADZZ
- 38	348421-1	37695	. INSULATOR	1		MD
- 39	939010-1	37695	. SHIELD, Electrical	1		XB
- 40	5220-32-2	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185173-222)	1		PADZZ
- 41	410903-1	37695	. PRINTED WIRING BOARD	1		XB
7-17-	914871-805	37695	CIRCUIT CARD ASSEMBLY, ... Memory I/O data converter board (See fig. 14 for nha) (Alternate part)	REF	A	PADLD

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-17-	914871-807	37695	CIRCUIT CARD ASSEMBLY, ... Memory I/O data converter board (See fig. 14 for nha) (Preferred part)	REF	B	
- 1	RCR05G514JS	81349	. RESISTOR	18		PADZZ
- 2	616379-901	37695	. MICROCIRCUIT, Digital	3		PADZZ
- 3	RCR05G103JS	81349	. RESISTOR	6		PADZZ
- 4	JANTX1N4454-1	81350	. SEMICONDUCTOR DEVICE	5		PADZZ
- 5	JM38510/17103 BCX	81349	. MICROCIRCUIT	1		PADZZ
*	M38510/17103 BCB	81349	. MICROCIRCUIT	1		PADZZ
=	615975-903	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 6	616387-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 7	RCR05G5R1JS	81349	. RESISTOR	5		PADZZ
- 8	RCR05G102JS	81349	. RESISTOR	8		PADZZ
- 9	RCR05G104JS	81349	. RESISTOR	6		PADZZ
- 10	RCR05G562JS	81349	. RESISTOR	1		PADZZ
- 11	JANTX1N751A1	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
- 12	JM38510/17501 BEX	81349	. MICROCIRCUIT	2		PADZZ
*	M38510/17501 BEB	81349	. MICROCIRCUIT	2		PADZZ
=	616503-904	37695	. MICROCIRCUIT, Digital	2		PADZZ
- 13	M39014/02-1230	81349	. CAPACITOR	3		PADZZ
*	M39014/02-1350	81349	. CAPACITOR	3		PADZZ
- 14	RCR05G152JS	81349	. RESISTOR	1		PADZZ
- 15	103008-9	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185627-17)	1		PADZZ
- 16	615699-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 17	615976-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 18	646337-5	37695	. MICROCIRCUIT, Digital	1	A	PADZZ
	647238-1	37695	. MICROCIRCUIT, Digital	1	B	
- 19	185763-220	37695	. CONNECTOR, Receptacle	1		PADZZ
- 20	348132-3	37695	. SPACER, Connector	1		XB
- 21	185763-219	37695	. CONNECTOR, Receptacle	1		PADZZ
- 22	348132-4	37695	. SPACER, Connector	1		XB
- 23	185763-212	37695	. CONNECTOR, Receptacle	1		PADZZ
- 24	348132-1	37695	. SPACER, Connector	1		XB
- 25	103008-4	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185627-23)	1		PADZZ
- 26	646339-1	37695	. MICROCIRCUIT, Digital	1		PADZZ
=	646339-2	37695	. MICROCIRCUIT, Digital	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-17- 27	616391-901	37695	. MICROCIRCUIT, Digital	4		PADZZ
- 28	M39003/01-2373	81349	. CAPACITOR	1		PADZZ
*	M39003/01-3093	81349	. CAPACITOR	1		PADZZ
- 29	JM38510/17601 BEX	81349	. MICROCIRCUIT	1		PADZZ
*	M38510/17601 BEB	81349	. MICROCIRCUIT	1		PADZZ
=	619998-1	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 30	616789-901	37695	. MICROCIRCUIT, Digital	2		PADZZ
- 31	616377-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 32	185763-222	37695	. CONNECTOR, Receptacle	1		PADZZ
- 33	615660-903	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 34	RCR05G513JS	81349	. RESISTOR	8		PADZZ
- 35	RCR05G510JS	81349	. RESISTOR	1		PADZZ
- 36	M39014/02-1407	81349	. CAPACITOR	1		PADZZ
*	M39014/02-1419	81349	. CAPACITOR	1		PADZZ
- 37	410904-1	37695	. PRINTED WIRING BOARD	1		XB
			A - Used on 914871-805 only B - Used on 914871-807 only			
7-18-	914892-803	37695	CIRCUIT CARD ASSEMBLY, ... Data converter/CPU (see fig. 14 for nha)	REF		PADLD
- 1	616391-901	37695	. MICROCIRCUIT, Digital	2		PADZZ
- 2	RCR05G102JS	81349	. RESISTOR	11		PADZZ
- 2A	RCR05G101JS	81349	. RESISTOR	1		PADZZ
- 3	RCR05G104JS	81349	. RESISTOR	21		PADZZ
- 4	RCR05G100JS	81349	. RESISTOR	3		PADZZ
- 5	RCR05G105JS	81349	. RESISTOR	1		PADZZ
- 6	616387-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 7	JM38510/47001 BQX	81349	. MICROCIRCUIT	1		
=	616388-902	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 8	87362-3	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185626-9)	1		PADZZ
- 9	RCR05G513JS	81349	. RESISTOR	8		PADZZ
- 10	87362-5	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185626-13)	1		PADZZ
- 11	JM38510/05252 BCX	81349	. MICROCIRCUIT	1		
=	616505-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 12	JM38510/17702 BCX	81349	. MICROCIRCUIT	1		
=	616377-901	37695	. MICROCIRCUIT, Digital	1		PADZZ

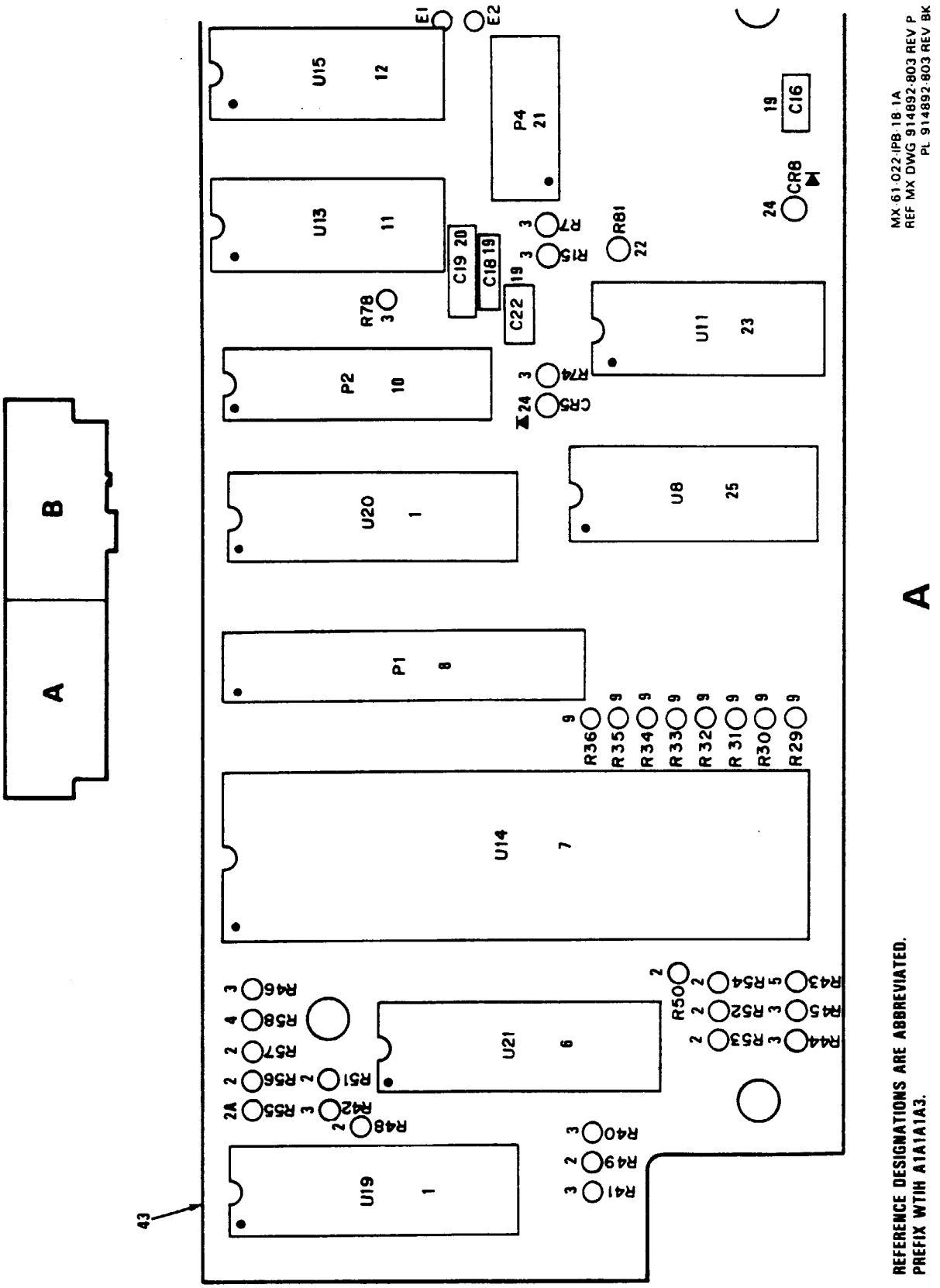


Figure 7-18. Data Converter - CPU Circuit Card Assembly (Sheet 1 of 2)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-18- 13 +	RCR05G514JS	81349	. RESISTOR	1		PADZZ
+	RCR05G564JS	81349	. RESISTOR	1		PADZZ
+	RCR05G624JS	81349	. RESISTOR	1		PADZZ
+	RCR05G684JS	81349	. RESISTOR	1		PADZZ
+	RCR05G754JS	81349	. RESISTOR	1		PADZZ
+	RCR05G824JS	81349	. RESISTOR	1		PADZZ
+	RCR05G914JS	81349	. RESISTOR	1		PADZZ
- 14	M39014/01-1455	81349	. CAPACITOR	2		PADZZ
*	M39014/01-1575	81349	. CAPACITOR	2		PADZZ
- 15	JM38510/17101 BCX	81349	. MICROCIRCUIT	2		PADZZ
=	615975-901	37695	. MICROCIRCUIT, Digital	2		PADZZ
- 16	RCR05G242JS	81349	. RESISTOR	2		PADZZ
- 17	RCR05G203JS	81349	. RESISTOR	2		PADZZ
- 18	RCR05G514JS	81349	. RESISTOR	2		PADZZ
- 19	M39014/01-1473	81349	. CAPACITOR	8		PADZZ
*	M39014/01-1593	81349	. CAPACITOR	8		PADZZ
- 20 +	M39014/01-1463	81349	. CAPACITOR	1		PADZZ
+*	M39014/01-1583	81349	. CAPACITOR	1		PADZZ
+	M39014/01-1464	81349	. CAPACITOR	1		PADZZ
+*	M39014/01-1584	81349	. CAPACITOR	1		PADZZ
+	M39014/01-1466	81349	. CAPACITOR	1		PADZZ
+*	M39014/01-1586	81349	. CAPACITOR	1		PADZZ
+	M39014/01-1467	81349	. CAPACITOR	1		PADZZ
+*	M39014/01-1587	81349	. CAPACITOR	1		PADZZ
+	M39014/01-1469	81349	. CAPACITOR	1		PADZZ
+*	M39014/01-1589	81349	. CAPACITOR	1		PADZZ
- 21	1-87518-0	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185626-10)	1		PADZZ
- 22	RCR05G103JS	81349	. RESISTOR	5		PADZZ
- 23	JM38510/17001 BCX	81349	. MICROCIRCUIT	1		
=	615976-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 24	JANTX1N4454-1	81350	. SEMICONDUCTOR DEVICE	4		PADZZ
- 25	JM38510/17501 BEX	81349	. MICROCIRCUIT	1		PADZZ
*	M38510/17501 BEB	81349	. MICROCIRCUIT	1		PADZZ
=	616503-904	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 26	616501-901	37695	. MICROCIRCUIT, Digital	3		PADZZ
- 27	RCR05G684JS	81349	. RESISTOR	1		PADZZ
- 28	646294-901	37695	. SEMICONDUCTOR DEVICE, ... Diode	2		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-18-	= 646294-902	37695	. SEMICONDUCTOR DEVICE, ... Diode	2		PADZZ
	= 646294-903	37695	. SEMICONDUCTOR DEVICE, ... Diode	2		PADZZ
- 29	RCR05G163JS	81349	. RESISTOR	1		PADZZ
- 30	JM38510/31302 BCX	81349	. MICROCIRCUIT	1		PADZZ
	* M38510/31302 BCB	81349	. MICROCIRCUIT	1		PADZZ
	= 645546-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 31	616670-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 32	646265-901	37695	. MICROCIRCUIT, Digital	1		PADZZ
- 33	RCR05G432JS	81349	. RESISTOR	1		PADZZ
- 34	CR69A/U3.2MHZ	81349	. CRYSTAL UNIT	1		PADZZ
	* CR69A/U3.20000 OMHZ	81349	. CRYSTAL UNIT	1		PADZZ
- 35	+ CCR05CG270JM	81349	. CAPACITOR	1		
	+* M39014/01-1327	81349	. CAPACITOR	1		PADZZ
	+ CCR05CG220JM	81349	. CAPACITOR	1		
	+ CCR05CG240JM	81349	. CAPACITOR	1		
	+* M39014/01-1330	81349	. CAPACITOR	1		PADZZ
	+ CCR05CG300JM	81349	. CAPACITOR	1		
	+* M39014/01-1330	81349	. CAPACITOR	1		PADZZ
	+ CCR05CG330JM	81349	. CAPACITOR	1		
	+* M39014/01-1332	81349	. CAPACITOR	1		PADZZ
	+ CCR05CG180JM	81349	. CAPACITOR	1		
	+* M39014/01-1333	81349	. CAPACITOR	1		PADZZ
	+ CCR05CG360JM	81349	. CAPACITOR	1		
	+* M39014/01-1335	81349	. CAPACITOR	1		PADZZ
- 36	M39012/96-0001	81349	. CONNECTOR	1		PADZZ
	= 16-0210-002	19505	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 189175-8)	1		
- 37	M39003/01-2273	81349	. CAPACITOR	1		PADZZ
	* M39003/01-2992	81349	. CAPACITOR	1		PADZZ
- 38	JANTX1N647-1	81350	. SEMICONDUCTOR DEVICE	2		PADZZ
- 39	103008-3	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185627-15)	1		PADZZ
- 40	JANTX2N2222A	81350	. TRANSISTOR	2		PADZZ
	7717-46N-WHITE	13103	. INSULATOR, Transistor (Magnavox spec cont dwg 445214-106)			
- 41	258268-1232	37695	. CAPACITOR	1		

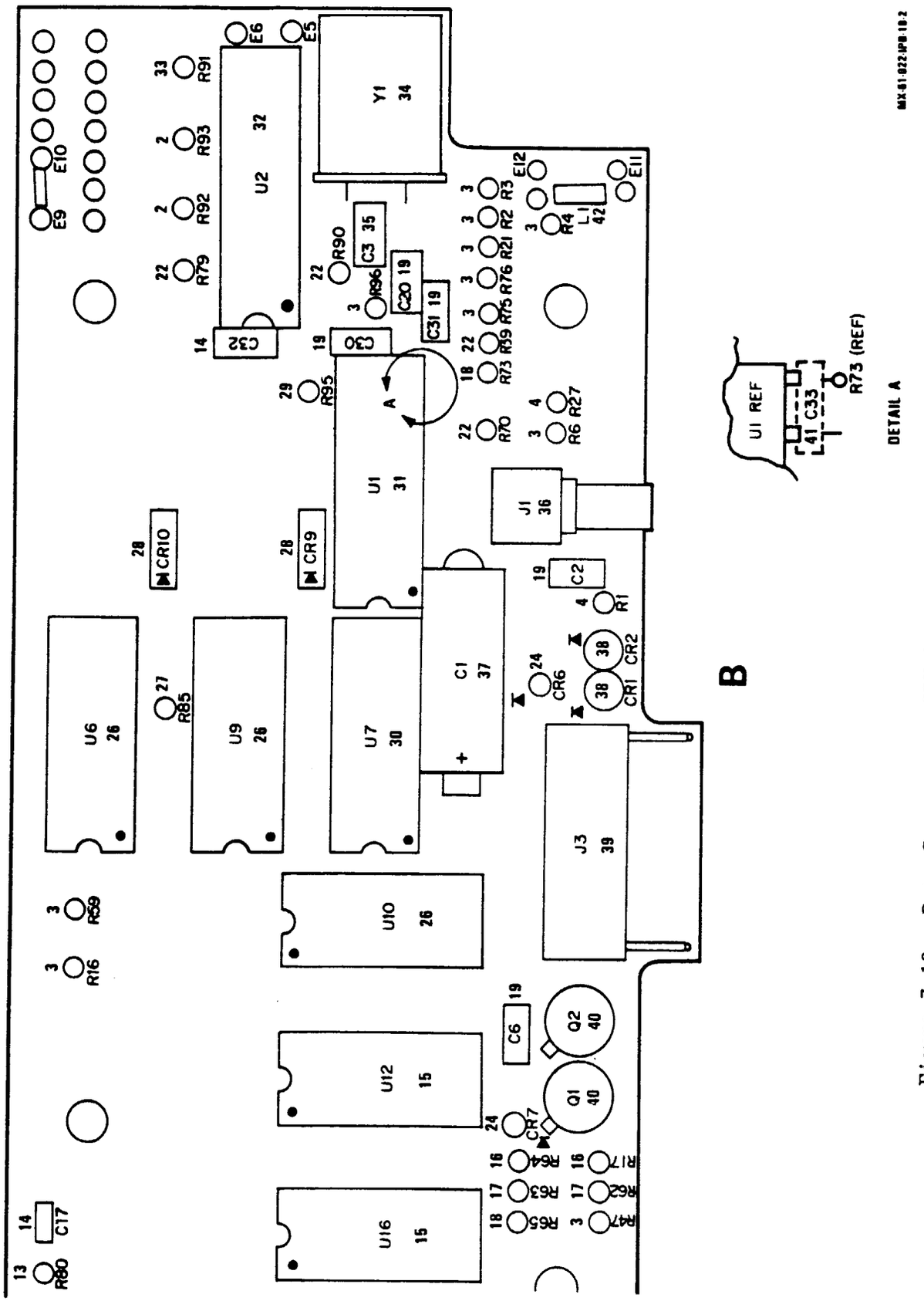


Figure 7-18. Data Converter - CPU Circuit Card Assembly (Sheet 2 of 2)

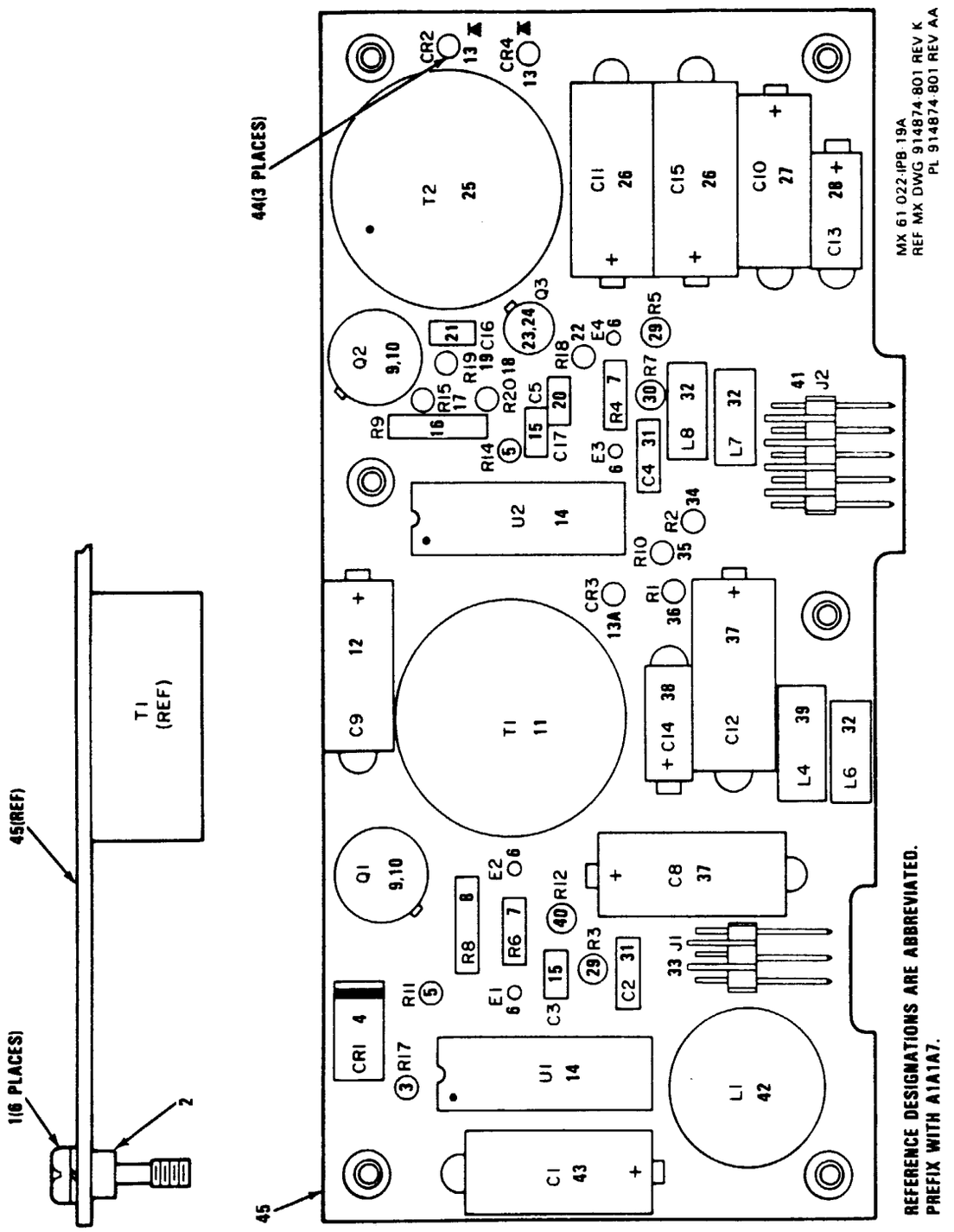


Figure 7-19. Power Regulator Circuit Card Assembly

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-18- 42 +	MS75085-1	96906	. COIL	1		PADZZ
+	MS75085-16	96906	. COIL	1		PADZZ
+	MS75085-3	96906	. COIL	1		PADZZ
+	MS75085-4	96906	. COIL	1		PADZZ
+	MS75085-5	96906	. COIL	1		PADZZ
- 43	410913-1	37695	. PRINTED WIRING BOARD	1		XB
7-19-	914874-801	37695	CIRCUIT CARD ASSEMBLY, ... Power regulator (see fig. 2 for nha)	REF		PAFLD
- 1	136435-14	37695	. SCREW, Panhead (AP)	6		PADZZ
	MS35338-135	96906	. WASHER (AP)	6		PADZZ
- 2	514886-1	37695	. WASHER, Threaded (AP)	6		PADZZ
- 3	RCR07G7R5JS	81349	. RESISTOR	1		PADZZ
- 4	616689-903	37695	. SEMICONDUCTOR DEVICE, ... Diode	1		PADZZ
- 5	RCR07G510JS	81349	. RESISTOR	2		PADZZ
- 6	M55155-29-5	81349	. TERMINAL	4		PADZZ
=	160-2085-02-05-03	71279	. TERMINAL, Stud ..... (Magnavox spec cont dwg 208462-1293)	4		PADZZ
- 7 +	RCR07G472JS	81349	. RESISTOR	2		PADZZ
+	RCR07G512JS	81349	. RESISTOR	2		PADZZ
+	RCR07G332JS	81349	. RESISTOR	2		PADZZ
+	RCR07G362JS	81349	. RESISTOR	2		PADZZ
+	RCR07G392JS	81349	. RESISTOR	2		PADZZ
+	RCR07G432JS	81349	. RESISTOR	2		PADZZ
- 8	RWR80SR402FP	81349	. RESISTOR	1		PADZZ
*	RWR80SR402FR	81349	. RESISTOR	1		PADZZ
- 9	JANTX2N2905A	81350	. TRANSISTOR	2		PADZZ
- 10	7717-15N	13103	. MOUNTING PAD (Magnavox ... spec cont dwg 447173-1)	2		PADZZ
=	7717-15DAP	13103	. MOUNTING PAD	2		PADZZ
- 11	MT-3785	37695	. TRANSFORMER, Power, ... step-up (Magnavox spec cont dwg 308202-1)	1		PADZZ
- 12	M39003/01-2379	81349	. CAPACITOR	1		PADZZ
*	M39003/01-3099	81349	. CAPACITOR	1		PADZZ
- 13	JANTX1N5802	81350	. SEMICONDUCTOR DEVICE	2		PADZZ
*	JANTX1N5804	81350	. SEMICONDUCTOR DEVICE	2		PADZZ
- 13A	JANTX1N5806	81350	. SEMICONDUCTOR DEVICE	1		PADZZ
- 14	616400-901	37695	. MICROCIRCUIT, Linear	2		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-19- 15	M39014/01-1237	81349	. CAPACITOR	2		PADZZ
*	M39014/01-1357	81349	. CAPACITOR	2		PADZZ
- 16	RWR80SR499FP	81349	. RESISTOR	1		PADZZ
*	RWR80SR499FR	81349	. RESISTOR	1		PADZZ
- 17	RCR07G100JS	81349	. RESISTOR	1		PADZZ
- 18	RCR07G6R8JS	81349	. RESISTOR	1		PADZZ
- 19	RCR07G101JS	81349	. RESISTOR	1		PADZZ
- 20	M39014/01-1446	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1566	81349	. CAPACITOR	1		PADZZ
- 21	M39014/01-1473	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1593	81349	. CAPACITOR	1		PADZZ
- 22	RCR07G103JS	81349	. RESISTOR	1		PADZZ
- 23	JANTX2N2907A	81350	. TRANSISTOR	1		PADZZ
- 24	7717-43N-WHITE	13103	. MOUNTING PAD (Magnavox ... spec cont dwg 447279-108)	1		PADZZ
=	7717-43DAP	13103	. MOUNTING PAD	1		PADZZ
- 25	MT-3786	37695	. TRANSFORMER, Power, ... step-up (Magnavox spec cont dwg 308201-1)	1		PADZZ
- 26	M39003/01-2302	81349	. CAPACITOR	2		PADZZ
*	M39003/01-3021	81349	. CAPACITOR	2		PADZZ
- 27	M39003/01-2296	81349	. CAPACITOR	1		PADZZ
*	M39003/01-3015	81349	. CAPACITOR	1		PADZZ
- 28	M39003/01-2290	81349	. CAPACITOR	1		PADZZ
*	M39003/01-3009	81349	. CAPACITOR	1		PADZZ
- 29	RNC55H1471FR	81349	. RESISTOR	2		PADZZ
*	RNC55H1471FS	81349	. RESISTOR	2		PADZZ
- 30	RNC55H1002FR	81349	. RESISTOR	1		PADZZ
*	RNC55H1002FS	81349	. RESISTOR	1		PADZZ
- 31	M39014/02-1407	81349	. CAPACITOR	2		PADZZ
*	M39014/02-1419	81349	. CAPACITOR	2		PADZZ
- 32	MS75089-3	96906	. COIL	3		PADZZ
=	M39010/3A220KX	81349	. COIL	3		PADZZ
- 33	185627-5	37695	. CONNECTOR, Receptacle, ... electrical	1		PADZZ
- 34	RCR07G123JS	81349	. RESISTOR	1		PADZZ
- 35	RCR07G105JS	81349	. RESISTOR	1		PADZZ
- 36	RCR07G184JS	81349	. RESISTOR	1		PADZZ
- 37	M39003/01-2273	81349	. CAPACITOR	2		PADZZ
*	M39003/01-2997	81349	. CAPACITOR	2		PADZZ
- 38	M39003/01-2369	81349	. CAPACITOR	1		PADZZ
*	M39003/01-3088	81349	. CAPACITOR	1		PADZZ
- 39	MS75101-4	96906	. COIL	1		PADZZ

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-19- 40	RNC55H4421FR	81349	. RESISTOR	1		PADZZ
*	RNC55H4421FS	81349	. RESISTOR	1		PADZZ
- 41	103008-2	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185627-14)	1		PADZZ
- 42	325277-1	37695	. REACTOR, Power	1		PADZZ
- 43	M39003/01-2381	81349	. CAPACITOR	1		PADZZ
*	M39003/01-3100	81349	. CAPACITOR	1		PADZZ
- 44	107240-40	37695	. WASHER, Nonmetallic	3		PADZZ
- 45	410907-1	37695	. PRINTED WIRING BOARD	1		XB
7-20-	811963-802	37695	CIRCUIT CARD ASSEMBLY, ... Power switching (See fig. 2 for nha) (Preferred item)	REF	A	PAFLD
	811963-801	37695	CIRCUIT CARD ASSEMBLY, ... Power switching (See fig. 2 for nha) (Alternate item)	REF	B	PAFLD
Q1 - 1	619999-902	37695	. TRANSISTOR	1		PADZZ
- 2	MS51957-16	96906	. SCREW (AP)	2		PADZZ
	348290-1	37695	. SPACER, Insulator (AP) ...	2		PADZZ
	MS35333-153	96906	. WASHER (AP)	2		PADZZ
	NAS671C4	80265	. NUT (AP)	2		PADZZ
- 3	449419-1	37695	. INSULATOR, Plate	1		PADZZ
- 4	439317-1	37695	. HEAT SINK, Transistor	1		PADZZ
- 5	348799-1	37695	. INSULATOR, Transistor	1		PADZZ
Q2 - 6	JANTX2N3029	81350	. HCI TRANSISTOR	1		PADZZ
=	615949-1	37695	. HCI TRANSISTOR	1		PADZZ
- 7	M38527/3-01N	81349	. MOUNTING PAD	2		PADZZ
*	M38527/3-01D	81349	. MOUNTING PAD	2		PADZZ
C23 - 8	JANTX2N4858	81350	. TRANSISTOR	1		PADZZ
- 9	RCR07G102JS	81349	. RESISTOR	1		PADZZ
- 10	M39014/01-1237	81349	. CAPACITOR	1		PADZZ
*	M39014/01-1357	81349	. CAPACITOR	1		PADZZ
- 11	136435-14	37695	. SCREW, Panhead (AP)	3		PAFZZ
- 11A	109429-8	37695	. WASHER, Insulator (AP) ...	1		
	MS35338-135	96906	. WASHER (AP)	3		PAFZZ
	NAS620C4	81205	. WASHER (AP)	3		PAFZZ
- 12	514886-1	37695	. WASHER, Threaded	1		PADZZ
- 13	616689-903	37695	. SEMICONDUCTOR DEVICE, ... Diode	2		PADZZ

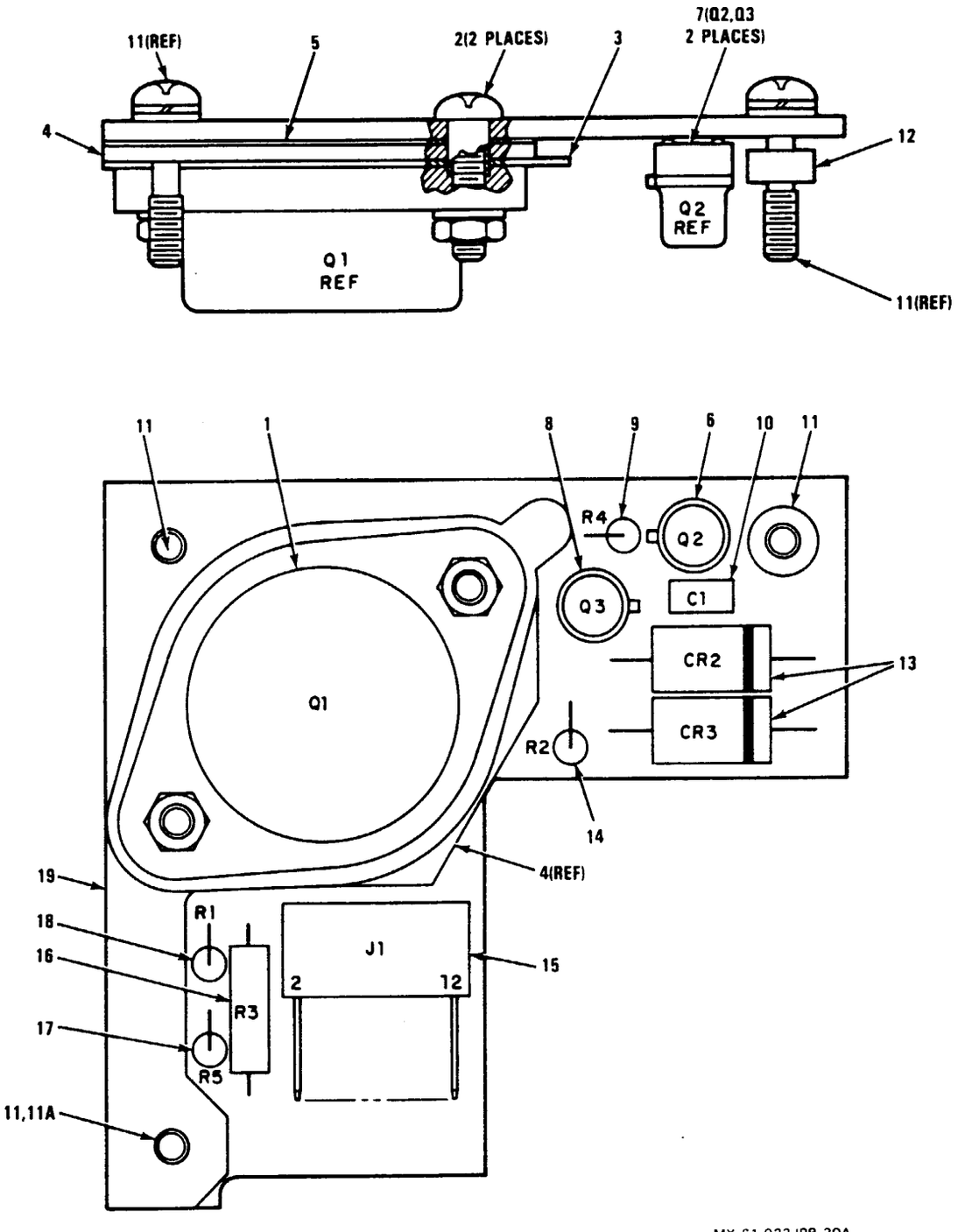
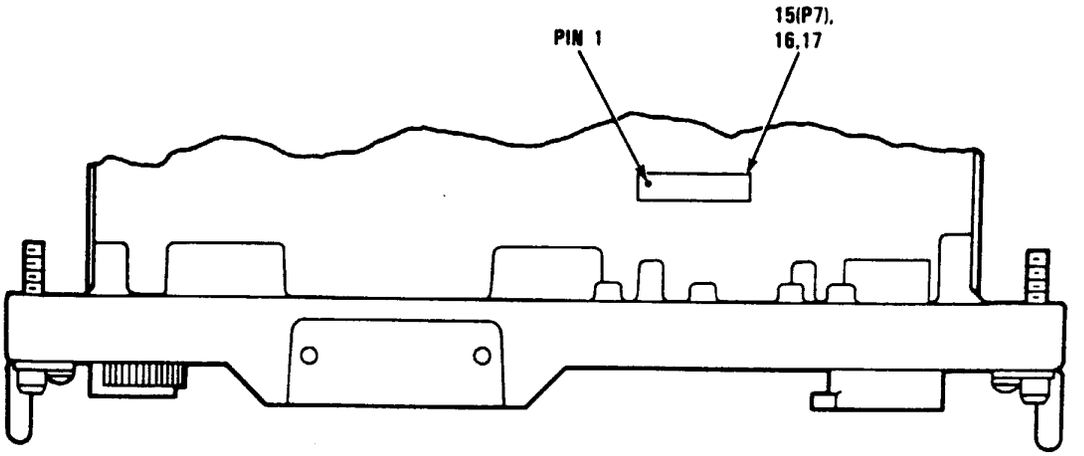
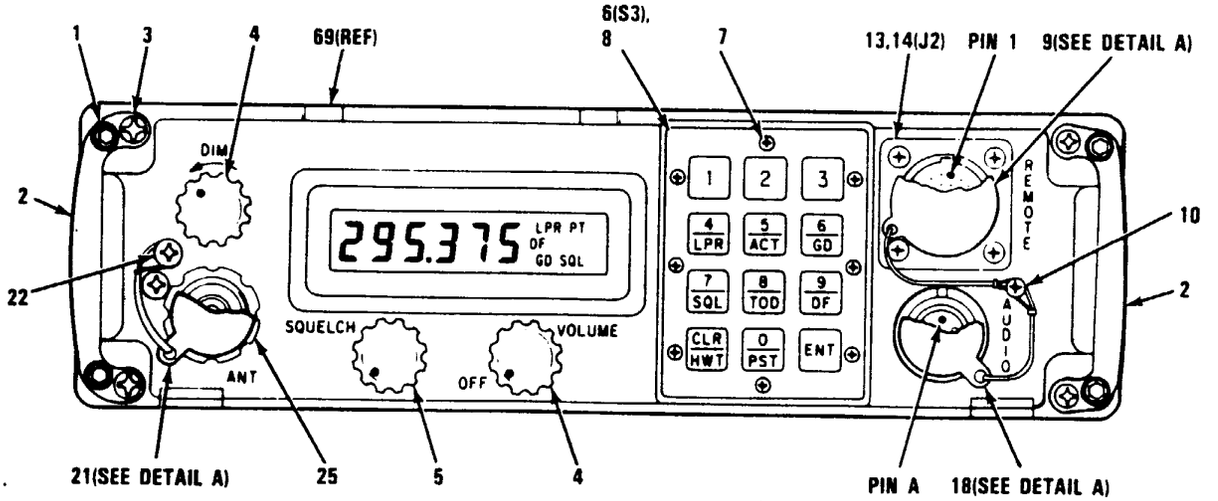


Figure 7-20. Power Switching Circuit Card Assembly





REFERENCE DESIGNATIONS ARE ABBREVIATED.
PREFIX WITH A1A8.

MX-81-022-IPB-21-1
REF MX DWG 914860-801 REV P
PL 914860-801 REV AE

Figure 7-21. Electrical Chassis.Assembly (Sheet 1 of 3)

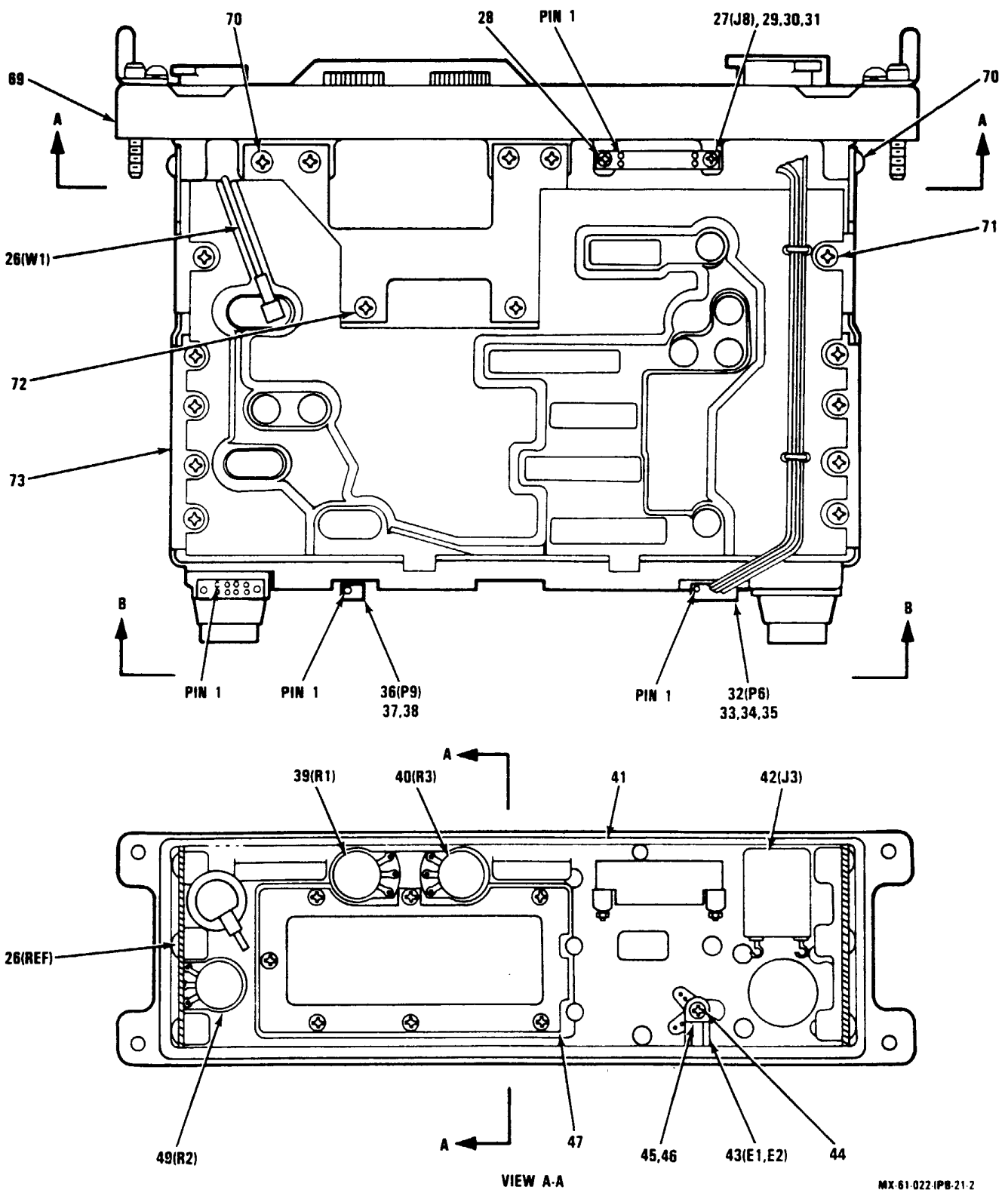


Figure 7-21. Electrical Chassis Assembly (Sheet 2 of 3)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-20- 14	RCR05G203JS	81349	. RESISTOR	1		PADZZ
- 15	86479-4	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185627-1)	1		PADZZ
=	185627-2	37695	. CONNECTOR, Receptacle	1		PADZZ
- 16	RWR80S2051FM	81349	. RESISTOR	1		PADZZ
*	RWR80S2051FR	81349	. RESISTOR	1		PADZZ
- 17	RCR07G303JS	81349	. RESISTOR	1		PADZZ
- 18	RCR07G103JS	81349	. RESISTOR	1		PADZZ
- 19	411964-1	37695	. PRINTED WIRING BOARD	1		XB
			A - Used on 811963-802 only B - Used on 811963-801 only			
7-21-	914860-801	37695	CHASSIS ASSEMBLY, ... Electrical (see fig. 2 for nha)	REF		XB
- 1	435645-102	37695	. SCREW, Externally (AP) ... relieved	4		PAFZZ
- 2	125259-1	37695	. HANDLE, Bow	2		PAOZZ
- 3	MS51957-13B	96906	. SCREW (AP)	2		PAFZZ
	MS35338-135B	96906	. WASHER (AP)	2		PAFZZ
- 4	101909-3	99813	. KNOB (Magnavox spec cont . dwg 145131-3)	2		PAFZZ
	NAS1081C04D3L	80205	. SETSCREW (AP)	2		PAFZZ
- 5	101909-1	99813	. KNOB (Magnavox spec cont . dwg 145131-1)	2		PAOZZ
	NAS1081C04D3L	80205	. SETSCREW (AP)	2		PAFZZ
- 6	ML12-25-MBE-3	51163	. KEYBOARD, Sealed ..... (Magnavox spec cont dwg 626483-3)	1		PAFZZ
- 7	MS51957-7B	96906	. SCREW (AP)	8		PADZZ
	MS35338-134B	96906	. WASHER (AP)	8		XB
- 8	347718-1	37695	. GASKET, Keyboard	1		PAFZZ
- 9	812187-801	37695	. CAP ASSEMBLY, Connector ..	1		PAOZZ
- 10	MS51957-16B	96906	. SCREW (AP)	1		PAFZZ
	MS35338-135B	96906	. WASHER (AP)	1		PAFZZ
	514919-2	37695	. RETAINER (AP)	1		PAFZZ
- 11	348919-1	37695	. . COVER, Connector	1		PAOZZ
- 12	938573-1	37695	. . CLIP	2		PAOZZ
- 13	842391-3	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 186169-1)	1		PADZZ
	MS51957-13B	96906	. SCREW (AP)	4		PAFZZ
- 14	21-0116-0022	12881	. SHIELDING GASKET ..... (Magnavox spec cont dwg 445994-7)	1		PADZZ

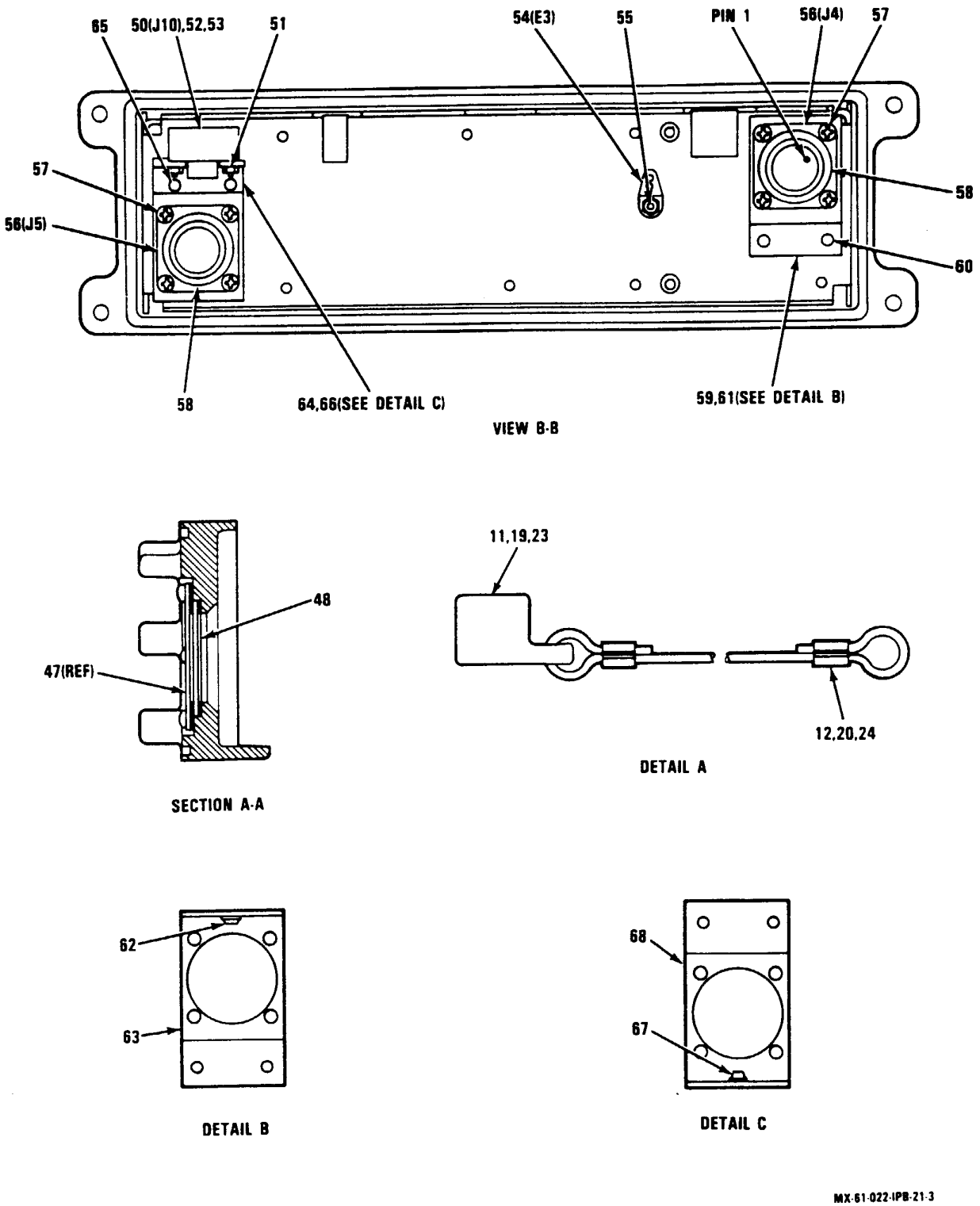


Figure 7-21. Electrical Chassis Assembly (Sheet 3 of 3)

FIGURE AND INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-21- 15	189341-31	37695	. CONNECTOR, Plug	1		PADZZ
- 16	86015-4	00779	. CONTACT, Electrical ..... (Magnavox spec cont dwg 168993-1)	17		PADZZ
- 17	87077-2	00779	. PLUG, Keying (Magnavox ... spec cont dwg 348427-1)	1		PADZZ
- 18	812187-802	37695	. CAP ASSEMBLY, Connector ..	1		XB
- 19	348205-2	37695	. . COVER, Connector	1		PAOZZ
- 20	938573-1	37695	. . CLIP	1		PAOZZ
- 21	812187-805	37695	. CAP ASSEMBLY, Connector ..	1		XB
- 22	MS51957-14B	96906	. SCREW (AP)	1		PAFZZ
	MS35338-135B	96906	. WASHER (AP)	1		PAFZZ
	514919-1	37695	. RETAINER (AP)	1		PAFZZ
- 23	348205-5	37695	. . COVER, Connector	1		PAOZZ
- 24	938573-1	37695	. . CLIP	1		PAOZZ
- 25	513770-1	37695	. ADAPTER	1		PADZZ
	MS16995-9	96906	. SCREW (AP)	1		PADZZ
- 26	566021-801	37695	. CABLE ASSEMBLY, Coaxial ..	1		PAFZZ
- 27	103355-1	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185652-9)	1		PADZZ
- 28	MS51959-10	96906	. SCREW (AP)	2		PADZZ
	MS35338-134	96906	. WASHER (AP)	2		PADZZ
	NAS671C2	80205	. NUT (AP)	2		PADZZ
- 29	86015-4	00779	. CONTACT, Electrical ..... (Magnavox spec cont dwg 168993-1)	22		PADZZ
- 30	86016-4	00779	. CONTACT, Electrical ..... (Magnavox spec cont dwg 168993-2)	1		PADZZ
- 31	87077-2	00779	. PLUG, Keying (Magnavox ... spec cont dwg 348427-1)	1		PADZZ
- 32	103333-2	00779	. CONNECTOR, Plug ..... (Magnavox spec cont dwg 189341-23)	1		PADZZ
- 33	86016-4	00779	. CONTACT, Electrical ..... (Magnavox spec cont dwg 168993-2)	10		PADZZ
- 34	87077-2	00779	. PLUG, Keying (Magnavox ... spec cont dwg 348427-1)	1		PADZZ
- 35	86015-4	00779	. CONTACT, Electrical ..... (Magnavox spec cont dwg 168993-1)	1		PADZZ

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7-21- 36	103333-1	00779	. CONNECTOR, Plug ..... (Magnavox spec cont dwg 189341-22)	1		PADZZ
- 37	86016-4	00779	. CONTACT, Electrical ..... (Magnavox spec cont dwg 168993-2)	4		PADZZ
- 38	87077-2	00779	. PLUG, Keying (Magnavox ... spec cont dwg 348427-1)	1		PADZZ
- 39	CM43842-6	50516	. RESISTOR, Variable ..... (Magnavox spec cont dwg 228115-6)	1		PADZZ
- 40	CM43842-1	50516	. RESISTOR, Variable ..... (Magnavox spec cont dwg 228115-1)	1		PADZZ
- 41	348201-1	37695	. GASKET, RFI	1		PAFZZ
- 42	QC283D-1	25330	. HCI CONNECTOR, Surge ..... (Magnavox spec cont dwg 186171-1)	1		PADZZ
- 43	MS77067-1	96906	. TERMINAL	2		PADZZ
- 44	MS51957-15	96906	. SCREW (AP)	1		PADZZ
	MS35338-135	96906	. WASHER (AP)	1		PADZZ
- 45	NAS1397R2B	80205	. CLAMP	1		PAFZZ
- 46	D4-128CAD PLATE IRID YELLOW	95987	. WASHER, Loop clamp ..... (Magnavox spec cont dwg 109605-1)	1		PAFZZ
- 47	439322-1	37695	. HCI SCREEN	1		PAFZZ
	MS51957-13	96906	. SCREW (AP)	7		PAFZZ
- 48	345957-1	37695	. WINDOW, Protective	1		PAFZZ
- 49	CM43842-8	50516	. RESISTOR, Variable ..... (Magnavox spec cont dwg 228115-8)	1		PADZZ
- 50	103355-2	00779	. CONNECTOR, Receptacle .... (Magnavox spec cont dwg 185652-8)	1		PADZZ
- 51	MS51959-8	96906	. SCREW (AP)	2		PADZZ
	MS35338-134	96906	. WASHER (AP)	2		PADZZ
	NAS671C2	80205	. NUT (AP)	2		PADZZ
- 52	87077-2	00779	. PLUG, Keying (Magnavox ... spec cont dwg 348427-1)	1		PADZZ
- 53	86015-4	00779	. CONTACT, Electrical ..... (Magnavox spec cont dwg 168993-1)	6		PADZZ
- 54	MS77068-1	96906	. TERMINAL	1		PADZZ
- 55	MS24693C2	96906	. SCREW (AP)	1		PADZZ
	NAS671C4	80205	. NUT (AP)	1		PADZZ

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- 57	MS51957-15	96906	. SCREW (AP)	4		PAFZZ
	516025-801	37695	. NUT PLATE (AP)	4		
- 58	348136-1	37695	. GASKET, Connector	2		PADZZ
- 59	939369-801	37695	. BRACKET ASSEMBLY, ... Connector mounting	1		XB
- 60	MS24693C2	96906	. SCREW (AP)	2		PAFZZ
	MS35338-135	96906	. WASHER (AP)	2		PAFZZ
	NAS671C4	80205	. NUT (AP)	2		PAFZZ
- 61	MS51957-3	96906	. SCREW (AP)	1		PAFZZ
- 62	M45938/5-1C	81349	. . NUT	1		PAFZZ
- 63	939369-1	37695	. . BRACKET	1		XB
- 64	939870-801	37695	. BRACKET ASSEMBLY, ... Connector mounting	1		XB
- 65	MS24693C2	96906	. SCREW (AP)	2		PAFZZ
	MS35338-135	96906	. WASHER (AP)	2		PAFZZ
	NAS671C4	80205	. NUT (AP)	2		PAFZZ
- 66	MS51959-3	96906	. SCREW (AP)	1		PAFZZ
- 67	M45938/5-1C	81349	. . NUT	1		PAFZZ
- 68	939370-1	37695	. . BRACKET	1		XB
- 69	660145-801	37695	. PANEL ASSEMBLY, Front	1		XB
- 70	MS51957-42	96906	. SCREW (AP)	10		XB
- 71	136435-13	37695	. SCREW, Panhead (AP)	2		PAFZZ
- 72	136435-12	37695	. SCREW, Panhead (AP)	10		PAFZZ
- 73	811839-801	37695	. CHASSIS ASSEMBLY	1		XB

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN
SECTION C
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		CCR05CG330JM	F7-18- 35	CDR14BG111EKSM	7- 9- 80
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		CCR09CG102GR	F7-11-123	CDR14BG161DGSM	F7- 4- 34
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A1A1A1A2U18	7-17- 2	A1A1A1A3R16	7-18- 3	A1A1A1A3R75	7-18- 3
A1A1A1A2U19	7-17- 30	A1A1A1A3R17	7-18- 16	A1A1A1A3R76	7-18- 3
A1A1A1A2U2	7-17- 2	A1A1A1A3R2	7-18- 3	A1A1A1A3R78	7-18- 3
A1A1A1A2U20	7-17- 30	A1A1A1A3R21	7-18- 3	A1A1A1A3R79	7-18- 22
A1A1A1A2U21	7-17- 6	A1A1A1A3R27	7-18- 4	A1A1A1A3R80	7-18- 13
A1A1A1A2U3	7-17- 2	A1A1A1A3R29	7-18- 9	A1A1A1A3R81	7-18- 22
A1A1A1A2U4	7-17- 12	A1A1A1A3R3	7-18- 3	A1A1A1A3R85	7-18- 27
A1A1A1A2U5	7-17- 16	A1A1A1A3R30	7-18- 9	A1A1A1A3R90	7-18- 22
A1A1A1A2U6	7-17- 12	A1A1A1A3R31	7-18- 9	A1A1A1A3R91	7-18- 33
A1A1A1A2U7	7-17- 18	A1A1A1A3R32	7-18- 9	A1A1A1A3R92	7-18- 2
A1A1A1A2U9	7-17- 26	A1A1A1A3R33	7-18- 9	A1A1A1A3R93	7-18- 2
A1A1A1A3	7-14- 9	A1A1A1A3R34	7-18- 9	A1A1A1A3R95	7-18- 29
A1A1A1A3	7-18-REF	A1A1A1A3R35	7-18- 9	A1A1A1A3R96	7-18- 3
A1A1A1A3CR1	7-18- 38	A1A1A1A3R36	7-18- 9	A1A1A1A3U1	7-18- 31
A1A1A1A3CR10	7-18- 28	A1A1A1A3R39	7-18- 22	A1A1A1A3U10	7-18- 26
A1A1A1A3CR2	7-18- 38	A1A1A1A3R4	7-18- 3	A1A1A1A3U11	7-18- 23

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A1A1A1A3U13	7-18- 11
A1A1A1A3U14	7-18- 7
A1A1A1A3U15	7-18- 12
A1A1A1A3U16	7-18- 15
A1A1A1A3U19	7-18- 1
A1A1A1A3U2	7-18- 32
A1A1A1A3U20	7-18- 1
A1A1A1A3U21	7-18- 6
A1A1A1A3U6	7-18- 26
A1A1A1A3U7	7-18- 30
A1A1A1A3U8	7-18- 25
A1A1A1A3U9	7-18- 25
A1A1A1A3Y1	7-18- 34
A1A1A1A4	7-14- 1
A1A1A1A4	7-15-REF
A1A1A1A4DS1	7-15- 8
A1A1A1A4DS2	7-15- 9
A1A1A1A4E1	7-15- 13
A1A1A1A4E2	7-15- 13
A1A1A1A4E3	7-15- 13
A1A1A1A4E4	7-15- 13
A1A1A1A4HR1	7-15- 14
A1A1A1A4P1	7-15- 1
A1A1A1A4R1	7-15- 2
A1A1A1A4U1	7-15- 3
A1A1A1A4U2	7-15- 3
A1A1A2	7- 2- 1
A1A1A2	7- 3-REF
A1A1A2A1	7- 3- 16
A1A1A2A1	7- 4-REF
A1A1A2A1A1	7- 4- 96
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A1A1A2A1A1CR17	7- 5- 4
A1A1A2A1A1CR18	7- 5- 4
A1A1A2A1A1CR19	7- 5- 4
A1A1A2A1A1CR20	7- 5- 13
A1A1A2A1A1CR21	7- 5- 13
A1A1A2A1A1C83	7- 5- 5
A1A1A2A1A1C84	7- 5- 5
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A1A1A2A1A1C87	7- 5- 11
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A1A1A2A1A1C91	7- 5- 15
A1A1A2A1A1C98	7- 5- 17
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A1A1A2A1A1E3	7- 5- 1
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A1A1A2A1A1L46	7- 5- 12
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A1A1A2A1CR1	7- 4- 27
A1A1A2A1CR10	7- 4- 9
A1A1A2A1CR11	7- 4- 9
A1A1A2A1CR12	7- 4- 9
A1A1A2A1CR13	7- 4- 64
A1A1A2A1CR14	7- 4- 64
A1A1A2A1CR15	7- 4- 9
A1A1A2A1CR16	7- 4- 9
A1A1A2A1CR2	7- 4- 6
A1A1A2A1CR22	7- 4- 23
A1A1A2A1CR23	7- 4- 23
A1A1A2A1CR24	7- 4- 23
A1A1A2A1CR25	7- 4- 23
A1A1A2A1CR26	7- 4- 23
A1A1A2A1CR27	7- 4- 23
A1A1A2A1CR28	7- 4- 64
A1A1A2A1CR3	7- 4- 6
A1A1A2A1CR4	7- 4- 23
A1A1A2A1CR5	7- 4- 6
A1A1A2A1CR6	7- 4- 9
A1A1A2A1CR7	7- 4- 9
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A1A1A2A1C101	7- 4- 16
A1A1A2A1C102	7- 4- 8
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A1A1A2A1C104	7- 4- 16
A1A1A2A1C11	7- 4- 16
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A1A1A2A1C21	7- 4- 8
A1A1A2A1C22	7- 4- 19
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A1A1A2A1C27	7- 4- 46A
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A1A1A2A1C31	7- 4- 8
A1A1A2A1C32	7- 4- 8
A1A1A2A1C33	7- 4- 58
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A1A1A2A1C36	7- 4- 59
A1A1A2A1C37	7- 4- 63
A1A1A2A1C39	7- 4- 48A
A1A1A2A1C40	7- 4- 47
A1A1A2A1C41	7- 4- 47
A1A1A2A1C42	7- 4- 82
A1A1A2A1C43	7- 4- 10
A1A1A2A1C44	7- 4- 30
A1A1A2A1C45	7- 4- 80
A1A1A2A1C46	7- 4- 19
A1A1A2A1C47	7- 4- 10
A1A1A2A1C48	7- 4- 12
A1A1A2A1C49	7- 4- 16

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A1A1A2A1C5	7- 4- 13	A1A1A2A1L1	7- 4- 31	A1A1A2A1L58	7- 4- 70
A1A1A2A1C50	7- 4- 16	A1A1A2A1L10	7- 4- 18	A1A1A2A1L59	7- 4- 72
A1A1A2A1C51	7- 4- 10	A1A1A2A1L11	7- 4- 5	A1A1A2A1L6	7- 4- 31
A1A1A2A1C52	7- 4- 8	A1A1A2A1L12	7- 4- 11	A1A1A2A1L60	7- 4- 95
A1A1A2A1C53	7- 4- 10	A1A1A2A1L13	7- 4- 11	A1A1A2A1L61	7- 4- 94
A1A1A2A1C54	7- 4- 8	A1A1A2A1L14	7- 4- 11	A1A1A2A1L62	7- 4- 95
A1A1A2A1C55	7- 4- 10	A1A1A2A1L15	7- 4- 11	A1A1A2A1L63	7- 4- 94
A1A1A2A1C56	7- 4- 8	A1A1A2A1L16	7- 4- 11	A1A1A2A1L64	7- 4- 88
A1A1A2A1C57	7- 4- 8	A1A1A2A1L17	7- 4- 11	A1A1A2A1L65	7- 4- 84
A1A1A2A1C58	7- 4- 8	A1A1A2A1L18	7- 4- 60	A1A1A2A1L66	7- 4- 68
A1A1A2A1C59	7- 4- 8	A1A1A2A1L19	7- 4- 60	A1A1A2A1L67	7- 4- 67
A1A1A2A1C6	7- 4- 16	A1A1A2A1L2	7- 4- 37	A1A1A2A1L68	7- 4- 86
A1A1A2A1C60	7- 4- 8	A1A1A2A1L20	7- 4- 7	A1A1A2A1L69	7- 4- 86
A1A1A2A1C62	7- 4- 71	A1A1A2A1L21	7- 4- 7	A1A1A2A1L7	7- 4- 7
A1A1A2A1C63	7- 4- 73	A1A1A2A1L22	7- 4- 50	A1A1A2A1L70	7- 4- 89
A1A1A2A1C64	7- 4- 93	A1A1A2A1L23	7- 4- 18	A1A1A2A1L71	7- 4- 84
A1A1A2A1C65	7- 4- 92	A1A1A2A1L24	7- 4- 38	A1A1A2A1L72	7- 4- 84
A1A1A2A1C66	7- 4- 66	A1A1A2A1L25	7- 4- 49	A1A1A2A1L73	7- 4- 88
A1A1A2A1C67	7- 4- 85	A1A1A2A1L26	7- 4- 81	A1A1A2A1L74	7- 4- 55
A1A1A2A1C68	7- 4- 87	A1A1A2A1L27	7- 4- 11	A1A1A2A1L75	7- 4- 61
A1A1A2A1C69	7- 4- 87	A1A1A2A1L28	7- 4- 11	A1A1A2A1L76	7- 4- 61
A1A1A2A1C7	7- 4- 36	A1A1A2A1L29	7- 4- 11	A1A1A2A1L77	7- 4- 45
A1A1A2A1C70	7- 4- 8	A1A1A2A1L3	7- 4- 40	A1A1A2A1L79	7- 4- 60
A1A1A2A1C71	7- 4- 8	A1A1A2A1L30	7- 4- 55	A1A1A2A1L8	7- 4- 2
A1A1A2A1C72	7- 4- 10	A1A1A2A1L31	7- 4- 55	A1A1A2A1L80	7- 4- 60
A1A1A2A1C73	7- 4- 8	A1A1A2A1L32	7- 4- 11	A1A1A2A1L81	7- 4- 50
A1A1A2A1C74	7- 4- 8	A1A1A2A1L33	7- 4- 42	A1A1A2A1L82	7- 4- 49
A1A1A2A1C75	7- 4- 10	A1A1A2A1L34	7- 4- 55	A1A1A2A1L83	7- 4- 83
A1A1A2A1C76	7- 4- 10	A1A1A2A1L35	7- 4- 55	A1A1A2A1L84	7- 4- 81
A1A1A2A1C77	7- 4- 8	A1A1A2A1L36	7- 4- 14	A1A1A2A1L9	7- 4- 2
A1A1A2A1C78	7- 4- 8	A1A1A2A1L37	7- 4- 55	A1A1A2A1Q2	7- 4- 24
A1A1A2A1C79	7- 4- 8	A1A1A2A1L38	7- 4- 55	A1A1A2A1Q5	7- 4- 53
A1A1A2A1C8	7- 4- 10	A1A1A2A1L39	7- 4- 11	A1A1A2A1Q6	7- 4- 53
A1A1A2A1C80	7- 4- 16	A1A1A2A1L4	7- 4- 38	A1A1A2A1Q7	7- 4- 24
A1A1A2A1C81	7- 4- 10	A1A1A2A1L40	7- 4- 11	A1A1A2A1RT1	7- 4- 51
A1A1A2A1C82	7- 4- 16	A1A1A2A1L41	7- 4- 55	A1A1A2A1R1	7- 4- 35
A1A1A2A1C9	7- 4- 8	A1A1A2A1L47	7- 4- 55	A1A1A2A1R10	7- 4- 41
A1A1A2A1C92	7- 4- 30	A1A1A2A1L48	7- 4- 45	A1A1A2A1R11	7- 4- 20
A1A1A2A1C93	7- 4- 48	A1A1A2A1L5	7- 4- 21	A1A1A2A1R12	7- 4- 15
A1A1A2A1C94	7- 4- 16	A1A1A2A1L50	7- 4- 78	A1A1A2A1R13	7- 4- 43
A1A1A2A1C95	7- 4- 39	A1A1A2A1L51	7- 4- 78	A1A1A2A1R14	7- 4- 43
A1A1A2A1C96	7- 4- 76	A1A1A2A1L52	7- 4- 37	A1A1A2A1R15	7- 4- 41
A1A1A2A1C97	7- 4- 8	A1A1A2A1L53	7- 4- 78	A1A1A2A1R16	7- 4- 41
A1A1A2A1J1	7- 4- 28	A1A1A2A1L54	7- 4- 78	A1A1A2A1R17	7- 4- 57
A1A1A2A1J4	7- 4- 77	A1A1A2A1L57	7- 4- 69	A1A1A2A1R18	7- 4- 74

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A1A1A2A1R19	7- 4- 74	A1A1A3A1	7-13-REF	A1A1A3A1C23	7-13-120
A1A1A2A1R2	7- 4- 32	A1A1A3A1CR1	7-13- 5	A1A1A3A1C24	7-13-120
A1A1A2A1R20	7- 4- 75	A1A1A3A1CR10	7-13- 5	A1A1A3A1C25	7-13-120
A1A1A2A1R21	7- 4- 43	A1A1A3A1CR11	7-13- 5	A1A1A3A1C3	7-13- 28
A1A1A2A1R22	7- 4- 65	A1A1A3A1CR13	7-13- 5	A1A1A3A1C31	7-13- 62
A1A1A2A1R23	7- 4- 91	A1A1A3A1CR14	7-13- 5	A1A1A3A1C32	7-13- 58
A1A1A2A1R24	7- 4- 90	A1A1A3A1CR15	7-13- 5	A1A1A3A1C33	7-13- 55
A1A1A2A1R25	7- 4- 43	A1A1A3A1CR16	7-13- 5	A1A1A3A1C34	7-13- 63
A1A1A2A1R26	7- 4- 65	A1A1A3A1CR17	7-13- 5	A1A1A3A1C35	7-13- 10
A1A1A2A1R27	7- 4- 91	A1A1A3A1CR2	7-13- 5	A1A1A3A1C36	7-13- 10
A1A1A2A1R28	7- 4- 90	A1A1A3A1CR20	7-13- 5	A1A1A3A1C37	7-13- 62
A1A1A2A1R3	7- 4- 33	A1A1A3A1CR21	7-13- 5	A1A1A3A1C38	7-13- 16
A1A1A2A1R36	7- 4- 25	A1A1A3A1CR22	7-13- 5	A1A1A3A1C39	7-13- 43
A1A1A2A1R37	7- 4- 54	A1A1A3A1CR23	7-13- 5	A1A1A3A1C4	7-13- 93
A1A1A2A1R38	7- 4- 54	A1A1A3A1CR24	7-13- 5	A1A1A3A1C41	7-13- 10
A1A1A2A1R39	7- 4- 56	A1A1A3A1CR27	7-13- 5	A1A1A3A1C42	7-13- 10
A1A1A2A1R4	7- 4- 17	A1A1A3A1CR28	7-13- 5	A1A1A3A1C43	7-13- 43
A1A1A2A1R40	7- 4- 54	A1A1A3A1CR3	7-13- 5	A1A1A3A1C44	7-13- 19
A1A1A2A1R41	7- 4- 52	A1A1A3A1CR31	7-13- 5	A1A1A3A1C49	7-13- 46
A1A1A2A1R42	7- 4- 52A	A1A1A3A1CR32	7-13- 5	A1A1A3A1C5	7-13- 88
A1A1A2A1R43	7- 4- 79	A1A1A3A1CR33	7-13- 5	A1A1A3A1C50	7-13- 64
A1A1A2A1R44	7- 4- 35	A1A1A3A1CR34	7-13- 5	A1A1A3A1C51	7-13- 33
A1A1A2A1R45	7- 4- 57	A1A1A3A1CR35	7-13- 5	A1A1A3A1C52	7-13- 10
A1A1A2A1R46	7- 4- 90	A1A1A3A1CR36	7-13- 5	A1A1A3A1C53	7-13- 12
A1A1A2A1R47	7- 4- 90	A1A1A3A1CR4	7-13- 5	A1A1A3A1C54	7-13- 21
A1A1A2A1R5	7- 4- 22	A1A1A3A1CR5	7-13- 5	A1A1A3A1C55	7-13- 47
A1A1A2A1R6	7- 4- 17	A1A1A3A1CR6	7-13-134	A1A1A3A1C56	7-13- 30
A1A1A2A1R7	7- 4- 25	A1A1A3A1CR7	7-13-134	A1A1A3A1C57	7-13- 45
A1A1A2A1R8	7- 4- 26	A1A1A3A1CR8	7-13-134	A1A1A3A1C58	7-13- 30
A1A1A2A1R9	7- 4- 57	A1A1A3A1CR9	7-13- 5	A1A1A3A1C59	7-13- 33
A1A1A2A1T1	7- 4- 29	A1A1A3A1C1	7-13- 62	A1A1A3A1C6	7-13- 62
A1A1A2A1T2	7- 4- 29	A1A1A3A1C10	7-13-120	A1A1A3A1C60	7-13- 30
A1A1A2A1T3	7- 4- 44	A1A1A3A1C11	7-13-120	A1A1A3A1C61	7-13- 10
A1A1A2A1T4	7- 4- 46	A1A1A3A1C12	7-13-120	A1A1A3A1C62	7-13- 30
A1A1A2C14	7- 3- 1	A1A1A3A1C13	7-13-120	A1A1A3A1C68	7-13- 12
A1A1A2C15	7- 3- 1	A1A1A3A1C14	7-13-124	A1A1A3A1C69	7-13- 12
A1A1A2C3	7- 3- 30	A1A1A3A1C15	7-13-135	A1A1A3A1C7	7-13- 62
A1A1A2C38	7- 3- 5	A1A1A3A1C16	7-13-129	A1A1A3A1C70	7-13- 81
A1A1A2C4	7- 3- 31	A1A1A3A1C17	7-13-130	A1A1A3A1C71	7-13- 86
A1A1A2Q1	7- 3- 29	A1A1A3A1C18	7-13-129	A1A1A3A1C77	7-13- 62
A1A1A2Q3	7- 3- 2	A1A1A3A1C19	7-13-129	A1A1A3A1C78	7-13- 62
A1A1A2Q4	7- 3- 6	A1A1A3A1C2	7-13- 62	A1A1A3A1C79	7-13- 62
A1A1A3	7- 2- 5	A1A1A3A1C20	7-13-120	A1A1A3A1C8	7-13- 19
A1A1A3	7-12-REF	A1A1A3A1C21	7-13-120	A1A1A3A1C80	7-13- 16
A1A1A3A1	7-12- 1	A1A1A3A1C22	7-13-120	A1A1A3A1C81	7-13-103

REFERENCE DESIGNATION	FIGURE AND INDEX NUMBER	REFERENCE DESIGNATION	FIGURE AND INDEX NUMBER	REFERENCE DESIGNATION	FIGURE AND INDEX NUMBER
A1A1A3A1C82	7-13- 88	A1A1A3A1Q8	7-13- 25	A1A1A3A1R139	7-13- 1
A1A1A3A1C83	7-13-103	A1A1A3A1Q9	7-13-127	A1A1A3A1R14	7-13- 60
A1A1A3A1C84	7-13- 88	A1A1A3A1R1	7-13- 78	A1A1A3A1R140	7-13- 32
A1A1A3A1C85	7-13-103	A1A1A3A1R10	7-13- 94	A1A1A3A1R141	7-13- 8
A1A1A3A1C86	7-13-103	A1A1A3A1R100	7-13- 68	A1A1A3A1R142	7-13- 79
A1A1A3A1C87	7-13- 88	A1A1A3A1R101	7-13- 35	A1A1A3A1R143	7-13- 80
A1A1A3A1C88	7-13-103	A1A1A3A1R102	7-13- 54	A1A1A3A1R144	7-13- 8
A1A1A3A1C89	7-13-103	A1A1A3A1R103	7-13- 57	A1A1A3A1R145	7-13- 17
A1A1A3A1C9	7-13- 62	A1A1A3A1R104	7-13- 35	A1A1A3A1R15	7-13- 92
A1A1A3A1C90	7-13- 62A	A1A1A3A1R105	7-13- 57	A1A1A3A1R156	7-13- 82
A1A1A3A1C91	7-13- 88	A1A1A3A1R106	7-13- 66	A1A1A3A1R157	7-13- 82
A1A1A3A1E1	7-13-117	A1A1A3A1R107	7-13- 9	A1A1A3A1R158	7-13- 82
A1A1A3A1J1	7-13-119	A1A1A3A1R108	7-13- 18	A1A1A3A1R159	7-13- 82
A1A1A3A1J2	7-13-119	A1A1A3A1R109	7-13- 9	A1A1A3A1R160	7-13- 82
A1A1A3A1J3	7-13-138	A1A1A3A1R11	7-13- 1	A1A1A3A1R161	7-13- 82
A1A1A3A1J4	7-13- 72	A1A1A3A1R110	7-13- 8	A1A1A3A1R162	7-13- 2
A1A1A3A1L1	7-13-123	A1A1A3A1R111	7-13- 8	A1A1A3A1R163	7-13- 2
A1A1A3A1L10	7-13-106	A1A1A3A1R112	7-13- 8	A1A1A3A1R164	7-13- 3
A1A1A3A1L11	7-13-106	A1A1A3A1R113	7-13- 26	A1A1A3A1R165	7-13- 3
A1A1A3A1L12	7-13-101	A1A1A3A1R114	7-13- 8	A1A1A3A1R166	7-13- 90
A1A1A3A1L13	7-13-101	A1A1A3A1R115	7-13- 77	A1A1A3A1R167	7-13- 87
A1A1A3A1L14	7-13-101	A1A1A3A1R116	7-13- 11	A1A1A3A1R168	7-13- 89
A1A1A3A1L15	7-13-139	A1A1A3A1R117	7-13- 15	A1A1A3A1R169	7-13- 50
A1A1A3A1L16	7-13-101	A1A1A3A1R118	7-13- 14	A1A1A3A1R17	7-13- 8
A1A1A3A1L2	7-13-123	A1A1A3A1R119	7-13- 48	A1A1A3A1R170	7-13- 87
A1A1A3A1L3	7-13-136	A1A1A3A1R12	7-13- 91	A1A1A3A1R171	7-13- 89
A1A1A3A1L4	7-13-133	A1A1A3A1R120	7-13- 48	A1A1A3A1R172	7-13- 14
A1A1A3A1L5	7-13-133	A1A1A3A1R121	7-13- 36	A1A1A3A1R173	7-13- 85
A1A1A3A1L6	7-13-132	A1A1A3A1R122	7-13- 48	A1A1A3A1R174	7-13- 40
A1A1A3A1L7	7-13-136	A1A1A3A1R123	7-13- 8	A1A1A3A1R18	7-13- 8
A1A1A3A1L8	7-13-128	A1A1A3A1R124	7-13- 8	A1A1A3A1R184	7-13-113
A1A1A3A1L9	7-13-136	A1A1A3A1R125	7-13- 44	A1A1A3A1R185	7-13- 82
A1A1A3A1Q1	7-13- 70	A1A1A3A1R126	7-13- 44	A1A1A3A1R186	7-13- 31
A1A1A3A1Q10	7-13- 25	A1A1A3A1R128	7-13- 44	A1A1A3A1R187	7-13-114
A1A1A3A1Q11	7-13- 97	A1A1A3A1R129	7-13- 34	A1A1A3A1R188	7-13-100
A1A1A3A1Q12	7-13- 97	A1A1A3A1R13	7-13- 94	A1A1A3A1R189	7-13- 60
A1A1A3A1Q13	7-13- 97	A1A1A3A1R130	7-13- 34	A1A1A3A1R19	7-13- 15
A1A1A3A1Q14	7-13- 70	A1A1A3A1R131	7-13- 35	A1A1A3A1R190	7-13-113
A1A1A3A1Q15	7-13- 25	A1A1A3A1R132	7-13- 34	A1A1A3A1R191	7-13- 82
A1A1A3A1Q2	7-13- 25	A1A1A3A1R133	7-13- 39	A1A1A3A1R192	7-13- 31
A1A1A3A1Q3	7-13- 70	A1A1A3A1R134	7-13- 39	A1A1A3A1R193	7-13-114
A1A1A3A1Q4	7-13- 25	A1A1A3A1R135	7-13- 37	A1A1A3A1R194	7-13-100
A1A1A3A1Q5	7-13- 70	A1A1A3A1R136	7-13- 39	A1A1A3A1R195	7-13- 99
A1A1A3A1Q6	7-13- 25	A1A1A3A1R137	7-13- 26	A1A1A3A1R196	7-13-140
A1A1A3A1Q7	7-13- 70	A1A1A3A1R138	7-13- 7	A1A1A3A1R197	7-13- 98

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A1A1A3A1R198	7-13- 44	A1A1A3A1R4	7-13-109	A1A1A3A1R89	7-13- 40
A1A1A3A1R199	7-13-113	A1A1A3A1R49	7-13-102	A1A1A3A1R9	7-13- 24
A1A1A3A1R2	7-13- 84	A1A1A3A1R5	7-13-111	A1A1A3A1R96	7-13- 69
A1A1A3A1R20	7-13- 32	A1A1A3A1R50	7-13-107	A1A1A3A1R98	7-13- 49
A1A1A3A1R200	7-13- 82	A1A1A3A1R51	7-13- 52	A1A1A3A1R99	7-13- 49
A1A1A3A1R201	7-13- 31	A1A1A3A1R52	7-13- 8	A1A1A3A1T1	7-13-131
A1A1A3A1R202	7-13-114	A1A1A3A1R53	7-13- 57	A1A1A3A1U1	7-13- 61
A1A1A3A1R203	7-13-100	A1A1A3A1R54	7-13- 8	A1A1A3A1U10	7-13- 6
A1A1A3A1R204	7-13- 60	A1A1A3A1R55	7-13- 77	A1A1A3A1U11	7-13- 76
A1A1A3A1R205	7-13- 75	A1A1A3A1R56	7-13- 60	A1A1A3A1U12	7-13- 76
A1A1A3A1R206	7-13- 3	A1A1A3A1R57	7-13- 50	A1A1A3A1U14	7-13- 96
A1A1A3A1R207	7-13-113	A1A1A3A1R58	7-13- 49	A1A1A3A1U15	7-13- 73A
A1A1A3A1R208	7-13-113	A1A1A3A1R59	7-13- 49	A1A1A3A1U2	7-13- 73
A1A1A3A1R209	7-13- 3	A1A1A3A1R6	7-13- 83	A1A1A3A1U4	7-13- 6
A1A1A3A1R21	7-13- 8	A1A1A3A1R60	7-13- 52A	A1A1A3A1U5	7-13- 6
A1A1A3A1R210	7-13- 35	A1A1A3A1R61	7-13- 53	A1A1A3A1U6	7-13- 73
A1A1A3A1R211	7-13- 74	A1A1A3A1R62	7-13- 59	A1A1A3A1U7	7-13- 6
A1A1A3A1R212	7-13- 35	A1A1A3A1R63	7-13- 60	A1A1A3A1U8	7-13- 42
A1A1A3A1R213	7-13-113A	A1A1A3A1R64	7-13- 51	A1A1A3A1U9	7-13- 42
A1A1A3A1R214	7-13- 48	A1A1A3A1R65	7-13- 8	A1A1A3A1VR1	7-13-110
A1A1A3A1R215	7-13-112	A1A1A3A1R66	7-13- 56	A1A1A3A1VR11	7-13- 67
A1A1A3A1R216	7-13- 14	A1A1A3A1R67	7-13- 24	A1A1A3A1VR2	7-13-137
A1A1A3A1R217	7-13- 82	A1A1A3A1R68	7-13- 26	A1A1A3A1VR5	7-13- 20
A1A1A3A1R218	7-13-113	A1A1A3A1R69	7-13- 31	A1A1A3A1VR6	7-13- 20
A1A1A3A1R219	7-13-113	A1A1A3A1R7	7-13- 95	A1A1A3A1VR7	7-13- 23
A1A1A3A1R22	7-13- 77	A1A1A3A1R70	7-13- 11	A1A1A3A1VR8	7-13- 23
A1A1A3A1R220	7-13- 8	A1A1A3A1R71	7-13- 27	A1A1A3A1Z1	7-13-104
A1A1A3A1R221	7-13- 8	A1A1A3A1R72	7-13- 38	A1A1A4	7- 2- 4
A1A1A3A1R23	7-13- 82	A1A1A3A1R73	7-13- 29	A1A1A4	7-10-REF
A1A1A3A1R24	7-13- 8	A1A1A3A1R74	7-13- 17	A1A1A4A1	7-10- 9
A1A1A3A1R25	7-13- 82	A1A1A3A1R75	7-13- 4	A1A1A4A1	7-11-REF
A1A1A3A1R26	7-13-122	A1A1A3A1R76	7-13- 4	A1A1A4A1CR1	7-11- 2
A1A1A3A1R27	7-13-125	A1A1A3A1R77	7-13- 22	A1A1A4A1CR10	7-11- 8
A1A1A3A1R28	7-13- 54	A1A1A3A1R78	7-13- 18	A1A1A4A1CR11	7-11- 8
A1A1A3A1R29	7-13-121	A1A1A3A1R79	7-13- 13	A1A1A4A1CR12	7-11- 8
A1A1A3A1R3	7-13- 91	A1A1A3A1R8	7-13- 35	A1A1A4A1CR13	7-11- 8
A1A1A3A1R30	7-13-126	A1A1A3A1R80	7-13- 13	A1A1A4A1CR14	7-11- 27
A1A1A3A1R31	7-13-126	A1A1A3A1R81	7-13- 11	A1A1A4A1CR15	7-11- 27
A1A1A3A1R32	7-13-126	A1A1A3A1R82	7-13- 3	A1A1A4A1CR16	7-11- 27
A1A1A3A1R33	7-13-126	A1A1A3A1R83	7-13- 2	A1A1A4A1CR17	7-11- 27
A1A1A3A1R34	7-13-107	A1A1A3A1R84	7-13- 2	A1A1A4A1CR18	7-11- 27
A1A1A3A1R35	7-13-121	A1A1A3A1R85	7-13- 3	A1A1A4A1CR19	7-11- 27
A1A1A3A1R36	7-13- 54	A1A1A3A1R86	7-13- 54	A1A1A4A1CR2	7-11- 2
A1A1A3A1R37	7-13- 8	A1A1A3A1R87	7-13- 41	A1A1A4A1CR20	7-11- 27
A1A1A3A1R38	7-13-107	A1A1A3A1R88	7-13- 8	A1A1A4A1CR21	7-11- 27

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A1A1A4A1CR22	7-11- 27	A1A1A4A1C105	7-11- 19	A1A1A4A1C23	7-11- 5
A1A1A4A1CR23	7-11- 27	A1A1A4A1C106	7-11- 90	A1A1A4A1C24	7-11- 11
A1A1A4A1CR24	7-11- 27	A1A1A4A1C107	7-11- 19	A1A1A4A1C25	7-11- 30
A1A1A4A1CR25	7-11- 27	A1A1A4A1C108	7-11- 19	A1A1A4A1C26	7-11- 19
A1A1A4A1CR26	7-11- 27	A1A1A4A1C109	7-11- 65	A1A1A4A1C27	7-11- 30
A1A1A4A1CR27	7-11- 27	A1A1A4A1C11	7-11- 30	A1A1A4A1C28	7-11- 5
A1A1A4A1CR28	7-11- 27	A1A1A4A1C110	7-11- 19	A1A1A4A1C29	7-11- 10
A1A1A4A1CR29	7-11- 27	A1A1A4A1C111	7-11- 90	A1A1A4A1C3	7-11- 10
A1A1A4A1CR3	7-11- 8	A1A1A4A1C112	7-11- 19	A1A1A4A1C30	7-11- 5
A1A1A4A1CR30	7-11- 27	A1A1A4A1C113	7-11- 89	A1A1A4A1C31	7-11- 5
A1A1A4A1CR31	7-11- 27	A1A1A4A1C115	7-11- 90	A1A1A4A1C32	7-11- 11
A1A1A4A1CR32	7-11- 27	A1A1A4A1C116	7-11- 19	A1A1A4A1C33	7-11- 30
A1A1A4A1CR33	7-11- 27	A1A1A4A1C117	7-11- 19	A1A1A4A1C34	7-11- 19
A1A1A4A1CR34	7-11- 2	A1A1A4A1C118	7-11- 90	A1A1A4A1C35	7-11- 41
A1A1A4A1CR35	7-11- 2	A1A1A4A1C119	7-11- 90	A1A1A4A1C36	7-11- 19
A1A1A4A1CR4	7-11- 8	A1A1A4A1C12	7-11- 41	A1A1A4A1C37	7-11-143
A1A1A4A1CR40	7-11- 31	A1A1A4A1C120	7-11- 19	A1A1A4A1C38	7-11- 49
A1A1A4A1CR41	7-11- 31	A1A1A4A1C121	7-11- 11	A1A1A4A1C39	7-11-144
A1A1A4A1CR43	7-11- 83	A1A1A4A1C122	7-11- 41	A1A1A4A1C4	7-11- 5
A1A1A4A1CR44	7-11- 31	A1A1A4A1C123	7-11- 90	A1A1A4A1C40	7-11- 11
A1A1A4A1CR45	7-11- 31	A1A1A4A1C124	7-11- 19	A1A1A4A1C41	7-11- 30
A1A1A4A1CR47	7-11- 31	A1A1A4A1C125	7-11- 19	A1A1A4A1C42	7-11- 19
A1A1A4A1CR5	7-11- 8	A1A1A4A1C128	7-11-120	A1A1A4A1C43	7-11- 30
A1A1A4A1CR51	7-11- 31	A1A1A4A1C13	7-11- 19	A1A1A4A1C44	7-11- 5
A1A1A4A1CR52	7-11- 31	A1A1A4A1C132	7-11- 19	A1A1A4A1C45	7-11- 51
A1A1A4A1CR53	7-11- 60	A1A1A4A1C133	7-11- 19	A1A1A4A1C46	7-11- 50
A1A1A4A1CR54	7-11- 60	A1A1A4A1C134	7-11- 90	A1A1A4A1C47	7-11- 50
A1A1A4A1CR55	7-11- 60	A1A1A4A1C135	7-11-103	A1A1A4A1C48	7-11- 53
A1A1A4A1CR56	7-11- 8	A1A1A4A1C136	7-11-120	A1A1A4A1C49	7-11- 5
A1A1A4A1CR57	7-11- 31	A1A1A4A1C137	7-11- 89	A1A1A4A1C5	7-11- 11
A1A1A4A1CR58	7-11- 31	A1A1A4A1C14	7-11- 41	A1A1A4A1C50	7-11- 30
A1A1A4A1CR59	7-11- 31	A1A1A4A1C140	7-11- 90	A1A1A4A1C51	7-11- 10
A1A1A4A1CR6	7-11- 8	A1A1A4A1C142	7-11- 90	A1A1A4A1C52	7-11- 55
A1A1A4A1CR60	7-11- 31	A1A1A4A1C144	7-11- 7	A1A1A4A1C53	7-11- 55
A1A1A4A1CR64	7-11- 31	A1A1A4A1C145	7-11- 7	A1A1A4A1C54	7-11- 55
A1A1A4A1CR65	7-11- 31	A1A1A4A1C146	7-11- 44	A1A1A4A1C55	7-11- 55
A1A1A4A1CR66	7-11- 31	A1A1A4A1C15	7-11- 19	A1A1A4A1C56	7-11- 72
A1A1A4A1CR67	7-11- 31	A1A1A4A1C16	7-11- 19	A1A1A4A1C57	7-11- 55
A1A1A4A1CR7	7-11- 8	A1A1A4A1C17	7-11- 13	A1A1A4A1C58	7-11- 50
A1A1A4A1CR8	7-11- 8	A1A1A4A1C18	7-11- 13	A1A1A4A1C6	7-11- 10
A1A1A4A1CR9	7-11- 8	A1A1A4A1C19	7-11- 10	A1A1A4A1C64	7-11- 55
A1A1A4A1C1	7-11-143	A1A1A4A1C2	7-11- 30	A1A1A4A1C65	7-11- 55
A1A1A4A1C10	7-11- 30	A1A1A4A1C20	7-11- 10	A1A1A4A1C66	7-11-107
A1A1A4A1C100	7-11-101	A1A1A4A1C21	7-11- 19	A1A1A4A1C67	7-11- 90
A1A1A4A1C104	7-11- 10	A1A1A4A1C22	7-11- 11	A1A1A4A1C68	7-11-129

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A1A1A4A1C69	7-11- 90	A1A1A4A1L21	7-11- 47	A1A1A4A1R102	7-11- 59
A1A1A4A1C7	7-11- 10	A1A1A4A1L22	7-11- 46	A1A1A4A1R103	7-11- 59
A1A1A4A1C70	7-11- 97	A1A1A4A1L25	7-11-111	A1A1A4A1R104	7-11- 38
A1A1A4A1C71	7-11- 98	A1A1A4A1L27	7-11-119	A1A1A4A1R105	7-11- 38
A1A1A4A1C72	7-11- 10	A1A1A4A1L28	7-11-102	A1A1A4A1R106	7-11- 85
A1A1A4A1C73	7-11-123	A1A1A4A1L29	7-11-108	A1A1A4A1R107	7-11- 91
A1A1A4A1C74	7-11-101	A1A1A4A1L3	7-11- 3A	A1A1A4A1R108	7-11- 92
A1A1A4A1C75	7-11-122	A1A1A4A1L30	7-11- 74	A1A1A4A1R109	7-11- 93
A1A1A4A1C77	7-11-127	A1A1A4A1L31	7-11- 74	A1A1A4A1R11	7-11- 9
A1A1A4A1C78	7-11- 55	A1A1A4A1L32	7-11- 74	A1A1A4A1R110	7-11- 67
A1A1A4A1C79	7-11-114	A1A1A4A1L33	7-11- 74	A1A1A4A1R111	7-11- 48
A1A1A4A1C8	7-11- 10	A1A1A4A1L34	7-11- 74	A1A1A4A1R112	7-11- 38
A1A1A4A1C80	7-11-113	A1A1A4A1L35	7-11- 74	A1A1A4A1R114	7-11- 37
A1A1A4A1C81	7-11-107	A1A1A4A1L36	7-11-108	A1A1A4A1R115	7-11- 94
A1A1A4A1C82	7-11- 90	A1A1A4A1L37	7-11- 24	A1A1A4A1R116	7-11- 94
A1A1A4A1C83	7-11- 55	A1A1A4A1L38	7-11- 24	A1A1A4A1R117	7-11-118
A1A1A4A1C84	7-11-117	A1A1A4A1L39	7-11- 74	A1A1A4A1R118	7-11- 88
A1A1A4A1C85	7-11- 90	A1A1A4A1L4	7-11- 4	A1A1A4A1R119	7-11- 38
A1A1A4A1C86	7-11- 90	A1A1A4A1L40	7-11- 24	A1A1A4A1R12	7-11- 14
A1A1A4A1C87	7-11- 90	A1A1A4A1L41	7-11- 24	A1A1A4A1R121	7-11- 38
A1A1A4A1C88	7-11- 90	A1A1A4A1L42	7-11- 43	A1A1A4A1R122	7-11- 84
A1A1A4A1C89	7-11- 90	A1A1A4A1L43	7-11- 24	A1A1A4A1R123	7-11-126
A1A1A4A1C9	7-11- 5	A1A1A4A1L44	7-11- 24	A1A1A4A1R124	7-11-130
A1A1A4A1C90	7-11-116	A1A1A4A1L5	7-11- 3	A1A1A4A1R125	7-11- 37
A1A1A4A1C91	7-11- 49	A1A1A4A1L6	7-11- 23	A1A1A4A1R126	7-11-104
A1A1A4A1C92	7-11- 50	A1A1A4A1L7	7-11- 3	A1A1A4A1R127	7-11-125
A1A1A4A1C93	7-11- 98	A1A1A4A1L8	7-11- 28	A1A1A4A1R128	7-11- 34A
A1A1A4A1C94	7-11- 55	A1A1A4A1L9	7-11- 39	A1A1A4A1R129	7-11- 34A
A1A1A4A1C95	7-11- 51	A1A1A4A1Q1	7-11- 16	A1A1A4A1R13	7-11- 42
A1A1A4A1C96	7-11- 55	A1A1A4A1Q10	7-11- 40	A1A1A4A1R130	7-11- 88
A1A1A4A1FL1	7-11- 81	A1A1A4A1Q11	7-11- 40	A1A1A4A1R131	7-11- 88
A1A1A4A1J1	7-11- 35	A1A1A4A1Q2	7-11- 16	A1A1A4A1R132	7-11- 84
A1A1A4A1J2	7-11- 35	A1A1A4A1Q3	7-11- 16	A1A1A4A1R133	7-11-125
A1A1A4A1J3	7-11- 95	A1A1A4A1Q4	7-11- 73	A1A1A4A1R14	7-11- 12
A1A1A4A1L10	7-11- 23	A1A1A4A1Q7	7-11- 32	A1A1A4A1R15	7-11- 15
A1A1A4A1L11	7-11- 29	A1A1A4A1Q8	7-11- 32	A1A1A4A1R16	7-11- 22
A1A1A4A1L12	7-11- 3	A1A1A4A1RT1	7-11- 20	A1A1A4A1R17	7-11- 21
A1A1A4A1L13	7-11- 28	A1A1A4A1RT2	7-11- 20	A1A1A4A1R18	7-11- 25
A1A1A4A1L14	7-11- 39	A1A1A4A1RT3	7-11- 20	A1A1A4A1R19	7-11- 9
A1A1A4A1L15	7-11- 28	A1A1A4A1RT4	7-11- 20	A1A1A4A1R2	7-11- 9
A1A1A4A1L16	7-11- 71	A1A1A4A1RT5	7-11-128	A1A1A4A1R20	7-11- 14
A1A1A4A1L17	7-11- 70	A1A1A4A1R1	7-11- 37	A1A1A4A1R21	7-11- 42
A1A1A4A1L18	7-11- 39	A1A1A4A1R10	7-11- 9	A1A1A4A1R22	7-11- 12
A1A1A4A1L19	7-11- 39	A1A1A4A1R100	7-11- 96	A1A1A4A1R23	7-11- 15
A1A1A4A1L20	7-11- 46	A1A1A4A1R101	7-11- 59	A1A1A4A1R24	7-11- 22

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A1A1A4A1R25	7-11- 21	A1A1A4A1R71	7-11-133	A1A1A5A1	7- 6- 1
A1A1A4A1R26	7-11- 25	A1A1A4A1R72	7-11-130	A1A1A5A1	7- 7-REF
A1A1A4A1R27	7-11- 9	A1A1A4A1R73	7-11-136	A1A1A5A1CR10	7- 7- 80
A1A1A4A1R28	7-11- 48	A1A1A4A1R76	7-11- 57	A1A1A5A1CR14	7- 7- 80
A1A1A4A1R29	7-11- 52	A1A1A4A1R77	7-11- 58	A1A1A5A1CR15	7- 7- 80
A1A1A4A1R3	7-11- 42	A1A1A4A1R8	7-11- 22	A1A1A5A1CR16	7- 7- 80
A1A1A4A1R30	7-11- 37	A1A1A4A1R84	7-11- 67	A1A1A5A1CR17	7- 7- 80
A1A1A4A1R31	7-11- 56A	A1A1A4A1R85	7-11- 36	A1A1A5A1CR18	7- 7- 80
A1A1A4A1R32	7-11- 54	A1A1A4A1R86	7-11- 33	A1A1A5A1CR19	7- 7- 80
A1A1A4A1R33	7-11- 54	A1A1A4A1R87	7-11- 37	A1A1A5A1CR20	7- 7-119
A1A1A4A1R34	7-11- 54	A1A1A4A1R88	7-11- 33	A1A1A5A1CR3	7- 7- 80
A1A1A4A1R35	7-11- 59	A1A1A4A1R89	7-11- 62	A1A1A5A1CR4	7- 7- 80
A1A1A4A1R36	7-11- 75	A1A1A4A1R9	7-11- 21	A1A1A5A1CR5	7- 7- 80
A1A1A4A1R38	7-11- 67	A1A1A4A1R90	7-11- 61	A1A1A5A1CR6	7- 7-119
A1A1A4A1R4	7-11- 12	A1A1A4A1R91	7-11- 64	A1A1A5A1CR7	7- 7- 80
A1A1A4A1R41	7-11- 48	A1A1A4A1R92	7-11- 64A	A1A1A5A1CR8	7- 7- 80
A1A1A4A1R42	7-11-106	A1A1A4A1R93	7-11- 63	A1A1A5A1CR9	7- 7- 80
A1A1A4A1R44	7-11-115	A1A1A4A1R94	7-11- 66	A1A1A5A1C10	7- 7- 25
A1A1A4A1R45	7-11- 37	A1A1A4A1R96	7-11- 87	A1A1A5A1C100	7- 7- 26
A1A1A4A1R46	7-11-121	A1A1A4A1R97	7-11- 87	A1A1A5A1C101	7- 7- 26
A1A1A4A1R48	7-11-124	A1A1A4A1R98	7-11- 86	A1A1A5A1C102	7- 7- 26
A1A1A4A1R49	7-11- 38	A1A1A4A1R99	7-11- 82	A1A1A5A1C103	7- 7- 26
A1A1A4A1R5	7-11- 15	A1A1A4A1TP1	7-11- 79	A1A1A5A1C105	7- 7- 49
A1A1A4A1R50	7-11-106	A1A1A4A1TP10	7-11- 79	A1A1A5A1C107	7- 7- 57
A1A1A4A1R51	7-11-115	A1A1A4A1TP2	7-11- 79	A1A1A5A1C108	7- 7- 62
A1A1A4A1R52	7-11-115	A1A1A4A1TP3	7-11- 79	A1A1A5A1C11	7- 7- 3
A1A1A4A1R53	7-11- 38	A1A1A4A1TP4	7-11- 79	A1A1A5A1C110	7- 7- 57
A1A1A4A1R54	7-11- 34	A1A1A4A1TP5	7-11- 79	A1A1A5A1C111	7- 7-134
A1A1A4A1R55	7-11- 88	A1A1A4A1TP6	7-11-137	A1A1A5A1C112	7- 7- 66
A1A1A4A1R56	7-11- 80	A1A1A4A1TP8	7-11- 79	A1A1A5A1C12	7- 7- 30
A1A1A4A1R57	7-11- 99	A1A1A4A1TP9	7-11- 79	A1A1A5A1C14	7- 7- 31
A1A1A4A1R58	7-11- 88	A1A1A4A1T1	7-11- 56	A1A1A5A1C15	7- 7- 32
A1A1A4A1R59	7-11- 94	A1A1A4A1T2	7-11- 76	A1A1A5A1C16	7- 7- 31
A1A1A4A1R6	7-11- 14	A1A1A4A1U1	7-11- 68	A1A1A5A1C20	7- 7- 54
A1A1A4A1R60	7-11- 37	A1A1A4A1U2	7-11-112	A1A1A5A1C21	7- 7- 42
A1A1A4A1R61	7-11- 37	A1A1A4A1U3	7-11-105	A1A1A5A1C22	7- 7- 46
A1A1A4A1R63	7-11- 77	A1A1A4A1U4	7-11- 78	A1A1A5A1C24	7- 7- 8
A1A1A4A1R64	7-11- 80	A1A1A4A1U5	7-11- 78	A1A1A5A1C25	7- 7- 3
A1A1A4A1R65	7-11-132	A1A1A4A1U6	7-11-131	A1A1A5A1C26	7- 7- 4
A1A1A4A1R66	7-11-100	A1A1A4A1U7	7-11- 69	A1A1A5A1C27	7- 7- 49
A1A1A4A1R67	7-11-118	A1A1A4A1Y1	7-11-109	A1A1A5A1C28	7- 7- 55
A1A1A4A1R68	7-11-134	A1A1A4A1Z1	7-11- 45	A1A1A5A1C29	7- 7- 53
A1A1A4A1R69	7-11-135	A1A1A4A1Z2	7-11- 39A	A1A1A5A1C3	7- 7- 12
A1A1A4A1R7	7-11- 25	A1A1A5	7- 2- 2	A1A1A5A1C30	7- 7- 49
A1A1A4A1R70	7-11-134	A1A1A5	7- 6-REF	A1A1A5A1C31	7- 7- 3

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A1A1A5A1C32	7- 7- 3	A1A1A5A1C81	7- 7-108	A1A1A5A1L6	7- 7- 11
A1A1A5A1C33	7- 7- 37	A1A1A5A1C82	7- 7- 99	A1A1A5A1L7	7- 7- 11
A1A1A5A1C34	7- 7- 37	A1A1A5A1C83	7- 7- 98	A1A1A5A1L9	7- 7- 51
A1A1A5A1C35	7- 7- 36	A1A1A5A1C84	7- 7- 95	A1A1A5A1Q1	7- 7- 20
A1A1A5A1C36	7- 7- 3	A1A1A5A1C85	7- 7- 57	A1A1A5A1Q3	7- 7- 20
A1A1A5A1C37	7- 7- 45	A1A1A5A1C86	7- 7- 92	A1A1A5A1Q4	7- 7- 60
A1A1A5A1C38	7- 7- 31	A1A1A5A1C87	7- 7- 57	A1A1A5A1Q5	7- 7- 61
A1A1A5A1C39	7- 7- 42	A1A1A5A1C88	7- 7- 57	A1A1A5A1Q8	7- 7- 83
A1A1A5A1C4	7- 7- 10	A1A1A5A1C89	7- 7- 57	A1A1A5A1Q9	7- 7- 41
A1A1A5A1C40	7- 7- 26	A1A1A5A1C9	7- 7- 26	A1A1A5A1RT1	7- 7- 28
A1A1A5A1C41	7- 7- 62	A1A1A5A1C90	7- 7- 57	A1A1A5A1RT4	7- 7-120
A1A1A5A1C42	7- 7- 57	A1A1A5A1C91	7- 7-107	A1A1A5A1R1	7- 7- 7
A1A1A5A1C43	7- 7- 57	A1A1A5A1C92	7- 7-111	A1A1A5A1R100	7- 7-124
A1A1A5A1C44	7- 7- 26	A1A1A5A1C93	7- 7- 53	A1A1A5A1R101	7- 7- 69
A1A1A5A1C45	7- 7- 57	A1A1A5A1C95	7- 7- 26	A1A1A5A1R102	7- 7- 68
A1A1A5A1C46	7- 7-110	A1A1A5A1C96	7- 7- 77	A1A1A5A1R103	7- 7-115
A1A1A5A1C5	7- 7- 8	A1A1A5A1C97	7- 7- 78	A1A1A5A1R104	7- 7-116
A1A1A5A1C55	7- 7-127	A1A1A5A1C98	7- 7- 57	A1A1A5A1R105	7- 7-117
A1A1A5A1C56	7- 7-127	A1A1A5A1C99	7- 7- 49	A1A1A5A1R106	7- 7- 79
A1A1A5A1C57	7- 7-130	A1A1A5A1FL1	7- 7- 59	A1A1A5A1R107	7- 7- 67
A1A1A5A1C58	7- 7-132	A1A1A5A1J1	7- 7- 13	A1A1A5A1R108	7- 7- 67
A1A1A5A1C59	7- 7- 87	A1A1A5A1J2	7- 7- 13	A1A1A5A1R109	7- 7- 70
A1A1A5A1C6	7- 7- 4	A1A1A5A1J3	7- 7-133	A1A1A5A1R110	7- 7-115
A1A1A5A1C60	7- 7- 53	A1A1A5A1L10	7- 7- 11	A1A1A5A1R111	7- 7-118
A1A1A5A1C61	7- 7- 49	A1A1A5A1L11	7- 7- 34	A1A1A5A1R112	7- 7- 70
A1A1A5A1C62	7- 7- 89	A1A1A5A1L12	7- 7- 43	A1A1A5A1R113	7- 7- 70
A1A1A5A1C63	7- 7- 57	A1A1A5A1L13	7- 7- 33	A1A1A5A1R114	7- 7- 70
A1A1A5A1C64	7- 7- 57	A1A1A5A1L14	7- 7- 33	A1A1A5A1R115	7- 7- 70
A1A1A5A1C66	7- 7- 57	A1A1A5A1L15	7- 7- 33	A1A1A5A1R17	7- 7- 56
A1A1A5A1C67	7- 7- 95	A1A1A5A1L16	7- 7- 33	A1A1A5A1R18	7- 7- 47
A1A1A5A1C68	7- 7- 49	A1A1A5A1L17	7- 7- 33	A1A1A5A1R19	7- 7- 48
A1A1A5A1C69	7- 7- 89	A1A1A5A1L18	7- 7- 33	A1A1A5A1R2	7- 7- 6
A1A1A5A1C7	7- 7- 3	A1A1A5A1L19	7- 7- 33	A1A1A5A1R20	7- 7- 47
A1A1A5A1C70	7- 7- 49	A1A1A5A1L20	7- 7- 51	A1A1A5A1R21	7- 7- 50
A1A1A5A1C71	7- 7- 86	A1A1A5A1L21	7- 7- 94	A1A1A5A1R22	7- 7- 52
A1A1A5A1C72	7- 7- 46	A1A1A5A1L22	7- 7-112	A1A1A5A1R24	7- 7- 22
A1A1A5A1C73	7- 7-109	A1A1A5A1L23	7- 7- 33	A1A1A5A1R25	7- 7- 44
A1A1A5A1C74	7- 7- 49	A1A1A5A1L24	7- 7- 21	A1A1A5A1R26	7- 7- 35
A1A1A5A1C75	7- 7- 49	A1A1A5A1L25	7- 7- 71	A1A1A5A1R27	7- 7- 9
A1A1A5A1C76	7- 7-113	A1A1A5A1L26	7- 7- 71	A1A1A5A1R28	7- 7- 29
A1A1A5A1C77	7- 7-109	A1A1A5A1L27	7- 7- 71	A1A1A5A1R29	7- 7- 40
A1A1A5A1C78	7- 7-102	A1A1A5A1L28	7- 7- 71	A1A1A5A1R3	7- 7- 5
A1A1A5A1C79	7- 7-104	A1A1A5A1L3	7- 7- 11	A1A1A5A1R30	7- 7- 63
A1A1A5A1C8	7- 7- 24	A1A1A5A1L4	7- 7- 23	A1A1A5A1R31	7- 7- 63
A1A1A5A1C80	7- 7-102	A1A1A5A1L5	7- 7- 21	A1A1A5A1R32	7- 7- 79

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A1A1A5A1R33	7- 7- 65	A1A1A5A1R87	7- 7- 76	A1A1A6A1CR21	7- 9- 32
A1A1A5A1R34	7- 7- 64	A1A1A5A1R88	7- 7- 93	A1A1A6A1CR22	7- 9- 32
A1A1A5A1R38	7- 7- 81	A1A1A5A1R89	7- 7- 93	A1A1A6A1CR23	7- 9- 32
A1A1A5A1R39	7- 7- 81	A1A1A5A1R91	7- 7- 74	A1A1A6A1CR25	7- 9- 18
A1A1A5A1R4	7- 7- 9	A1A1A5A1R92	7- 7- 65	A1A1A6A1CR26	7- 9- 32
A1A1A5A1R41	7- 7- 88	A1A1A5A1R93	7- 7- 72	A1A1A6A1CR27	7- 9- 32
A1A1A5A1R42	7- 7- 70	A1A1A5A1R94	7- 7- 73	A1A1A6A1CR28	7- 9-117
A1A1A5A1R47	7- 7- 79	A1A1A5A1R95	7- 7- 70	A1A1A6A1CR3	7- 9- 18
A1A1A5A1R48	7- 7- 90	A1A1A5A1R96	7- 7- 82	A1A1A6A1CR4	7- 9- 7
A1A1A5A1R5	7- 7- 29	A1A1A5A1R97	7- 7- 97	A1A1A6A1CR5	7- 9- 7
A1A1A5A1R52	7- 7- 79	A1A1A5A1R98	7- 7- 79	A1A1A6A1CR6	7- 9- 18
A1A1A5A1R53	7- 7- 90	A1A1A5A1R99	7- 7- 79	A1A1A6A1CR8	7- 9-132
A1A1A5A1R54	7- 7- 76	A1A1A5A1TP1	7- 7- 58	A1A1A6A1CR9	7- 9- 7
A1A1A5A1R55	7- 7-129	A1A1A5A1TP10	7- 7- 58	A1A1A6A1C1	7- 9-123
A1A1A5A1R56	7- 7- 76	A1A1A5A1TP5	7- 7- 2	A1A1A6A1C10	7- 9-138
A1A1A5A1R58	7- 7- 64	A1A1A5A1TP6	7- 7-125	A1A1A6A1C100	7- 9- 47
A1A1A5A1R59	7- 7-131	A1A1A5A1TP7	7- 7-125	A1A1A6A1C101	7- 9- 47
A1A1A5A1R6	7- 7- 27	A1A1A5A1TP8	7- 7-125	A1A1A6A1C102	7- 9- 47
A1A1A5A1R60	7- 7- 84	A1A1A5A1T1	7- 7- 85	A1A1A6A1C103	7- 9- 20
A1A1A5A1R61	7- 7- 82	A1A1A5A1U1	7- 7-121	A1A1A6A1C11	7- 9- 4
A1A1A5A1R62	7- 7- 72	A1A1A5A1U2	7- 7-122	A1A1A6A1C12	7- 9- 16
A1A1A5A1R63	7- 7-123	A1A1A5A1U5	7- 7- 91	A1A1A6A1C13	7- 9-140
A1A1A5A1R64	7- 7-126	A1A1A5A1U6	7- 7-100	A1A1A6A1C14	7- 9-139
A1A1A5A1R65	7- 7- 63	A1A1A5A1U7	7- 7- 75	A1A1A6A1C15	7- 9- 4
A1A1A5A1R66	7- 7-114	A1A1A5A1U8	7- 7- 75	A1A1A6A1C16	7- 9-140
A1A1A5A1R67	7- 7-128	A1A1A5A1U9	7- 7-105	A1A1A6A1C17	7- 9- 47
A1A1A5A1R68	7- 7- 90	A1A1A5A1Y1	7- 7- 38	A1A1A6A1C18	7- 9- 16
A1A1A5A1R69	7- 7- 88	A1A1A5A1Y2	7- 7- 96	A1A1A6A1C19	7- 9- 13
A1A1A5A1R7	7- 7- 22	A1A1A6	7- 2- 3	A1A1A6A1C20	7- 9- 47
A1A1A5A1R70	7- 7-106	A1A1A6	7- 8-REF	A1A1A6A1C21	7- 9- 19
A1A1A5A1R71	7- 7- 79	A1A1A6A1	7- 8- 1	A1A1A6A1C22	7- 9- 47
A1A1A5A1R72	7- 7-124	A1A1A6A1	7- 9-REF	A1A1A6A1C23	7- 9- 47
A1A1A5A1R73	7- 7-101	A1A1A6A1CR1	7- 9- 18	A1A1A6A1C24	7- 9- 11
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GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

1.3 A BAR (—) ABOVE A SIGNAL NAME MEANS THE INVERTED (NOT) FORM OF THE SIGNAL.

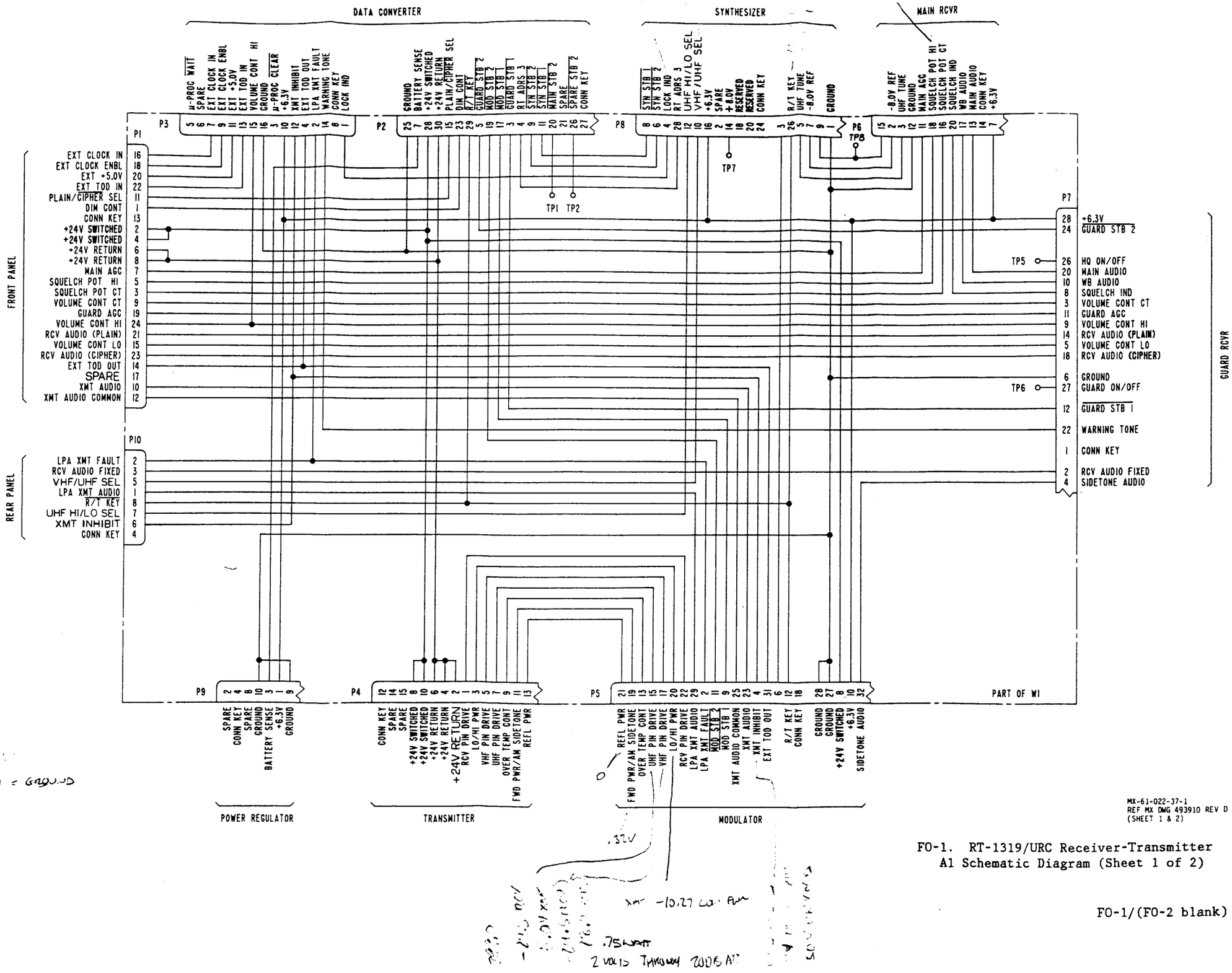
2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED: VOLTAGES ARE DC.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION IAIAI.

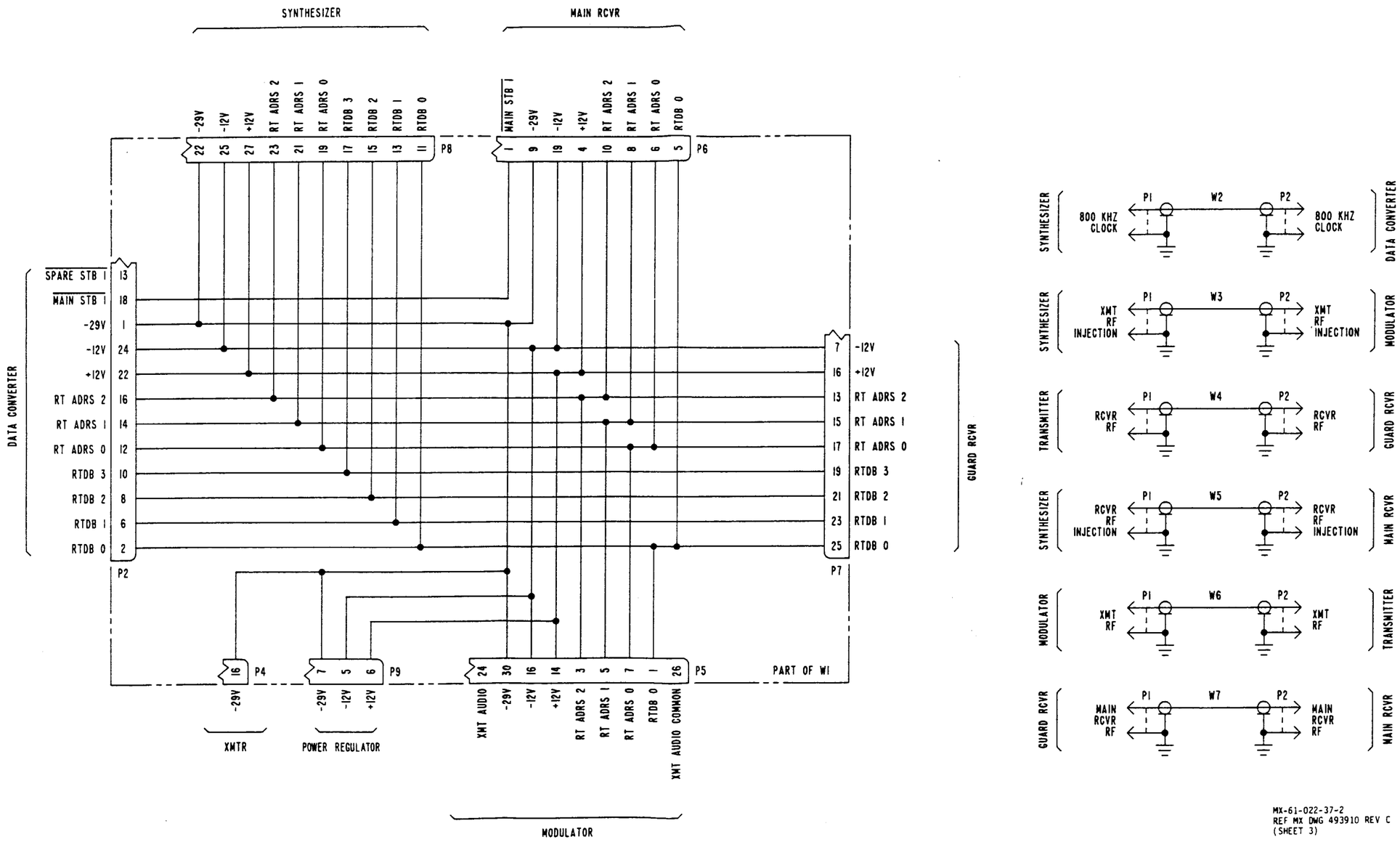
2.3 REFERENCE:
ASSEMBLY NUMBER 914858-801,-803.
W1 ASSEMBLY NUMBER 566102-801.
PRINTED WIRING BOARD 566586-1.

REF DESIGNATION	
HIGHEST USED	NOT USED
P10 TP7 W7	



MX-61-022-37-1
REF MX DWG 493910 REV D
(SHEET 1 & 2)

FO-1. RT-1319/URC Receiver-Transmitter A1 Schematic Diagram (Sheet 1 of 2)



MX-61-022-37-2
REF MX DWG 493910 REV C
(SHEET 3)

FO-1. RT-1319/URC Receiver-Transmitter
A1 Schematic Diagram (Sheet 2 of 2)

REF DESIGNATION	
HIGHEST USED	NOT USED
A4	
A1 ASSY	
J3 P1	J1
A2 ASSY	
J6	
A3 ASSY	
J3 P4	J2 P3
A4 ASSY	
P1	

CROSS REFERENCE TABLE			
REFERENCE DESIGNATION	ASSEMBLY NUMBER	PRINTED WIRING BOARD	SCHEMATIC
A1	914870-801	410903-1	493906
A2	914871-804	410904-1	493908
	914871-805		
	914871-806		
	914871-807		
	815881-801	413536-1	395871
A3	914892-803	410913-1	493907
	914892-804		
A4	811947-801	411952-1	494412

NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

1.3 A NUMBER SIGN (#) FOLLOWING A SIGNAL NAME MEANS THE INVERTED (NOT) FORM OF THE SIGNAL.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
VOLTAGES ARE DC.

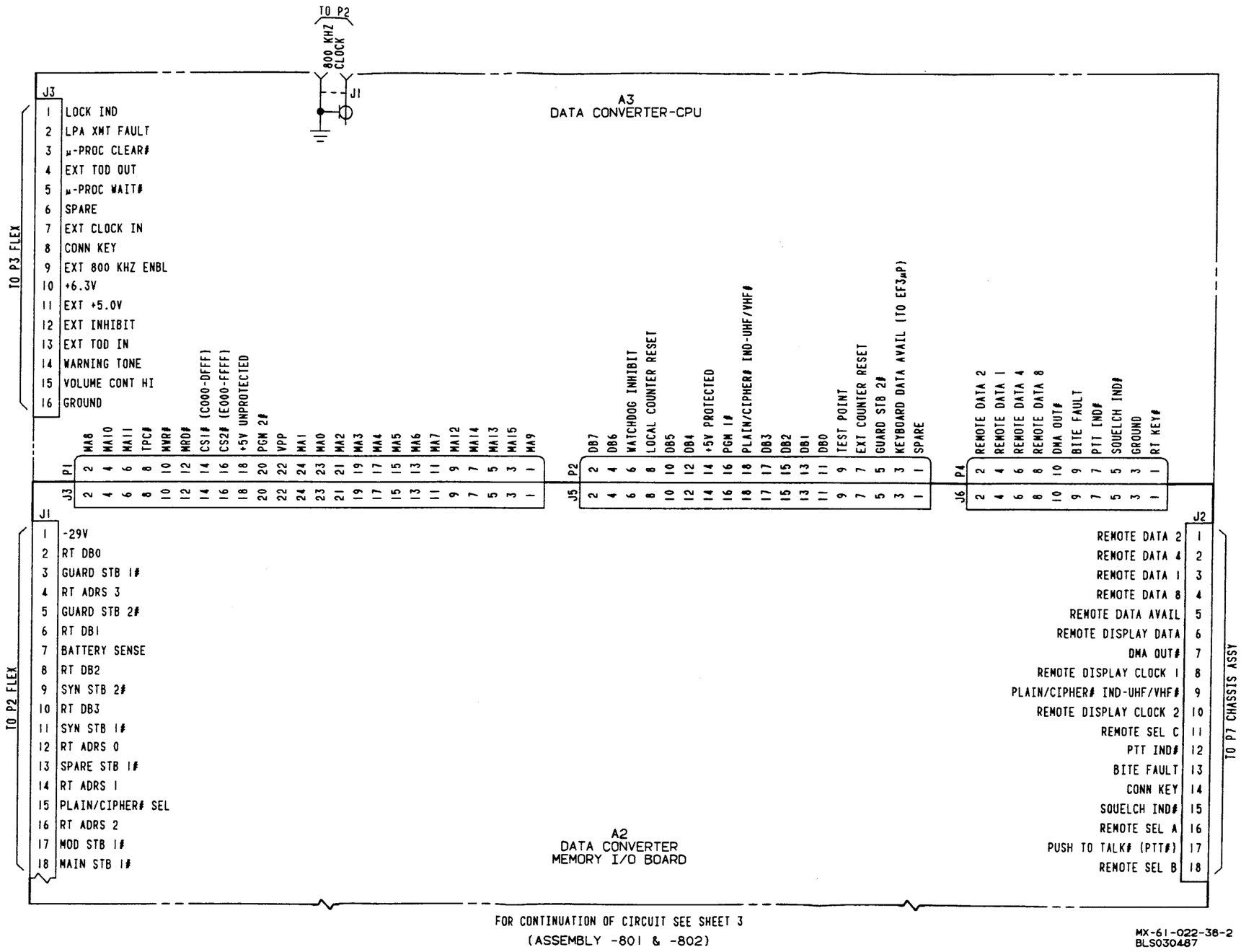
2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION 1A1A1A1.

2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 493886 & 493910.

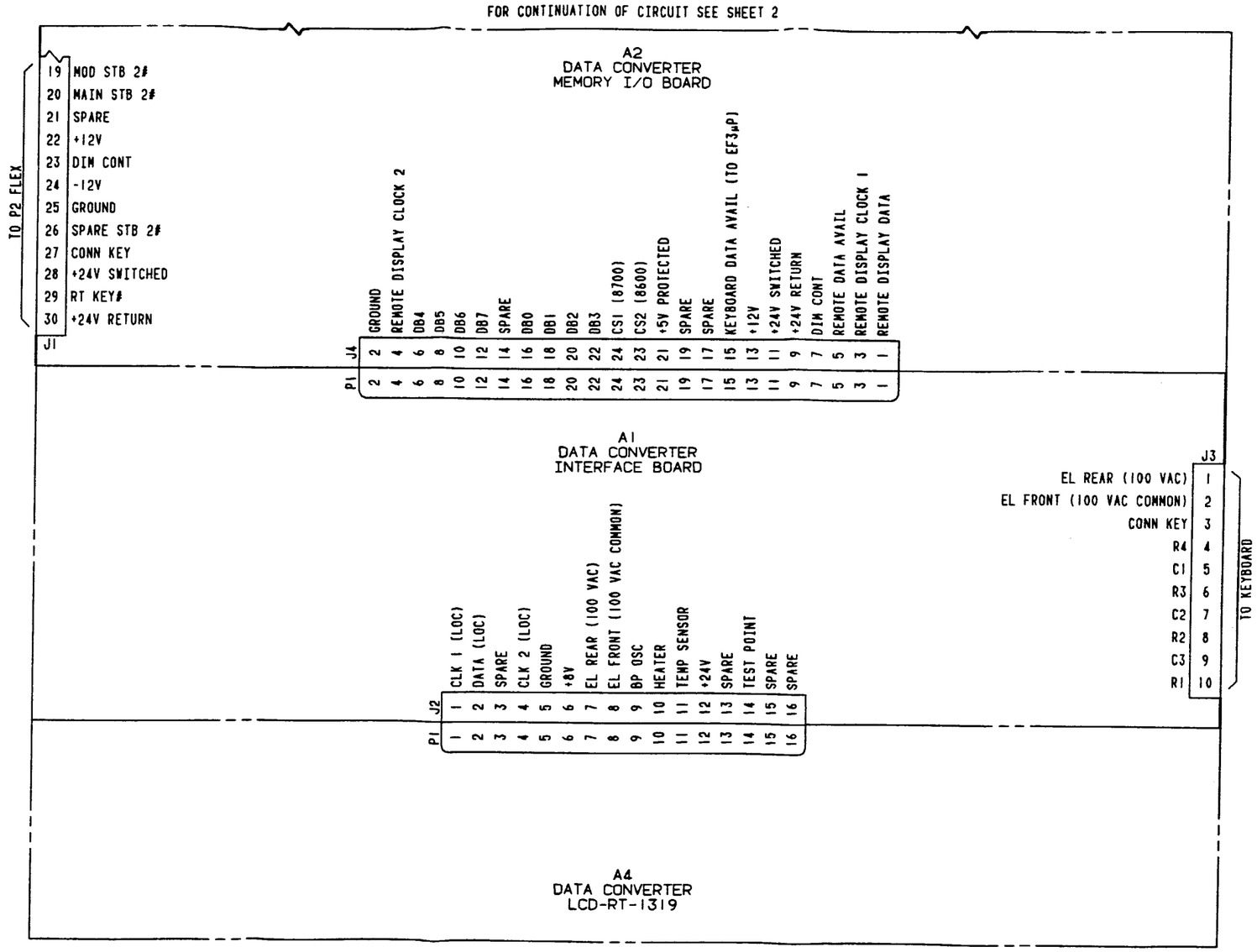
2.4 REFERENCE:
ASSEMBLY PART NUMBER 914861-801, -802 & -803.

MX-61-022-38-1
MADE FROM DWG 492691 REV C
BLS 041587

FO-2. Control/Data Converter CCA A1A1A1
Schematic Diagram
(Sheet 1 of 3)



FO-2. Control/Data Converter CCA A1A1A1
Schematic Diagram
(Sheet 2 of 3)



FO-2. Control/Data Converter CCA A1A1A1
Schematic Diagram
(Sheet 3 of 3)

REF DESIGNATION	
HIGHEST USED	NOT USED
C12 CR2 E4 J3 P1 PS1 Q3 R33 U6	C3,C6 J1 R13,R14

	INTEGRATED CIRCUIT TABLE						
	REFERENCE DESIGNATION	SECOND TAGGING LINE SYM	PART NUMBER	POWER INPUT PINS			
				+5V	+8V	GND	
	U4,5	M1	JM38510/11201BCX	NA	3	12	
	U6	M2	616195-910	NA	NA	NA	
2.4	U1	M3	616391-901	20	NA	10	
2.4	U3	M4	JM38510/05151BCX	14	NA	7	
2.4	U2	M5	616667-901	18	NA	9	

UNUSED LOGIC FUNCTIONS							
SECOND TAGGING LINE SYM	REF DES & SECTION	PIN NUMBERS					
		IN	OUT	IN	OUT	IN	OUT
M1	U5B,C,D	6,7	1	8,9	14	10,11	13

NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

1.3 A NUMBER SIGN (#) FOLLOWING A SIGNAL NAME MEANS THE INVERTED (NOT) FORM OF THE SIGNAL.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 5%, 1/8W.
CAPACITANCE VALUES ARE IN MICROFARADS.
VOLTAGES ARE DC.
DIODES AND/OR TRANSISTORS ARE JANTX TYPE.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION A1A1A1A1.

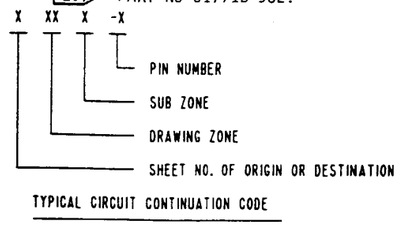
2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 492691.

2.4 THIS DEVICE REQUIRES SPECIAL HANDLING AND PROCESSING TO PREVENT DAMAGE FROM ELECTROSTATIC DISCHARGE TRANSIENTS.

2.5 REFERENCE:
ASSEMBLY NUMBER 914870-801.
PRINTED WIRING BOARD 410903-1.
SPECIFICATION, TEST 979186

2.6 SELECT AT TEST.

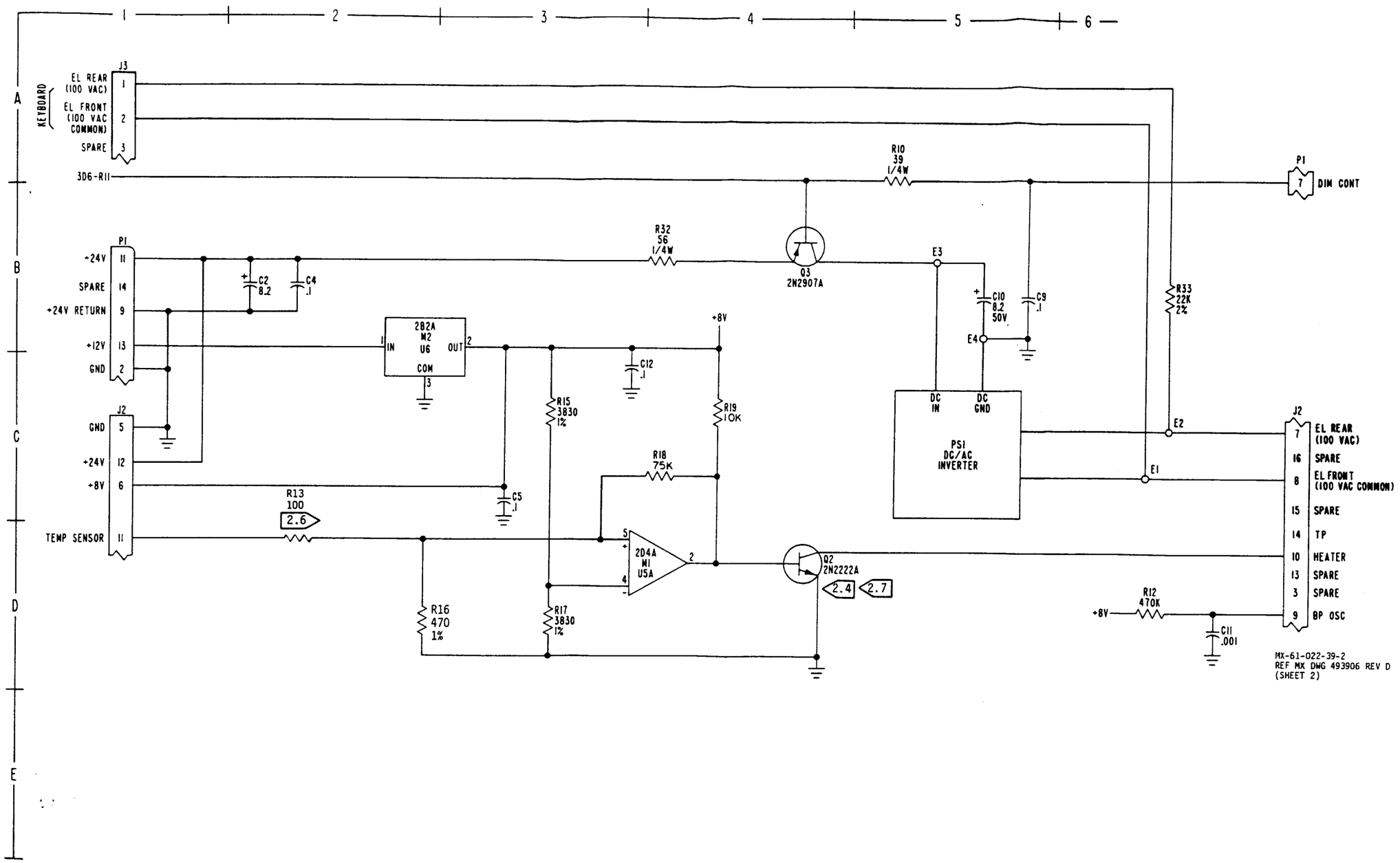
2.7 PART NO 617713-902.



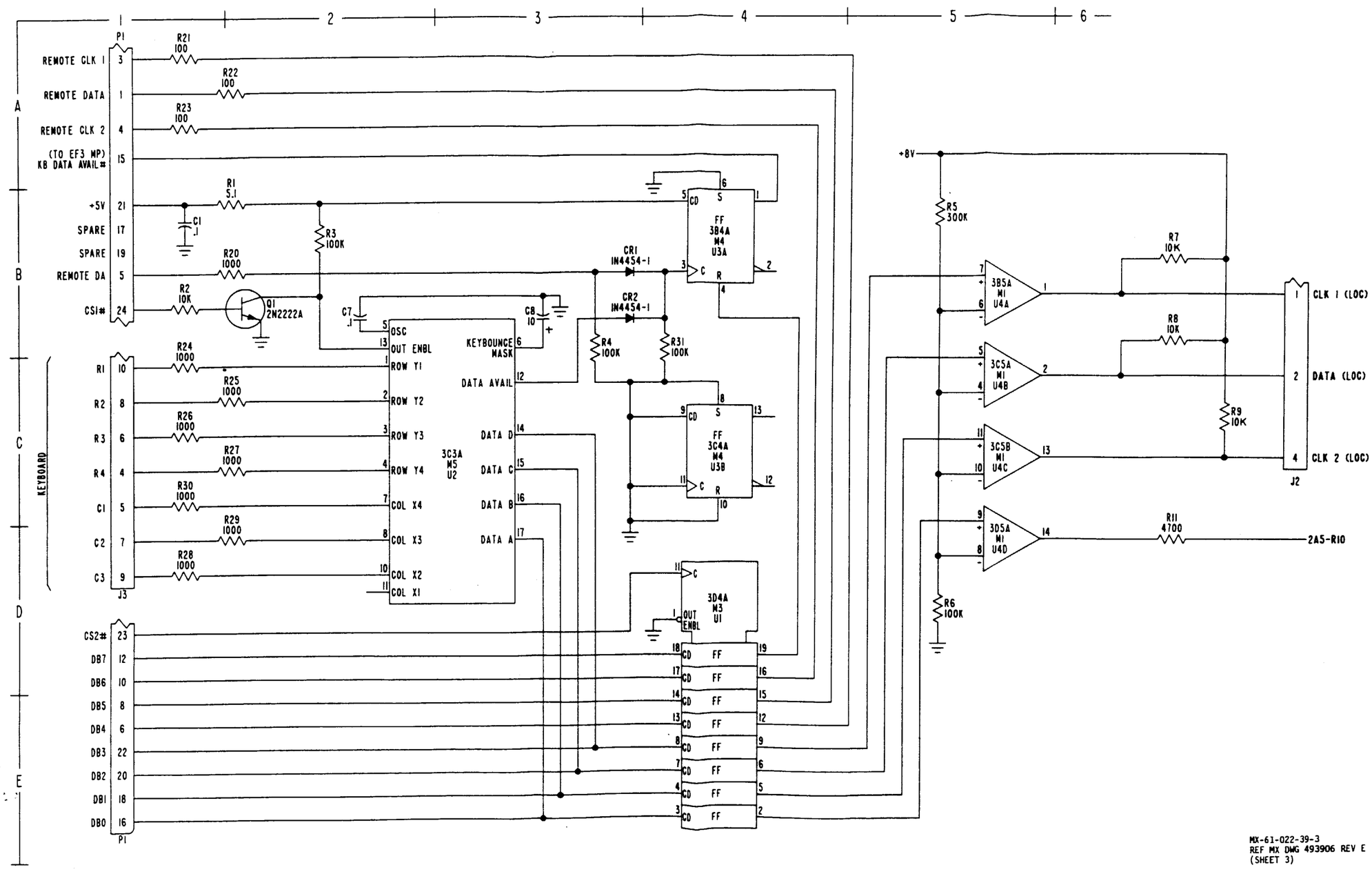
TYPICAL CIRCUIT CONTINUATION CODE

MX-61-022-39-1
MADE FROM DWG 493906 REV F
(SHEET 1)

FO-3. Interface Data Converter CCA A1A1A1A1 Schematic Diagram (Sheet 1 of 3)

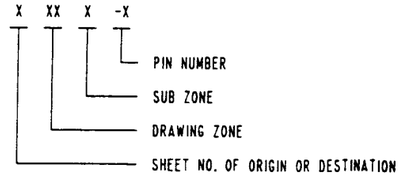


FO-3. Interface Data Converter CCA
A1A1A1A1 Schematic Diagram
(Sheet 2 of 3)



FO-3. Interface Data Converter CCA A1A1A1A1 Schematic Diagram (Sheet 3 of 3)

INTEGRATED CIRCUIT TABLE				
REF DES	SECOND TAGGING LINE SYM	PART NUMBER	PWR INPUT PINS	
			GND	PWR
2.4 U15	M1	615660-903	19	AS SHOWN
2.4 U5	M2	615699-901	8	
2.4 U17	M3	JM38510/17103BCX	7	
2.4 U16	M4	JM38510/17001BCX	7	
2.4 U12	M5	JM38510/17702BCX	7	
2.4 U2,3,18	M6	616379-901	8	
2.4 U21	M7	616387-901	10	
U1,11,13,14	M8	616391-901	10	
2.4 U4,6	M9	JM38510/17501BEX	8	
2.4 U19,20	M10	616789-901	9	
2.4 U10	M11	JM38510/17601BEX	8	
2.8 2.4 U7	M12	646337-1/646337-3	14	
2.9 2.4 U7	M12	646337-5	14	
2.10 2.4 U7	M12	647238-1	14	
2.11 2.4 U8	M13	646337-4	14	
2.12 2.4 U8	M13	647238-2	14	
2.8 2.4 U9	M14	646339-1	12	
2.13 2.4 U9	M14	646339-2	12	



TYPICAL CIRCUIT CONTINUATION CODE

REFERENCE DESIGNATIONS	
HIGHEST USED	NOT USED
C5	
CR6	
J6	
Q1	
R62	R6,31,34
U18	R57,60

NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

1.3 A NUMBER SIGN (#) FOLLOWING A SIGNAL NAME MEANS THE INVERTED (NOT) FORM OF THE SIGNAL.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 5%, 1/8 WATT.
CAPACITANCE VALUES ARE IN MICROFARADS.
VOLTAGES ARE DC.
DIODES AND/OR TRANSISTORS ARE JANTX TYPE.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION 1A1A1A1A2.

2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 492691.

2.4 THIS DEVICE REQUIRES SPECIAL HANDLING AND PROCESSING TO PREVENT DAMAGE FROM ELECTROSTATIC DISCHARGE TRANSIENTS.

2.5 USED IN ASSEMBLY 914871-801,-805 & -807 ONLY.

2.6 USED IN ASSEMBLY 914871-804 & -806 ONLY.

2.7 REFERENCE:
ASSEMBLY NUMBER 914871-801 THRU 914871-807.
PRINTED WIRING BOARD 410904-1.

2.8 USED ON ASSEMBLY 914871-801 ONLY.

2.9 USED ON ASSEMBLY 914871-804 & -805 ONLY.

2.10 USED ON ASSEMBLY 914871-806 & -807 ONLY.

2.11 USED ON ASSEMBLY 914871-804 ONLY.

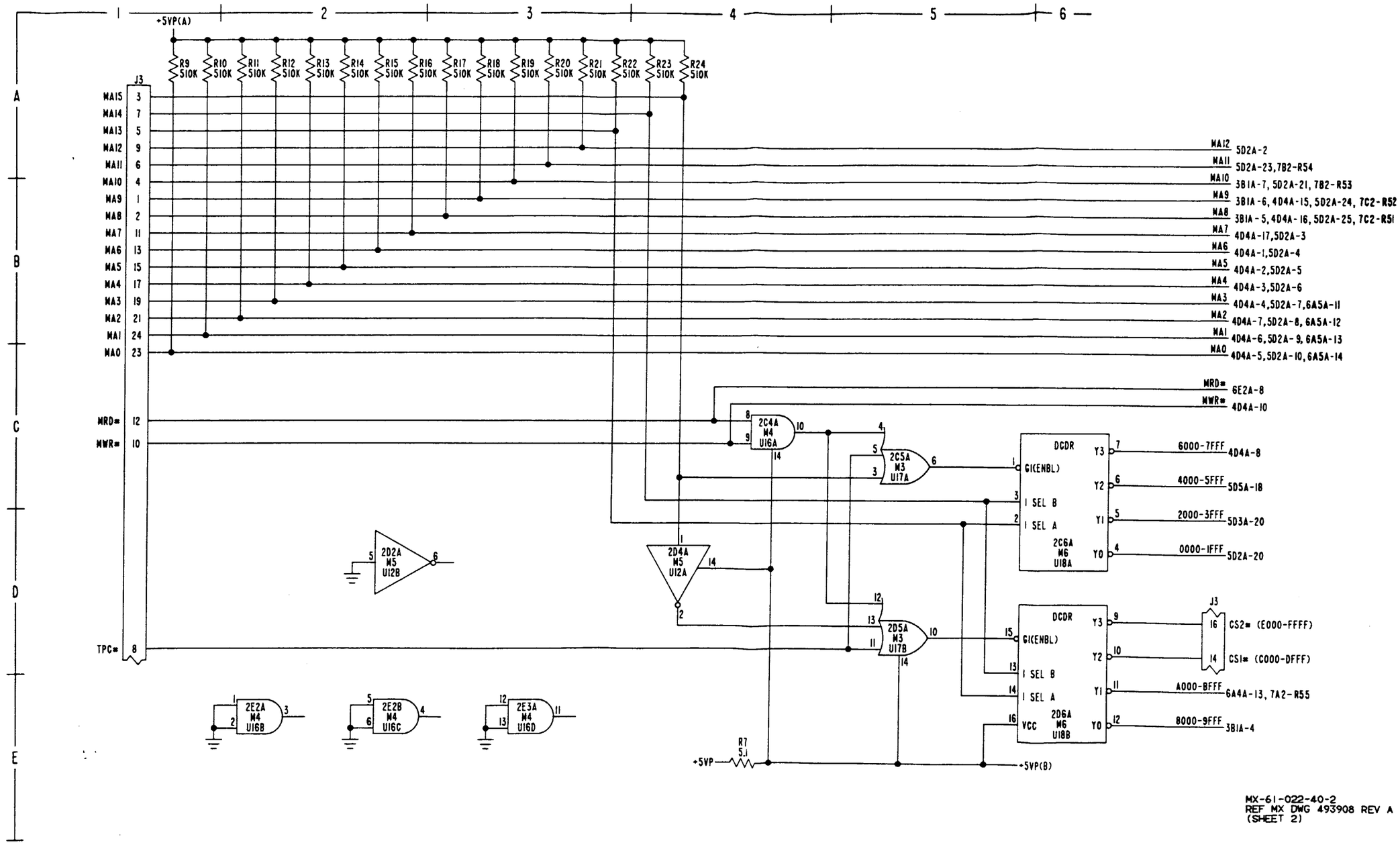
2.12 USED ON ASSEMBLY 914871-806 ONLY.

2.13 USED ON ASSEMBLY 914871-804,-805,-806 & -807 ONLY.

2.14 OPTIONAL BYASS CAPACITOR INSTALLED ONLY IF NEEDED. SAME VALUE AND PART NO. AS C5.

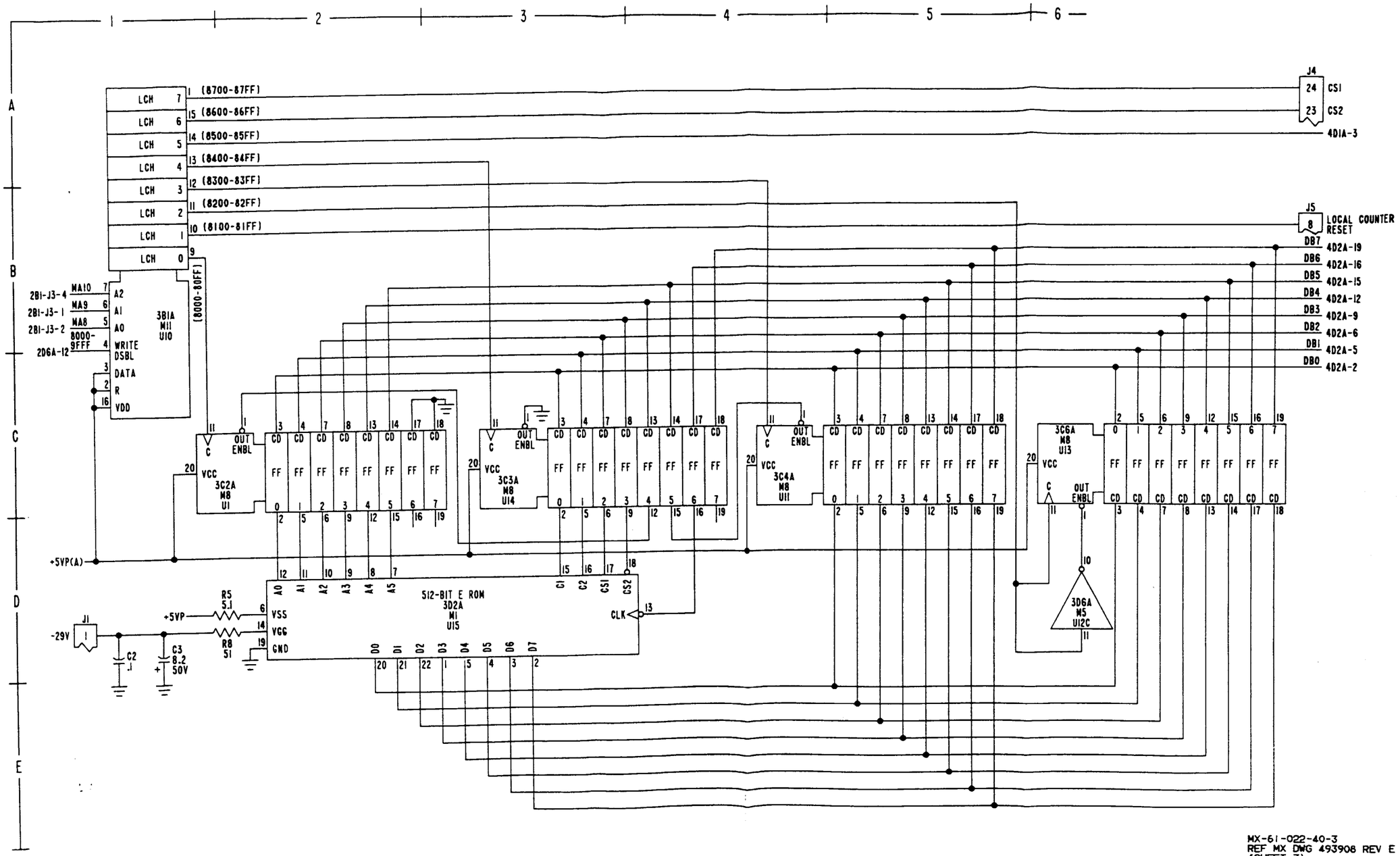
MX-61-022-40-1
REF MX DWG 493908 REV F
(SHEET 1)

FO-4. Memory I/O Data Converter CCA A1A1A1A2 Schematic Diagram (Sheet 1 of 7)



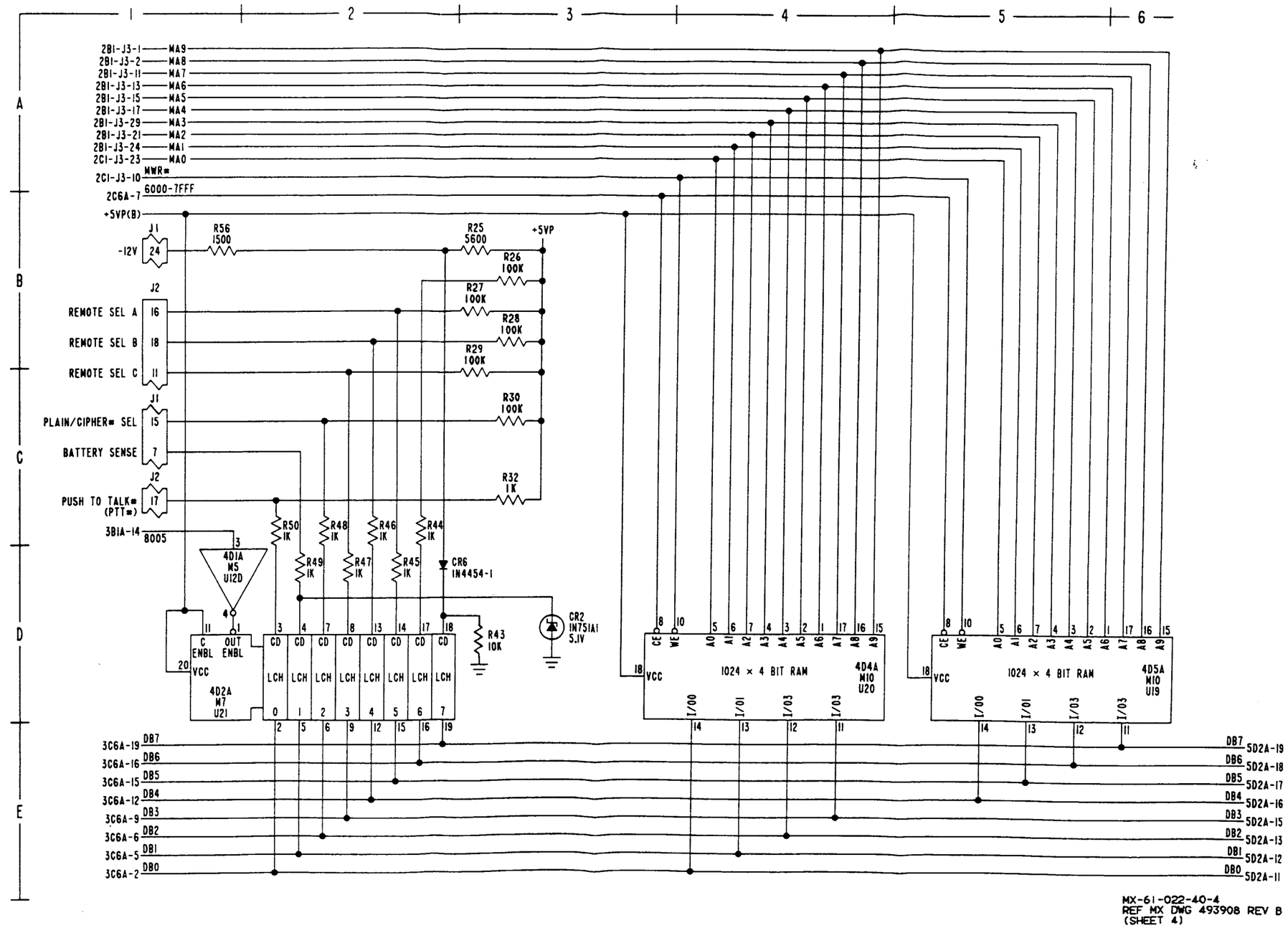
MX-61-022-40-2
REF MX DWG 493908 REV A
(SHEET 2)

FO-4. Memory I/O Data Converter CCA A1A1A1A2 Schematic Diagram (Sheet 2 of 7)



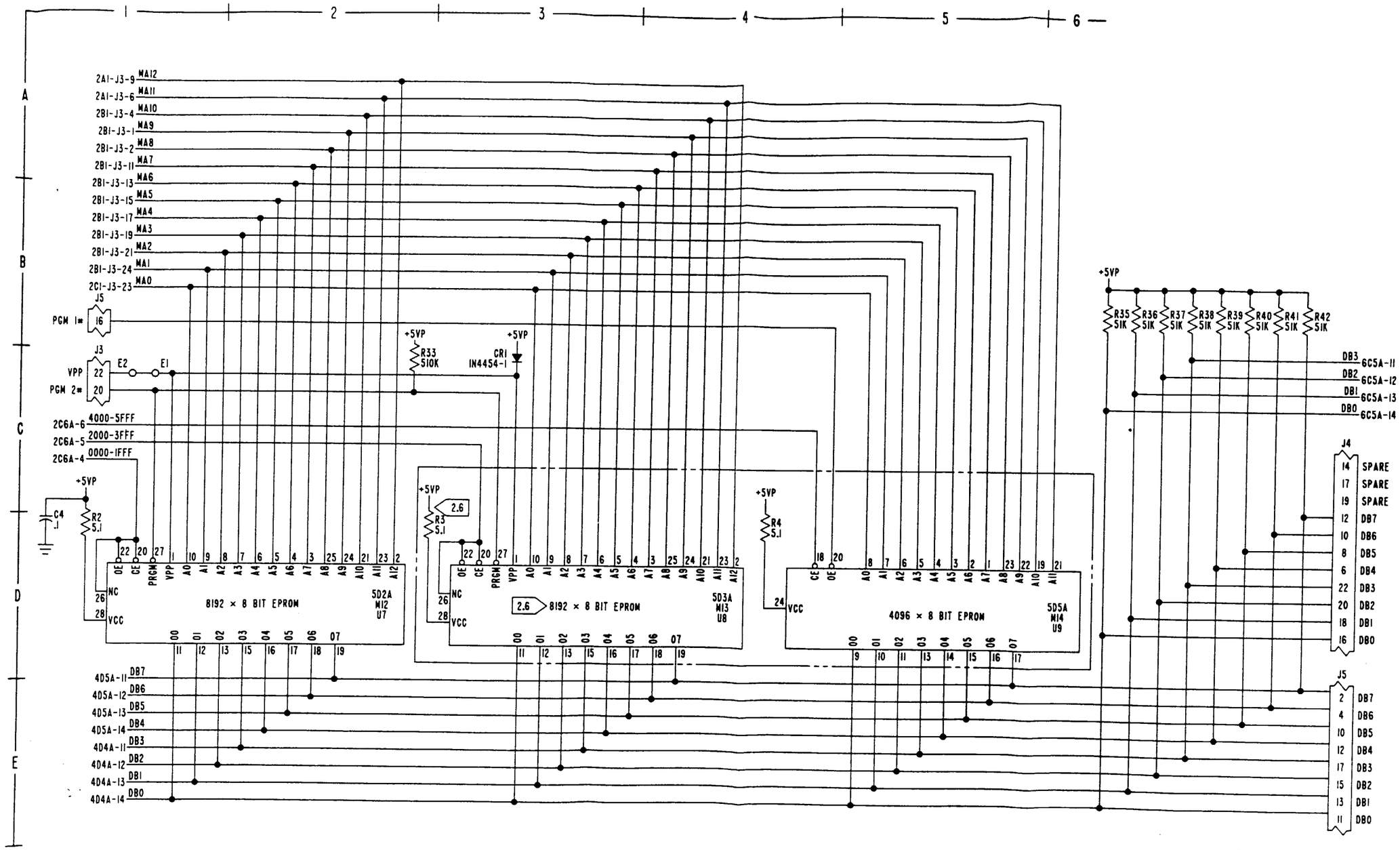
MX-61-022-40-3
REF MX DWG 493908 REV E
(SHEET 3)

FO-4. Memory I/O Data Converter CCA A1A1A1A2 Schematic Diagram (Sheet 3 of 7)



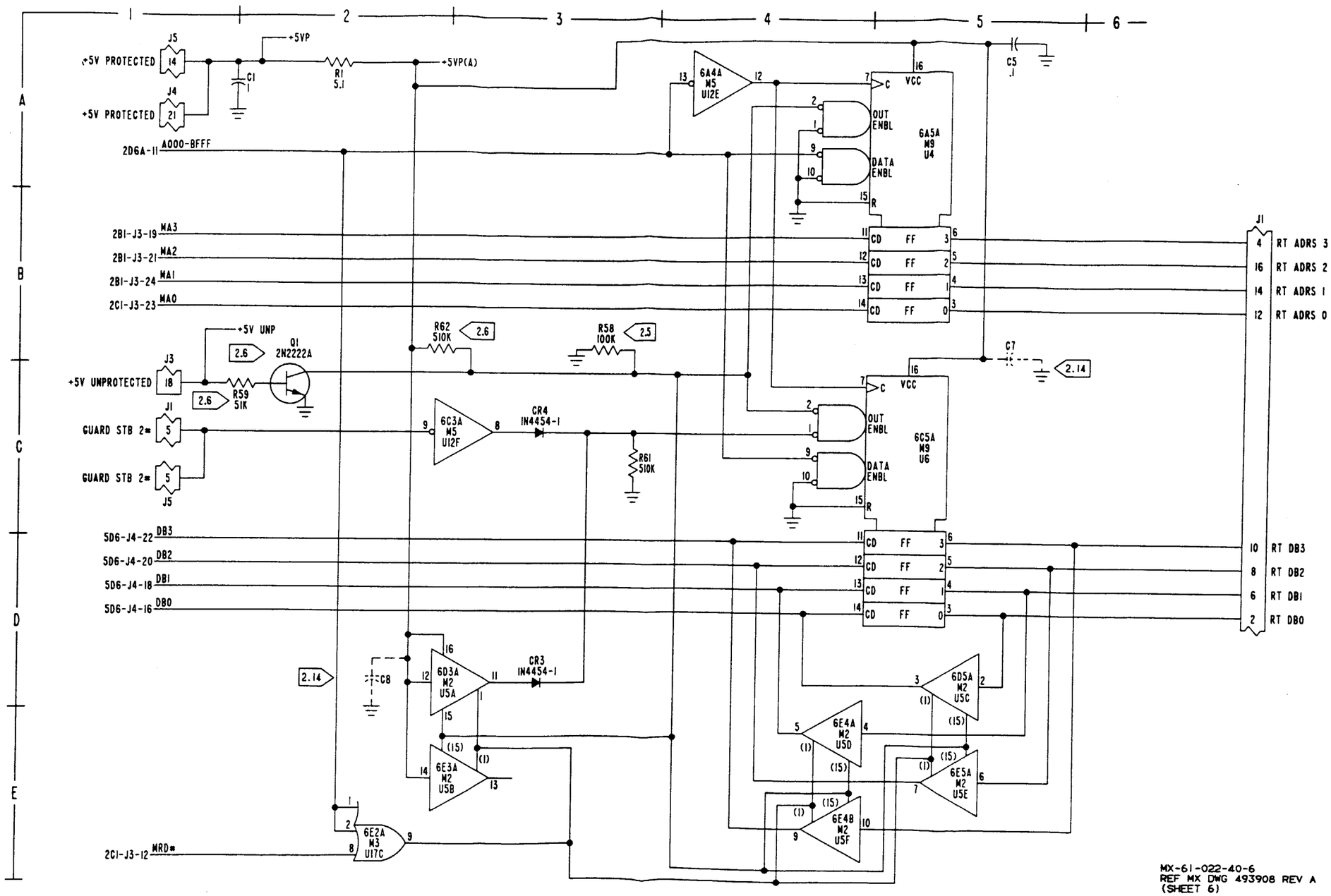
MX-61-022-40-4
REF MX DWG 493908 REV B
(SHEET 4)

FO-4. Memory I/O Data Converter CCA
A1A1A1A2 Schematic Diagram
(Sheet 4 of 7)

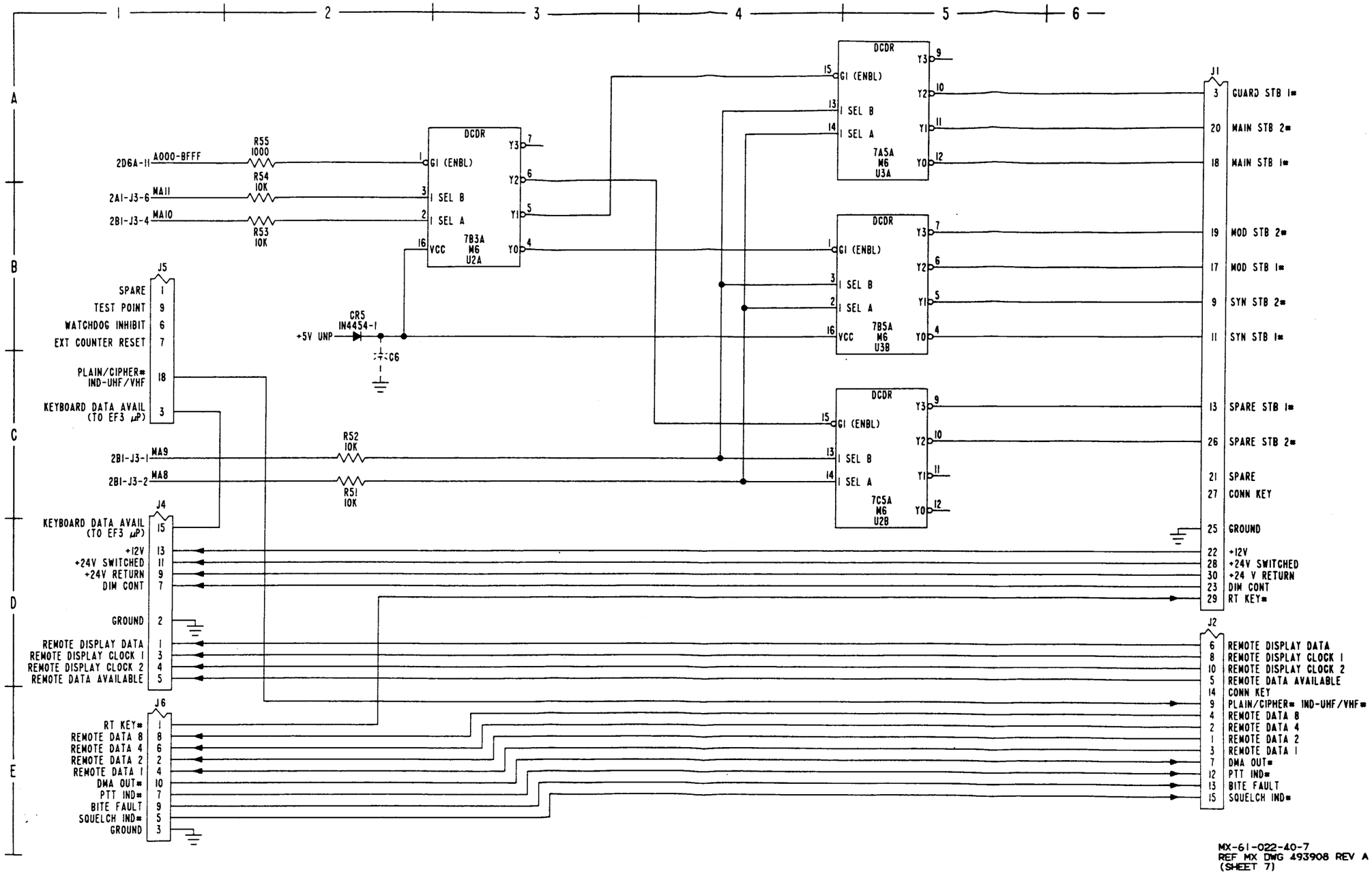


MX-61-022-40-5
REF MX DWG 493908 REV C
(SHEET 5)

FO-4. Memory I/O Data Converter CCA A1A1A1A2 Schematic Diagram (Sheet 5 of 7)



FO-4. Memory I/O Data Converter CCA
A1A1A1A2 Schematic Diagram
(Sheet 6 of 7)



MX-61-022-40-7
REF MX DWG 493908 REV A
(SHEET 7)

FO-4. Memory I/O Data Converter CCA
A1A1A1A2 Schematic Diagram
(Sheet 7 of 7)

INTEGRATED CIRCUIT TABLE							
	REF DES	SECOND TAGGING LINE SYM	PART NUMBER	POWER INPUT PINS			
				+5V	+5VA	+5VB	GND
2.6	U12,16	M1	JM38510/17101BCX	NA	NA	14	7
2.6	U11	M2	JM38510/17001BCX	NA	NA	14	7
2.6	U15	M3	JM38510/17702BCX	NA	NA	14	7
2.6	U21	M4	616387-901	NA	NA	20	10
2.6	U14	M5	JM38510/47001BQX	NA	NA	40,16	20
2.6	U19,20	M6	616391-901	NA	NA	20	10
2.6	U6	M7	616501-901	NA	14	NA	7
	U9,10			NA	NA	14	7
2.6	U8	M8	JM38510/17501BEX	NA	NA	16	8
2.6	U13	M9	JM38510/05252BCX	NA	NA	14	7
2.6	U1	M10	616670-901	NA	16	NA	7,8
	U7	M11	JM38510/31302BCX	NA	NA	14	7
2.8 2.6	U4,5	M12	JM38510/18107BEX	NA	16	NA	8
	U17	M13	616139-901	8	NA	NA	4
	U18	M14	616386-901	4	NA	NA	7
2.8 2.6	U3	M15	645526-901	NA	5	NA	10
2.6	U2	M16	646265-901	NA	1	NA	18

REF DESIGNATION	
ASSY 914892-801	
HIGHEST USED	NOT USED
C32	C4,5,7-15, 17,23,29
CR10	CR3,4
J3	J2
L1	
P4	P3
Q2	
R85	R5,8-14, 18-20,22-26, 28,37,38,60, 61,67-69,71, 72,77,82-84, 94
U21	U3-5,17,18
Y1	

REF DESIGNATION	
ASSY 914892-803	
HIGHEST USED	NOT USED
C33	C4,5,7-15, 17,23,29
CR10	CR3,4
J3	J2
L1	
P4	P3
Q2	
R85	R5,8-14, 18-20,22-26, 28,37,38,60, 61,66,67-69, 71,72,77, 82-84,94
U21	U3-5,17,18
Y1	

REF DESIGNATION	
ASSY 914892-804	
HIGHEST USED	NOT USED
C33	C4,5,18,19, 21,23-29
CR10	
J3	J2
L1	
P4	P3
Q3	
R96	R5,28,37,66, 69,71,72, 80-84,86-89, 94
U21	
Y1	

NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

1.3 A NUMBER SIGN (#) FOLLOWING A SIGNAL NAME MEANS THE INVERTED (NOT) FORM OF THE SIGNAL.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 5%,1/8W.
CAPACITANCE VALUES ARE IN MICROFARADS.
VOLTAGES ARE DC.
DIODES AND/OR TRANSISTORS ARE JANTX TYPE.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION 1A1A1A1A3.

2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 492691.

2.4 VALUE SELECTED AT TEST. NOMINAL VALUE SHOWN.

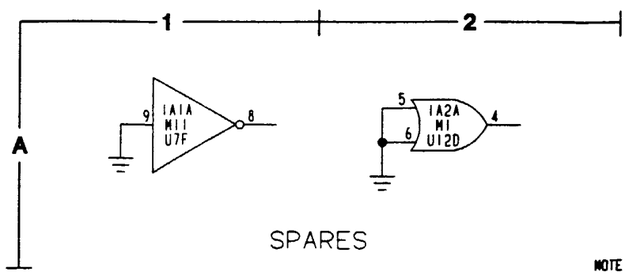
2.5 PART NUMBER 616532-901.

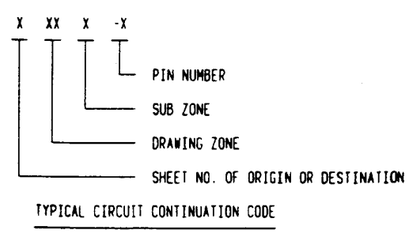
2.6 THIS DEVICE REQUIRES SPECIAL HANDLING AND PROCESSING TO PREVENT DAMAGE FROM ELECTROSTATIC DISCHARGE TRANSIENTS.

2.7 JUMPER TO BE ADDED AT PRODUCTION ON 914892-801 AND -803 ONLY.

2.8 TO BE USED IN ASSEMBLY 914892-804 ONLY.

2.9 REFERENCE:
ASSEMBLY NUMBER 914892-801, -803 & -804.
PRINTED WIRING BOARD 410913-1.



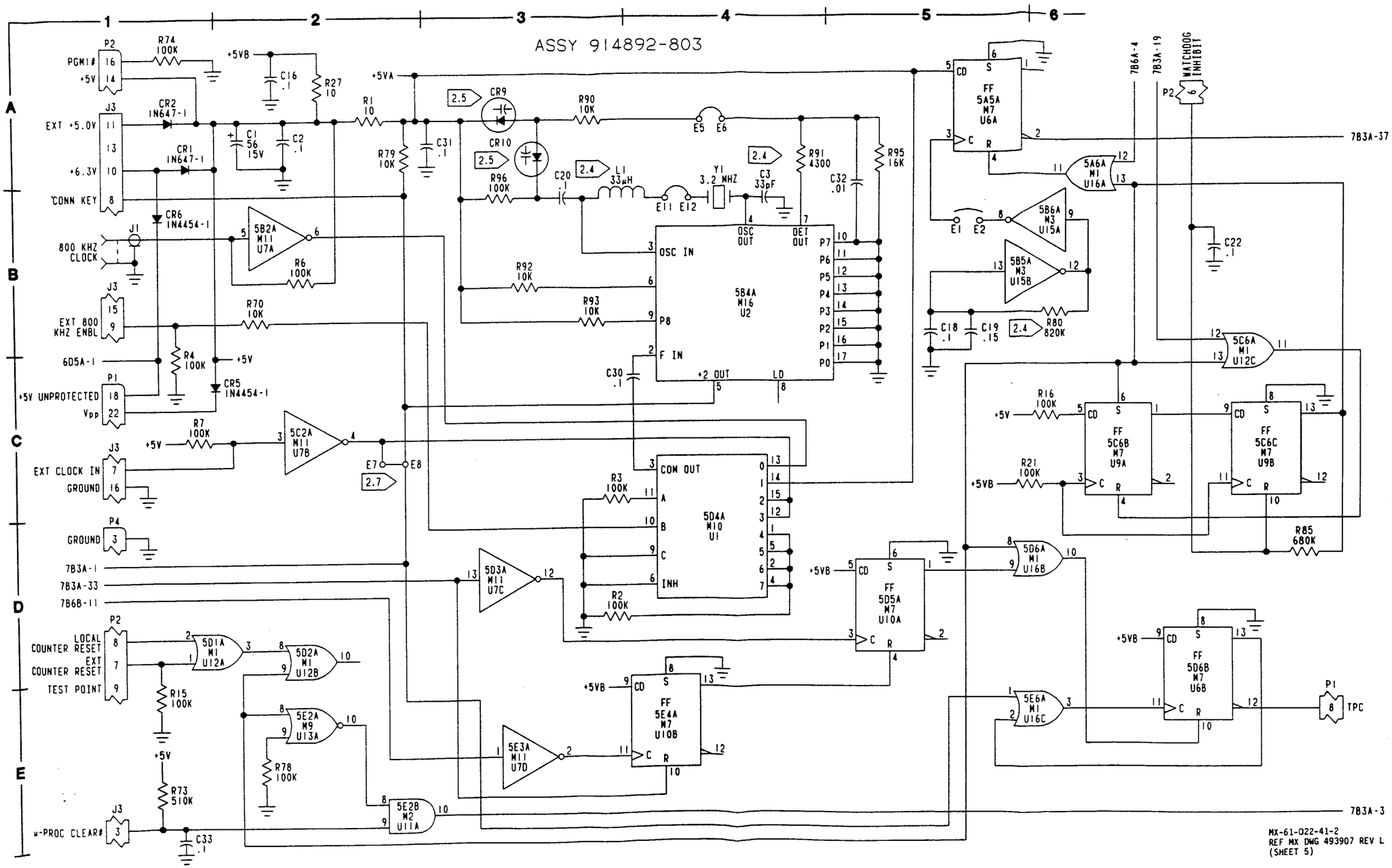


TYPICAL CIRCUIT CONTINUATION CODE

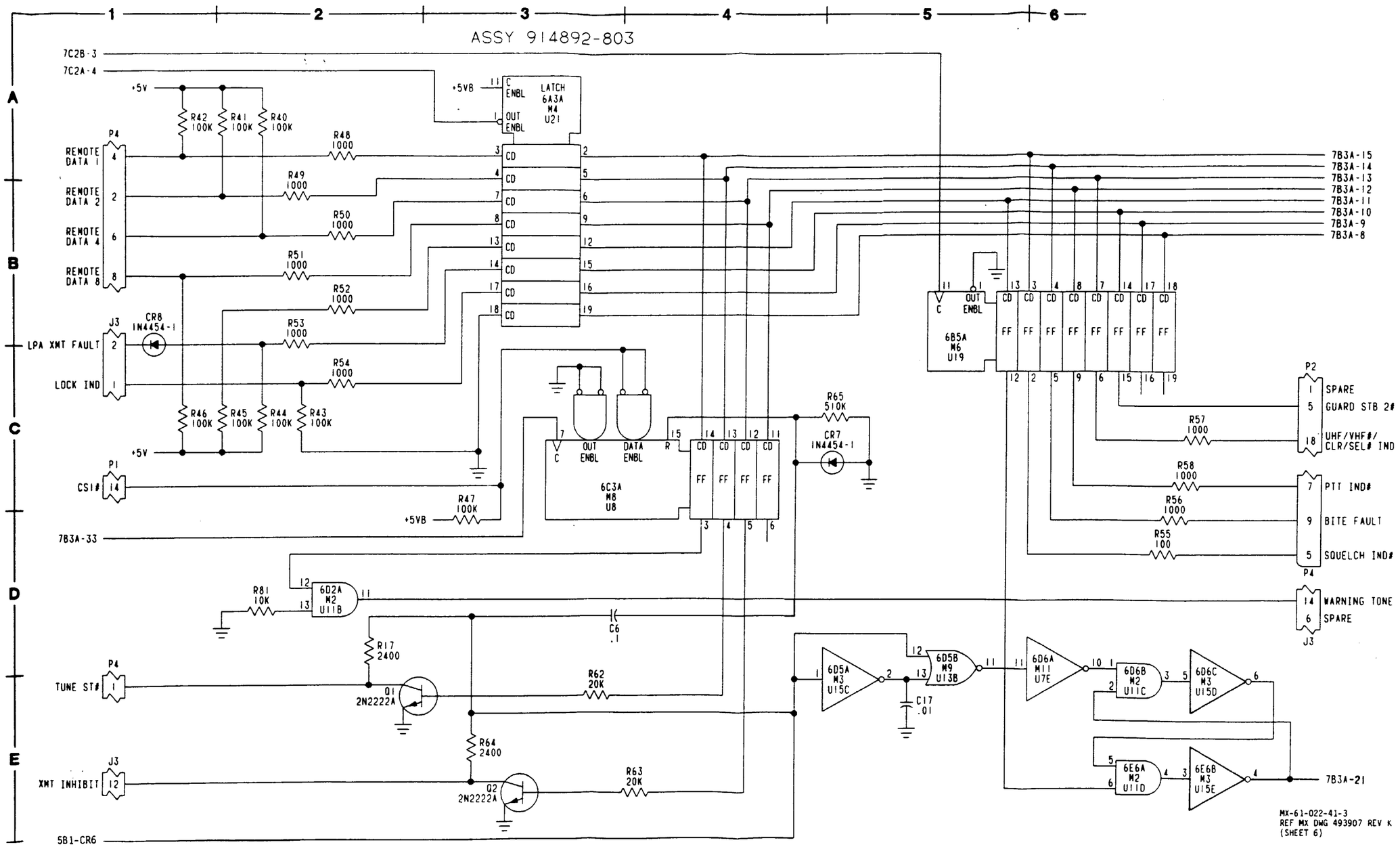
NOTE TO USER: USE THIS SHEET NUMBER FOR CIRCUIT CONTINUATION CODE LOCATOR.

MX-61-022-41-1
MADE FROM DWG 493907 REV L
(SHEET 1)

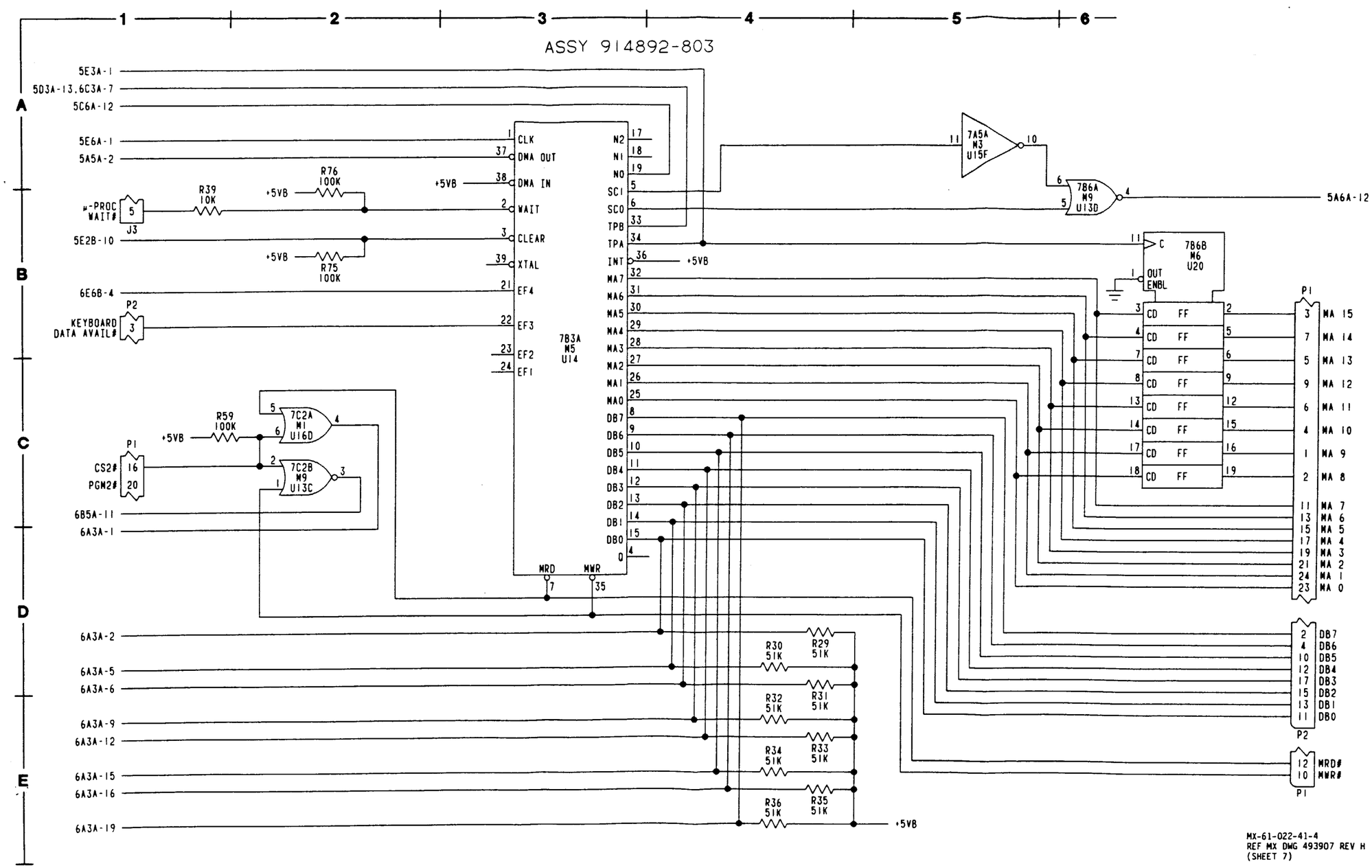
FO-5. Data Converter-CPU CCA A1A1A1A3 Schematic Diagram (Sheet 1 of 4)



FO-5. Data Converter-CPU CCA A1A1A1A3
Schematic Diagram (Sheet 2 of 4)



FO-5. Data Converter-CPU CCA A1A1A1A3
Schematic Diagram (Sheet 3 of 4)



FO-5. Data Converter-CPU CCA A1A1A1A3
Schematic Diagram (Sheet 4 of 4)

NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS. ,
RESISTORS ARE 1%, 1/8W.
VOLTAGES ARE DC.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION 1A1A1A1A4.

2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 492691.

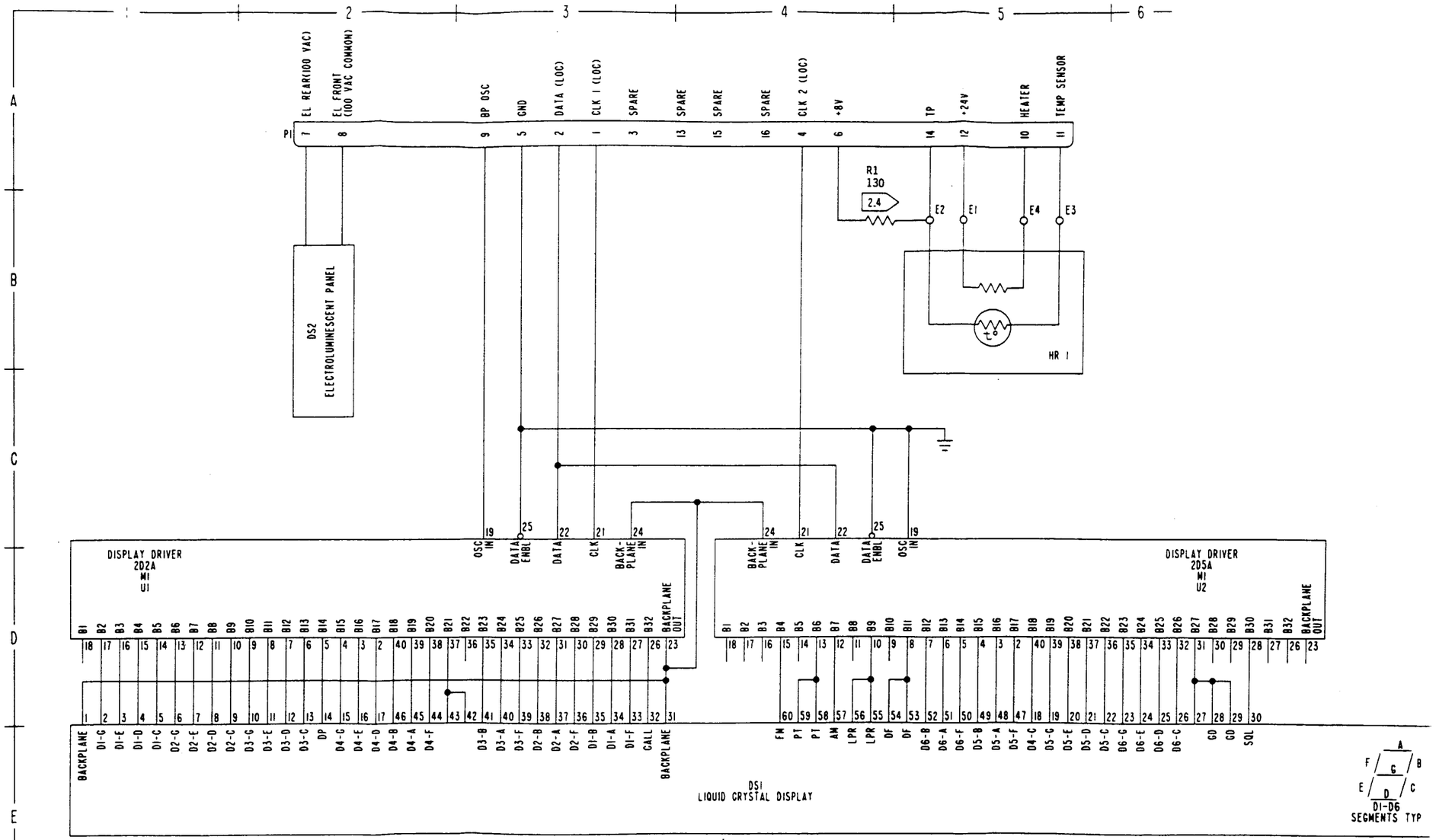
2.4 VALUE SELECTED AT TEST, NOMINAL VALUE SHOWN.

2.5 THIS DEVICE REQUIRES SPECIAL HANDLING AND PROCESSING TO PREVENT DAMAGE FROM ELECTROSTATIC DISCHARGE TRANSIENTS.

2.6 REFERENCE:
ASSEMBLY NUMBER 811947-801.
PRINTED WIRING BOARD 411952-1.

REF DESIGNATION	
HIGHEST USED	NOT USED
DS2 E4 HR 1 P1 R1 U2	

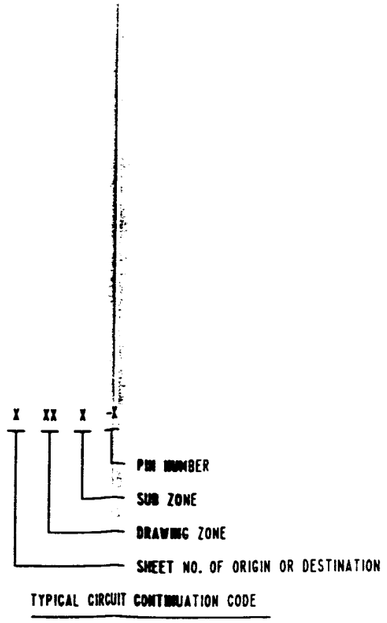
INTEGRATED CIRCUIT TABLE				
REFERENCE DESIGNATION	SECOND TAGGING LINE SYM	PART NUMBER	POWER INPUT PINS	
			+8V	GND
U1, 2	M1	645448-801	20	1



MX-61-022-42
REF MX DWG 494412 REV
(SHEET 1 AND 2)

FO-6. Data Converter CCA (LCD)
A1A1A1A4 Schematic Diagram

REF DESIGNATION	
HIGHEST USED	NOT USED
A1 C38 Q4	C1,2,5-13, 16-37 Q2
A1	
A1 C104 CR28 J4 L84 Q7 R47 RT 1 T4	C3,4,14,15 38,61,83-91, 98,99 CR17-21 J2,3 L42-46,49, 55,56,78 Q1,3,4 R29-35
A1A1	
C98 CR21 J3 L78 R35	C1-82,92-97, CR1-16 J1 L1-41,47-77 R1-28



NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 5%, 1/4W.
CAPACITANCE VALUES ARE IN PICOFARADS.
VOLTAGES ARE DC.
DIODES AND/OR TRANSISTORS ARE JANTX TYPE.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION 1A1A1A2.

2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 493886.

2.4 PART NUMBER 615467-904.

2.5 PART NUMBER 615467-905.

2.6 PART NUMBER 645512-903.

2.7 PART NUMBER 619691-905.

2.8 PART NUMBER 619915-902.

2.9 PART NUMBER 615485-2.

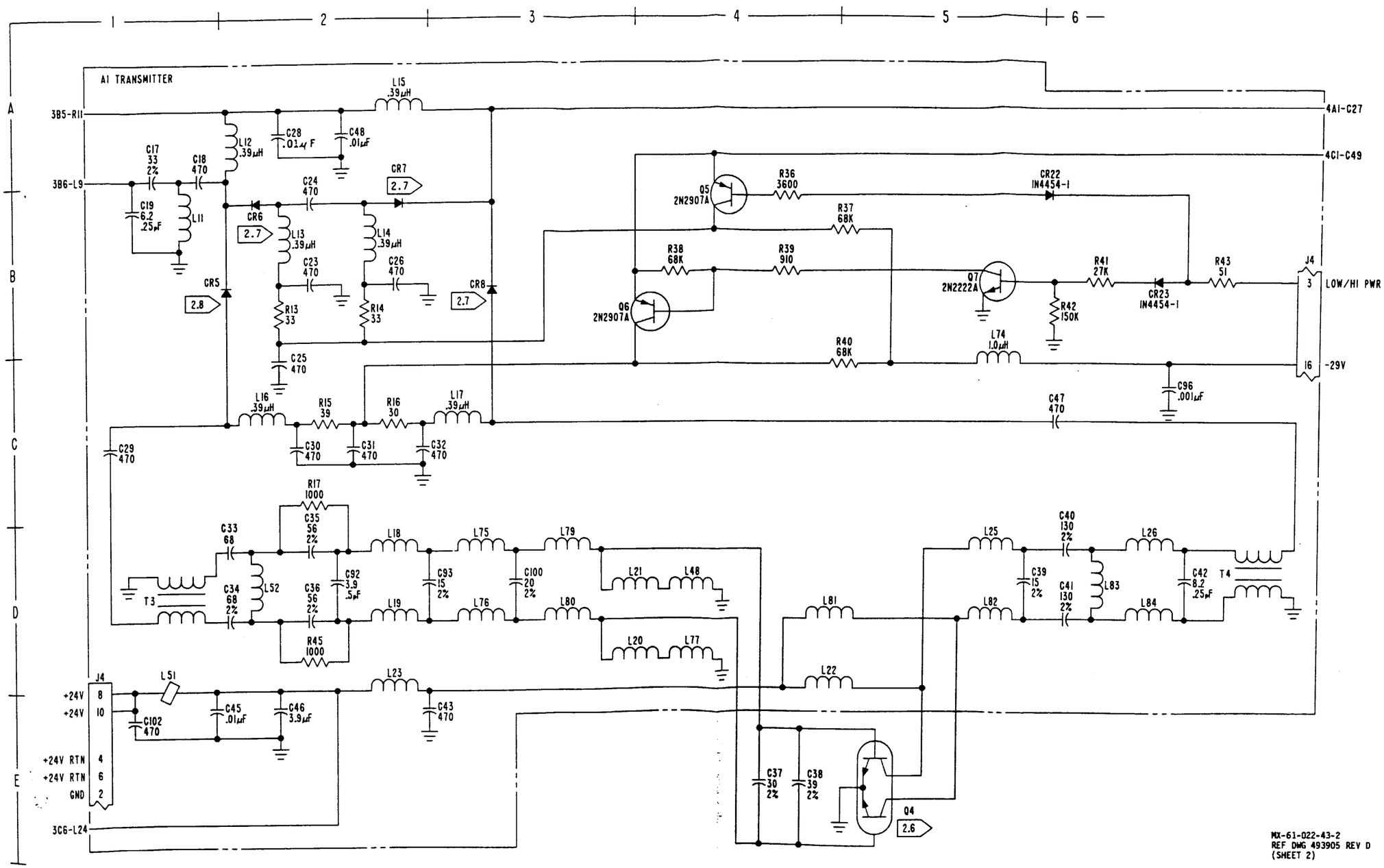
2.10 PART NUMBER 619915-903.

2.11 VALUE SELECTED AT TEST. NOMINAL VALUE SHOWN.

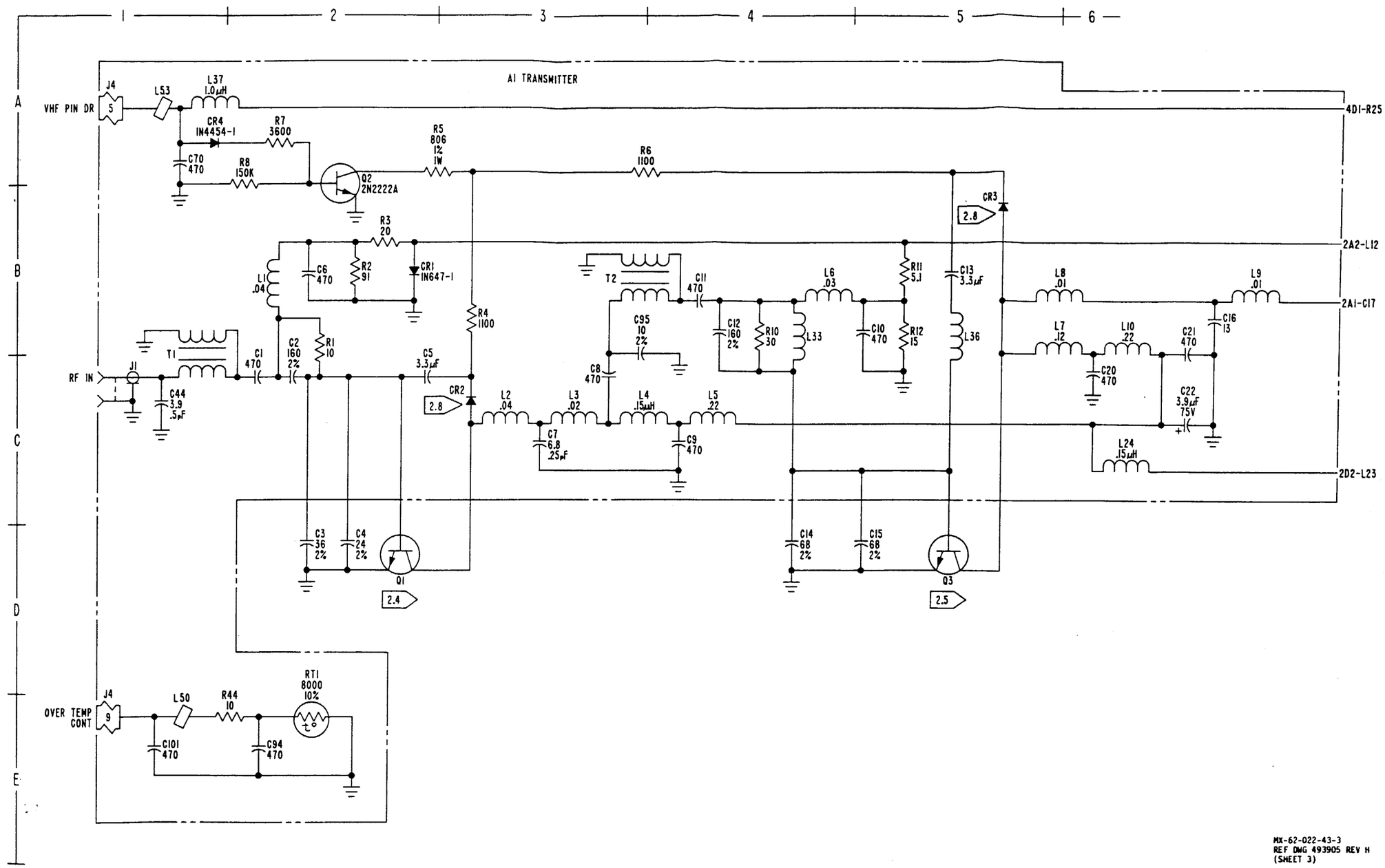
3.0 REFERENCE
ASSEMBLY NUMBER 914862-801
A1 ASSEMBLY NUMBER 914873-801.
PRINTED WIRING BOARD 410906.
A1A1 ASSEMBLY NUMBER 810075-801.
PRINTED WIRING BOARD 410949-1.

MX-61-022-43-1
REF MX DWG 493905 REV H
(SHEET 1)

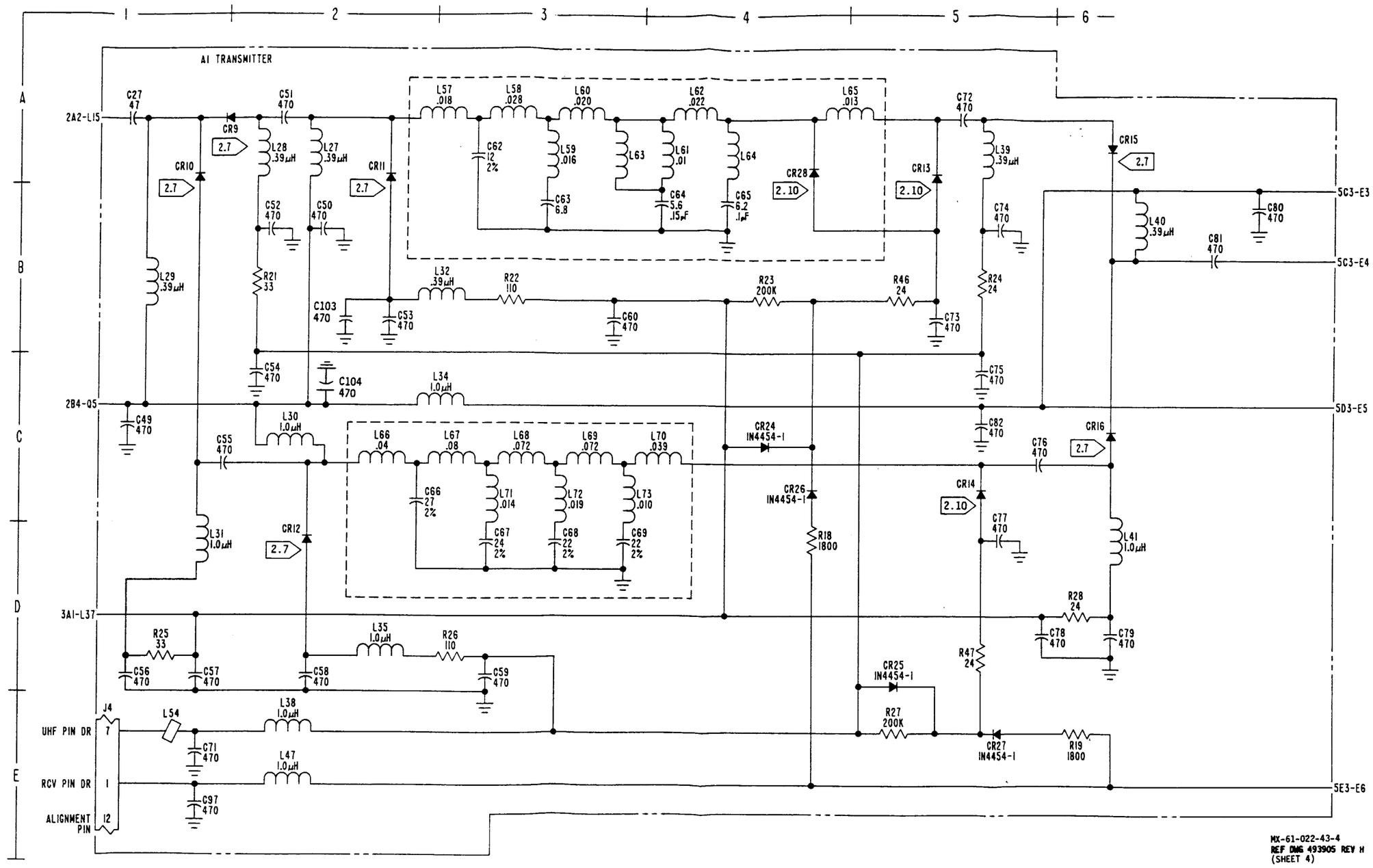
FO-7. Transmitter CCA A1A1A2
Schematic Diagram
(Sheet 1 of 5)



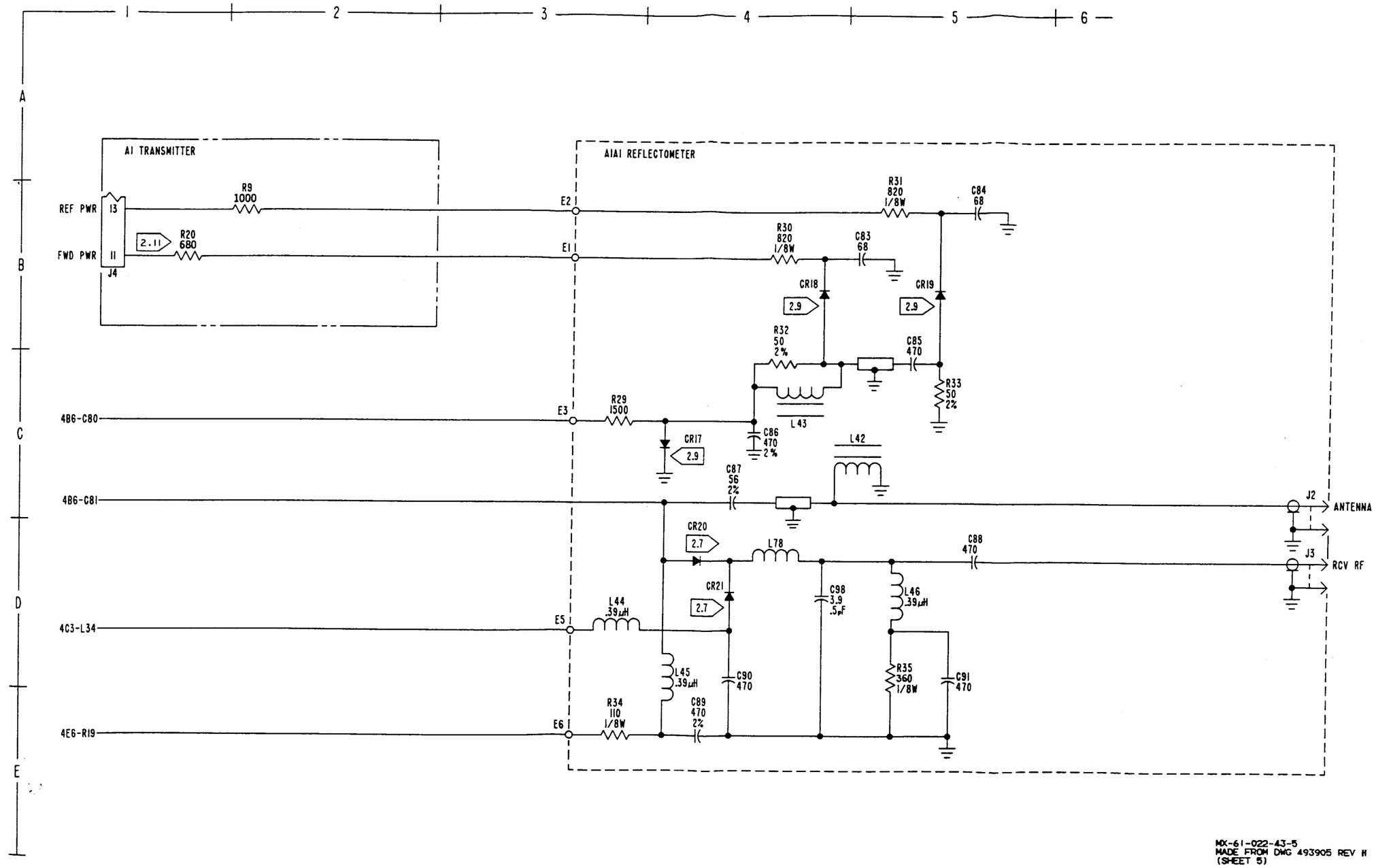
FO-7. Transmitter CCA A1A1A2
Schematic Diagram
(Sheet 2 of 5)



FO-7. Transmitter CCA A1A1A2
Schematic Diagram
(Sheet 3 of 5)



FO-7. Transmitter CCA A1A1A2
Schematic Diagram
(Sheet 4 of 5)



MX-61-022-43-5
MADE FROM DWG 493905 REV H
(SHEET 5)

FO-7. Transmitter CCA A1A1A2
Schematic Diagram
(Sheet 5 of 5)

INTEGRATED CIRCUIT TABLE		
REFERENCE DESIGNATION	SECOND TAGGING LINE SYM	PART NUMBER
U14	M1	JM38510/10103 BGX
2.8 U2,U6	M2	JM38510/12304 BEX
U1	M3	615234-901
U4,U5,U7,U10	M4	JM38510/11001 BCX
U8,U9	M5	JM38510/10102 BIX
Z1	M6	M8340105M4703JC
2.8 U11,U12	M7	JM38510/17601 BEX
U15	M8	647025-1

REF DESIGNATIONS	
HIGHEST USED	NOT USED
C91	C26 THRU 30 C45 THRU 48 C63 THRU 67 C72 THRU 76
CR36	CR12,18,19,25 CR26,29,30
J4	
L16	
Q15	
R221	R16 R39 THRU 48 R90 THRU 95 R97 R146 THRU 155 R175 THRU 183
T1	
U15	U3,13
VR11	VR3,4,9,10
Z1	

X XX X -X

- -X — PIN NUMBER
- X — SUB ZONE
- XX — DRAWING ZONE
- X — SHEET NO. OF ORIGIN OR DESTINATION

TYPICAL CIRCUIT CONTINUATION CODE

NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 5%, 1/4W.
1% RESISTORS ARE 1/8 W.
CAPACITANCE VALUES ARE IN MICROFARADS.
INDUCTANCE VALUES ARE IN MICROHENRIES.
VOLTAGES ARE DC.
DIODES AND/OR TRANSISTORS ARE JANTX TYPE.
DIODES ARE 1N4454-1.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION 1A1A1A3A1.

2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 493886.

2.4 VALUE SELECTED AT TEST. NOMINAL VALUE SHOWN.

2.5 PART NUMBER 645797-901.

2.6 PART NUMBER 619915-902.

2.7 PART NUMBER 617713-902. 2.8

2.8 THIS DEVICE REQUIRES SPECIAL HANDLING AND PROCESSING TO PREVENT DAMAGE FROM ELECTROSTATIC DISCHARGE TRANSIENTS.

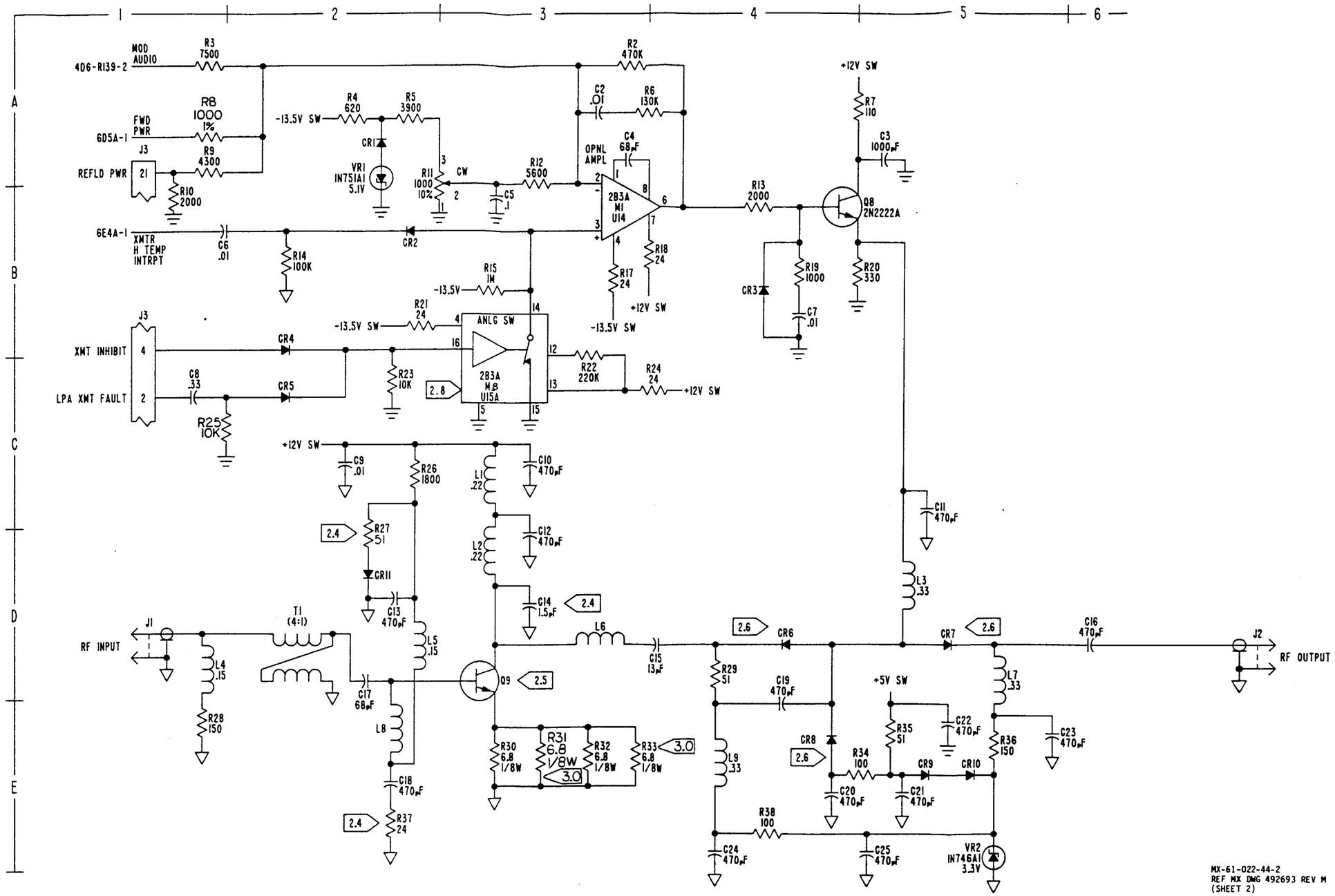
2.9 ANALOG SWITCHES ARE SHOWN IN THE AM HIGH POWER PLAIN TRANSMIT MODE.

2.10 REFERENCE:
ASSEMBLY NUMBER 811827-801.
CKT CARD ASSY 914863-801
PRINTED WIRING BOARD 412277-1.

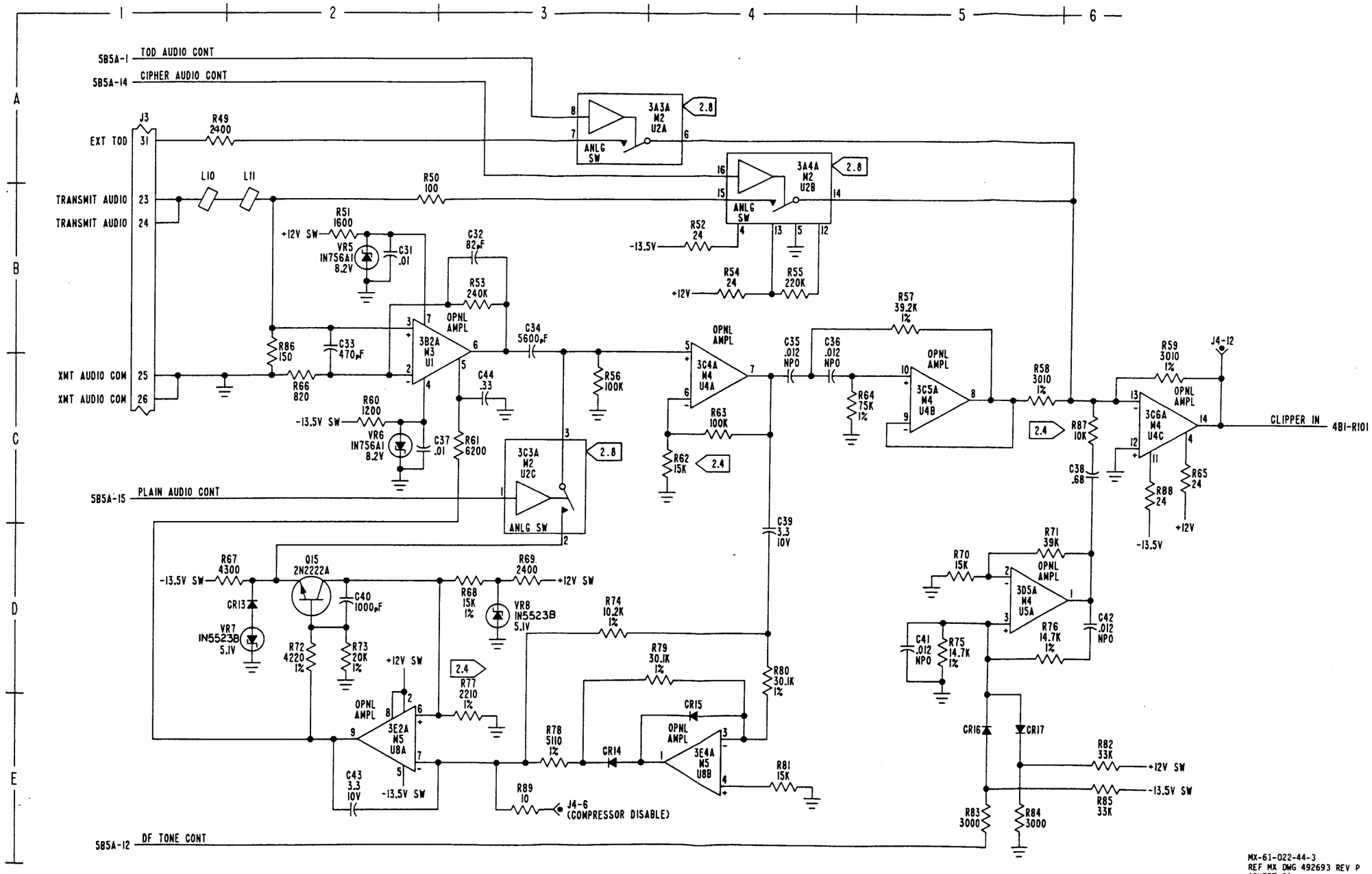
3.0 REQUIREMENT AND USAGE OF RESISTORS R31 AND R33 SHALL BE DETERMINED AT TESTING.

MX-61-022-44-1
REF MX DWG 492693 REV P
(SHEET 1)

FO-8. Modulator CCA A1A1A3A1
Schematic Diagram
(Sheet 1 of 6)

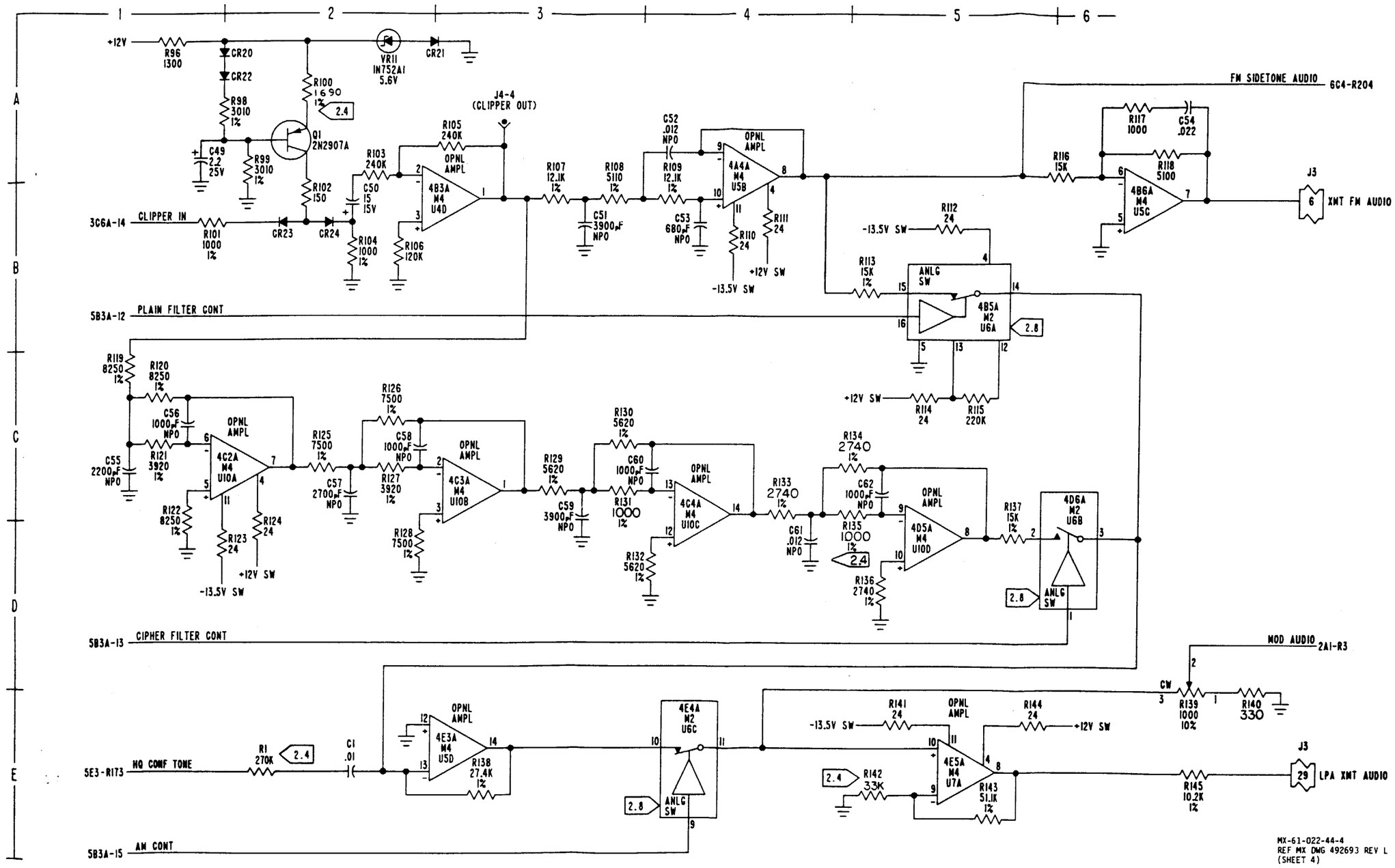


FO-8. Modulator CCA A1A1A3A1
Schematic Diagram
(Sheet 2 of 6)

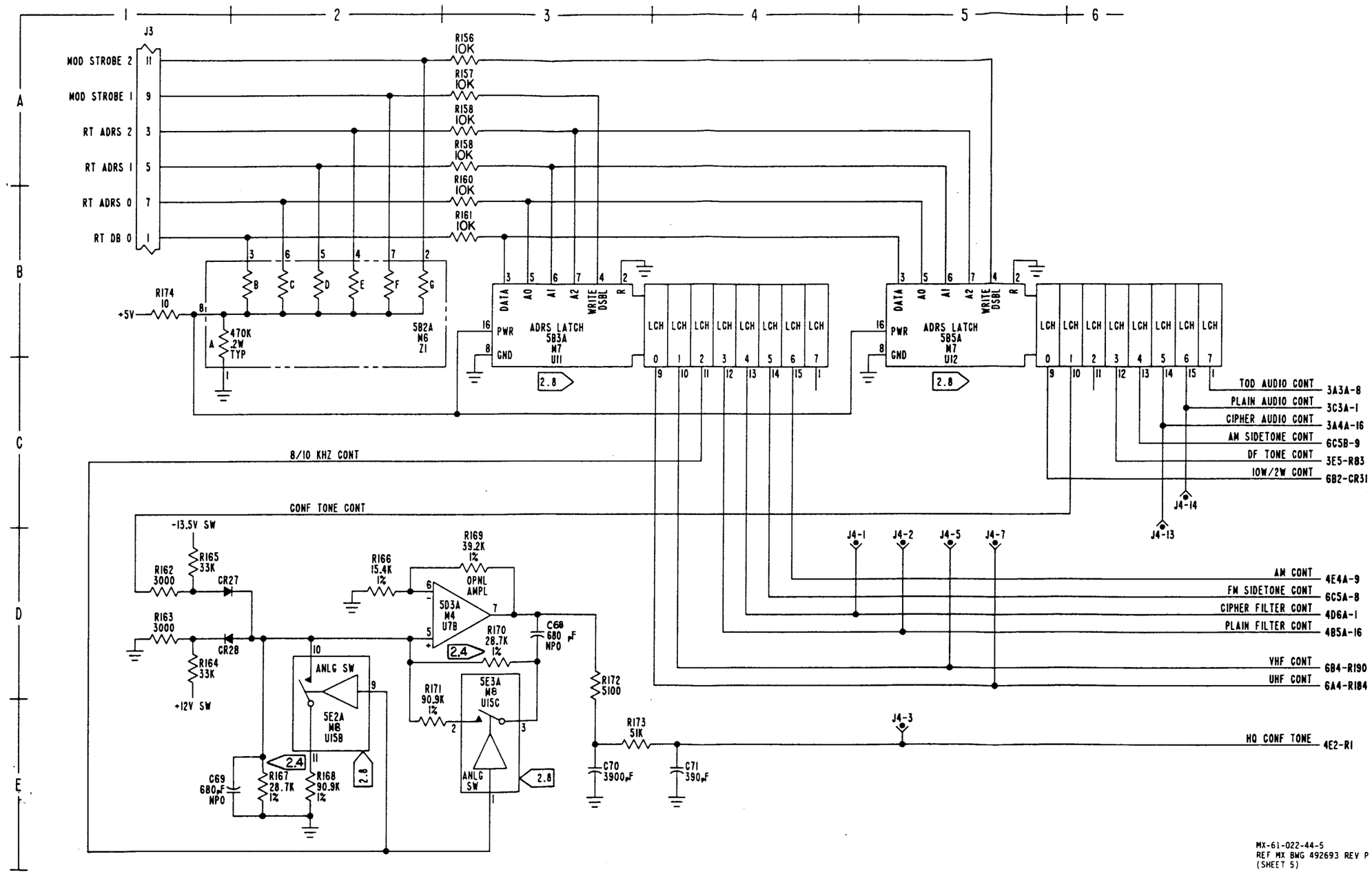


MX-61-022-44-3
REF MX DWG 492693 REV P
(SHEET 3)

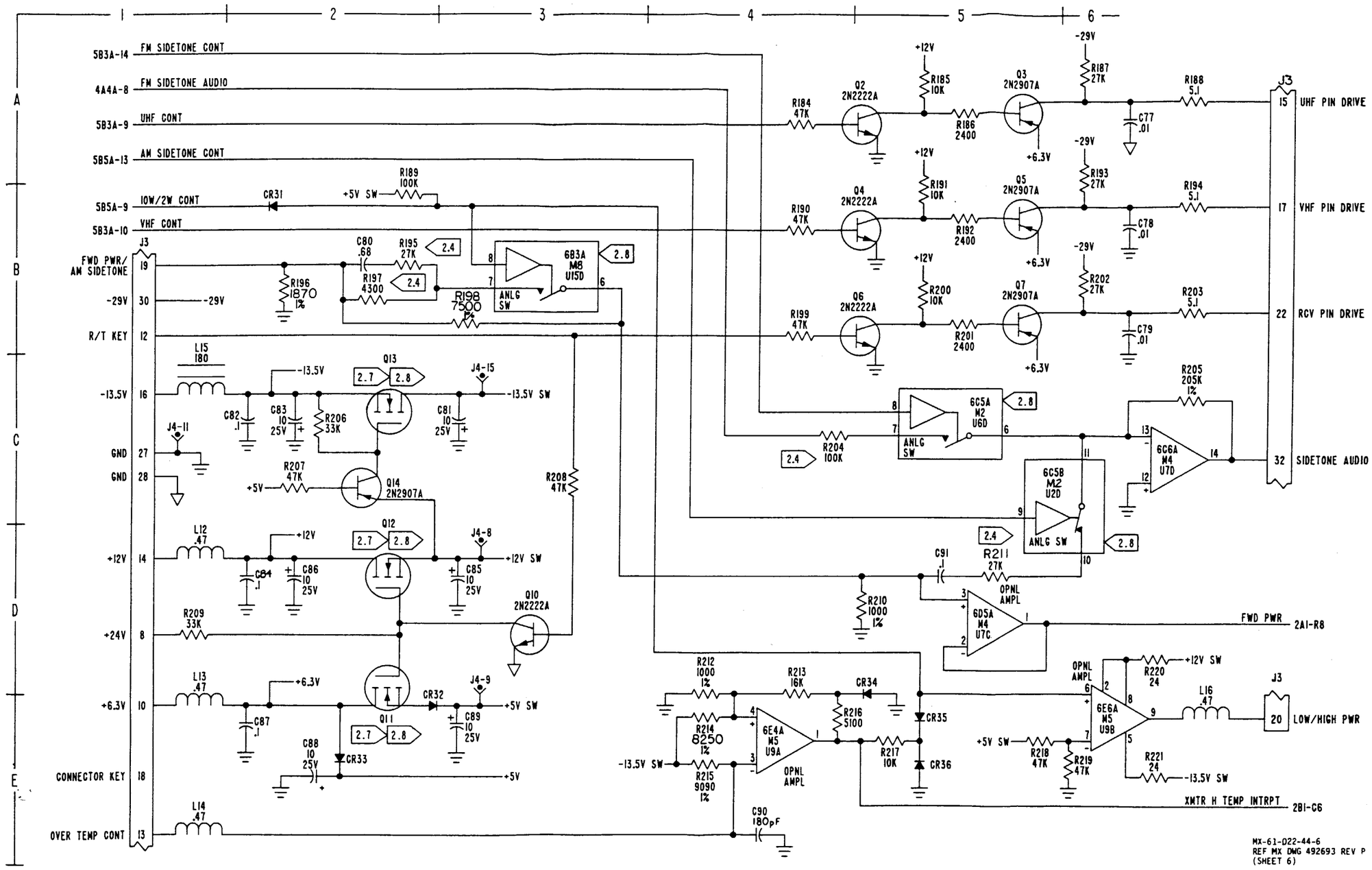
FO-8. Modulator CCA A1A1A3A1
Schematic Diagram
(Sheet 3 of 6)



FO-8. Modulator CCA A1A1A3A1
Schematic Diagram
(Sheet 4 of 6)



FO-8. Modulator CCA A1A1A3A1
Schematic Diagram
(Sheet 5 of 6)

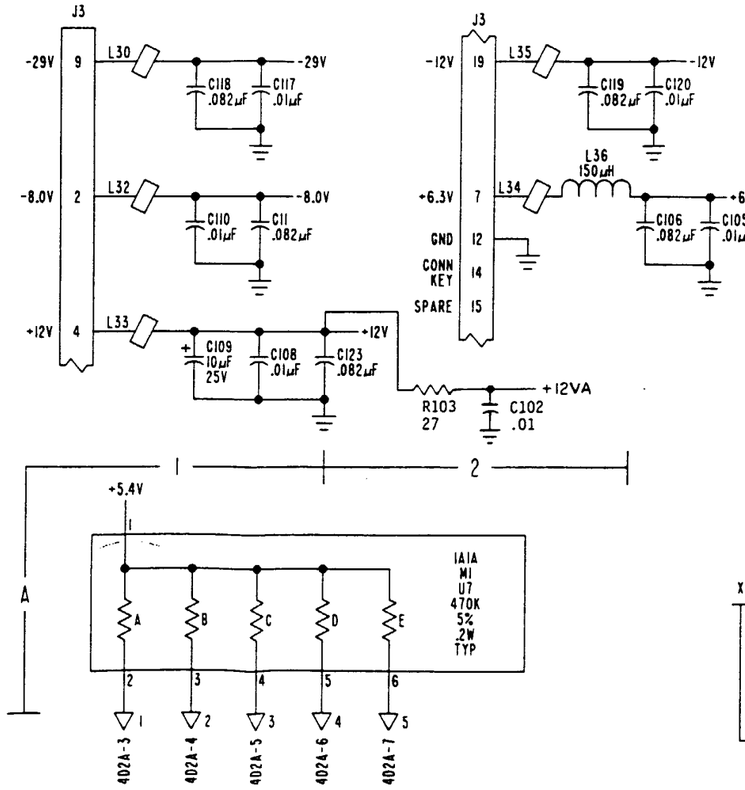


FO-8. Modulator CCA A1A1A3A1
Schematic Diagram
(Sheet 6 of 6)

REF DESIGNATION	
ASSY 811826-801	
HIGHEST USED	NOT USED
A1	
A1 ASSY 914864-801	
C146	C59-63,76, 97-99,101-103, 114,126,127, 129-131,138, 139,141,143,
CR67	CR36-39,42, 46,48-50, 61-63
FL1	
J3	
L44	L23,24,26
Q11	Q5,6,9
R133	R37,39,40,43, 47,62,74,75,78, 81-83,95,113, 120
RT5	
T2	
TP10	TP7
U7	
Y1	
Z1	

REF DESIGNATION	
ASSY 811826-803	
HIGHEST USED	NOT USED
A1	
A1 ASSY 914864-803	
C146	C76,97-99,101 -103,114,126, 127,129-131, 138,139,141, 143,
CR67	CR42,46, 48-50, 61-63
FL2	
J3	
L44	L26
Q11	Q5,6,9
R133	R37,43,47,62, 74,75,78,81-83, 95,113,120
RT5	
T2	
TP10	TP7
U7	
Y1	
Z1	

INTEGRATED CIRCUIT TABLE							
REF DES	SECOND TAGGING LINE SYM	PART NUMBER	POWER INPUT PINS				
			+5.4V	+6.3V	+12V	-12V	GND
U7	M1	M8340104M4703JC	(1)	NA	NA	NA	NA
	M2						
U4,5	M3	JM38510/11001BCX	NA	NA	(4)	(11)	NA
U2	M4	616594-901	NA	(4)	NA	NA	(15)
U3	M5	617714-902	NA	NA	NA	NA	(17)
2.12 U6	M6	617761-1	(16)	NA	(13)	(4)	(5)
2.12 U1	M7	JM38510/17601BEX	(16)	NA	NA	NA	(8)



NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 5%, 1/4W.
CAPACITANCE VALUES ARE IN PICOFARADS.
VOLTAGES ARE DC.
DIODES AND/OR TRANSISTORS ARE JANTX TYPE.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION 1A1A1A4A1.

2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 493886.

2.4 PART NUMBER JANTX3N204

2.5 PART NUMBER 615238-905.

2.6 PART NUMBER JANTX1N5712

2.7 PART NUMBER 616543-902

2.8 PART NUMBER 619915-901.

2.9 PART NUMBER 646264-901.

2.10 FOR ASSEMBLY -801 ONLY.

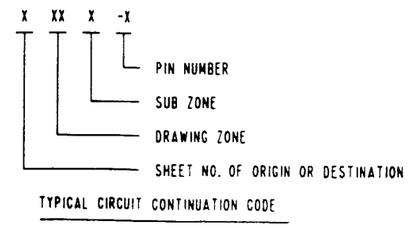
2.11 FOR ASSEMBLY -803 ONLY.

2.12 THIS DEVICE REQUIRES SPECIAL HANDLING AND PROCESSING TO PREVENT DAMAGE FROM ELECTROSTATIC DISCHARGE TRANSIENTS.

2.13 VALUE SELECTED AT TEST, NOMINAL VALUE SHOWN.

2.14 REFERENCE:
ASSEMBLY NUMBER 811826-801.
A1 ASSEMBLY NUMBER 914864-801.
PRINTED WIRING BOARD 410899-1.
ASSEMBLY NUMBER 811826-803.
A1 ASSEMBLY NUMBER 914864-803.
PRINTED WIRING BOARD 410899-1.

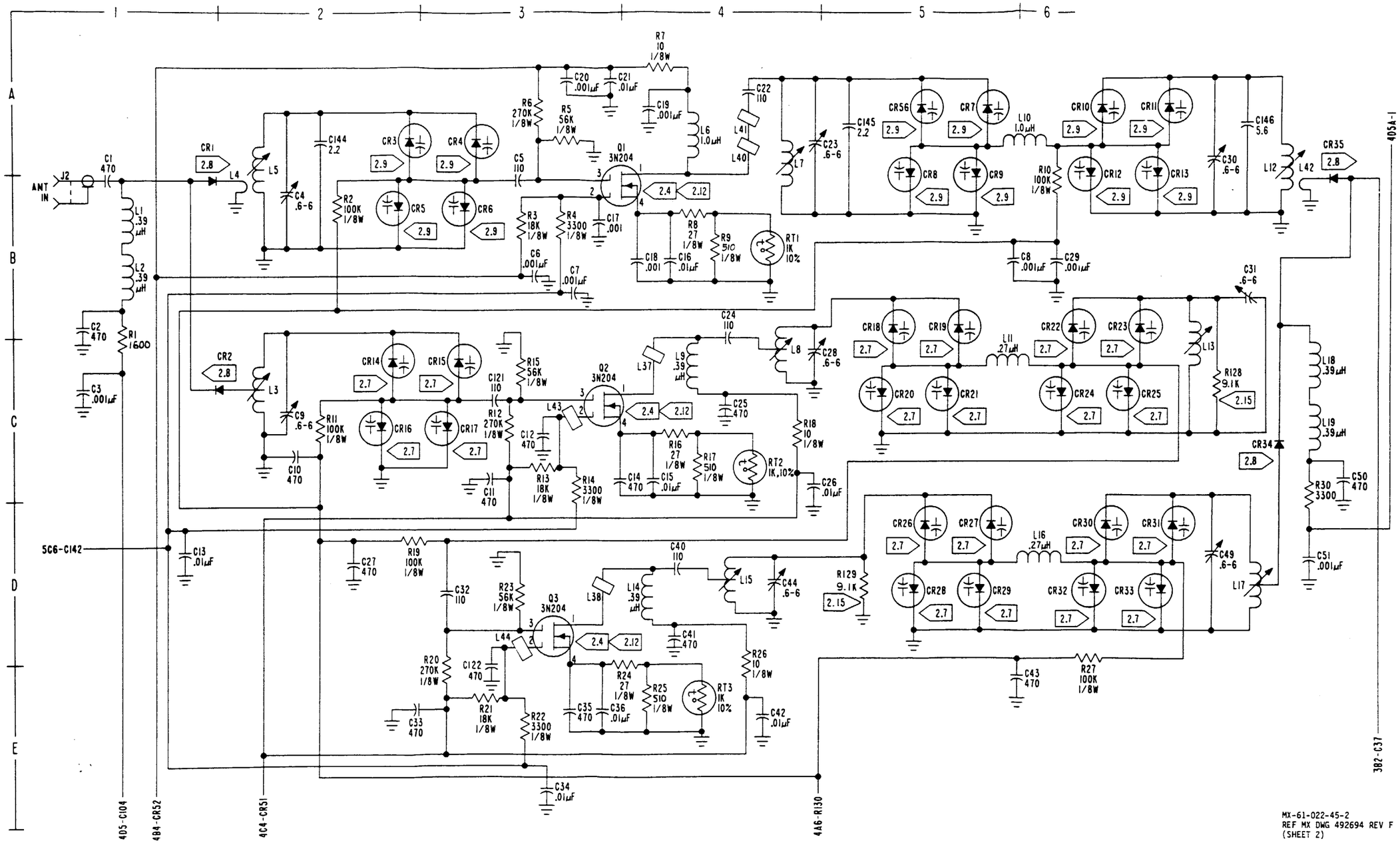
2.15 REFER TO ALIGNMENT/TEST PROCEDURE 978944 FOR INSTALLATION OF R128 AND R129.



TYPICAL CIRCUIT CONTINUATION CODE

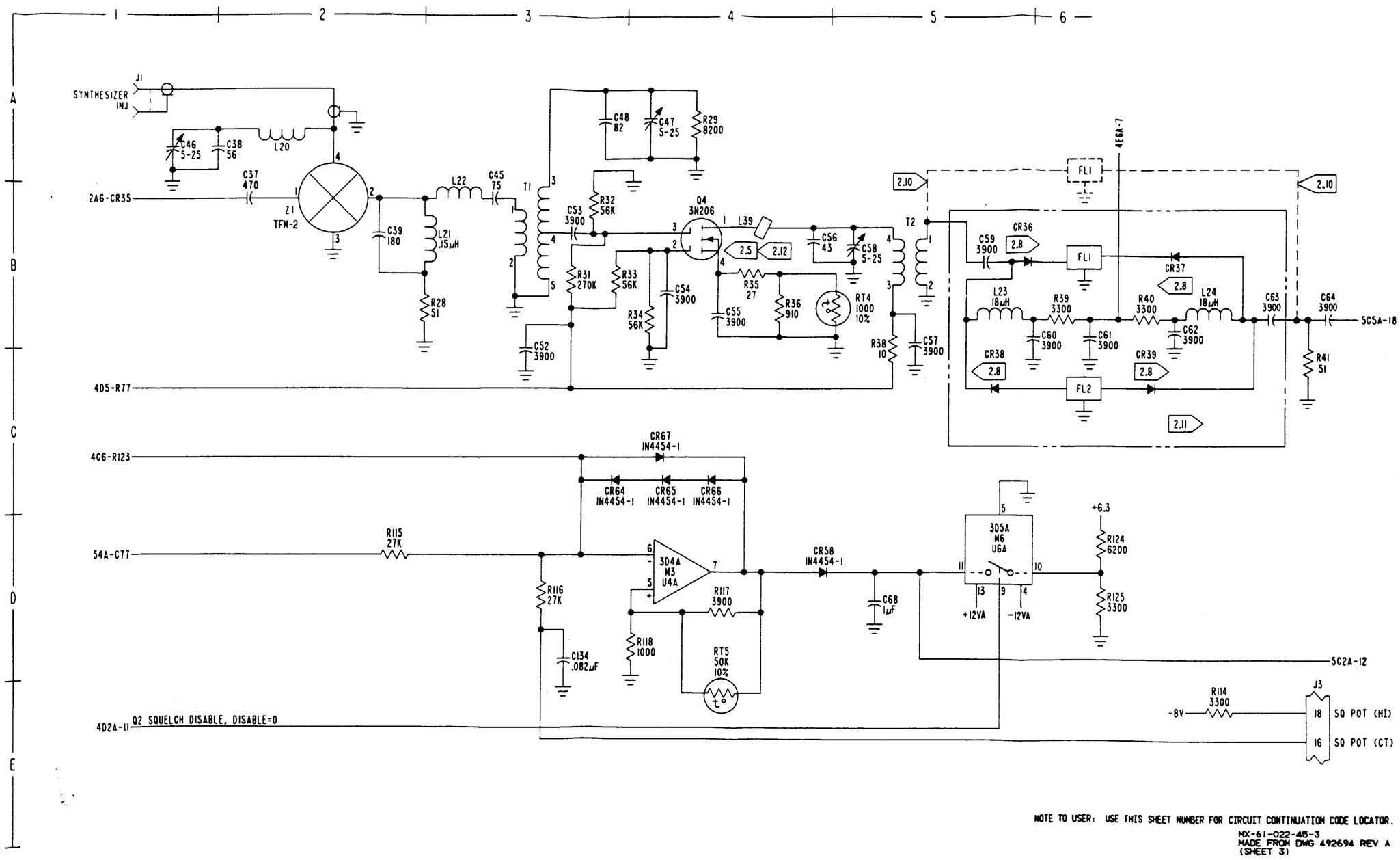
MX-61-022-45-1
REF MX DWG 492694 REV F
(SHEET 1)

FO-9. Main Receiver CCA A1A1A4A1 Schematic Diagram (Sheet 1 of 5)



MX-61-022-45-2
REF MX DWG 492694 REV F
(SHEET 2)

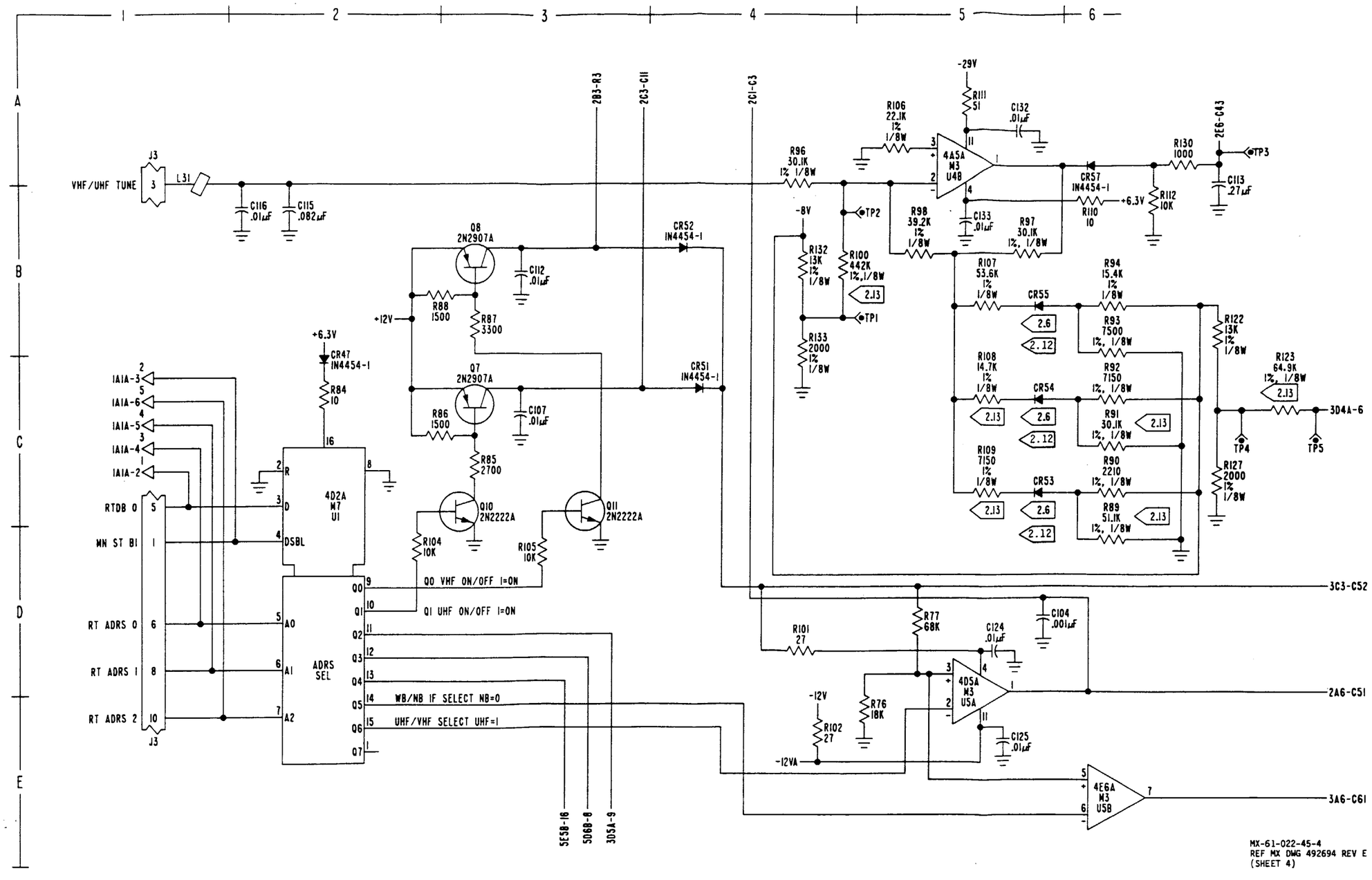
FO-9. Main Receiver CCA A1A1A4A1
Schematic Diagram (Sheet 2 of 5)



NOTE TO USER: USE THIS SHEET NUMBER FOR CIRCUIT CONTINUATION CODE LOCATOR.

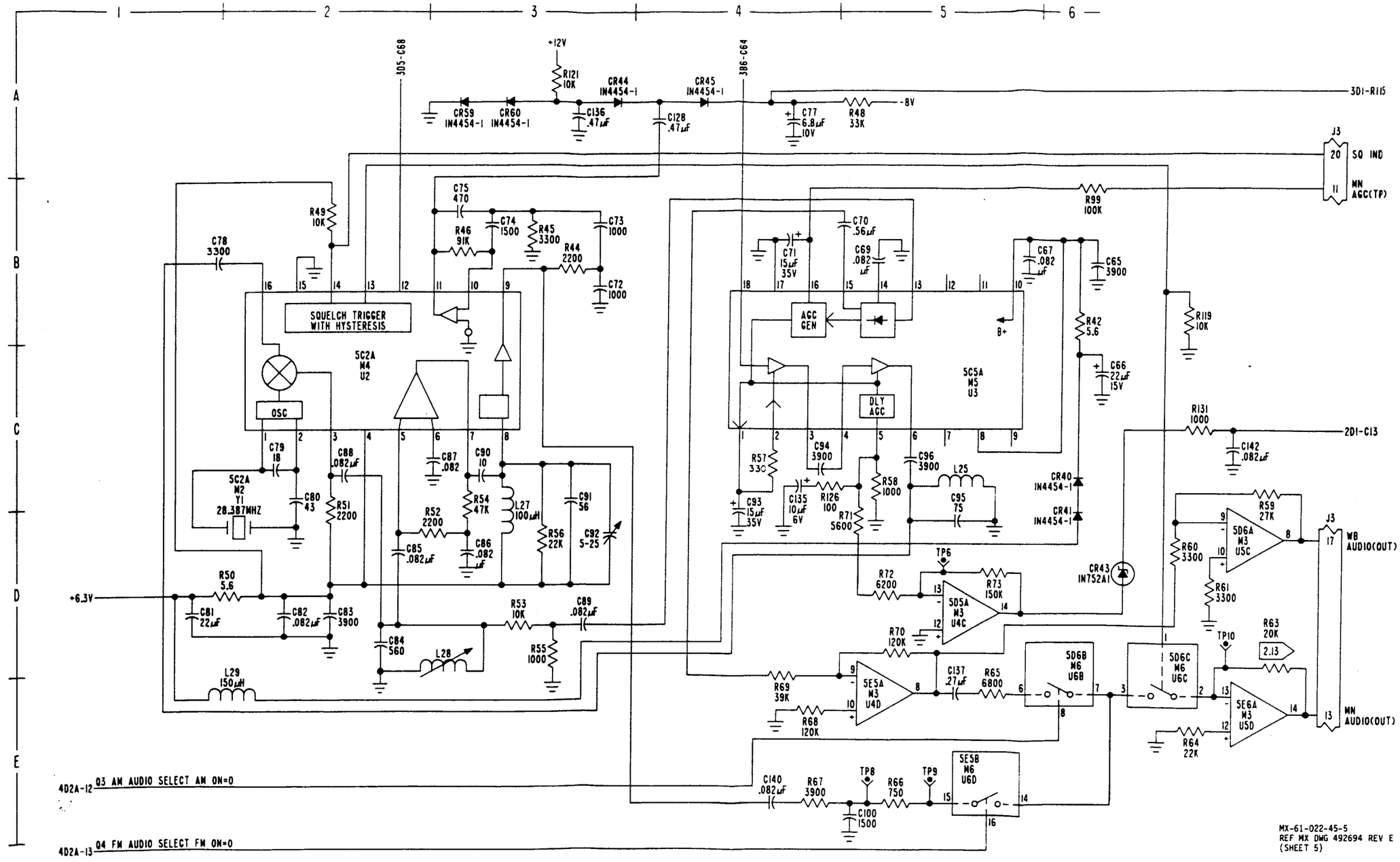
MX-61-022-45-3
MADE FROM DWG 492694 REV A
(SHEET 3)

FO-9. Main Receiver CCA A1A1A4A1
Schematic Diagram (Sheet 3 of 5)



MX-61-022-45-4
REF MX DWG 492694 REV E
(SHEET 4)

FO-9. Main Receiver CCA A1A1A4A1 Schematic Diagram (Sheet 4 of 5)



FO-9. Main Receiver CCA A1A1A4A1 Schematic Diagram (Sheet 5 of 5)

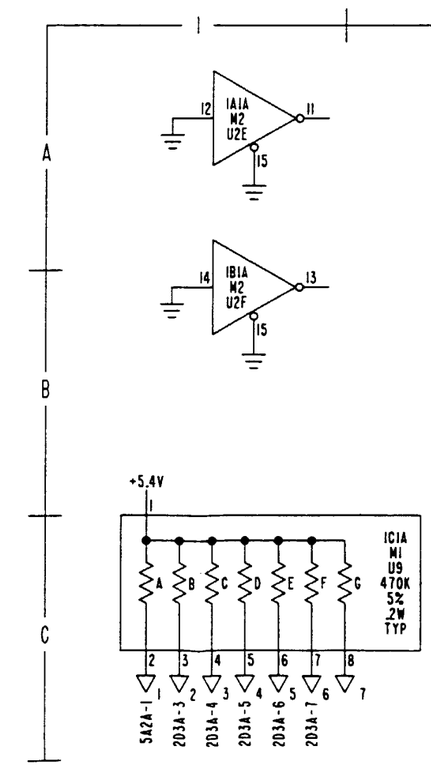
REF DESIGNATION	
ASSY 811955-801	
HIGHEST USED	NOT USED
A1	
A1 ASSY 914865-801	
C112	C1,2,13, 17-19,23, 47-54,65, 94,106, 109,111
CR20	CR1,2,11,12,13
FL1	
J3	
L28	L1,2,8
Q9	Q2,7
R115	R8-16,23,35-37, 40,43-46, 49-51,76,90
RT4	RT2,3
T1	
TP10	TP2,3,4,9
U9	U3,4
Y2	

REF DESIGNATION	
ASSY 811955-802	
HIGHEST USED	NOT USED
A1	
A1 ASSY 914865-802	
HIGHEST USED	NOT USED
C112	C1,2,13, 17-19,23, 94,106,109, 111
CR20	CR1,2,11,12,13
FL1	
J3	
L28	L1,2,8
Q9	Q2,7
R115	R8-16,23,40,76
RT4	RT2,3
T1	
TP14	TP2,3,4,9
U9	
Y2	

2.8 VALUE SELECTED AT TEST, NOMINAL VALUE SHOWN.

2.9 REFER TO TEST SPEC 978942 FOR INSTALLATION OF C112.

INTEGRATED CIRCUIT TABLE						
REF DES	SECOND TAGGING LINE SYM	PART NUMBER	POWER INPUT PINS +5.4V	+12V	-12V	GND
U9	M1	M8340105M4703JC	(1)	NA	NA	NA
2.5 U2	M2	615699-903	16	NA	NA	8
U7,8	M3	JM38510/11001BCX	NA	(4)	(11)	NA
U6	M4	616594-901	NA	NA	NA	(15)
U5	M5	617714-902	NA	NA	NA	(17)
2.5 U1	M6	JM38510/17601BEX	(16)	NA	NA	(8)
2.6 U3,4	M7	616386-903	NA	NA	NA	(7)



NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 5%, 1/4W.
CAPACITANCE VALUES ARE IN PICOFARADS.
VOLTAGES ARE DC.
DIODES AND/OR TRANSISTORS ARE JANTX TYPE.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION 1A1A1A5.

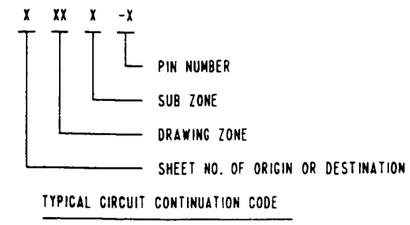
2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 493886.

2.4 PART NUMBER JANTX3N204

2.5 THIS DEVICE REQUIRES SPECIAL HANDLING AND PROCESSING TO PREVENT DAMAGE FROM ELECTROSTATIC DISCHARGE TRANSIENTS.

2.6 USED IN ASSEMBLY 811955-802 (914865-802) ONLY.

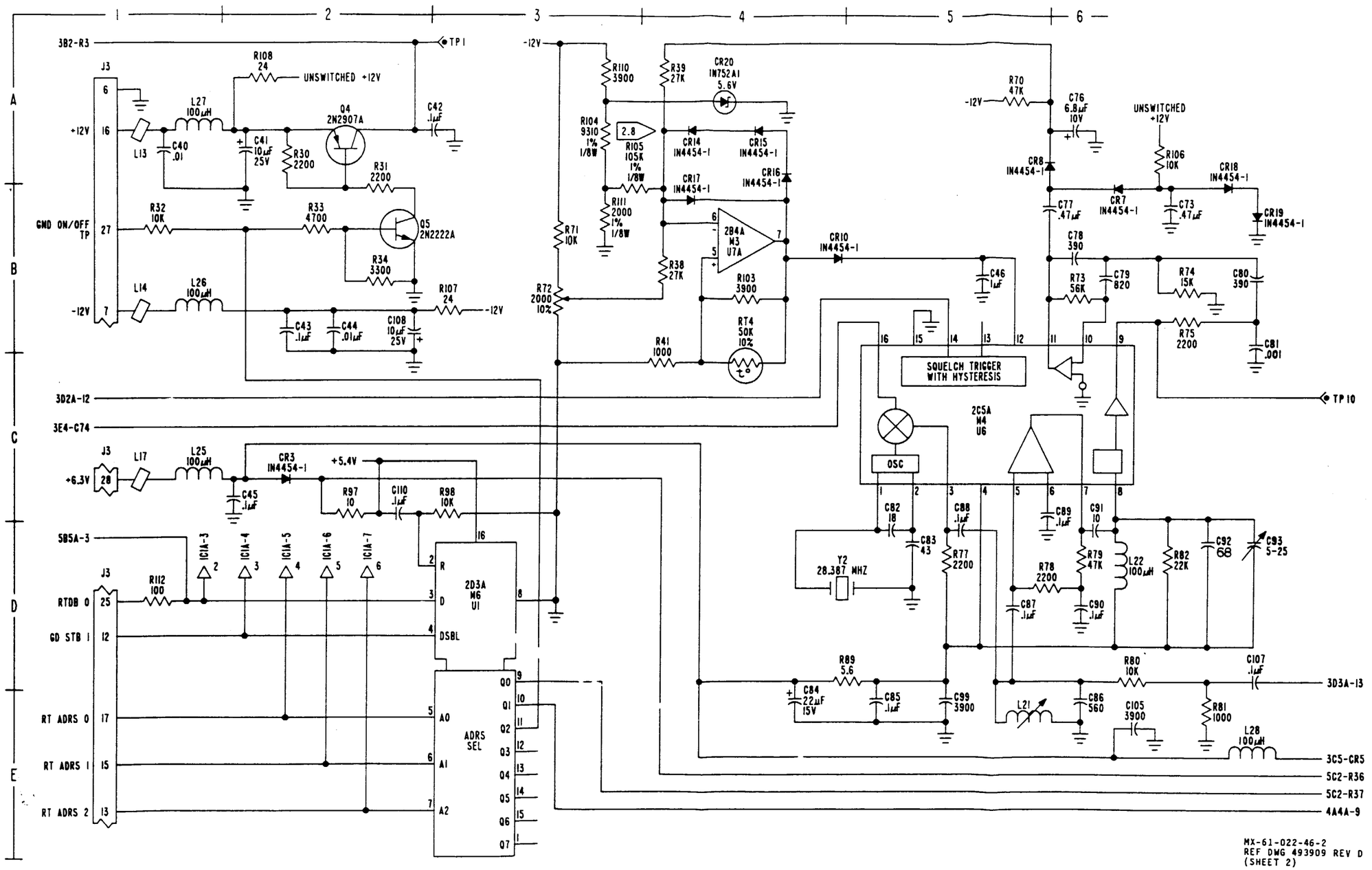
2.7 REFERENCE:
ASSEMBLY NUMBER 811955-801.
A1 ASSEMBLY NUMBER 914865-801.
PRINTED WIRING BOARD 410900-1.
TEST SPEC 978942
ASSEMBLY NUMBER 811955-802
A1 ASSEMBLY NUMBER 914865-802
PRINTED WIRING BOARD 410900-1
TEST SPEC 978942



TYPICAL CIRCUIT CONTINUATION CODE

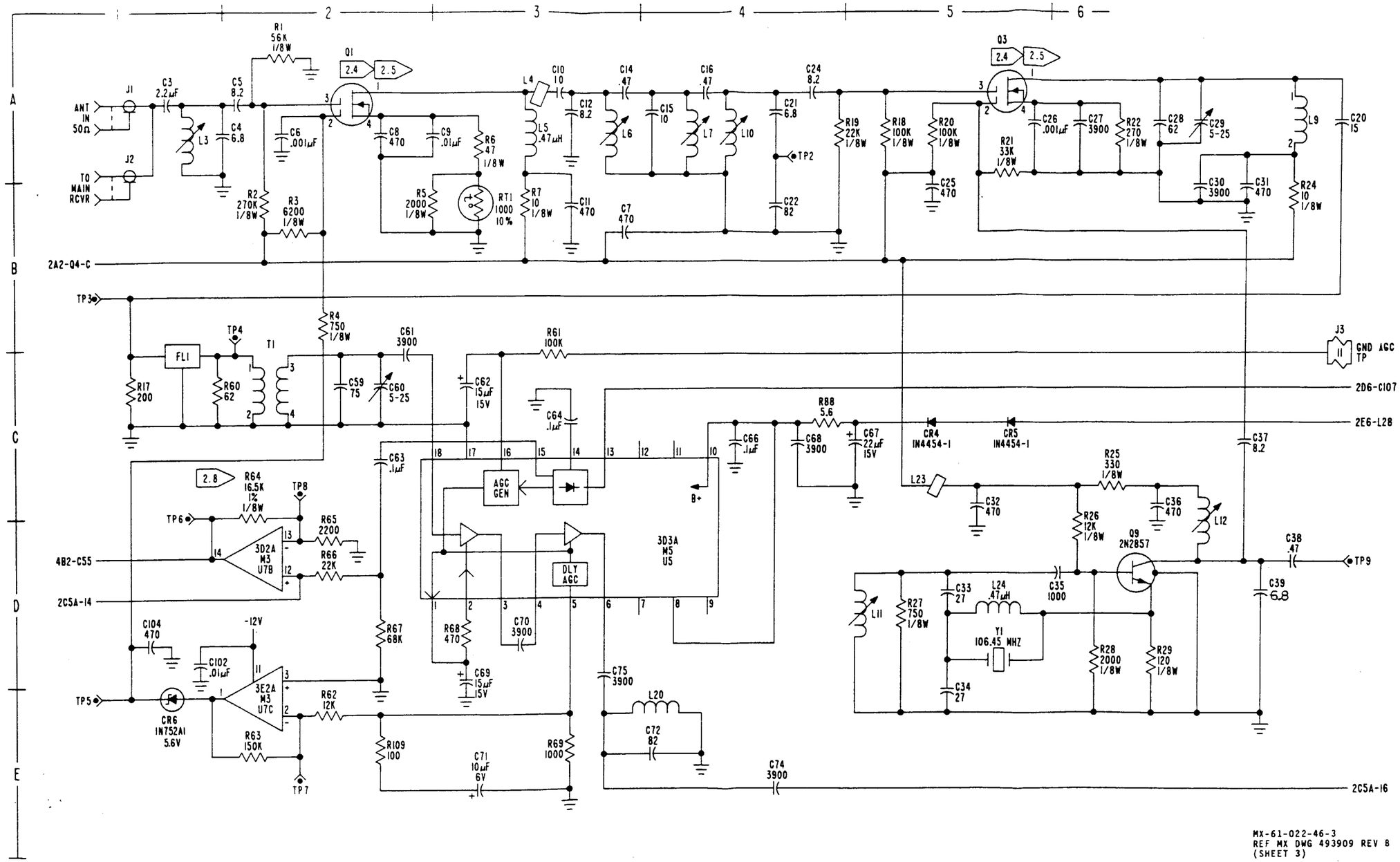
MX-61-022-46-1
REF MX DWG 493909 REV D
(SHEET 1)

FO-10. Guard Receiver CCA A1A1A5A1 Schematic Diagram (Sheet 1 of 5)



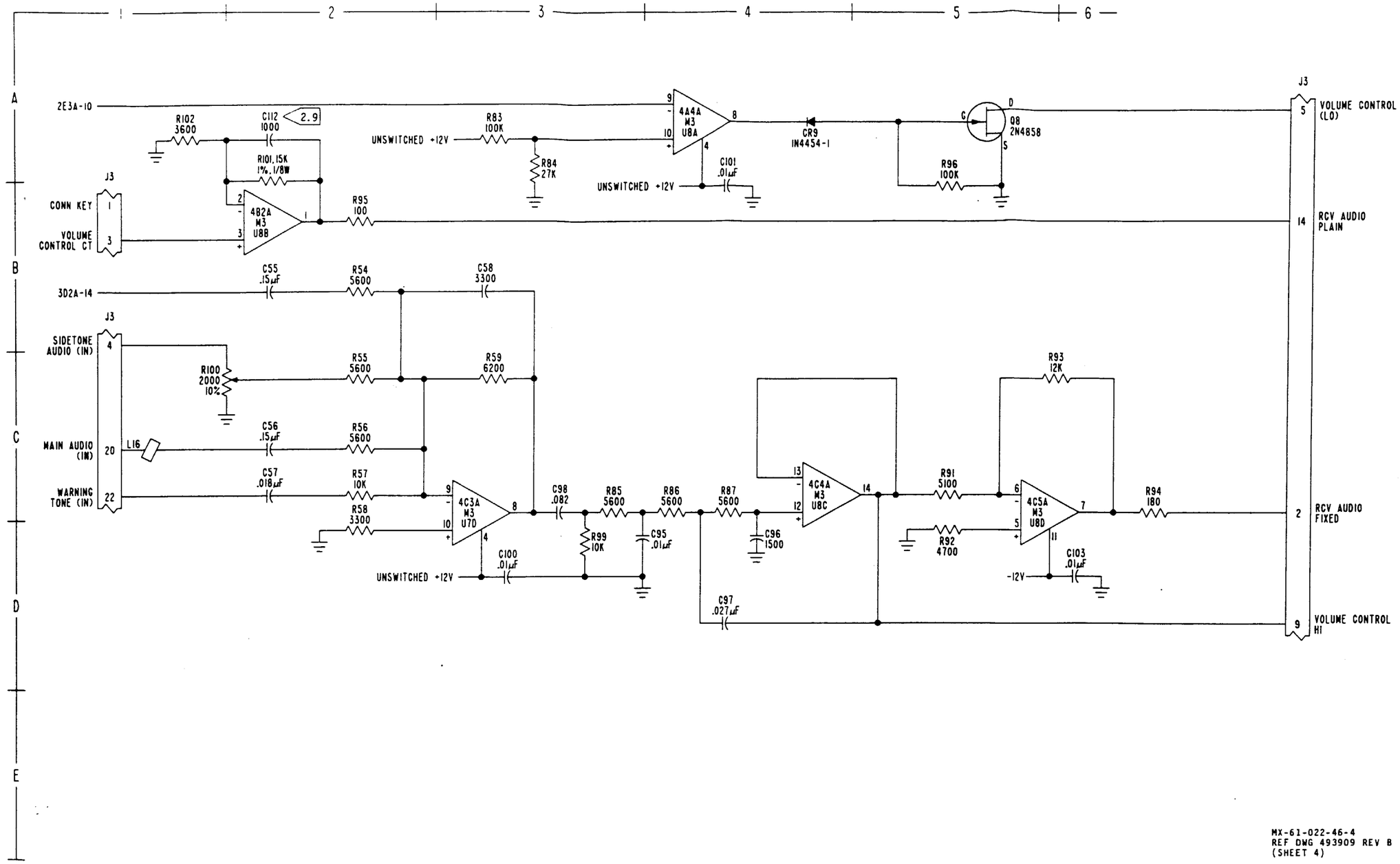
MX-61-022-46-2
REF DWG 493909 REV D
(SHEET 2)

FO-10. Guard Receiver CCA A1A1A5A1
Schematic Diagram
(Sheet 2 of 5)



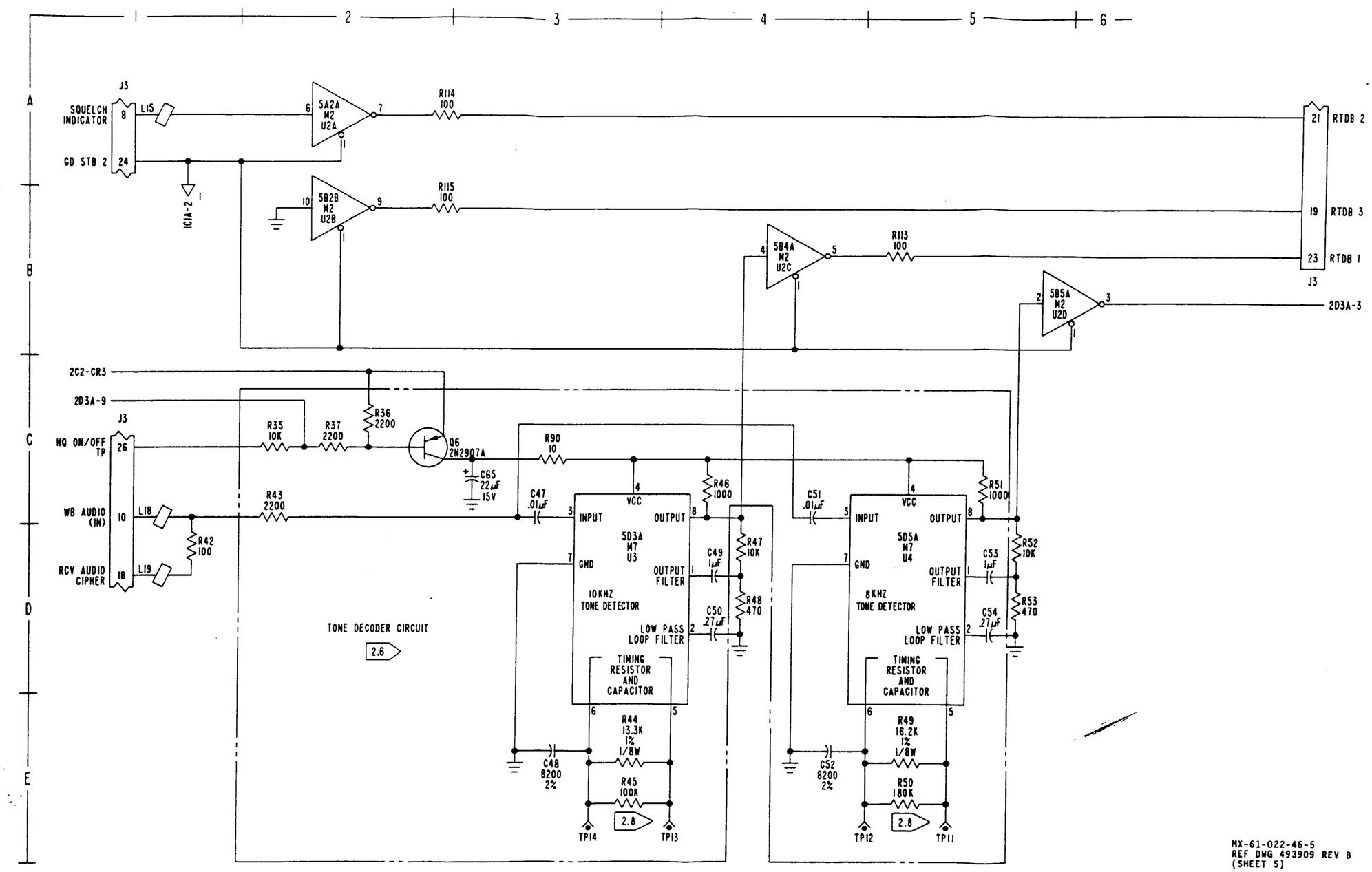
MX-61-022-46-3
REF MX DWG 493909 REV B
(SHEET 3)

FO-10. Guard Receiver CCA A1A1A5A1
Schematic Diagram
(Sheet 3 of 5)



MX-61-022-46-4
REF DWG 493909 REV B
(SHEET 4)

FO-10. Guard Receiver CCA A1A1A5A1
Schematic Diagram
(Sheet 4 of 5)



MX-61-022-46-5
REF DWG 493909 REV B
(SHEET 5)

FO-10. Guard Receiver CCA A1A1A5A1 Schematic Diagram (Sheet 5 of 5)

INTEGRATED CIRCUIT TABLE		
REFERENCE DESIGNATION	SECOND TAGGING LINE SYM	PART NUMBER
U3	M1	M8340105M4703JC
U5	M3	JM38510/11001 BCX
U10	M4	616194-901
U14	M5	616195-910
U11	M6	616385-901
2.9 U13	M7	616501-902
2.9 U7	M8	JM38510/12304 BEX
2.9 U4	M9	617763-901
U9	M10	619604-903
2.9 U2	M11	JM38510/17601 BEX
2.9 U1	M12	645794-901
Y1	M13	626164-4
Z1	M14	626730-1
Z2	M15	815016-801

X XX X -X

- PIN NUMBER
- SUB ZONE
- DRAWING ZONE
- SHEET NO. OF ORIGIN OR DESTINATION

TYPICAL CIRCUIT CONTINUATION CODE

REF DESIGNATIONS	
HIGHEST USED	NOT USED
C103	C2,77
CR28	CR7,24
E9	
FL1	
J4	
L23	L2,3,10,16
Q14	
R145	R21,22,29, 30,33-35, 48,49,51, 53-57,65, 84,87,123, 124,132,133, 141
T5	
TP5	
U14	U8,12,6
Y1	
Z2	

NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

1.3 A NUMBER SIGN (#) FOLLOWING A SIGNAL NAME MEANS THE INVERTED (NOT) FORM OF THE SIGNAL.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 5%, 1/4W.
CAPACITANCE VALUES ARE IN PICOFARADS.
VOLTAGES ARE DC.
DIODES AND/OR TRANSISTORS ARE JANTX TYPE.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION A1A1A6A1.

2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 493910.

2.4 VALUE SELECTED AT TEST, NOMINAL VALUE SHOWN.

2.5 PART NUMBER 615468-902.

2.6 PART NUMBER 616380-901.

2.7 PART NUMBER 619915-901.

2.8 PART NUMBER 645796-901.

2.9 THIS DEVICE REQUIRES SPECIAL HANDLING AND PROCESSING TO PREVENT DAMAGE FROM ELECTROSTATIC DISCHARGE TRANSIENTS.

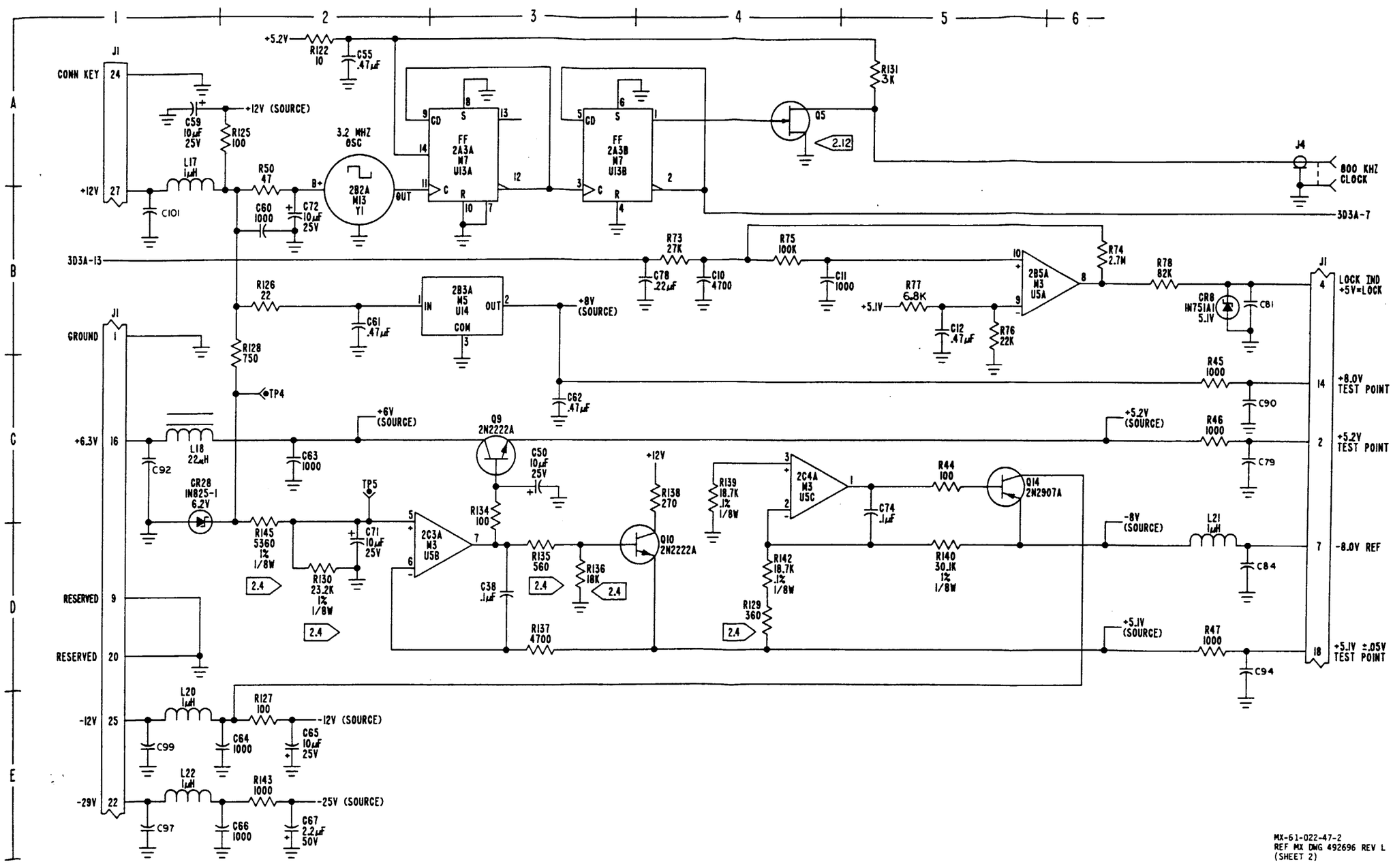
2.10 REFERENCE:
ASSEMBLY NUMBER 914866-801, -802.
PRINTED WIRING BOARD 410901-1.
TEST SPECIFICATION 575324.
CONTROL SPECIFICATION 575122.

2.11

2.12 PART NUMBER 645733-901

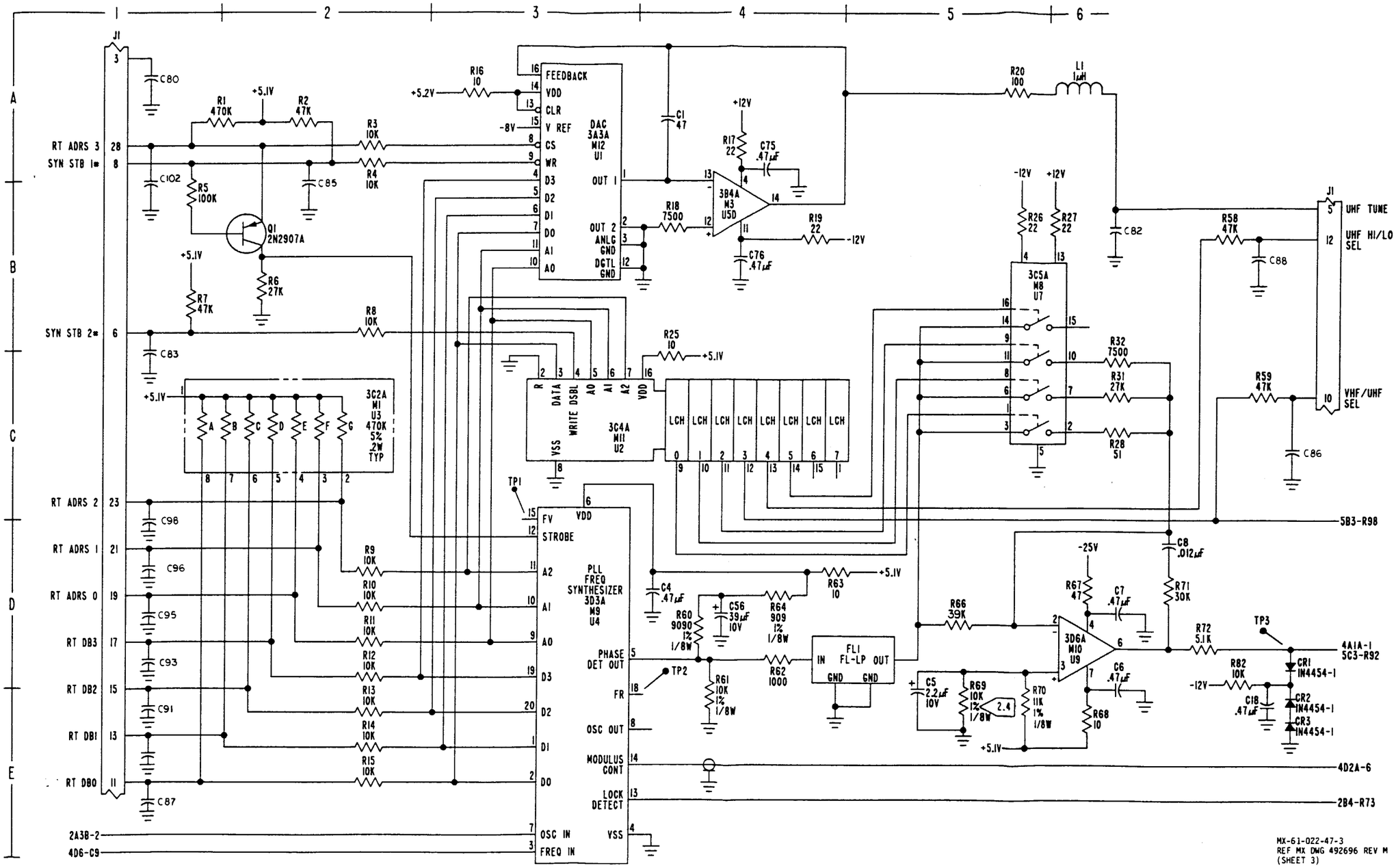
MX-61-022-47-1
REF MX DWG 492696 REV N
(SHEET 1)

FO-11. Synthesizer CCA A1A1A1A6A1 Schematic Diagram (Sheet 1 of 5)

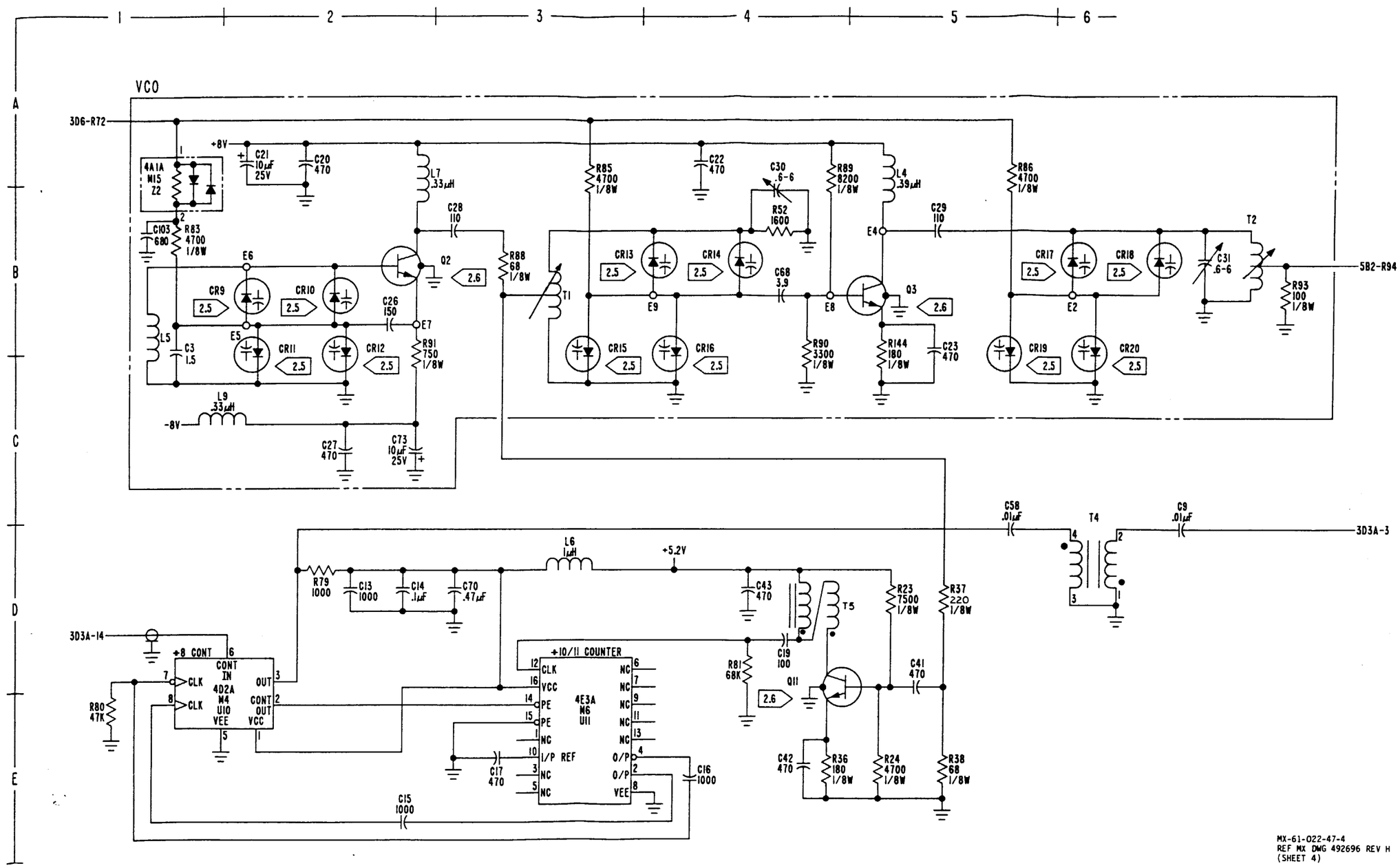


MX-61-022-47-2
REF MX DWG 492696 REV L
(SHEET 2)

FO-11. Synthesizer CCA A1A1A1A6A1 Schematic Diagram (Sheet 2 of 5)

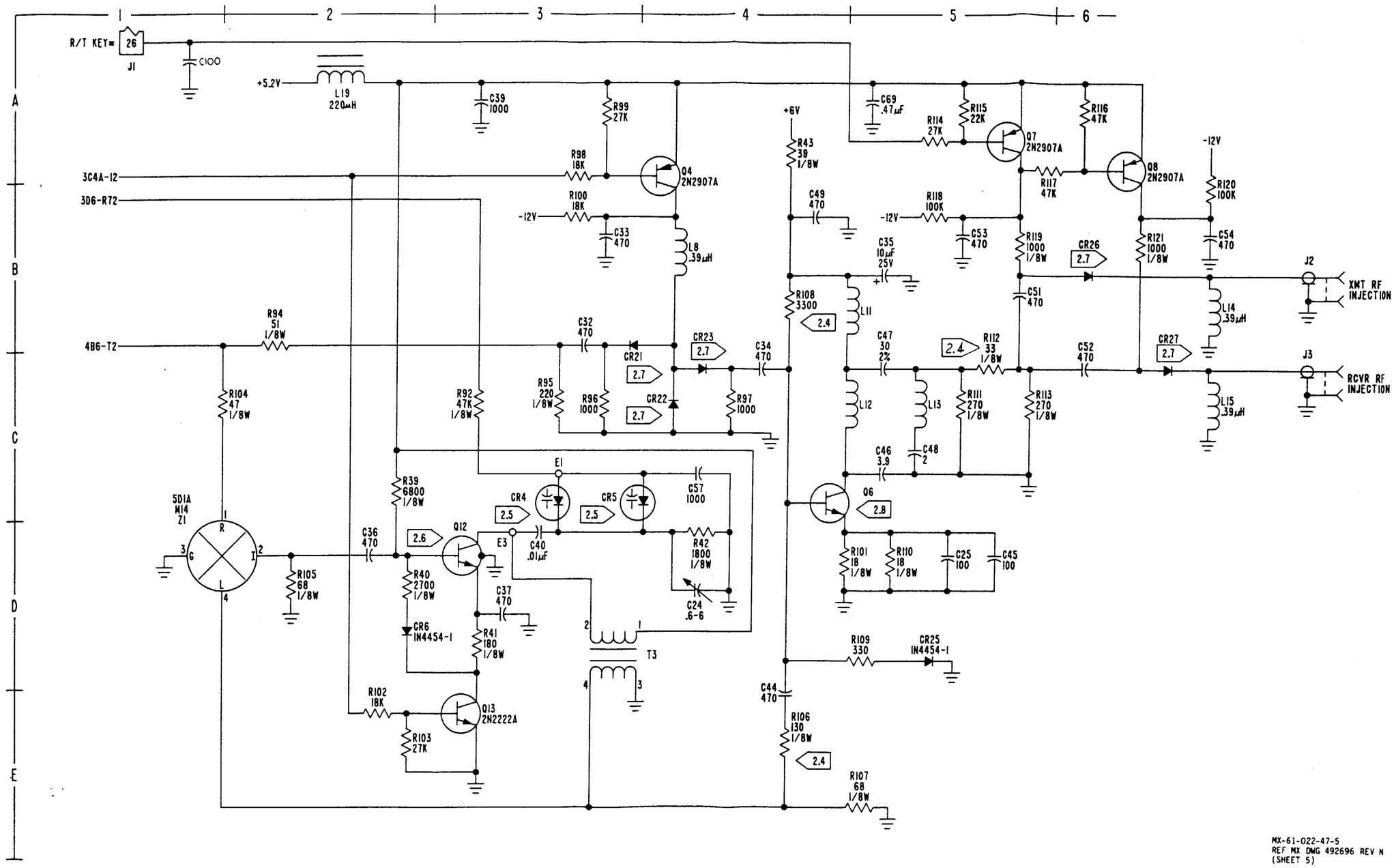


FO-11. Synthesizer CCA A1A1A1A6A1
Schematic Diagram (Sheet 3 of 5)



MX-61-022-47-4
REF MX DWG 492696 REV H
(SHEET 4)

FO-11. Synthesizer CCA A1A1A1A6A1 Schematic Diagram (Sheet 4 of 5)



MX-61-022-47-5
REF MX DWG 492696 REV N
(SHEET 5)

FO-11. Synthesizer CCA A1A1A1A6A1 Schematic Diagram (Sheet 5 of 5)

NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 5%, 1/4W.
CAPACITANCE VALUES ARE IN MICROFARADS.
VOLTAGES ARE DC.
DIODES AND/OR TRANSISTORS ARE JANTX TYPE.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION 1A1A1A7.

2.3 FOR CONTINUATION OF CIRCUIT SEE SCHEMATIC 493886.

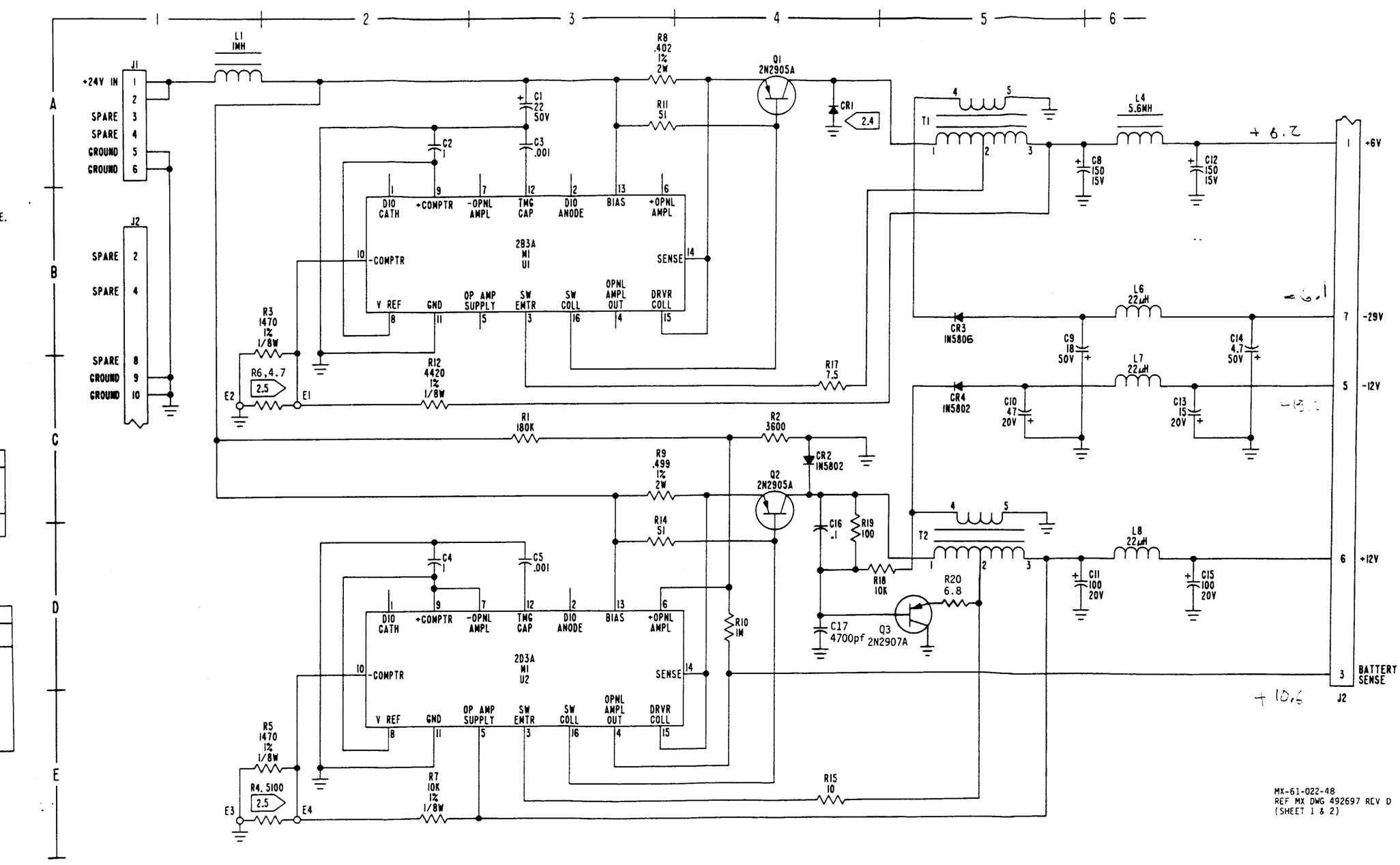
2.4 PART NUMBER 616689-903.

2.5 VALUE SELECTED AT TEST, NOMINAL VALUE SHOWN.

2.6 REFERENCE:
ASSEMBLY NUMBER 914874-801.
PRINTED WIRING BOARD 410907-1.

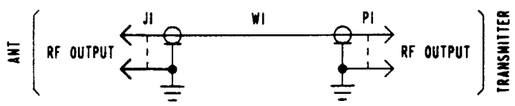
INTEGRATED CIRCUIT TABLE		
REF DES.	SECOND TAGGING LINE SYM	PART NO.
U1, 2	M1	616400-901

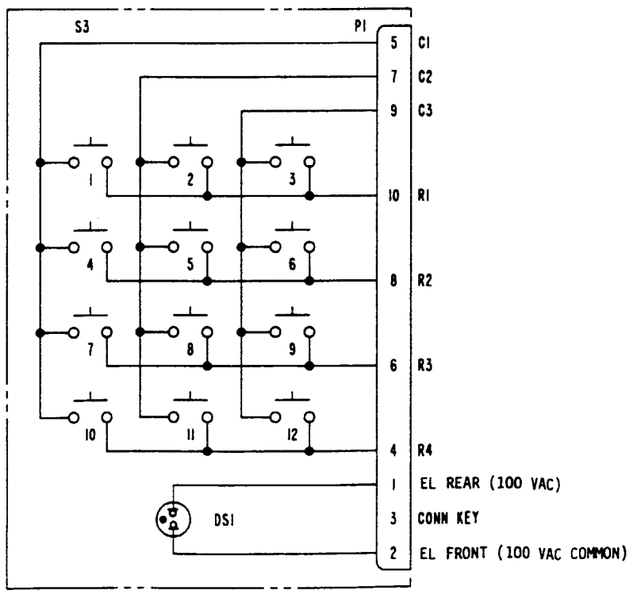
REF DES.	
HIGHEST USED	NOT USED
C17	C6,7
CR4	
J2	
L8	L2,3,5
Q3	
R20	R13,16
T2	
U2	



FO-12. Power Regulator CCA A1A1A7 Schematic Diagram

REF DESIGNATION	
HIGHEST USED	NOT USED
J10 P9 R3 S3 E3 W1	J6,7,9 P2 THRU 5.8





NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

1.3 A BAR (—) ABOVE A SIGNAL NAME MEANS THE INVERTED (NOT) FORM OF THE SIGNAL.

2.0 SPECIFIC:

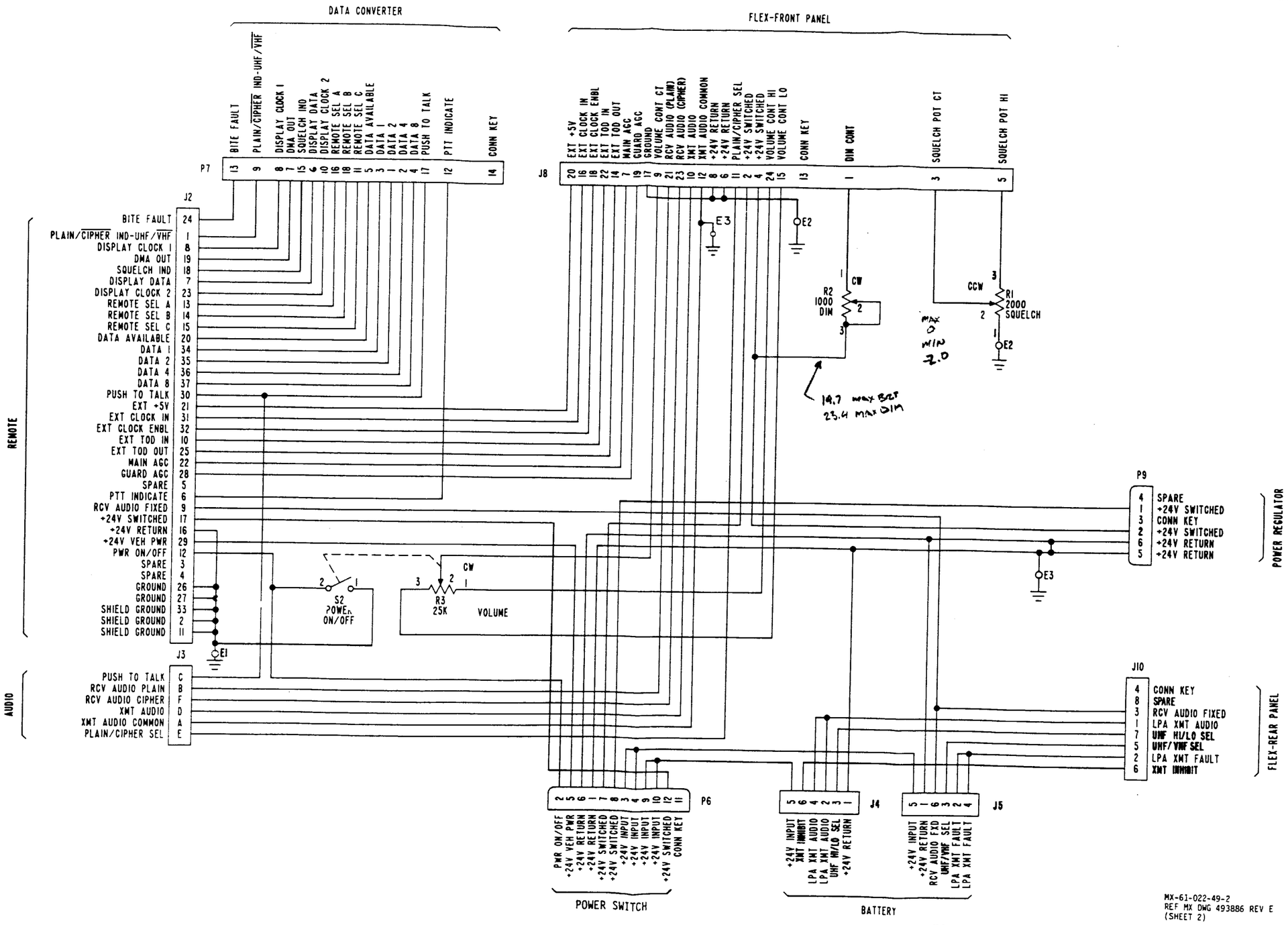
2.1 UNLESS OTHERWISE SPECIFIED:
VOLTAGES ARE DC.
RESISTORS ARE 10%.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBL ' DESIGNATION 1A1A1A8.

2.3 REFERENCE:
ASSEMBLY NUMBER : 4860-801.

MX-61-022-49-1
REF MX DWG 493886 REV E
(SHEET 1)

FO-13. Electrical Chassis Assembly A1A8 Schematic Diagram (Sheet 1 of 2)



FO-13. Electrical Chassis Assembly A1A8 Schematic Diagram (Sheet 2 of 2)

NOTES:

1.0 GENERAL:

1.1 INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY DOD-STD-100.

1.2 DATA INCLUDED IN PARENTHESIS, ( ), IS FOR REFERENCE ONLY.

2.0 SPECIFIC:

2.1 UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS.
RESISTORS ARE 5%, 1/4W.
CAPACITANCE VALUES ARE IN PICOFARADS.
VOLTAGES ARE DC.

2.2 PARTIAL REFERENCE DESIGNATIONS ARE SHOWN: FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY DESIGNATION A1A1A9.

2.3 FOR CONTINUATION OF CIRCUIT SEE 493910.

2.4 PART NUMBER 619999-902.

2.5 REFERENCE:
ASSEMBLY NUMBER 811963-801.
PRINTED WIRING BOARD 411952-1.
TEST PROCEDURE 979165

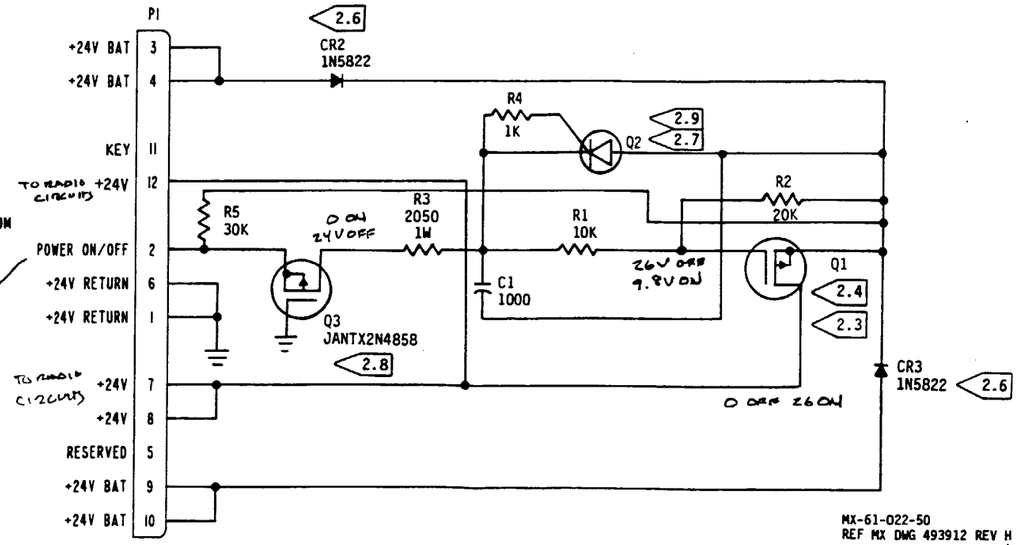
2.6 PART NUMBER 619689-903.

2.7 PART NUMBER JANTX2N3029.

2.8 THIS DEVICE REQUIRES SPECIAL HANDLING AND PROCESSING TO PREVENT DAMAGE FROM ELECTROSTATIC DISCHARGE TRANSIENTS.

2.9 ITEMS LISTED ON PARTS LIST AS ALTERNATE ITEMS MAY BE USED INTERCHANGEABLY.

+23.4 OFF
0 ON



FO-14. Power Switching CCA A1A1A9 Schematic Diagram

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