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USER MANUAL

SWITCH104™
10/100 ETHERNET SWITCHING HUB

4/21/2005

MNL-0490C-01

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SWITCH104™
10/100 ETHERNET SWITCHING HUB
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INTRODUCTION

PRODUCT DESCRIPTION



The Switch104™ is a rugged 5-port PC/104 Fast Ethernet switching hub featuring very low power dissipation (1.5 watts typical) and highly reliable extended-temperature operation up to +85°c (185°f).

Supporting auto-MDI-MDIX network installation, the Switch104 is designed for simple plug-and-play operation, enabling up to five embedded computing devices to be networked together using 10BaseT or 100BaseTX Local Area Network (LAN) connections. Fully IEEE 802.3 and IEEE 802.3u compliant, its five transceiver ports are flexibly designed so that any port can serve as an uplink.

The Switch104 can either be used as a standalone network switch (no processor board required) or in combination with embedded systems that support a PC/104 (ISA) bus. The board integrates fully independent media access controllers (MACs), an embedded frame buffer memory, and a high-speed address look-up engine, along with support for auto-crossover, auto-polarity, auto-negotiation, auto-speed sensing, and bridge loop prevention.

This compact Ethernet switch is ideally suited to space-constrained, high reliability aviation, industrial, military, and transportation applications. The unit is only 3.550” x 3.775” (90x96 mm) in size, and it boasts a very high MTBF of 1.51 million hours. Network connections are made through either onboard RJ-45 jacks or via right-angle 4-pin Molex connectors if panel mounting the RJ-45 jacks into a faceplate, endplate or enclosure. Power can be applied through either the PC/104 bus or through a 2-pin power connector if not installed in a PC/104 system. Mounting holes are also included to facilitate simple installation.

FEATURES

- RJ-45 jack or Molex panel mount connectors
- LED activities indicators
- Low power dissipation
- Store-and-forward switching mode
- 5 Auto-configured ports (straight/twist)
- Auto-negotiation and speed auto-sensing support
- Ports can work at 10Mbps or 100 Mbps, full duplex or half duplex mode
- Simple networking installation through auto-MDI/MDIX (All ports can act as uplink)
- Pause frame-based switch fabric delivers true non-blocking switching
- Back pressure-based flow control of half duplex ports
- Baseline wander correction circuitry
- Highly integrated DSP-based 10/100 switch
- Look-up engine supports as many as 1,024 MAC address entries
- 2-Pin Power Header for External Power Connections (PRV-1059-03, -04 Only)
- 16-bit PC/104 Bus (PRV-1059-01, -02 Only)

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ABOUT PC/104

The PC/104 specification is characterized by its small form-factor (3.550" x 3.775"), stackable 104-pin/socket ISA bus connector, and reduced bus signal drive, making PC/104's size, durability, expandability, reliability, quality, and power consumption ideal for embedded computing. PC/104 technology leverages the same readily available development tools used with personal desktop computers to dramatically improve time-to-market for embedded systems development. The full PC/104 specification can be found at the PC/104 Consortium Web site:
http://www.pc104.org/technology/pc104_tech.html

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SECTION 1 – INSTALLATION

1.1 Board Installation

The hub does not require drivers or software configuration. Carefully remove the board from its anti-static bag. Users can immediately use any of the features of the product simply by attaching the cables and supplying power to the unit through either the PC/104 bus or 2-pin power header, depending on the version purchased. For PC/104 applications, make sure all pins are lined up before insertion. Attach the 10/100 Ethernet Switching Hub into a PC/104 card stack by mating PC/104 bus connector to PC/104 bus connector.

1.2 Installing Network Cables

The following types of cabling can be used with the 10/100 Ethernet Switching Hub:

1. 10BaseT Category 3,4 or 5 UTP/STP
2. 100BaseTX Category 5 UTP/STP

Although Port 0 is defined as the uplink port, all five ports have been implemented and can serve as an uplink port. Twisted-pair crossed cabling (10BaseT or 100BaseT) is recommended yet not required for the uplink connection (hub-to-hub). Straight cabling for the remaining port connections (Hub-to-PC) is similarly recommended, but not required.

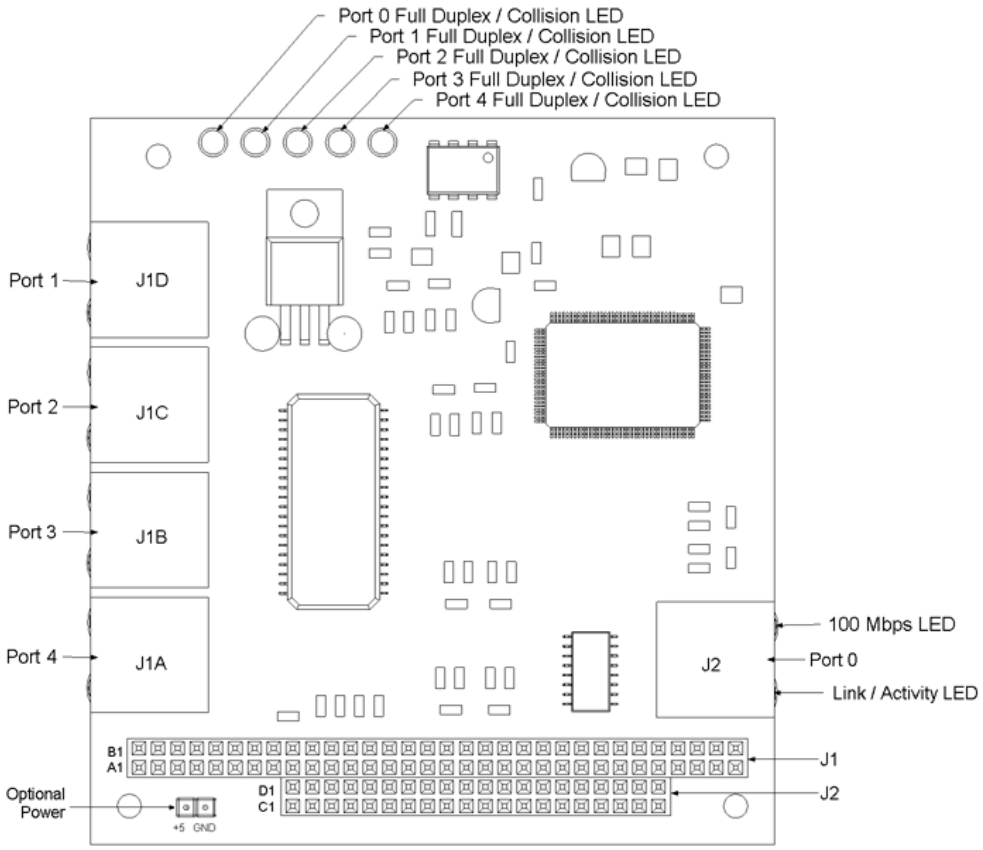
The board supports Auto MDI-/MDIX Crossover, which allows it to determine whether or not it needs to cross over between pairs, virtually eliminating the need for an external crossover cable. If it interoperates with a device that cannot automatically correct for crossover, the switching hub makes the necessary adjustment prior to commencing auto-negotiation. Similarly, if the hub interoperates with a device that implements MDI-MDIX crossover, a random algorithm determines which device performs the crossover.

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Section 2 - CONNECTIONS

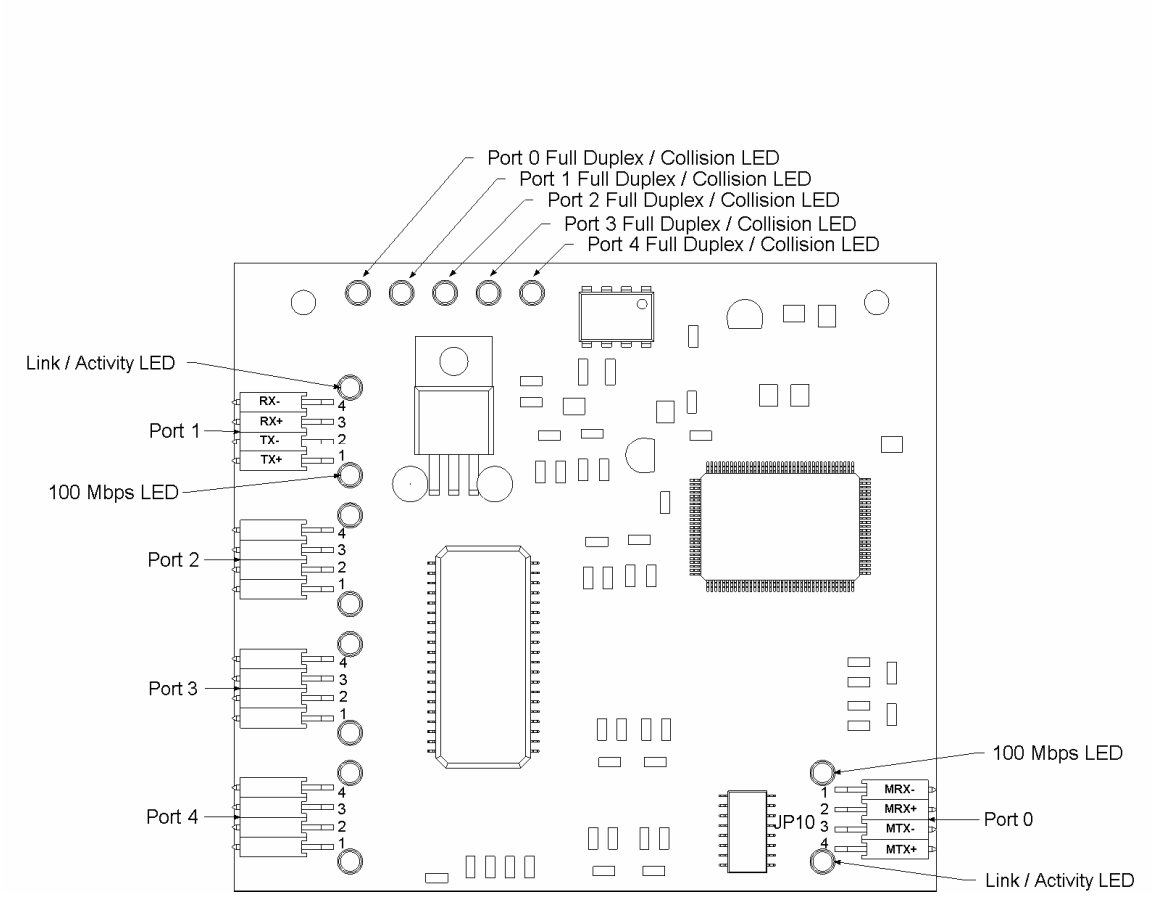
2.1 Connector Placement

10/100 Ethernet Switching Hub (w/ local RJ-45 Jacks)



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10/100 Ethernet Switching Hub (w/ 4-pin Molex Connectors)



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2.2 Connector Pinouts

Pin Description Port 0	
Pin	**Signal**
4	MTX +
3	MTX -
2	MRX +
1	MRX -

Pin Description Ports 1-4	
Pin	**Signal**
1	TX +
2	TX -
3	RX +
4	RX-

CON2/J101: 2-Pin Power Connector (Not Loaded on PC/104 versions)	
Pin 1	+5VDC
Pin 2	GND

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J1/J2: PC/104 Bus				
Pin	Row A	Row B	Row C	Row D
0	--	--	GND	GND
1	/IOck	GND	/SBHE	/MCS16
2	SD7	Rstdrv	LA23	/IOCS16
3	SD6	+5v	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	-5v	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12v	LA18	IRQ14
8	SD1	/Exfer	LA17	/DA0
9	SD0	+12v	/MR	DRQ0
10	IOrdy	(key)	/MW	/DA5
11	AEN	/SMW	SD8	DRQ5
12	SA19	/SMR	SD9	/DA6
13	SA18	/IOW	SD10	DRQ6
14	SA17	/IOR	SD11	/DA7
15	SA16	/DA3	SD12	DRQ7
16	SA15	DRQ3	SD13	+5v
17	SA14	/DA1	SD14	/MSTR
18	SA13	DRQ1	SD15	GND
19	SA12	/Rfrsh	(key)	GND
20	SA11	SCLK	--	--
21	SA10	IRQ7	--	--
22	SA9	IRQ6	--	--
23	SA8	IRQ5	--	--
24	SA7	IRQ4	--	--
25	SA6	IRQ3	--	--
26	SA5	/DA2	--	--
27	SA4	TC	--	--
28	SA3	BALE	--	--
29	SA2	+5v	--	--
30	SA1	OSC	--	--
31	SA0	GND	--	--
32	GND	GND	--	--

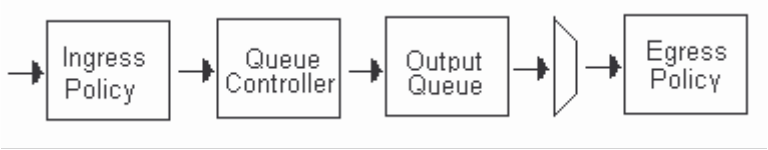
The PC/104 bus always uses Row A and B, while Row C and D are for 16 bit systems. B10 and C19 are keyed locations. For more information about the PC/104 specification, please visit the PC/104 Consortium Web site: http://www.pc104.org/technology/pc104_tech.html

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Section 3 – OPERATION

3.1 Switch Data Flow

The switch portion of the Ethernet Switch Hub receives good packets from the MAC's, processes them, and forwards them to the appropriate MACs for transmission. Processing the frames is the key activity, and involves the Ingress Policy, the Queue Controller, the Output Queues, and the Egress Policy blocks shown below. Each port has it's own Ingress and Egress Policies.



3.2 Media Access Controllers

Five independent Media Access Controllers (MACs) perform the 802.3 protocol functions, including frame formatting, frame stripping, CRC checking, CSMA/CD enforcement, collision handling, etc. Before a packet can be sent out, the transmit block must check if the line is available for transmission. The transmit line is available all the time when the port is in full-duplex mode, but the line could be busy receiving a packet if the port is in half-duplex mode. If the line is busy, the transmitter waits by deferring its transmission. When the line is available, the transmission insures a minimum interpacket gap of at least 96 bits has occurred and then transmits a 56-bit preamble and an 8-bit Start of Frame Delimiter (SFD) ahead the basic frame.

For half-duplex mode, the hub also monitors the collision signals while it is transmitting. If a collision is detected (i.e. both transmitter and receiver of a half-duplex MAC are active at the same time), the MAC transmits a JAM pattern and then delays the retransmission for a random time period determined by the IEE 802.3 backoff algorithm. In full-duplex mode, the collision signal and backoff algorithm is ignored.

3.2.1 Backoff

In half-duplex mode, the Ethernet Hub's MACs implement a truncated binary exponential backoff algorithm, starting with a randomly small backoff time followed by progressively longer and longer random backoff times. The random times prevent two or more MACs from always attempting re-transmission at exactly the same time. The progressively longer backoff times give a wider random range giving congested links a better chance of finding a winning transmitter. The MACs will rest the progressively longer backoff time circuit after 16 consecutive re-transmit trials.

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3.2.2 Half- and Full-Duplex Flow Control

Half- and Full-duplex flow control is used to throttle the end station to avoid dropping packets during network congestion. When the free buffer space is almost empty or the output queue is almost full, the MACs force a collision in the input port when sensing an incoming packet. Full-Duplex uses frame pauses to handle the congestion.

3.3 Address Management

The switching function of the module involves the learning how to switch packets to the correct MACs, and only to the correct ones. The switch learns what port to which an end station is connected by remembering each packet's Source Address, and the port number the packet came in on.

When a packet is directed to an unlearned MAC address, the packet is transmitted to all of the ports. When an end-station responds back, its address is learned and stored until it is aged (see section 3.4.4). Once a MAC address/port is learned, all future packets directed to that address will be forwarded solely to that port.

When an end station is moved from one port to another, a new MAC address/port number association will have to be learned, and the new one replaced. For this to occur, the old association needs to expire or "age". These issues are handled by the "Aging" function (see section 3.4.4).

3.3.1 Address Translation Unit

The Lookup Engine or Address Translation Unit (ATU) reads the Destination Address (DA) and Source Address (SA) from each received packet, performing all address searching, learning and aging functions for all five ports at "wire speed" rates. It uses a hashing technique for quick storage and retrieval. If there is a hash collision, there is a four entry bin to hold MAC address with the same hash. The address table has storage for up to 1024 entries in the embedded SRAM, and has a default 300 second (5 min) aging time.

3.3.2 Address Searching

The address search engine searches the address database to obtain the output port number, called the Destination Port Vector (DPV), for each frame's Destination Address (DA). It arbitrates destination address requests from the ports and grants one lookup at a time. The MAC address is hashed, and then data is read from the SRAM table and compared to the MAC address for a match. If the compare matches, the DPV is returned to the output port queue manager, where is may be modified by the VLANTable data. When no match is found, a unique default DPV is returned to the output port queue manger, which typically sends the frame to all ports (to learn the MAC address).

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3.3.3 Address Learning

An address-learning engine is used to learn the source address. Up to 1024 MAC address/port number mappings can be stored in the address table.

When a frame comes in, the MAC address gets hashed into the database. If no match is found, the MAC address/port association needs to be learned. Learning consists of the following: the frame is forwarded to all of the ports, awaiting a response from one the ports. Once a port responds, the association is made and "learned" into the address table. If multiple ports respond, the associations are not learned. Once a MAC address/port is learned, all future packets directed to that address will be forwarded solely to that port.

3.3.4 Address Aging

Continuous address aging ensures an up-to-data address table and rapid address look-up. Once a node is disconnected from the network segment, or if it becomes inactive, its entry is removed from the address table. Every time a MAC address is found in the address table, the age is refreshed, keeping it active. Aging occurs by default every 5 minutes.

Each MAC address entry in the address table contains an age value, Entry_State. The initial value of Entry_State is 0xE. Aging occurs with a sweep of the table, the ATU reads each entry in the address table and decrements its Entry_State. Once the Entry_state of a MAC address reaches zero, the entry is killed and purged from the table. The speed at which aging occurs is default at 300 seconds.

3.4 Auto-Negotiation

Auto negotiating occurs when the switch negotiate with a link partner to determine the speed and duplex with which to operate. It the partner is unable to negotiate, the switch goes to a detection mode to determine the speed and the duplex will lock at half-duplex.

3.5 Auto MDI-/MDIX Crossover

The board determines whether or not it needs to cross over between pairs, virtually eliminating the need for an external crossover cable. If it interoperates with a device that cannot automatically correct for crossover, the switching hub makes the necessary adjustment prior to commencing auto-negotiation. Similarly, if the hub interoperates with a device that implements MDI-MDIX crossover, a random algorithm determines which device performs the crossover.

Note: For questions related to older revisions of this board (based on older Marvell 88E6050 chip), please contact Parvus technical support at tsupport@parvus.com or 801-483-1533 for assistance.

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Section 4 – SPECIFICATIONS

Environmental	
Operating Temperature	-40ºC to +85ºC
Storage Temperature	-55ºC to +100ºC
Electrical	
Requirements	+5VDC Input
Power Consumption	1.5 Watts (typical) with all ports @ 100Mbps (5 Volts @ 274mA)
Mechanical	
Dimensions	3.550” x 3.775”
Weight	Up to 86 grams (0.190 lbs)
MTBF	

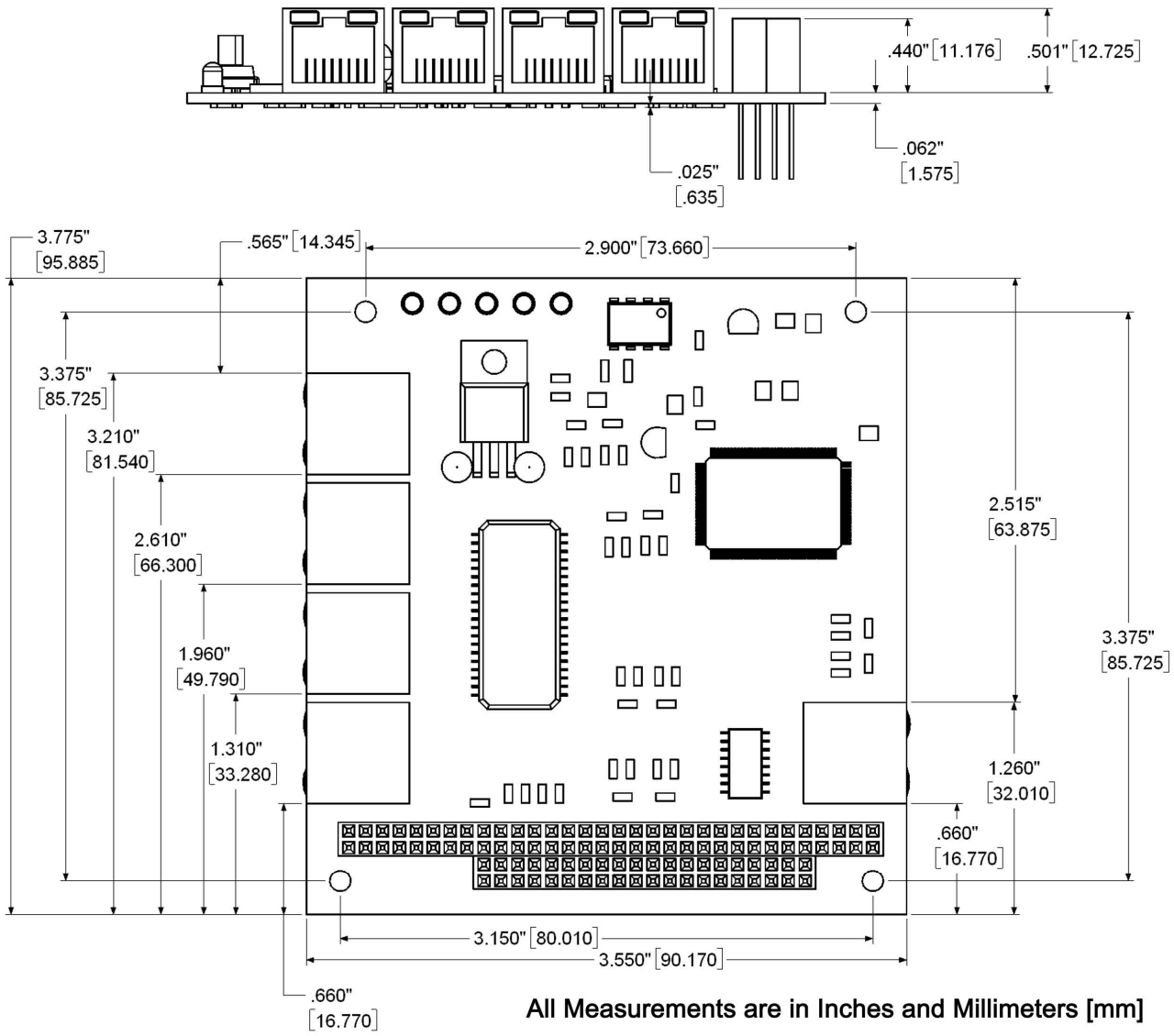
1.52 Million Hours @ 40°C (Per MIL-HDBK-217F, Ground Benign, Controlled GB, GC)

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Section 4 – APPENDIX

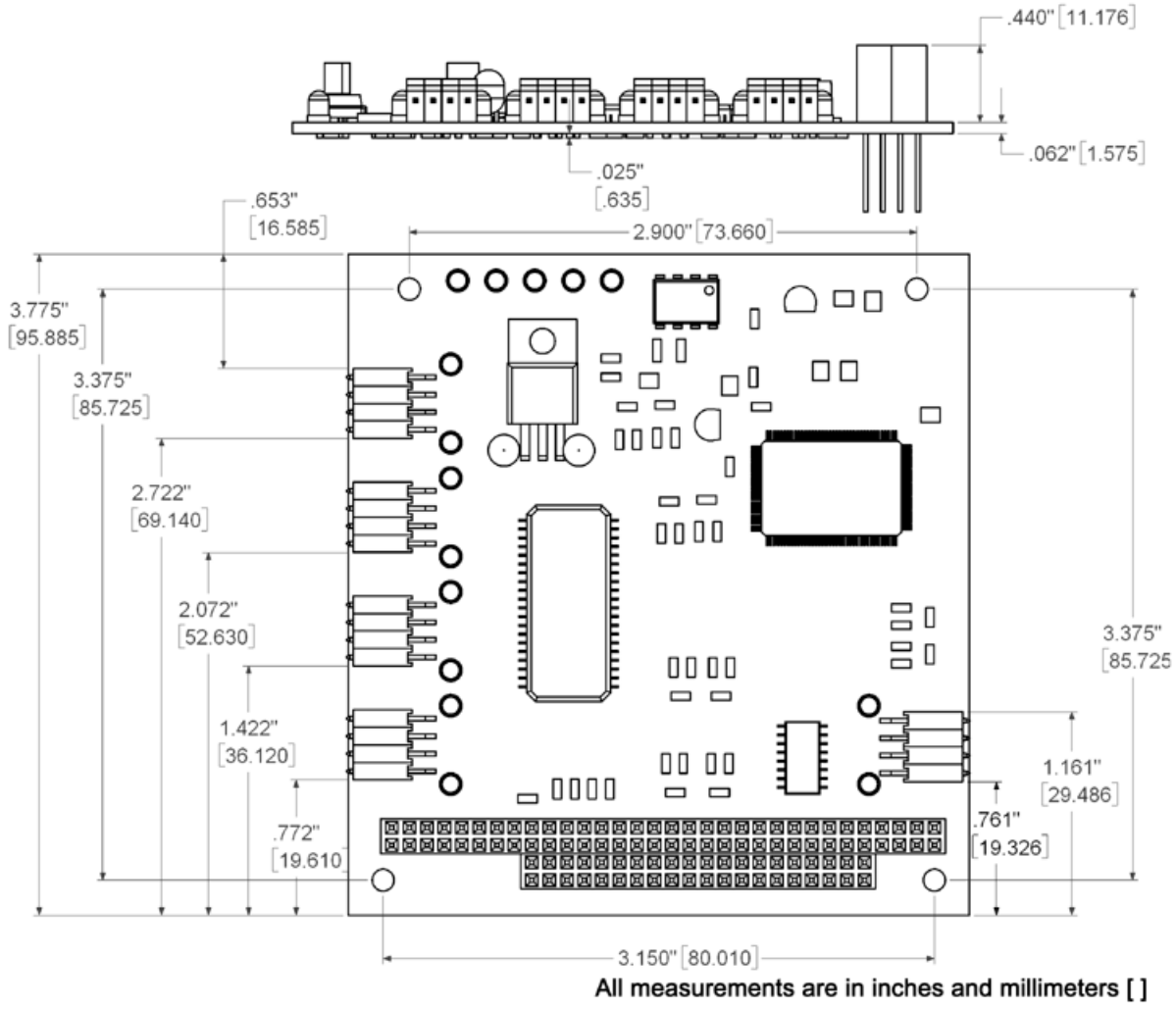
Dimensional Line Drawings

RJ-45 Version



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Molex Version



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Warning: The equipment described herein has been designed to comply with the limits for a Class B computing device, pursuant to Subpart J of Part 15 of FCC rules. Only peripherals (computer input/output devices, terminals, printers, etc.) designed to comply with the Class B limits may be attached to this computer.

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