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64EP3 6U VME
SINGLE BOARD COMPUTER
with MULTI-FUNCTION I/O



OPERATIONS MANUAL

MODEL 64EP3

6U, VME, SINGLE BOARD COMPUTER WITH MULTI-FUNCTION I/O

Features

- SBC with multi-function I/O in a single 6U VME slot
- Automatic background BIT (module-dependant)
- VME Bus and/or Dual Gigabit Ethernet Interfaces
- Front and/or Rear I/O Support
- Designed for Commercial and Rugged applications
- Software Support Kit(s) and Driver(s) are available

Conduction Cooled



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Processor Options

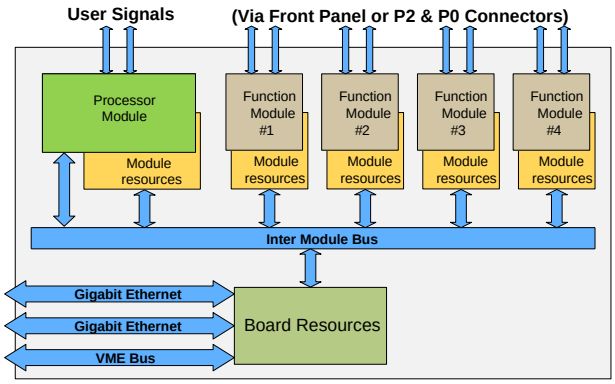
Freescale PowerPC MPC8536 @ 1.0 GHz Processor

- 1 GB SDRAM (program execution)
- 256 MB Flash (OS/application program)
- Dual Gigabit Ethernet
- Serial/ SPI Flash/USB support (debug/data storage)
- VxWorks 6.x BSP

Analog Devices (ADI) BF533 @ 500 MHz Processor

- Extremely Low Power High Performance Processor
- Windows PC Development – ADI Visual DSP++
- Ethernet, RS232, USB, I^2C, Differential and TTL I/O

Description



The 64EP3 is a single slot, 6U VME, low-power/high-performance Single Board Computer (SBC) with configurable multi-function I/O. Powered by a choice of Freescale's 1.0 GHz MPC8536 PowerPC (**U3**) or Analog Devices' 500 MHz BF533 (**U2**) processor modules, the 64EP3 offers an extremely low power, cost-conscious SBC solution for today's demanding, space-constrained and resource limited embedded systems. Four I/O module slots enable integrators to mix-n-match a variety of I/O and communication functions. The functions include Digital I/O (Discrete, Differential, TTL), Analog I/O (A/D, D/A, RTD, Strain Gage), Motion Control and Sensor Interfaces (Synchro/Resolver/LVDT/RVDT Measurement and Simulation, Encoder/Counter), and Communication Interfaces (RS-232/422/423(MIL-STD-188C)/485, MIL-STD-1553, CANBus and ARINC 429/575). The 64EP3 SBC configured with up to four modules allows systems integrators to confidently manage monitor and process a host of sensor interfacing requirements with NAI's flexible, leading-edge, fully programmable and continuous background built-in-test (BIT) enabled I/O function modules.

The 64EP3 SBC with multi-function I/O and full complement of I/O libraries and drivers are ideally suited for a multitude of commercial and rugged embedded processing and I/O systems. The 64EP3 SBC with Master VME Bus capability may be utilized with other NAI high-density, multi-function I/O boards to provide a complete, expandable, low power/high performance, programmable solution for sensor and communication data acquisition, management, processing and distribution. All I/O sensor data is available on the VME Bus or Gigabit Ethernet.

Advantages of using the 64EP3 SBC for board or system-level solutions:

- Process and control of I/O functions without the need of a separate SBC or mission computer
- Direct processing and control of I/O functions via MIL-STD-1553, RS232/422/485, CANBus, ARINC 429/575 and/or other functions
- Reduction of raw data to offload main mission computer—enabling performance of customer-specific algorithms such as FFT and digital filtering
- Ability to manage and process control/servo loops without mission computer intervention

General Board Specifications

●**Power:** +5VDC / ± 12VDC (certain modules) ●**Operating Temp:** 0° C to 70° C or -40° C to 85° C ●**Size:** – 233mm x 20mm x 160mm (6U)

Processor Modules

Processor	Module	Flash	SDRAM	Frequency	Software Support
ADI Blackfin BF533	U2	8MB	512KB	500 MHz	ADI Visual DSP++ /Function Library
PowerPC MPC8536	U3	256MB	1GB DDR2	1.0 GHz	Wind River BSP/VxWorks 6.x/Library

Available Function Modules

(GEN3 Platforms)

Note 1 – Indicates wide selection (See part number in Operations Manual)

Note 2 – Contact factory for availability

Note 3 – Additional channels on some platform front I/O (check pinouts)

A/D Converter	**Module**	**Channels**	**Input Scaling**	**Resolution**	**Accuracy** (±)	**Sampling (programmable)**
	C1	10	±1.25,2.5,5 or 10 VDC	16-bit	0.05% FS	200 KHz max
	C2	10	±5,10,20 or 40 VDC	16-bit	0.1% FS	200 KHz max
	C3	10	0-25 mA	16-bit	0.1% FS	200 KHz max
	C4	10	±6.25,12.5,25 or 50 VDC	16-bit	0.1% FS	200 KHz max
	CA	10	(Channels 1-6 are C2 type and Channels 7-10 are C3 type)			
D/A Converter	**Module**	**Channels**	**Output Range**	**Resolution**	**Accuracy** (±)	**Settling time**
	F1	10	±10 or 0-10 VDC	16-bit	0.05% FS	15µs max
	F3	10	±5 or 0-5 VDC	16-bit	0.05% FS	10µs max
	F5	4	±20 or 0-20 VDC	16-bit	0.05% FS	10µs max
	J3	10	±1.25 or 0-1.25 VDC	16-bit	0.05% FS	10µs max
	J5	10	±2.5 or 0-2.5 VDC	16-bit	0.05% FS	10µs max
	J8	4	±20 to ±80 VDC	16-bit	0.15% FS	350µs max
Thermocouple	**Module**	**Channels**	**Update rate**	**Resolution**	**Accuracy** (±)	**Thermocouple Interface**
	G3	6	4.17 – 470 Hz	24-bit	0.75 – 2.0 °C	NIST J,K,T,E,N,B,R,S & ±100 mV)
RTD	**Module**	**Channels**	**Update rate**	**Resolution**	**Accuracy** (±)	**Interface**
	G4	6	16.7 Hz/channel	16-bit	0.05% FS	2, 3 or 4 wire
Strain Gage	**Module**	**Channels**	**Update rate**	**Resolution**	**Accuracy** (±)	**Interface**
	G5[2]	4	4.7 Hz – 4.8KHz	16-bit	0.1% FS	Conventional 4-Arm Bridge
Encoder/Counter	**Module**	**Channels**	**Signal Voltage**	**Resolution**	**Modes**	
	E7	4	RS422 / 24 VDC	32-bit	Encoder (SSI, A-Quad-B), Counter (up/down)	
L(R)VDT/D	**Module**	**Channels**	**Frequency**	**Resolution**	**Accuracy** (±)	**Interface**
	L[1]	4	360 Hz to 20 KHz	16-bit	0.025% FS 2 or 3/4 wire	
SYN(RSL)/D	**Module**	**Channels**	**Frequency**	**Resolution**	**Accuracy** (±)	**Tracking Rate**
	S[1]	4	50 Hz to 20 KHz	16-bit	1 arc-min	190 RPS
D/SYN(RSL)	**Module**	**Channels**	**Frequency**	**Resolution**	**Accuracy** (±)	**Power**
	6[1]	3	47 Hz – 10 KHz	16-bit	0.1°	0.25 VA / channel
D/L(R)VDT	**Module**	**Channels**	**Frequency**	**Resolution**	**Accuracy** (±)	**Power**
	5[1]	3	47 Hz – 10 KHz	16-bit	0.2% FS	0.1 VA / channel
I/O, TTL/CMOS	**Module**	**Channels**	**Input Range**	**Output level**	**Programmable**	
	D7	16	0 – 5.5 V	TTL/CMOS	Input or Output	
I/O, Differential	**Module**	**Channels**	**Input Range (422)**	**Input Range (485)**	**Output Range (422/485)**	
	D8	11 (16)[3]	-10V to +10V	-7V to +12V	-0.25V to +5V	
I/O, Discrete	**Module**	**Channels**	**Input Range**	**Output Range**	**Programmable**	**Notes**
	K6 (v4)	16	0 – 60 VDC	0 – 60 VDC	Input or Output	(500 mA – 2 A) (source/sink)
	K7[2]	12 (16)[3]	±80V	±80V	Input or Output	Isolated switch (600mA)
Relay	**Module**	**Channels**	**Type**	**SW Volt/Current**	**SW Power (max)**	**Notes**
	KN[2], KL[2]	4	DPDT (1 CH Form C)	220V / 2A (max)	60W / 62.5 VA	KN=non-latch, KL=latching
Serial Communications	**Module**	**Channels**	**HW Interface levels support**		**Bit rate (Async/Sync)**	**Tx/Rx Buffer** **Notes**
	P8	4	RS-232/422/423(MIL-STD-188C)/485		1 / 4 Mbit/s per Ch.	32KB Partial modem
	PC[2]	4	Isolated RS422/485		1 / 4 Mbit/s per Ch.	32KB Partial modem
CANBus	**Module**	**Channels**	**CAN protocol**	**Message Buffer**	**Data rate (Prog)**	**Notes**
	P6, PA	4	P6= 2.0A/B / PA=J1939	16K RX/TX	1 Mb/s max.	Bosch® IP Core
MIL-STD-1553	**Module**	**Channels**	**Operational Modes**	**Onboard RAM**	**Coupled**	
	N7, N8	2	BC,RT, BM, BM/RT	128Kbyte per ch	N7 = Transformer / N8 = Direct	
ARINC 429/575	**Module**	**Channels**	**Frequency**	**Input/output**	**Message Buffer**	
	A4	6	100 KHz or 12.5 KHz	RX/TX	256 word Tx/Rx	
DC Power Supply	**Module**	**Channels**	**Voltage Output**	**VOut Regulation**	**Current Output**	
	V1, V2	1, 2	± 15V	± 1%	± 450 mA(max)	
AC Reference	**Module**	**Channels**	**Frequency**	**Accuracy**	**Voltage**	**Power**
	W[1]	1	47 Hz – 20KHz	± 3%	2 – 115 VRMS	6 VA (max.)

SOFTWARE SUPPORT

The E*NA*IBL Software Support Kit (SSK) is supplied with all system platform based board level products. This platform's SSK contents include html format help documentation which defines board specific library functions and their respective parameter requirements. A board specific library and its source code is provided (module level 'C' and header files) to facilitate function implementation independent of user operating system (O/S). Portability files are provided to identify Board Support Package (BSP) dependent functions and help port code to other common system BSPs. With the use of the provided help documentation, these libraries are easily ported to any 32-bit O/S such as RTOS or Linux.

The latest version of a board specific SSK can be downloaded from our website www.naii.com in the software downloads section. A Quick-Start Software Manual is also available for download where the SSK contents are detailed, Quick-Start Instructions provided and GUI applications are described therein. For other operating system support, contact factory.

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SPECIFICATIONS

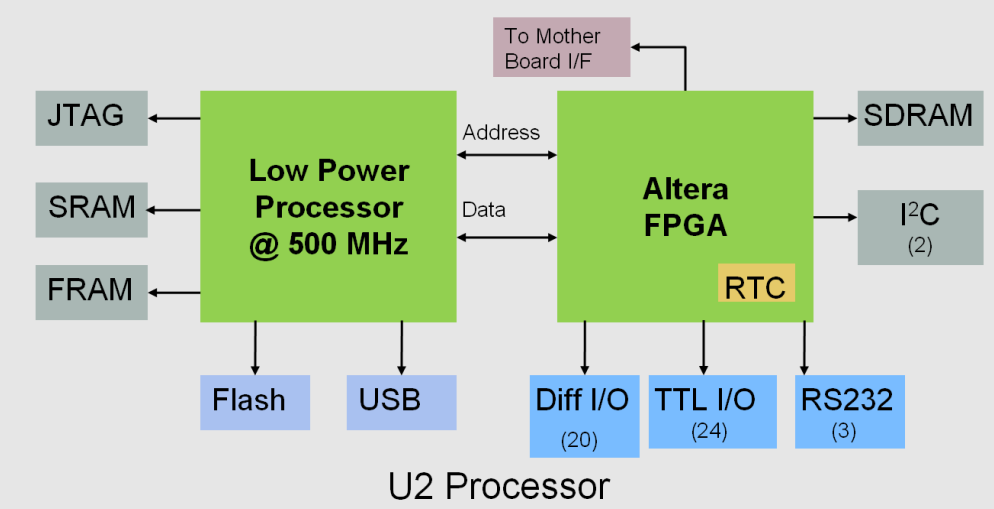
General − For the Motherboard

VME Data Transfer:	Data transfers within 200 ns
Interrupts:	One interrupt capability is implemented. Seven priority lines can be specified
Power (Motherboard):	+5 VDC @ 1.0 A then add power for each individual module
Temperature, Operating:	"C" =0°C to +70°C, "E" =-40°C to +85°C (see part number)
Storage Temperature:	-55°C to +105°C
Temperature Cycling:	Each board is cycled from -40°C to +85°C for 24 hrs for options “E” or “H” (See part number)
Size:	Height 9.2” (233.4 mm) (6U) Width 0.8” (20.3 mm) (4HP) Depth 6.3” (160 mm)
Weight:	16 oz. (454 g) unpopulated, then add weight for each module (See module spec) Add 2 oz. (57g) for optional reference supply Add 2 oz. (57g) for wedgelocks

Processor (Module U2)

Blackfin Processor and General Purpose I/O Resource for User Operational Programs and Control

Processor:	Analog Device's Blackfin® BF533, for overall system processing. This is an extension of the multi-function board architecture which uses Blackfin processors to implement the motherboard, module and signal processing functions. The Blackfin is an ideal choice for this use due to its wide application and availability of third party software and design services.
FPGA:	A moderate scale FPGA (Altera Cyclone II family) is added to provide additional flexibility for system functions
Flash Memory:	8 MB for program and data storage
Processor Clock Rate:	500MHz
Ferro-Electric RAM:	8 KB for non-volatile data storage
SDRAM:	16 MB for program execution
RAM:	512KB for real time cache
I/O Interfaces:	2, I2C interfaces to allow the processor to power supply module temperature I/O capability to support box level monitor capability and/or external interface capability including 24 digital TTL interfaces, 20 digital differential interfaces and 3 RS232 serial interfaces
Power:	5V @ 1150 mA (est./typ. duty cycle)
Weight:	2 oz. (57g)



U2 Processor Description

Based on Analog Devices' Blackfin BF-533 DSP processor, users can confidently take advantage of the powerful Analog Devices, Inc. (ADI) Visual DSP++ Development Environment. The 64D2 fitted with the U2 Processor allows users to develop application code in support of their I/O and communication intensive application without the need for a single board computer. The U2 coupled with NAI's extensive I/O function capabilities and software library support offers developers a real-time embedded system environment. Additionally, this low power solution can interface directly to the I/O, perform embedded algorithms and communicate directly to system and sub-system computers. Operating system, run time and overhead are reduced due to direct DSP control. Additional core interfaces added to the FPGA allows for a flexible communication interface selection for controlling I/O specific modules. Reference the U2 programmer's guide for detailed operation documentation.

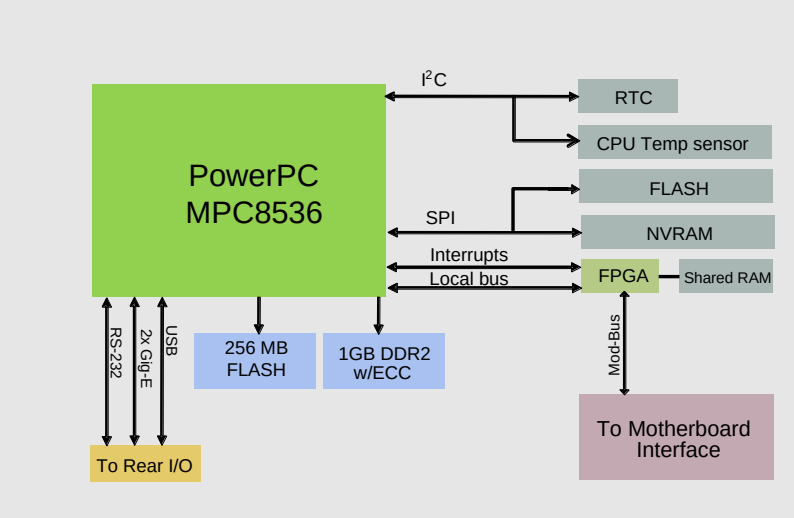
User Requirements/Utility Library

- Analog Device's Visual DSP++ 4.5
- Blackfin emulator
- NAI I/O and communications library support

Processor (Module U3)

PowerPC Processor and General Purpose I/O Resource for User Operational Programs and Control

Processor:	The MPC8536, high-performance member of the PowerQUICC III™ processor family combines a computation intensive super scalar Power Architecture™ processor core with high performance system peripherals and advanced power management techniques; Internally integrates SATA, USB, multi-lane PCI express, gigabit Ethernet, and DDR memory to increase data bandwidths, reduce valuable board real estate, and lower overall power consumption.
Processor Clock Rate:	1.0 GHz
NAND Flash:	256 MB for OS/application program storage
Ferro-Electric RAM:	8 KB for non-volatile data storage
SDRAM:	1 GB for program execution
SPI Flash:	16 MB for program and data storage
User I/O:	Serial communications and USB port
Power:	5V @ 1650 mA (est./typ. duty cycle)
Weight:	2 oz. (57g)



U3 Processor Module Block Diagram

U3 Processor Description

Based on FreeScale's MPC8536 processor, users can confidently take advantage of the familiar VxWorks RTC environment for developing control and application software. Boards fitted with the U3 Processor allow users to develop application code in support of their I/O and communication intensive application without the need for a separate single board computer. The U3 coupled with NAI's extensive I/O function capabilities and BSP/library support offers developers a real time embedded system environment. Additionally, this solution can interface directly to the I/O, other cards on the system bus (bus-master capability), perform embedded algorithms and communicate directly to system and sub-system computers. Operating system run time and overhead are reduced due to direct processor control.

User Requirements/Utility Library

- VxWorks 6.x development environment
- NAI U3 VxWorks 6.x BSP
- NAI I/O and communications library support

ARINC 429/575 (Module A4) – Six RX/TX Channels, Configurable

Input/Output Format:	6 channels can be programmed for either RX or TX per channel
Frequency:	100 KHz or 12.5 KHz operation
Buffers:	RX/TX FIFO buffering Label/SDI filtering
Self-Test:	Loop back test
Format:	AR429 or 575 programmable/channel
Power:	+5V @ 850 mA (nominal) ±12 V @ 55 mA (nominal)
Ground:	Ground return is to system ground
Weight:	1 oz. (28g)

MIL-STD-1553 (Module N7) – Two Dual/Redundant Channels, Transformer Coupled

Onboard RAM:	128 KB per dual-redundant channel
Operational Modes:	BC, RT, BM, or BC/RT
Output Signal	28 Vp-p, as per 1553 standard
Power:	+5 VDC @ 1.6 A max at 100% duty cycle (2 channels)
Ground:	Bus signals isolated from system ground
Weight:	1 oz. (28g)

MIL-STD-1553 (Module N8) – Two Dual/Redundant Channels, Directly Coupled

Onboard RAM:	128 KB per dual-redundant channel
Operational Modes:	BC, RT, BM, or BC/RT
Output Signal:	28 Vp-p, as per 1553 standard
Power:	+5 VDC @ 1.6 A max at 100% duty cycle (2 channels)
Ground:	Bus signals isolated from system ground
Weight:	1 oz. (28g)

CANBus (Module P6, PA) – Four CANBus Interfaces

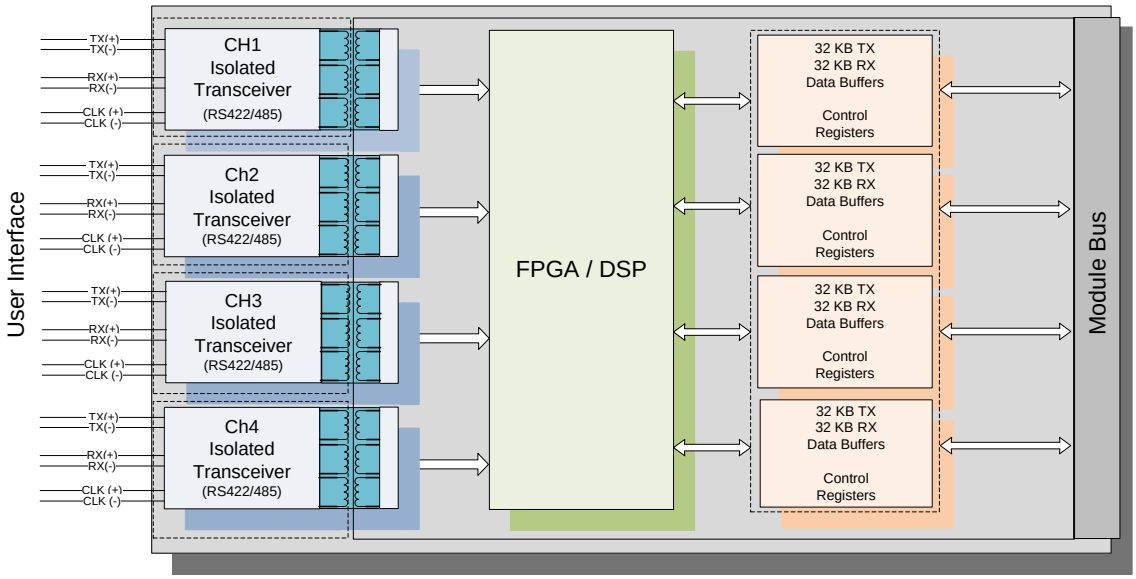
Channels:	Four independent isolated RX and TX
CAN Protocol:	P6 = CANBus Version 2.0 A & B protocol support PA = CANBus Version J1939 protocol support Standard (11-bit) and Extended (29-bit) (identifier) Data Frames Integrated BOSCH® CANBus IP Core
Data Rate:	Up to 1 Mbps per channel
Data Length:	0-250 bytes
Power:	210 mA @ 5V / CH; (1.05 W / CH) (typ.)
Ground:	Isolated; Galvanic (500V) isolation from channel-to-channel and system ground
Weight:	1 oz. (28g)

Serial Comms (Module P8) – High Speed, RS-232/422/423(188C)/485

Number of Channels:	Four (4) fully programmable Note: Due to pin count constraints, extended 'handshaking' capability not available (see pin-outs)
Data Rate:	4 Mbits/s per channel in Synchronous/HDLC mode 1 Mbits/s per channel in Asynchronous mode (RS-422 & RS-485) 250 Kb/s RS-423, MIL-STD-188C unbalanced Data rate will be within 1% of commanded rate. Data can be read 4µs after receipt in UART. These data rates are verified with all channels running simultaneously (RS423/Mil-Std-188C, unbalanced, sec. 7.2.1, prior to Notice 1 support added as of DOM 1/2013)
Data Transfer:	**Data transfers within 300 ns, no latency issues**
Receive/Transmit Buffers:	32 KB for each Receive and Transmit buffer. 16 bit data word format only
Power:	+5 VDC @ 0.2 A per module (typical/average – all channels operating)
Ground:	Ground return is to system ground
Weight:	1 oz. (28g)

RS-422/485 (Module PC) – Isolated, Four High Speed RS-422 / 485 Serial Communications

Number of Channels:	Four (4) fully programmable Note: Due to pin count constraints, extended 'handshaking' capability not available (see pin-outs)
Data Rate:	4 Mbits/s per channel in Synchronous/HDLC mode 1 Mbits/s per channel in Asynchronous mode (RS-422 & RS-485) Data rate will be within 1% of commanded rate. Data can be read 4µs after receipt in UART. These data rates are verified with all channels running simultaneously
Data Transfer:	**Data transfers within 300 ns, no latency issues**
Receive/Transmit Buffers:	32 KB for each Receive and Transmit buffer. Accessed in 16 bit mode only
Protection:	+/- 15KV ESD (human body model)
Transceiver:	Complies with ANSI/TIA/EIA-422/485-A-98 and ISO 8482:1987(E)
Power:	+5 VDC @ 0.4 A per module (typical/average – all channels operating)
Ground:	0.5 KV (min) isolation / independent channels isolated from system ground
Weight:	1 oz. (28g)



A/D (Module C1) – Ten A/D Channels (1.25 to 10.0 VDC FS) Uni or Bipolar

Resolution:	16-bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as Full Scale (FS) range inputs of 10.00, 5.00, 2.50, or 1.25 volts where range is -FS to +FS, or 0 to FS VDC. The ability to set lower voltages for FS assures the utilization of the full resolution.
Over-voltage protection:	No damage up to ±12 V continuous; ±30 V momentary
Open input sense:	This module will sense and report unconnected Inputs
Input impedance:	1 MΩ min.
Accuracy:	0.05 % FS range over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB's max. over temperature
Sampling rate:	200 KHz max per channel, programmable
Data buffering/triggering:	See Operations Manual for details
Bandwidth:	20 KHz per channel
Group delay:	30 μs (time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz
Common mode voltage:	Signal voltage plus Common mode voltage is 10.5 volts Note: A/D differential inputs must not "float". Input source must have return path to ground.
Output logic:	Bipolar output in two's complement. Bipolar output range from 8000 max. negative; 7FFF is max. positive (FS) Unipolar output range from 0 to FFFF (FS)
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2 (4KV transient with a peak current of 7.5A and T_C of approximately 60 ns)
Power:	+5 VDC @ 500mA typical, 750mA max.
Ground:	Channel inputs are differential, but referenced to system ground.
Weight:	1 oz. (28g)

A/D (Module C2) – Ten A/D Channels (5.0 to 40.0 VDC FS) Uni or Bipolar

Resolution:	16-bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as Full Scale (FS) range inputs of 40.00, 20.00, 10.00, or 5.00 volts where range is -FS to +FS, or 0 to FS VDC. The ability to set lower voltages for Full Scale Input assures the utilization of the full resolution. This module will not sense open Inputs.
Over-voltage protection:	±100 Volts
Input impedance:	500 KΩ min. (Differential)/ 250 KΩ min. (Single ended)
Accuracy:	0.1 % FS range over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB's max. over temperature
Sampling rate:	200 KHz max per channel, programmable
Data buffering/triggering:	See Operations Manual for details
Bandwidth:	20 KHz per channel
Group delay:	30 μs (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz
Output logic:	Bipolar output in two's complement. Bipolar output range from 8000 max. negative; 7FFF is max. positive (FS) Unipolar output range from 0 to FFFF (FS)
Common mode voltage:	Signal voltage plus Common mode voltage is 80 volts. Note: A/D differential inputs must not "float". Input source must have return path to ground.
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and T_C of approximately 60 ns)
Power:	+5 VDC @ 500mA typical, 750mA max.
Ground:	Channel inputs are differential, but referenced to system ground.
Weight:	1 oz. (28g)

A/D (Module C3) – Ten A/D Channels (4-25mA)

Resolution:	16-bit A/D converters. One per channel
Input format:	Single Ended
Input scaling:	Ten (10) unipolar channels, 0-25ma Full Scale (FS) This module will not sense open Inputs
Input voltage:	Not to exceed ±3 volts
Input impedance:	100 Ω min.
Accuracy:	0.1 % FS range over temperature. (no missing codes to 16 bits)
Linearity error:	±8 LSB's max. over temperature
Sampling rate:	200 KHz max per channel, programmable
Data buffering/triggering:	See Operations Manual for details
Bandwidth:	20 KHz per channel
Group delay:	30 μs (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz.
Common mode voltage:	Signal voltage plus Common mode voltage is 80 volts. Note: A/D differential inputs must not "float". Input source must have return path to ground.
Output logic:	Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and T_C of approximately 60 ns)
Power:	+5 VDC @ 500mA typical, 750mA max.
Ground:	Channel inputs are differential, but referenced to system ground.
Weight:	1 oz. (28g)

A/D (Module C4) – Ten A/D Channels (6.25 to 50.0 VDC FS) Uni or Bipolar

Resolution:	16-bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as Full Scale (FS) range inputs of 50.00, 25.00, 12.50, or 6.25 volts where range is -FS to +FS, or 0 to FS VDC. The ability to set lower voltages for Full Scale Input assures the utilization of the full resolution. This module will not sense open inputs.
Over-voltage protection:	±100 Volts
Input Impedance:	500 KΩ min. (Differential)/ 250 KΩ min. (Single ended)
Accuracy:	0.1 % FS range over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB's max. over temperature
Sampling rate:	200 KHz max per channel, programmable
Data buffering/triggering:	See Operations Manual for details
Bandwidth:	20 KHz per channel
Group delay:	30 μs (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz.
Common mode voltage:	Signal voltage plus Common mode voltage is 80 volts. Note: A/D differential inputs must not "float". Input source must have return path to ground.
Output logic:	Bipolar output range from 8000 max. negative; 7FFF is max. positive (FS) Unipolar output range from 0 to FFFF (FS)
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and T_C of approximately 60 ns)
Power:	+5 VDC @ 500mA typical, 750mA max.
Ground:	Channel inputs are differential, but referenced to system ground.
Weight:	1 oz. (28g)

A/D Combo (Module CA) – Six Channels (±40VDC) & Four Channels (4-25mA)

Specifications applicable to channels 1-6 (40 VDC A/D)

Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as Full Scale (FS) inputs of: 40.00, 20.00, 10.00, or 5.00 volts where range is -FS to +FS, or 0 to FS VDC. The ability to set lower voltages for Full Scale Input assures the utilization of the full resolution. This module will not sense open Inputs.
Over-voltage protection:	±100 Volts
Input impedance:	500 KΩ min. (Differential)/ 250 KΩ min. (Single ended)
Accuracy:	0.1 % FS range over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB's max. over temperature
Output logic:	Bipolar output range from 8000 max. negative; 7FFF is max. positive (FS) Unipolar output range from 0 to FFFF (FS)

Specifications applicable to channels 7-10 (4-25mA A/D)

Input format:	Differential (may be used as single ended by grounding one input, 0-25ma)
Input scaling:	Ten (10) unipolar channels, 0-25ma Full Scale (FS). This module will not sense open inputs
Input voltage:	Not to exceed ±3 volts
Input impedance:	100 Ω min.
Accuracy:	0.1 % FS range over temperature. (no missing codes to 16 bits)
Linearity error:	±8 LSB's max. over temperature
Sampling rate:	200 KHz max per channel, programmable 200 KHz per channel
Data buffering/triggering:	See Operations Manual for details)
Bandwidth:	20 KHz per channel
Group delay:	30 μs (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Output logic:	Unipolar output range from 0 to FFFF full scale

Specifications applicable to ALL channels:

Resolution:	16-bit A/D converters. One per channel
Sampling rate:	200 KHz max per channel, programmable
Data buffering/triggering:	26 KB FIFO/CH; See Operations Manual for details
Bandwidth:	20 KHz per channel
Group delay:	30 μs (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz.
Common mode voltage:	Signal voltage plus Common mode voltage is 80 volts. Note: A/D differential inputs must not "float". Input source must have return path to ground.
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and T_C of approximately 60 ns)
Power:	+5 VDC @ 500 mA typical, 750mA max.
Ground:	Channel inputs are differential, but referenced to system ground.
Weight:	1 oz. (28g)

I/O (Module D7) – Sixteen TTL Channels— Programmable for I/O

TTL Input

Input levels:	TTL and CMOS compatible, single ended inputs. Each channel incorporates a 100 KΩ pull-down resistor.
V in L:	0.8 V = "0"
V in H:	2.0 V = "1"
V in Max.:	5.5 V
I in:	± 50μA
Read delay:	300 ns
De-bounce:	Programmable per bit from 0 to 343s. LSB=programmable

TTL Output

Output levels:	TTL/CMOS, single ended outputs
Drive capability:	V out L: +0.55 V max. Low level output current: 24 mA (sink) V out H: 2.4 V min. High level output current 24 mA (source)
Rise/Fall time:	10 ns into a 50pf load
Write delay:	300 ns
Power:	+5 VDC @ 75 mA unloaded (@ 460 mA max if all Ch. max source)
Ground:	All grounds are common and connected/referenced to system ground
Weight:	1 oz. (28g)

I/O (Module D8) – Eleven (Sixteen*) Differential Multi-Mode Transceiver Channels

(* 16 channels available on certain supported platforms – either front and/or rear I/O connectivity – check pinouts)

Mode of Operation:	**RS-422 (Differential)**	**RS-485 (Differential)**
Differential Input		
Receiver Input Levels:	-10V to +10V (wrt system GND)	-7V to +12V (wrt system GND)
Receiver Input Sensitivity:	±200mV (differential)	±200mV (differential)
Receiver Input Resistance:	120Ω	>12kΩ
	(Each channel incorporates a 120 Ω termination resistor that can be programmed on a channel by channel basis)	
Read Delay:	300 ns	
De-Bounce:	Programmable per bit from 0 to 343s. LSB=programmable	
Differential Output		
Driver Output Voltage:	-0.25V to +5V max. (from either (+) or (-) pin with respect to system GND)	
Driver Output Signal Level: (Loaded Minimum)	±2V (differential)	±1.5V (differential)
Driver Output signal Level: (Unloaded Maximum)	±5V (differential)	±5V (differential)
Driver Load Impedance:	100Ω	54Ω
Max. Driver Current In Hi Z State (Power ON):	N/A	±100μA (differential)
Max. Driver current In Hi Z State (Power OFF):	±10 μA (differential)	±10 μA (differential)
Write Delay:	300 ns	300 ns
Protection:	Short circuit protected, thermal shutdown, built-in current limiting	
Rise/Fall Time:	31 ns into a 50pf load	
Power (Per 11 Channel Module):	+5VDC @ 200 mA, 360 mA fully loaded (54Ω load per channel)	
Ground:	All grounds are common and connected to system ground	
Weight:	1 oz. (28g)	

D/A (Module F1) – Ten D/A Outputs (±10 VDC)

Resolution:	16 bits/channel for either output range
Output Format:	Single ended
Output Range:	±10 VDC or 0 to 10 VDC, programmable
Output Impedance:	<1 Ω
System Protection:	Output is set to 0 at reset or power-on
Accuracy:	±0.05% FS range
Offset:	<1 mV over temperature
Non-Linearity:	±0.01% FS range over temperature
Gain Error:	±0.02% over temperature
Settling Time:	10 μs typ. (15 μs max.)
Data Buffer:	See Operations Manual for details
Load:	Can drive a capacitive load of 0.1 mfd. 20 mA/CH max. (Source or Sink). Short circuit protected. When current exceeds 20 mA for any channel, for >50ms, that channel is set to zero and a flag is set. All channels can be reset by a control port command.
Update Rate:	5 μs per channel
ESD Protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and T_C of approximately 60 ns)
Power:	+5 VDC @ 300 mA typical; add 2 mA per 1 mA load per channel
Ground:	All grounds are common, but are isolated from system ground
Weight:	1 oz. (28g)

D/A (Module F3) – Ten D/A Outputs (±5 VDC)

Resolution:	16 bits/channel for either output range
Output Format:	Single ended
Output Range:	±5 VDC or 0 to 5 VDC, programmable
Output Impedance:	<1 Ω
System Protection:	Output is set to 0 at reset or power-on
Accuracy:	±0.05% FS range
Offset:	<1 mV over temperature
Non-Linearity:	±0.01% FS over temperature
Gain Error:	±0.02% over temperature
Settling Time:	10 μs max
Data Buffer:	See Operations Manual for details
Load:	Can drive a capacitive load of 0.1 mfd. 20 mA/CH max.(Source or Sink). Short circuit protected. When current exceeds 20 mA for any channel, for >50ms, that channel is set to zero and a flag is set. All channels can be reset by a control port command
Update Rate:	5 μs per channel
ESD Protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and T_C of approximately 60 ns)
Power:	+5 VDC @ 300 mA typical; add 2 mA per 1 mA load per channel
Ground:	All grounds are common, but are isolated from system ground
Weight:	1 oz. (28g)

D/A (Module F5) – Four D/A High Current Outputs (±20VDC at 100 mA)

Resolution:	16 bits/channel for either output range
Output Format:	Single ended/Differential
Output Range:	±20 VDC or 0 to 20 VDC, programmable
Output Impedance:	<1 Ω
System Protection:	Output is set to 0 at reset or power-on
Accuracy:	0.05% FS range
Offset:	<1 mV over temperature
Non-Linearity:	±0.01% FS range over temperature
Gain Error:	±0.02% over temperature
Settling Time:	10 μs max
Data Buffer:	See Operations Manual for details
Load:	Can drive a capacitive load of 0.1 mfd. 100 mA/CH max. (Source or Sink). Short circuit protected. When current exceeds 110 mA for any channel, for >50ms, that channel is set to zero and a flag is set. All channels can be reset by a control port command.
Update Rate:	5 μs per channel
ESD Protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and T_C of approximately 60 ns)
Power:	+5 VDC @ 400 mA max. ±12 VDC @ 250 mA max.
Ground:	All grounds are common, but are isolated from system ground
Weight:	1 oz. (28g)

D/A (Module J3) – Ten D/A Outputs (±1.25 VDC)

Resolution:	16 bits/channel for either output range
Output Format:	Single ended
Output Range:	±1.25 VDC or 0 to +1.25 VDC, programmable
Output Impedance:	<1 Ω
System Protection:	Output is set to 0 at reset or power-on
Accuracy:	±0.05% FS range
Offset:	<1 mV over temperature
Settling Time:	10 μs max.
Data Buffer:	See Operations Manual for details
Load:	Can drive a capacitive load of 0.1 mfd. 20 mA/CH max. (Source or Sink). Short circuit protected. When current exceeds 20 mA for any channel, for >50ms, that channel is set to zero and a flag is set. All channels can be reset by a control port command.
Update Rate:	5 μs per channel
ESD Protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and TC of approximately 60 ns)
Power:	+5 VDC @ 300 mA typical; add 2 mA per 1 mA load per channel
Ground:	All grounds are common, but are isolated from system ground
Weight:	1 oz. (28g)

D/A (Module J5) – Ten D/A Outputs (±2.5 VDC)

Resolution:	16 bits/channel for either output range
Output Format:	Single ended
Output Range:	±2.5 VDC or 0 to +2.5 VDC, programmable. For other ranges contact factory
Output Impedance:	<1 Ω
System Protection:	Output is set to 0 at reset or power-on
Accuracy:	±0.05% FS range
Offset:	<1 mV over temperature
Settling Time:	350 μs max
Data Buffer:	See Operations Manual for details
Load:	Can drive a capacitive load of 0.1 mfd. 20 mA/CH max. (Source or Sink). Short circuit protected. When current exceeds 20 mA for any channel, for >50ms, that channel is set to zero and a flag is set. All channels can be reset by a control port command.
Update Rate:	5 μs per channel
ESD Protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and T_C of approximately 60 ns)
Ground:	All grounds are common, but are isolated from system ground
Power:	+5 VDC @ 300 mA typical; add 2 mA per 1 mA load per channel
Weight:	1 oz. (28g)

D/A (Module J8) – Four D/A High Voltage Outputs (± 20 to ± 80 VDC)

Resolution:	16 bits/channel
Output Range:	±20 to ±80 VDC Full Scale (FS) range. The ranges are programmable in pairs (i.e. one register controls the range for channels 1 and 2 and another register controls the range for channels 3 and 4)
Output Impedance:	<1 Ω
System Protection:	Output is set to 0 at reset or power-on
Accuracy (overall):	±20mV for ≤10V commanded output voltage (0ºC to 85ºC) (derates linearly to ±30mV from 0ºC to -40ºC) ±0.2% of commanded output voltage for >10V (0ºC to 85ºC) (derates linearly to ±0.3% from 0ºC to -40ºC)
Settling Time:	350 μs
Data Buffer:	See Operations Manual for details
Load:	10 ma/channel max. (Source or Sink up to 100 VDC). Short circuit protected
Update Rate:	5 μs per channel
Output Control:	Enable/Disable of DC/DC converter for output amplifier stage, via software.
Power:	+5 VDC @ 400 mA max. ±12 VDC @ 250 mA max.
Ground:	Each D/A channel has a separate return (ground) pin. Channel 1 and 2 share a common return. Channel 3 and 4 share a common return. The returns for all four channels are isolated from system (power) ground
Weight:	1 oz. (28g)

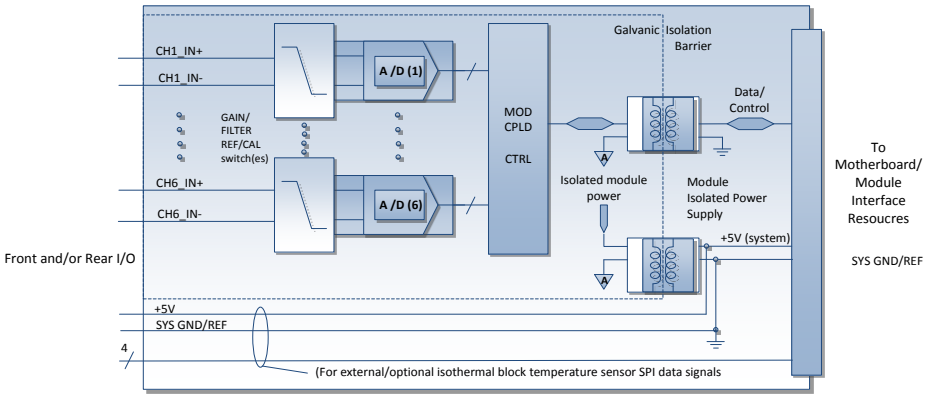
Thermocouple (Module G3) – Six Channel, Thermocouple Measurement Module

Number of channels:	Six; thermocouple or low-voltage A/D measurement (programmable)
Input Interface:	Independent differential input channels for thermocouple (or A/D) measurement
A/D Converter:	Independent 24-bit Sigma-Delta type (one for each channel)
Temperature range:	NIST temperature range (J, K, T, E, N, B, R, S thermocouple types)
Voltage measurement range:	±100 mV
Over-voltage input tolerance:	No damage to ±5 V continuous (applied at signal input)
50/60 Hz noise rejection:	>70 dB
CMR:	85 dB (minimum)
Differential input impedance:	>10M ohm
Digital output:	• IEEE 754-2008 (binary32) programmable for °C, °F, °K (programmed for temperature) • 24-bit (signed), based on % FSR (+/-100 mV) (programmed for raw A/D V-meas.)
Accuracy:	Based on minimum update rate and w/thermocouple block I/F compensation (interim – gain compensation pending*):

Type	Sub-range #1	Accuracy*	Sub-range #2	Accuracy*
J	-210 °C to 1200 °C	±1.2°C	-200 °C to 800 °C	±0.75 °C
N	-200 °C to 1300 °C	±1.2°C	-200 °C to 800 °C	±0.75 °C
K	-200 °C to 1372 °C	±1.3°C	-200 °C to 800 °C	±0.75 °C
T	-200 °C to 400 °C	±0.75°C	n/a	n/a
E	-200 °C to 1000 °C	±1.0°C	n/a	n/a
R / S	-50 °C to 1768.1 °C	±2.0°C	n/a	n/a
B	250 °C to 1820 °C	±2.0°C	n/a	n/a

± 0.2% FSR (programmed as/for raw A/D digital output)

Resolution:	0.01° (programmed for temperature)
Update rate:	Programmable between 4.17 – 470 Hz
Thermo-block interface:	Optional NAI ISO thermoblock: NAI P/N: ACC-ISO-THERM-BLK1 16-bit SPI digital temperature sensor (ADT 7320 or equivalent) +5V supply input required (<10 mA); transient protection on SPI (junction temperature @ ±1.0 °C deviation for range / 0 °C ice-bath design verified)
BIT (Built-in test):	Continuous background 'on-line' accuracy, OPEN detection capability
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4 KV transient with a peak current of 7.5A and a Tc of approximately 60 ns)
Power:	+5 VDC @ 310 mA typical (est.)
Ground:	Independent channels, isolated from system ground
Weight:	1 oz. (28g)



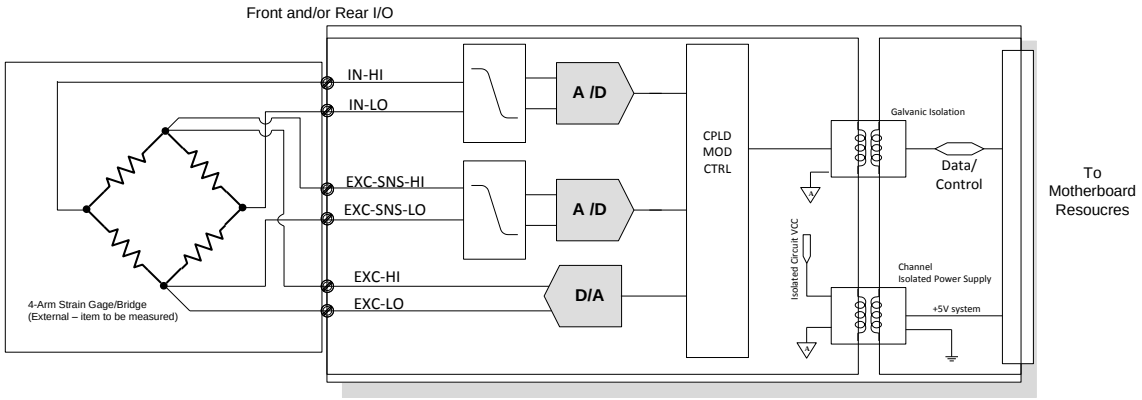
G3 Thermocouple (6 CH module)
Simplified Block Diagram

RTD (Module G4) – Six Channel RTD Measurement

Resolution:	16 bits/channel
RTD Interface:	4, 3, or 2-wire RTD interface capability. Specifically designed for use with 100Ω 200Ω, 500Ω, 1000Ω, and 2000Ω RTD's, or any RTD whose maximum operating resistance is less than 6500Ω.
Open Line Detection:	Ability to detect an open in any line or RTD in all wire modes
Excitation:	210 µA per channel
Accuracy:	0.05% of full-scale value
Update Rate:	Each channel is updated at 16.7Hz
Output Format:	Resistance
ESD Protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a T_C of approximately 60 ns
Power:	+5 VDC @ 100 mA typical
Ground:	All channel returns are common but are isolated from system ground
Weight:	1 oz. (28g)

Load/Strain (Module G5) – Four Channel, Load Cell / Strain Gage Module

Number of Channels:	Four differential Input channels for load cell measurement
Input Interface:	Conventional 4-arm Wheatstone bridge, 4 or six wire interface
A/D Converter:	24 bit Sigma-Delta
Output Resolution:	24 or 16-bit
Accuracy:	± 0.1% Full-Scale (FS) range
Digital Output:	Percent of Full Scale (Ratio (Vin/Vexc))
Gain Settings:	1, 8, 16, 32, 64, and 128 (programmable)
Input Impedance:	> 10 M-ohm
Input Coupling:	DC
Bridge Excitation Voltage:	Dual Independent Sources, Programmable 0 – 4.85 V DC (source 1 for CH1,CH2; source 2 for CH3, CH4)
Output Current (Maximum):	210 mA / source (maximum current is cumulative between channel pairs)
Remote Voltage Sensing:	Yes
Output Data Rate:	4.7 Hz to 4.8 KHz (dependent on programmable filter settings)
BIT (Built-in test):	Continuous background 'on-line' accuracy, OPEN detection capability
ESD Protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4 KV transient with a peak current of 7.5A and a Tc of approximately 60 ns)
Power:	+5 VDC @ 210 mA typical (est.)
Ground:	Channels isolated from each other and system ground
Weight:	1 oz. (28g)



G5 Strain Gage (4 CH isolated)
Single Channel Example Block

DISCRETE (Module K6) (ver. 4) – Sixteen (16) Programmable Discrete I/O Channel

Features:

- Programmable for Input (voltage or contact sensing) or Output (current source, sink or push-pull) per channel/bank
- Continuous Background BIT Testing (during normal operation, status provided for channel health and operation feedback)
- Ability to sense broken input connection and if input is shorted to +V or to ground
- Ability to read I/O voltage and output current for improved diagnostics (indicates if load is connected)
- Ability to current share, by connecting multiple outputs in parallel, to sink/source up to 2A per channel/bank
- Ability to handle high inrush current loads (e.g. two #327 incandescent lamps in parallel)
- Supports 'dual turn-on" (series channel output) applications (e.g. dual series 'key' missile launch control)
- Software compatible with previous versions – additional functions provided via supplementary memory register locations

Input Characteristics:

Input Range:	0 to +60 VDC. Programmable for either voltage or switch closure sensing
Over-Voltage Surge Protection:	80 VDC max. (< 50ms);100 VDC max. (< 1µs)
Voltage/Contact Sensing:	Software selectable per bank. When the input channel is utilized for direct voltage sense, Vcc is not required. When input is used to detect switch closures, Vcc is required to provide a current source (pull-up). Vcc per channel bank must be between 5 VDC min. and 60 VDC max. A module has 4 Vcc banks, each with 4 channels for a total of 16 channels/ module.
Input Pulse Detection:	A pulse, of 20.48µs minimum width, will be sensed and reported by the appropriate High–Low or Low-High transition status/interrupt
Input Impedance:	1MΩ (with or without power applied to module)
Switching Threshold:	Four levels (High, Low, Short to +V, Short to ground) are programmable from 0 to 60 VDC with 10-bit resolution
Voltage Measurement:	User can read input voltage of each channel LSB=100mV; Accuracy: ±3 LSB's (300 mV) over temp.
HIGH/LOW Differential (Hysteresis):	0.25 V min. recommended; Programmable by using Upper & Lower thresholds
De-bounce:	Programmable per channel from 0 to 1.34 seconds (LSB= 20.48 µs; 16-bit resolution)
Update Rate:	Each channel is updated every 20.48 µs

Output Characteristics:

Output Formats:	Low-Side (I sink), High-Side (I source) or Push-Pull (I source-sink); programmable per channel
Output Voltage Range:	0 to +60 VDC. (Output voltage is defined by the user provided Vcc applied to channel bank). Low-side drive does not require Vcc. High-side and push-pull drive requires Vcc.
Over-Voltage Surge Protection:	80 VDC max. (< 50ms) 100 VDC max. (<1µs)
Output Current:	0.5A maximum (28V Vcc typical) per channel. 2A total per Vcc bank if outputs are through front panel connectors (total Module capacity 8A). 1A total per Vcc bank if outputs are through rear connectors (total Module capacity is then 4A). Short circuit protected.
Current Share Applications:	Outputs may be connected in parallel to provide up to 2A source/sink per Vcc bank (See programming details)
Over-Current Protection:	Individual channel will shut down when an over-current (0.75 A) is sensed for @ 20 µs.
Output Load:	Directly drives inductive loads (relays); Reverse current diode is incorporated Can handle high inrush current lamp loads (e.g. two #327 lamps in parallel)
Output Impedance:	Lo-side drive: 0.25 Ω typical; Hi-side drive: 0.5 Ω typical;
Write Delay:	20.48 µs
Update Rate:	Each channel is updated every 20.48 µs
Current Measurement:	User can read output current of each channel LSB=3mA; Accuracy: The greater of ±10% of Signal or ±20 mA over temp.
Voltage Measurement:	User can read voltage of each channel LSB=100mV; Accuracy: ±3 LSB's (300 mV) over temp.

General Characteristics:

Isolation:	Module power returns (GND) and I/O to System Ground: 500 volts; Proper polarity for Vcc/GND and I/O must be preserved (GND ≤ I/O ≤ Ext. VCC)
Power:	5 VDC @ 400 mA. For contact sensing, add (Vcc x Iset) x4 per bank of 4 channels
Ground:	Four (4) ground pins per module (one for each bank of 4 channels). All grounds are common within the module but are isolated from system ground
Weight:	1 oz. (28g)

Discrete (Module K7) - Isolated, Programmable, Bi-Directional I/O Switch

Input

Channels/Module:	12 / (16 CH available on select platforms) (I/O channel count may be limited to 12 channels on certain platforms; check pin-out)
Input Range:	0 to ±80 VDC
Input Pulse Detection:	A pulse, of 40µs min. width, will be sensed and indicated by the appropriate Hi–Lo or Lo-Hi Transition Interrupt
Input Impedance:	2 MΩ
Switching Threshold:	Levels are programmable from 0 to 80 Vrms with 10-bit resolution (0.98% FS) On/Off
Accuracy of Set Point:	The greater of 5% signal value or 0.25 V
ON/OFF Differential:	0.50 V minimum recommended
De-bounce:	Programmable per bit from 0 to 2.62s LSB= 40µs
Update Rate:	Each channel is updated every 5µs
Over-Voltage Protection:	Input clamped at ±80 V_{DC} or external source voltage applied to 'VCC' pin (whichever is smaller; see pinout)
Voltage Measurement:	User can read output voltage of each channel (isolated 10-bit A/D) LSB=163mV; Accuracy: ±3 LSB's (498 mV) over temperature

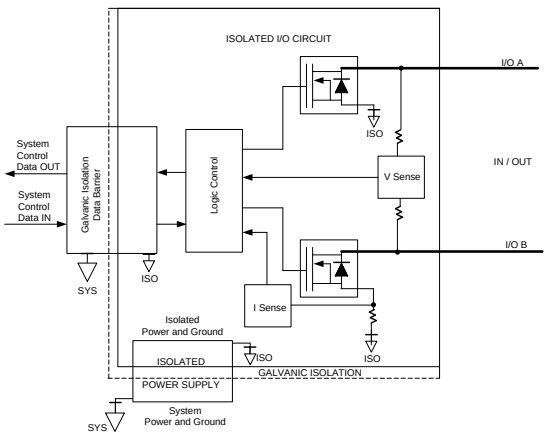
Bi-Directional Switch

Switch Format:	Isolated bi-directional (AC/DC) MOSFET switch
Switch Current:	0-600mA per channel
Switch Impedance Open:	2 MΩ
Switch Impedance Closed:	0.5Ω typical, 1Ω max
Current Measurement:	User can read AC/DC current through switch, independently for each channel LSB=3mA; Accuracy: The greater of ±10% of Signal, or ±20mA over temperature
Measurement Update Rate:	Each channel is updated every 5 µs

Isolation

Isolation:	500 V (between channels and each channel to system GND)
Power (Per Module):	+5VDC / 340 mA (est. typ.)
Weight:	1 oz. (28g)

K7 MODULE
Channel Block Diagram

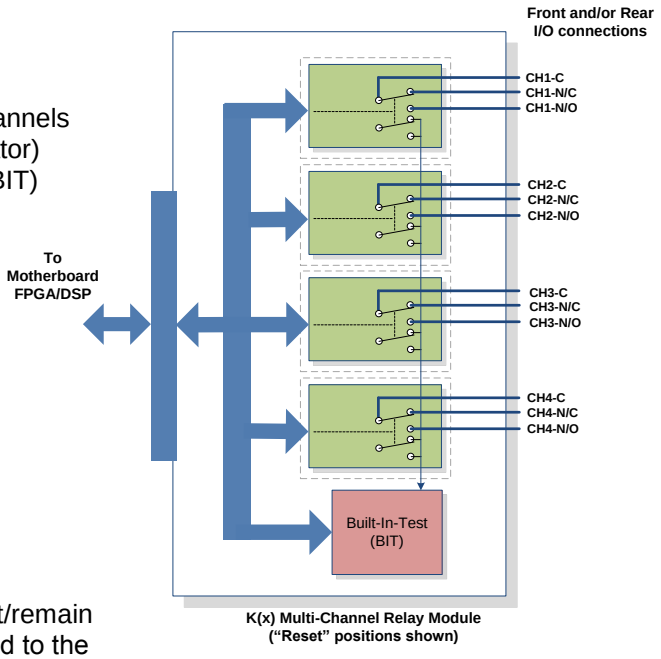


Relay (Module KN, KL) – Isolated, Four Independent Relay Channels

Channels:	Four (4), independent, isolated from each other and system/power ground
Switching voltage:	220 V_{DC} / 250 V_{AC} (max.) (with resistive load)
Switching current:	2 A (max.)
Switching power:	60 W / 62.5 VA (max.)
Initial contact resistance:	< 150 mΩ
Contact type/material:	Bifurcated / PdRu + Au covered
Operate time:	1 ms (typ.), 3 ms (max.)
Release time:	1 ms (typ.), 3 ms (max.)
Bounce time:	1 ms (typ.), 5 ms (max.)
Initial dielectric strength:	500 Vrms (between open and adjacent contacts) 1500 Vrms (between contact and coil)
Surge withstanding voltage:	500 Vrms (between open and adjacent contacts) 2000 Vrms (between contact and coil)
Capacitance:	10 pf (max.) (between coil, adjacent & open contacts)
Mechanical endurance:	1 x 10^8 operations/cycles (typ.)
Power:	+5 V_{DC} @ 220 mA (est. typ., all channels energized)
Ground:	Isolated signal/contacts
Weight:	1 oz. (28g)

Features

- ✓ (4) independently controlled mechanical contact relay channels
- ✓ Non-Latching or Latching options (see type/code designator)
- ✓ 1 Form C contacts DPDT / changeover (2nd Form C for BIT)
- ✓ Continuous Background Built-In-Test (BIT)



K(x) Multi-Channel Relay Module ("Reset" positions shown)

K* - Module Relay Type / Code Designator

Module Designation	RELAY type
KN	4x Non-Latching
KL	4x Latching

Description (Relay Code Type):

KN: The relays utilized on the KN module power-on default/remain de-energized or in the "reset position" until commanded to the "set" position. The contacts will then remain in the "set" position until commanded to the "reset" position or if power is removed from the card/module.

KL: The relays utilized on the KL module utilize magnetic latching to assure that once a relay channel is 'set' or 'reset', even if power is removed from the card/module, the channel will remain at the last commanded position.

LVDT (Module L*) – Four Isolated LVDT Measurement Channels (2, 3 or 4 Wire)

***See P/N**

Resolution:	16 bit
Input Format:	LVDT or RVDT
Input Voltage:	Auto ranging from 2.0 to 28 V_{RMS}
Excitation Voltage:	2-28 Vrms; Required for computation of 2-wire digital measurement output, 3 or 4 wire out-of-phase signal/noise rejection and for excitation loss status
Input Impedance:	60 KΩ
Accuracy:	±0.025% FS range
Bandwidth (BW):	Default factory setting is 10% of excitation to 100 Hz max. However, BW is programmable on a per channel basis. User has to program all parameters for each boot up or parameter will be set to the default value.
Frequency:	Specify between 360 Hz to 20 KHz, (See Part Number)
Phase Shift:	Automatically compensates for phase shifts between the transducer excitation and output up to ± 60° (3, 4-wire units ignore phase shift)
Wrap Around Self-Test:	Three powerful test methods are described in the Programming Instructions
Power:	+ 5 VDC @ 400mA
Ground:	Isolated signal and excitation. Channels individually isolated from each other and from system ground
Weight:	1 oz. (28g)

S/D (Module S*) – Four Isolated Synchro/Resolver Measurement Channels

***See P/N**

Resolution:	16 bits (up to 24 bits for two-speed configuration)
Input Format:	Synchro/Resolver programmable. Default will be Synchro.
Input Voltage:	See P/N
Input Impedance:	60 KΩ min. at 26V_{L-L}; 260 KΩ min. at 90V_{L-L}
Accuracy:	±1 arc-minute for single speed inputs ±1 arc-minute divided by the gear ratio for two-speed inputs
Tracking Rate:	190 RPS (Referred to the Fine input for two-speed configuration)
Bandwidth:	Default set at factory but per channel field programmable
Frequency Input:	50 Hz to 20 KHz (See part number)
Phase Shift:	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°.
Wrap Around Self Test:	The three different powerful test methods are detailed in the Description section and further described in the Programming Instructions.
Reference Input:	See P/N
Reference Zin:	100 KΩ min.
Angle Change Alert:	Each channel can be set to a different angle differential. When that differential is exceeded, an interrupt (if enabled) is triggered. Default: “Ch. Disabled”. MSB=180°; Min. differential is 0.05°. Max differential that can be programmed is 179.9°.
Velocity, Digital:	16-bit resolution; Linearity: 0.1%. Scalable to 0.1°/sec resolution
Power:	+ 5 VDC @ 400 mA
Ground:	Isolated signal and reference. Channels individually isolated from each other and from system ground
Weight:	1 oz. (28g)

D/S (Module 6*) – Three Isolated Digital-to-SYN/RSL Ch, 0.25 VA Power Output

***See P/N**	(Applies to each channel unless noted otherwise)
Number of Channels:	Three
Resolution:	16 bits (.0055°)
Accuracy:	± 0.1°
Output Format:	Synchro or Resolver, galvanic isolation (see part number)
Output Load:	0.25 VA @ 90 VL-L, 26 VL-L and 11.8 VL-L (Power reduces linearly as output voltage is reduced) Short circuit protected
Output Control:	Module outputs can be turned ON/OFF
Regulation (VL-L):	±5% max. (No load to Full load)
Ratio:	Dual speed, Programmable, Set any ratio between 2 and 255 (CH 1 and 2)
Rotation:	Continuous rotation or programmable Start and Stop angles. 0 to ±13.6 RPS with a resolution of 0.015°/sec. Step size is 16 bits (0.0055)° up to 1.5 RPS, then linearly increases to 12 bits (0.088°) at 13.6 RPS
Reference Input Voltage:	Galvanic isolation. Uses 1 ma max/Channel (See part number)
Reference Frequency:	47 Hz to 10 KHz (See part number)
Phase Shift:	0.5° max. (Between output and reference)
Settling Time:	Less than 100 microseconds
Module Power:	+5VDC @ 30 mA ±12VDC @ 190 mA (no-load) (Add 13mA of ±12VDC for every 0.1 VA of output load per channel)
Ground:	Isolated signal and reference. Channels individually isolated from each other and from system ground
Weight:	1 oz. (28g)

DLV (Module 5*) – Three Isolated DLV Stimulus Channels, LVDT or RVDT Outputs

***See P/N**

	(Applies to each channel unless noted otherwise) Programmable 3/4 or 2-Wire
Number of Channels:	3 (2-wire or 3,4 - wire)
Resolution:	16 bits (.001526% FS)
Linearity:	±0.1% FS
Output Gain:	±0.1%
Output Format:	Configurable for either 3/4-wire or 2-wire. Galvanically isolated. Output voltage is programmable fixed or ratio-metric
Output Voltage:	Programmable (See code table and part number)
Output Load:	0.1 VA max @ 11.8 Vrms or 28 Vrms (de-rates linearly as voltage is decreased) (See code table)
Regulation (VL-L):	±5% max. No load to Full load
Excitation Input Voltage:	(See part number), Galvanic isolated. Uses 1 mA max/Channel
Excitation Frequency:	47 Hz to 10 KHz (See part number)
Phase Shift (A/B):	0.5° max. (Between output and reference) (Programmable phase shift)
Settling Time:	Less than 100 microseconds
Module Power:	+5 VDC @ 30 mA ±12 VDC @ 190 mA (no-load) (Add 0.013 A of ±12 VDC for every 0.1 VA of output load per channel
Ground:	Isolated signal and excitation. Channels individually isolated from each other and from system ground
Weight:	1 oz. (28g)

Encoder (Module E7) – Four (4) Isolated SSI, A-Quad-B Encoder / General Counter

Channels/Module:	4 channels; individually isolated; Independently programmable for selected operation mode

SSI Mode

I/O Voltage Range:	TTL/RS422/485 (single-ended or differential)
Operational Modes:	Each channel, programmable for either “Standard Controller” or “Listen Only”
SSI “Listen / Standard” Mode:	SSI Data Word Length (up to 32 bit programmable)
Data Word Encoding:	Binary or Gray Code (programmable)
Parity:	Odd, Even, None with “0-bit” (programmable)
Interrupt Generation:	Programmable event(s)
SSI “Standard” Mode:	SSI clock rate: 1 μs to 32 μs (1 μs resolution programmable) SSI clock transition: Rising / Falling edge (programmable) SSI clock watchdog: Preload (up to 32-bit programmable)

Incremental Quadrature (A-QUAD-B) Encoder / Counter Mode

Programmable Type:	Quadrature (Differential; A, B, INDEX), UP, DOWN, PRE-LOAD, MODULUS-N
Pre-Load / Compare Registers:	32 bit
Resolution:	Programmable 1x, 2x or 4x resolution multiplier
De-Bounce (Filter):	Programmable per bit from 0 to 3.2768 ms (16-bit resolution). LSB= 50 ns
Timer:	Programmable internal interval timer with 32-bit pre-scaler
Count Rate:	25 MHz (max)

General

Maximum Signal Voltage:	24 VDC
Isolation:	500 V (between channels and each channel to system GND)
Power (Per 4 Channel Module):	+5 VDC @ 1 A (max)
Weight:	1 oz. (28g)

DC Power Supply (Module V*) - Isolated ±15V DC/DC converter

The V* module provides either one (V1) or two (V2) identical fully isolated bipolar ±15VDC DC/DC converters. Each DC/DC converter can source and sinks up to 450mA. Each converter can be used independently and features current output and voltage output monitoring, and a programmable current limit. Both converters are isolated and may be tied in series for applications requiring higher output voltages. For clarity, the two converters are referenced as channel 1 & 2.

V* - Module Type Designator

Module Designation	Channels
V1	Single Channel, Isolated
V2	Dual Channel , Isolated

Input

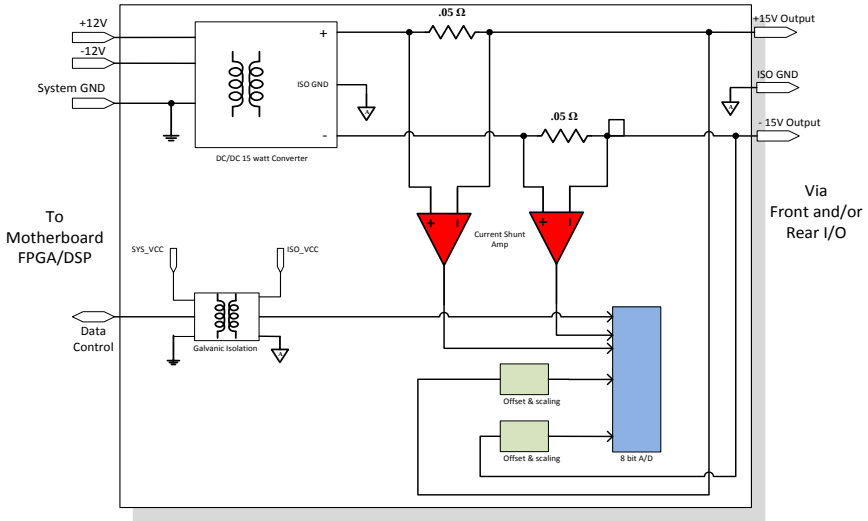
Input Voltage:	±12V_{DC}
Input Voltage tolerance	±20%

Output

Output Voltage:	±15V_{DC}
Output Regulation	±1%
Output Current (maximum):	±450 mA
Output Voltage Measurement:	Output voltage, 1mV; Accuracy: ±1 LSB
Output Current Measurement:	Output voltage, 1mA; Accuracy: ±1 LSB
Output Overload protection:	Programmable from 1mA to 450mA
Efficiency:	> 80%

Power Input

Power +5V:	+5V_{DC} / 210 mA max
Power ±12V_{DC}:	±12V_{DC} / 550 mA max.
Ground:	Each channel isolated from each other and system/power GND.
Weight:	1 oz. (28g)

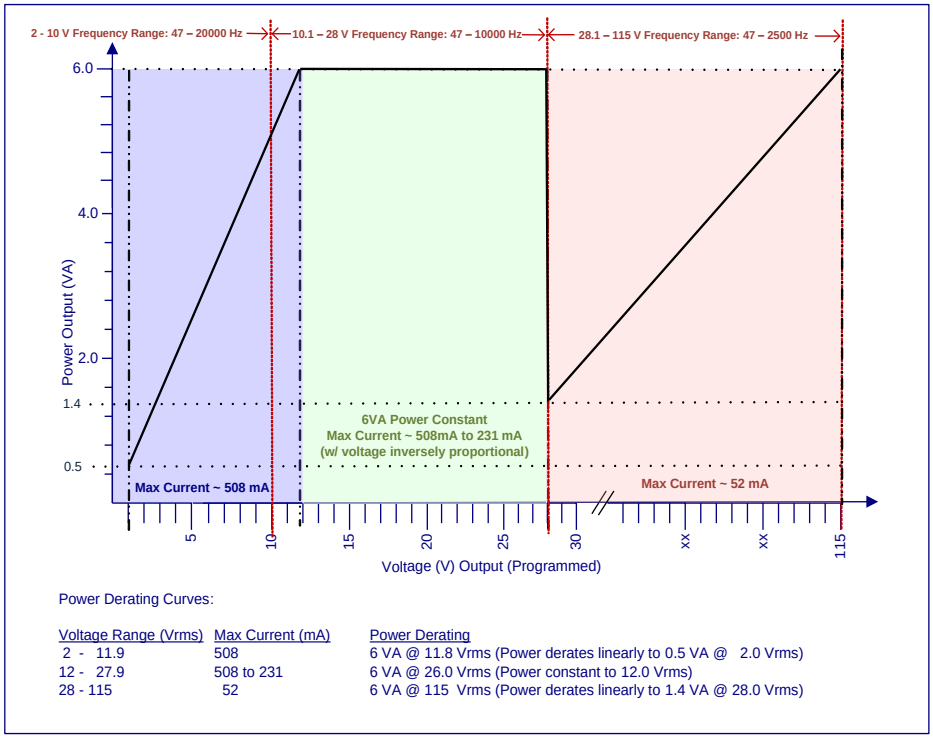


Block diagram: (1) Channel example

Reference (Module W*) – AC Source, Isolated, Programmable

*See P/N

Voltage Output:	2 Vrms to 115 Vrms, Programmable with a resolution of 0.1V 2.0 to 10.0 Vrms / 47 Hz to 20 KHz frequency range 10.1 to 28.0 Vrms / 47 Hz to 10 KHz frequency range 28.1 to 115.0 Vrms / 47 Hz to 2.5 KHz frequency range
Accuracy (No Load):	±3% of setting < 15 KHz ±6% of setting ≥ 15 KHz
Regulation:	±5% (No Load to Full Load)
Output Drive:	6 VA maximum (See detailed description of Output Drive)
Output Protection:	Over-current (10x automatic retry; @ 1.3 sec int.; afterwards, shutdown w/ manual reset)
Frequency:	47 Hz to 20 KHz Programmable with 0.1 Hz steps
Frequency Accuracy:	±0.1% of programmed frequency or ±1 Hz (whichever is greater)
THD:	3% (maximum)
Reference Output Drive:	(See detailed characterization)
Power:	+5 VDC @ 10 mA ±12 VDC @ 150 mA (Quiescent, no load) Add ±12 VDC @ 46 mA for every 1 VA Load
Ground:	Isolated from system ground
Weight:	1 oz. (28g)



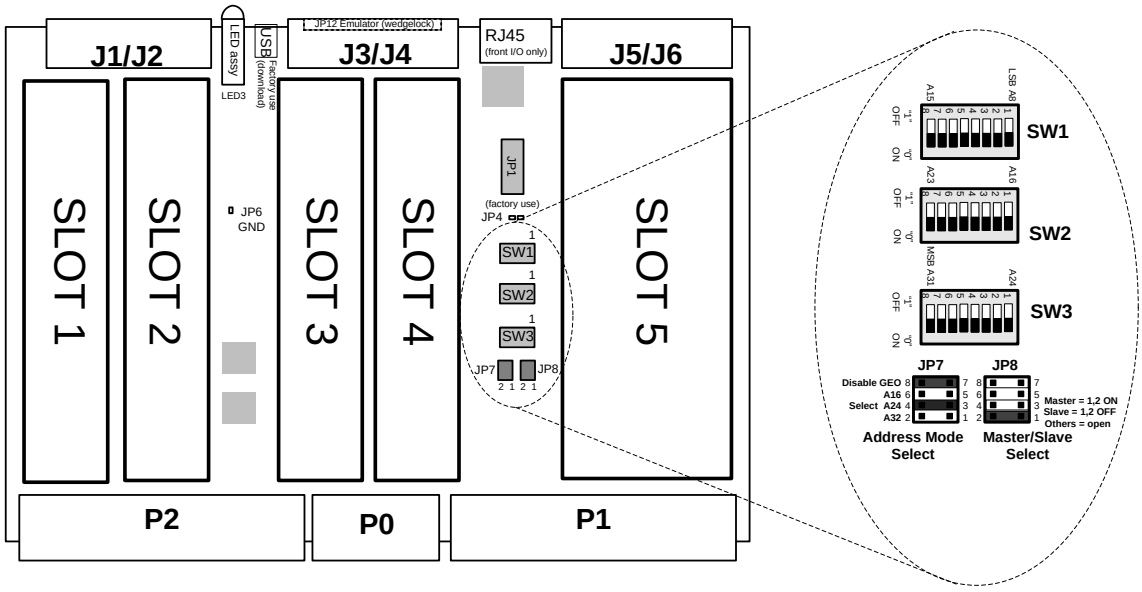
Power Derating Curves:

Voltage Range (Vrms)	Max Current (mA)	Power Derating
2 - 11.9	508	6 VA @ 11.8 Vrms (Power derates linearly to 0.5 VA @ 2.0 Vrms)
12 - 27.9	508 to 231	6 VA @ 26.0 Vrms (Power constant to 12.0 Vrms)
28 - 115	52	6 VA @ 115 Vrms (Power derates linearly to 1.4 VA @ 28.0 Vrms)

64EP3 Address Configuration

Master/Slave Configuration

The 64EP3 motherboard may be set in a 'Master' or 'Slave' VMEbus card mode. This is accomplished by setting a specific jumper configuration. Upon power-up, the card will determine the VMEbus mode based on the jumper configuration. In 'Slave' mode, the card will respond to slave W/R commands and provide typical memory defined register data access/requests. In 'Master' mode, the card will respond to W/R data access, but also can be used as a conduit for VMEbus requests to other NAI cards on the VMEbus. Master VMEbus mode would typically be used in a multi-card application when either Ethernet or the processor control is used for direct multi-card access through one 'Master' card (i.e. can function as a typical slot 0 master controller).



(**Note:** Picture not to scale)

Slave Configuration

The VME bus interface will respond to A32:D16, A24:D16 and A16:D16 DTB cycles.

A32 mode: Unit responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 4096 byte boundaries.

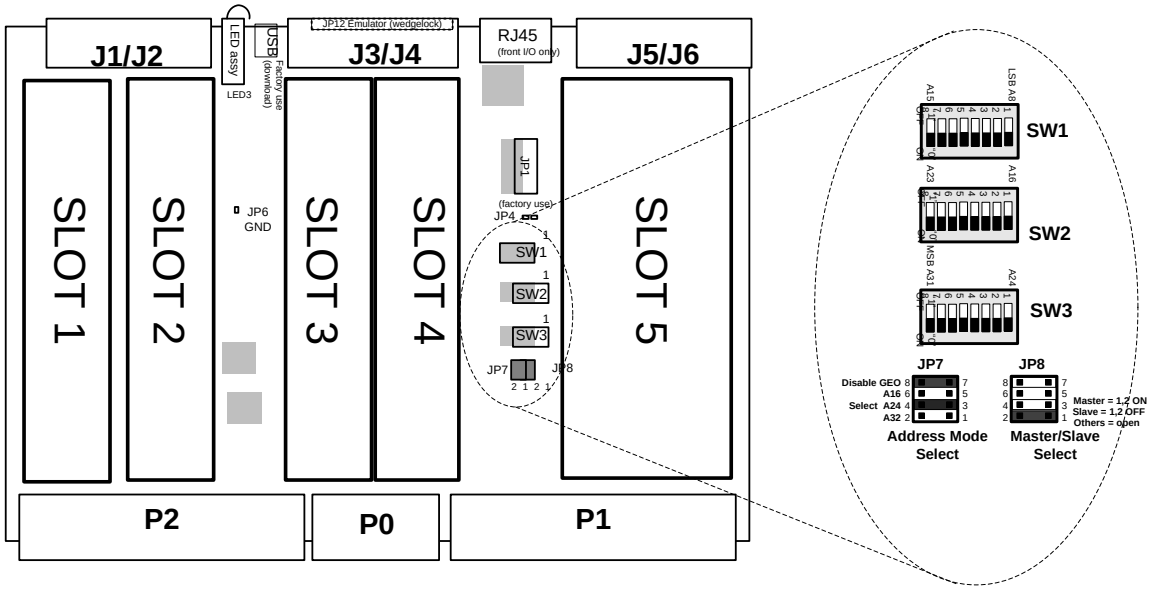
A24 mode: Responds to address modifiers 3A, 3D, 3E and 39. Base address can be set anywhere in the 16 Megabyte address space on 4096 EVEN byte boundaries.

A16 mode: Responds to address modifiers 2A, 2D, 2E and 29. Base address can be set anywhere in the 64 Kbyte address space on 4096 byte boundaries.

Geographical Addressing

Enable Geographical Addressing by removing jumper from JP7-7,8. Disable Geographical Addressing by adding jumper to JP7-7,8. See card layout figure above. Address switches A8, A9, A10 & A11 are ignored. Card requires 4096 byte boundaries. For detailed examples, click here to view the 64xxx_VME_Board_Addressing document**,** or visit the download section of our website http://www.naii.com/downloads/**.**

(**Note**: Picture not to scale)



This card will respond to address modifier 2Fh for A24 Address mode, where the 5 MSBs of the A24 address are the 5 bits defined by the slot in VME backplane. The card can optionally be interrogated at 2Fh to determine resource requirements and available functionally. Using the address modifier 2Fh, the following need to be written to the card:

- The base address that the card should respond to
- The address modifier (A16, A24, A32)
- Then enable the card

For example: If the card is in slot #10 of the system rack/chassis, the 5 MSBs are 01010 so the address of the CSR registers are: 0101 0 111 1111 1111 xxxx xxxx or 57FFxx h (xx is CSR register offset)

- Write to address 57FF63 h, the A31 – A24 base address bits, for example 01h
- Write to address 57FF67 h, the A23 – A16 base address bits, for example 02h
- Write to address 57FF6B h, the A15 – A8 base address bits, for example 04h
- Write to address 57FF6F h, the address modifier to respond to shifted up 2 bits, for example 28h(0A<< 2)
- Then Write to address 57FFFBh, 10h to enable the card

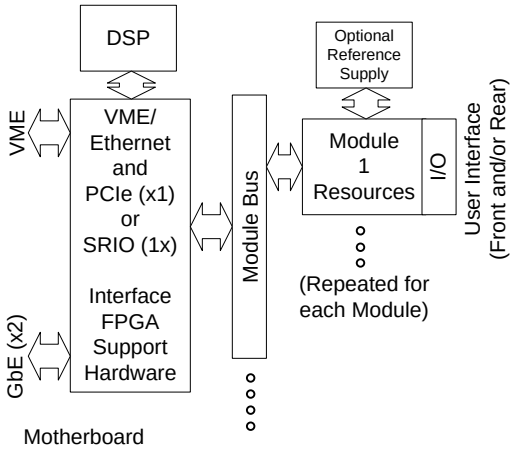
The card will now respond to the base address (010204 in the example) and address modifier (0A in example) programmed. The base address and address modifier can be changed at any time

PRODUCT CONFIGURATION AND MEMORY MAP

This design provides multiple functions on a single VME card. When ordering, the customer selects an assortment of up to five modules to populate this 5-slot motherboard. The memory map follows the order of modules specified in the part number.

To address the register of any module, use the Base address to the entire card, add the Module Offset depending upon its slot (400, 800, 1000…etc.) and then add the Register Offset of interest (see module memory map). The memory map of each selected module counts from, or is superimposed over its respective module offset.

Thus, Address = Base + Module Offset + Register Offset.



Motherboard
Block Diagram

For example, if a Digital I/O module were selected to populate module 1 and a Discrete I/O module were selected to populate module 4, then:

Address = Base + Module 1 Offset 400 + Digital I/O register 410 = Base + 410 hex
Address = Base + Module 4 Offset 1000 + Discrete I/O register 022 = Base + 1022 hex

(See following page for memory map pictorial.)

64EP3 Card-Level Module Configuration and Memory Mapping

0000	General Use (Board Level)…
0002	
0004	General Use
0006	Offset 000
0008	
.	
.	
.	
03FC	
03FE	

0400	Module 1 Function Registers…	**400 + Len(M1) + Len(M2)**	Module 3 Function Registers…	400 + Len(M1) + Len(M2) + **Len(M3) +** Len(M4)	Module 5 Function Registers…
0402		402 + Len(M1) + Len(M2)		402 + Len(M1) + Len(M2) + **Len(M3) +** Len(M4)	
0404		.		1004	
0406	Slot 1	.	Slot 3	.	Processor Slot 5
0408	*1 Offset 400	.	*1 Offset C00	.	*1 Offset 1400
.		.		.	
.		.		.	
.		.		.	
07FC		.		.	
400 + Len(M1) -2		400 + Len(M1) + Len(M2) + Len(M3) - 2		400 + Len(M1) + Len(M2) + **Len(M3) +** Len(M4) + Len(M5) - 2	

400 + Len(M1)	Module 2 Function Registers…	**400 + Len(M1) + Len(M2) + Len(M3)**	Module 4 Function Registers…
402 + Len(M1)		402 + Len(M1) + Len(M2) **+ Len(M3)**	
.		.	
.	Slot 2	.	Slot 4
.	*1 Offset 800	.	*1 Offset 1000
.		.	
.		.	
.		.	
400 + Len(M1) + Len(M2) -2		400 + Len(M1) + Len(M2) + **Len(M3) +** Len(M4) - 2	

*1 Unless otherwise specified in the module descriptions or memory maps, module (slots) 1-4 (A-size modules) typically requires module memory space 'length' (Len) or 'size' defined as 0x400 – offsets noted are provided for convenience.

All Addresses not specified through xFFF(H) are reserved (where x is the next highest integer rounded up). Any address NOT SPECIFIED within 2048 byte block (up to 7FFh) is reserved.

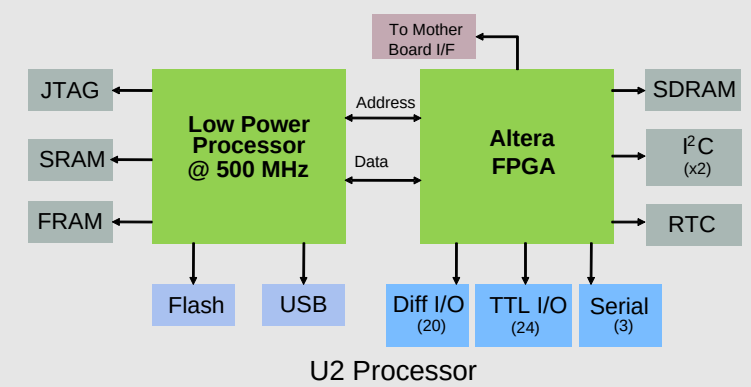
PROCESSOR (MODULE U2)

Principle of Operation

The U2 is a platform module for the development of custom application solutions. It was designed to support user development utilizing VisualDSP++ which is an integrated software development and debugging environment (IDDE) used with Analog Devices' Blackfin processors. The U2 module adds single board computer resources and the computational power of the Analog Device's (ADI) Blackfin® BF533, to NAI processor module-supported platforms (i.e. NAI 75DP3, 64EP3, 64DP3) with additional configurable multi-function I/O capabilities.

Blackfin BF533 Features

- High performance Blackfin processor
- 40-bit shifter
- 148K bytes of on-chip memory
- 2 memory-to-memory DMAs
- Three 32-bit timer/counters
- Real time clock and watchdog timer
- 32-bit core timer
- UART



U2 Processor

U2 Module Resources

- 16MB of SDRAM
- 8MB of nonvolatile flash memory
- 16MB of nonvolatile serial SPI flash memory (available for program storage)
- 128Kwords of multiport shared SRAM
- 8Kbytes of nonvolatile ferroelectric random access memory (FRAM)
- VME/PCI bus slave and bus mastering (or controller)
- Modbus system, access to local and off card resources
- Battery backed up RTC
- 24 TTL, programmable GPIO signals
- 20 differential, programmable GPIO signals
- JTAG-Plug that supports all of Analog Devices' JTAG Emulator

Processor Overview

In addition to being the primary processor for interfacing to other onboard multi-function modules, the U2 processor module, based on the Analog Devices Blackfin 533 DSP Processor itself, has many built in feature that can be easily accessed.

The U2 processor module, based on the Analog Devices Blackfin 533 DSP processor, is the primary processor module for interfacing to other onboard multi-function modules and has many built in features that can be easily accessed, including:

- Real time clock
- TTL I/O
- Differential I/O
- FRAM
- FLASH
- SRAM
- SDRAM
- RS232
- I2C
- USB

The real time clock (RTC) can be used to provide a system time and date function or can be used as an event timer. Methods are provided in the U2 proc library to access the RTC features. These methods are located in the ProcRTC.c and ProcRTC.h files.

The U2 processor module provides 24 TTL inputs/outputs. These lines can be set up by the user as needed. Methods are provided in the U2 proc library to access the TTL I/O features. These methods are located in the ProcTTL.c and ProcTTL.h files. (**Note:** Only TTL – CH13 and CH14 are available in the SIU chassis).

The U2 processor module provides 20 differential inputs/outputs. These lines can be set up by the user as needed. Methods are provided in the U2 proc library to access the Differential I/O features. These methods are located in the ProcDIFF.c and ProcDIFF.h files. (**Note:** Only DIFF – CH3, CH6, CH12 and CH13 are available in the SIU chassis).

There are 8Kbytes (8192) of non-volatile ferroelectric random access memory (FRAM) available for data storage. This can be used to store any data that needs to be available after a system power down. The FRAM is connected to the processor through the serial peripheral interface (SPI). Methods are provided in the U2 proc library to access the FRAM features. These methods are located in the ProcFRAM.c and ProcFRAM.h files

There is 8MB of nonvolatile flash memory (FLASH) on the U2 module. It is arranged in 8 - 4Kword (8Kbyte) boot sectors and 127 - 32 Kword (64Kbyte) sectors. The first 52 sectors (1440 Kwords / 2880Kbytes) are reserved for system parameter storage and the default U2 program. This leaves 83 sectors (2656 Kwords / 5312Kbytes) available for the user's program and data storage. Data can be written to an erased sector one word at a time. The flash must be erased in 32Kword (4Kword for boot) sectors. The flash program memory map describes flash address allocations. Methods are provided in the U2 proc library to access the FLASH features. These methods are located in the ProcFLASH.c and ProcFLASH.h files.

There is 128Kwords of RAM that is allocated as a Shared RAM area. This SRAM area resides on the U2 processor card and can be accessed by the U2 processor, as well as, the VME64D2 interface processor and other modules on the VME64D2 card. This area can be used to pass data between modules. [**Note:** the first 8Kwords (0x0000 – 0x1FFF) are reserved for the processor library methods. The user area begins at 0x2000 and extends to 0x1FFFF.] Methods are provided in the U2 proc library to access the SRAM features. These methods are located in the ProcSRAM.c and ProcSRAM.h files.

There is 8MB of volatile synchronous dynamic random access memory (SDRAM) available for program and data storage. This area is not directly accessible by the user.

There are three RS232 channels available. One of these channels is wired to a header on the front of the U2 card and can be used as a debug message port. The other two ports are currently not available for use. Methods are provided in the U2 proc library to access the RS232 features. These methods are located in the ProcUART.c and ProcUART.h files.

Note: Only one channel is available in the SIU chassis.

There are three I2C channels available. One of these channels is wired to the RTC, the other two channels are available to the user. Methods are provided in the U2 proc library to access the I2C features. These methods are located in the ProcI2C.c and ProcI2C.h files. (**Note:** The I2C channels are not available on the 64D2 card).

There is one USB port. This USB interface is only available to download the U2 program to flash.

Architectural Overview

The following drawing illustrates an example of the interconnection of the various modules, bus and processors on our VME64DP3 card.

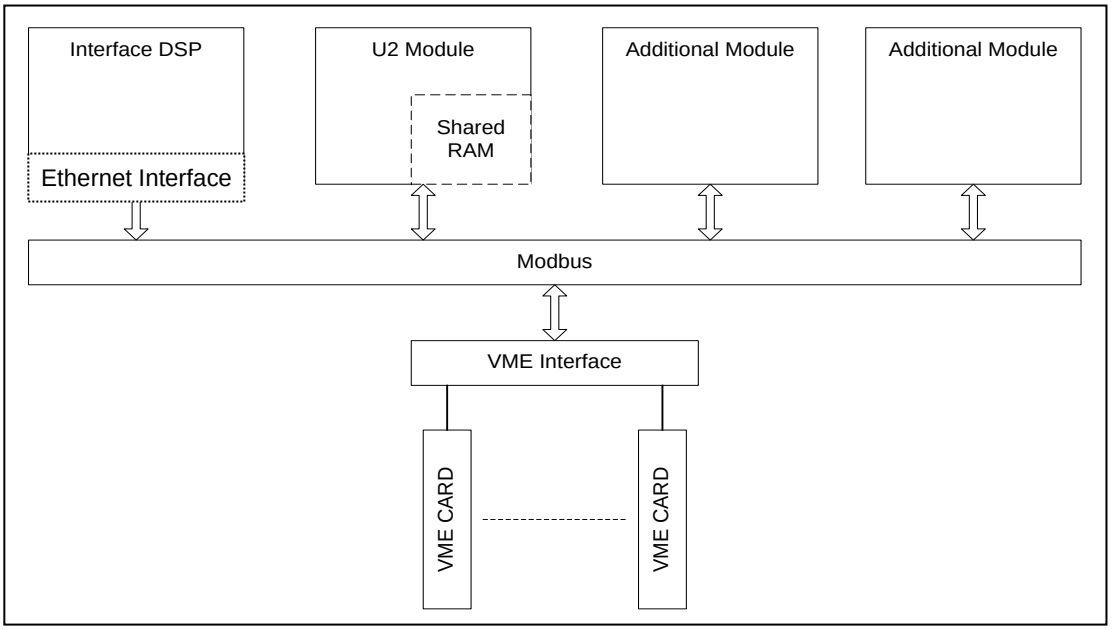


Figure 1 - Interconnect diagram

From this drawing we can see that the ModBus is the common channel for communication between the interface DSP, modules, and VME bus. For each of the devices capable of bus mastership, (interface and U2 DSP) a means is provided for access to ModBus. From there, access is available to the VME, U2 Shared RAM, and other modules.

Programming Reference

Programming Support

The *Programmer's Reference Guide* for NAI U2 is an overview of the U2 processor module and software support library. This is intended to help the programmer obtain an understanding of how to write software for the U2 processor module and how this module interacts with the various platform boards.

The *Programmer's Reference Guide* for the NAI U2 processor can be downloaded at: www.naii.com

Each platform board that supports the U2, the (e.g. 64EP3, 75DP3, and 64DP3) has a software support kit. The software support kit for NAI U2 processor can be downloaded at: www.naii.com

Development System Connection

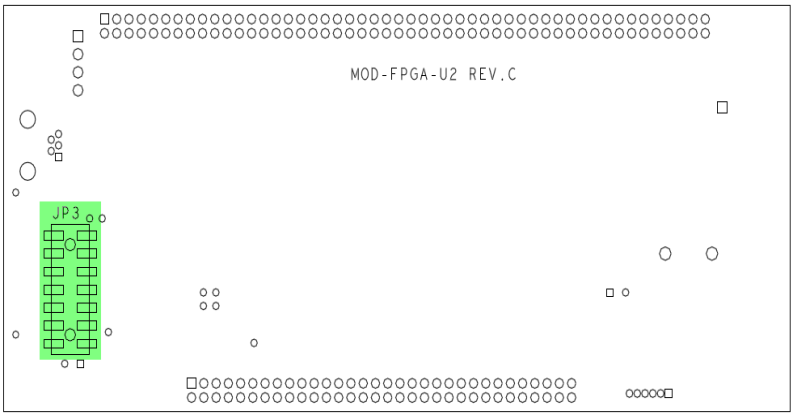
Please refer to the manual for the emulator you plan on using. Follow the installation instructions in the presented order to ensure correct operation of your software and hardware.

1. Install VisualDSP++ 5.0 Update 7 (or higher). VisualDSPICE-100B emulator
2. Set the JTAG clock frequency. High-performance PCI-ICE and high-performance USB-ICE emulators support a JTAG clock operation up to 50MHz. USB-ICE emulators support a JTAG clock operation of 10MHz.
3. Select the operating voltage of the target DSP JTAG interface. Some emulators will automatically set the JTAG operating voltage. On some emulators, like the ICE-100B the operating voltage is set with jumpers. The U2 JTAG operating voltage is 3.3V.

JTAG System Connections

Analog Devices, Inc. carries a wide range of in-circuit emulation products. Analog Devices' JTAG emulators offer fast communication between the host PC and target hardware.

The U2 module supports JTAG with a JTAG ICE 14-pin header. JTAG debug connector JP3 is available on the bottom of the U3 module. For applications development a surface mount 14-pin header (part #1234) can be soldered to JP3 PCB pads. The picture below indicates position for JP3.



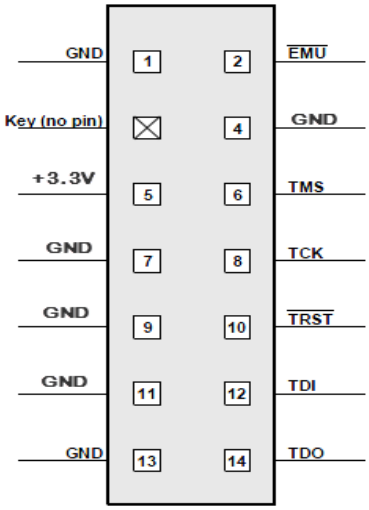
Note: The U2 module is installed on the platform card bottom up. With the cover removed from the platform card connecter JP3 would be facing the user.

Depending on the card or embedded system type and/or configuration, the emulator (JTAG) port will be available from the front of the card and may require an adapter cable assembly (will be provided if necessary) to interface from the motherboard to the Analog Devices emulator pod.

JTAG Pin-Outs

The 14-pin connector is keyed at pin 3 on the emulator connector to ensure that the signals mate correctly with the 14-pin target emulation header. The target board should also have pin 3 of the JTAG interface connector cut.

Connecter JP3 is connected as indicated below.



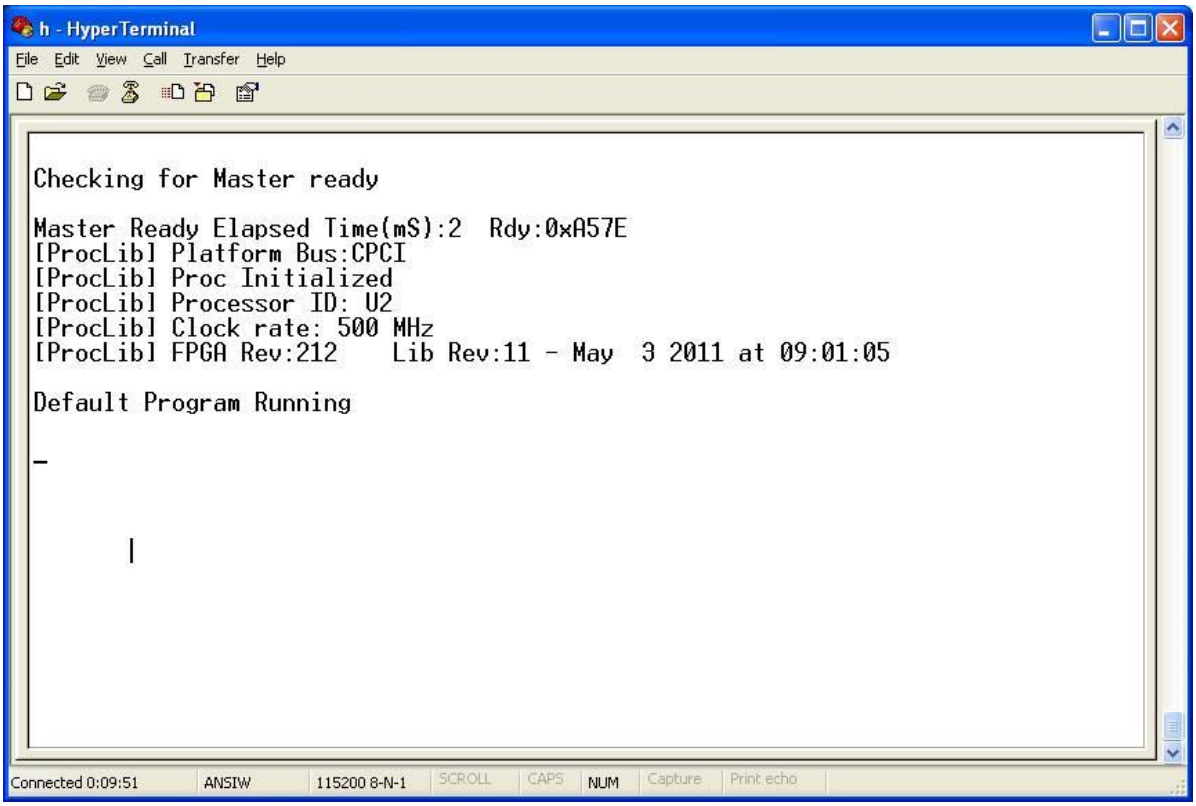
Console

The BF533 serial UART transmit and received data connections are available on edge connector JP7 on the U2 module. Part # (xxxx) may be used as the mating connector. The console connections may be available on the platform board. The pin-outs are platform dependent; please refer to the pin-out section of this document.

JP7

Pin	Signal
1	SERIAL_TX (Out)
2	SERIAL_TX (In)
3	N/C
4	Signal Return (GND)

The console (or sometimes referred to as the ‘debug’ port) will be available on all processor enabled platforms. Loaded on the U2, when delivered, will be a simple ‘program’ loop which runs on the processor. Connecting to the console (debug) serial port via hyperterminal or other communications type program, at default 115,200/8-bit/no parity/1-stop, will yield the following (or similar) output:



Initial Startup

The object of the section of the document is to provide the user with the initial system connection and startup procedures.

NAI Ethernet Download

The NAI U2 Processor Module Download Application is a Microsoft Windows based application that allows the user to download custom software to the U2 processor flash. The application connects to a specified IP Address, then downloads and verifies the loader file transfer.

Requirements

The following is necessary to use the NAI U2 Ethernet Download Application to download the binary “LDR” file to the flash for the U2 module processor:

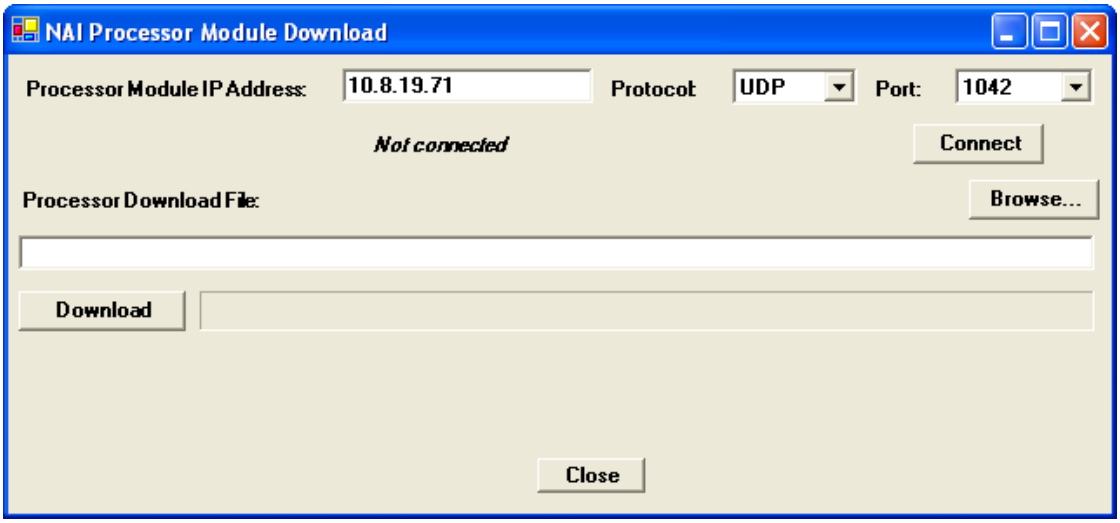
Windows XP

Microsoft .NET Framework 1.1 or greater – the latest version can be downloaded from:

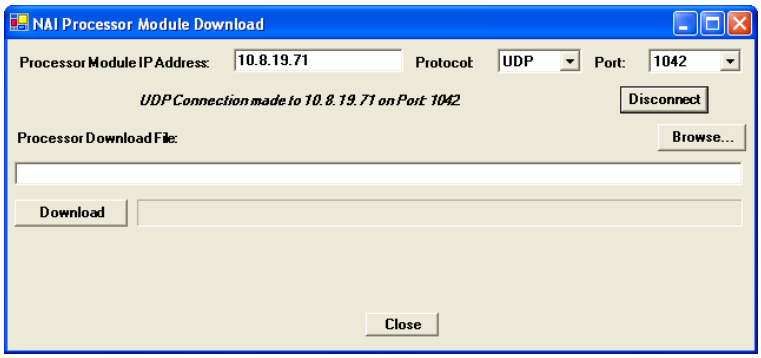
http://msdn.microsoft.com/netframework/downloads/updates/default.aspx

U2 Ethernet Download Application

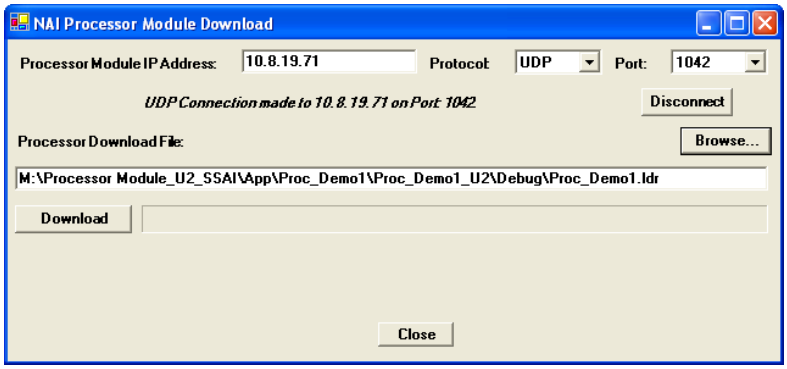
To start the NAI U2 Processor Module Download Application, run the “NAI Processor Download.exe” file under the folder labeled “..\Utilities\U2_Ethernet_Download_App”. You should see the screen shown below.



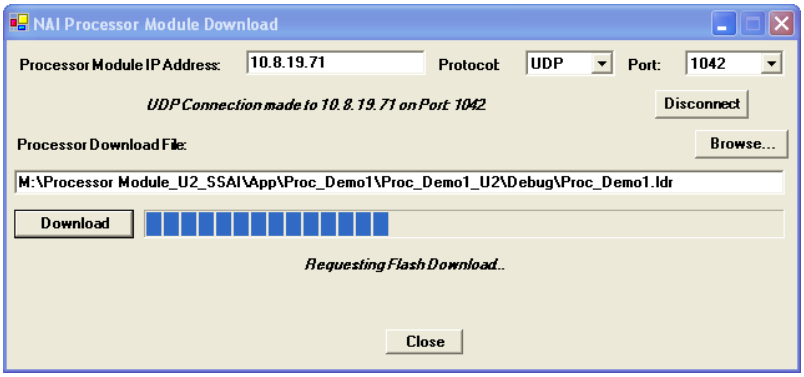
Press the ‘Connect’ button and verify that the program has connected to the card.



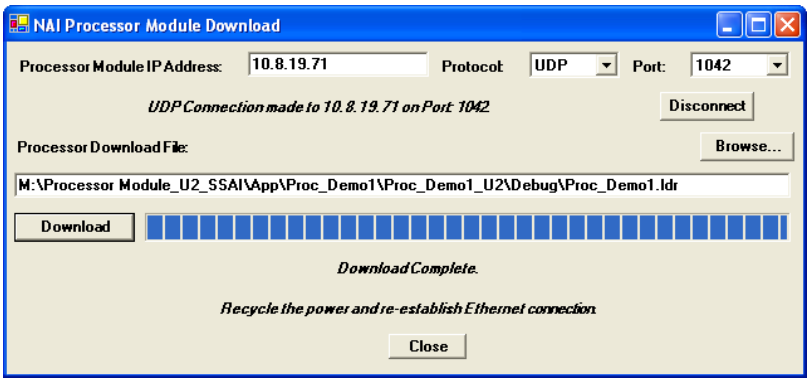
Use the ‘Browse’ button to navigate to the loader (*.ldr) file to be downloaded.



Press the ‘Download’ button to download the file to the U2 processor flash memory.



Upon a successful download, restart the processor to run the downloaded program.



Hardware Reference

External Bus (EBIU)

The external bus interface unit (EBIU) connects local memory resources to the ADSP-BF533 processor. The EBIU includes a 16-bit wide data bus, an address bus, and a control bus. Both 16-bit and 8-bit accesses are supported.

Local Memory

FLASH

The U2 supports 8 MB of nonvolatile MirrorBit (NOR) flash memory. The flash consists of a single device S29GL064M90BAIR40. This flash is selected by the asynchronous memory select signal ~AMS0.

The first 52 sectors of flash (1440 Kwords / 2880Kbytes) are reserved for system parameter storage and the default U2 program. This leaves 83 sectors (2656 Kwords / 5312Kbytes) available for the user’s program and data storage. Data can be written to an erased sector one word at a time. The flash must be erased in 32Kword (4Kword for boot) sectors.

Flash Program Memory Map

There is 8Mb of nonvolatile flash memory (FLASH) on the U2 module. It is arranged in 8 - 4Kword (8Kbyte) boot sectors and 127 - 32Kword (64Kbyte) sectors.

Address Range	Sector Range	Function
0x00000000 – 0x00002FFF	0 -2	Reserved
0x00003000 – 0x00003FFF	3	Blackfin 533 Configuration Data
0x00004000 – 0x00007FFF	4 - 7	Reserved
0x00008000 – 0x0010FFFF	8 - 40	Reserved
0x00110000 – 0x0015FFFF	41 - 50	Factory Default Program
0x00160000 – 0x0016FFFF	51 - 52	U2 Parameter Data
0x00170000 – 0x003FFFFF	53 - 127	User Program and Data

SDRAM

16 MB (8M x 16 bits) of SDRAM. The SDRAM is supplied by a MT48LC8M16LF Mobile SDRAM device. This device is selected by the synchronous memory select 0 (~SMS0) pin.

FRAM

The FM25CL64 is a 64-kilobit **Ferroelectric Nonvolatile RAM**. The FM25CL64 is organized as 8,192 x 8 bits, and has unlimited read and write cycles. The FRAM device is attached to the BF533 synchronous serial port serial port 0 (SPORT0). BF533 pins RSCLK0, RFS0, DR0PRI, and DT0PRI are used to support the connection between the FRAM and Blackfin. Methods are provided in the U3 BSP and proc library to access the FRAM features.

ADSP-BF533 Pin Assignment	FM25CL64
RSCLK0 (Out)	SCK (In)
RFS0 (Out)	CS#
DR0PRI	SO (Data Out)
DT0PRI	SI (Data In)

Shared Resources

Shared SRAM

128Kwords of SRAM is attached through the local bus via the FPGA. This static ram is allocated as Shared-RAM. This SRAM area resides on the U2 processor card and can be accessed by the U2 processor, as well as, the VME/PCI bus, interface processor and other modules residing on the ModBus.

To access the SRAM space from the U2 processor, a combination of the SRAM page offset and the SRAM access window are used. Each 'window' is 4K words and there are 64 pages.

For example, if the address of interest is 0x2020432, the SRAM page offset will be loaded with 0004, SRAM access window will be 0321 (page = address & 0x000F F000, window = address & 0x0000 0FFF). This register access is handled automatically when the U2 proc library functions SRAMReadAbsolute or SRAMWriteAbsolute are used.

SRAM Address Allocations

Address Range				Function
U2	Module 1	Module 2	Module 3	
0x20203000 – 0x20203FFE	0xFF400000 – 0xFF43FFFE	0xFF600000 – 0xFF63FFFE	0xFF800000 – 0xFF83FFFE	Shared RAM (256K Words)

Modbus Module Addressing

The ModBus is a 16MB area of internal address space used for communication between the Interface DSP and card modules on the platform cards. Both the Interface DSP and U3 module can access this space.

Other modules (i.e. 1553) are also mapped to this space. This space is accessed through the use of windows.

To access the ModBus space a combination of the ModBus address offset and the ModBus access window are used.

For example, with the U2 processor located in slot 3 and the card to access in slot 1, the following would occur:

If the address of interest is 0xFF401234, the ModBus address offset high will be loaded with 0x000F, ModBus address offset low will be loaded 0xF401 and ModBus access Window will be 0x0234.

(High = address & 0xF000 0000, Low = address & 0x0FFF F000, access = address & 0x00000FFF).

This register access is handled automatically when the U2 proc library functions ModWriteAbsolute or ModReadAbsolute are used.

ON-Module I/O

LED

The U2 module has one status LED. This led is placed on the top side of the PCB, and is not visible when the U2 module is installed on a platform board. The bit that controls the LED is mapped into address space at address 0x20202016, bit[0]. Please refer to FPGA Memory Map Address Allocation in the appendix for details.

Asynchronous Serial

The U2 has one asynchronous serial port. Connections to the BF533 UART are available on the platform board. SERIAL_TX and SERIAL_RX (RS232) signals are connected to J2 on the module to a Samtec QTS-025-02 high speed terminal strip. The UART connections on the platform board are platform dependent. Please refer to the pin-out section of this document. The BF533 UART, SERIAL_TX and SERIAL_RX connections are also brought out to an edge connector JP7 on the U2 Module.

Methods are located in the ProcUART.c and ProcUART.h files.

Differential I/O

The U2 processor module provides 20 differential inputs/outputs attached through the Local bus via the FPGA. These lines can be set up by the user as needed. Methods are provided in the U2 proc library to access the differential I/O features.

Differential I/O Register Descriptions

Addresses for these registers can be found in the FPGA Memory Map Address Allocation table.

Diff_ I/O Data [20:1]

Bit	Description	Access	Reset Value
[20:1]	Reading this register returns the state of the I/O pin. Writing the differential I/O data register stores the value that will be applied when the data direction is set to (1), transmit mode.	R	N/A

Diff_Direction [20:1]

Bit	Description	Access	Reset Value
[20:1]	0 = Differential transceiver is set to receive. The data in the differential I/O data register reflects the state of the input signal at the I/O pin.	R/W	0
	1 = Differential transceiver is set to transmit mode. The data stored in the differential I/O is expressed on the associated differential I/O pin		

Diff_ I/O Terminators [20:1]

Bit	Description	Access	Reset Value
[20:1]	0 = Differential termination is open, input impedance ~ 125K Ω	R/W	0
	1 = Differential transceiver termination is closed. Input impedance is set 120Ω		

Note: Although it is possible to set the Driver Enable (transmit mode) and Termination Enable bit on, their operation should be considered mutually exclusive. The 120 ohm termination should be enabled when the channel is in receive mode and disabled for transmit.

Differential I/O Slow Bits [20, 10]

Bit	Description	Access	Reset Value
[10]	0 = Slew rate control is enabled for differential I/O signals [10:1]	R/W	0
	1 = Normal mode for differential I/O signals [10:1]		
[20]	0 = Slew rate control is enabled for differential I/O signals [20:11]		
	1 = Normal mode for differential I/O signals [10:1]		

The U2 module utilizes LTC2859 as the differential I/O transceivers. The LTC2859 feature is a logic-selectable reduced slew mode that softens the driver output edges to control the high frequency EMI emissions from equipment and data cables. The reduced slew rate mode limits the data rate limited to about 250kbps. Slew limiting also mitigates the adverse effects of imperfect transmission line termination caused by stubs or mismatched cables.

Differential I/O Specifications

Note: The differential I/O signals are non-isolated. All grounds are common and connected to system ground.

Input

Input Levels:	-10V to +10V
Input Sensitivity:	± 200mV
Input Resistance (Termination Enabled):	120Ω
Input Resistance (No Termination):	125KΩ typical

Output

Output Voltage:	-0.25V to +5V max
Output Signal Level (Loaded Minimum):	2V ±1.5V (loaded minimum)
Output Signal Level 5V (Unloaded Maximum):	±5V (unloaded maximum)
Driver Load Impedance:	27Ω (|Vod| 2.0V minimum)
Protection:	Short circuit protected, thermal shutdown, built-in current limiting

TTL

The U2 processor module provides 24 TTL inputs/outputs and is attached via the Local bus the FPGA. These I/O signals can be set up by the user as needed. The U2 utilizes 24 74LVCH1T45 single-bit, single ended transceivers with 3-state outputs to support the 24 TTL I/O.

Three groups of I/O pins TTL_DAT_CH [8:1], TTL_DAT_CH [16:9], and TTL_DAT_CH [24:17] can be programmed to use the onboard 3.3V power supply or an external power supply. If an external power supply is selected Vout H (max) for the group is determined by the voltage of the external supply.

If utilized, the external power supply voltage must be maintained between 1.65V and 5.5V (max).

Each I/O pin incorporates a 22 ohm series resistor.

TTL Register Description

TTL Output Data [24:1]

Bit	Description	Access	Reset Value
[24:1]	The Differential I/O data register stores the value that will be applied when the data direction is set to (1), transmit mode.	R/W	0

TTL I/O Direction [24:1]

Bit	Description	Access	Reset Value
[24:1]	0 = TTL transceiver is set to receive. The data in the differential I/O data register reflects the state of the input signal at the I/O pin.	R/W	0
	1 = TTL transceiver is set to transmit mode. The data stored in the differential I/O is expressed on the associated differential I/O pin		

TTL I/O Power Ctrl [2:0]

Bit	Description	Access	Reset value
[2]	0 = TTL_DAT_CH [24:17] use the internal 3.3V supply	R/W	0
	1 = TTL_DAT_CH [24:17] use the external supply		
[1]	0 = TTL_DAT_CH [16:9], use the internal 3.3V supply	R/W	0
	1 = TTL_DAT_CH [16:9], use the external supply		
[0]	0 = TTL_DAT_CH [8:1], use the internal 3.3V supply	R/W	0
	1 = TTL_DAT_CH [8:1] use the external supply		

TTL I/O Rising Edge Detect [24:1]

Bit	Description	Access	Reset Value
[24:1]	0 = Indicates that no rising edge on I/O pin has occurred since this register was last read.	R	0
	1 = Indicates that a rising edge has occurred on this I/O pin since the register was last read		

TTL I/O Falling Edge Detect [24:1]

Bit	Description	Access	Reset Value
[24:1]	0 = Indicates that no falling edge on the I/O pin has occurred since this register was last read.	R	0
	1 = Indicates that a rising falling has occurred on this I/O pin since the register was last read		

Note: Updating the direction or data output registers may affect both the rising edge and falling edge detect registers. A read should both edge detect register after making any TTL setting changes.

TTL Input Data [24:1]

Bit	Description	Access	Reset Value
[24:1]	Reading this register returns the state of the I/O pin.	R	N/A

TTL I/O Specifications

Note: The differential I/O signals are non-isolated. All grounds are common and connected to system ground.

TLL Input

Input Levels: TTL and CMOS compatible, single ended inputs
VinL (Max): 0.8 V
V in H (Min): 2.0 V
Vin (Max): TTL_VCC +.5 V (TTL_VCC can be supplied by an external power supply)

TTL Output

Output Levels: TTL/CMOS, single ended outputs

Drive Capability

Vout L (Max): 0.55 V max @24 mA (sink)

V out H (Min): 2.4 V @ 24 mA (source)

Vout H (Max): VCC, (unloaded)

Rise/Fall Time: 10 ns into a 50pf load

I2C

I2C is a 2-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices.

The FPGA contains three identical I2C Master only channels. One of these channels is wired to the RTC. The other two channels are wired to connecter JP2 and may be available to the user, dependent on the platform board and configuration. Methods are provided in the U2 proc library to access the I2C features.

Real Time Clock

Attached through the I2C controller 0 in the FPGA, is the Intersil ISL1208IU8, the real time clock (RTC). The RTC can be used to provide a system time and date function, or can be used as an event timer.

Features

- Real time clock/calendar
- Tracks time in hours, minutes, and seconds
- Day of the week, day, month, and year
- Single alarm
- Set to the second, minute, hour, day of the week, day, or month
- Single event or pulse interrupt mode

Programmable Flags (PFs)

The BF533 processor has 16-bit directional programmable flag for general-purpose I/O pins, PF[15:0]. The U2 module has the PFs assigned as indicated in the table below. The designation N/U indicates “not used”.

Processor Pin	U2 Module Function
PF0 –PF1	N/U
PF2- PF3	FPGA Configuration
PF4	USB Interrupt
PF5	FPGA Interrupt
PF6	N/U
PF7	Flash Program Enable
PF8- PF9	N/U
PF10	DAP_A20 (Address)
PF11	DAP_A21 (Address)
PF12	DAP_A22 (Address)
PF13	DSP_A[0]
PF14	DSP_A[1]
PF15	

Interrupts

Interrupts may be generated by the VME/PCI bus or the modules installed on the platform board. These interrupts may be detected and serviced by either the platform board or U2. It is important that the system design permits only one of these devices to service the interrupts.

VME/PCI Interrupts

VME/PCI Interrupts are controlled via a register mapped into Modbus space, permitting either the platform board or U2 to manage them. When an interrupt request occurs on the VME/PCI bus, the interrupt is serviced immediately and the vector and interrupt level are captured and held until the interrupt is processed. Note that until processed, no more VME/PCI interrupts can be serviced; that is, there is no hardware FIFO for VME/PCI interrupts. A single control register in Modbus space is provided for handing VME/PCI interrupts organized as follows:

Register	Modbus address (byte)	Function
VME/PCI Interrupt Control	0x201FF2	B15: Interrupt Pending (Write 1 to Clear) B14: Interrupt Enable (1= Enabled) B(13..11): (Unused) B(10..8): Interrupt Level B(7..0): Interrupt Vector

Module Interrupts

Interrupts from modules other than the U2 are controlled via a register mapped into Modbus space, permitting either the platform or U2 to manage them. When a module generates an interrupt, the interrupt is serviced immediately and the module and interrupt numbers are captured and held until they are processed. Note that until they are processed, no more non-U2 module interrupts can be serviced; that is, there is no hardware FIFO for module interrupts.

Interrupts from the U2 module are handled differently. A pair of flags is provided to moderate inter-processor communications, one for each direction. A downstream flag is provided that may be set by the U2. The Platform CPU may be interrupted when this flag is set, after which the flag may be cleared. An upstream flag is provided that may be set by the platform. The platform may be interrupted when the flag is cleared by the U2, indicating it is again available for use.

This scheme is intended for passing information between the platform CPU and U2 via the shared memory (at Modbus space 0x800000—0x87FFFF). The platform can transfer a structure containing a block of information to the shared memory and then set the upstream flag to indicate to the U2 that it is available. In the same manner, the U2 can transfer data to the shared memory and set the downstream flag to inform the platform that the data is available.

A single control register in Modbus space is provided for handing module interrupts, organized as follows:

Register	Modbus Address (Byte)	Function
Module Interrupt Control	0x201FFE	B15: Non-U2 Interrupt Pending (Write 1 to Clear) B14: Upstream Flag (to U2) is Ready (=0) B13: Downstream Flag (from U2) is Pending (=1) B(12..8): (Unused) B(7..5): Non-U2 Interrupt Module Number B(4..0): Non-U2 Interrupt Number

The actual flags for inter-processor communication are located on the U2, and may be accessed as follows:

Register	Modbus Address (Byte)	Function
Inter-Processor Control Register	0x880000	B(15..6): (Unused) B5: 1= Permit Interrupt on Downstream (from U2) Flag B4: 1= Permit Interrupt on Upstream (to U2) Flag Cleared B3: 1= Set Upstream (to U2) Flag B2: 1= Clear Downstream (from U2) Flag B1: Downstream(from U2) Flag State B0: Upstream (to U2) Flag State

Clocks

An external 25MHZ clock is connected to the processor's CLKIN pin. The core clock (CCLK) and system peripheral clocks (SCLK) are derived from the input clock (CLKIN) signal. An on-chip PLL is capable of multiplying the CLKIN signal by a user programmable 0.5x to 64x multiplication factor. The user however should consider the SCLK, and CLKIN setting as fixed.

Default program values:

CCLK

SCLK

Reset

BMODE

The BF-533 samples the BMODE pins during power-on resets and software-initiated resets. The U2 has the BMODE [1:0] hardwired to {0,1}. The BF-533 will boot from 16-bit external flash memory.

The flash boot routine located in boot ROM memory space is set up using asynchronous memory bank 0. All configuration settings are set for the slowest device possible (3-cycle hold time; 15-cycle R/W access times; 4-cycle setup).

Address Map

U2 Memory Map Address Allocation

Address Range	Description	U2 Functionality
Internal Blackfin 533 Memory		
0xFFE00000 - 0xFFFFFFFF	Core MMR Registers (2MB)	
0xFFC00000 - 0xFFDFFFFF	System MMR Registers (2MB)	
0xFFB01000 - 0xFFBFFFFF	Reserved	
0xFFB00000 - 0xFFB00FFF	Scratch SRAM (4K)	
0xFFA10000 - 0xFFA13FFF	Code SRAM / Cache (16K)	
0xFFA00000 - 0xFFA0FFFF	Code SRAM (64K)	
0xFF908000 - 0xFF9FFFFF	Reserved	
0xFF904000 - 0xFF907FFF	Data Bank B SRAM / Cache (16K)	
0xFF900000 - 0xFF903FFF	Data Bank B SRAM (16K)	
0xFF808000 - 0xFF8FFFFF	Data Bank A SRAM / Cache (16K)	
0xFF804000 - 0xFF807FFF	Data Bank A SRAM (16K)	
0xEF000000 - 0xFF7FFFFF	Reserved	
0x20400000 - 0xEEFFFFFF	Reserved	
I / O Peripherals and Memory		
0x20300000 - 0x203FFFFF	ASYNC MEMORY BANK 3 (1MB)	USB Interface
0x20200000 - 0x202FFFFF	ASYNC MEMORY BANK 2 (1MB)	Altera FPGA (SeeTable 2)
0x20000000 - 0x200FFFFF	ASYNC MEMORY BANK 1 (1MB)	Boot loader Shunt
0x20000000 - 0x200FFFFF	ASYNC MEMORY BANK 0 (1MB)	Flash 8MB (Page Accessed)
SDRAM		
0x00000000 - 0x04000000	EZ-Kit SDRAM MEMORY (32MB)	
0x00000000 - 0x07FFFFFF	SDRAM MEMORY (16MB - 128MB)	SDRAM (8MB)

Table 1 - U2 Memory Map

FPGA Memory Map Address Allocation

Address Range	Function
0x20200000 – 0x20201FFE	Mod Bus Access Window
FPGA Control	
0x20202000	FPGA Revision
0x20202008	0xabcd When Ready
0x20202010	ModBus Address Offset High
0x20202012	ModBus Address Offset Low
0x20202014	ModBus Arbitration Number (2,3,4)
0x20202016	b0 = LED
0x20202018	Shared RAM Page Offset (Addr Bits A17...A12)
0x2020201A	Interrupts Pending
0x2020201C	Interrupts Enabled
0x2020201E	RAM Flag Triggers
0x20202080	Reset System
Differential IO	
0x20202200	Differential I/O Data Bits 16..1
0x20202202	Differential I/O Data Bits 20..17
0x20202204	Direction Bits 16..1 (1 = Out)
0x20202206	Direction Bits 20..17 (0 = In)
0x20202208	Differential I/O Terminators 16..1 (1 = Term)
0x2020220A	Differential I/O Terminators 20..17 (0 = Open)
0x2020220C	Differential I/O Slow Bits 20,10 (1 = Norm, 0 = Slow)
TTL IO	
0x20202300	TTL Output Data Bits 16..1
0x20202302	TTL Output Data Bits 24..17
0x20202304	TTL I/O Direction Bits 16..1 (0 = In)
0x20202306	TTL I/O Direction Bits 24..17 (1 = Out)
0x20202308	TTL I/O Power Ctrl Bits 2..0 (0 = Int, 1 = ext)
0x2020230A	TTL I/O Rising Edge Detect Bits 16..1
0x2020230C	TTL I/O Rising Edge Detect Bits 24..17
0x2020230E	TTL I/O Falling Edge Detect Bits 16..1
0x20202310	TTL I/O Falling Edge Detect Bits 24..17
0x20202312	TTL Input Data Bits 16..1
0x20202314	TTL Input Data Bits 24..17
I^2C IO	
0x20202400	Chan 0 Ctrl, RDd0
0x20202402	Chan 0 Addr,RD1
0x20202404	Chan 0 Data,RD2
0x20202406	Chan 0 Count,RD3
0x20202420	Chan 1 Ctrl
0x20202422	Chan 1 Addr
0x20202424	Chan 1 Data
0x20202426	Chan 1 Count
0x20202440	Chan 2 Ctrl (Used for Real Time Clock)
0x20202442	Chan 2 Addr (Used for Real Time Clock)
0x20202444	Chan 2 Data (Used for Real Time Clock)
0x20202446	Chan 2 Count (Used for Real Time Clock)
0x20202460	RX Done Bits (xxxx xxxx xxxx x210)
RAM	
0x20202500	RAM Address Bits B15..14 = (Unused) B13: 0 = Shared SRAM 1 = SDRAM (Unimplemented) 12..0 = RAM Addr Bits 23..11
0x20202F00 – 0x20202FFF	Discretes (Not Used)
0x20202FFE	Write 1 to Reset
0x20203000 – 0x20203FFF	Shared RAM 4K Access Window

Table 2 - FPGA Memory Map

Software Libraries

U2 Processor Module Library

The U2 Processor library package provides function interfaces to the 'on module functionality' as well as the ModBus and VME/PCI interfaces. This package contains *Help* documentation (in html format) that explains all the functions available in the library. The package also contains the source code (*.h, *.c) files as well as the files needed to build the library using the Analog Device VisualDSP++ IDE. Example programs are also provided to demonstrate the usage of the libraries in typical applications of the module.

Example of platform specific libraries that can be utilized in conjunction w/ U2 module specific library:

64C3 Library

The VME64C3 library package provides function interfaces to all the modules available for this multi-function I/O card. This package contains Help documentation (in html format) that explains all the functions available in the library. The package also contains the source code (*.h, *.c) files as well as the files needed to build the library using the Analog Device VisualDSP++ IDE. Example programs are also provided to demonstrate the usage of the libraries in typical applications of this card.

Associated Documents

NAI documents

Programmer's Reference Guide for NAI U2 Processor Module

U2 Ethernet Download

U2 USB Download

ADI documents

Related Processor Publications

Title	Description
ADSP-BF536/ADSP-BF537 Embedded Processor Data Sheet	General functional description, pin-out, and timing
ADSP-BF537 Blackfin Processor Hardware Reference	Description of internal processor architecture and all register functions
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions
Engineer-to-Engineer Note EE-240	Describes the booting process for the ADSP- ADSP-BF533

Related VisualDSP++ Publications

Title	Description
VisualDSP++ User's Guide	Description of the VisualDSP++ features and usage
VisualDSP++ Assembler and Preprocessor Manuals	Description of the assembler function and commands
VisualDSP++ Linker and Utilities Manual	Description of the linker function and commands
VisualDSP ++ Loader and Utilities Manual	Description of the loader/splitter function and commands
VisualDSP++ C/C++ Complier and Library Manual for Blackfin Processors	Description of the complier function and commands for Blackfin processors

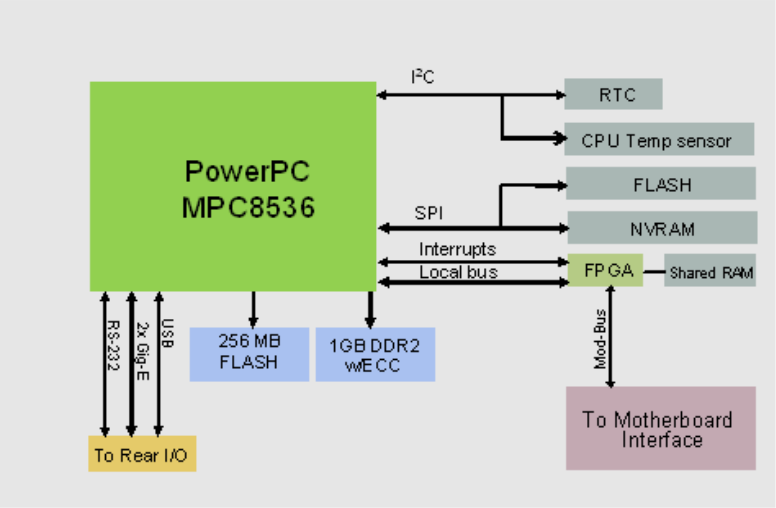
PROCESSOR (MODULE U3)

Principle of Operation

The U3 is a platform module for the development of custom application solutions. This module adds single board computer resources and computational power of the Freescale™ MPC8536 to NAI processor module supported platforms (NAI 75DP3, 64EP3, 64DP3) with additional configurable multi-function I/O module capabilities. The MPC8536, high-performance member of the PowerQUICC III™ processor family combines a computation-intensive super-scalar Power Architecture™ processor core with high performance system peripherals and advanced power management techniques. The U3 module internally integrates SATA, USB, multi-lane PCI Express, Gigabit Ethernet, and DDR memory to increase data bandwidths, and lower overall power consumption in certain platform configurations.

U3 MPC8536 Features

- High-performance PowerPC e500v2 core with
- 36-bit physical addressing
- 512-Kbyte L2 cache with ECC
- Integrated security engine (SEC) with XOR acceleration
- Advanced power management controller
- Two USB host controllers (one port available)
- Two integrated 10/100/1000 Mb enhanced three-speed Ethernet controllers (eTSECs) with TCP/IP acceleration and classification capabilities
- PCI Express
- Two serial ATA interfaces (not user accessible)
- DDR2 SDRAM memory controller
- Programmable interrupt controller (PIC)
- Enhanced serial peripheral interface (eSPI)
- Four-channel DMA controller
- I^2C controller (not user accessible)
- DUART
- Enhanced local bus controller (eLBC)



U3 Processor Module Block Diagram

U3 Module Resources

- Bus slave and bus mastering
- Modbus system, access to local and off card resources
- Multiport shared SRAM
- Up to three USB ports and two Ethernet ports, dependent on board platform

Processor Overview

In addition to being the primary processor for interfacing to other onboard multi-function modules, the U3 processor module is based on the Freescale MPC8536 PowerQUICC™III integrated processor and has many built in features that can easily be accessed. The following is a list of these features:

- Real time clock
- FRAM
- FLASH
- SRAM
- SDRAM
- RS232
- USB
- Ethernet
- SATA (not user accessible from card platform I/O pins)
- SD card (not user accessible from card platform I/O pins)
- PCIe (not user accessible from card platform I/O pins)

The Real time clock (RTC) can be used to provide a system time and date function or can be used as an event timer. Methods are provided in the U3 BSP to access the RTC features.

There are 8K (8192) bytes of nonvolatile ferroelectric random access memory (FRAM) available for data storage. This can be used to store any data that needs to be available after a system power down. The FRAM is connected to the processor through the serial peripheral interface (SPI). Methods are provided in the U3 BSP and proc library to access the FRAM features.

There is 16MB of nonvolatile flash memory (FLASH) on the U3 module. It is arranged in 64 sectors, each containing 1024 pages. Each page is 256 Bytes wide. The memory can be programmed 1 to 256 Bytes at a time, using the page program instruction. The flash can be erased one sector at a time or the entire flash. Methods are provided in the U3 BSP and proc library to access the FLASH features.

There is 128Kwords of RAM that is allocated as a Shared RAM area. This SRAM area resides on the U3 processor card and can be accessed by the U3 processor, as well as, the VME64D3/VME64E3 interface processor and other modules on the VME64D3/VME64E3 card. This area can be used to pass data between modules. (**Note:** the first 8Kwords (0x0000 – 0x1FFF) are reserved for the processor library methods. The user area begins at 0x2000 and extends to 0x1FFFF.) Methods are provided in the U3 proc library to access the SRAM features.

There is 1GB of volatile synchronous dynamic random access memory (SDRAM) available for program and data storage. This area is not directly accessible by the user.

There are 2 RS232 channels available. One of these channels is VxWorks default (debug output) serial port (default 115,200, 8-bit, 1-stop, no parity, no flow control).

Architectural Overview

The following drawing illustrates an example of the interconnection of the various modules, bus and processors on our VME64DP3 card.

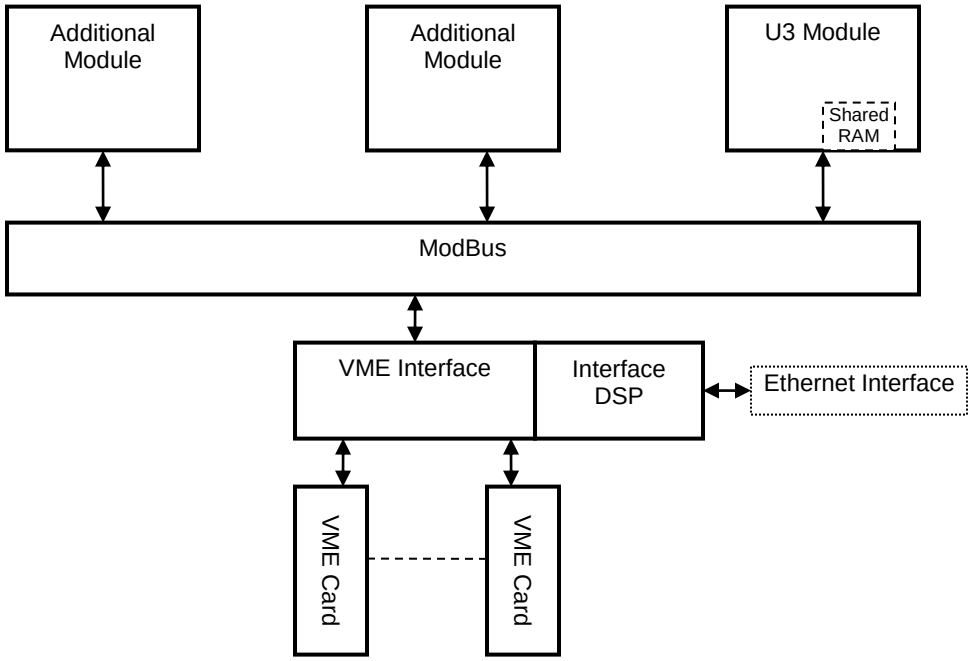


Figure 2 - Interconnect Diagram

From this drawing we can see that the ModBus is the common channel for communication between the Interface DSP, Modules, and VME bus. For each of the devices capable of bus mastership (Interface DSP and U3) a means is provided for access to ModBus. From there, access is available to the VME (where applicable), U3 Shared RAM, and other modules.

Programming Reference

Programming Support

The *Programmer's Reference Guide* for NAI U3 is an overview of the U3 processor module and software support library. This is intended to help the programmer obtain an understanding of how to write software for the U3 processor module and how this module interacts with the various platform boards. The U3 is provided with a Board Support Package (BSP). The BSP is a set of files used to support the U3 module hardware design. The set of files could be source code or binary files, or a mix of both. The BSP, in conjunction with the platform specific module function software support kit (SSK), provides a complete software integration set for controlling and accessing all the specific functions on the platform as well as in some applications, interfacing and providing data to/from other boards in a system chassis (master/slave capabilities).

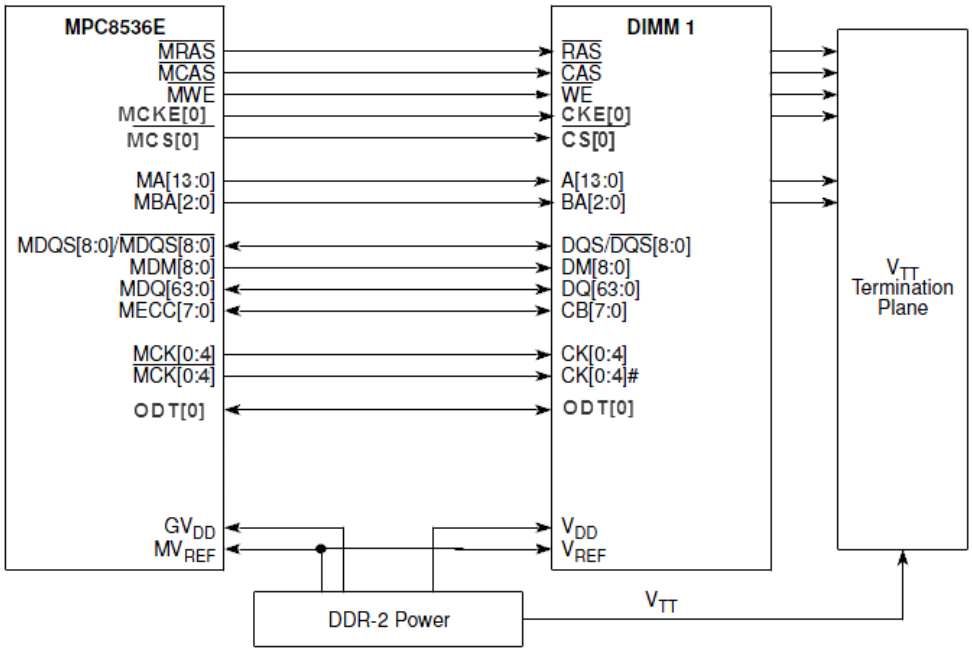
The *Programmer's Reference Guide* for NAI U3 Processor can be downloaded at: www.naii.com

Each platform board that supports the U3, the (e.g. 64EP3, 75DP3, and 64DP3) has a software support kit. The software support kit for NAI U3 processor can be downloaded from the specific platform product web page: www.naii.com

Local Memory

Ram DDR2

The U3 provides a total of 1G Byte of ECC DDR memory. The MPC8536 contains a 64-bit DDR2 memory controller. The controllers have full ECC error-correction support, with the ability to detect multi-bit errors and correct single-bit errors within a nibble. DDR2 memory port signals and connections are summarized below.



The U3 DDR2 memory is organized as four 32K x8 x8 devices, with a fifth device providing storage for ECC data. In total 5 MT47H128M16RT-25EIT. Please consult the Micron data sheet for DDR device specific details.

Flash

The U3 supports 256Mbytes of flash. Flash is configured as an 8-bit wide device, using the 8-bit asynchronous data access interface. Details on this mode of operation can be found in the Open NAND Flash Interface (ONFI 2_2) Specification. The flash supports page-mode accesses to allow maximum bus bandwidth and must be written as 32-bits. The flash is arranged in 256K byte sectors, has an erase capacity of 100,000 cycles per sector and typical data retention of 20 years.

The MPC8536 accesses this flash through NAND Flash Control Machine (FCM).

Flash Asynchronous Data Interface

Signal	Input / Output	Description
R/Bx#	O	Ready / Busy#
REx#	I	Read Enable / (Write / Read# Direction)
W/Rx#	I	Read Enable / (Write / Read# Direction)
CE#	I	Chip Enable
CLE	I	Command Latch Enable
ALE	I	Address Latch Enable
WEx#	I	Write Enable, Latching Data in the Asynchronous Data Interface.
WPx#	I	Write Protect
IO0 – IO7	I/O	Data Inputs/Outputs

Local Bus

The MPC8536 local bus provides access for SRAM, Modbus interface, and VME (where supported) through an interface FPGA. VME access is for platform boards that contain VME interfaces, not all platforms have a VME bus interface.

LB_SRAM

Attached to the Local Bus via the Modbus FPGA is 128Kwords of SRAM that is allocated as Shared RAM. This SRAM resides on the U3 Processor card and can be accessed by the MPC8536, as well as the VME64D3/VME64E3 interface processor and other modules on the VME64D3/VME64E3 card. This area can be used to pass data between modules. The first 8Kwords (0x0000 – 0x1FFF) are reserved for the processor library methods. The user area begins at 0x2000 and extends to 0x1FFFF.

Modbus Module Addressing

The ModBus is a 16MB area of internal address space used for communication between the interface DSP and card modules on the VME64D3/E3 card. Both the interface DSP and U3 module can access this space. Other modules (e.g. 1553) are also mapped to this space. This space is accessed through the use of windows. (See reference xxx.x). To access the ModBus space from the U3 Processor, a combination of the ModBus Address Offset and the ModBus access window are used.

VME (Where Supported)

The VME bus interface is implemented as a ModBus device. Though 2MB of the ModBus space is available, the width of the VME interface is limited to 8KB (the size of the ModBus interface windows in both the Interface and U3 Module DSP space (See reference xxx.x). The VME address map located in the Appendix describes the address allocations. To access the VME space from the U3 processor, a combination of the VME address offset and the VME access window are used.

I/O

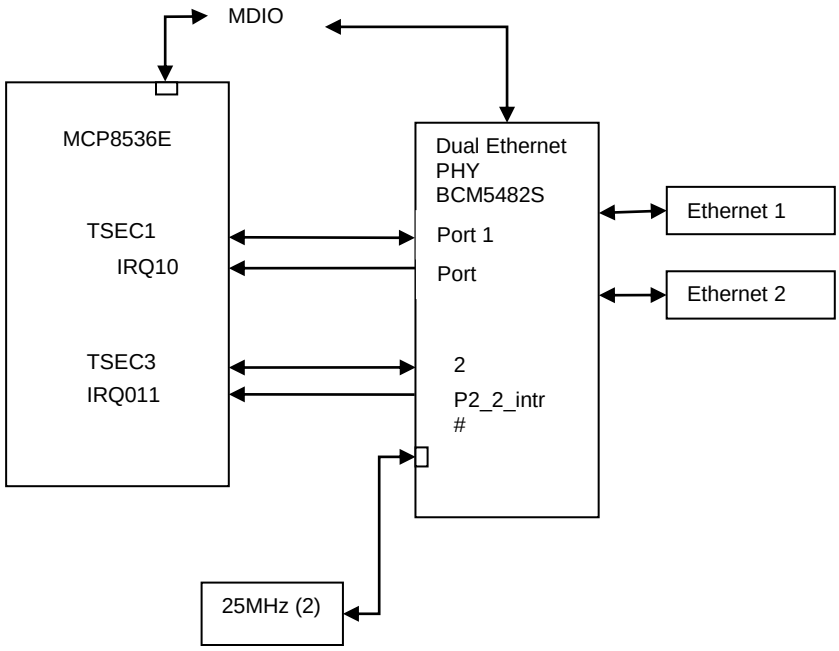
Ethernet

The MPC8536 supports two 10/100/1000Base-T Ethernet ports. These are 'direct' Ethernet ports to the module and maybe configured as pass-through via the specific platform motherboard. The U3 Ethernet ports support:

- Detection and correction of pair swaps (MDI crossover) and pair polarity
- MAC-side and line-side loopback
- Auto-negotiation

To support the MP8536E, the U3 module uses the Broadcom BCM5482S dual-PHY. The BVM5436E provides a direct connection to the MPC8536's two GMACs via a RGMII configuration. Both Ethernet ports support 4-pair, full-duplex 1G connection.

The figure below illustrates the connections between the MPC8536 and the BCM5482S PHY. Note the PHY requires two MPC8536 hardware interrupts (IRQ10 and IRQQ11).



The two 10/100/1G Ethernet ports are connected to a Samtec QTS-025-02 high speed terminal strip on the U3 module. The Ethernet connections for the 64EP3 can be found in the Pin-Out section of this document.

BCM5482S

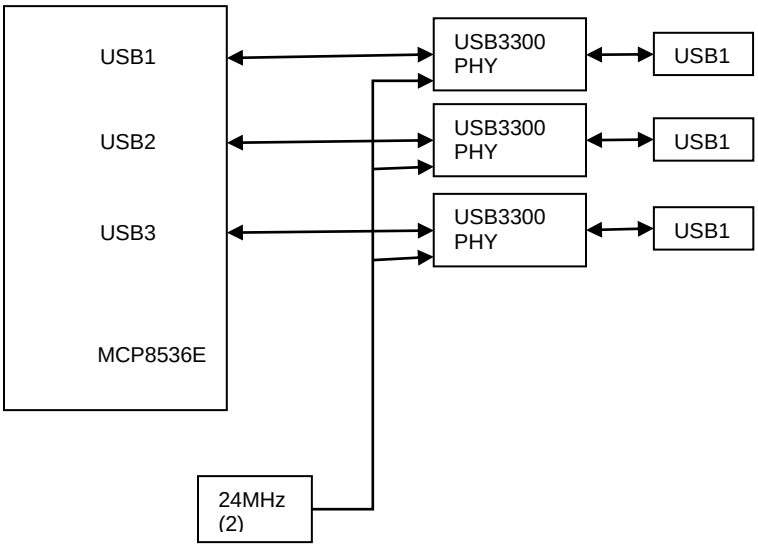
The BCM4882 PHY address used for MII management will default to MII PHY address 0x02h with power-on reset.

Ethernet LED

The U3 module has four open drain signals used to drive external status LEDs. The default functions for the LED's is Ethernet link speed and link activity indicators. The bits that control these LEDs are mapped into address space at address 0xE000'000A, bits gpout[11:8]. Please refer to VME Address Map in the Appendix for details.

USB

The MPC8536 supports three dual-role (DR) USB interfaces. DR being both host and device. All three controllers are USB 2.0 and support all three speed definitions: HS (480 Mbps), FS (12 Mbps) and LS (1.5Mbps). The PHY used is the SMSC USB3300 device, which is capable of being configured as either a device or a host. The USB3300 uses ULPI interface to connect with the MPC8536. The Figure below shows the overall connections of the USB ports.



The 24MHz reference clock is derived from the 25MHz system reference by a PLL in the interface FPGA. All three USB interfaces are connected to a Samtec QTS-025-02 high speed terminal strip.The external USB connections beyond the module are platform dependent (e.g. 64EP3, 5DP3).

Note: Only “USB2” port is accessible as external I/O from card platform.

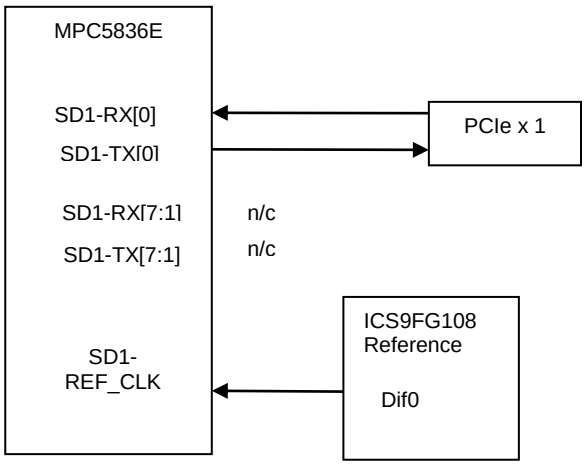
PCI Express

(not externally accessible from card platform I/O pins)

The U3 PCI Express controller supports endpoint and root complex configurations, with a x1 2.5GHz serial link. As both an initiator and a target device, the PCI Express interface is capable of high-bandwidth data transfer and is designed to support next generation I/O devices. Upon coming out of reset, the PCI Express interface performs link width negotiation and exchanges flow control credits with its link partner. Once link auto negotiation is successful, the controller is in operation.

The MPC8536 processor contains two high-speed serializer /deserializer (SerDes) ports. SerDes1 is used for PCIe connectivity. The MPC8536 uses SerDes1 configured to operate as a PCIe x1 interface.

- Compatible with the PCI Express™ Base Specification, Revision 1.0a
- Supports root complex (RC) and endpoint (EP) configurations
- 32- and 64-bit address support
- x1 link support
- Supports accesses to all PCI Express memory and I/O address spaces (requestor only)
- Supports posting of processor-to-PCI Express and PCI Express-to-memory writes
- Supports strong and relaxed transaction ordering rules
- Baseline and advanced error reporting support
- One virtual channel (VC0)
- 256-byte maximum payload size (MAX_PAYLOAD_SIZE)
- Supports three inbound general-purpose translation windows and one configuration window
- Supports four outbound translation windows and one default window
- Supports eight non-posted and four posted PCI Express transactions
- Supports up to six priority 0 internal platform reads and eight priority 0 to 2 internal platform writes. (The maximum number of outstanding transactions at any given time is eight.)
- Credit-based flow control management
- Supports PCI Express messages and interrupts



As an initiator, the PCI Express controller supports memory read and write operations with a maximum transaction size of 256 bytes. In addition, configuration and I/O transactions are supported if the PCI

Express controller is in Root Complex mode. As a target interface, the PCI Express controller accepts read and write operations to local memory space. When configured as an End Point device, the PCI Express controller accepts configuration transactions to the internal PCI Express configuration registers. Message generation and acceptance are supported in both RC and EP modes. Locked transactions and inbound I/O transactions are not supported.

The PCIe x1 interface is connected to a Samtec QTS-025-02 High speed terminal strip.The PCIe connections beyond the module are platform dependent (e.g. 64EP3, 5DP3).

PCI Express Reference Clock

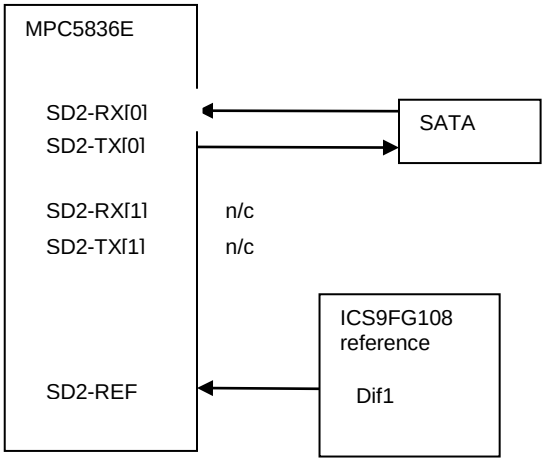
PCI express clock reference is supplied by the ICS9GF108, programmable time generator. The reference input clock is crystal derived 25MHz. The output frequency of the ICS9FG108 is fixed at 100MHz. The spread spectrum option for ISC9FG108 is disabled.

SATA

(not externally accessible from card platform I/O pins)

On the U3 module, SerDes2 can be configured to operate as a SATA controller. Interface selection is determined at power-on reset. Please refer to Table (xx) in the appendix for power-on reset values. On the U3 module the MPC8536 uses SerDes2 strictly for a single SATA connection.

- Complies with Serial ATA 2.5 Specification
- Supports speeds: 1.5 Gbps (first-generation SATA), 3 Gbps (second-generation SATA and eSATA)
- Supports advanced technology attachment packet interface (ATAPI) devices
- Contains high-speed descriptor-based DMA controller
- Supports native command queuing (NCQ) commands
- Supports port multiplier operation
- Supports hot plug including asynchronous signal recovery



The SATA interface is connected to a Samtec QTS-025-02 high speed terminal strip. The SATA connections beyond the module are platform dependent (e.g. 64EP3, 5DP3).

SATA Reference Clock

SATA clock reference is supplied by the ICS9GF108 at fixed at 100MHz. This clock is shared with the PCIe block.

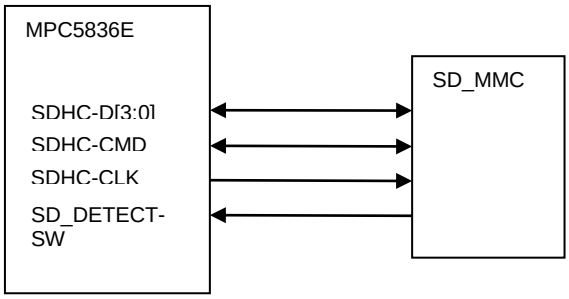
Enhanced Secure Digital Host Controller

(not externally accessible from card platform I/O pins)

The enhanced secure digital host controller (eSDHC) provides an interface between the host system and these types of memory cards:

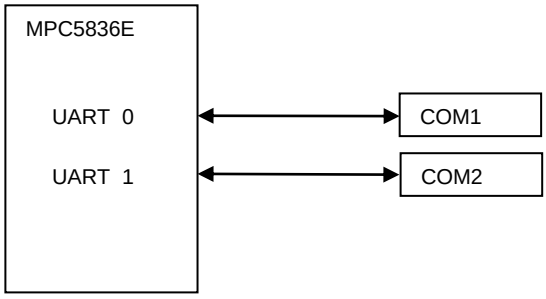
MultiMediaCard (MMC) - MMC is a universal low-cost data storage and communication medium designed to cover a wide area of applications. Old MMC cards are based on a 7-pin serial bus with a single data pin, while the new high-speed MMC communication is based on an advanced 11-pin serial bus designed to operate in a low voltage range.

Secure Digital (SD) Card - The secure digital (SD) card is an evolution of old MMC technology. It is specifically designed to meet the security, capacity, performance, and environment requirements inherent in the emerging audio and video consumer electronic devices. The physical form factor, pin assignments, and data transfer protocol are forward-compatible with the old MMC.



Serial Ports

The MPC8536DS connects four wires (RTS, CTS, TXD, RXD) for both serial ports to serial level transceivers. The default mode is 4-wire, so RTS/CTS flow control is supported on these connectors.



I2C Addressing

(not externally accessible from card platform I/O pins)

I2C

The MPC8536 has two separate I2C buses. The I2C bus connections are summarized below:

I2C Bus Device Map

I2C Address	Device
0x6E	SerDes1 Clock Generation (ICS9FG108)
0x69	Serdes 2 Clock Generation (ICS841)
0x68	Battery Backed Up RTC with 236 Bytes of SRAM (DS3232)
0x57	System ID EEPROM (Write Protected)
0x4C	Temperature Monitor (ADT7461).

Real Time Clock

The Real Time Clock (RTC) can be used to provide a system time and date function or can be used as an event timer.

Device: Intersil ISL1208IU8

I2C address: 0x68

Temperature Sensor

The MPC8536 has two pins connected to a thermal body diode on the die, allowing direct temperature measurement. These pins are connected to the ADT7461 device, which contains standard PC-compatible hardware monitoring logic, including a thermal measurement port. This device allows direct reading of the temperature of the die and is accurate to ± 1°C.

Device: On Semi, ADT7461ARMZ

I2C address: 0x4C

SPI

FRAM

The FM25CL64 is a 64KB nonvolatile memory. The FRAM is connected to the processor through the serial peripheral interface (SPI). Methods are provided in the U3 BSP and proc library to access the FRAM features.

- Organized as 8,192 x 8 bits
- Unlimited read/write cycles

EEPROM

M25P128VME6

The M25P128 is a multi-level 128Mbit (16Mbit x 8) serial flash memory, with advanced write.

Protection mechanisms accessed by a high speed SPI-compatible bus.

The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction. The memory is organized as 64 sectors, each containing 1,024 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 65,536 pages, or 16,777,216 bytes. The whole memory can be erased using the Bulk Erase instruction or a sector at a time, using the Sector Erase instruction.

Clocks

Table below summarizes the clock requirements of the MPC8536DS. Completely independent and isolated clocks, such as those of the DDR interfaces, are not discussed here.

SYSCLK/DDCLK

Timing within the MPC8536 is derived from the SYSCLK and DDRCLK input pin. SYSCLK and DDRCLK are generated by two IDT5V40501 frequency synthesizers. The syclk-s[1:0] value is factory programmed in to CPLD U3. Table below summarizes the default settings programmed into U3. Input reference frequency is 25.0 MHz.

Clock	Destination	Clock Frequency	Type	Notes
SYSCLK	MPC8536 SYSCLK	120.0 MHz	LVTTL	Programmed Default
DDRCLK	MPC8536 DDRCLK	78.125 MHz	LVTTL	Programmed Default
REFCLK ICS9F108	MPC8536 SD1_REFCLK(p,n)	100.00 MHz	LVDS	PEX: 100.00 MHz
	MPC8536 SD2_REFCLK(p,n)			
	SD2-CLK0			

GPIO

The MPC8536 processor has no user assignable GPIO signals. Hardware signal assignments are, however, listed in the Appendix for reference.

Configuration

Boot Location/ Boot Hold-Off

The U3 provides startup configuration information for u-boot or Linux, VxWorks, etc. The MPC8536 local bus provides access to boot code stored in flash memory and to general-purpose peripherals. For the MPC8536DS, the primary purpose of the local bus is access to the bootable flash images and to system configuration/control through the onboard FPGA.

Boot ROM location is controlled on board jumper JP[9:8].

JP[9:8]	Boot		Note
0 0	On-Chip Boot ROM SPI Configuration.	Boot Hold-Off Mode = 1	
0 1	On-Chip Boot ROM eSDHC Configuration.	Boot Hold-Off Mode = 1	
1 0	Local Bus FCM 8-Bit NAND Flash Large Page.ECC.	Boot Hold-Off Mode = 0	
1 1	Local Bus FCM 8-Bit NAND Flash Large Page ECC.	Boot Hold-Off Mode	Default

JP[x] 0, indicates jumper is in

Boot sequencer configuration **cfg_boot_seq[0:1]** 11 Boot sequencer is disabled

U3 Address Map

OFFSET (Byte)	Name	Function/Notes
0xE000'0000	U3ID	0x5533 = "U3"
0xE000'0002	ModOff	Modbus Offset (2..0). Selects position of CS2 Modbus access window into modbus space. This nominally correlates to module select: 7: Corresponds to Modbus (31) – Unused 6..1 Corresponds to Modbus(30..25) 0: Unused
0xE000'0004	Revision	
0xE000'0006	Ints	15: Test Interrupt – Always Active 14..11 Unused 10: Temperature 9: VME Interrupt – Write 1 to Clear (AKA upint1) 8: Module Interrupt – Write 1 to Clear (AKA upint0) 7..0: TRAM Touched (by Mod/Vme, Not MPC8536) (For bits 9..0, Write 1 to Clear)
0xE000'0008	Intmask	Mask for Above
0xE000'000A	Gpout	14..12: Unused 11: Ethactled2 10: Ethspdled2 9: Ethactled1 8: Ethspdled1 7: Eefclk_spr 6..4: Refclk_sel[6..4] 3: Usb_rst 2: Eth_rst_n 1: Framwr_n 0: Eewr_n
0xE000'000C	Dummyhi	15..3 Unused 2 PROC_PWR_EN 1 PROC_ASLEEP 0 Mod_rd_n
0xE000'000E	Dummylo	15..12 Unused 11..8 MPClwe_n 7 MPClgpl5 6 MPClgpl3 5 MPClgpl2 4 MPClgpl1 3 MPClgpl0 2..0 Unused
0xE000'0010	Reset	Write 55AA Here for a Hardware Reset
0xE000'0012- 0xE000'001F	(Unused)	
0xE000'0020- 0xE000'003F	Test ROM	Build Time Alterable Test Pattern
0xE100'0000- 0xE13F'FFFF	TRAM	Transfer RAM (SRAM)
0xE200'0000- 0xE3FF'FFFF	Modbus	Access Window Based at ModOff 0xE000'0002) <<24

Software Libraries

U3 BSP Processor Module Library

The U3 processor library package provides function interfaces to the on module functionality as well as the ModBus and VME/PCI interfaces. This package contains *Help* documentation (in html format) that explains all the functions available in the library. The package also contains the source code (*.h, *.c) files as well as the files needed to build the library using VxWorks or similar. Example programs are also provided to demonstrate the usage of the libraries in typical applications of the module.

Example of platform specific libraries that can be utilized in conjunction w/ U3 module specific library:

64C3 Library

The VME64C3 library package provides function interfaces to all the modules available for this multi-function I/O card. This package contains Help documentation (in html format) that explains all the functions available in the library. The package also contains the source code (*.h, *.c) files as well as the files needed to build the library using the Analog Device VisualDSP++ IDE. Example programs are also provided to demonstrate the usage of the libraries in typical applications of this card.

Associated Documents

NAI Documents (PENDING – All documentation available from U3 BSP/SSK)

- Programmer's Reference Guide for NAI U3 Processor Module
- U3 Ethernet Download
- U3 USB Download

Processor

- MPC8536 PowerQUICC™ III Processor Family Reference Manual
- (MPC8536RM) — This document describes the MPC8536 architecture and functionality in detail
- PowerQUICC DDR2 SDRAM Controller Register Setting Considerations (AN3369)

Booting from On-Chip ROM (eSDHC or eSPI)

Freescale Semiconductor AN3659 rev 1, 12/2010

ARINC 429/575 Six Channel, Tx/Rx (Module A4)

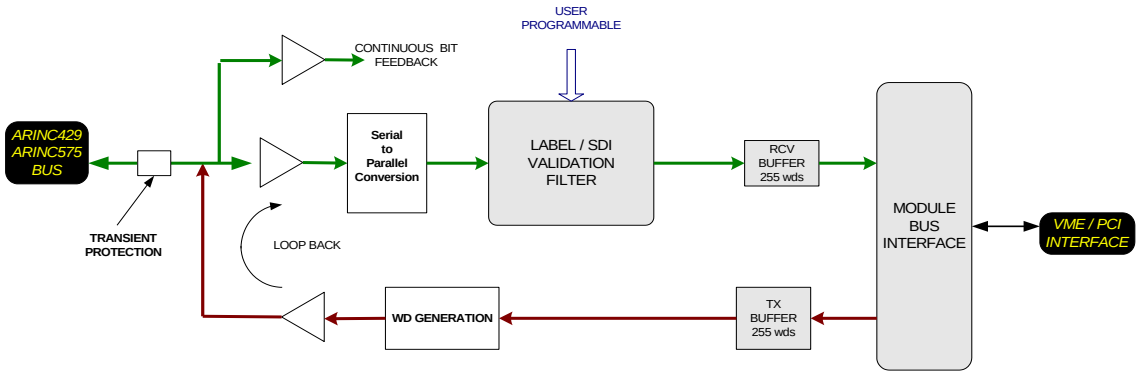
Features

- Receive / Transmit mode programmable / per channel
- 100 KHz or 12.5 KHz operation per channel
- Transmit: 255 word FIFO or scheduled transmits per channel
- Async transmits during scheduled transmits
- Receive: 255 word FIFO or mailbox buffering per channel
- SDI/Label filtering programmable / per channel
- AR429 or 575 mode programmable / per channel
- Selectable hardware parity generation/checking
- Receive time stamping
- Double buffered Rx / Tx
- Continuous BIT
- Loop-back test
- Tri-stateable Outputs
- Hi and Lo speed Slew Rate Outputs

ARINC 429/575 Overview

ARINC 429 is the most commonly used data bus for commercial and transport aircraft. It employs unidirectional transmission of 32 bit words over two wire twisted pairs using bipolar RZ format. Messages are transmitted at 12.5 kbps, or 100 kbps to other system elements that are monitoring the bus messages. The transmitter is always transmitting either 32-bit data words or the Null state. **ARINC SPECIFICATION 429 PART1-16** defines the electrical standard, data characteristics and protocols.

ARINC 575 is an older specification very similar to ARINC 429 but now obsolete. Electrically, ARINC 575 is generally compatible with low speed ARINC 429. There are some ARINC 575 implementations that use a bit rate that is much slower than ARINC 429 and are not electrically compatible. Also, in some cases, ARINC 575 words use bit 32 as parity (as does ARINC 429); in other cases bit 32 is used as data.



Configurable Rcv/Txmit ARINC Channel

Functional Description

The AR429 module provides up to six programmable ARINC-429 channels. Each channel is software selectable for transmit and/or receive, Hi or Lo speed, and odd or no parity. Thus the module can support multiple ARINC429 and 575 channels simultaneously.

Receive Operation

Serial BRZ data is decoded for logic states: one, zero or null. Once Word Gap is detected (4 null states) the receiver waits for either a zero or one state to start the serial to parallel shift function. If a waveform timing fault is detected before the serial/parallel function is complete, operation is terminated and the receiver returns to waiting for Word Gap detection. The serial to parallel output data can validated for odd parity, Label and SDI. If validation (filtering) is enabled, the module compares the SDI/Label of incoming ARINC messages to a list of desired SDI/Labels in validation (match) memory and only stores messages with an SDI/Label in the list. The message is stored in the receive FIFO or mailbox, depending if the channel is in FIFO receive mode or mailbox receive mode. In FIFO Receive Mode, received ARINC messages / words are stored with an associated status word and an optional time-stamp value in the channel's receive FIFO. In mailbox mode, received ARINC words are stored in mailboxes or records that are indexed by the SDI/Label of the ARINC word. Each mailbox contains a status word associated with the message, the ARINC message / word, and an optional 32 bit timestamp value. The status word indicates parity error status and whether the message is a new message or one that has been read already. Each receive channel is double buffered to prevent reading partially received ARINC words and timestamps.

Transmit Operation

Transmitters are tri-stated when TX is not enabled. Transmit operates in one of three modes: Immediate FIFO, Triggered FIFO, and Scheduled. In immediate mode, ARINC data is sent as soon as data is written to the transmit FIFO. In Triggered FIFO mode, a write to the trigger register is needed to start transmission of the transmit FIFO contents. Transmission continues until the FIFO is empty. To transmit more data after the FIFO empties out, issue a new trigger after filling the transmit FIFO with new data.

For either FIFO mode, a transmit FIFO Rate register is provided to control rate of transmission. The contents of this register specify the gap time between transmitted words from the FIFO. The default is the minimum ARINC gap time of 4-bit times.

Schedule mode transmits ARINC data words according to a prebuilt schedule in Schedule memory. In the table, various commands define what messages are sent and at what rate they are transmitted at. The ARINC data words are stored in the TX Message memory and can be updated on the fly as the schedule executes. While in Schedule Mode, an ARINC word can be transmitted asynchronously during gap times that are long enough to accommodate the 40 bit times that it takes to transmit a a 4 bit gap time plus the async data word and its 4 bit gap time. While the schedule is running, write the data word to the last location of the Tx Message memory. After it has transmitted, the Async Data Available bit will be cleared from the Channel Status register and the Async Data Sent Interrupt will be set if enabled. The Async Data Available bit in Channel Status also gets cleared by a Stop Cmd in a schedule or if a Transmit Stop command is issued from the Transmit Stop register. Use the Fixedgap command instead of the Gap command to disable async transmissions during the schedule gap time. Gap and Fixed-gap commands can both be used when building the transmit schedule. Each transmit channel is double buffered to prevent transmission of partially written 32-bit ARINC words.

Schedule Transmit Commands

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TX SCHEDULE MEMORY	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	STOP CMD
	0	0	0	1	X	X	X	X	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	**MESSAGE CMD[1]**
	0	0	1	0	X	X	X	X	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	GAP CMD[1]
	0	0	1	1	X	X	X	X	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	FIXEDGAP CMD[1]
	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	PAUSE CMD
	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	SCH INTERRUPT CMD
	0	1	1	0	X	X	X	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	JUMP CMD[2]

Note 1: MA7-MA0 = Address of ARINC data word or gap time in Tx Message memory (organized as 256x32).
Note 2: SA8-SA0 = Address of next command in Tx Schedule memory (organized as 512x16) to execute.

Schedule mode begins execution at Schedule memory address 000h.

Message

This command points to a location in Transmit Message memory which contains the actual ARINC data word to be sent. The word is transmitted when the next Message, Gap, or Fixed-gap command is executed. The ARINC word in Tx Message memory can be updated while the schedule is running.

Gap

This command points to a location in Transmit Message memory which contains a 20 bit number that specifies the gap time in bits to wait. Values less than 4 are invalid. If the previous command was Message, then that message is transmitted and then the transmitter waits out the specified gap time transmitting nulls. An exception to this is if there is an async data word available. If the gap time is greater or equal to 40 bit times (4-bit gap time plus one ARINC word plus another 4-bit gap time) then the following occurs. The message appended with a 4 bit gap time is transmitted, and then the async data word is transmitted. If a new async data word is made available and the remaining gap time is large enough to accommodate another async data word transmission then the new async data word will be transmitted after a 4-bit gap time. Multiple async data word transmissions can thus occur as long as the remaining gap time is large enough to accommodate a message and the required minimum 4-bit gap time. Otherwise, the transmitter waits out the remaining gap time before executing the next command.

If the previous command was not Message, then the transmitter waits the specified gap time before executing the next command. However, if there is an async data word available and the remaining gap time is greater or equal to 40 bit times (4 bit gap time plus one ARINC word plus another 4 bit gap time) then the following occurs. The async data word appended with a 4 bit gap time is transmitted. If a new async data word is made available and the remaining gap time is large enough to accommodate another async data word transmission then the new async data word will be transmitted after a 4 bit gap time. Multiple async data word transmissions can thus occur as long as the remaining gap time is large enough to accommodate a message and the required minimum 4 bit gap time. Otherwise, the transmitter waits out the remaining gap time before executing the next command.

FixedGap

This command points to a location in Transmit Message memory which contains a 20-bit number that specifies the gap time in bits to wait. Values less than 4 are invalid. If the previous command was Message, then that message is transmitted with the specified gap time appended. If the previous command was not Message, then the transmitter waits the specified gap time before executing the next command. The difference between the FixedGap and Gap command is that FixedGap will prevent the transmission of async data words during the gap time. Use FixedGap to only allow nulls to be transmitted during the gap time.

Pause

This command causes the transmitter to pause execution of the schedule after transmitting the current word. Either a Transmit Trigger command is issued to resume execution or a Transmit Stop command is issued to halt execution.

Interrupt

This command causes the Schedule Interrupt to be set if Schedule Interrupt is enabled. An unlatched version of this flag is also visible in the channel status register.

Jump

Jumps to the 9 bit address in Schedule memory pointed to by this command and begins execution there.

Stop

This command causes the transmitter to stop execution of the schedule after transmitting the current word.

Transient Protection

The module is normally configured for transient protection, but can be specified without if protection is implemented externally.

Built-In-Test

In Transmit operations, internal transmit data is compared to loop-back data received by the ARINC receivers. If the data does not match, the BIT ERROR bit is set and held in the channel status register and/or an interrupt is generated if enabled. When the channel is configured for Receive operation, receive data is continuously monitored via a secondary parallel path circuit and compared to the primary input receive data. If the data does not match, the BIT ERROR bit is set and held in the bit status register and channel status register and/or an interrupt is generated if enabled. The BIT ERROR bit can be cleared by reading the bit status register. BIT is always active regardless of whether channel RX or TX is enabled. BIT can be disabled on a per channel basis via the Channel Control Low register.

Loop-Back

Transmit data is looped-back continuously through the unused receive logic of the same channel and is made available for user verification if the channel receiver is also enabled.

Specifications

Specifications	ARINC 429	ARINC 575
Mode of Operation	Differential	Differential
Data Rate	100 KHz	12.5KHz
Driver Output Signal Level (Min Loaded)	±10.0V	±10.0V
Receiver Input Voltage Range	-17V to +17V	-17V to +17V
Receiver Input Resistance (Ohms)	15K	15K
Module Supply current, no load (nom):	0.8A@+5V; 0.05A@+12V; 0.05A@-12V	
Module Supply current, no load (peak):	1.0A@+5V; 0.1A@+12V; 0.1A@-12V	

Module Factory Defaults

Speed:	12.5Khz
Gap Time:	4 bits
Interrupt Level:	0
Interrupt Vector:	0x00
Mode:	FIFO
Parity (Odd):	Enabled
Receivers:	Disabled
Transmitters:	Disabled
SDI/Label Matching:	Disabled
Number of Words TX Buffer:	0
Number of Words RX Buffer:	0
RX Buffer, Almost Full:	0x80h
TX Buffer, Almost Empty:	0x20h
TX-RX Configuration High:	0
TX-RX Configuration Low:	0
Channel Control High:	0
Channel Control Low:	0
Built-In-Test:	Enabled

Registers and Delays

There can be a delay of up to 10us before these commands take effect:

- Enabling or Disabling Tx or Rx

Changing Speeds - There can be a delay of up to 100us before these commands take effect:

- Reset/Clear Commands in Channel Control High register
- Reset Module command
- There can be a delay of up to 1 sec after the Interrupt Vector register is written before they take effect

Tx (Transmit) Buffer (FIFO)

Type: unsigned character word
Range: 0 to FFFFh
Read/Write: W
Initialized Value: Not Applicable

This register is the transmit data FIFO. In immediate or triggered FIFO modes, transmit data is placed here prior to transmission. ARINC data words are 32-bits and are placed into the FIFO 16bits at a time starting with the UPPER 16 bits. The FIFO level is incremented after the LOWER 16 bits are written. This memory is shared with the Tx Message memory and is only available in Tx FIFO modes.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TRANSMIT FIFO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Rx (Receive) Buffer (FIFO)

Type: unsigned integer word
Range: 0 to FFFFh
Read/Write: R
Initialized Value: Not Applicable

In FIFO receive mode, the received ARINC messages are read back from here. Perform three reads from this register to retrieve the Status word, the upper 16 bits of the ARINC data word, and the lower 16 bits of the ARINC data word, respectively. If Time Stamping is enabled, perform 2 more reads to retrieve the upper and lower 16 bits of the timestamp respectively.

In Mbox receive mode, this FIFO contains the 10 bit SDI/Label of newly received messages. This provides a list to the user showing which mailboxes contain new messages since the last time this FIFO was read.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
FIFO mode	X	X	X	X	X	X	X	X	X	X	X	X	X	X	N	PE	Message Status Wd
FIFO mode	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	Data Words
MBOX mode:	X	X	X	X	X	X	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	SDI/Label of received ARINC word

PE = Parity Error — '1' Calculated parity does not match the received parity bit
N = New message — '1' Message has not been read yet
A10 – A1 — Lower 10 bits of the ARINC data word where A8 is the msb of the Label and A1 is the lsb. A10 and A9 are the SDI bits.

Rx FIFO (Buffer) Threshold

Type: unsigned integer
Range: 0 to 255
Read/Write: R/W
Initialized Value: 128 (80h)

This register specifies the level of the receive buffer, equal or above, at which the RxFIFO Almost Full Status bit D1 in the Channel Status register is flagged (High True). If the interrupt is enabled (see **Interrupt Enable Register)**, a SYSTEM interrupt will be generated when the receive FIFO level increases and reaches this level. This register does NOT get reset by a channel reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Rx BUFFER AF VALUE	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Tx FIFO (Buffer) Threshold

Type: unsigned integer
Range: 0 to 255
Read/Write: R/W
Initialized Value: 32 decimal (20h)

This register specifies the level of the transmit buffer, equal or below, at which the TxFIFO Almost Empty Status bit D5 in the Channel Status register is flagged (High True). If the interrupt is enabled (see **Interrupt Enable Register**), a SYSTEM interrupt will be generated when the transmit FIFO falls to this level. This register does NOT get reset by a channel reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Tx BUFFER AE VALUE	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Rx FIFO (Buffer) Level (Number of Rx Buffer Words)

Type: unsigned integer word
Range: 0 to 255
Read/Write: R
Initialized Value: 0

This register contains the number of ARINC messages in the receive FIFO in Receive FIFO mode. A message consists of the message status word, the upper 16 and lower 16 bits of the ARINC data word, and optionally the upper and lower 16 bits of the 32 bit timestamp. In Receive Mbox mode, this register contains the number of newly received messages.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
NUM WORDS RX BUFFER	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Tx FIFO (Buffer) Level (Number of Tx Buffer Words)

Type: unsigned integer word
Range: 0 to 255
Read/Write: R
Initialized Value: 0

Used only in the FIFO transmit modes, this register contains the number of ARINC 32 bit words in the transmit FIFO.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
NUM WORDS TX BUFFER	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Channel Control Low

Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: 0

This register is used for channel configuration. Allow 10us for commands to take effect. The Receiver Enable bit should be set after all receive parameters and filters have been set up. After setting this bit, the module will look for a minimum 4bit gap time before decoding any ARINC bits to prevent it from receiving a partial ARINC word. The Transmit Enable bit should be set after all transmit parameters have been set up. This is especially important in Immediate FIFO Transmit mode since this mode will start transmitting as soon as data is put into the Tx FIFO.

For the other transmit modes, a TX Trigger is required before transmission begins. The Parity Disable bit when set to 0, causes ARINC bit 32 to be treated as an odd parity bit. The transmitter calculates the ARINC odd parity bit and transmits it as bit 32. The receiver will check the received ARINC word for odd parity and will flag an error if is not. When set to Disable (1), parity generation and checking will be disabled and both the transmitter and receiver will treat ARINC bit 32 as data and pass it on unchanged. When the Match Enable bit is set to 1, the receiver will only store ARINC words which match the SDI/Labels enabled in Rx Match memory. If the STORE ON ERROR bit is set to (0) and MATCH Enable is set to (1) and parity is enabled, received words with a parity error that match the filter list will be stored in the receive buffer. Set the STORE ON ERROR bit to (1) to not store received words that contain parity errors.

When Time Stamp Enable bit is set to 1, the receiver will store a 32-bit time stamp value along with the received ARINC word. There is one time stamp counter per module and it is used across all 6 channels. It has 4 selectable resolutions and can be reset via the Time Stamp Control register. It is recommended to clear the Receive FIFOs whenever the Receive mode or Time Stamp Enable mode is changed to ensure that extraneous data is not leftover from a previous receive operation. When the STORE ON ERROR DISABLE bit is set (1) and odd parity is enabled, received words that contain a parity error will not be stored in the receive buffer.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CONTROL LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	RECEIVER ENABLE =1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	RECEIVE MODE: 0=FIFO / 1=MBOX
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	TRANSMIT ENABLE =1
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	TRANSMIT MODE0[1]
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	TRANSMIT MODE1[1]
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	SPEED: 0=12.5KHZ / 1=100KHZ
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	PARITY DISABLE = 1
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	MATCH ENABLE = 1
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	TIMESTAMP ENABLE = 1
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	BUILT-IN-TEST DISABLE = 1
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	STORE ON ERROR DISABLE = 1
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	RESERVED
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED

Notes: **1**. Transmit modes: (D4:D3)

(0:0) = Immediate FIFO mode
(0:1) = Schedule mode
(1:0) = Triggered FIFO mode
(1:1) = Invalid mode

Channel Control High

Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: 0

This register is used to clear the FIFOs and match memory. The channel reset bit will clear out Channel Control Low and Interrupt Enable registers as well as reset the transmit and receive circuits. However, it will not reset the channel Transmit FIFO Rate, Tx Buffer Almost Empty, and Rx Buffer Almost Full registers. If Schedule Interrupts are enabled in the Interrupt Enable register, then reading the Interrupt Status register will clear the bit in both the Channel Status and Interrupt Status registers. The Schedule Interrupt Clear bit D5 can be used to clear the Schedule Interrupt bit D10 in the Channel Status register if the interrupt is not enabled.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION[1]
CONTROL HI	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	**1**	TRANSMIT FIFO CLEAR
	X	X	X	X	X	X	X	X	X	X	X	0	0	0	**1**	0	RECEIVE FIFO CLEAR
	X	X	X	X	X	X	X	X	X	X	X	0	0	**1**	0	0	MATCH MEMORY CLEAR
	X	X	X	X	X	X	X	X	X	X	X	0	**1**	0	0	0	CHANNEL RESET
	X	X	X	X	X	X	X	X	X	X	X	**1**	0	0	0	0	RESERVED
	X	X	X	X	X	X	X	X	X	X	**1**	0	0	0	0	0	SCHEDULE INTR. CLEAR

Note: 1. Firmware will clear bit. Allow 100us for command to complete.

Channel Status

Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: not applicable

This register describes the status of 14 different events. Some events are NOT latched. They are dynamic. Use this register to read current or real-time status. The BUILT-IN-TEST (BIT) ERROR bit is latched and will stay set once an error is detected and can be cleared by reading the BIT Status register. The Schedule Interrupt bit can be cleared by reading the Interrupt Status register if its interrupt is enabled or it can be cleared via the Channel Control High register. See specific registers for function description and programming. The Rx Data Available bit is set when the receive FIFO is not empty. The Rx FIFO Overflow bit will set whenever the receiver has to discard data because the receive FIFO was full and new data was received. The Async Data Available bit in Channel Status also gets cleared by a Stop Cmd in a schedule or if a Transmit Stop command is issued from the Transmit Stop register. The Tx Run bit is set whenever the transmitter is executing a schedule or actively transmitting the contents of the transmit FIFO. The Tx Pause bit is set whenever the transmitter has been paused in schedule mode.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CHANNEL STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	RX DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	RX FIFO ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	RX FIFO FULL
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	RX FIFO OVERFLOW
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	TX FIFO EMPTY
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	TX FIFO ALMOST EMPTY
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	TX FIFO FULL
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	PARITY ERROR
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	RECEIVE ERROR
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	BUILT-IN-TEST ERROR
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	SCHEDULE INTERRUPT
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	ASYNC DATA AVAILABLE
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	TX RUN
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	TX PAUSE
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED

Interrupt Enable

Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: not applicable

This register provides for Interrupt Enabling. Set bit high True to enable interrupts. Status will still be reported in status registers. See specific registers for function description and programming.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERRUPT ENABLE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	RX DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	RX FIFO ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	RX FIFO FULL
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	RX FIFO OVERFLOW
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	TX FIFO EMPTY
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	TX FIFO ALMOST EMPTY
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	RESERVED
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	PARITY ERROR
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	RECEIVE ERROR
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	BUILT-IN-TEST ERROR
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	SCHEDULE INTERRUPT
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	ASYNC DATA SENT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	TX COMPLETE
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED

Interrupt Status

Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: not applicable

This register describes the status of 12 different events. These events are latched when they occur and are enabled by their corresponding Interrupt Enable bits in the Interrupt Enable register. See specific registers for function description and programming. Reading this register clears the interrupts that were set. The Rx Data Available interrupt sets when the first data word is received into an empty receive FIFO. The Rx FIFO Overflow bit will set whenever the receiver has to discard data because the receive FIFO was full and new data was received. The Schedule interrupt will set when the schedule interrupt command is executed in the programmed schedule. The Tx Complete interrupt will set when Tx Run goes inactive.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERRUPT STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	RX DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	RX FIFO ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	RX FIFO FULL
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	RX FIFO OVERFLOW
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	TX FIFO EMPTY
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	TX FIFO ALMOST EMPTY
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	RESERVED
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	PARITY ERROR
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	RECEIVE ERROR
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	BUILT-IN-TEST ERROR
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	SCHEDULE INTERRUPT
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	ASYNC DATA SENT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	TX COMPLETE
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RESERVED

Transmit FIFO Rate (Hi+Lo)

Type: 20-bit unsigned integer
Range: 0-FFFFFh , Rate High & Low Registers combined
Read/Write: R/W
Initialized Value: 4
Mode: FIFO

Both the Rate High Register and Rate Low Register combined together determine the Gap time between transmitted ARINC messages in FIFO transmit modes. Each LSB is 1 bit time. Rates less than 4 are not valid. This register does NOT get reset by a channel reset.

RATE HIGH REGISTER																	RATE LOW REGISTER															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Mailbox (MBOX) Address Register

Type: unsigned integer word
Range: 0 to FFFFh
Read/Write: R/W
Initialized Value: 0
Mode: MBOX

Before a MBOX message is accessed, set this register to point to the mailbox to be accessed. The five word message (status word, ARINC Hi, ARINC Low, Timestamp Hi, Time Stamp Lo) can then be accessed by reading the MBOX STATUS and MBOX DATA registers.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MBOX ADDRESS	X	X	X	X	X	X	**A10**	**A9**	**A8**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	

A10 – A1 = Lower 10 bits of the ARINC data word where A8 is the msb of the Label and A1 is the lsb. A10 and A9 are the SDI bits.

Mailbox (MBOX) Status Register

Type: unsigned integer word
Range: 0 to FFFFh
Read/Write: R
Initialized Value: 0
Mode: MBOX

After writing the MBOX Address Register, this register MUST BE READ FIRST to retrieve the message status word. Next, read the MBOX Data register twice to retrieve the upper and lower 16 bits of the ARINC data word respectively. If Time Stamping is enabled, read the MBOX Data register two more times in succession to retrieve the upper and lower 16 bits of the timestamp respectively.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MBOX STATUS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**N**	**PE**	Message Status Wd

PE = Parity Error '1' Calculated parity does not match the received parity bit
N = New message '1' Message has not been read yet
Note* : If Time stamping enabled.
Note: This register must be read first before retrieving valid data from the MBOX Data register.

Mailbox (MBOX) Data Register

Type: unsigned integer word
Range: 0 to FFFFh
Read/Write: R
Initialized Value: 0
Mode: MBOX

After reading the MBOX Status register first, read this MBOX Data register in succession to retrieve the upper and lower 16 bits of the ARINC data word respectively. If Time Stamping is enabled, read the MBOX Data register two more times in succession to retrieve the upper and lower 16 bits of the timestamp respectively.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MBOX DATA(0)	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	Hi ARINC Data Word
MBOX DATA(1)	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	Lo ARINC Data Word
MBOX DATA(2)	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	Hi Timestamp Data Word*
MBOX DATA(3)	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	Lo Timestamp Data Word*

Note* : If Time Stamping enabled.
Note: MBOX STATUS register must be read first before retrieving valid data from this register.

Receive Data Unbuffered Register

Type: binary word
Range: not applicable
Read/Write: R
Initialized Value: 0h

This register contains the unbuffered receive signals from the ARINC receivers. This register is only used for test purposes.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Receive Data Unbuffered	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**A+**	**B-**	CHANNEL 1 RX SIGNAL
	X	X	X	X	X	X	X	X	X	X	X	X	**A+**	**B-**	X	X	CHANNEL 2 RX SIGNAL
	X	X	X	X	X	X	X	X	X	X	**A+**	**B-**	X	X	X	X	CHANNEL 3 RX SIGNAL
	X	X	X	X	X	X	X	X	**A+**	**B-**	X	X	X	X	X	X	CHANNEL 4 RX SIGNAL
	X	X	X	X	X	X	**A+**	**B-**	X	X	X	X	X	X	X	X	CHANNEL 5 RX SIGNAL
	X	X	X	X	**A+**	**B-**	X	X	X	X	X	X	X	X	X	X	CHANNEL 6 RX SIGNAL

Transmit Trigger Register

Type: binary word
Range: not applicable
Read/Write: W
Initialized Value: 0h
Modes Affected: Triggered FIFO and Schedule Transmit

This register sends a trigger command to the transmitter and is used to start transmission in Triggered FIFO or Scheduled Transmit modes. It is also used to resume transmission after a scheduled pause or Transmit pause command.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TRANSMIT TRIGGER	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	TRIGGER CH1
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	TRIGGER CH2
	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	TRIGGER CH3
	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	TRIGGER CH4
	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	X	TRIGGER CH5
	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	X	X	TRIGGER CH6

Transmit Pause Register

Type: binary word
Range: not applicable
Read/Write: W
Initialized Value: 0h
Modes Affected: Triggered FIFO and Schedule Transmit

This register sends a command to pause the transmitter after the current word and gap time has finished transmitting. Used to pause transmission in Triggered FIFO or Scheduled Transmit modes. Issue a Transmit Trigger command to resume transmission or issue a Transmit Stop command to halt transmission.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TRANSMIT PAUSE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	PAUSE CH1
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	PAUSE CH2
	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	PAUSE CH3
	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	PAUSE CH4
	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	X	PAUSE CH5
	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	X	X	PAUSE CH6

Transmit Stop Register

Type: binary word
Range: not applicable
Read/Write: W
Initialized Value: 0h
Modes Affected: All Transmit modes

This register sends a command to stop the transmitter after the current word and gap time has been transmitted. Also clears the transmit FIFO.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TRANSMIT STOP	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	STOP CH1
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	STOP CH2
	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	STOP CH3
	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	STOP CH4
	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	X	STOP CH5
	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	X	X	STOP CH6

Time Stamp Control Register

Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: 0000h (1 usec)

This register bit field determines the resolution of the timestamp counter. The LSB can have one of four time values. Set bit D2 to zero out the timestamp counter. The default LSB value is 1us. Bits D4-D3 is a binary count of how many times the module PLL has lost lock and should be zero. The count is reset when this register is read.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TIMESTAMP CONTROL	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	RESOLUTION[1]
	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	ZERO TIMESTAMP[2]
	X	X	X	X	X	X	X	X	X	X	X	**P1**	**P0**	X	X	X	PLL ERROR COUNT[3]

Note: 1: (D1:D0) LSB value, Read/write
0:0 1us
0:1 10us
1:0 100us
1:1 1ms

Note: 2: (D2) = Bit write only

Note: 3: (P1:P0) = Count of how many times PLL lost lock, resets to 0 on read. Read only. For internal test use.

Timestamp Hi + Lo Register

Type: unsigned integer
Range: 0 to 65535
Read/Write: R
Initialized Value: not applicable

The current 32-bit timestamp value can be read back through here. Read the upper word first to latch the entire 32-bit value into a holding register. The time value of each LSB is determined by the resolution set in the Timestamp Control Register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TIMESTAMP HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	UPPER WORD[1]
TIMESTAMP LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	LOWER WORD[1]

Note: 1: Read Hi register first.

Module Reset Register

Type: binary word
Range: not applicable
Read/Write: W
Initialized Value: 0h

This register sends a command to reset the entire 6 channel module to power up conditions. All FIFOs are cleared. However, it does not clear out any memories.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE RESET	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	

Memory Page Register

Type: unsigned integer word
Range: 0 to FFFFh
Read/Write: R/W
Initialized Value: 0

Due to the limited module address space available, the various module memories are accessed via a paging scheme. Before a memory is accessed, set this register to point to the page of memory that needs to be accessed. The 128 word page can then be accessed by reading or writing to the page window.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MEMORY PAGE	**CH2**	**CH1**	**CH0**	**M1**	**M0**	**P10**	**P9**	**P8**	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**	MEMORY PAGE REG
RCV. MEMORY	X	X	X	**1**	**1**	**A17**	**A16**	**A15**	**A14**	**A13**	**A12**	**A11**	**A10**	**A9**	**A8**	**A7**	RCV MEMORY ADDRESS

Ch2 -Ch0= Channel number : “000” to “101” corresponds to channels 1 to 6

M1- M0= Memory select:

“00” = Transmit Message memory 256x32. Accessed as 512x16, with even locations holding the upper word. 4 pages per channel. Used in Tx Schedule mode. Writes to a memory location must always be sequentially written with the upper then lower 16 bits since the data is internally buffered and written to memory as a 32 bit word.

“01” = Transmit Schedule memory 512x16. 4 pages per channel. Used in Tx Schedule mode.

“10” = Match Memory 1024x1. 8 pages per channel.

“11” = RCV memory 256kx16, CH2 – CH0 bits are ignored when accessing this memory. 2048 pages total. This mode is only used for testing. Normally accessed via receive FIFO or receive mbox registers.

P10 - P0 = Desired memory page. Each page is 128 x16 in size.
A17 - A7= Desired RCV memory page. 2048 pages of 128 x 16.

Memory Page Window

Type: unsigned integer word
Range: 0 to FFFFh
Read/Write: R/W
Initialized Value: N/A
Access the 128 word page of memory pointed to by Memory Page Register by reading or writing to 200h + offset, where offset is 0 to FEh in increments of 2 since these are 16-bit word accesses, not byte accesses.

Tx Message Memory Format

Type: unsigned integer word
Range: 0 to FFFFh
Read/Write: R/W
Initialized Value: N/A

This memory is shared with the Tx FIFO memory and is only available in Tx Schedule mode. The internal memory is 256 deep and 32 bits wide but is accessed via the 16 bit data bus as 512 x 16. Writes to a memory location must always be sequentially written with the upper then lower 16 bits since the data is internally buffered and written to memory as a 32 bit word. When reading back a memory location, the memory looks like a 512 x 16 memory and the upper 16 bits is read from the even locations and the lower 16 from the odd locations. This memory is also used to hold the 20 bit gap time value for the Gap and FixedGap commands in Tx Schedule mode. Values of 4 or less for the gap time are invalid. Each LSB equals one bit period of time, i.e. 10 us in High speed and 80 us in Low speed.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TX MESSAGE MEMORY	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	ARINC UPPER 16
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	ARINC LOWER 16
	X	X	X	X	X	X	X	X	X	X	X	X	G19	G18	G17	G16	GAP TIME UPPER 4
	G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	GAP TIME LOWER 16

Gap time values < 4 are invalid.

Tx Schedule Program Memory Format

Type: unsigned integer word
Range: 0 to FFFFh
Read/Write: R/W
Initialized Value: N/A

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TX SCHEDULE MEMORY	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	STOP CMD
	0	0	0	1	X	X	X	X	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	MESSAGE CMD[1]
	0	0	1	0	X	X	X	X	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	GAP CMD[1]
	0	0	1	1	X	X	X	X	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	FIXEDGAP CMD[1]
	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	PAUSE CMD
	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	SCH INTERRUPT CMD
	0	1	1	0	X	X	X	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	JUMP CMD[2]
	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	RESERVED
	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RESERVED

Note 1: MA7-MA0 = Address of Tx Message memory organized as 256x32.
Note 2: SA8-SA0 = Address of Tx Schedule memory organized as 512x16.

Rx Match Memory Layout

Type: unsigned integer word
Range: 0 to FFFFh
Read/Write: R/W
Initialized Value: 0

The address of the Rx Match memory corresponds to the SDI/Label messages to be received and stored. A10 – A1 = Lower 10 bits of the ARINC data word where A8 is the msb and A1 is the lsb of the Label. A10 and A9 are the SDI bits. This memory can be all cleared by setting the Match Memory Clear bit in the channel control high register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RX MATCH MEMORY	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	ENABLE MATCH=1

Async Tx Data (Hi + Lo)

Type: unsigned character word
Range: 0 to FFFFh
Read/Write: R/W
Initialized Value: 0

This memory location is the transmit async data buffer. Data intended to be transmitted asynchronously must be placed here prior to transmission. ARINC data words are 32-bits and are placed into the register 16 bits at a time starting with the HI 16 bits. The Async Data Available bit in Channel Status will automatically set after the LO 16 bits are written.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0xFC ASYNC TX DATA HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
0xFE ASYNC TX DATA LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

BIT Status Register

Type: binary word
Range: not applicable
Read/Write: R
Initialized Value: 0h

This register contains the Built-In-Test (BIT) status of all six channels on the module. When a BIT error is detected, the channel's respective bit is set to '1' in this register. Reading this register clears any set bits.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	BUILT-IN-TEST ERROR CH1
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	BUILT-IN-TEST ERROR CH2
	X	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	BUILT-IN-TEST ERROR CH3
	X	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	BUILT-IN-TEST ERROR CH4
	X	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	X	BUILT-IN-TEST ERROR CH5
	X	X	X	X	X	X	X	X	X	X	**1**	X	X	X	X	X	BUILT-IN-TEST ERROR CH6

DSP Compile Time

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value:

Read registers to determine DSP Compile Time in ASCII. The following table shows an example of the format. "Jul 27 2009 at 11:41:33" (factory use/reference only).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	ASCII
390h	0	1	1	1	0	1	0	1	0	1	0	0	1	0	1	0	"uJ"
392h	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	" l"
394h	0	0	1	1	0	1	1	1	0	0	1	1	0	0	1	0	"72"
396h	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	0	"2 "
398h	0	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0	"00"
39Ah	0	0	1	0	0	0	0	0	0	0	1	1	1	0	0	1	" 9"
39Ch	0	1	1	1	0	1	0	0	0	1	1	0	0	0	0	1	"ta"
39Eh	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0	0	"1 "
3A0h	0	0	1	1	1	0	1	0	0	0	1	1	0	0	0	1	":1"
3A2h	0	0	1	1	0	0	0	1	0	0	1	1	0	1	0	0	"14"
3A4h	0	0	1	1	0	0	1	1	0	0	1	1	1	0	1	0	"3:"
3A6h	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	" 3"

Interrupt Vector

Type: unsigned character
Range: 00h to FFh
Read/Write: R/W
Initialized Value: 0

This register contains the interrupt vector, or address to the interrupt service routine. There can be a delay of up to 1 sec after the Interrupt Vector register is written before it takes effect.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERRUPT VECTOR	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

MODULE MEMORY MAP – 6 CHANNEL ARINC COMMUNICATIONS (A4)

000	Tx Buffer	Ch 1	W	090	Tx Buffer	Ch 4	W	12C	RECEIVE DATA UNBUFFERED	R
004	Rx Buffer	Ch 1	R	094	Rx Buffer	Ch 4	R			
008	Rx FIFO Threshold	Ch 1	R/W	098	Rx FIFO Threshold	Ch 4	R/W	130	TX TRIGGER REG	W
00A	Tx FIFO Threshold	Ch 1	R/W	09A	Tx FIFO Threshold	Ch 4	R/W	132	TX PAUSE REG	W
00C	Rx FIFO Level	Ch 1	R	09C	Rx FIFO Level	Ch 4	R	134	TX STOP REG	W
00E	Tx FIFO Level	Ch 1	R	09E	Tx FIFO Level	Ch 4	R	136	TIMESTAMP CONTROL REG	W
010	Channel Control Low	Ch 1	R/W	0A0	Channel Control Low	Ch 4	R/W	138	TIMESTAMP HIGH REG	R
012	Channel Control High	Ch 1	R/W	0A2	Channel Control High	Ch 4	R/W	13A	TIMESTAMP LOW REG	R
014	Channel Status	Ch 1	R/W	0A4	Channel Status	Ch 4	R/W	13C	MODULE RESET	W
016	Channel Interrupt Enable	Ch 1	R/W	0A6	Channel Interrupt Enable	Ch 4	R/W			
018	Channel Interrupt Status	Ch 1	R/W	0A8	Channel Interrupt Status	Ch 4	R/W	1FE	MEMORY PAGE REG	R/W
01A	Channel Tx FIFO Rate High	Ch 1	R/W	0AA	Channel Tx FIFO Rate High	Ch 4	R/W	200	MEMORY WINDOW BOTTOM	R/W
01C	Channel Tx FIFO Rate Low	Ch 1	R/W	0AC	Channel Tx FIFO Rate Low	Ch 4	R/W	2FE	MEMORY WINDOW TOP	R/W
01E	MBOX Addr Reg	Ch 1	R/W	0AE	MBOX Addr Reg	Ch 4	R/W			
020	MBOX StatusWd	Ch 1	R	0B0	MBOX StatusWd	Ch4	R	380	BIT STATUS	R
022	MBOX DataWd	Ch 1	R	0B2	MBOX DataWd	Ch 4	R			
								390	DSP Compile Time – Begin	R
030	Tx Buffer	Ch 2	W	0C0	Tx Buffer	Ch 5	W	3A6	DSP Compile Time – End	R
034	Rx Buffer	Ch 2	R	0C4	Rx Buffer	Ch 5	R			
038	Rx FIFO Threshold	Ch 2	R/W	0C8	Rx FIFO Threshold	Ch 5	R/W	3B4	Module Design Version	R
03A	Tx FIFO Threshold	Ch2	R/W	0CA	Tx FIFO Threshold	Ch 5	R/W	3B6	Module Design Revision	R
03C	Rx FIFO Level	Ch 2	R	0CC	Rx FIFO Level	Ch 5	R	3B8	DSP Rev	R
03E	Tx FIFO Level	Ch 2	R	0CE	Tx FIFO Level	Ch 5	R	3BA	FPGA Rev	R
040	Channel Control Low	Ch 2	R/W	0D0	Channel Control Low	Ch 5	R/W	3BC	Module ID	R
042	Channel Control High	Ch 2	R/W	0D2	Channel Control High	Ch 5	R/W			
044	Channel Status	Ch 2	R/W	0D4	Channel Status	Ch 5	R/W	3C2	FPGA Int 1 Chan 1 Vector	R/W
046	Channel Interrupt Enable	Ch 2	R/W	0D6	Channel Interrupt Enable	Ch 5	R/W	3C4	FPGA Int 2 Chan 2 Vector	R/W
048	Channel Interrupt Status	Ch 2	R/W	0D8	Channel Interrupt Status	Ch 5	R/W	3C6	FPGA Int 3 Chan 3 Vector	R/W
04A	Channel Tx FIFO Rate High	Ch2	R/W	0DA	Channel Tx FIFO Rate High	Ch 5	R/W	3C8	FPGA Int 4 Chan 4 Vector	R/W
04C	Channel Tx FIFO Rate Low	Ch 2	R/W	0DC	Channel Tx FIFO Rate Low	Ch 5	R/W	3CA	FPGA Int 5 Chan 5 Vector	R/W
04E	MBOX Addr Reg	Ch 2	R/W	0DE	MBOX Addr Reg	Ch 5	R/W	3CC	FPGA Int 6 Chan 6 Vector	R/W
050	MBOX StatusWd	Ch 2	R	0E0	MBOX StatusWd	Ch 5	R			
052	MBOX DataWd	Ch 2	R	0E2	MBOX DataWd	Ch 5	R			
060	Tx Buffer	Ch 3	W	0F0	Tx Buffer	Ch 6	W			
064	Rx Buffer	Ch 3	R	0F4	Rx Buffer	Ch 6	R			
068	Rx FIFO Threshold	Ch 3	R/W	0F8	Rx FIFO Threshold	Ch 6	R/W			
06A	Tx FIFO Threshold	Ch 3	R/W	0FA	Tx FIFO Threshold	Ch 6	R/W			
06C	Rx FIFO Level	Ch 3	R	0FC	Rx FIFO Level	Ch 6	R			
06E	Tx FIFO Level	Ch 3	R	0FE	Tx FIFO Level	Ch 6	R			
070	Channel Control Low	Ch 3	R/W	100	Channel Control Low	Ch 6	R/W			
072	Channel Control High	Ch 3	R/W	102	Channel Control High	Ch 6	R/W			
074	Channel Status	Ch 3	R/W	104	Channel Status	Ch 6	R/W			
076	Channel Interrupt Enable	Ch 3	R/W	106	Channel Interrupt Enable	Ch 6	R/W			
078	Channel Interrupt Status	Ch 3	R/W	108	Channel Interrupt Status	Ch 6	R/W			
07A	Channel Tx FIFO Rate High	Ch 3	R/W	10A	Channel Tx FIFO Rate High	Ch 6	R/W			
07C	Channel Tx FIFO Rate Low	Ch 3	R/W	10C	Channel Tx FIFO Rate Low	Ch 6	R/W			
07E	MBOX Addr Reg	Ch 3	R/W	10E	MBOX Addr Reg	Ch 6	R/W			
080	MBOX StatusWd	Ch3	R	110	MBOX StatusWd	Ch 6	R			
082	MBOX DataWd	Ch 3	R	112	MBOX DataWd	Ch 6	R			

1553 COMMUNICATIONS (MODULES N7 AND N8)

This module provides 2 dual-redundant MIL-STD-1553B Notice 2 interface channels. Each channel can be configured to act as a Bus Controller (BC), Remote Terminal (RT) or Monitor (MT).

Features

- Two (2) independent MIL-STD-1553 interface channels
- Bus controller, remote terminal, or monitor operation
- 128Kbyte (64K words) on board memory per channel
- Register compatible with the SµMMIT™ family of devices from Aeroflex Inc.
- Supports automatic message return
- Automatic health monitoring

MIL-STD-1553 defines a local area network (LAN). This digital, command-response, time-division multiplexing network protocol is used in many military and commercial applications where fast, positive control is required. The standard defines the handshaking, data formats and timing requirements of the protocol as well as the electrical characteristics of the bus and the terminals' interface electronics. Words are 16 bits long and are transmitted at one megabit per second. Messages can have up to 32 words.
One terminal is designated as the bus controller; all others are remote terminals each with a specific terminal address. All transmissions are initiated by the bus controller by transmitting a command word. Encoded into the command word is a terminal address, a TR (transmit/receive) bit, a sub-address and a word count. Remote terminals monitor the bus and respond only to commands that contain its own terminal address. Remote Terminal address is either hardwire configurable and/or programmable via the front or rear panel interface connectors. The remote terminal transmits or receives the specified number of words from/to the specified sub-address. A status word that includes its terminal address is transmitted by a remote terminal before transmitting data words or to confirm reception of data words. A loop back built-In-Test will alert the host of any system problems, before they affect the data integrity. Its built-in transmitter watch-dog timeout, memory access failure, loop-back self test, and terminal address parity will set internal 1553 BIT word register. These Modules have been validated to the MIL-STD-1553 RT Validation Test Plan (VTP) by an outside recognized 1553 consultant.

As a Remote Terminal

Indexing: Bulk transfers up to 256 messages per sub-address Core can signal host via interrupt.

Buffer Ping-Pong: Using dual buffers per sub-address for data processing Core may process message while host can access secondary buffer.

Circular Buffers: Simplify software servicing during periodic or burst data transfers.
User selects circular buffer mode at start-up or as default.

Broadcast: Filter or segregate broadcast from non-broadcast commands.

Interrupts: Can Store up to 16 interrupts and the sub-address or command block that generated it in a 32-word buffer prior to servicing.

As a Bus Monitor

Message Processing: Pull messages from the bus and store information (command, status and data locations) in monitor blocks, eight-word locations in memory

Terminal Addresses: Monitor specific terminal addresses as required

As a Bus Controller

Multiple Message Processing: Chain multiple 1553 commands into major and minor frames as needed.
Message Scheduling performs periodic message transactions with multiple remote terminals.

Polling: Request status-word responses from selected RTs.
Poll to determine what action, if any, should be taken by the core.

Automatic Retry: Core supports message retry.

Module Memory Map (Length=40000h)

00000	RAM Channel 1	R/W
1FF80	Operating Mode Registers* Channel 1	R/W
20000	RAM Channel 2	R/W
3FF80	Operating Mode Registers* Channel 2	R/W

* Register assignments are based on Operational Mode. (See Actel Handbook.) and

1553 Module (Nx) Programmer's Reference Guide for detailed API function/register descriptions.

CANBUS CONTROL AREA NETWORK (MODULE P6, PA)

Principle of Operation

P6 = **CAN A/B**

PA = **CAN J1939**

CAN is a serial bus system with multi-master capabilities, that is, all CAN nodes are able to transmit data and several CAN nodes can request the bus simultaneously. The serial bus system with real time capabilities is the subject of the ISO 11898 International standard and covers the lowest two layers of the ISO/OSI reference model.

CAN is a multi-master broadcast serial bus standard for connecting Electronic Control Units (ECUs).

Each node is able to send and receive messages, but not simultaneously. A message consists primarily of an ID (identifier), which represents the priority of the message, and up to eight data bytes.

The devices that are connected by a CAN network are typically sensors, actuators, and other control devices. These devices are not connected directly to the bus, but through a host processor and a CAN controller.

If the bus is idle which is represented by recessive level (Logical 1), any node may begin to transmit. If two or more nodes begin sending messages at the same time, the message with the more dominant ID (which has more dominant bits, i.e., zeroes) will overwrite other nodes' less dominant IDs, so that eventually (after this arbitration on the ID.) only the dominant message remains and is received by all nodes. This mechanism is referred to as priority based bus arbitration. Messages with numerically smaller values of IDs have higher priority and are transmitted first.

Each node (the P6 or PA CAN module on an appropriate board/system platform provides a node) provides:

Host module processing. The host (on-module) processor decides what received messages mean and which messages it wants to transmit itself. Sensors, actuators and control devices can be connected to the host processor.

CAN controller; hardware with a synchronous clock.

> Receiving: the CAN controller stores received bits serially from the bus until an entire message is available, which can then be fetched by the host processor (usually after the CAN controller has triggered an interrupt).
>
> Sending: the host processor stores ithe transmit messages to a CAN controller, which transmits the bits serially onto the bus.

Transceiver

> Receiving: it adapts signal levels from the bus to levels that the CAN controller expects and has protective circuitry that protects the CAN controller.
>
> Transmitting: it converts the transmit-bit signal received from the CAN controller into a signal that is sent onto the bus.

Bit rates up to 1 Mbit/s are possible at network lengths below 40 m. Decreasing the bit rate allows longer network distances (e.g., 500 m at 125 kbit/s). The improved CAN (CAN FD) extends the speed of the data section by a factor of up to 8 of the arbitration bit rate.

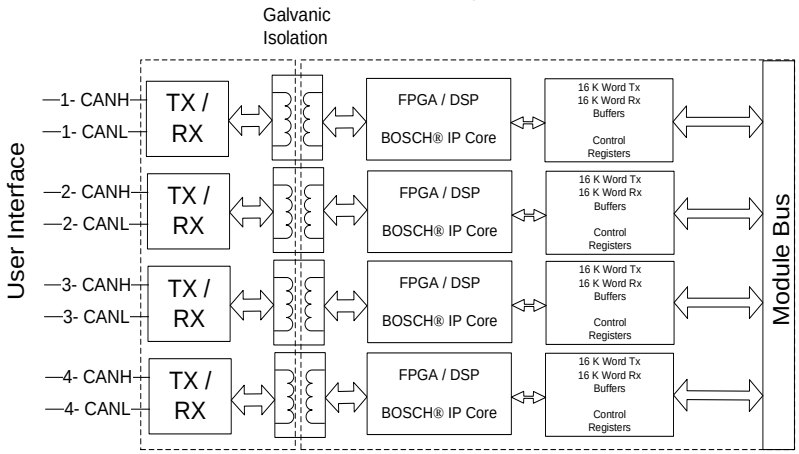
The P6 and PA provide the CAN data link layer protocol as standardized in ISO 11898-1 (2003). This standard describes mainly the data link layer (composed of the logical link control (LLC) sublayer and the media access control (MAC) sublayer) and some aspects of the physical layer of the OSI reference model. All the other protocol layers are the network designer's choice.

The P6 or PA CANBus module provides independent, isolated, channels of CAN serial data bus links, and conforms to the ISO 11898 International Standard. Both CAN A & B (P6 module) and J1939 (PA module) protocols are supported. The CAN protocol was developed by Robert Bosch GmbH and is recognized and protected by patents and licensed by Bosch.

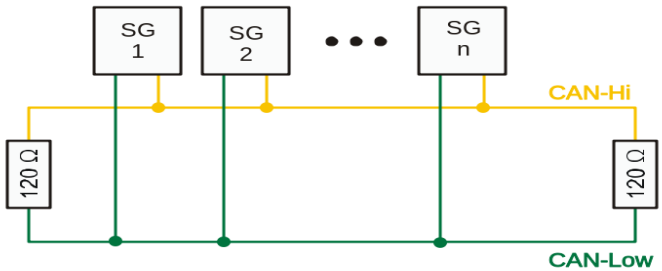
Features

- Four independent galvanically isolated channels
- Implemented with Bosch® FPGA core
- ANSI C fully Compliant Network, Transport and DataLink layers
- Addressing can be set to be Self-configurable, Non-Configurable or Command Configurable by the ECU
- **PA** module stack design conforms to the SAE J1939 protocol specification, with address claiming option
- Network layer IAW SAE section J1939/81 for self-configurable or non-configurable device (PA module)
- Transport and DataLink layers IAW SAE section J1939/21 (PA module)
- **P6** module CAN A & B supported; each channel is independently configurable
- Continuous Health Monitoring (BIT) / Error Status Registers / Self-Test Mode
- Adjustable baud rate; Speeds up to 1 Mbit/sec supported
- Sleep-mode configurable for each channel
- MilCAN compliant

CANBus IO Module Block Diagram



The P6 or PA CANBus module conforms to the standard CANBus architecture. As applications may require many nodes (SG) which are not predetermined, as such, the P6/PA channel(s) are not provided with any bus termination. Proper bus termination is dependent on the end-use application. 120 ohm resistors must be applied to each end of the CANBus – this termination is expected for proper operation and must be provided or applied externally to the P6 or PA module channel(s). (Below fig. – example of expected/proper CANBus termination).



P6 Specific CAN A/B Register Descriptions

Control Register (set per channel) (P6 – CAN A/B Only)

Flags for controlling transmit and receive activity.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Control	D	x	x	x	x	x	x	x	x	X	D	D	D	D	x	D	D=DATA BIT

D0: Enable transmit. When set to 1 : transmit any complete frames loaded into the TX FIFO. When set to 0, transmission is held off and the queued data in the FIFO held until set to 1.

D2: Enable receive. When set to 1: enables channel to receive data from CAN bus to RX FIFO.

D3: Use Acceptance Mask and Acceptance Code for Rx filtering. When set to 1: Acceptance Mask and Acceptance Code registers will be used to filter receive messages. When set to 0: all activity will be accepted.

D4: Use CAN-A/CAN-B filtering. When set to 1: the Filter Standard/Extended bit (D5) will be used to filter receive messages. When set to 0: the type of message (Standard or Extended) cannot inhibit the acceptance filtering.

D5: Filter Standard/Extended. When set to 1 (and D4 set to 1): this channel will only receive Standard Mode Messages. When set to 0(and D4 set to 1): this channel will only receive Extended Mode messages.

D15: Reset Channel. Clears receive and transmit FIFOs for the channel. If the channel is in the Bus_Off state, this reset initiates a recovery sequence. Once a recovery sequence has started, the device will wait for 129 occurrences of Bus Idle before resuming normal operations. At the end of the Bus_Off recovery cycle, the Error Management Counters will be reset.

Acceptance Mask HI (set per channel) (P6 – CAN A/B Only)

Register contains the Acceptance mask of an 11-bit identifier, or the upper 16 bits of a 29-bit identifier.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AC_MSK_HI	x	x	x	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

For CAN-A Messages (11-bit Identifiers)

D15-D13: Unused

D12-D2: The mask of an 11-bit Identifier. The MSB of the Identifier is D12.

D1-D0: Unused

For CAN-B Messages (29-bit Identifiers)

D15-D13: Unused

D12-D0: The thirteen most significant bits of a 29-bit Identifier. The MSB of the Identifier is D12.

0=The corresponding bit in the Acceptance Code Register cannot inhibit the match in the acceptance filtering.

1=The corresponding bit in the Acceptance Code Register is used for acceptance filtering.

Acceptance Mask LO (set per channel) (P6 – CAN A/B Only)

Register contains the lower 16 bits of an acceptance mask for a 29-bit identifier.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AC_MSK_LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

For CAN-A Messages (11-bit Identifiers)

D15-D0: Unused.

For CAN-B Messages (29-bit Identifiers)

D15-D0: The least significant 16 bits of a 29-bit Identifier.

0=The corresponding bit in the Acceptance Code Register cannot inhibit the match in the acceptance filtering.

1=The corresponding bit in the Acceptance Code Register is used for acceptance filtering

Acceptance Code HI (set per channel) (P6 – CAN A/B Only)

Register contains the Acceptance Code; upper 11-bits for CAN-A, upper 16 bits for CAN-B.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AC_COD_HI	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

For CAN-A Messages (11-bit code)

D15-D13: Unused

D12-D2: 11-bit code.The MSB of the code is D12.

D1-D0: Unused

For CAN-B Messages (29-bit code)

D15-D13: Unused.

D12-D0: The thirteen most significant pits of a 29-bit code. The MSB of the code is D12.

Acceptance Code LO (set per channel) (P6 – CAN A/B Only)

Register contains the lower 16 bits of a 29-bit acceptance code.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AC_COD_LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

For CAN-A Messages (11-bit Identifiers)

D15-D0: Unused.

For CAN-B Messages (29-bit Identifiers)

D15-D0: The least significant 16 bits of a 29-bit code.

FIFO Frame Components (P6 – CAN A/B Only)

When an Interface Slot is configured to receive and a message comes in, a message will be loaded into the IFx_FIFO. The message will be constructed as follows:

MSG_ID4	MSG_ID3	MSG_ID2	MSG_ID1	Data Size	Data1	...	Data8

MSG_ID4

The upper 5 bits of the Message ID.

Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MSG_ID4	1	0	D	x	x	x	x	x	x	x	x	D	D	D	D	D	D=DATA BIT

D15: Start of Message Flag. Always equals 1 because this is the beginning of a message.

D14: End of Message Flag. Always equals 0.

D13: Message Identifier type. Equals 1 if message type is Can A. Equals 0 if message is Can B.

For CAN-A Messages (11-bit Identifiers)

D13-D5: Unused.

D4-D0: Five most significant bits.

For CAN-B Messages (29-bit Identifiers)

D13-D5: Unused.

D4-D0: Five most significant bits

MSG_ID3

The lower 6 bits of an 11-bit Identifier, or the 24th through 17th bits of a 29-bit Identifier.

Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MSG_ID3	0	0	x	x	x	x	x	x	D	D	D	D	D	D	D	D	D=DATA BIT

D15: Start of Message Flag. Always equals 0.

D14: End of Message Flag. Always equals 0

For CAN-A Messages (11-bit Identifiers)

D13-D8: Unused

D7-D2: Six least significant bits

D1-D0: Unused

For CAN-B Messages (29-bit Identifiers)

D13-D8: Unused

D7-D0: The 24th through 17th bits of a 29-bit Identifier

MSG_ID2

The 16th through 9th bits of a 29-bit Identifier

Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MSG_ID2	0	0	x	x	x	x	x	x	D	D	D	D	D	D	D	D	D=DATA BIT

D15: Start of Message Flag. Always equals 0.

D14: End of Message Flag. Always equals 0.

For CAN-A Messages (11-bit Identifiers)

D13- D0 Unused, but must be present

For CAN-B Messages (29-bit Identifiers)

D13-D8: Unused

D7-D0 The 16th through 9th bits of a 29-bit Identifier

MSG_ID1

The 8th through 1st bits of a 29-bit Identifier

Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MSG_ID1	0	0	x	x	x	x	x	x	D	D	D	D	D	D	D	D	D=DATA BIT

D15: Start of Message Flag. Always equals 0

D14: End of Message Flag. Always equals 0

For CAN-A Messages (11-bit Identifiers)

D13-D0 Unused, but must be present.

For CAN-B Messages (29-bit Identifiers)

D13-D8: Unused

D7-D0: The 8th through 1st bits of a 29-bit Identifier

Data Size

Indicates the number of bytes of data in the CAN message payload.

Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data Size	0	D	x	x	x	x	x	x	x	x	x	x	D	D	D	D	D=DATA BIT

D15: Start of Message Flag. Always equals 0.

D14: End of Message Flag. Equals 1 if there is no data payload.

D13-D4: Unused

D4-D0: Size of Payload. Any number between 8 to 0. This value must equal the number of DataX entries that follow in the FIFO.

DataX

The data of the message. This field is only present if the message has data (non zero Data Size specified). This field varies in size depending on the amount of data received with a maximum size of 8 words.

Description	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Message Data	x	D	x	x	x	x	x	x	D	D	D	D	D	D	D	D	D=DATA BIT

D15: Start of Message Flag. Always equals 0.

D14: End of Message Flag. Equals 1 if this is the last byte of CAN data.

D13-D8: Unused

D7-D0: Byte of data to put in the CAN message payload

PA Specific J1939 Register Descriptions

CH X Control (PA - J1939 only)

Flags for controlling transmit and receive activity (set per channel).

Clarification: The PGN (Parameter Group Number) uniquely identifies the Parameter Group (PG) that is being transmitted in the message. Each PG (a grouping of specific parameters) has a definition that includes the assignment of each parameter within the 8-byte data field (size in bytes, location of LSB) and the transmission rate and priority of the message. The structure of a PGN permits a total of up to 8672 different parameter groups to be defined. When an ECU receives a message, it uses the PGN in the identifier to recognize the type of data that was sent in the message.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Control	D	0	0	0	0	0	0	0	0	D	D	D	D	D	D	D	D=DATA BIT

D0: Enable transmit. 1= transmit complete frames loaded into the TX FIFO.

D2: Enable receive. 1= transfer activity received from CAN bus to RX FIFO.

D3: Enable PGN filter. If set, only store received packets that match the PGN loaded into the Receive Filter registers.

D4: Enable Destination Address Filter. If set, only store received packets that match the Destination Address loaded into the Receive Filter registers.

D5: Enable Source Address Filter. If set, only store received packets that match the Source Address loaded into the Receive Filter registers.

D6: Enable Priority Filter. If set, only store received packets that match the Priority loaded into the Receive Filter registers.

D15: Reset Channel. Clears FIFOs. If the channel is in the Bus_Off state, this reset initiates a recovery sequence. Once a recovery sequence has started, the device will wait for 129 occurrences of Bus Idle before resuming normal operations. At the end of the Bus_Off recovery cycle, the Error Management Counters will be reset.

Receive Filter Ch X Priority/PGN_HI (PA - J1939 only)

The high bits of the PGN and Priority that can be used as receive filters.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PGN_HI	1	0	0	0	0	0	0	0	0	0	0	D	D	D	D	D	D=DATA BIT

D1, D0: The two most significant bits of the PGN to be used as a receive filter.

D4-D2: The CAN Priority to be used as a receive filter.

Receive Filter Ch X PGN_LO (PA - J1939 only)

The low bits of the PGN that can be used as receive filters.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PGN_LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Receive Filter Ch X Dest/Src Address (PA - J1939 only)

The Destination and Source address that can be used as receive filters.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Dest./Src. Addr.	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

D15-D8: Destination address

D7-D0: Source address

P6 (CAN A/B) or PA (J1939) Global Register Descriptions

Hardware Error Register (Global)

A flag is set if the motherboard failed to talk to the module FPGA.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
HRDW ERR	0	0	0	0	0	0	0	0	0	0	0	D	D	D	D	D	D=DATA BIT

D0: Channel 1 FPGA Status. Set if motherboard failed to communicate with channel 1 FPGA

D1: Channel 2 FPGA Status. Set if motherboard failed to communicate with channel 2 FPGA

D2: Channel 3 FPGA Status. Set if motherboard failed to communicate with channel 3 FPGA

D3: Channel 4 FPGA Status. Set if motherboard failed to communicate with channel 4 FPGA

D4: FPGA is working, but wrong FPGA file is loaded

Last Error Code for Channel X (Global)

The last error code to occur on the CANBus. The last error code to be received on this channel. Reading this register resets to 7.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Last Error	0	0	0	0	0	0	0	0	0	0	0	0	0	D	D	D	D=DATA BIT

0 = **No Error**

1 = **Stuff Error :** More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.

2 = **Form Error :** A fixed format part of a received frame has the wrong format.

3 = **AckError :** The message this D_CAN Core transmitted was not acknowledged by another node.

4 = **Bit1Error :** During the transmission of a message (with the exception of the arbitration field), the device wanted to send a *recessive* level (bit of logical value '1'), but the monitored bus value was *dominant*.

5 = **Bit0Error :** During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a *dominant* level (data or identifier bit logical value '0'), but the monitored bus value was *recessive*. During *Bus_Off* recovery this status is set each time a sequence of 11 *recessive* bits has been monitored. This enables the CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at *dominant* or continuously disturbed).

6 = **CRCError :** The CRC check sum was incorrect in the message received, the CRC received for an incoming message does not match with the calculated CRC for the received data.

7 = **NoChange :** Any read access to the Status Register re initializes the **LEC** to '7'. When the **LEC** shows the value '7', no CAN bus event was detected since the last CPU read access to the Status Register.

Comm Status for Channel X (Global)

CAN status register.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Comm. Stat.	0	0	0	0	0	0	0	D	D	D	D	D	D	0	0	0	D=DATA BIT

D8: Parity Error detected

0=No parity error detected since last read access.

1=Parity error, this bit will be reset if Status Register is read.

D7: Bus_Off Status

0=The CAN module is not Bus_Off.

1=The CAN module is in Bus_Off state.

D6: Warning Status

0=Both error counters are below the error warning limit of 96.

1=At least one of the error counters in the EML has reached the error warning limit of 96.

D5: Error Passive

0=The CAN Core is in the error active state. It normally takes part in bus communication and sends an active error flag when an error has been detected.

1=The CAN Core is in the error passive state as defined in the CAN Specification.

D4: Received a Message Successfully

0=Since this bit was last read by the CPU, no message has been successfully received.

1= Since this bit was last reset by a read access of the CPU, a message has been successfully received (independently of the result of acceptance filtering). This bit will be reset by reading the Status Register.

D3: Transmitted a Message Successfully

0=Since this bit was read by the CPU, no message has been successfully transmitted.

1= Since this bit was last reset by a read access of the CPU, a message has been successfully (error free and acknowledged by at least one other node) transmitted. This bit will be reset by reading the Status Register.

Ch X Baud / Bit Timing Register (Global)

Configuration for baud and bit sampling point. Changing baud / timing settings while a message is transmitting will cause that message to be stopped.

The bit time is divided into four segments: According to the CAN specification, the bit time is divided into four segments: The Synchronization Segment, the Propagation Time Segment, the Phase Buffer Segment 1, and the Phase Buffer Segment 2. Each segment consists of a specific, programmable number of time quanta. The length of the time quantum (tq), which is the basic time unit of the bit time, is defined by the CAN controller's system clock frequency fpclk and the Baud Rate Prescaler (BRP): tq = BRP / 8MHz.

The time The Baud Rate Prescaler and the Baud Rate Prescaler extension are used to divide down the internal 8MHz clock.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Baud / Bit Timing	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

D15 Assert new settings. Writing a 1 will cause the channel to reset and restart with the Baud / Bit timing settings in this register and the Baud Rate Prescaler register. This bit will return to 0 after the setting has taken effect.

D14:12 TSeg2: The time segment after the sample point. 0x0 to 0x7 are valid values.

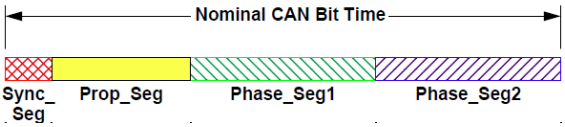
D11:8 TSeg1: The time segment before the sample point. 0x1 to 0xF are valid values.

D7:6 SJW: (Re) Synchronization Jump Width. 0x0-0x3 are valid programmed values. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

D5:0 BRP: Baud Rate Prescaler. 0x00-0x3F are valid values. The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta. Valid values for the Baud Rate Prescaler are [0 … 63]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.

The CAN bit time may be programmed in the range of [4 … 25] time quanta. The CAN time quantum may be programmed in the range of [1 … 1024] **CAN_CLK** periods. For details see Application Note 001 "Configuration of Bit Timing". The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. **TSeg1** is the sum of Prop_Seg and Phase_Seg1. **TSeg2** is Phase_Seg2. Therefore the length of the bit time is (programmed values) [**TSeg1** + **TSeg2** + 3] tq or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] tq.

Example: 1 MHz CANBus Bit Sample Time / Baud rate programming calculation(s)



Module channel(s) are based on 8 MHz clock; 125 ns is the quantum:

The bit time is defined as **Tbit = TSeg1 + TSeg2 + 3**

For programming 1 MHz data rate (1usec) we need 8 quanta, so the pre-scaler register is set to (0). The actual pre-scaler value is one more than the register value or 1:

8(quantum) = **TSeg1 + TSeg2 + 3(quantum)** or **5(quantum) = TSeg1 + TSeg2**

The Sync_Seq is defined by the specification as 1(quantum), so, to center sample the CAN bit, the center would be at 4(quantum):

4(quantum) = 1(quantum) + TSeg1 or **TSeg1 = 3(quantum).**

Therefore, for 1 MHz baud rate, the prescaler and time segment timing register bits should be set as follows:

PRESCALER = 0

TSEG1 = 3

TSEG2 = 2

Note: The sample point can be 'moved/adjusted' for system(s) known to have a long rise time or propagation delay. However, the relationship 5(quantum) = TSeg1 + TSeg2 must be maintained.

Ch X Baud Rate Prescaler Extension Reg (Global)

Configuration for baud prescaler. Writing to this register will not have any effect until D15 of Ch X Baud / Bit Timing Register is set.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Baud Prescaler	0	0	0	0	0	0	0	0	0	0	0	0	D	D	D	D	D=DATA BIT

D3:0 BRPE: Baud Rate Prescaler Extension. 0x00-0x0F are valid values. By programming BRPE the Baud Rate Prescaler can be extended to values up to 1023. The actual interpretation by the hardware is that one more than the value programmed by BRPE (MSBs) and BRP (LSBs) is used.

Ch X TX/RX Error Counter (Global)

Transmit and receive errors detected at the physical layer.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TX/RX Error Counter	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

D15 RP: Receive Error Passive

0= The Receive Error Counter is below the *error passive* level.

1= The Receive Error Counter has reached the *error passive* level as defined in the CAN Specification.

D14:D8 REC6-0: Receive Error Counter. Actual state of Receive Error Counter. Values between 0 & 127.

D7:D0 TEC7-0: Transmit Error Counter. Actual state of Transmit Error Counter. Values between 0 & 255.

Level Control (Global)

(Factory Use Only – For REFERENCE ONLY)

Put device in diagnostic mode and transmit a constant dominant. Setting a "1" will cause the drivers to pulse a dominant for at least 300 µs. The duration of the pulse is limited by the Dominant Time-Out feature of the transceiver. The spec for the time-out states Minimum:300 µs, Typical:400 µs, Maximum: 700 µs.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TX/RX Error Counter	0	0	0	0	0	0	0	0	0	0	0	0	D	D	D	D	D=DATA BIT

D1: Channel 1

D2: Channel 2

D3: Channel 3

D4: Channel 4

All transmit and receive activity is stopped in diagnostic mode. The unit stays in this mode until a "0" is written.

FIFO Frame (Global)

When an Interface Slot is configured to receive and a message comes in, a message will be loaded into the IFx_FIFO. The message will be constructed as follows:

PGN_HI	PGN_LO	Source Addr	Dest. Addr Or Priority	Data Size	Data1	...	Data250

PGN_HI (Global)

The high 9 bits of the PGN. The most significant bit is high for only PGN_HI.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PGN_HI	1	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

PGN_LO (Global)

The low 9 bits of the PGN.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PGN_LO	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

Source Address (Global)

The source address of the CAN message. This field is included for receive messages only.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Source Address	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D

Priority (Global)

The priority of the CAN message. This field is included for transmit messages only.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Priority	X	X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D=DATA BIT

Destination Address (Global)

The source address of the CAN message. Set to zero if destination address doesn't apply.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Dest. Addr.	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Data Size (Global)

The number of bytes of data in the message. Maximum value: 250. Minimum value: 0. If Data Size=0, then this is the last word of the message and D14 will be set to one. Otherwise, D14=0.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data Size	0	D	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D=DATA BIT

Data1..Data250 (Global)

The data of the message. This field is only present if the message has data. This field varies in size according to the amount of data received with a maximum size of 250 words. The last word of the message and D14 will be set to one. Otherwise, D14 = 0.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data	0	D	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D=DATA BIT

Empty (Global)

If the user reads the FIFO buffer when it is empty D13 will be set high. If more data comes in before the user has had a chance to read the first frame, the second frame will be added to the FIFO and the user can read out this and all subsequent messages all at once.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Empty	X	X	D	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Vector Address (Global)

Program the value of the vector assignment (typically a unique number/identifier) for the associated channel (used in conjunction with enabled interrupt mechanism) that the Interrupt Service Routine (ISR)) will utilize.

Register	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CHx Vector Addr.	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

MODULE (P6) CANBUS CAN A/B VME REGISTER MAP

Module Length (size) = 400h

The registers that are defined differently than a CAN module with J1939 protocol support are highlighted **bold**

000	Ch 1 Control	R/W	040	Ch 3 Control	R/W	080	Hardware Error Register	R
002	Ch 1 RX FIFO	R	042	Ch 3 RX FIFO	R	082	Interrupt Enable Register	R/W
004	Ch 1 RX FIFO Count	R	044	Ch 3 RX FIFO Count	R	092	Interrupt Status Register	R/W
006	Ch 1 RX Frame Count	R	046	Ch 3 RX Frame Count	R		(skipped)	
008	Ch 1 TX FIFO	R/W	048	Ch 3 TX FIFO	R/W	37A	Level Control Register	R/W
00A	Ch 1 TX FIFO Count	R	04A	Ch 3 TX FIFO Count	R		(skipped)	
00C	Ch 1 TX Frame Count	R	04C	Ch 3 TX Frame Count	R		(skipped)	
00E	**Ch 1 AC_MSK_HI**	R/W	04E	**Ch 3 AC_MSK_HI**	R/W		(skipped)	
010	**Ch 1 AC_MSK_LO**	R/W	050	**Ch 3 AC_MSK_LO**	R/W		(skipped)	
012	**Ch 1 AC_COD_HI**	R/W	052	**Ch 3 AC_COD_HI**	R/W		(skipped)	
014	Last Error Code for Channel 1	R	054	Last Error Code for Channel 3	R		(skipped)	
016	Comm Status for Channel 1	R	056	Comm Status for Channel 3	R		(skipped)	
018	**Ch 1 AC_COD_LO**	R/W	058	**Ch 3 AC_COD_LO**	R/W		(skipped)	
01A	Ch 1 Baud / Bit Timing Register	R/W	05A	Ch 3 Baud / Bit Timing Register	R/W		(skipped)	
01C	Ch 1 Baud Rate Prescaler Ext Reg	R/W	05C	Ch 3 Baud Rate Prescaler Ext Reg	R/W		(skipped)	
01E	Ch 1 Error Counter	R	05E	Ch 3 Error Counter	R		(skipped)	
	(skipped)			(skipped)			(skipped)	
020	Ch 2 Control	R/W	060	Ch 4 Control	R/W		(skipped)	
022	Ch 2 RX FIFO	R	062	Ch 4 RX FIFO	R		(skipped)	
024	Ch 2 RX FIFO Count	R	064	Ch 4 RX FIFO Count	R		(skipped)	
026	Ch 2 RX Frame Count	R	066	Ch 4 RX Frame Count	R		(skipped)	
028	Ch 2 TX FIFO	R/W	068	Ch 4 TX FIFO	R/W		(skipped)	
02A	Ch 2 TX FIFO Count	R	06A	Ch 4 TX FIFO Count	R		(skipped)	
02C	Ch 2 TX Frame Count	R	06C	Ch 4 TX Frame Count	R	388	Ch 1 - FPGA1 Rev	R
02E	**Ch 2 AC_MSK_HI**	R/W	06E	**Ch 4 AC_MSK_HI**	R/W	38A	Ch 2 - FPGA1 Rev	R
030	**Ch 2 AC_MSK_LO**	R/W	070	**Ch 4 AC_MSK_LO**	R/W	38C	Ch 3 - FPGA1 Rev	R
032	**Ch 2 AC_COD_HI**	R/W	072	**Ch 4 AC_COD_HI**	R/W	38E	Ch 4 - FPGA1 Rev	R
034	Last Error Code for Channel 2	R	074	Last Error Code for Channel 4	R		(skipped)	
036	Comm Status for Channel 2	R	076	Comm Status for Channel 4	R	3B4	Design Version	R
038	**Ch 2 AC_COD_LO**	R/W	078	**Ch 4 AC_COD_LO**	R/W	3B6	Design Revision	R
03A	Ch 2 Baud / Bit Timing Register	R/W	07A	Ch 4 Baud / Bit Timing Register	R/W	3B8	DSP Rev	R
03C	Ch 2 Baud Rate Prescaler Ext Reg	R/W	07C	Ch 4 Baud Rate Prescaler Ext Reg	R/W	3BA	FPGA Rev	R
03E	Ch 2 Error Counter	R	07E	Ch 4 Error Counter	R	3BC	Module ID	R
						3C2	CH1 Interrupt Vector Address	R/W
						3C4	CH2 Interrupt Vector Address	R/W
						3C6	CH3 Interrupt Vector Address	R/W
						3C8	CH4 Interrupt Vector Address	R/W

MODULE (PA) CANBUS J1939 VME REGISTER MAP

Module Length (size) = 400h (800h)

The registers that are defined differently than a CAN module with CAN A/B protocol support are highlighted **bold**

000	Ch 1 Control	R/W	040	Ch 3 Control	R/W	080	Hardware Error Register	R
002	Ch 1 RX FIFO	R	042	Ch 3 RX FIFO	R	082	Interrupt Enable Register	R/W
004	Ch 1 RX FIFO Count	R	044	Ch 3 RX FIFO Count	R	092	Interrupt Status Register	R/W
006	Ch 1 RX Frame Count	R	046	Ch 3 RX Frame Count	R		(skipped)	
008	Ch 1 TX FIFO	R/W	048	Ch 3 TX FIFO	R/W	37A	Level Control Register	R/W
00A	Ch 1 TX FIFO Count	R	04A	Ch 3 TX FIFO Count	R		(skipped)	
00C	Ch 1 TX Frame Count	R	04C	Ch 3 TX Frame Count	R		(skipped)	
00E	**Receive Filter Ch 1 Priority/ PGN-hi**	R/W	04E	**Receive Filter Ch 3 Priority/ PGN-hi**	R/W		(skipped)	
010	**Receive Filter Ch 1 PGN-lo**	R/W	050	**Receive Filter Ch 3 PGN-lo**	R/W		(skipped)	
012	**Receive Filter Ch 1 Dest/Src Address**	R/W	052	**Receive Filter Ch 3 Dest/Src Address**	R/W		(skipped)	
014	Last Error Code for Channel 1	R	054	Last Error Code for Channel 3	R		(skipped)	
016	Comm Status for Channel 1	R	056	Comm Status for Channel 3	R		(skipped)	
018	**Ch 1 Address**	R/W	058	**Ch 3 Address**	R/W		(skipped)	
01A	Ch 1 Baud / Bit Timing Register	R/W	05A	Ch 3 Baud / Bit Timing Register	R/W		(skipped)	
01C	Ch 1 Baud Rate Prescaler Ext Reg	R/W	05C	Ch 3 Baud Rate Prescaler Ext Reg	R/W		(skipped)	
01E	Ch 1 Error Counter	R	05E	Ch 3 Error Counter	R		(skipped)	
	(skipped)			(skipped)			(skipped)	
020	Ch 2 Control	R/W	060	Ch 4 Control	R/W		(skipped)	
022	Ch 2 RX FIFO	R	062	Ch 4 RX FIFO	R		(skipped)	
024	Ch 2 RX FIFO Count	R	064	Ch 4 RX FIFO Count	R		(skipped)	
026	Ch 2 RX Frame Count	R	066	Ch 4 RX Frame Count	R		(skipped)	
028	Ch 2 TX FIFO	R/W	068	Ch 4 TX FIFO	R/W		(skipped)	
02A	Ch 2 TX FIFO Count	R	06A	Ch 4 TX FIFO Count	R		(skipped)	
02C	Ch 2 TX Frame Count	R	06C	Ch 4 TX Frame Count	R	388	Ch1-FPGA1 Rev	R
02E	**Receive Filter Ch 2 Priority/ PGN-hi**	R/W	06E	**Receive Filter Ch 4 Priority/ PGN-hi**	R/W	38A	Ch2-FPGA1 Rev	R
030	**Receive Filter Ch 2 PGN-lo**	R/W	070	**Receive Filter Ch 4 PGN-lo**	R/W	38C	Ch3-FPGA1 Rev	R
032	**Receive Filter Ch 2 Dest/Src Address**	R/W	072	**Receive Filter Ch 4 Dest/Src Address**	R/W	38E	Ch4-FPGA1 Rev	R
034	Last Error Code for Channel 2	R	074	Last Error Code for Channel 4	R		(skipped)	
036	Comm Status for Channel 2	R	076	Comm Status for Channel 4	R	3B4	Design Version	R
038	Ch 2 Address	R/W	078	Ch 4 Address	R/W	3B6	Design Revision	R
03A	Ch 2 Baud / Bit Timing Register	R/W	07A	Ch 4 Baud / Bit Timing Register	R/W	3B8	DSP Rev	R
03C	Ch 2 Baud Rate Prescaler Ext Reg	R/W	07C	Ch 4 Baud Rate Prescaler Ext Reg	R/W	3BA	FPGA Rev	R
03E	Ch 2 Error Counter	R	07E	Ch 4 Error Counter	R	3BC	Module ID	R
						3C2	CH1 Interrupt Vector Address	R/W
						3C4	CH2 Interrupt Vector Address	R/W
						3C6	CH3 Interrupt Vector Address	R/W
						3C8	CH4 Interrupt Vector Address	R/W

FOUR CHANNEL, SERIAL (RS232/422/485) (MODULE P8) / ISOLATED RS-422/RS-485 (MODULE PC)

This sophisticated, 4 channel, high-speed communications module supports intelligent, full duplex communications that can be individually software configured for RS-232C (P8 only), RS-422 or RS-485 Synchronous or Asynchronous Communication (P8 or Isolated PC). The architecture avoids latency problems because all data transfer is done in hardware and not in software. Any incoming data, no matter how many channels are active, in whatever mode, can be immediately extracted. A BREAK sequence capability is also incorporated. Bus Data is transferred within 300 ns. FPGA design simplifies programming and usage.

Note: Due to pin count constraints, extended handshaking capability is not supported.

An **Internal Loop Back Self-Test** performed when power is applied, and results are stored in registers (certain platform support only). During Loop Back test, the outputs are disconnected. Each channel can be programmed into a Loop Back mode that internally wraps the transmitter around the receiver without the need of external wiring. Output short circuit capability is continuous and bullet proof. If the card is not powered, neither the inputs nor outputs will load down the lines. Inputs and outputs can withstand ±15 volts under any condition. All serial lines are transient protected to IEC1000 4-2, 4-4, & 4-5.

Serial Data Transmit Enhancement: An additional asynchronous mode to support "Immediate Transmit" operation has been incorporated. This mode immediately transmits serial data anytime the transmit buffer is not empty when the Tx Always bit (D1) is set to "1" of the *Channel Control High* register. There is no requirement to set the "TX Initiate" bit after each byte where system traffic and overhead can be simplified, since only the actual data byte being transmitted needs be sent to the transmit buffer. Each channel has its own 32 Kbyte Transmit and Receive buffer. While in Asynchronous mode, the upper byte of each received word provides status information for that word.

Receiver Enable/Disable: A Receiver Enable/Disable function allows the user to turn selected receivers ON/OFF. When a receiver is disabled, no data will be placed in the buffer. CRC code generation and detection is also available for message integrity when used in Synchronous and HDLC modes.

This serial card can operate in an **Interrupt Driven Environment** to provide notification of all events to the system. It supports hardware flow control (CTS/RTS) as well as software flow control (XON, XOFF). When a flow control mode is selected, the serial card does the operation automatically with minimal system intervention.

A Parity Error Interrupt is provided for each single byte throughout the communications data stream.

Multi-Drop Link Mode: (RS-485). The transmitter and receivers of up to 32 cards can be tied together in either Half or Full Duplex mode. While in Multi-Drop Link Mode, the transmit line for each channel can automatically change from tri-state to enabled to transmit any data as soon as it is placed in the transmit buffer (by setting the "Tristate Transmit Line" bit (D8) to "1" of the *Channel Control Low* register and when the Tx Always bit (D1) is set to "1" of the *Channel Control High* register). Once transmission is completed, the transmit line is automatically changed back to tri-state mode. Alternatively, data transmission of a pre-loaded Tx buffer can be triggered upon command using the "Tx Initiate" bit (D0) of the *Channel Control High* register. When set for RS-485 mode, the internal 120 ohm Rx termination is "disabled". When set for RS422 mode, the internal 120 ohm Rx termination is enabled.

Half-Duplex Mode: For applications requiring one transmission line pair for both Tx and Rx, channel Rx and Tx pairs must be hard-wired in parallel externally. Automatic transmitter control is invoked by setting the "Tristate Transmit Line" bit (D8) of the *Channel Control Low* register to "1"; the transmit line for each channel will automatically change from tri-state to enabled to transmit. Alternatively, data transmission of a pre-loaded Tx buffer can be triggered upon command using the "Tx Initiate" bit (D0) of the *Channel Control High* register. Since the Tx and Rx lines are tied in parallel, any transmitted characters will appear in the Rx buffer. If suppression of the echoed transmitted characters is desired, set the Rx Buffer Suppression bit "D7" of the *Tx-Rx Configuration High* register to "1" (added function **DOM 9/2013**).

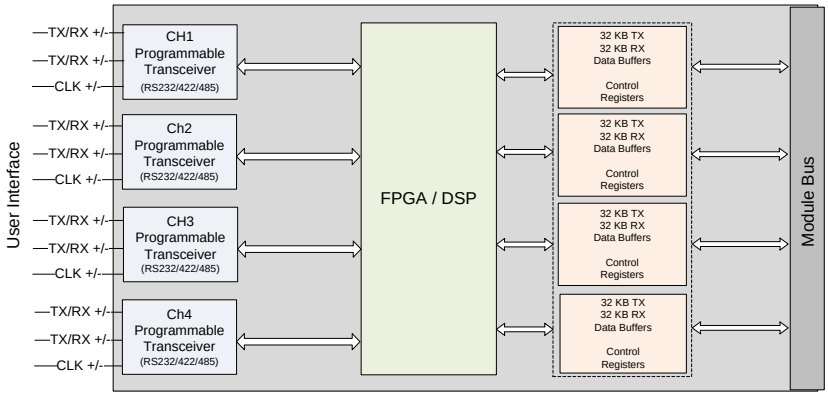
Paired Channel Flow/Control Mode: (added function DOM 6/1/10) As supported, when selected, Paired Channel Flow/Control Mode will provide up to two channels differential mode (RS-422) with CTS/RTS differential flow control or GPIO functions. This feature, when enabled, provides enhanced channel operation to the odd channels (CH1 and/or CH3) of the defined channel pair (CH1,2 and or CH3,4). When selected, CH1 and/or CH3 operation will allow differential CTS(+/-) and RTS(+/-) flow control when programmed for RS422 mode. Implementation will re-direct the CTS and RTS signal pair to the respective channel pair RXD/TXD compliment pinouts. For example, when selected, CH1 and/or CH3 CTS(+/-) will be available on the CH2 and/or CH4 RXD (+/-) outputs and CH1 and/or CH3 RTS(+/-) will be available on the CH2 and/or CH4 TXD(+/-) outputs (CH2 and/or CH4 is unused as a port).

RS422 CTS or RTS GPIO: (Added function **DOM 6/1/10**) When operating (async) in RS-422 mode, the RTS or CTS signal will be available as a general purpose differential input on the CLK (+/-) lines. If D14 is not set, “0” (default), and channel is set for RS-422 (asynchronous), CTS (+/-) will be available as an input. Alternatively, if bit D14 is set, RTS is available as a GPIO differential output on these lines.

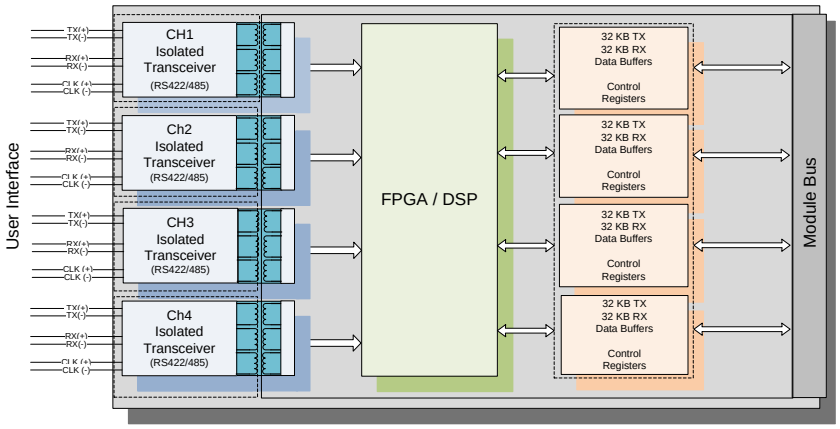
Serial Communications Specifications

Specifications	RS232 (P8 only)	RS422	RS485
Mode of Operation	Single Ended*	Differential	Differential
Total number of Drivers & Receivers on one line	1 driver, 1 receiver	1 driver, 1 receiver	1 driver, 32 receivers
Maximum Data Rate	120 kb/s	1Mb/s Asynch 4Mb/s Synch	1Mb/s Asynch 4Mb/s Synch
Driver Output Signal Level (Min Loaded)	±5V @3kΩ load	±2.0V@100Ω load	±1.5V@54Ω load
Driver Load Impedance (Ohms)	3k min	100	54
Max Driver Current in High Z State (Power On)	N/A	N/A	±100uA
Max Driver Current in High Z State (Power Off)	±6mA@±2V	±100uA	±100uA
Receiver Input Voltage Range	±15V	-10V to +10V	-7V to +12V
Receiver Input Sensitivity	±3V	±200mV	±200mV
Receiver Input Resistance (Ohms)	3k to 7k	120	10k

Note: The EIA232 standard uses negative, bipolar logic in which a negative voltage signal represents logic '1', and positive voltage represents logic '0'. RS232 active signals are provided on the (-) pin (see pinouts) (applies to P8 only).



(P8) module block diagram



(PC) module block diagram

Communication Module Factory Defaults: Registers and Delays

Address Recognition:	Off
Baud Rate:	9600
CTS/RTS:	Disabled
Protocol:	0, Asynchronous
Clock Select:	Internal
Clock Mode:	0
Interface Levels:	5
HDLC RX Address/Sync Character:	0x00A5h
HDLC TX Address/Sync Character:	0x00A5h
Termination Character:	0x0003h
Interrupt Level:	0
Interrupt Vector:	0x00
Mode:	Tri-State, asynchronous
Number of Data Bits:	8
Parity:	Disabled
Receivers:	Disabled
Number of Words TX Buffer:	0
Number of Words RX Buffer:	0
RX Buffer, Almost Full:	0x7F9Bh
Stop Bits:	1
TX Buffer, Almost Empty:	0x0064h
TX-RX Configuration High:	0
TX-RX Configuration Low:	0
Channel Control High:	0
Channel Control Low:	0
Channel Control Extended:	0
Data Configuration:	0
Preamble:	0
RX Buffer High Watermark:	0x7F9Bh
RX Buffer Low Watermark:	0x0800h
XON:	0x0011h
XOFF:	0x0013h
XON/XOFF:	Disabled
Time Out Value:	0x9C40h

A write to the following registers takes place immediately:

Transmit data
Channel control high
Transmit near empty
Receive near full
High watermark
Low watermark
Timeout timer value
Interrupt enable
Extended channel control

For all other registers, there is a 100 msec wait to become effective.

Transmit Buffer

Type: unsigned character word

Range: 00h or FFh

Read/Write: W

Initialized Value: Not Applicable

This register is the transmit data buffer. Data intended to be transmitted must be placed here prior to transmission. Data words are 8-bit and occupy the register's lowest significant bits (LSBs), or low byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TRANSMIT BUFFER	X	X	X	X	X	X	X	D[1]	D	D	D	D	D	D	D	D	X=DON'T CARE, D=DATA BIT

1. Data only in Asynchronous 9bit mode

Receive Buffer

Type: unsigned integer word.

Range: 00h or FFh (for low byte and for high byte)

Read/Write: R

Initialized Value: Not Applicable

This register is the receive data buffer. Data is received in the low byte as unsigned integer. The high byte is used for status.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RECEIVE BUFFER	S	S	S	S	S	S	S	S	D	D	D	D	D	D	D	D	S=STATUS BIT, D=DATA BIT
Asynchronous	PE	FE	OE	X	X	EOF	P	D	D	D	D	D	D	D	D	D	EOF only if Termination Char is used
Bi/Mono Synchronous	X	X	X	X	X	CRC	EOF	X	D	D	D	D	D	D	D	D	
HDLC Mode	X	BOF	X	ER2	ER1	ER0	EOF	X	D	D	D	D	X	X	D	X	Last Word is Status Word

PE	= Parity Error	'1' Calculated parity does not match the received parity bit
FE	= Framing Error	'1' A character framing error was detected.
OE	= Overrun Error	'1' A character was received while the FIFO was full
BOF	= Beginning Of Frame	'1' Indicates first character of frame Useful to identify multiple frames in large buffer
EOF	= End Of Frame	'1' Indicates End of Frame. Useful to identify multiple frames in large buffer
P	= Parity Bit	This bit carries the parity bit of the last received character
ER2.0:		HDLC Error Code:
		000 = Good Frame
		111 = CRC Error
		001 = Frame Aborted

Number of Words Tx Buffer

Type: unsigned integer word

Range: 0 to 32767

Read/Write: R

Initialized Value: 0

This register contains the number of words to be transmitted.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
NUM WORDS TX BUFFER	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Number of Words Rx Buffer

Type: unsigned integer word

Range: 0 to 32767

Read/Write: R

Initialized Value: 0

This register contains the number of words in the Rx Buffer.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
NUM WORDS RX BUFFER	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Protocol

Type: unsigned integer word

Range: not applicable

Read/Write: W

Initialized Value: 0, Asynchronous

This register is used to configure the associated channel for either asynchronous, mono-synchronous, bi-synchronous, or HDLC mode.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PROTOCOL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ASYNC
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	MONO-SYNC
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	BI-SYNC
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	HDLC

Clock Mode

Type: unsigned integer word

Range: not applicable

Read/Write: W

Initialized Value: 0

This register configures for internal (driven) or external (received) transmit/receive clocks. Applicable only for Sync or HDLC.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CLOCK MODE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Internal
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	External
	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	INVERT Tx Clock[1]
	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	INVERT Rx Clock[1]

[1]Functionality added DOM 1/1/2013 and later

Interface Levels

Type: unsigned integer word

Range: not applicable

Read/Write: W

Initialized Value: 5

This register is used to configure the interface level (RS232, RS422, RS485, Loop Back, or Tri-State) for associated channel. Loop Back selection connects the channel's transmit and receive line internally. To implement, user must send data and look at Receive FIFO to verify that the sent data. Loop Back is usually used for test.

Note 1: If bit D15 of channel 1 is raised while the system is configured for RS422 on channels 1 and 2, the RTS and CTS lines of channel 1 will become available as differential signals on the TXD/RXD lines of channel 2, and channel 2 will be otherwise unusable. The same may be done for channels 3 and 4.

Note 2: When operating (asynchronously) in RS422 mode, the CTS signal is available as a general-purpose differential input on the CLK+/- lines. Alternatively, if bit D14 is set, RTS is available as a general-purpose differential output on these lines.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERFACE LEVELS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RS232
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	RS422
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	RS485
	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	RS423[3]
	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	MANUAL LOOP BACK
	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	TRI-STATE
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Enables Paired Mode[1]
	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RS422 RTS GP OUT[2]
	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	INVERT Tx Data[3]
	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	INVERT Rx Data[3]
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	Extended CTS/RTS pin enable[4]

[3]Functionality added DOM 1/1/2013 and later. MIL-STD-188C hardware interface levels enabled by setting RS423 bit and use of Tx/Rx Data inversion as/if required

[4]Functionality clarified. D13 set to "1" will enable GEN3 platform front panel connector pin-outs (i.e. extended 44-pin front panel connector types) to support separate CTS/RTS lines (in lieu of multiplexed CTS/RTS with CLK+/-). If set to "0", RTS/CTS are multiplexed with CLK+/- (legacy and GEN2 platforms) (retro DOM 7/2012 or later).

Tx-Rx Configuration Low

Type: binary word

Range: not applicable

Read/Write: R/W

Initialized Value: 0

This register is used to set the transmit/receive configuration for the associated channel. Functions depend upon programmed protocol (see *Protocol Register*).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Tx-Rx CONFIG LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RTS/CTS FLOW CONTROL
	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	ADDRESS RECOGNITION (HDLC ONLY)
	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	ADDRESS LENGTH (HDLC ONLY) 1=16 / 0=8 BITS
	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	SYNC CHAR LENGTH 1=(8)MONO,(16)BiSync 0=(6)MONO,(12)BiSync
	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR AS DATA 1=KEPT / 0=STRIPPED
	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	TERMINATION CHAR DETECTION
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	XON/XOFF FLOW CONTROL
	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	XON/XOFF CHAR AS DATA 1=KEPT / 0=STRIPPED
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TIME OUT DETECTION

Tx-Rx Configuration High

Type: binary word

Range: not applicable

Read/Write: R/W

Initialized Value: 0

This register is used to configure CRC function and OPEN and IDLE flags. In HDLC mode, error protection is done by CRC generation and checking. The frame sequence at the end of each frame consisted of two or four bytes of CRC checksum. 32-bit or CCITT algorithms can be selected.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	CRC SELECT: HDLC: 1=32BIT CRC 0=16BIT CRC-CCITT SYNC: 1=16BIT CRC-CCITT 0=16BIT CRC
	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1=APPEND CRC TO Tx DATA, EXPECT CRC WITH Rx DATA, 0=no CRC
	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	DATA INVERSION 1=INVERTED / 0=NORMAL
	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	IDLE FLAG TRANSMISSION
	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	Rx Buffer Suppression[1]

[1]When Rx Buffer Suppression is set to “1”, the Rx buffer is disabled during transmission periods (typically applied in half-duplex transmission applications when transmitted data is preferred not to be echoed in Rx buffer) (feature added on platforms DOM 9/2013 or later; Earliest Acceptable Revision (EAR) module DSP rev. 56 / FPGA rev. 20).

Channel Control Low

Type: binary word

Range: not applicable

Read/Write: R/W

Initialized Value: 0

This register is used to for channel control configuration.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CONTROL LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	RTS/GPIO 1[1]
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	CTS/GPIO 2[1,3]
	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	TRISTATE TRANSMIT LINE [4]
	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	SET/RELEASE BREAK
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	RESET CHANNEL FIFOs & UART[2]
	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLEAR Rx FIFO[2]
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLEAR Tx FIFO[2]

Notes: 1. Disable D0 through D4 to enter GPIO control. RTS/CTS as GPIO when RTS/CTS Flow Control disabled.

2. When Reset/Clear is done after commanded, bit is set to 0.

3. Read-only

4. Tristate Transmit Line – used primarily in half-duplex, multi-drop or RS-485 type applications – when set to “1”, will automatically set the channel transmitter to high-Z state after data transmission.

Channel Control High

Type: binary word

Range: not applicable

Read/Write: R/W

Initialized Value: 0

This register is used to for channel control configuration.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CONTROL HI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	Tx INITIATE[1]
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	Tx ALWAYS (ASYNC ONLY) [2]
	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	ENABLE RECEIVER
	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	Clear Termination Char Rcvd

[1] Firmware will clear bit when all data from TX Buffer is transmitted. Use for applications desiring pre-load of TxBuffer and then command/control/trigger transmission.

[2] When Tx ALWAYS is set to “1”, transmission will occur as soon as data is placed in Tx Buffer

Channel Control Extended

Type: binary word

Range: not applicable

Read/Write: R/W

Initialized Value: 0

Write to this register to recover from a lost xon/xoff character. For example, if an incoming xon was lost for any reason, the system could “hang” waiting for a xon that was already sent. Using this bit as part of a timeout routine, setting D0 to **1** will force XON true re-establishing transmission.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CONTROL EXT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**D**	Read To determine the flow control State (1= on, 0 = off)

Data Configuration

Type: binary word

Range: not applicable

Read/Write: R/W

Initialized Value: 0

This register is used for channel data configuration.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
DATA CONFIG	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	9 DATA BITS
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8 DATA BITS
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	7 DATA BITS
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	6 DATA BITS
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	5 DATA BITS
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NO PARITY
	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	SPACE PARITY
	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	ODD PARITY
	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	EVEN PARITY
	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	MARK PARITY
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1 STOP BIT
	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	2 STOP BITS
	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	NRZ DATA ENCODING
	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	NRZI DATA ENCODING
	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	FM0 DATA ENCODING
	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	FM1 DATA ENCODING
	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	MANCHESTER DATA ENCODING

Baud Rate

Type: 24-bit unsigned integer

Range: 300 to 4Mbps Sync (1Mbps Async), Baud Rate High & Low Registers combined

Read/Write: R/W

Initialized Value: 9600 Baud

Both the *Baud Rate High Register* and *Baud Rate Low Register* combined together determine the communications baud rate. Enter desired baud rate directly as 24-bit unsigned integer.

BAUD RATE HIGH REGISTER																BAUD RATE LOW REGISTER															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Preamble

Type: binary word

Range: High word 80h, A0h, C0h, or E0h; Low word 00h to FFh

Read/Write: R/W

Initialized Value: 0

Modes Affected: HDLC, Bi-Sync

This register determines both the number of preambles and the preamble pattern sent out during preamble transmission. The high byte decodes 1, 2, 4 or 8 preambles; the low byte describes the preamble pattern. Preamble transmission applies to both the HDLC and Sync modes. In HDLC-mode, zero-bit insertion is disabled during preamble transmission. Access timing differences may cause 1-2 additional preamble characters to be sent.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PREAMBLE	1	0	0	0	0	0	0	0	D	D	D	D	D	D	D	D	1 PREAMBLE (VALUE 0xNN)
	1	0	1	0	0	0	0	0	D	D	D	D	D	D	D	D	2 PREAMBLES (VALUE 0xNN)
	1	1	0	0	0	0	0	0	D	D	D	D	D	D	D	D	4 PREAMBLES (VALUE 0xNN)
	1	1	1	0	0	0	0	0	D	D	D	D	D	D	D	D	8 PREAMBLES (VALUE 0xNN)

Tx Buffer Almost Empty

Type: unsigned integer

Range: 0 to 32767

Read/Write: R/W

Initialized Value: 100 decimal (64h)

This register specifies the minimum size, in bytes, of the transmit buffer before the TxFIFO Almost Empty Status bit D1 in the FIFO Status register is flagged (High True). If the interrupt is enabled (see Interrupt Enable register), a SYSTEM interrupt will be generated.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Tx BUFFER AE VALUE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Rx Buffer Almost Full

Type: unsigned integer

Range: 0 to 32767

Read/Write: R/W

Initialized Value: 32667 (0x7F9B)

This register specifies the maximum size, in bytes, of the receive buffer before the RxFIFO Almost Full Status bit D0 in the FIFO Status register is flagged (High True). If the interrupt is enabled (see **Interrupt Enable register)**, a SYSTEM interrupt will be generated.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Rx BUFFER AF VALUE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Rx Buffer High Watermark

Type: binary word

Range: *Low Watermark* < *High Watermark* < 32767

Read/Write: R/W

Initialized Value: 32667decimal (0x7F9B)

This register defines the *Receive Buffer High Watermark* value. When Rx Buffer size equals the High Watermark value, FIFO Status bit D3 is flagged and:

If XON/XOFF is enabled, XOFF is sent, **and/or**

If RTS/CTS is enabled, RTS goes inactive.

The Watermark registers are used for XON/XOFF and/or RTS/CTS flow control. The *Receive Buffer High Watermark* register value controls when the XOFF character is sent when using software flow control and controls when the RTS signal would be negated when using hardware flow control. For software flow control operation, the XOFF character would be sent once when the number of bytes in the RX FIFO equals the value in the *Receive Buffer High Watermark* register. Once the XOFF has been sent, it cannot be sent again until the XON character has been sent. The valid state transitions to sending the XOFF character can be either no previous XON/XOFF character sent or a previous XON character sent. There is also a *High Watermark Reached* interrupt enable/ disable bit in the Interrupt Enable Register and a *High Watermark Reached* bit in the ISR, (Interrupt Status Register). When the *High Watermark* is reached, an interrupt request will be generated, when enabled.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
HI WATERMARK VALUE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Rx Buffer Low Watermark

Type: binary word

Range: 0 < *Low Watermark* < *High Watermark* < 32767

Read/Write: R/W

Initialized Value: 2048 decimal (800h)

This register defines the *Receive Buffer Low Watermark* value. When the Rx Buffer size is less than the Low Watermark value, FIFO Status bit D3 is flagged.

If XON/XOFF is enabled, XON is sent, **and/or**

If RTS/CTS is enabled, RTS goes active

The Watermark registers are used for XON/XOFF and/or RTS/CTS flow control. The *Receive Buffer Low Watermark* register value controls when the XON character is sent when using software flow control and controls when the RTS signal would be asserted when using hardware flow control. For software flow control operation, the XON character would be sent once when the number of bytes in the Rx FIFO equals the value in the *Receive Buffer Low Watermark* register AND an XOFF character has be sent prior to this XON character. The valid state transition to sending the XON character can only be from the state of a previous XOFF character that has been sent. There is a *Low Watermark Reached* interrupt enable/disable bit in the Interrupt Enable Register and a *Low Watermark Reached* bit in the ISR, (Interrupt Status Register). When the *Low Watermark* is reached, an interrupt request will be generated, when enabled.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
LO WATERMARK VALUE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

HDLC Rx Address/Sync Character

Type: unsigned character word

Range: not applicable

Read/Write: R/W

Initialized Value: A5h

Modes Affected: HDLC and Synchronous

This register is mode dependent. If using HDLC mode, this value is compared to the address is received message and if it's equal, the message is stored in the receive buffer. If using Mono/Bi-Synchronous mode, this value is considered the "Sync Character" and is used for communication synchronization. The receiver searches incoming data for the Sync Character. Once found, communication is synchronized and additional data is valid. When in 16-bit, high byte sent before low byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
HDLC RX/SYNC CHAR	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

HDLC Tx Address/Sync Character

Type: unsigned character word

Range: not applicable

Read/Write: R/W

Initialized Value: A5h

Modes Affected: HDLC and Synchronous

This register is mode dependent. If using HDLC mode, this value is compared to the address is received message and if it's equal, the message is stored in the receive buffer. If using Mono/Bi-Synchronous mode, this value is considered the "Sync Character" and is used for communication synchronization. The receiver searches incoming data for the Sync Character. Once found, communication is synchronized and additional data is valid. When in 16 bit, high byte sent before low byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
HDLC TX/SYNC CHAR	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Termination Character

Type: unsigned character (usually a member of the ASCII data set)

Range: not applicable

Read/Write: R/W

Initialized Value: 3h

Modes Affected: Async and Sync

This register contains the termination character used for termination detection. When using the Asynchronous or Bi-Synchronous modes, the receive data stream is monitored for the occurrence of the termination character. When this character is detected, an interrupt is generated, if enabled and not masked.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TERMINATION CHAR	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

XON Character

Type: unsigned character (usually a member of the ASCII data set)

Range: not applicable

Read/Write: R/W

Initialized Value: 11h

Modes Affected: Async

This register bit field specifies the XON character for in-band flow control in Async mode.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
XON CHAR	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

XOFF Character

Type: unsigned character (usually a member of the ASCII data set)

Range: not applicable

Read/Write: R/W

Initialized Value: 13h

Modes Affected: Async

This register bit field specifies the XOFF character for in-band flow control in Async mode.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
XOFF CHAR	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

FIFO Status

Type: binary word

Range: not applicable

Read/Write: R

Initialized Value: not applicable

This register describes current FIFO Status. See Rx Almost Full, Tx Almost Empty, Rx High Watermark and Rx Low Watermark specific registers for function description and programming.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
FIFO STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	RxFIFO ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	TxFIFO ALMOST EMPTY
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	HIGH WATERMARK REACHED
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	LOW WATERMARK REACHED
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx EMPTY
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Tx FULL

Time Out Value

Type: unsigned integer

Range: 0 to 65535

Read/Write: R/W

Initialized Value: 9C40h (1 second)

Modes Affected: Async

This register bit field determines the time out period. If there is no receive line activity for the configured period of time, a time out is indicated in the Interrupt Status Register, bit D10. LSB is 25µs.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TIME OUT VALUE	D	D	D	D	D	D	D	D	D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Interrupt Enable

Type: binary word

Range: not applicable

Read/Write: R/W

Initialized Value: not applicable

This register provides for Interrupt Enabling. Set bit high True to enable interrupts. Status will still be reported in status registers. See specific registers for function description and programming

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERRUPT ENABLE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	PARITY ERROR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	Rx BUFFER ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	CRC ERROR (sync & hdlc only)
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	Rx COMPLETE / ETX RECEIVED
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Rx OVERRUN
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	HIGH WATERMARK REACHED
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	LOW WATERMARK REACHED
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	Tx BUFFER ALMOST EMPTY
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	Tx COMPLETE
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	TIME OUT OCCURRED
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	BREAK / ABORT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR DETECTED
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS HIGH Detect (rise) [1]
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS LOW Detect (fall) [1]

[1] **Note:** Added function 6/1/10; When and as selected, CTS (rise and/or fall) can be set as an interruptible condition.

Interrupt Status

Type: binary word

Range: not applicable

Read/Write: R/W

Initialized Value: not applicable

This register describes the status of 15 different events. These events are latched and unlatched when read. See specific registers for function description and programming.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERRUPT STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	PARITY ERROR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	Rx BUFFER ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	CRC ERROR (sync & hdlc only)
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	Rx COMPLETE / ETX RECEIVED
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Rx OVERRUN
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	HIGH WATERMARK REACHED
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	LOW WATERMARK REACHED
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	Tx BUFFER ALMOST EMPTY
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	Tx COMPLETE
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	TIME OUT OCCURRED
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	BREAK / ABORT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR DETECTED
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS HIGH Detect (rise) [1]
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS LOW Detect (fall) [1]

[1] **Note:** Added function 6/1/10; When and as selected, CTS (rise and/or fall) can be set as an interruptible condition.

Interrupt Vector

Type: unsigned character

Range: 00h to FFh

Read/Write: R/W

Initialized Value: 0

This register contains the interrupt vector, or address to the interrupt service routine.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERRUPT VECTOR	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Channel Status

Type: binary word

Range: not applicable

Read/Write: R/W

Initialized Value: not applicable

This register describes the status of 15 different events. These events are NOT latched. They are dynamic. Use this register to read current or real-time status. See specific registers for function description and programming.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CHANNEL STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	PARITY ERROR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	Rx BUFFER ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	CRC ERROR (sync & hdlc only)
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	Rx COMPLETE / ETX RECEIVED
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Rx OVERRUN
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	HIGH WATERMARK REACHED
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	LOW WATERMARK REACHED
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	Tx BUFFER ALMOST EMPTY
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	Tx COMPLETE
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	TIME OUT OCCURRED
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	BREAK / ABORT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR DETECTED
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS HIGH Detect (rise) 1
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS LOW Detect (fall) 1

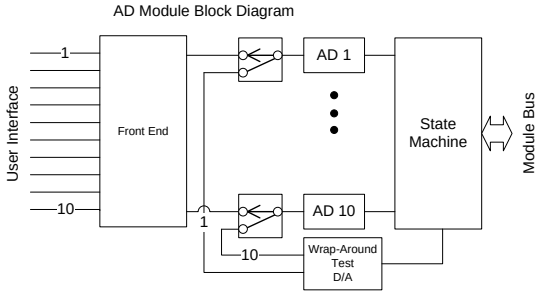
[1] **Note:** Added function 6/1/10; When and as selected, CTS (rise and/or fall) can be monitored as an event status.

FOUR CHANNEL SERIAL COMMUNICATIONS (MODULE P8/PC) VME MEMORY MAP

000	Tx Buffer	Ch. 1	W	078	Channel 4 Control Low		R/W	0FC	XON Character	Ch. 1	R/W
002	Tx Buffer	Ch. 2	W	07A	Channel 4 Control High		R/W	0FE	XON Character	Ch. 2	R/W
004	Tx Buffer	Ch. 3	W	084	Data Configuration	Ch. 1	R/W	100	XON Character	Ch. 3	R/W
006	Tx Buffer	Ch. 4	W	086	Data Configuration	Ch. 2	R/W	102	XON Character	Ch. 4	R/W
00C	Rx Buffer	Ch. 1	R	088	Data Configuration	Ch. 3	R/W	108	XOFF Character	Ch. 1	R/W
00E	Rx Buffer	Ch. 2	R	08A	Data Configuration	Ch. 4	R/W	10A	XOFF Character	Ch. 2	R/W
010	Rx Buffer	Ch. 3	R	090	Baud Rate Low	Ch. 1	R/W	10C	XOFF Character	Ch. 3	R/W
012	Rx Buffer	Ch. 4	R	092	Baud Rate High	Ch. 1	R/W	10E	XOFF Character	Ch. 4	R/W
018	Number Of Words Tx Buffer	Ch. 1	R	094	Baud Rate Low	Ch. 2	R/W	114	FIFO Flags	Ch. 1	R
01A	Number Of Words Tx Buffer	Ch. 2	R	096	Baud Rate High	Ch. 2	R/W	116	FIFO Flags	Ch. 2	R
01C	Number Of Words Tx Buffer1	Ch. 3	R	098	Baud Rate Low	Ch. 3	R/W	118	FIFO Flags	Ch. 3	R
01E	Number Of Words Tx Buffer	Ch. 4	R	09A	Baud Rate High	Ch. 3	R/W	11A	FIFO Flags	Ch. 4	R
024	Number Of Words Rx Buffer	Ch. 1	R	09C	Baud Rate Low	Ch. 4	R/W	120	Time Out Value	Ch. 1	R/W
026	Number Of Words Rx Buffer	Ch. 2	R	09E	Baud Rate High	Ch. 4	R/W	122	Time Out Value	Ch. 2	R/W
028	Number Of Words Rx Buffer	Ch. 3	R	0A8	Preamble	Ch. 1	R/W	124	Time Out Value	Ch. 3	R/W
02A	Number Of Words Rx Buffer	Ch. 4	R	0AA	Preamble	Ch. 2	R/W	126	Time Out Value	Ch. 4	R/W
030	Protocol	Ch. 1	W	0AC	Preamble	Ch. 3	R/W	144	HDLC Tx Address/Sync Char	Ch 1	R/W
032	Protocol	Ch. 2	W	0AE	Preamble	Ch. 4	R/W	146	HDLC Tx Address/Sync Char	Ch 2	R/W
034	Protocol	Ch. 3	W	0B4	Tx Buffer Almost Empty	Ch. 1	R/W	148	HDLC Tx Address/Sync Char	Ch 3	R/W
036	Protocol	Ch. 4	W	0B6	Tx Buffer Almost Empty	Ch. 2	R/W	14A	HDLC Tx Address/Sync Char	Ch 4	R/W
03C	Clock Mode	Ch. 1	W	0B8	Tx Buffer Almost Empty	Ch. 3	R/W	180	Interrupt Enable	Ch.1	R/W
03E	Clock Mode	Ch. 2	W	0BA	Tx Buffer Almost Empty	Ch. 4	R/W	182	Interrupt Enable	Ch.2	R/W
040	Clock Mode	Ch. 3	W	0C0	Rx Buffer Almost Full	Ch. 1	R/W	184	Interrupt Enable	Ch.3	R/W
042	Clock Mode	Ch. 4	W	0C2	Rx Buffer Almost Full	Ch. 2	R/W	186	Interrupt Enable	Ch.4	R/W
048	Interface Levels	Ch. 1	W	0C4	Rx Buffer Almost Full	Ch. 3	R/W	18C	Interrupt Status	Ch.1	R/W
04A	Interface Levels	Ch. 2	W	0C6	Rx Buffer Almost Full	Ch. 4	R/W	18E	Interrupt Status	Ch.2	R/W
04C	Interface Levels	Ch. 3	W	0CC	Rx Buffer High Watermark	Ch. 1	R/W	190	Interrupt Status	Ch.3	R/W
04E	Interface Levels	Ch. 4	W	0CE	Rx Buffer High Watermark	Ch. 2	R/W	192	Interrupt Status	Ch.4	R/W
054	Tx-Rx Configuration Low	Ch. 1	R/W	0D0	Rx Buffer High Watermark	Ch. 3	R/W	1A4	Channel Status 1		R
056	Tx-Rx Configuration High	Ch. 1	R/W	0D2	Rx Buffer High Watermark	Ch. 4	R/W	1A6	Channel Status 2		R
058	Tx-Rx Configuration Low	Ch. 2	R/W	0D8	Rx Buffer Low Watermark	Ch. 1	R/W	1A8	Channel Status 3		R
05A	Tx-Rx Configuration High	Ch. 2	R/W	0DA	Rx Buffer Low Watermark	Ch. 2	R/W	1AA	Channel Status 4		R
								138	Channel Control Extend Ch.1		R/W
								13A	Channel Control Extend Ch.2		R/W
								13C	Channel Control Extend Ch.3		R/W
								13E	Channel Control Extend Ch.4		R/W
05C	Tx-Rx Configuration Low	Ch. 3	R/W	0DC	Rx Buffer Low Watermark	Ch. 3	R/W	3C2	Interrupt Vector	Ch.1	R/W
05E	Tx-Rx Configuration High	Ch. 3	R/W	0DE	Rx Buffer Low Watermark	Ch. 4	R/W	3C4	Interrupt Vector	Ch.2	R/W
060	Tx-Rx Configuration Low	Ch. 4	R/W	0E4	HDLC Rx Address/Sync Char	Ch 1	R/W	3C6	Interrupt Vector	Ch.3	R/W
062	Tx-Rx Configuration High	Ch. 4	R/W	0E6	HDLC Rx Address/Sync Char	Ch 2	R/W	3C8	Interrupt Vector	Ch.4	R/W
06C	Channel 1 Control Low		R/W	0E8	HDLC Rx Address/Sync Char	Ch 3	R/W				
06E	Channel 1 Control High		R/W	0EA	HDLC Rx Address/Sync Char	Ch 4	R/W	3B4	Design Version		R
070	Channel 2 Control Low		R/W	0F0	Termination Character	Ch. 1	R/W	3B6	Design Revision		R
072	Channel 2 Control High		R/W	0F2	Termination Character	Ch. 2	R/W	3B8	DSP Version		R
074	Channel 3 Control Low		R/W	0F4	Termination Character	Ch. 3	R/W	3BA	FPGA Version		R
076	Channel 3 Control High		R/W	0F6	Termination Character	Ch. 4	R/W	3BC	Module ID		R

A/D (MODULES C1, C2, C3, C4 & CA)

Principle of Operation



Modules C1, C2 and C4 provide up to 10 differential (non-isolated) distinct individual A/D channels for a wide range of input voltages (up to 50V, bipolar). Module C3 provides 10 channels of direct current (0-25 mA FS range) measurement. Module CA combines six C2 (channels 1-6) and four C3 channels (channels 7-10). Each channel utilizes a separate 16-bit A/D converter. Sample rates are programmable (200 KHz max.) and common for all channels available on the module. Each differential channel includes a second order anti-aliasing filter and a post filter that has a digitally programmable break point that enables user to field adjust the filtering for each channel. All A/D channels are self-calibrating because each channel, on a rotating basis, is automatically calibrated to eliminate offset and gain errors. The input range and gain is field programmable for each channel. The ability to set lower voltages for Full Scale Input assures maximum resolution (does not apply to Current Measurement Module C3 which is fixed unipolar, 0-25mA FS). Module C1 provides 'open wire' status capability. Open inputs cannot be sensed for other module types because precision scaling input resistor networks are utilized. All inputs are double buffered for immediate data availability. The "Latch" feature permits the user to read all A/D channels at the same time. The module(s) now includes A/D FIFO Buffering for greater control of the incoming signal (data) for analysis and display. When initialized/triggered, the A/D buffer will accept/store the data at the same rate as the base A/D sampling rate or as a divided multiple as set in the Sample Rate Register. Programmable buffer sample thresholds can be utilized for data flow control.

Built-In Test (BIT) / Diagnostic Capability

Three different tests, one on-line (D2) and two off-line (D0, D3), can be selected:

The on-line (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 0.2% FS. Any failure triggers an Interrupt (if enabled) with the results available in BIT status register. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus. In addition, all channels are monitored for open input on Module C1.

The off-line (D3) test starts an initiated BIT test that disconnects all A/D's from the I/O and then connects them across an internal stimulus. Each channel will be checked to a test accuracy of 0.2% FS and monitored for open inputs. Test cycle is completed within 20 seconds and results can be read from the Status registers when D3 changes from "1" to "0". The test can be stopped at any time and requires no user programming and can be enabled or disabled via the bus. A/D Open Circuit monitoring is disabled during D3 testing.

An off-line (D0) test is used to check the card and interface. Write "1" to D0 of *Test enable* register to disconnect all A/D channels from the I/O and to connect them across an internal D/A. Test parameters are controlled by the user and are entered in the *D0 Test Voltage* and *D0 Test Range* registers. The outputs from the A/D channels are monitored by an internal D/A for proper conversion. External reference voltage is not required.

Data Read

Two's complement format for bipolar mode; 7FFFh=+FS, 8,000h=-FS. For unipolar mode, range is from 0h to FFFFh = FS.

Range & Polarity

Format input for range and polarity. Range is dependent upon module. Encode range using data bits D0 through D3. Program polarity using data bit D4. Enter per table. Does not apply to Current Measurement Module (C3).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RANGE & POLARITY	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**

MODULE	C4	C2	C1					
RANGE	50.0 V	40.0 V	N/A	*	**1**	**0**	**1**	**0**
	25.0 V	20.0 V	N/A	*	**1**	**0**	**0**	**1**
	12.5 V	10.0 V	10.0 V	*	**0**	**0**	**0**	**0**
	6.25 V	5.00 V	5.00 V	*	**0**	**0**	**0**	**1**
	N/A	N/A	2.50 V	*	**0**	**0**	**1**	**0**
	N/A	N/A	1.25 V	*	**0**	**0**	**1**	**1**
	N/A	N/A	N/A	*	**0**	**1**	**0**	**0**

∗ For bipolar/uni-polar selection, program D4 as "0" for unipolar and "1" for bipolar.

Filter Break Frequency

The break frequency is the 3 db point of a single pole low pass filter. Enter desired frequency for each channel between 10 Hz to 10 KHz as a 16-bit binary number. (1 Hz LSB). The break frequency must not be less than 10% of the clock rate frequency. (Example: For a clock rate frequency of 2 KHz, the Filter Break Frequency should be no less than 200 Hz). Zero disables filter.

Latch All A/Ds

Latch all A/D channels by writing "1" to D0 of Latch register. Write "0" to unlatch all channels.

D0 Test Range

Specify voltage range for A/D module under test. D0 test is performed only on A/D modules. Enter per table.

NOTE: for Current Measurement Module C3, enter up to 2.5V for 25mA FS, unipolar selection only.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A/D D0 TEST RANGE	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**

MODULE	C4	C2	C1					
RANGE	50.0 V	40.0 V	N/A	*	**1**	**0**	**1**	**0**
	25.0 V	20.0 V	N/A	*	**1**	**0**	**0**	**1**
	12.5 V	10.0 V	10.0 V	*	**0**	**0**	**0**	**0**
	6.25 V	5.00 V	5.00 V	*	**0**	**0**	**0**	**1**
	N/A	N/A	2.50 V	*	**0**	**0**	**1**	**0**
	N/A	N/A	1.25 V	*	**0**	**0**	**1**	**1**

∗ For bipolar/uni-polar selection, program D4 as "0" for unipolar and "1" for bipolar.

D0 Test Voltage

Specify voltage to be applied by D0 test to A/D module under test. D0 test is performed only on A/D modules. If using bi-polar mode, write 16-bit two's complement word (7FFFh=+FS, 8000h=-FS). If using uni-polar mode, write 16-bit binary word (range: 0 to FFFFh=FS).

Example 1: if using uni-polar mode with 10v range, enter 8000h for 5v test voltage.

Example 2: if using bi-polar mode with 10v range, enter 4000h for 5v test voltage. Enter C000h for –5v.

Calibration Interval Delay

This register sets up automatic background calibration delay between individual channels. Defaults to 30 s. Program in integer decimal format (LSB=1 second, example 30 seconds = 1Eh). May effect total time for BIT and open status registers to update. Effective 1/1/09.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Calibration Interval Delay	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

FIFO Buffer Operational Description

FIFO Buffer Data (per channel):

The available data in the FIFO buffer can be retrieved, one word at a time (16-bits), in the following memory addresses. The data is presented in two's complement format. For bipolar mode; 7FFFh=+FS, 8,000h=-FS. For unipolar mode, range is from 0h to FFFFh = FS.

Data Range: (0x0000-0xFFFF)

Words in FIFO (per channel):

This is a counter that reports the number of data in WORDS (2 byte) stored in the FIFO buffer. Every time when a read operation is made to the A/D Data memory address, its corresponding "Words in FIFO" counter will be decremented by one. The maximum number of words can be stored in the FIFO is 26,213(0x6665).

Data Range: (0x0000-0x6665)

Hi-Threshold (per channel):

The hi-threshold level is used to set or reset the high limit bit (B2) of the individual channel status register in memory location. When the "Words in FIFO" counter is greater than or equal to the value stored in the hi-threshold register, the high limit bit (B2) of the channel status register will be set. When the "Words in FIFO" counter is less than the value stored in the hi-threshold, the high limit bit (B2) of the channel status register will be reset.

Set = "logical 1"

Reset = "logical 0"

Data Range: (0x0000-0x6665)

Low-Threshold (per channel):

The low-threshold level is used to set or reset the low limit bit (B1) of the individual channel status register in memory location. When the "Words in FIFO" counter is less or equal than the value stored in the low-threshold, the low limit bit (B1) of the channel status register will be set. When the "Words in FIFO" counter is greater than or equal to the value stored in the low-threshold, the low limit bit (B1) of the channel status register will be reset.

Set = "logical 1

"Reset = "logical 0"

Data Range: (0x0000-0x6665)

Delay (per channel):

Set the number of delay samples before the actual FIFO data collection begins. The data collected during the delay period will be discarded.

Data Range: (0x0000-0xFFFF)

FIFO Size (per channel):

Sets the number of samples to be taken and placed into the FIFO when a trigger occurs. Note that the size of each sample (number of words written to the FIFO per sample) is determined by the sample format described by the *Buffer Control* register (see Buffer Control for more info). Data Range: (0x0000-0x6665)

Sample Rate (per channel):

The sample rate sets the sampling rate for the FIFO buffer. For a 200 KHz base clock the rate is based on the product of 5 μs x Sample Rate. For example, if the address (0x1C0) is set to 2, the FIFO buffer will be sampling at 5 * 2 = 10 μs.

Data Range: (0x0000-0xFFFF)

Clear FIFO (per channel):

Whenever the Clear memory is set or reset for the individual channel, it initializes the "Words in FIFO" to zero. Clear FIFO does not clear data in the buffer. A read to the buffer data will give "aged" data.

Data Range: (0x0000-0xFFFF)

Buffer Control (per channel):

Sets the format of the samples to be stored in the FIFO buffer. The following bit map defines the type/format of data that will be put into the FIFO buffer.

B0 = Data (16-bit Hi). 16-bit resolution data for unipolar and bipolar.

B1 = Data (8 Bit Lo). Combine with B0 to form a 24-bit resolution for unipolar and bipolar data.

B2 = Data Type. 0 = Raw (unfiltered); 1 = Filtered.

B3 = Reserved

B4 = Time Stamp. An integer counter that counts from 0 to 65,535 and wraps around when it overflows.

B5 = Reserved

B6 = Reserved

B7 = Reserved

Note: Each data format (B0 – B4) requires one word of storage space from the FIFO buffer. For example, if B0, B1 and B4 are set (0x13) and the Size register is set to 1, a FIFO write will put 3 words of data to the FIFO memory space per sample. Since the maximum physical size of FIFO is 26,213 for each channel, the value in the Size and Buffer Control register could cause an overflow to the FIFO buffer. When an overflow condition occurs, any un-stored data will be lost.

Set the bits for Buffer Control

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Buffer Control	X	X	X	X	X	X	X	X	X	X	X	**B4**	**B3**	**B2**	**B1**	**B0**

Description	Buffer Ctrl.(16-bit hex)
Buf. Ctrl. in ch1-10	Data Range: B0-B4

Trigger Control (per channel):

The FIFO can be started/triggered by different sources.

B0-B1 = Source Select (Choose one only

0x0 = Ext. Trigger 2

0x1 = Ext. Trigger 1

0x2 = Software Trigger

B3 = Reserved

B4-B7 = Trigger Type (Choose one only)

0x10 = Negative Slope

0x20 = Trigger Pulse Enable

0x40 = Trigger Pulse/Trigger Enable Select

0x80 = Trigger Clear

Data Range: B0-B7

Register Write	Trig Source	Slope
0x20	Ext Trigger 2	Positive
0x21	Ext Trigger 1	Positive
0x22	SW Trigger	Positive (Don't care)
0x30	Ext Trigger 2	Negative
0x31	Ext Trigger 1	Negative
0x32	SW Trigger	Negative (Don't care)
0x40	Initiate	
0x80	Stop (Clear Trigger)	

FIFO Status (per channel):

The FIFO status register indicates the current condition of the FIFO buffer. B0-B4 is used to show the different conditions of the buffer (Register latched; read until clear).

B0 = Empty. When "Words in FIFO" register is zero, B0 = 1; otherwise B0 =0.

B1 = Low Limit. When "Words in FIFO" register ≤ "Low-Threshold", B1= 1; otherwise B1 =0.

B2 = High Limit. When "Words in FIFO" register ≥ "Hi-Threshold", B2=1; otherwise B2 =0.

B3 = FIFO Full. When "Words in FIFO" register = "26,213", B3=1; otherwise B3 =0.

B4 = Sample Done. When "Words in FIFO" register = "Size", B4=1; otherwise B4 =0.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FIFO Status	X	X	X	X	X	X	X	X	X	X	X	**B4**	**B3**	**B2**	**B1**	**B0**

Description FIFO Status (16-bit hex)

FIFO Status CH1-10 Data Range: B0-B4

Interrupt Enable (per channel):

Interrupt(s) may be enabled based on the following:

B0 = Empty. When "Words in FIFO" register is zero, B0 = 1; otherwise B0 =0.

B1 = Low Limit. When "Words in FIFO" register ≤ "Low-Threshold", B1= 1; otherwise B1 =0.

B2 = High Limit. When "Words in FIFO" register ≥ "Hi-Threshold", B2=1; otherwise B2 =0.

B3 = FIFO Full. When "Words in FIFO" register = "26,213", B3=1; otherwise B3 =0.

B4 = Sample Done. When "Words in FIFO" register = "Size", B4=1; otherwise B4 =0.

Note: If an interrupt is enabled utilizing the low and high limit thresholds, the interrupt will not be "reset" or generate a new interrupt until the opposite threshold has been crossed (hysteresis). For example, if an interrupt enable is set for High Limit Threshold, once set, a new High Limit Threshold interrupt will not be generated until the Low Limit Threshold has been crossed (to reset) and then the High Limit Threshold is crossed (set).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	**B4**	**B3**	**B2**	**B1**	**B0**

Description Interrupt Enable(16-bit hex)

Interrupt Enable CH1-10 Data Range: B0-B4

Software Trigger (per channel):

Software trigger is used to kick start the FIFO buffer and the collection of data. In order to use this operation, the "Trigger Ctrl" register must be set up properly. Setting or resetting the "Software Trigger" will start FIFO data collection for ALL channels.

Description	Software Trigger (16-bit hex)
Software Trigger	Data Range: 0x0-0xFFFF

Clock Rate Input

(Setting the BASE sample rate clock)

Utilize the Clock Rate Input Registers to set the actual or Base Sample Rate of the A/D (LSB of Clock Rate Input LO = 1 Hz). (32-bit word total)

For example, setting a Base Sample Rate of 44100 Hz would be set by initializing the Clock Rate Input HI and LO registers as such:

44100 = AC44(h);

REG (Hi) = 0000

REG (Lo) = AC44(h)

Setting a Base Sample Rate at the maximum 200 KHz would be set by initializing the Clock Rate Input HI and LO registers as such:

200000 = 30D40(h)

REG (Hi) = 0003(h)

REG (Lo) = 0D40(h)

Clock Rate Input Hi:

Description	Software Trigger (16-bit hex)
Clk Rate Adder Input Hi	Data Range: 0x0-0xFFFF

Clock Rate Adder Low:

Description	Software Trigger (16-bit hex)
Clk Rate Adder Input Low	Data Range: 0x0-0xFFFF

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
CLK Rate Input (HI)	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
CLK Rate Input (LO)	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	LSB=1Hz=DATA BIT=D

NOTE: Base Sample Rate Range (combined 32-bit word) 2000 to 200,000.

Test Enable

Set bit to enable associated Built-In Self Test D3, D2, or D0.

Write “1” to D2 to initiate automatic background BIT testing. Card will (every 1 second) write 55h at *Test (D2) verifiy* register when D2 is enabled. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 1 second, to verify that background bit testing is activated. D3 test cycle is completed within 20 seconds (depending on sample rate) and results can be read from the associated status registers when D3 changes from “1” to “0”. Any failure triggers an Interrupt (if enabled). All testing requires no external programming and is initiated by writing “1” or terminated by writing “0”.

The (D2) Test initiates automatic background BIT testing. Each channel is checked every 10% from +FS to -FS to a testing accuracy of 0.2% FS and each Signal and Reference is always monitored. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled.

The (D3) Test initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests each channel to a test accuracy of 0.2% FS. Results can be read from registers and external reference is not required. Any failure triggers an Interrupt (if enabled). The testing requires no external programming, and can be initiated or stopped.

The (D0) Test is used to check the card and the interface. All channels are disconnected from the outside world, allowing the user to write any angle to all channels on the card and then to read the data from the interface. External reference is not required.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0

Test (D2) Verify

Card will write 55h at *Test (D2) Verification* register when (D2) is enabled (maximum one second). User can clear to 00h and then read again, after approximately one second, to verify that background bit testing is activated.

Active Channels

Set the bit corresponding to each channel to be monitored during BIT and Open Status (C1 Module only) testing in the *Active Channel* register. Set bit to “1” for active channels and clear bit to “0” for those not used. **Note:** Omitting this step will produce false alarms, because unused channels will set faults.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Active Channels	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status

Check the corresponding bit for a channel’s BIT Status. A “0” =Normal; “1” = Non-compliant A/D conversion (outside 0.2% FS accuracy spec). Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status

Check for an open or disconnect to the A/D input. Status of each channel is indicated at its corresponding bit. A "0" =Normal and "1" = Open. An open or disconnect to the input of an A/D channel is detected within 10 seconds and will latch the corresponding bit in the *Open Status* register. Reading any status bit will unlatch the entire register. Open Status is part of background testing and the status register may be checked or polled at any given time. NOTE: Open Status capabilities apply only to Module C1.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Open Status. Open Status applies only to Module C1.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Interrupt Vector

When a BIT Interrupt is enabled and occurs, the contents of *BIT Interrupt Vector register* is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT Interrupt Vector	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Open Interrupt Vector

When an Open Interrupt is enabled and occurs, the contents of *Open Interrupt Vector register* is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Open Interrupt Vector	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

FIFO Buffer Interrupt Vector

When a FIFO Buffer Interrupt is enabled and occurs, the contents of *FIFO Buffer Interrupt Vector register* is the value that is reported to the user (per channel).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
FIFO Buffer Interrupt Vector	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding “latching” – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are “latching”; as defined, any noted transitional change on any channel will “latch” the entire Status Register.
- Once latched, there will be no further state change “sensed” by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will “unlatch” that particular status register (doesn’t necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will “latch” the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read “until cleared”.

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- Power-up
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern (“loop to clear”) - this would also be similar to an Interrupt Service Routine (ISR) “loop to clear” function.

    Ex: Running the ‘loop to clear’ on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are “cleared” and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- Interrupt Software Routine (ISR)

  The ISR is typically a software (SW) handling branch (part of host application software) structured to “loop to read and clear” the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should “read” the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were “latched” – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively “re-arm” for the next transition to occur.

  Ex: The ISR should have the ‘loop to clear’ – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also “latch” the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

A/D (MODULES C1, C2, C3, C4, & CA) VME MEMORY MAP

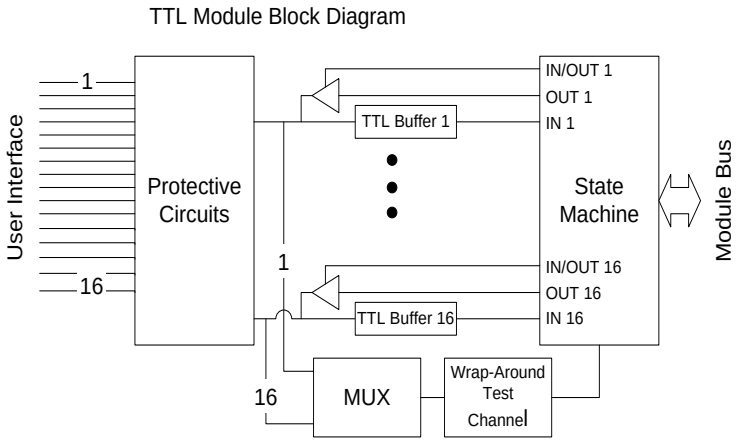
000	Data Read 1	R	14E	CH8 FIFO Buffer Hi-Threshold	R/W	20E	CH8 FIFO Buffer Control	R/W
002	Data Read 2	R	150	CH9 FIFO Buffer Hi-Threshold	R/W	210	CH9 FIFO Buffer Control	R/W
004	Data Read 3	R	152	CH10 FIFO Buffer Hi-Threshold	R/W	212	CH10 FIFO Buffer Control	R/W
006	Data Read 4	R						
008	Data Read 5	R	160	CH1 FIFO Buffer Lo-Threshold	R/W	220	CH1 FIFO Trig Control R/W	R/W
00A	Data Read 6	R	162	CH2 FIFO Buffer Lo-Threshold	R/W	222	CH2 FIFO Trig Control R/W	R/W
00C	Data Read 7	R	164	CH3 FIFO Buffer Lo-Threshold	R/W	224	CH3 FIFO Trig Control R/W	R/W
00E	Data Read 8	R	166	CH4 FIFO Buffer Lo-Threshold	R/W	226	CH4 FIFO Trig Control R/W	R/W
010	Data Read 9	R	168	CH5 FIFO Buffer Lo-Threshold	R/W	228	CH5 FIFO Trig Control R/W	R/W
012	Data Read 10	R	16A	CH6 FIFO Buffer Lo-Threshold	R/W	22A	CH6 FIFO Trig Control R/W	R/W
			16C	CH7 FIFO Buffer Lo-Threshold	R/W	22C	CH7 FIFO Trig Control R/W	R/W
016	Range & Polarity 2	R/W	16E	CH8 FIFO Buffer Lo-Threshold	R/W	230	CH9 FIFO Trig Control R/W	R/W
018	Range & Polarity 3	R/W	170	CH9 FIFO Buffer Lo-Threshold	R/W	232	CH10 FIFO Trig Control R/W	R/W
01A	Range & Polarity 4	R/W	172	CH10 FIFO Buffer Lo-Threshold	R/W			
01C	Range & Polarity 5	R/W				240	CH1 FIFO Status	R
01E	Range & Polarity 6	R/W	180	CH1 FIFO Buffer Delay	R/W	242	CH2 FIFO Status	R
020	Range & Polarity 7	R/W	182	CH2 FIFO Buffer Delay	R/W	244	CH3 FIFO Status	R
022	Range & Polarity 8	R/W	184	CH3 FIFO Buffer Delay	R/W	246	CH4 FIFO Status	R
024	Range & Polarity 9	R/W	186	CH4 FIFO Buffer Delay	R/W	248	CH5 FIFO Status	R
026	Range & Polarity 10	R/W	188	CH5 FIFO Buffer Delay	R/W	24A	CH6 FIFO Status	R
			18A	CH6 FIFO Buffer Delay	R/W	24C	CH7 FIFO Status	R
028	Filter Break Freq 1	R/W	18C	CH7 FIFO Buffer Delay	R/W	24E	CH8 FIFO Status	R
02A	Filter Break Freq 2	R/W	18E	CH8 FIFO Buffer Delay	R/W	250	CH9 FIFO Status	R
02C	Filter Break Freq 3	R/W	190	CH9 FIFO Buffer Delay	R/W	252	CH10 FIFO Status	R
02E	Filter Break Freq 4	R/W	192	CH10 FIFO Buffer Delay	R/W			
030	Filter Break Freq 5	R/W				260	CH1 FIFO Interrupt Enable	R/W
032	Filter Break Freq 6	R/W	1A0	CH1 FIFO Size	R/W	262	CH2 FIFO Interrupt Enable	R/W
034	Filter Break Freq 7	R/W	1A2	CH2 FIFO Size	R/W	264	CH3 FIFO Interrupt Enable	R/W
036	Filter Break Freq 8	R/W	1A4	CH3 FIFO Size	R/W	266	CH4 FIFO Interrupt Enable	R/W
038	Filter Break Freq 9	R/W	1A6	CH4 FIFO Size	R/W	268	CH5 FIFO Interrupt Enable	R/W
03A	Filter Break Freq 10	R/W	1A8	CH5 FIFO Size	R/W	26A	CH6 FIFO Interrupt Enable	R/W
			1AA	CH6 FIFO Size	R/W	26C	CH7 FIFO Interrupt Enable	R/W
0F0	Latch all A/D	R/W	1AC	CH7 FIFO Size	R/W	26E	CH8 FIFO Interrupt Enable	R/W
0F2	D0 Test Range	R/W	1AE	CH8 FIFO Size	R/W	270	CH9 FIFO Interrupt Enable	R/W
0F4	D0 Test Voltage	R/W	1B0	CH9 FIFO Size	R/W	272	CH10 FIFO Interrupt Enable	R/W
0F6	Calibration Interval Delay	R/W	1B2	CH10 FIFO Size	R/W			
100	CH1 FIFO Buffer Data	R	1C0	CH1 FIFO Buffer Sample Rate	R/W	280	Software Trigger	R/W
102	CH2 FIFO Buffer Data	R	1C2	CH2 FIFO Buffer Sample Rate	R/W	282	Clk Rate Adder Input Hi	R/W
104	CH3 FIFO Buffer Data	R	1C4	CH3 FIFO Buffer Sample Rate	R/W	284	Clk Rate Adder Input Lo	R/W
106	CH4 FIFO Buffer Data	R	1C6	CH4 FIFO Buffer Sample Rate	R/W	28A	Active Channels	R/W
108	CH5 FIFO Buffer Data	R	1C8	CH5 FIFO Buffer Sample Rate	R/W	37C	Test Enable	R/W
10A	CH6 FIFO Buffer Data	R	1CA	CH6 FIFO Buffer Sample Rate	R/W	37E	Test (D2) verify	R/W
10C	CH7 FIFO Buffer Data	R	1CC	CH7 FIFO Buffer Sample Rate	R/W	380	BIT Status CH.1-10	R
10E	CH8 FIFO Buffer Data	R	1CE	CH8 FIFO Buffer Sample Rate	R/W	382	Open Status CH.1-10	R
110	CH9 FIFO Buffer Data	R	1D0	CH9 FIFO Buffer Sample Rate	R/W	384	BIT Stat Int Enbl CH.1-10	R
112	CH10 FIFO Buffer Data	R	1D2	CH10 FIFO Buffer Sample Rate	R/W	386	Open Stat Int Enbl CH.1-10	R
						3E0	BIT Interrupt Vector	R/W
120	CH1 FIFO Buffer Words	R	1E0	CH1 Clear FIFO	R/W	3E2	Open Interrupt Vector	R/W
122	CH2 FIFO Buffer Words	R	1E2	CH2 Clear FIFO	R/W			
124	CH3 FIFO Buffer Words	R	1E4	CH3 Clear FIFO	R/W	3C2	CH1 FIFO Interrupt Vector	R/W
126	CH4 FIFO Buffer Words	R	1E6	CH4 Clear FIFO	R/W	3C4	CH2 FIFO Interrupt Vector	R/W
128	CH5 FIFO Buffer Words	R	1E8	CH5 Clear FIFO	R/W	3C6	CH3 FIFO Interrupt Vector	R/W
12A	CH6 FIFO Buffer Words	R	1EA	CH6 Clear FIFO	R/W	3C8	CH4 FIFO Interrupt Vector	R/W

12C	CH7 FIFO Buffer Words	R	1EC	CH7 Clear FIFO	R/W	3CA	CH5 FIFO Interrupt Vector	R/W
12E	CH8 FIFO Buffer Words	R	1EE	CH8 Clear FIFO	R/W	3CC	CH6 FIFO Interrupt Vector	R/W
130	CH9 FIFO Buffer Words	R	1F0	CH9 Clear FIFO	R/W	3CE	CH7 FIFO Interrupt Vector	R/W
132	CH10 FIFO Buffer Words	R	1F2	CH10 Clear FIFO	R/W	3D0	CH8 FIFO Interrupt Vector	R/W
						3D2	CH9 FIFO Interrupt Vector	R/W
140	CH1 FIFO Buffer Hi-Threshold	R/W	200	CH1 FIFO Buffer Control	R/W	3D4	CH10 FIFO Interrupt Vector	R/W
142	CH2 FIFO Buffer Hi-Threshold	R/W	202	CH2 FIFO Buffer Control	R/W			
144	CH3 FIFO Buffer Hi-Threshold	R/W	204	CH3 FIFO Buffer Control	R/W	3B4	Module Design Version	R
146	CH4 FIFO Buffer Hi-Threshold	R/W	206	CH4 FIFO Buffer Control	R/W	3B6	Module Design Revision	R
148	CH5 FIFO Buffer Hi-Threshold	R/W	208	CH5 FIFO Buffer Control	R/W	3B8	Module DSP	R
14A	CH6 FIFO Buffer Hi-Threshold	R/W	20A	CH6 FIFO Buffer Control	R/W	3BA	Module FPGA	R
14C	CH7 FIFO Buffer Hi-Threshold	R/W	20C	CH7 FIFO Buffer Control	R/W	3BC	Module ID	R

I/O DIGITAL TTL/CMOS (MODULE D7)

Principle of Operation

This module provides (up to) 16 individual Digital TTL/CMOS I/O channels (depending on platform and I/O connector pin availability), which are programmable for either Input or Output, and include extensive diagnostics. Interrupt(s) can be selected, for each channel, to indicate transition on rising edge, transition on falling edge, or both. De-bounce circuits for each channel offer a selectable time delay to eliminate false signals resulting from contact bounce commonly experienced with mechanical relays and switches. Each TTL/CMOS channel has an internal 100KΩ pull-down resistor. All inputs are continually scanned and the data is double buffered for immediate availability.



Automatic Background Built-In Test (BIT)/Diagnostic Capability

The module contains automatic background BIT testing that verifies channel processing (data read or write logic), tests for over-current conditions and provides status for threshold signal transitioning. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus (see further details in register description), and continually checks that each channel is functional. This capability is accomplished by an additional test comparator that is incorporated into each 16-channel module. The test comparator is sequentially connected across each channel and is compared against the operational channel. Depending upon the configuration, the Input data read or Output logic written of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low-to-High and High-to-Low logic transitions are indicated. Additional testing of output logic indicates Over-current condition when output logic is invalid for a period greater than 80µs.

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16-bit binary word. Each bit corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Read Input or Output

Independent of channel configuration (Input or Output), read logic state High ("1") or Low ("0") as defined by channel threshold values. Each bit of 16-bit binary word corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

External VCC Select

A user provided VCC may be applied to Channel banks (bank defined as 4 channels per bank) for applications requiring output voltages other than the default 3.3 VCC. External VCC must be within the range -0.3V to +5.3V with a maximum current source of 30 mA. Set the respective bit to "1" for External VCC. Default is 0x0000=Internal VCC.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
													4	3	2	1	Bank
													12-16	**9-12**	**5-8**	**1-4**	Channel
READ I/O	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**D**	**D**	**D**	**D**	D=DATA BIT

De-bounce Time

De-bounce time can be utilized when channel is selected as an input to "filter" or "ignore" spurious initial transitions. Enter required de-bounce time into appropriate channel registers. LSB weight determined from *Debounce LSB register.* Once a signal level is a logic voltage level period longer than the De-bounce time (Logic High > 2.0 v, and Logic Low < 0.8 v), a logic transition is validated. Signal pulse widths less than De-bounce time are filtered. Once valid, the transition status register flag is set for the channel and the output logic changes state. Enter a value of 0 to disable De-bounce filtering. De-bounce defaults to 00h upon reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
DE-BOUNCE TIME	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT LSB=Programmable

De-bounce LSB

De-bounce resolution= 160 ns x 2 (de-bounce LSB value)

This results in a minimum resolution of 160 ns (Debounce LSB=0) and a maximum resolution of 5.24 ms (De-bounce LSB=15).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
DE-BOUNCE LSB	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output Format

Configure channels in groups of 8. Write integer 0 for input, 3 for output: Default is configured for Input.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
INPUT/OUTPUT CH 09-16	Ch.16		Ch.15		Ch.14		Ch.13		Ch.12		Ch.11		Ch.10		Ch.09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT

Integer	D_H	D_L	
0	**0**	**0**	Input
3	**1**	**1**	Output

Reset Over-Current

Write integer "1" to reset all sixteen channels (per module), which is used to reset disabled channel(s) following an over-current condition. When reset process is complete, processor will write a "0" back to the *Reset Over-Current* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESET OVER-CURRENT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	D=DATA BIT

Status Indications

The following status conditions can be monitored (latching registers):
Fault: When a fault is detected, it will be indicated within 10 ms. A fault is latched until read.
Lo-Hi Transition: If a Lo to High transition is sensed, status is indicated (bit is set) within 100 ns.
Hi-Low Transition: If a High to Low transition is sensed, status is indicated (bit is set) within 100 ns.
Over-current: If over-current or overload condition is sensed, status is indicated (bit is set) within 10 ms. Output is, however, immediately disabled at time of over-current condition. When status is "indicated," or bit is "set," bit value is logic "1." Reading will unlatch Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Interrupt Vectors

The Interrupt Vector Registers store the vectors for the specific interrupts generated by the module. When an Interrupt is enabled and occurs, the contents of corresponding Interrupt Vector register is the value that is reported to the user:

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Interrupt Vector Lo-Hi Transition	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT
Interrupt Vector Hi-Lo Transition	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT
Interrupt Vector BIT	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT
Interrupt Vector Over-current	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding "latching" – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are "latching"; as defined, any noted transitional change on any channel will "latch" the entire Status Register.
- Once latched, there will be no further state change "sensed" by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will "unlatch" that particular status register (doesn't necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will "latch" the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read "until cleared".

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern ("loop to clear") - this would also be similar to an Interrupt Service Routine (ISR) "loop to clear" function.

    Ex: Running the 'loop to clear' on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are "cleared" and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

  The ISR is typically a software (SW) handling branch (part of host application software) structured to "loop to read and clear" the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should "read" the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were "latched" – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively "re-arm" for the next transition to occur.

  Ex: The ISR should have the 'loop to clear' – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

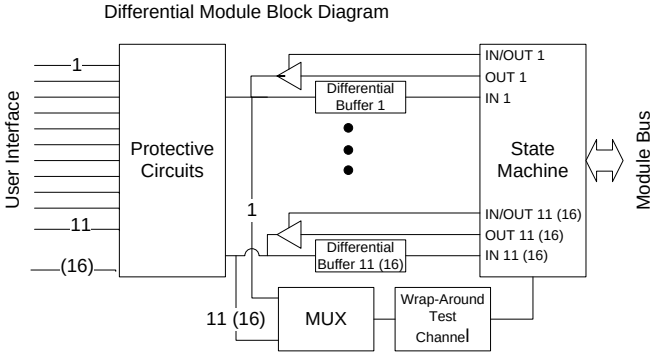
- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also "latch" the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

I/O DIGITAL TTL/CMOS (MODULE D7) VME MEMORY MAP

000	Write Output,	Ch.1-16	R/W	07A	Debounce time	Ch.12	R/W	0E8	Interrupt Fault Enable	Ch.1-16	R/W
002	Read I/O,	Ch.1-16	R	084	Debounce time	Ch.13	R/W	0EC	Interrupt Over-Current Enable	Ch.1-16	R/W
				08E	Debounce time	Ch.14	R/W	0F4	Interrupt Lo-Hi Transition Enable	Ch.1-16	R/W
00C	Debounce time	Ch.1	R/W	098	Debounce time	Ch.15	R/W	0F6	Interrupt Hi-Lo Transition Enable	Ch.1-16	R/W
016	Debounce time	Ch.2	R/W	0A2	Debounce time	Ch.16	R/W				
020	Debounce time	Ch.3	R/W	0A4	Input/Output Format	Ch.01-8	R/W	3B4	Module Design Version		R
02A	Debounce time	Ch.4	R/W	0A6	Input/Output Format	Ch.9-16	R/W	3B6	Module Design Revision		R
034	Debounce time	Ch.5	R/W	0B8	External VCC Select	Bank 1-4	R/W	3B8	Module DSP		R
03E	Debounce time	Ch.6	R/W	0BA	Debounce LSB	Ch.1-16	R/W	3BA	Module FPGA		R
048	Debounce time	Ch.7	R/W	0BC	Reset Over-Current	Ch.1-16	R/W	3BC	Module ID		R
052	Debounce time	Ch.8	R/W	0D0	Status Fault	Ch.1-16	R	3C4	Interrupt Vector Lo-Hi Transition		R/W
05C	Debounce time	Ch.9	R/W	0D4	Status Over-Current	Ch.1-16	R	3C6	Interrupt Vector Hi-Lo Transition		R/W
066	Debounce time	Ch.10	R/W	0DC	Status Lo-Hi Transition	Ch.1-16	R	3E0	Interrupt Vector Bit		R/W
070	Debounce time	Ch.11	R/W	0DE	Status Hi-Lo Transition	Ch.1-16	R	3E2	Interrupt Vector Over-current		R/W

DIFFERENTIAL MULTI-MODE TRANSCEIVERS (MODULE D8)

Principle of Operation



This module provides 11 (or 16 with platforms utilizing 44-pin front panel connectors) individual Differential RS422/RS485 I/O channels that are programmable, per channel, for either Input or Output, and include extensive diagnostics. Each Differential input channel has a selectable internal termination resistor (120Ω or >96kΩ) across its inputs. Interrupt can be selected, for each channel, to indicate transition on rising edge, transition on falling edge, or both. De-bounce circuits for each channel offer a selectable time delay to eliminate false signals resulting from contact bounce commonly experienced with mechanical relays and switches. All inputs are continually scanned and the data is double buffered for immediate availability.

Automatic Background Built-In Test (BIT) / Diagnostic capability

The module contains automatic background BIT testing that verifies channel processing (data read or write logic), tests for over-current conditions and fault status. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus (See further details in register description), and continually checks that each channel is functional. This capability is accomplished by an additional test comparator that is incorporated into each 11 (16) channel modules. The test comparator is sequentially connected across each channel and is compared against the operational channel. Depending upon the configuration, the Input data read or Output logic write of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low to High and High to Low logic transitions are indicated. Additional testing of output logic indicates Over-current condition when output logic is invalid for a period greater than 80µs.

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16-bit binary word. Each bit corresponds to one of 11 (16) channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Read Input or Output

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”). Each bit of 16-bit binary word corresponds to one of 11 (16) channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

De-bounce Time

De-bounce time can be utilized when channel is selected as an input to "filter" or "ignore" spurious initial transitions. Enter required de-bounce time into appropriate channel registers. LSB weight determined from *Debounce LSB register.*. Once a signal level is a logic voltage level period longer than the De-bounce time (Logic High > 2.0 v, and Logic Low < 0.8 v), a logic transition is validated. Signal pulse widths less than De-bounce time are filtered. Once valid, the transition status register flag is set for the channel and the output logic changes state. Enter a value of 0 to disable De-bounce filtering. De-bounce defaults to 00h upon reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
DE-BOUNCE TIME	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT LSB=Programmable

De-bounce LSB

De-bounce resolution= 160 ns x 2 de-bounce LSB value

This results in a minimum resolution of 160 ns (Debounce LSB=0) and a maximum resolution of 5.24 ms (Debounce LSB=15).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
DE-BOUNCE LSB	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	D=DATA BIT

Slew Rate Mode

Logic selectable reduced slew rate mode softens the driver output edges to control high frequency EMI emissions. With "slow" mode selected, the data rate is limited to about 250 kbps. "1" = normal mode, "0" = slow mode.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
													B4	B3	B2	B1	Bank
SLEW RATE MODE	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	D=DATA BIT

Bank	**Channel**
B1	1-4
B2	5-8
B3	9-12
B4	13-16

Input Termination Control

Each differential input pair can be programmed to have an input termination of @ 120Ω or 12kΩ. Write logic '1' to select 120Ω for each channel. Default is @ 12KΩ

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
INPUT TERMINATION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output Format

Configure channels in groups of 8. Write integer 0 for input, 3 for output: Default is configured for Input.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch 08		Ch 07		Ch 06		Ch 05		Ch 04		Ch 03		Ch 02		Ch 01		Channel
INPUT/OUTPUT CH 09-11	Ch 16		Ch 15		Ch 14		Ch 13		Ch 12		Ch 11		Ch 10		Ch 09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT
Integer	D_H	D_L															
0	**0**	**0**	Input														
3	**1**	**1**	Output														

Reset Over-Current

Write integer “1” to reset all eleven channels (per module), which is used to reset disabled channel(s) following an over-current condition. When reset process is complete, processor will write a “0” back to the *Reset Over-Current* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESET OVER-CURRENT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	D=DATA BIT

Status Indications

The following status conditions can be monitored (latching registers – reading register will un-latch):

- **Fault**: When a BIT fault (redundant read back discrepancy – may also be caused by over-current or overload condition) is detected, it will be indicated within 10 ms. A fault is latched until read. Note: Programming/switching channel(s) between input/output with a high impedance load may cause spurious Fault Status – read register to un-latch and clear any ‘false’ status at time of initialization.

- **Lo-Hi Transition:** If a Lo to High transition is sensed, status is indicated (bit is set) within 100 ns.

- **Hi-Low Transition:** If a High to Low transition is sensed, status is indicated (bit is set) within 100 ns.

- **Over-current (BIT Status)**: If an overcurrent fault (may also be caused by programming/switching channel(s) between input/output with a high impedance load may cause spurious Fault Status – read register to un-latch and clear any ‘false’ status at time of initialization) is sensed, status is indicated (bit is set) within 10 ms. Output is, however, immediately disabled at time of BIT fault or over-current condition. When status is “indicated,” or bit is “set,” bit value is logic “1.” Reading will unlatch Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Interrupt Vectors

The Interrupt Vector Registers store the vectors for the specific interrupts generated by the module:

- When a Lo-Hi Transition Interrupt is enabled and occurs, the contents of Interrupt Vector Lo-Hi Transition register is the value that is reported to the user.
- When a Hi-Lo Transition Interrupt is enabled and occurs, the contents of Interrupt Vector Hi-Lo Transition register is the value that is reported to the user.
- When a BIT Interrupt is enabled and occurs, the contents of Interrupt Vector BIT register is the value that is reported to the user.
- When an Over current Interrupt is enabled and occurs, the contents of Interrupt Vector Over-current register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Interrupt Vector Lo-Hi Transition	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT
Interrupt Vector Hi-Lo Transition	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT
Interrupt Vector BIT	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT
Interrupt Vector Over-current	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding "latching" – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are "latching"; as defined, any noted transitional change on any channel will "latch" the entire Status Register.
- Once latched, there will be no further state change "sensed" by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will "unlatch" that particular status register (doesn't necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will "latch" the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read "until cleared".

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- Power-up
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern ("loop to clear") - this would also be similar to an Interrupt Service Routine (ISR) "loop to clear" function.

    Ex: Running the 'loop to clear' on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are "cleared" and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- Interrupt Software Routine (ISR)

  The ISR is typically a software (SW) handling branch (part of host application software) structured to "loop to read and clear" the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should "read" the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were "latched" – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively "re-arm" for the next transition to occur.

  Ex: The ISR should have the 'loop to clear' – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also "latch" the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

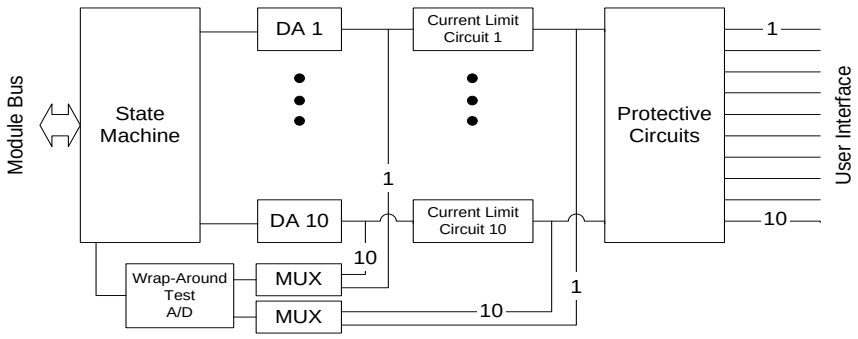
I/O (Module D8) VME Memory Map

000	Write Output CH.1-16	R/W	09E	Slew rate Mode CH.1-16	R/W	0F4	Interrupt Lo-Hi Transition Enable CH.1-16	R/W
002	Read I/O CH.1-16	R	0A0	Input Termination CH 1-16	R/W	0F6	Interrupt Hi-Lo Transition Enable CH.1-16	R/W
00C	De-bounce Time CH.1	R/W	0A4	Input/Output Format CH.1-8	R/W			
016	De-bounce Time CH.2	R/W	0A6	Input/Output Format CH.9-16	R/W	3B4	Module Design Version	R
020	De-bounce Time CH.3	R/W	0BA	De-bounce LSB CH.1-16	R/W	3B6	Module Design Revision	R
02A	De-bounce Time CH.4	R/W	0BC	Reset Over Current CH.1-16	R/W	3B8	Module DSP	R
034	De-bounce Time CH.5	R/W				3BA	Module FPGA	R
03E	De-bounce Time CH.6	R/W	0D0	Status Fault CH.1-16	R	3BC	Module ID	R
048	De-bounce Time CH.7	R/W	0D4	Status Over Current CH.1-16	R			
052	De-bounce Time CH.8	R/W	0DC	Status Lo-Hi Transition CH.1-16	R	3C4	Interrupt Lo-Hi Transition	R/W
05C	De-bounce Time CH.9	R/W	0DE	Status Hi-Lo Transition CH.1-16	R	3C6	Interrupt Hi-Lo Transition	R/W
066	De-bounce Time CH.10	R/W	0E8	Interrupt Fault Enable CH.1-16	R/W	3E0	Interrupt Vector Bit	R/W
070	De-bounce Time CH.11	R/W	0EC	Interrupt Over Current Enable CH.1-16	R/W	3E2	Interrupt Vector Over Current	R/W
07A	De-bounce Time CH.12	R/W						
084	De-bounce Time CH.13	R/W						
08E	De-bounce Time CH.14	R/W						
098	De-bounce Time CH.15	R/W						
0A2	De-bounce Time CH.16	R/W						

D/A (Modules F & J, Except J8)

Principle of Operation

DA Module Block Diagram



Ten D/A channels (Modules F1, F3, J3, J5) or four D/A High Current at 100 mA (Module F5) channels are provided per module and includes extensive diagnostics. Overloaded outputs will be detected, with the results displayed in a status word. This module incorporates major diagnostic capabilities that offer substantial improvements to system reliability because user is alerted to malfunctions within five seconds.

The system includes D/A FIFO Buffering for greater control of the output voltage and signal data. The FIFO D/A buffer will accept, store and output the voltage once enabled and triggered, for applications requiring simulation of waveform generation. The data can be "outputted" from the buffer at a maximum D/A Buffer base rate of 390.625 KHz .The thresholds of the buffer can be utilized for data flow control.

Built-In Test (BIT) / Diagnostic Capability

Two different tests, one on-line (D2) and one off-line (D3), can be selected:

The on-line (D2) test initiates automatic background BIT testing, where each channel is checked to a test accuracy of 0.2% FS and monitored for shorted output. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The off-line (D3) test uses an internal A/D that measures all D/A channels while they remain connected to the I/O. Each channel will be checked to a test accuracy of 0.2% FS. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from '1' to "0". The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus.

CAUTION: D/A Outputs are active during D3 test. Check connected loads for interaction. D/A Over-Current (short circuit) monitoring is disabled during D3 testing.

Data (Write D/A) Output (F1, F3, J3, J5 Modules)

If using bi-polar mode, write 16-bit two's complement word to the channel's Data register (7FFFh=+FS, 8000h=-FS) If using uni-polar mode, write 16-bit binary word to the channel's Data register (range: 0 to FFFFh=FS).

Data (Write D/A) Output (F5 Module Only)

If using bi-polar and single ended modes, write 16-bit two's complement word to the channel's *Data register* (range: 7FFFh=+FS, 8000h=-FS) If using unipolar and single ended modes, write 16-bit binary word to the channel's *Data register* (range: 0 to FFFFh=FS).

If using bi-polar and differential modes, write 16-bit two's complement word to channel 1 or channel 3's *Data register* (range: 7FFFh=+FS, 8000h=-FS) and the respective channel will go to that voltage. Additionally, the other channel in the pair (channel 1 is paired with channel 2, and channel 3 is paired with channel 4) will go to the two's complement of the Data register. Channel 2 and channel 4's *Data registers* aren't used in this configuration.

If using uni-polar and differential modes, write 16-bit binary word to channel 1 or channel 3's Data register (range: 0 to FFFFh=FS) and the respective channel will go to Data register / 2 + 7FFFh. Additionally, the other channel in the pair (channel 1 is paired with channel 2, and channel 3 is paired with channel 4) will go to 7FFFh - (Data register / 2). Channel 2 and channel 4's Data registers aren't used in this configuration.

D/A Polarity

Write integer 4 to the channel's *D/A Polarity register* for unipolar mode. Write integer 0 to the channel's *D/A range register* for bi-polar mode.

D/A Wrap Voltage

Read D/A *wrap voltage* register, 16-bit two's complement word (7FFFh=+FS, 8000h=-FS) for b-ipolar mode, or 16-bit binary word (range 0 to FFFFh=FS) for unipolar mode. Accuracy is 0.2% FS.

Filter Function

In process of being upgraded

Current Reading

Current reading register allows for a general read on actual current of D/A outputs being delivered per channel. The reading is in two's complement. Accuracy is approximately 5%. LSB is 0.1 mA.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Current Reading	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Output Data Trigger

DA output voltages can be programmed to change only with a synchronizing trigger, or constantly update based on the DA Data register. This control is on a channel-by-channel basis. There is a separate register for each channel. The whole system (not just the module) has two trigger lines that are shared and can be used for any DA channel.

Write "2" to D1 and D0 to constantly update the output voltage without a trigger. Write "0" to set this channel to update on the rising edge of Trigger 1 (See Section "Front and Rear Panel Connectors"). Write '1' to set this channel to update on the rising edge of Trigger 2.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Trigger	X	X	X	X	X	X	X	X	X	X	D5	D4	X	X	D1	D0	
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	Constant Update
	X	X	X	X	X	X	X	X	X	X	1	0	X	X	0	0	Trigger 1, Positive Slope
	X	X	X	X	X	X	X	X	X	X	1	1	X	X	0	0	Trigger 1, Negative Slope
	X	X	X	X	X	X	X	X	X	X	1	0	X	X	0	1	Trigger 2, Positive Slope
	X	X	X	X	X	X	X	X	X	X	1	1	X	X	0	1	Trigger 2, Negative Slope

Reset to Zero

Sets all channel outputs to 0V output. Write a '1' and module will clear this register when it sets all the outputs to zero.

Retry Overload

Module will attempt to recover from an over current condition once a second. Write a '1' to enable retry for all four channels. User writes a '0' to disable retry.

Reset Overload

Write a '1' to clear any over-current conditions and module will clear this register when any over current conditions are removed and all outputs are enabled.

Over Current Override

Write '1' to turn off over current protection. Write "0" to enable over current protection. Default value equals "0".

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Over Current Override	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Power Sup. Ch 1 & 2, Ch 3 & 4

This is the value of an AD that measures the top board power supply. It is for internal use only. It varies with the range selection, but not what the DA count for individual channels.

1 DA count equals 0.182 volts. 165 DA counts equal 30 volts.

Single/Differential Mode Selector Ch 1 & 2, Ch 3 & 4 (For F5 Module Only)

Select Single Ended or Differential mode. When in single ended mode, the pair of channels operate independently of each other. When in differential mode, the respective channels act as a pair with the output centered around zero (in bi-polar mode) or centered around half of full scale (in uni-polar mode). See Write D/A output section for more details.

0 = Single Ended Mode

1 = Differential Mode

Range Ch. 1 & 2, Ch. 3 & 4 (For F5 Module Only)

There is one range control for channels 1 and 2, and a separate one for channels 3 and 4.

5 Volt Range = 5

10 Volt Range = 10

15 Volt Range = 15

20 Volt Range = 20

25 Volt Range = 25

D/A FIFO Buffer Operational Description

The D/A FIFO Buffering offers greater control of the output voltages/signal (data). The FIFO D/A buffer will accept, store and output the voltage, once enabled and triggered, for applications requiring simulation of waveform generation. The data can be "outputted" from the buffer at a D/A Buffer base rate of 390.625 KHz or at an integer divided rate as programmed in the Sample Rate Register(s). The thresholds of the buffer can be utilized for data flow control.

D/A Data:

The available data in the FIFO buffer is stored in system memory on the card (Reference the D/A Memory Map for module's register offset address location) and can be retrieved one "WORD" (16 bits) at a time." Example: for CH1 this memory address location will be the board base address + module offset + register offset (CH1 FIFO Buffer Data register offset 0x0100h). The data is presented in two's complement format depending on the range and polarity setting of the individual channel. For bipolar mode; 7FFFh=+FS, 8,000h=-FS. For unipolar mode, range is from 0h to FFFFh = FS.

Description	D/A Data (16-bit hex)
Data ch1-10	Data Range: (0x0000-0xFFFF)

Words in FIFO:

This is a counter that reports the number of data in a 2-byte word stored in the FIFO buffer. Every time a read operation is made to the D/A FIFO Buffer Data memory address, its corresponding "*Words in FIFO*" counter will be decremented by one. This register contains the number of data words in the buffer and is "dynamically" updated. In single shot mode (buffer control = 0x01), the software trigger pops out 'size – 1' words from the FIFO. **Example**: When Words in FIFO=10, and Size=11, initiating a trigger will read ten words from the FIFO resulting in Words in FIFO=0. The maximum number of words that can be stored in the FIFO is 26,213(0x6665).

Description	Words in FIFO (16-bit hex)
Words in ch1-10	Data Range: (0x0000-0x6665)

Hi-Threshold:

The Hi-Threshold level is a value used to set the high limit bit (B2) of the individual channel status register in System memory location: 0x240 – 0x252. When the "Words in FIFO" counter is greater than or equal to the value stored in the hi-threshold register, the high limit bit (B2) of the channel status register will be set. When the "Words in FIFO" counter is less than or equal to the value stored in the Lo-threshold register, the high limit bit (B2) of the channel status register will be reset (defaulted hysteresis).

Set = "logical 1"

Reset = "logical 0"

Description	Hi-Threshold (16-bit hex)
Hi-Threshold in ch1-10	Data Range: (0x0000-0x6665)

Lo-Threshold:

The Lo-Threshold level is a value used to set or reset the low limit bit (B1) of the individual channel status register in System memory location: 0x240 – 0x252. When the "Words in FIFO" counter is less than or equal to the value stored in the Lo-Threshold, the low limit bit (B1) of the channel status register will be set. When the "Words in FIFO" counter is greater than or equal to the value stored in the Hi-Threshold, the low limit bit (B1) of the channel status register will be reset (defaulted hysteresis).

Set = "logical 1"

Reset = "logical 0"

Description	Low-Threshold (16-bit hex)
Low-Threshold in ch1-10	Data Range: (0x0000-0x6665)

Delay:

Set the number of delay samples (based on the sample rate) before the actual FIFO data is "outputted" after a trigger is initiated. This sets a delay time after trigger prior to "outputting" the data.

Description	Delay (16-bit hex)
Delay in ch1-10	Data Range: (0x0000-0xFFFF)

Size:

Sets the size of the FIFO buffer. The largest size that a FIFO buffer can be is 26,213(0x6665)

Description	Size (16-bit hex)
Size in ch1-10	Data Range: (0x0000-0x6665)

(If size is set to **0, the buffer will be read and output** after triggering. The user must insure (via threshold or equivalent) that data is being "fed" to the buffer. **Otherwise, i**f data in the buffer empties, the channel will output the last value. **Note**: It is recommended that Size be set as part of an initialization. It is not recommended to change Size while there are words in the buffer.

Sample Rate:

The sample rate sets the "output update" rate for the FIFO buffer. The number entered in the Sample (update) Rate register will be the divisor of the actual Base D/A sample rate (Clock Rate Control). **For example,** the Base D/A Sample Rate is 390.625 KHz and the Sample Rate register is set to 2. After triggering, the output data rate will be 195.3125 KHz. For full Base D/A output rate from data stored in the buffer (390.625 KHz), the sampling rate would be set to '1'.

Description	Sample Rate (16-bit hex)
Rate in ch1-10	Data Range: (0x0001-0xFFFF)

Clear FIFO:

Whenever the Clear FIFO is set for the individual channel, it initializes the "Words in FIFO" to zero. A "write" of 0x0h initiates the clear. All the counters are reset and the output of the channel reverts back to whatever was set in the "DATA" register. To re-start the buffer output, the data would need to be re-loaded and re-triggered. **Note**: After setting the *Clear FIFO* register, the FIFO Status register must be read twice to update the empty status flag. Also, Clear FIFO will not clear Sample Done status bit.

Description	Clear FIFO (16-bit hex)
Clear in ch1-10	Data Range: (0x0000)

Buffer Control:

Defines the Buffer Operation Modes.

B0 = Buffer Enable

1 = Enable	Enables buffer data to be output, once triggered, at set sample rate and data size
0 = Disable	Disables Buffer Data "output". Output is directly controlled from DATA register.

B1 = Mode Bit

0 = "1-Shot" Mode:	The data will be "outputted" from the FIFO Buffer, once triggered" at the set sample rate (and set sample size) one time.
1 = "Repeat" Mode:	The data will be "outputted" from the FIFO Buffer, once triggered" at the set sample rate (and set sample size) and continuously repeat. Once disabled, the data will finish cycle and stay with output at last value.

B2 = Reserved

B3 = Reserved

B4 = Reserved

B5 = Reserved

B6 = Reserved

B7 = Reserved

Set the bits for Buffer Control

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Buffer Control	X	X	X	X	X	X	X	X	X	X	X	X	X	X	B1	B0

Description	Buffer Ctrl.(16-bit hex)
Buf. Ctrl. in ch1-10	Data Range: B0-B1

Trigger Control:

The FIFO can be started/triggered by different sources (either software control or via external pulse).

D0-D1 = Trigger Source Select (choose one only)

00 = Ext. Trigger 2
01 = Ext. Trigger 1
10 = Software Trigger

D2 = Reserved
D3 = Reserved
D4 = Slope (External Trigger)
0 = Positive Slope
1 = Negative Slope
D5 = Trigger Enable
0 = Trigger Disable
1 = Trigger Enable
D6 = Reserved
D7 = Trigger Clear (Stops from continuous trigger)
0 = Not Clear
1 = Clear
(**Note**: Must set back to "0" after clear to allow next trigger)

Register Write	Trig Source	Slope
0x20	Ext Trigger 2	Positive
0x21	Ext Trigger 1	Positive
0x22	SW Trigger	Positive (Don't care)
0x30	Ext Trigger 2	Negative
0x31	Ext Trigger 1	Negative
0x32	SW Trigger	Negative (Don't care)
0x40	Initiate	
0x80	Stop (Clear Trigger)	

Set the bits for Trigger Control

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Trigger Control	X	X	X	X	X	X	X	X	Trigger Clear	X	Trigger Enable	Slope	X	X	Trigger Source	

Description — Trigger Ctrl.(16-bit hex)

Trigger Ctrl. in ch1-10 — Data Range: D0-D7

FIFO Status:

The FIFO status register indicates the current condition of the FIFO buffer. B0-B4 is used to show the different conditions of the buffer. **Note**: After setting the *Clear FIFO* register, the FIFO Status register must be read twice to update the empty status flag.

B0 = Empty. When "Words In FIFO" register is zero, B0 = 1; otherwise B0 =0.
B1 = Low Limit. When "Words In FIFO" register" ≤ "Low-Threshold", B1= 1; otherwise B1 =0.
B2 = High Limit. When "Words In FIFO" register" ≥ "Hi-Threshold", B2=1; otherwise B2 =0.
B3 = FIFO Full. When "Words In FIFO" register" = 26213, B3=1; otherwise B3 =0.
B4 = Sample Done. When "Words In FIFO" register = "Size", B4=1; otherwise B4 =0.

Description — FIFO Status (16-bit hex)

FIFO Status in ch1-10 — Data Range: B0-B4

Interrupt Enable:

Interrupt(s) may be enabled based on the following:

B0 = Empty. When "Words In FIFO" register is zero, B0 = 1; otherwise B0 =0.

B1 = Low Limit. When "Words In FIFO" register" < "Low-Threshold", B1= 1; otherwise B1 =0.

B2 = High Limit. When "Words In FIFO" register" > "Hi-Threshold", B2=1; otherwise B2 =0.

B3 = FIFO Full. When "Words In FIFO" register" = 26213, B3=1; otherwise B3 =0.

B4 = Sample Done. When "Words In FIFO" register = "Size", B4=1; otherwise B4 =0.

Note: If an interrupt is enabled utilizing the low and high limit thresholds, the interrupt will not be "reset" or generate a new interrupt until the opposite threshold has been crossed (hysteresis). **For example**, if an interrupt enable is set for High Limit Threshold, once set, a new High Limit Threshold interrupt will not be generated until the Low Limit Threshold has been crossed.

Description	FIFO Status (16-bit hex)
Interrupt Enable CH1-10	Data Range: B0-B4

Software Trigger:

Software trigger is used to kick start the FIFO buffer and the collection of data. In order to use this operation, the "Trigger Ctrl" register must be set up properly. Setting or resetting the "Software Trigger" will start FIFO data collection for ALL

Description	Software Trigger (16-bit hex)
Software Trigger	Data Range: 0x0-0xFFFF

Clock Rate Input:

(Not implemented – Pending)

Test Enable

Set bit to enable associated Built-In Self Test (D2) or (D3).

Write '1' to (D2) to initiate automatic background BIT testing status reporting. Card will (once every second) write 55h at *D2 Test Verify* register when D2 is enabled. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 1 second, to verify that background bit testing is activated.

The off-line (D3) test cycle, when activated, is completed within 10 seconds and results can be read from the associated status registers when (D3) enable changes from '1' to "0". Any failure triggers an Interrupt (if enabled). All testing requires no external programming and is initiated by writing '1' or terminated by writing "0".

CAUTION: D/A Outputs are active during D3 test. Check connected loads for interaction. D/A Over-Current (short circuit) monitoring is disabled during D3 testing.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TEST ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0

D2 Test Verify

Card will write 55h at *D2 Test Verify* register when (D2) is enabled (maximum 1 second). User can clear to 00h and then read again, after 1 second, to verify that background bit testing is activated.

BIT Status

Check the register contents to verify the corresponding bit for a channel's BIT Status. A "0" =Normal; '1' = Non-compliant D/A conversion (outside 0.2% FS accuracy spec). Register latches on any channel bit fault. Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status

Check the corresponding bit of the *Over Current Status* registers for over current draw for each active channel. A "0" =Normal; '1' = Over Current. An over current draw from the output of any D/A channel is detected within 2 seconds and will latch the corresponding bit in the *Over Current Status* register. Reading any status bit will unlatch the entire register.

Note: reading this register does not cause any outputs to be enabled; only *Retry Overload* or *Reset Overload* registers can re-enable outputs. Over Current Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Over Current Status.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status Intr Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Interrupt Vector

When a BIT Interrupt is enabled and occurs, the contents of BIT Interrupt Vector register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT Interrupt Vector	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Channel X FIFO Interrupt Vector

When a FIFO Interrupt is enabled and occurs, the contents of Channel X FIFO Vector register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Channel X FIFO Interrupt Vector	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Over-Current Interrupt Vector

When an Over-Current Interrupt is enabled and occurs, the contents of Over-Current Interrupt Vector register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Over-Current Interrupt Vector	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding “latching” – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are “latching”; as defined, any noted transitional change on any channel will “latch” the entire Status Register.
- Once latched, there will be no further state change “sensed” by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will “unlatch” that particular status register (doesn’t necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will “latch” the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read “until cleared”.

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern (“loop to clear”) - this would also be similar to an Interrupt Service Routine (ISR) “loop to clear” function.

    Ex: Running the ‘loop to clear’ on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are “cleared” and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

  The ISR is typically a software (SW) handling branch (part of host application software) structured to “loop to read and clear” the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should “read” the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were “latched” – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively “re-arm” for the next transition to occur.

  Ex: The ISR should have the ‘loop to clear’ – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also “latch” the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

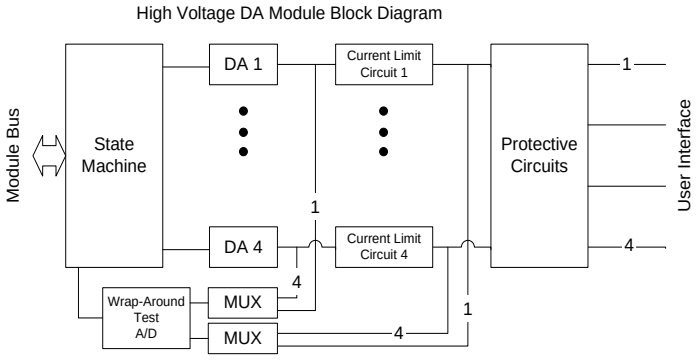
D/A (MODULE F OR J, EXCEPT J8) VME MEMORY MAP

000	Data 1	R/W	100	CH1 FIFO Buffer Data	W	1C0	CH1 Sample Rate	R/W	280	Software Trigger	R/W
002	Data 2	R/W	102	CH2 FIFO Buffer Data	W	1C2	CH2 Sample Rate	R/W			
004	Data 3	R/W	104	CH3 FIFO Buffer Data	W	1C4	CH3 Sample Rate	R/W	37C	Test Enable	R/W
006	Data 4	R/W	106	CH4 FIFO Buffer Data	W	1C6	CH4 Sample Rate	R/W	37E	D2 Test verify	R/W
008	Data 5	R/W	108	CH5 FIFO Buffer Data	W	1C8	CH5 Sample Rate	R/W	380	BIT Status Ch.1-10	R
00A	Data 6	R/W	10A	CH6 FIFO Buffer Data	W	1CA	CH6 Sample Rate	R/W	382	Over Curr. Status Ch.1-10	R
00C	Data 7	R/W	10C	CH7 FIFO Buffer Data	W	1CC	CH7 Sample Rate	R/W	384	BIT Stat Inter. Enable Ch.1-10	R
00E	Data 8	R/W	10E	CH8 FIFO Buffer Data	W	1CE	CH8 Sample Rate	R/W	386	O.C. Interrupt Enable Ch.1-10	R
010	Data 9	R/W	110	CH9 FIFO Buffer Data	W	1D0	CH9 Sample Rate	R/W			
012	Data 10	R/W	112	CH10 FIFO Buffer Data	W	1D2	CH10 Sample Rate	R/W	3C2	CH1 FIFO Interrupt Vector	R/W
									3C4	CH 2 FIFO Interrupt Vector	R/W
014	Polarity 1	R/W	120	CH1 FIFO Words	R	1E0	CH1 Clear FIFO	R/W	3C6	CH 3 FIFO Interrupt Vector	R/W
016	Polarity 2	R/W	122	CH2 FIFO Words	R	1E2	CH2 Clear FIFO	R/W	3C8	CH 4 FIFO Interrupt Vector	R/W
018	Polarity 3	R/W	124	CH3 FIFO Words	R	1E4	CH3 Clear FIFO	R/W	3CA	CH 5 FIFO Interrupt Vector	R/W
01A	Polarity 4	R/W	126	CH4 FIFO Words	R	1E6	CH4 Clear FIFO	R/W	3CC	CH 6 FIFO Interrupt Vector	R/W
01C	Polarity 5	R/W	128	CH5 FIFO Words	R	1E8	CH5 Clear FIFO	R/W	3CE	CH 7 FIFO Interrupt Vector	R/W
01E	Polarity 6	R/W	12A	CH6 FIFO Words	R	1EA	CH6 Clear FIFO	R/W	3D0	CH 8 FIFO Interrupt Vector	R/W
020	Polarity 7	R/W	12C	CH7 FIFO Words	R	1EC	CH7 Clear FIFO	R/W	3D2	CH 9 FIFO Interrupt Vector	R/W
022	Polarity 8	R/W	12E	CH8 FIFO Words	R	1EE	CH8 Clear FIFO	R/W	3D4	CH 10 FIFO Interrupt Vector	R/W
024	Polarity 9	R/W	130	CH9 FIFO Words	R	1F0	CH9 Clear FIFO	R/W			
026	Polarity 10	R/W	132	CH10 FIFO Words	R	1F2	CH10 Clear FIFO	R/W	3E0	BIT Interrupt Vector	R/W
									3E2	Over Curr. Interrupt Vector	R/W
028	Wrap Voltage 1	R	140	CH1 Hi-Threshold	R/W	200	CH1 Buffer Control	R/W			
02A	Wrap Voltage 2	R	142	CH2 Hi-Threshold	R/W	202	CH2 Buffer Control	R/W	3B4	Module Design Ver.	R
02C	Wrap Voltage 3	R	144	CH3 Hi-Threshold	R/W	204	CH3 Buffer Control	R/W	3B6	Module Design Rev.	R
02E	Wrap Voltage 4	R	146	CH4 Hi-Threshold	R/W	206	CH4 Buffer Control	R/W	3B8	Module DSP	R
030	Wrap Voltage 5	R	148	CH5 Hi-Threshold	R/W	208	CH5 Buffer Control	R/W	3BA	Module FPGA	R
032	Wrap Voltage 6	R	14A	CH6 Hi-Threshold	R/W	20A	CH6 Buffer Control	R/W	3BC	Module ID	R
034	Wrap Voltage 7	R	14C	CH7 Hi-Threshold	R/W	20C	CH7 Buffer Control	R/W			
036	Wrap Voltage 8	R	14E	CH8 Hi-Threshold	R/W	20E	CH8 Buffer Control	R/W			
038	Wrap Voltage 9	R	150	CH9 Hi-Threshold	R/W	210	CH9 Buffer Control	R/W			
03A	Wrap Voltage 10	R	152	CH10 Hi-Threshold	R/W	212	CH10 Buffer Control	R/W			
03C	Current Reading 1	R	160	CH1 Lo-Threshold	R/W	220	CH1 FIFO Trig Control	R/W			
03E	Current Reading 2	R	162	CH2 Lo-Threshold	R/W	222	CH2 FIFO Trig Control	R/W			
040	Current Reading 3	R	164	CH3 Lo-Threshold	R/W	224	CH3 FIFO Trig Control	R/W			
042	Current Reading 4	R	166	CH4 Lo-Threshold	R/W	226	CH4 FIFO Trig Control	R/W			
044	Current Reading 5	R	168	CH5 Lo-Threshold	R/W	228	CH5 FIFO Trig Control	R/W			
046	Current Reading 6	R	16A	CH6 Lo-Threshold	R/W	22A	CH6 FIFO Trig Control	R/W			
048	Current Reading 7	R	16C	CH7 Lo-Threshold	R/W	22C	CH7 FIFO Trig Control	R/W			
04A	Current Reading 8	R	16E	CH8 Lo-Threshold	R/W	22E	CH8 FIFO Trig Control	R/W			
04C	Current Reading 9	R	170	CH9 Lo-Threshold	R/W	230	CH9 FIFO Trig Control	R/W			
04E	Current Reading 10	R	172	CH10 Lo-Threshold	R/W	232	CH10 FIFO Trig Control	R/W			
050	Output Data Trigger 1	R/W	180	CH1 Delay	R/W	240	CH1 FIFO Status	R			
052	Output Data Trigger 2	R/W	182	CH2 Delay	R/W	242	CH2 FIFO Status	R			
054	Output Data Trigger 3	R/W	184	CH3 Delay	R/W	244	CH3 FIFO Status	R			
056	Output Data Trigger 4	R/W	186	CH4 Delay	R/W	246	CH4 FIFO Status	R			
058	Output Data Trigger 5	R/W	188	CH5 Delay	R/W	248	CH5 FIFO Status	R			
05A	Output Data Trigger 6	R/W	18A	CH6 Delay	R/W	24A	CH6 FIFO Status	R			
05C	Output Data Trigger 7	R/W	18C	CH7 Delay	R/W	24C	CH7 FIFO Status	R			
05E	Output Data Trigger 8	R/W	18E	CH8 Delay	R/W	24E	CH8 FIFO Status	R			
060	Output Data Trigger 9	R/W	190	CH9 Delay	R/W	250	CH9 FIFO Status	R			
062	Output Data Trigger 10	R/W	192	CH10 Delay	R/W	252	CH10 FIFO Status	R			
068	D/A Reset to zero	R/W	1A0	CH1 FIFO Size	R/W	260	CH1 Interrupt Enable	R/W			
06A	D/A Retry Overload	R/W	1A2	CH2 FIFO Size	R/W	262	CH2 Interrupt Enable	R/W			
06C	D/A Reset Overload	R/W	1A4	CH3 FIFO Size	R/W	264	CH3 Interrupt Enable	R/W			
06E	Over Current Override	R/W	1A6	CH4 FIFO Size	R/W	266	CH4 Interrupt Enable	R/W			
072	Power Sup Ch 1 & 2	R	1A8	CH5 FIFO Size	R/W	268	CH5 Interrupt Enable	R/W			
074	Power Sup Ch 3 & 4	R	1AA	CH6 FIFO Size	R/W	26A	CH6 Interrupt Enable	R/W			
076	Ch 1 & 2 Single/Diffr Sel	R/W	1AC	CH7 FIFO Size	R/W	26C	CH7 Interrupt Enable	R/W			
078	Ch 3 & 4 Single/Diffr Sel	R/W	1AE	CH8 FIFO Size	R/W	26E	CH8 Interrupt Enable	R/W			
07A	Range Ch 1 & 2	R/W	1B0	CH9 FIFO Size	R/W	270	CH9 Interrupt Enable	R/W			
07C	Range Ch 3 & 4	R/W	1B2	CH10 FIFO Size	R/W	272	CH10 Interrupt Enable	R/W			

HIGH VOLTAGE D/A (MODULE J8)

Principle of Operation

Four D/A channels are provided per module and include extensive diagnostics. The output data command word is formatted as a percentage of the Full Scale (FS) range selection which allows for maximum resolution and accuracy at lower voltage ranges. Overloaded outputs will be detected, with the results displayed in a status word. This module incorporates major diagnostic capabilities that offer substantial improvements to system reliability because user is alerted to malfunctions within 500 milliseconds.



Built-In-Test (BIT) / Diagnostic Capability

Two different tests, one on-line (D2) and one off-line (D3) can be selected:

The on-line (D2) test initiates **automatic** background BIT testing, where each channel is verified to a test accuracy of 2% FS. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The off-line (D3) test uses an internal A/D that measures all D/A channels while they remain connected to the I/O. Each channel will be checked to a test accuracy of 2% FS. The test cycle runs through nine output levels within the programmed range and polarity of the channel pair (@ 0.125% steps of FS). The test cycle is completed within 10 seconds and results can be read from the Bit Status register when (D3) test enable changes from "1" to "0". The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus.

CAUTION: D/A Outputs are active during D3 test. Check connected loads for interaction. D/A Over-Current (short circuit) monitoring is disabled during D3 testing.

Data (Write D/A) Output

If using bi-polar mode, write 16 bit two's complement word to the channel's *Data* register (7FFFh=+FS, 8000h=-FS) If using uni-polar mode, write 16 bit binary word to the channel's *Data* register (range: 0 to FFFFh=FS). At power-on, output is initialized to 0 volts.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
DATA OUTPUT	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

D/A Output Range

Program voltage range for channel pairs (1 & 2, or 3 & 4) from 20 to 100 volts to the channel's *Range* register. For 20 volts, enter integer 20. Resolution is 10 volts. 10 ma/channel maximum (source or sink) for up to 100VDC. Power on default is 0.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
										64	32	16	8	4	2	1	value in volts (LSB=1volt)
D/A OUTPUT RANGE	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

0	**0**	**0**	**0**	**0**	**0**	**0**	0 volts (or OFF)
0	**0**	**1**	**0**	**1**	**0**	**0**	20 volts
0	**0**	**1**	**1**	**1**	**1**	**0**	30 volts
0	**1**	**0**	**1**	**0**	**0**	**0**	40 volts
0	**1**	**1**	**0**	**0**	**1**	**0**	50 volts
0	**1**	**1**	**1**	**1**	**0**	**0**	60 volts
1	**0**	**0**	**0**	**1**	**1**	**0**	70 volts
1	**0**	**1**	**0**	**0**	**0**	**0**	80 volts
1	**0**	**1**	**1**	**0**	**1**	**0**	90 volts
1	**1**	**0**	**0**	**1**	**0**	**0**	100 volts

D/A Output Polarity

Write integer 4 to the channel's *D/A Polarity* register for unipolar mode. Write integer "0" to the channel's *D/A polarity* register for bi-polar mode. Power on default is bipolar (0).

D/A Wrap-Around

Read D/A *wrap-around data* register, 16 bit two's complement word (7FFFh=+FS, 8000h=-FS) for bipolar mode, or 16 bit binary word (range 0 to FFFFh=FS) for unipolar.

Current Reading

Current reading register allows for a general read on actual current of D/A outputs being delivered per channel. The reading is in two's complement. Accuracy is approximately 5%. LSB is 0.1 mA.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Current Reading	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

Reset to Zero

Sets all channel outputs to 0V output. Write a '1' and module will clear this register when it sets all the outputs to zero.

Retry Overload

Module will attempt to recover from an over current condition once a second. Write a '1' to enable retry for all four channels. Write a '0' to disable retry.

Reset Overload

Write a '1' to clear any over-current conditions and module will clear this register when any over current conditions are removed and all outputs are enabled.

Over Current Override

Write “1” to turn off over current protection. Write “0” to enable over current protection. Default value equals “0”.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Over Current Override	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Test Enable

Set bit to enable associated Built-In Self Test (D2) or (D3).

Write “1” to (D2) to initiate automatic background BIT testing status reporting. Card will (once every second) write 55h at *D2 Test Verify* register when D2 is enabled. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 1 second, to verify that background bit testing is activated.

The off-line (D3) test cycle, when activated, is completed within 10 seconds and results can be read from the associated status registers when (D3) enable changes from “1” to “0”. Any failure triggers an Interrupt (if enabled). All testing requires no external programming and is initiated by writing “1” or terminated by writing “0”.

CAUTION: D/A Outputs are active during D3 test. Check connected loads for interaction. D/A Over-Current (short circuit) monitoring is disabled during D3 testing.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TEST ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0

D2 Test Verify

Card will write 55h at *D2 Test Verify* register when (D2) is enabled (maximum 1 second). User can clear to 00h and then read again, after 1 second, to verify that background bit testing is activated.

BIT Status

Check the corresponding bit for a channel’s BIT Status. A “0” =Normal; “1” = Non-compliant D/A conversion (outside 2% FS accuracy spec). This register becomes latched when BIT detects a non-compliant status. Reading this register will cause that bit to be unlatched. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status

Check the corresponding bit of the *Over-Current Status* register for over current draw for each active channel. A “0” =Normal; “1” = Over Current. An over current draw from the output of any D/A channel is detected within 500 milliseconds. This register becomes latched when an Over Current condition occurs. Reading the Over Current Status register will cause this status register to unlatch. **NOTE:** reading this register does not cause any outputs to be enabled; only *Retry Overload* or *Reset Overload* registers can re-enable outputs. Over Current Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT STATUS INTR ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Over Current Status.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OVER CURRENT INTR ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

BIT Interrupt Vector

When a BIT Interrupt is enabled and occurs, the contents of BIT Interrupt Vector register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT Interrupt Vector	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Over-Current Interrupt Vector

When an Over-Current Interrupt is enabled and occurs, the contents of Over-Current Interrupt Vector register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Over-Current Interrupt Vector	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding “latching” – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are “latching”; as defined, any noted transitional change on any channel will “latch” the entire Status Register.
- Once latched, there will be no further state change “sensed” by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will “unlatch” that particular status register (doesn’t necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will “latch” the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read “until cleared”.

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern (“loop to clear”) - this would also be similar to an Interrupt Service Routine (ISR) “loop to clear” function.

    Ex: Running the ‘loop to clear’ on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are “cleared” and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

  The ISR is typically a software (SW) handling branch (part of host application software) structured to “loop to read and clear” the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should “read” the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were “latched” – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively “re-arm” for the next transition to occur.

  Ex: The ISR should have the ‘loop to clear’ – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also “latch” the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

D/A (MODULE J8) VME MEMORY MAP

000	Data	CH1	W/R	018	Wrap-around CH3	R	380	BIT Status CH1-4	R
002	Data	CH2	W/R	01A	Wrap-around CH4	R	382	Over Current Status CH1-4	R
004	Data	CH3	W/R				384	BIT Status Interrupt Enable CH1-4	W/R
006	Data	CH4	W/R	01C	Current Read CH1	R	386	Over Current Interrupt Enable CH1-4	W/R
				01E	Current Read CH2	R			
008	Range	CH 1 & 2	W/R	020	Current Read CH3	R	3B4	Module Design Version	R
00A	Range	CH 3 & 4	W/R	022	Current Read CH4	R	3B6	Module Design Revision	R
							3B8	Module DSP	R
00C	Polarity	CH1	W/R	068	Reset to Zero	W/R	3BA	Module FGPA	R
00E	Polarity	CH2	W/R	06A	Retry Overload	W/R	3BC	Module ID	R
010	Polarity	CH3	W/R	06C	Reset Overload	W/R			
012	Polarity	CH4	W/R	06E	Over Current Override	R/W	3E0	BIT Interrupt Vector	W/R
							3E2	Over-Current Interrupt Vector	W/R
014	Wrap-around	CH1	R	37C	Test Enable	W/R			
016	Wrap-around	CH2	R	37E	D2 Test Verify	W/R			

THERMOCOUPLE MEASUREMENT (MODULE G3)

Principle of Operation

The thermocouple is a temperature-measuring device typically consisting of two dissimilar conductors that contact each other at one or more spots. It produces a voltage when the temperature of one of the spots differs from the reference temperature at other parts of the circuit. Thermocouples are a widely used type of temperature sensor for measurement and control, and can also convert a temperature gradient into electricity. In contrast to most other methods of temperature measurement, thermocouples are self-powered and require no external form of excitation. The main limitation with thermocouples is accuracy; system errors of less than 1°C can be difficult to achieve. Thermocouples are suitable for measuring over a large temperature range, up to 2300 °C. Applications include temperature measurement for rocket and/or jet engines, gas turbine exhaust, diesel engines and other MIL/AERO/INDUSTRIAL embedded or test processes. They are arguably less suitable for applications where smaller temperature differences need to be measured with high accuracy, for example the range 0–100 °C with 0.1 °C accuracy. For such applications resistance temperature detectors (RTDs) may be more suitable.

The Thermocouple Measurement **G3** Module provides up to six individual isolated thermocouple or low-voltage range measurement channels. Full featured programmability provides interfaces for virtually all industry standard NIST temperature ranges (J, K, T, E, N, B, R, and S thermocouple types).

Equipped with an external mounted (@ 2” x 2”) iso-thermal interface/terminal block (optional accessory, NAI P/N ACC-ISO-THERM-BLK1) for connecting thermocouple wiring and housing a cold-junction-compensation temperature sensor, the TC1 has a direct interface and automatically provides compensated measurements at accuracies up to ±0.2°C. As an option, for certain rugged embedded systems and applications, the junction temperature offsets may be directly programmed for standalone operation or via ambient/junction temperature measurement by other means including internal temperature sensor.

The fundamental design is based on independent 24-bit Sigma-Delta A/D converters for each channel, therefore, the G3 may be alternatively programmed and used for direct precision low voltage measurements (±100 mV) for uses in other low-voltage range A/D applications (i.e. shunt resistor voltage/current sense measurements).

The G3 is designed for rugged embedded “on-the-move” or laboratory-grade environments, and provides continuous background built-in-test (BIT) capabilities for accuracy and “open” detection monitoring and flagging.

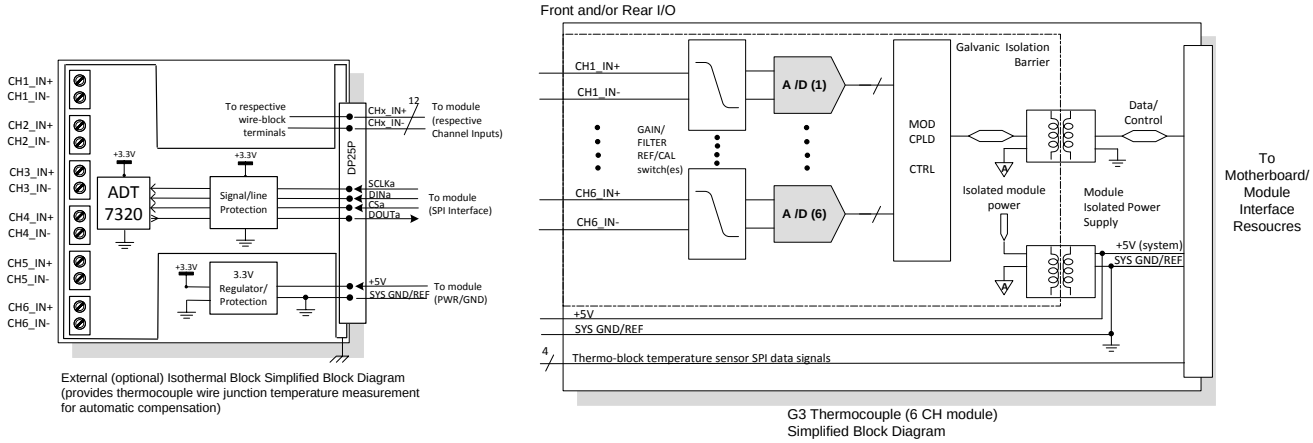


Figure 1: Simplified G3 Block Diagram

Built-In-Test (BIT) / Diagnostic Capability

Automatic background BIT testing, where each channel is functionally checked for correct A/D operation using a dedicated on-board precision reference and also monitors for any open leads. Any failure triggers an interrupt (if

enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled.

Temperature

Type: 32-bit IEEE754 binary

Range: N/A

Read/Write: R

Initialized Value: N/A

Temperature measurement is a 32-bit IEEE 754 binary word and the value is dependent upon the appropriate and expected selections made in the *Thermocouple Type* register and the units selected in the *Temperature Units* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Temperature - Hi	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
REGISTER	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
Temperature - Lo	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Thermocouple Type

Type: ASCII Hex

Range: N/A

Read/Write: R/W

Initialized Value: N/A

Enter the thermocouple type expected to be interfaced OR select the channel operation for “raw voltage”.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Thermocouple type	0	0	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D=DATA BIT

Thermocouple type	ASCII entry (hex conversion)		Thermocouple type	ASCII entry (hex conversion)
E	0x0045		B	0x0042
J	0x004A		R	0x0052
K	0x004B		S	0x0053
T	0x0054			
N	0x004E		X	0x0058
NOTE: ASCII entry “X” set the channel for “raw A/D” mode – voltage measurement provided (no thermocouple wire used / NOT converted to Temperature)				

Operational Mode

Type: 16-bit unsigned integer

Range: 0, 1

Read/Write: R/W

Initialized Value: 0

0 = standard operating mode (default); 1 = read on-board reference voltage source (47.8 mV +/- 0.2%) (For test mode only) (Module-level, applied to all channels).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Operational Mode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D	D=DATA BIT

ADC Data (RAW)

Type: 24-bit (2's complement)

Range: N/A

Read/Write: R

Initialized Value: N/A

When channel Thermocouple Type is set for ASCII "X", valid "raw" (after gain) ADC voltage measurement is available.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ADC Data (RAW) - Hi	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT
REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ADC Data (RAW) - Lo	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Thermocouple Voltage

Type: 32-bit IEEE754 binary

Range: N/A

Read/Write: R

Initialized Value: N/A

Thermocouple voltage measurement is a 32-bit IEEE 754 binary word and the value is dependent upon the valid and expected selections made in the *Thermocouple Type*.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Thermocouple Volt. - Hi	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Thermocouple Volt. - Lo	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

External Compensation Temperature

Type: 32-bit IEEE754 binary

Range: N/A

Read/Write: R

Initialized Value: N/A

Contains either the measured value of the external thermo-block temperature measurement used for compensation calculations (applies when the "*Compensation Type*" register is set for "external compensation thermo-block", or, is the user "entry" (user writes) measurement used for compensation calculations (applies when the "*Compensation Type*" register is set for "user entry". Value is a 32-bit IEEE 754 binary word. (module-level, applied to all channels).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Ext. Comp. Temp. High	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Ext. Comp. Temp. Low	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Compensation Type

Type: 16-bit binary

Range: N/A

Read/Write: R/W

Initialized Value: N/A

Sets the expected usage type (or input preference) for the junction temperature compensation (junction temperature of thermocouple wire and copper module I/O pin wiring) value. There are three compensation usage types; 1) **Internal module sensor** (where the junction temperature is determined by an on-board module sensor. 2) **External thermo-block** compensation utilized (where the junction temperature is determined by sensor interface located in the actual thermo-block) (also note, thermo-block temperature can be read from the "*External Compensation Temperature*" register. 3) **User "entry"** of compensation temperature (junction temperature is determined by user entry (i.e. if junction temperature is available and measured by some external device, the temperature can be written to the "*External Compensation Temperature*" register. (module-level, applied to all channels).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Compensation Type	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D	D	D=DATA BIT

Compensation Type	ASCII entry (hex conversion)
0x0000	Internal module sensor used
0x0001	External compensation thermo-block used
0x0002	User "entry" compensation temperature used

DPRAM Busy

Indicates the module is currently performing either BIT/OPEN detection or a background alignment is taking place. A/D or Temperature data is not being updated while DPRAM BUSY is active (BUSY = '1').

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DPRAM BUSY	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**

BIT/Open Test Interval

Time interval between successive BIT/OPEN detection tests. LSB = based upon 1 / minimum update rate (LSB = @ 239.8 ms). Writing '0' to this register disables BIT/OPEN detection. During BIT/Open Interval operation, actual measured data will be "unavailable" and qualified with DPRAM Busy bit being set in *the DPRAM Busy* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT/OPEN Test Interval	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

Update Rate

Select/enter the desired A/D update rate (module-level, applied to all channels). Does NOT affect the *BIT/Open Interval* register LSB time interval calculation.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Update Rate	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Update Rate Select	Update Rate (Hz)		Update Rate Select	Update Rate (Hz)
0x0001	470			
0x0002	242		0x0009	<<skipped>>
0x0003	123		0x000A	16.7
0x0004	62		0x000B	12.5
0x0005	50		0x000C	10.0
0x0006	39		0x000D	8.33
0x0007	33.2		0x000E	6.25
0x0008	19.6		0x000F	4.17

Temperature Units

Select the desired units of temperature measurement (directly affects the value provided in the *Temperature* register) (individual, channel-level).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Units	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Temperature Units (ASCII)	ASCII entry (hex conversion)
Celsius (C)	0x0043
Fahrenheit (F)	0x0046
Kelvin (K)	0x004B

BIT Status

Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = non-functional A/D conversion (background BIT, if enabled, fails to read on-module reference voltage within +/- 10 % tolerance. Reading any status bit will unlatch the entire register. Detected after time interval specified by *BIT/OPEN Interval* register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Detect Status

Check the corresponding bit of the *Open Detection Status* register for open/disconnected thermocouple or leads for each channel. A "0" =Normal, "1" = Open. Detected after time interval specified by *BIT/OPEN Interval* register. Reading any status bit will cause that bit to be unlatched. Open Detection Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Detection Status	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Open Detection Status. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status Interrupt Enable	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Interrupt Vector

When a BIT Interrupt is enabled and occurs, the contents of *BIT Interrupt Vector* register is the value that is reported to the user (Interrupt Service Routine (ISR)).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT Interrupt Vector	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Open Circuit Interrupt Vector

When an Open Circuit Interrupt is enabled and occurs, the contents of *Open Circuit Interrupt* Vector register is the value that is reported to the user (Interrupt Service Routine (ISR)).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Oven Circuit Interrupt Vector	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding “latching” – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are “latching”; as defined, any noted transitional change on any channel will “latch” the entire Status Register.
- Once latched, there will be no further state change “sensed” by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will “unlatch” that particular status register (doesn’t necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will “latch” the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read “until cleared”.

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern (“loop to clear”) - this would also be similar to an Interrupt Service Routine (ISR) “loop to clear” function.

    Ex: Running the ‘loop to clear’ on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are “cleared” and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

The ISR is typically a software (SW) handling branch (part of host application software) structured to “loop to read and clear” the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should “read” the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were “latched” – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively “re-arm” for the next transition to occur.

Ex: The ISR should have the ‘loop to clear’ – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also “latch” the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

Appendix A (IEEE 754 Format)

IEEE 754 Binary Formats

Type	Sign	Exponent	Significand	Total bits	Exponent bias	Bits precision
Half (IEEE 754-2008)	1	5	10	16	15	11
Single	1	8	23	32	127	24
Double	1	11	52	64	1023	53
Quad	1	15	112	128	16383	113

Sign Bit

The sign bit is as simple as it gets. 0 denotes a positive number; 1 denotes a negative number. Flipping the value of this bit flips the sign of the number.

Exponent

The exponent field needs to represent both positive and negative exponents. To do this, a bias is added to the actual exponent in order to get the stored exponent. For IEEE single-precision floats, this value is 127. Thus, an exponent of zero means that 127 is stored in the exponent field. A stored value of 200 indicates an exponent of (200-127), or 73. For reasons discussed later, exponents of -127 (all 0s) and +128 (all 1s) are reserved for special numbers.

For double precision, the exponent field is 11 bits, and has a bias of 1023.

Significand

The significand, also known as the mantissa, represents the precision bits of the number. It is composed of an implicit leading bit and the fraction bits. To find out the value of the implicit leading bit, consider that any number can be expressed in scientific notation in many different ways. For example, the number five can be represented as any of these:

5.00 × 100

0.05 × 102

5000 × 10-3

In order to maximize the quantity of representable numbers, floating-point numbers are typically stored in normalized form. This puts the radix point after the first non-zero digit. In normalized form, five is represented as 5.0 × 100.

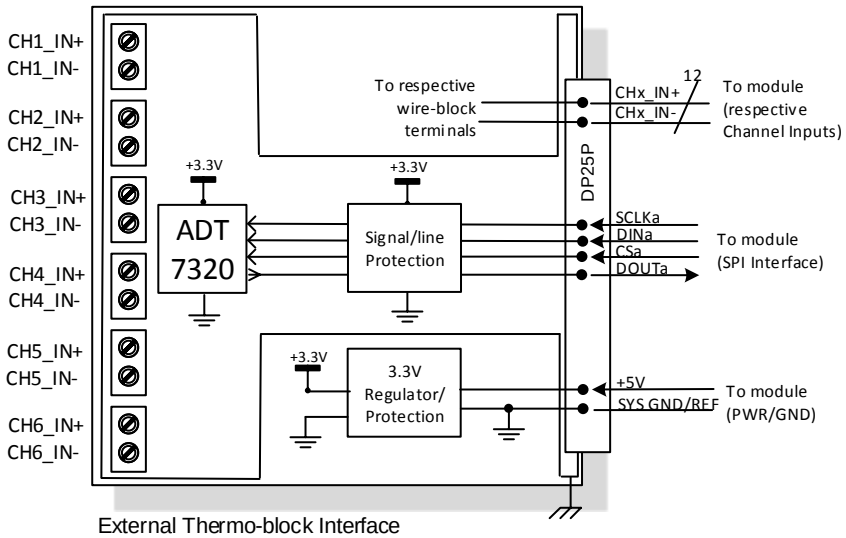
Appendix B (G3 Optional External Isothermal Block Accessory)

Isothermal Block Applications

Applications requiring the base motherboard/module to be at considerable distance from the measuring points of the thermocouples themselves may require the use of conventional (copper) wiring to be connected to the thermocouple leads. Conventional wiring (copper) when connected to the thermocouple wire will create a junction of dissimilar metals. When a junction of dissimilar metals occurs, there will be an additional flow of current that acts, in effect, as an additional thermocouple, which will affect the current flow the primary thermocouple, which ultimately affects the overall accuracy of the actual (primary) thermocouple measurement.

The primary purpose of the isothermal block is to house screw-down terminal blocks for directly connecting thermocouple wires to the interface interconnect for conventional wiring back to the board/module. The isothermal block contains a digital temperature sensor and is constructed to minimize temperature variances between channels and the isothermal block itself. In theory, the temperature of the isothermal block will be the junction temperature of the thermocouple wiring interconnect at the terminals.

The NAI P/N **ACC-ISO-THERM-BLK1** is a semi-rugged, non-sealed housing designed with terminals to secure up to (6) thermocouple interconnects (one for each channel of the G3). It is designed to be mounted/secured to a “cold plate” (surface/mass that is expected to maintain a relative constant temperature over time). The isothermal block built-in temperature sensor (ADT 7320 or equivalent) has a 16-bit SPI digital interface for direct reading by the G3 module. The G3 module, when programmed for external block compensation mode, will utilize this reference temperature and provide automatic thermocouple measurement compensation based on the temperature reading of the sensor.

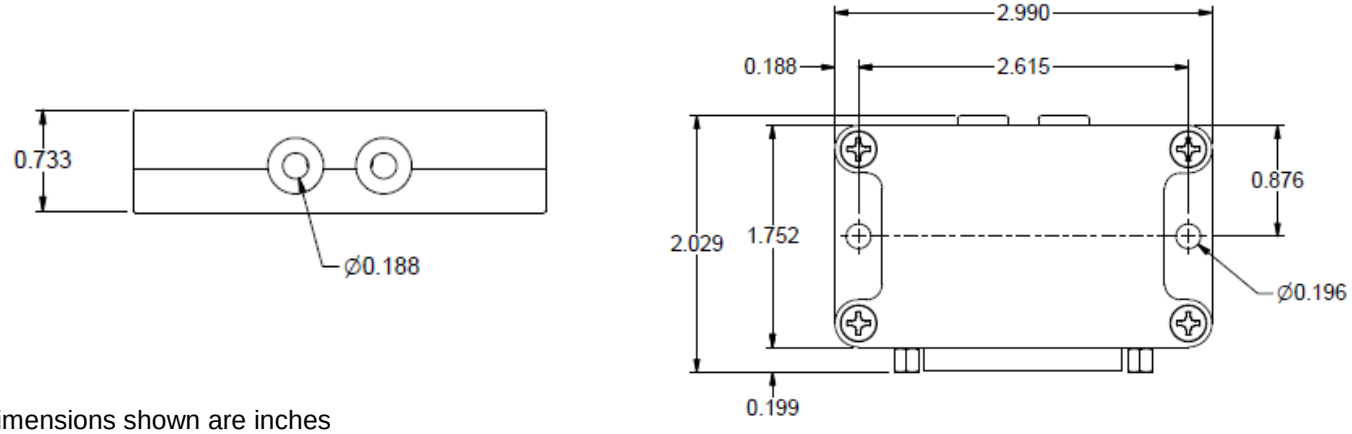


External Thermo-block Interface
(provides thermocouple wire junction temperature measurement for automatic compensation)



Optional Accessory NAI P/N ACC-ISO-THERM-BLK1

Mechanical Outline

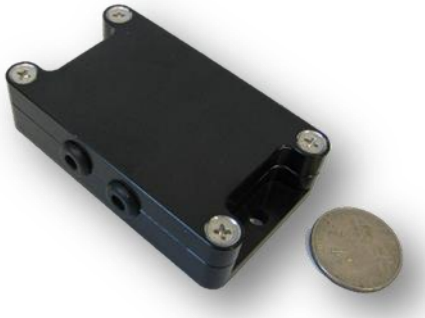


Dimensions shown are inches

Interface Details

Module Interface Connector: 25-pin DSUB-Male, AMP 747238-4 (or equivalent) / w/ Jackposts

Thermocouple wire terminal: 2-position terminal block, internal, screw-secure, Tyco, 282834-2 (or equivalent) (6 total)





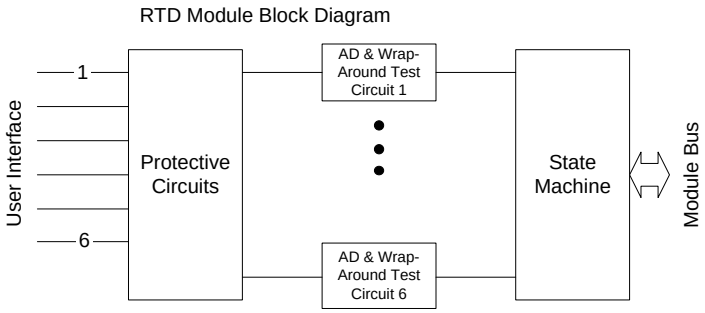
THERMOCOUPLE (MODULE G3) VME MEMORY MAP

Module length (size) – 0x400

000	Temperature – Hi Ch. 1	R	030	ADC Data (Raw) – Hi Ch. 1	R	0A8	External Comp. Temp. – Hi	R/W
002	Temperature – Lo Ch. 1	R	032	ADC Data (Raw) – Lo Ch. 1	R	0AA	External Comp. Temp. – Lo	R/W
004	Temperature – Hi Ch. 2	R	034	ADC Data (Raw) – Hi Ch. 2	R	0AC	Compensation Type	R/W
006	Temperature – Lo Ch. 2	R	036	ADC Data (Raw) – Lo Ch. 2	R			
008	Temperature – Hi Ch. 3	R	038	ADC Data (Raw) – Hi Ch. 3	R	0C0	DPRAM Busy	R
00A	Temperature – Lo Ch. 3	R	03A	ADC Data (Raw) – Lo Ch. 3	R	0C2	BIT/OPEN Test Interval	R/W
00C	Temperature – Hi Ch. 4	R	03C	ADC Data (Raw) – Hi Ch. 4	R			
00E	Temperature – Lo Ch. 4	R	03E	ADC Data (Raw) – Lo Ch. 4	R	0C6	Update Rate	R/W
010	Temperature – Hi Ch. 5	R	040	ADC Data (Raw) – Hi Ch. 5	R	0C8	Temperature Units	R/W
012	Temperature – Lo Ch. 5	R	042	ADC Data (Raw) – Lo Ch. 5	R			
014	Temperature – Hi Ch. 6	R	044	ADC Data (Raw) – Hi Ch. 6	R	0D0	BIT, Status Ch.1-6	R
016	Temperature – Lo Ch. 6	R	046	ADC Data (Raw) – Lo Ch. 6	R	0D2	Open Detect, Status Ch.1-6	R
018	Thermocouple Type Ch. 1	R/W	090	Thermocouple Volt. – Hi Ch. 1	R	0E8	Interrupt Enable, BIT	R/W
01A	Thermocouple Type Ch. 2	R/W	092	Thermocouple Volt. – Lo Ch. 1	R	0EA	Interrupt Enable, Open Detect	R/W
01C	Thermocouple Type Ch. 3	R/W	094	Thermocouple Volt. – Hi Ch. 2	R			
01E	Thermocouple Type Ch. 4	R/W	096	Thermocouple Volt. – Lo Ch. 2	R	3B4	Module Design Version	R
020	Thermocouple Type Ch. 5	R/W	098	Thermocouple Volt. – Hi Ch. 3	R	3B6	Module Design Revision	R
022	Thermocouple Type Ch. 6	R/W	09A	Thermocouple Volt. – Lo Ch. 3	R	3B8	Module DSP	R
			09C	Thermocouple Volt. – Hi Ch. 4	R	3BA	Module FPGA	R
024	Operational Mode Ch. 1	R/W	09E	Thermocouple Volt. – Lo Ch. 4	R	3BC	Module ID	R
026	Operational Mode Ch. 2	R/W	0A0	Thermocouple Volt. – Hi Ch. 5	R			
028	Operational Mode Ch. 3	R/W	0A2	Thermocouple Volt. – Lo Ch. 5	R	3E0	BIT Interrupt Vector	R/W
02A	Operational Mode Ch. 4	R/W	0A4	Thermocouple Volt. – Hi Ch. 6	R	3E2	Open Detect Interrupt Vector	R/W
02C	Operational Mode Ch. 5	R/W	0A6	Thermocouple Volt. – Lo Ch. 6	R			
02E	Operational Mode Ch. 6	R/W						

RTD (MODULE G4)

Principle of Operation



Module G4 provides six resistance temperature detectors (RTD) measurement channels. Each channel is configurable for use with the 4-wire, 3-wire or 2-wire RTD devices. The 4-wire mode (default) is the most accurate, providing excellent stability and repeatability. All RTD channels are self-calibrating because each channel is automatically calibrated to eliminate offset and gain errors. Open inputs will be detected, with the results displayed in a status word. All inputs are double buffered for immediate availability. External excitation is not required. There are six programmable full-scale ranges designed around the three most common RTD devices: 200Ω, 400Ω, 800Ω, 2000Ω, and 4000Ω from -260°C to +850°C (except for the highest range which is limited to 6500Ω or about +640°C).

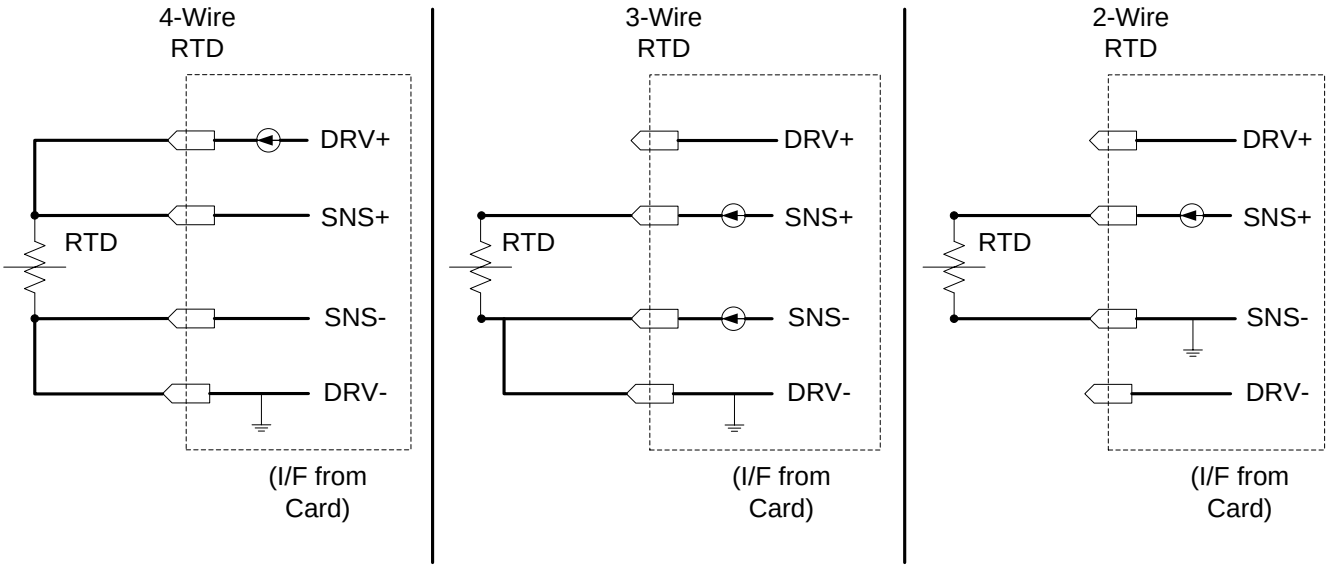


Figure 1: Typical RTD Module Connections

Built-In-Test (BIT) / Diagnostic Capability

Automatic background BIT testing, where each channel is functionally checked for correct A/D operation using a dedicated test resistor and also monitors for any open leads. Any failure triggers an interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled.

Resistance

Type: binary word

Range: N/A

Read/Write: R/W

Initialized Value: N/A

Resistance measurement is a binary word and is dependent upon range the range selected. For example, if Range '2' is selected and the register value is 0x6400:

Resistance = 0x6400 x 0.02 Ω = 512 Ω

The resistance/temperature relationship varies among RTDs and is a function of its composite material (i.e. Platinum, Copper, Nickel-Iron, Nickel, etc). An RTD's "Alpha" Temperature Coefficient and its nominal resistance (at 0°C), while operating within its applicable resistance range, provide for a first order approximation. For best accuracy, use resistance/temperature relationship provided by the RTD manufacturer:

1. Select associated *Range* (see below)
2. Read *Resistance* and scale according to selected *Range*
3. Calculate temperature using RTD manufacturer provided resistance/temperature relationship (a quadratic equation).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESISTANCE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Range

Type: 16-bit unsigned integer

Range: 0 – 5

Read/Write: R/W

Initialized Value: 0

There are six ranges to select from:

Write '0' for a 0 – 200Ω. LSB value in 'Resistance' register = 0.005 Ω.

Write '1' for a 0 – 400Ω. LSB value in 'Resistance' register = 0.01 Ω.

Write '2' for a 0 – 800Ω. LSB value in 'Resistance' register = 0.02 Ω.

Write '3' for a 0 – 2000Ω. LSB value in 'Resistance' register = 0.04 Ω.

Write '4' for a 0 – 4000Ω. LSB value in 'Resistance' register = 0.08 Ω.

Write '5' for a 0 – 6500Ω. LSB value in 'Resistance' register = 0.16 Ω.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RANGE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Wire Mode

Type: 16-bit unsigned integer

Range: 2 – 4

Read/Write: R/W

Initialized Value: 4

There are three (3) RTD wire configurations to choose from:

Write '2' for 2-wire configuration.

Write '3' for 3-wire configuration.

Write '4' for 4-wire configuration.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
WIRE MODE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

2-Wire Lead Resistance Compensation

Only used when a selected channel is set for 2-wire in the '2, 3, 4 Wire Mode' register. User enters TOTAL lead resistance measured. The LSB value is dependent on the range selected in the 'Range' register for that channel.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
2-WIRE LEAD RESISTANCE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Busy

Indicates the module is currently performing either BIT/OPEN detection or a background Calibration. Resistance data is not being updated while BUSY is active (BUSY = '1').

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BUSY	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D

BIT/Open Interval

Time interval between successive BIT/OPEN detection tests. LSB = 60ms (A/D update rate). Minimum of 1.2s (20 LSB's) is required. Writing '0' to this register disables BIT/OPEN detection. Default is 20s.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT/OPEN INTERVAL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

CAL Interval

Time interval between successive background calibrations. LSB = 60ms (A/D update rate). Minimum of 1.2s (20 LSB's) is required. Writing "0000" to this register disables background calibration. Writing a "FFFF" forces an immediate background calibration, with the register automatically being set back to "0000" upon completion of the background calibration. Default is 10 min.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CAL INTERVAL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

BIT Status

Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = Non-functional A/D conversion. Reading any status bit will unlatch the entire register. Detected after time interval specified by *BIT/OPEN Interval* register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Detection Status

Check the corresponding bit of the *Open Detection Status* register for open/disconnected RTD or leads for each channel. A "0" =Normal, "1" = Open. Detected after time interval specified by *BIT/OPEN Interval* register. Reading any status bit will cause that bit to be unlatched. Open Detection Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Detection Status	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Open Detection Status. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status Interrupt Enable	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Interrupt Vector

When a BIT Interrupt is enabled and occurs, the contents of *BIT Interrupt Vector* register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT Interrupt Vector	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Open Circuit Interrupt Vector

When an Over-Current Interrupt is enabled and occurs, the contents of *Over-Current Interrupt* Vector register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Oven Circuit Interrupt Vector	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding “latching” – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are “latching”; as defined, any noted transitional change on any channel will “latch” the entire Status Register.
- Once latched, there will be no further state change “sensed” by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will “unlatch” that particular status register (doesn’t necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will “latch” the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read “until cleared”.

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern (“loop to clear”) - this would also be similar to an Interrupt Service Routine (ISR) “loop to clear” function.

    Ex: Running the ‘loop to clear’ on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are “cleared” and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

The ISR is typically a software (SW) handling branch (part of host application software) structured to “loop to read and clear” the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should “read” the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were “latched” – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively “re-arm” for the next transition to occur.

Ex: The ISR should have the ‘loop to clear’ – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also “latch” the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

RTD (MODULE G4) VME MEMORY MAP

000	Resistance 1	R	018	Wire Mode 1[1]	R/W	0C0	BUSY	R/W
002	Resistance 2	R	01A	Wire Mode 2[1]	R/W	0C2	BIT/OPEN Interval	R/W
004	Resistance 3	R	01C	Wire Mode 3[1]	R/W	0C4	CAL Interval	R/W
006	Resistance 4	R	01E	Wire Mode 4[1]	R/W	0D0	BIT Status Ch.1-6	R
008	Resistance 5	R	020	Wire Mode 5[1]	R/W	0D2	Open Detection Status Ch.1-6	R
00A	Resistance 6	R	022	Wire Mode 6[1]	R/W	0E8	BIT Status Interrupt Enable Ch.1-6	R/W
						0EA	Open Status Interrupt Enable Ch.1-6	R/W
00C	Range 1	R/W	024	2-Wire Lead Res Ch.1	R/W	3E0	BIT Interrupt Vector	R/W
00E	Range 2	R/W	026	2-Wire Lead Res Ch.2	R/W	3E2	Over Current Interrupt Vector	R/W
010	Range 3	R/W	028	2-Wire Lead Res Ch.3	R/W	3B4	Module Design Version	R
012	Range 4	R/W	02A	2-Wire Lead Res Ch.4	R/W	3B6	Module Design Revision	R
014	Range 5	R/W	02C	2-Wire Lead Res Ch.5	R/W	3B8	Module DSP	R
016	Range 6	R/W	02E	2-Wire Lead Res Ch.6	R/W	3BA	Module FPGA	R
						3BC	Module ID	R

Note 1: Default is 4-Wire Mode.

LOAD/STRAIN (MODULE G5)

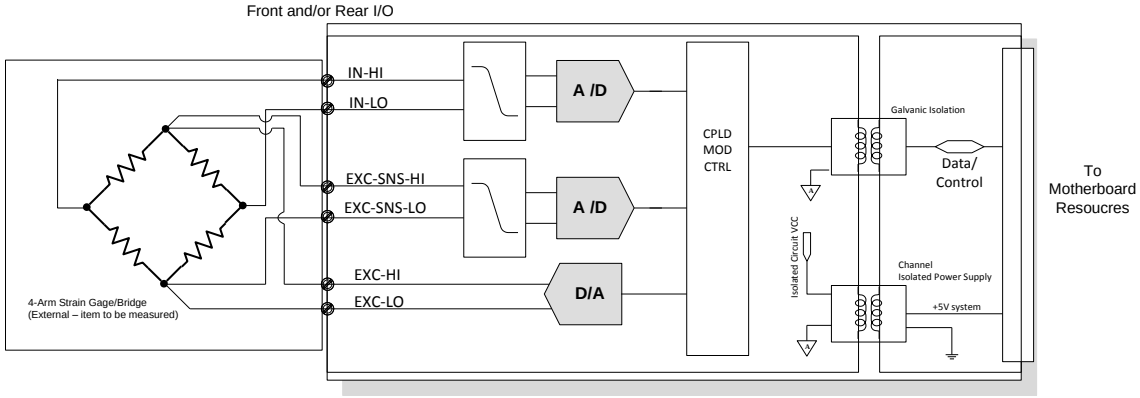
Principles of Operation

The G5 module is an intelligent four-channel module utilizing four A/Ds and the motherboard resources processor/FPGA. The G5 module is designed to read output signals, and supply excitation voltages that are commonly used in applications with pressure transducers, weigh scales, and strain gages. Each channel incorporates an Σ-Δ modulator, a PGA, and on-chip digital filtering intended for the measurement of wide dynamic range signals. Each channel contains a fourth order digital filter, with several programmable filter options. When properly applied the filter has deep notches at either 50 or 60 Hz.

The G5 may be utilized with AC or DC excited load cells. When using AC excitation, the G5 module switches the polarity of the excitation voltage from cycle to cycle. When utilizing AC excitation, consecutive A/D samples are averaged using different reference voltage polarity removing any system wide dc offsets.

The 'on-board' processor removes the user from the details of managing the A/D communication, register access and sample timing. The processor firmware provides the user with a simpler user interface with high-level commands and post calibration data. The module also contains internal factory calibration values, stored in Flash. The G5 automatically recalibrates for changes in reference voltage and die temperature.

Both internal and system calibration are included on chip; thus, the user has the option of removing offset/gain errors internal to the A/Ds only, or removing the offset/gain errors of the complete end system.



G5 Strain Gage (4 CH isolated)
Single Channel Example Block

A 6-wire load cell with SENSE_HI and SENSE_LO, with connections as shown allows the G5 to compensate for DC drops in wires connecting the Gauge to the module. The type of connection is typically referred to as a Kelvin connection. Some load cells may also have additional internal resistors, for temperature compensation purposes.

Built-In Test (BIT) / Diagnostic Capability

Automatic background BIT Built in Test functionally checks for correct A/D operation using on board dedicated test voltage divider resistor network.BIT also monitors for any open leads. Any failure triggers an interrupt (if enabled) with the results available in status registers. The testing is transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled.

Data 16

The Data 16 register returns the 16 bits resulting from the A/D conversion, and the sign bit. The A/D output is formatted as 16 bit signed two's complemented. The value read from this register is post firmware calibration. This register is read-only.

Data 16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RANGE	d23	d22	d21	d20	d19	d18	d17	d16	d15	d14	d13	d12	d11	d10	d9	d8	D=DATA BIT

Data 24

The Data 24 Hi, and Data 24 Lo, return 24 bit signed 2's complemented data as indicated in the bit map as indicated. Unused MSB of the Data 24 Hi register are zeroed.

Data 24 high	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RANGE	0	0	0	0	0	0	0	0	d23	d22	d21	d20	d19	d18	d17	d16	D=DATA BIT

Data 24 low	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RANGE	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	D=DATA BIT

Output Force

Output Force is represented as a single precision IEEE 754 floating-point number*. This value is calculated by the G5 module using the following formula:

Output Force = ((A/D data / A/D full scale range) * Gain) / ((Load Cell Full Scale Sensitivity) × (Load Cell Sensitivity))

From the perspective of the G5 module, this number is unit less. From the perspective the user, the Output Force will be in the same units used when entering the Load cell full scale Sensitivity and Load Cell Sensitivity.

Output Force High	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data	d31	d30	d29	d28	0d27	d26	D25	d24	d23	d22	d21	d20	d19	d18	d17	d16	D=DATA BIT

Output Force Low	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	D=DATA BIT

*IEEE 754 floating point format information can be found in the appendix.

Output V/V

Output in V/V (volts per volt) is represented as a single precision 32-bit floating-point number. This is a unit less ratio of Vout / Vin.

Output in V/V = A/D Data / A/D Reference

Data V/V high	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data	d31	d30	d29	d28	0d27	d26	D25	d24	d23	d22	d21	d20	d19	d18	d17	d16	D=DATA BIT

Data V/V low	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	D=DATA BIT

Range

The Range/Gain setting bits are described in the A/D specification. This register reflects the CON[2:0] bits in the A/D Configuration register

Most metallic strain gauges have low GF (gage factor) of approximately 2, where:

GF = (ΔR/R)/(ΔL/L).

Because of the low Δ Output voltage, the recommended gain setting is 128.Note that changing the gain setting affects the usable ADC input range and the factory calibration values.

G[2:0]	Gain	ADC Input range(5 v reference)
0x0	1	±5 V
0x1	Reserved	
0x2	Reserved	
0x3	8	±625 mV
0x4	16	±312.5 mV
0x5	32	±156.2 mV
0x6	64	±78.125 mV
0x7	128	±39.06 mV

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RANGE	x	x	x	x	x	x	x	x	x	x	x	x	x	G2	G1	G0	D=DATA BIT

Remote Sense Select

Remote Sense Select bit selects the source of the bridge excitation voltage. When the Ref_Sel bit is set (1) the G5 module supplies the excitation voltage. When (0) the reference voltage is source externally.

Specifications for external voltage source

Filter Configuration	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Ref_Sel	
Data	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	D=DATA BIT

Excitation Select

Excitation Select register controls the A/D ACX (AC excitation enable bit). If the signal source is ac excited, this bit must be set to 1. For dc-excited inputs, this bit must be 0. With the ACX bit at 1, the A/D assumes that the voltage at the AIN(+)/AIN(–) and REFIN(+)/REFIN(–) input terminals are reversed on alternate input sampling cycles (that is, chopped).

The Bit CHOP must be set to 1 when ac excitation is enabled. ACX, AC excitation enable bit. If the signal source to the A/D is ac excited, this bit must be set to 1.

Filter Configuration	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	ACX	
Data	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	D=DATA BIT

Chop Enable

Chop enable bit. When the CHOP bit is cleared, chop is disabled. When the CHOP bit is set, chop is enabled. When chop is enabled, the offset and offset drift of the ADC are continuously removed. However, this increases the conversion time and settling time of the ADC.

Filter Configuration	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CHOP	
Data	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	D=DATA BIT

Excitation Voltage

The Excitation Voltage register controls an external eight-bit D/A converter. When the G5 module is programmed to operate with an internal reference voltage (Remote Sense Select, Ref_Sel bit =1) Excitation voltage maximum when using internal reverence is 6.25V max, (LSB =24mv).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	X	X	X	X	X	X	X	X	3137	1569	784	392	196	98	49	24.5	Excitation Voltage in mV
RANGE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Load Cell Sensitivity

Load Cell Sensitivity is represented as a single precision (32-bit) floating-point number. Sensitivity is defined as the minimum amount of force needed to cause a change in a load cells output. Load cell sensitivity is the cell transducer output (V/V) at full-scale.

If a load cell has a 5 Volt DC (VDC) excitation voltage and a 0-250 mV output, the resultant ratio is 250mV/5VDC. This equates to 50 mV per Volt or 50:1 ratio (.02). The G5 typically programmed with a PGA gain of 128. This is because m most metallic strain gauges have low GF (gage factor) of approximately 2.

Output force high	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data	d31	d30	d29	d28	d27	d26	D25	d24	d23	d22	d21	d20	d19	d18	d17	d16	D=DATA BIT

Output force low	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	D=DATA BIT

Load Cell Full Scale Sensitivity

Load cell full-scale Sensitivity is a unit less floating point number that represent the Sensors maximum full-scale value. The sensor would specify this number in lbs, kilograms, N, etc.

Output force high	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data	d31	d30	d29	d28	d27	d26	D25	d24	d23	d22	d21	d20	d19	d18	d17	d16	D=DATA BIT

Output force low	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Data	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	D=DATA BIT

Filter Configuration

The A/D offers a lot of flexibility in the digital filter. The device has four filter options. The device can be operated with a sinc3 or sinc4 filter, chop can be enabled or disabled, and zero latency can be enabled. The filter Configuration along with the PGA gain setting selected affects the output data rate, settling time, and 50 Hz/60 Hz rejection.

The following sections describe each filter type, indicating the available output data rates for each filter option. The filter response along with the settling time and 50 Hz/60 Hz rejection is also discussed.

Filter Configuration	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	SINC3	0	0	0	SINGLE	REJ60	FS[9]	FS[8]	FS[7]	FS[6]	FS[5]	FS[4]	FS[3]	FS[2]	FS[1]	FS[0]	
Data	d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	D=DATA BIT

SINC3

Sinc3 filter select bit. When this bit is cleared, the sinc4 filter is used (default value). When this bit is set, the sinc3 filter is used. The benefit of the sinc3 filter compared to the sinc4 filter is its lower settling time. For a given output data rate, fADC, the sinc3 filter has a settling time of 3/fADC while the sinc4 filter has a settling time of 4/fADC when chop is disabled. The sinc4 filter, due to its deeper notches, gives better 50 Hz/60 Hz rejection. At low output data rates, both filters give similar RMS noise and similar no missing codes for a given output data rate. At higher output data rates (FS values less than 5), the sinc4 filter gives better performance than the sinc3 filter for RMS noise and no missing codes.

SINGLE

Single cycle conversion enable bit. When this bit is set, the A/D settles in one conversion cycle so that it functions as a zero-latency ADC. This bit has no effect when multiple analog input channels are enabled or when the single conversion mode is selected.

REJ60

This bit enables a notch at 60 Hz when the first notch of the SINC filter is at 50 Hz. When REJ60 is set, a filter notch is placed at 60 Hz when the SINC filter first notch is at 50 Hz. This allows simultaneous 50 Hz/ 60 Hz rejection.

FS[9:0]

FS[9:0] determine the filter cut-off frequency, the position of the first notch of the filter, and the output data rate for the part. In association with the gain selection, they also determine the output noise (and, therefore, the effective resolution) of the device (Please refer to Table 6 through Table 17 of the A/D specification).

When chop is disabled and continuous conversion mode is selected;

Output Data Rate = (MCLK/1024)/FS

Where FS is the decimal equivalent of the code FS[9:0] and is in the range 1 to 1023, and MCLK is the master clock frequency. With a nominal MCLK of 4.92 MHz, this results in an output data rate from 4.69 Hz to 4.8 kHz.

With chop disabled, the first notch frequency is equal to the output data rate when converting on a single channel. When chop is enabled;

Output Data Rate = (MCLK/1024)/(N × FS)

Where FS is the decimal equivalent of the code in FS[9:0] and is in the range 1 to 1023, and MCLK is the master clock frequency. With a nominal MCLK of 4.92 MHz, this results in a conversion rate from 4.69/N Hz to 4.8/N kHz, where N is the order of the SINC filter. The SINC filter's first notch frequency is equal to N × output data rate. The chopping introduces notches at odd integer multiples of (output data rate/2).

BUSY

Indicates the module is currently performing either BIT/OPEN detection or a background Calibration. Resistance data is not being updated while BUSY is active (BUSY = '1').

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BUSY	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D

BIT/OPEN Interval

Time interval between successive BIT/OPEN detection tests. LSB = 60ms (A/D update rate). Minimum of 1.2s (20 LSB's) is required. Writing '0' to this register disables BIT/OPEN detection. Default is 20s.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT/OPEN INTERVAL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

CAL Interval

Time interval between successive background calibrations. LSB = 60ms (A/D update rate). Minimum of 1.2s (20 LSB's) is required. Writing "0000" to this register disables background calibration. Writing a "FFFF" forces an immediate background calibration, with the register automatically being set back to "0000" upon completion of the background calibration. Default is 10 min.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CAL INTERVAL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

BIT Status

Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = Non-functional A/D conversion. Reading any status bit will unlatch the entire register. Detected after time interval specified by BIT/OPEN Interval register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Detection Status

Check the corresponding bit of the Open Detection Status register for open/disconnected RTD or leads for each channel. A "0" =Normal, "1" = Open. Detected after time interval specified by BIT/OPEN Interval register. Reading any status bit will cause that bit to be unlatched. Open Detection Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Detection Status	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Open Detection Status. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status Interrupt Enable	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Interrupt Vector

When a BIT Interrupt is enabled and occurs, the contents of BIT Interrupt Vector register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT Interrupt Vector	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Open Circuit Interrupt Vector

When an Over-Current Interrupt is enabled and occurs, the contents of Over-Current Interrupt Vector register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Open Circuit Interrupt Vector	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding “latching” – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are “latching”; as defined, any noted transitional change on any channel will “latch” the entire Status Register.
- Once latched, there will be no further state change “sensed” by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will “unlatch” that particular status register (doesn’t necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will “latch” the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read “until cleared”.

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern (“loop to clear”) - this would also be similar to an Interrupt Service Routine (ISR) “loop to clear” function.

    Ex: Running the ‘loop to clear’ on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are “cleared” and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

  The ISR is typically a software (SW) handling branch (part of host application software) structured to “loop to read and clear” the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should “read” the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were “latched” – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively “re-arm” for the next transition to occur.

  Ex: The ISR should have the ‘loop to clear’ – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also “latch” the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

Appendix (G5)

IEEE 754 Binary Formats

Type	Sign	Exponent	Significand	Total bits	Exponent bias	Bits precision
Half (IEEE 754-2008)	1	5	10	16	15	11
Single	1	8	23	32	127	24
Double	1	11	52	64	1023	53
Quad	1	15	112	128	16383	113

Sign Bit

The sign bit is as simple as it gets. 0 denotes a positive number; 1 denotes a negative number. Flipping the value of this bit flips the sign of the number.

Exponent

The exponent field needs to represent both positive and negative exponents. To do this, a bias is added to the actual exponent in order to get the stored exponent. For IEEE single-precision floats, this value is 127. Thus, an exponent of zero means that 127 is stored in the exponent field. A stored value of 200 indicates an exponent of (200-127), or 73. For reasons discussed later, exponents of -127 (all 0s) and +128 (all 1s) are reserved for special numbers.

For double precision, the exponent field is 11 bits, and has a bias of 1023.

Significand

The significand, also known as the mantissa, represents the precision bits of the number. It is composed of an implicit leading bit and the fraction bits. To find out the value of the implicit leading bit, consider that any number can be expressed in scientific notation in many different ways. For example, the number five can be represented as any of these:

5.00 × 100

0.05 × 102

5000 × 10-3

In order to maximize the quantity of representable numbers, floating-point numbers are typically stored in normalized form. This puts the radix point after the first non-zero digit. In normalized form, five is represented as 5.0 × 100.

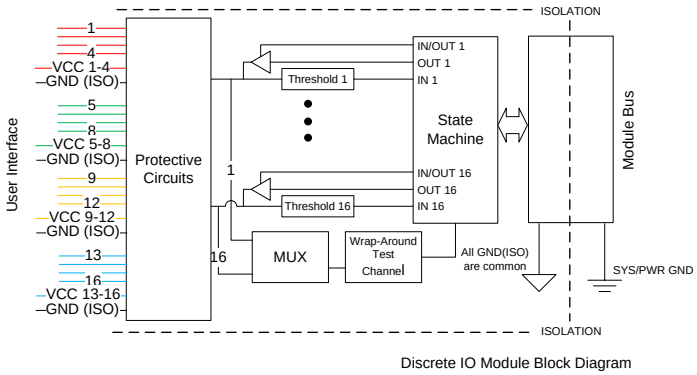
STRAIN GAGE (MODULE G5) VME MODULE MEMORY REGISTER MAP

Module length (size) = 400h

000	Output Data 16-bit	Ch1	R	070	Load cell full scale sensitivity lo	Ch1	R/W
002	Output Data 16-bit	Ch2	R	072	Load cell full scale sensitivity hi	Ch1	R/W
004	Output Data 16-bit	Ch3	R	074	Load cell full scale sensitivity lo	Ch2	R/W
006	Output Data 16-bit	Ch4	R	076	Load cell full scale sensitivity hi	Ch2	R/W
				078	Load cell full scale sensitivity lo	Ch3	R/W
010	Output Data 24-bit lo	Ch1	R	07A	Load cell full scale sensitivity hi	Ch3	R/W
012	Output Data 24-bit hi	Ch1	R	07C	Load cell full scale sensitivity lo	Ch4	R/W
014	Output Data 24-bit lo	Ch2	R	07E	Load cell full scale sensitivity hi	Ch4	R/W
016	Output Data 24-bit hi	Ch2	R				
018	Output Data 24-bit lo	Ch3	R				
01A	Output Data 24-bit hi	Ch3	R	0A0	Chop Enable		R/W
01C	Output Data 24-bit lo	Ch4	R	0A2	Filter Configuration		R/W
01E	Output Data 24-bit hi	Ch4	R				
020	Output Data Force lo	Ch1	R/W				
022	Output Data Force hi	Ch1	R/W	0C0	Busy		R
024	Output Data Force lo	Ch2	R/W	0C2	Bit Open Interval		R/W
026	Output Data Force hi	Ch2	R/W	0C4	Calibration Interval		R/W
028	Output Data Force lo	Ch3	R/W	0C6	Calibration Type		R/W
02A	Output Data Force hi	Ch3	R/W	0C8	Calibration Command		R/W
02C	Output Data Force lo	Ch4	R/W	0CA	Calibration Use Factory Values		R/W
02E	Output Data Force hi	Ch4	R/W	0CC	Calibration Clear User Flash Calibration		R/W
030	Output V/V lo	Ch1	R				
032	Output V/V hi	Ch1	R	0D0	Status BIT		R/W
034	Output V/V lo	Ch2	R	0D2	Status OPEN		R/W
036	Output V/V hi	Ch2	R	0D4	Status ERR		R/W
038	Output V/V lo	Ch3	R				
03A	Output V/V hi	Ch3	R				
03C	Output V/V lo	Ch4	R	0E8	Interrupt Enable BIT		R/W
03E	Output V/V hi	Ch4	R	0EA	Interrupt Enable OPEN		R/W
040	Range	Ch1	R/W	0EC	Interrupt Enable ERR		R/W
042	Range	Ch2	R/W				
044	Range	Ch3	R/W				
046	Range	Ch4	R/W				
048	Remote Sense Select	Ch1	R/W	3B4	Module Design Version		R
04A	Remote Sense Select	Ch2	R/W	3B6	Module Design Revision		R
04C	Remote Sense Select	Ch3	R/W	3B8	Module DSP Revision		R
04E	Remote Sense Select	Ch4	R/W	3BA	Module FPGA Revision		R
050	Excitation Mode	Ch1	R/W	3BC	Module ID		R
052	Excitation Mode	Ch2	R/W				
054	Excitation Mode	Ch3	R/W				
056	Excitation Mode	Ch4	R/W				
058	Excitation Voltage	Ch1	R/W				
05A	Excitation Voltage	Ch2	R/W				
05C	Excitation Voltage	Ch3	R/W				
05E	Excitation Voltage	Ch4	R/W				
060	Load cell sensitivity lo	Ch1	R/W				
062	Load cell sensitivity hi	Ch1	R/W				
064	Load cell sensitivity lo	Ch2	R/W				
066	Load cell sensitivity hi	Ch2	R/W				
068	Load cell sensitivity lo	Ch3	R/W				
06A	Load cell sensitivity hi	Ch3	R/W				
06C	Load cell sensitivity lo	Ch4	R/W				
06E	Load cell sensitivity hi	Ch4	R/W				

I/O DISCRETE (MODULE K6 VER. 4)

Description



Discrete IO Module Block Diagram

Each module provides sixteen channels that are programmable for either Input or Output per channel. When programmed for input, they can be used for either voltage or contact sensing. Channels programmed for input contact sensing can be programmed with either a current source or current sink effectively providing a ‘pull-up’ or ‘pull-down’ for the open condition contact sense - this unique design eliminates the need for external resistors or mechanical jumpers. Instead, this design offers a current source/sink (in banks of 4 channels) that the user programs to a desired current level. An external source VCC must be wired for proper output operation and input operation when requiring a current source/sink. External I/O and/or VCC source GND/Return must be wired for all configurations. When programmed for output, each channel can be set for high-side (current-source), lo-side (current-sink) or push-pull (current-source-sink) operation. Diode clamping is provided (useful for inductive loads, such as relays) and thermal protection. The 16 channels are grouped in an independent isolated GND/Return system (GND) which is isolated from other module and system power GND/Return. Within each isolated GND system, there are (4) external input VCC pins, each providing the source input capability for (4) channels within the associated VCC channel bank.

FEATURES

The following (Ver. 4 - Identified as Module Design Version 4) capabilities are not available on previous versions:

Current share and current/voltage read capabilities.

- Programmable for Input (voltage or contact sensing) or Output (current source, sink or push-pull) per channel/bank
- Continuous Background BIT Testing (during normal operation, status provided for channel health and operation feedback)
- Ability to sense broken input connection and if input is shorted to +V or to ground
- Ability to read I/O voltage and output current for improved diagnostics (indicates if load is connected)
- Ability to current share, by connecting multiple outputs in parallel, to sink/source up to 2A per bank
- Ability to handle high inrush current loads (e.g. two #327 incandescent lamps in parallel)
- Supports ‘dual turn-on’ (series channel output) applications (e.g. dual series ‘key’ missile launch control)

Continuous Background BIT Testing

BIT is always enabled and continually checks that each channel is functioning correctly. This capability is accomplished by internal test circuitry that is incorporated into each 16 channel module. The test circuit is sequentially connected across each channel, checks that the commanded Mode (Input or Output) is correctly set, and then, depending upon the configuration, verifies that the channel data agrees with the test data or a fault is indicated. Additionally, each output is continually checked for over current.

All four threshold levels (On, Off, Short to +V, Short to ground) must be set for each Input or Output channel to validate BIT testing. Testing is totally transparent to the user, requires no external programming, and has no effect on the standard operation of this card. Associated status register(s) can be checked or polled at any given time. To Enable Interrupts, within any interrupt enable register, set the appropriate channel bits to “1”.

Input/Output Format

Each individual channel may be programmed for either input or output. Channel configuration is programmed in groups of 8. Write integer 0 for input; 1, 2 or 3 for specific output format. When configured for Input Contact Sense a pull-up/down current value (> 0 mA) must be programmed. If the current value is set at the default of 0 mA then Voltage sense will be used as Input.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Input/OutputT Ch. 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
Input/OutputT Ch. 09-16	Ch.16		Ch.15		Ch.14		Ch.13		Ch.12		Ch.11		Ch.10		Ch.09		Channel
Input/Output	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT
Integer	D_H	D_L															
0	**0**	**0**	Input														
1	**0**	**1**	Output, Low-side switched, with/without current pull up														
2	**1**	**0**	Output, High-side switched, with/without current pull down														
3	**1**	**1**	Output, push-pull														

Input/Output Interface

The Input/Output (I/O) Interface can be configured in a variety of ways. A pair of drive FETs and current circuits are provided at each I/O pin. See I/O interface diagram below.

Output: When configured as an output, the interface can act as a "High-Side", "Low-Side" or "Push-Pull" drive, providing up to 500ma per channel or 1A when two channels are connected in parallel. The total output per module (16 channels) cannot exceed 8.0 amps (Maximum source current 'rules' for rear I/O connectors still apply – see general specifications).

Input: When configured as an input, output drivers are disabled. I/O interface can act as a current source, current sink or voltage sensing circuit. For contact sensing, set each channel for pull-up or pull-down using the *Pull-Up/Down Current Configuration* register and enter the appropriate current level in the *Current For Sink/Source* register. Define contact closure and hysteresis using Upper and Lower Threshold. See *Read I/O* register to read input signal logic state. *No additional resistors or hardware is required to provide for current flow.* A current value of zero disables the current source/sink circuits and configures for voltage sensing. Default is voltage sensing. Level or contact sensing can be mixed within a channel bank, if the contact sensing channels are *externally* pulled up or pulled down. If this module supplies the current for the contact sensing, then level and contact sensing cannot be mixed within a channel bank.

All four threshold levels must be programmed. For input, threshold levels define logic state. For output, threshold levels are used in BIT test (wrap-around) signal monitoring.

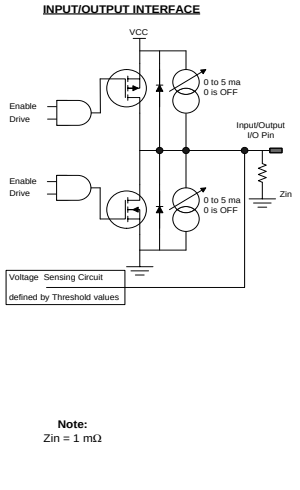


Fig 1

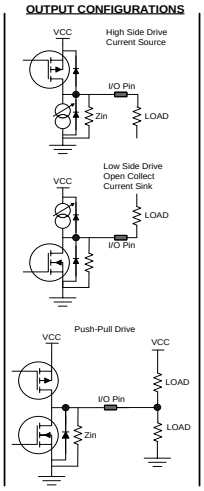


Fig 2

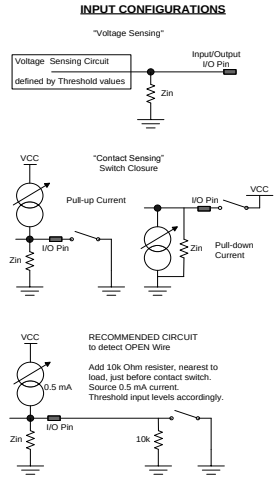


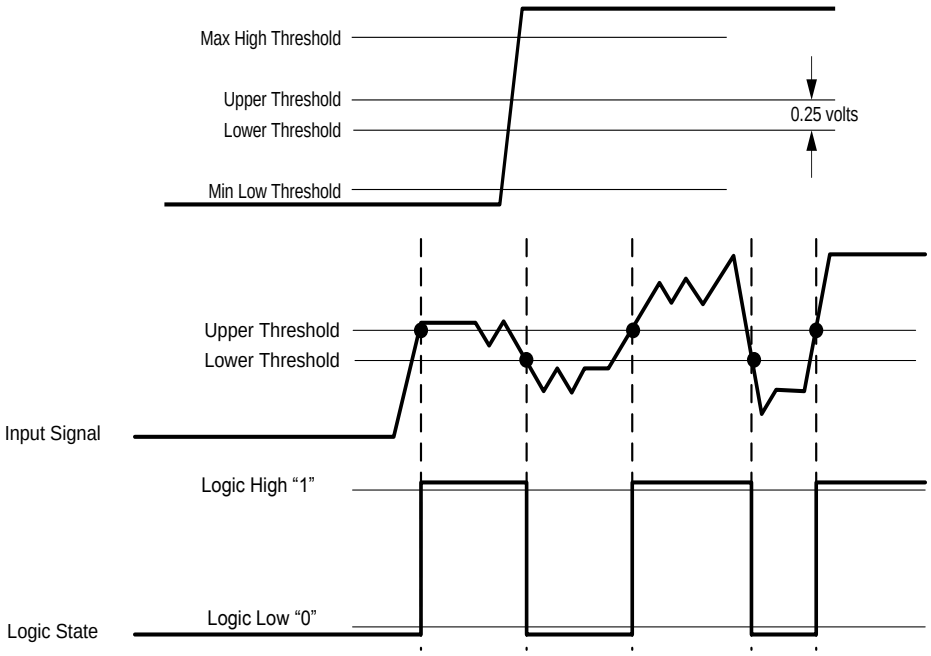
Fig 3

Threshold Programming

Four threshold levels (*Max High, Upper, Lower, Min Low*) offer maximum user flexibility. All four threshold levels must be programmed. For Input or output, the threshold levels will define the logic states. For proper operation, the threshold values should be programmed such that:

Max High Threshold > Upper Threshold > Lower Threshold > Min Low Threshold.

Program Upper and Lower Thresholds, keeping the 0.25V min. differential in mind, and then add de-bounce time as required. When the input signal exceeds the Upper Threshold, a logic high "1" is maintained until the input signal falls below the Lower Threshold. Conversely, when the input signal falls below the Lower Threshold, a logic low "0" is maintained until the input signal rises above the Upper Threshold.



When the input signal exceeds the Upper Threshold, a logic high "1" is maintained until the input signal falls below the Lower Threshold. Conversely, the same is true as the signal changes from low to high, or high to low.

Max High Threshold

Maximum High Threshold is programmable per channel from 0 VDC to 60 VDC, with binary 10-bit word resolution (LSB=100 mv). This assumes that the programmed level is the minimum voltage used to indicate a Max High Threshold. If a signal is greater than the Max High Threshold value, a flag is set in the *Max High Threshold Status register*. The Max High Threshold register may be used to monitor any type of high signal voltage condition or threshold such as a "Short to +V" as it applies to input measurement as well as contact sensing applications.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
							51.2	25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	value in Volts (LSB=100mV)
MAX HIGH THRESHOLD	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Upper Threshold

Upper Threshold is programmable per channel from 0 VDC to 60 VDC, with binary 10-bit word resolution (LSB=100 mv). A signal is considered logic High ("1") when its value exceeds the Upper threshold and does not consequently fall below the Lower threshold in less than the programmed De-bounce time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
							51.2	25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	value in Volts (LSB=100mV)
UPPER THRESHOLD	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Lower Threshold

Lower Threshold is programmable per channel from 0 VDC to 60 VDC, with binary 10-bit word resolution (LSB=100 mv). A signal is considered logic Low ("0") when its value falls below the Lower threshold and does not consequently rise above the Upper Threshold in less than the programmed De-bounce time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
							51.2	25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	value in Volts (LSB=100mV)
LOWER THRESHOLD	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

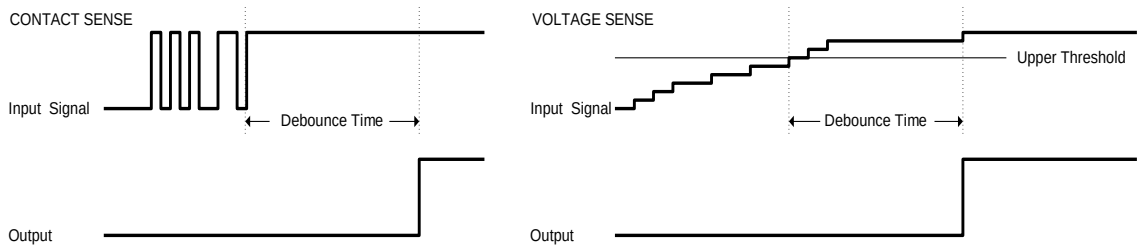
Min Low Threshold

Minimum Low Threshold is programmable per channel 0 VDC to 60 VDC, with binary 10-bit word resolution (LSB=100 mv). This assumes that the programmed level is the maximum voltage used to indicate a Min Low Threshold. If a signal is less than the Min Low Threshold value, a flag is set in the *Min Low Threshold Status register*. The Min Low Threshold register may be used to monitor any type of low signal voltage condition or threshold such as a "Short to Ground" as it applies to input measurement as well as contact sensing applications.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
							51.2	25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	value in Volts (LSB=100mV)
MIN LOW THRESHOLD	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

De-bounce Time

For contact sensing, De-bounce time is much like a glitch filter. Signal pulse widths less than the De-bounce time are filtered or ignored. Once a signal level is stable for a period longer than the De-bounce time (See Upper and Lower Threshold described above), a logic transition is validated. For voltage sensing, the input signal level must exceed its associated threshold for a time greater than the De-bounce time for the logic transition to be validated (See Upper and Lower Threshold described above). Once valid, the interrupt transition register channel flag is set and the output logic changes state. To utilize these features, enter required de-bounce time into the appropriate channel registers. Enter time in 20.48 μs increments, up to (approx) 1.34 seconds. (LSB approximately 20 μs). Value is 15 bits (MSB=don't care). De-bounce defaults to "0" upon reset. Enter a value of "0" to disable De-bounce filtering.



REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	~656	~328	~164	82	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.020	Approximate value in mS (LSB~20.48 µS)
DE-BOUNCE TIME	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Read I/O

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”) as defined by channel threshold values. Each bit of 16-bit binary word corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input Programming Examples

Figure	INPUT/OUTPUT FORMAT 2 bits per channel	Integer	PULL-UP/DOWN Configuration 1 bit per 4-channel bank	Integer	CURRENT FOR SOURCE/SINK One register per 4-channel bank	Integer
4	Input Ch1-8, voltage sensing (default)	0	without current source/sink	X	NO current source (default)	0
5	Input Ch1-8, contact sensing	0	Ch1-8 with current pull up	3	1 ma	10
6	Input Ch1-8, contact sensing	0	Ch1-8 with current pull down	12	2 ma	20
7	Input Ch1-8, OPEN line detect, load is current sink	0	Ch1-8 with current pull up	3	0.5 ma Program Max Upper Threshold[2]	5
6[1]	Input Ch1-8, OPEN line detect, load is current source	0	Ch1-8 with current pull down	12	0.5 ma Program Min Lower Threshold[3]	5

Notes: 1. Figure 6 with 10k ohm resistor nearest load (as in figure 7)

2. $Vcc > T_{mu} > I_{od}R_{od}$, where load is current sinking

3. $T_{ml} < Vcc - I_{od}R_{od}$, where load is current sourcing

Vcc Value

Read Vcc voltage at input pin per four channel bank. Value is binary 10 bit word, where LSB=100 mv. A Vcc applied to the Bank Vcc pin is required except when a channel is configured as an input Voltage Level sensing, or configured as an output where user does not intend to use the programmable pull-up/down current feature.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
							51.2	25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	value in volts (LSB=100mv)
VCC VALUE	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Pull-Up/Down Current Configuration

For contact (switch closure) applications, a current supply (VCC) is required for internal pull-up.

Set bit “1”=to configure Bank to Pull-up, or clear bit “0” to configure Bank to Pull-down. Each data bit configures entire bank of 4 channels. Defaults to “1”; pull-up configuration.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CURRENT CONFIGURATION	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	1=Pull-Up, 0=Pull-Down
D0 configures bank 1, channels 1-4 of that module.																**D**	Configure Ch.01-04
D1 configures bank 2, channels 5-8 of that module.															**D**		Configure Ch.05-08
D2 configures bank 3, channels 9-12 of that module.														**D**			Configure Ch.09-12
D3 configures bank 4, channels 13-16 of that module.													**D**				Configure Ch.13-16

Current for Source/Sink

Program any current from 0 to 5 ma. Programs entire bank; there are 4 channels per bank. For 5ma, enter integer 50. Resolution is 100µa per bit (LSB=100µa). A current value of zero disables the current source/sink circuits and configures for voltage sensing if configured as Input.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
											3.2	1.6	0.8	0.4	0.2	0.1	value in mA (LSB=100µA)
CURRENT	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Examples: Register value is integer:

Register Value	Data Bits			Channel Configuration, Module 1		
	D15-D2	**D1**	**D0**	Ch. 9-16	Ch. 5-8	Ch. 1-4
0	**0000 0000 0000 00 - -**	**0**	**0**	Pull-Down	Pull-Down	Pull-Down
1	**0000 0000 0000 00 - -**	**0**	**1**	Pull- Down	Pull-Down	Pull-Up
2	**0000 0000 0000 00 - -**	**1**	**0**	Pull- Down	Pull-Up	Pull-Down
3	**0000 0000 0000 00 - -**	**1**	**1**	Pull- Down	Pull-Up	Pull-Up

To detect an OPEN line when **contact sensing,** add 10k ohm resistor R_{nl} nearest to load. Program open detect current I_{od} and calculate open contact condition, drop voltage V_{open} at I/O pin. Select sourcing current I_{od} such that drop voltage ΔV is about 80% of Vcc. If open detect resistance R_{od} is the parallel combination of the near load resistance R_{nl} and the circuit input impedance Z_{in}. Then (example, Zin = 105K):

R_{od} = R_{nl} || Z_{in} = 10k || 105k = 9.13 k. 105 K used as example for K6 (v3)

If user provided Vcc is 10v, Must RECALCULATE example for actual Zin

K6 (v4) Zin = 1 MΩ

I_{od} = 0.8 Vcc / R_{od} = 0.8 x 10 / 9.13k = 0.876 mA.

If I_{od} = 1mA, we get open contact condition, drop voltage V_{open} at the I/O pin,

V_{open} = $I_{od}R_{od}$ = .0876 mA x 9.13 kΩ = 8.0 volts.

If load is current sink, Program Maximum Upper Threshold T_{mu} some 20% greater than V_{open} , maintaining

Vcc > T_{mu} > V_{open} > T_{ut}

T_{mu} = 1.2 V_{open} = 1.2 x 8 = 9.6 volts.

Program Upper Threshold T_{ut} 20% less then V_{open}

T_{ut} = 0.8 V_{open} = 0.8 x 8 = 6.4 volts.

Accordingly, program Lower Threshold T_{lt} at 20% Vcc and Minimum Lower Threshold T_{ml} at 10% Vcc

T_{lt} = 0.2 Vcc = 0.2 x 10 = 2 volts.
T_{ml} = 0.1 Vcc = 0.1 x 10 = 1 volts.

To detect a line shorted to either ground or Vcc when contact sensing, continuing with this example, the user needs to add series resistance nearest to load, Rs, and calculate closed contact condition, drop voltage V_{closed} at I/O pin. Resistance nearest to load, R_s, should be negligible as compared to the near load resistance R_{nl} but at least a magnitude greater than any resistance due to wire length. A value of 150 ohms would be appropriate for Rs. Then:

V_{closed} = $I_{od}R_s$ = 0.876 mA x 0.15 kΩ = 0.13 volts.

Program Lower Threshold T_{mu} greater than V_{closed} maintaining

Vcc >> T_{lt} > V_{closed} > T_{ml} > 0

T_{lt} > 1.2 V_{closed} > 1.2 x 0.13 = 0.156 volts.

Program Minimum Lower Threshold T_{ut} 20% less than V_{open}

T_{ml} < 0.8 V_{closed} < 0.8 x 0.13 = 0.1 volts.

In general,

$Vcc > T_{mu} > V_{open} > T_{ut} > T_{lt} > V_{closed} > T_{ml} > 0$, $T_{ut} - T_{lt} \geq 0.25mV$ for hysteresis configuration

To detect a Short to Vcc, Program Maximum Upper Threshold T_{mu} where

$Vcc > T_{mu} > V_{loadmax}$ where $V_{loadmax}$ is the maximum voltage potential on the I/O pin.

To detect a Short to Ground, Program Minimum Lower Threshold T_{ml} where

$Vcc > > V_{loadmin} > T_{ml}$ where $V_{loadmin}$ is the minimum voltage potential on the I/O pin.

Consider the following programming options:

Output Programming Examples

Figure	INPUT/OUTPUT FORMAT 2 bits per channel	Integer	PULL-UP/DOWN Configuration 1 bit per 4-channel bank	Integer	CURRENT FOR SOURCE/SINK One register per 4-channel bank	Integer
1	Output Ch1, High Side Drive	2	without current pull down	X	NO current source	0
1	Output Ch1-4, High Side Drive	170	Ch1-4 with current pull down[1]	14	1 ma	10
1	Output Ch5-8, High Side Drive	43520	Ch5-8 with current pull down[1]	13	2 ma	20
1	Output Ch1-8, High Side Drive	43690	Ch1-8 with current pull down[1]	12	2 ma	20
2	Output Ch1, Low Side Drive	1	without current pull up	X	NO current source	0
2	Output Ch1-4, Low Side Drive	85	Ch1-4 with current pull up[1]	1	1 ma	10
2	Output Ch1-8, Low Side Drive	21845	Ch1-8 with current pull up[1]	3	2 ma	20
3	Output Ch1, Push-Pull	3	Not Applicable – DON'T CARE	X	Not Applicable – DON'T CARE	X

Note 1: Use current source for Wired-OR or other related applications.

Write Output

When a channel is configured for Output, write logic level High ("1") or Low ("0") to associated channel bit, in 16 bit binary word. Each bit corresponds to one of 16 channels (See Register Bit Map.) Output logic is defined by the provided Vcc voltage to that channel bank. There are four channels per bank (See ***Front and Rear Panel Connectors*** section).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Current Share Configuration

Multiple channels, from the same current bank, may be connected together to sink/source a greater cumulative current. Channel, bank and motherboard current rules must be adhered to (0.5A max per channel, 2A max per bank, 8A max per module (4A max if utilizing rear I/O connections). Write the appropriate value to the current share configuration register for implementing channel share output configuration per bank.

(BANK reference)	BANK 4				BANK 3				BANK 2				BANK 1				
REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CURRENT SHARE CONFIGURATION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Write the (4) bit-pattern channel configuration for the associated channel bank to set channel share configuration required:

Channel Current Share Configuration	BIT PATTERN	Comments
All (4) channels individual configuration (no share)	0000	Default
Channels 1 - 2 shared (Channels 3, 4 individual)	0010	
Channels 3 - 4 shared (Channels 1, 2 individual)	1000	
Channels 1 - 2 and Channels 3 - 4 shared	1010	
Channels 1 - 3 shared (Channel 4 individual)	0110	
Channels 1 - 4 shared (NO channels individual)	1111	

Read Output Voltage

Read actual output voltage at I/O pin per individual channel. Value is an unsigned binary 16 bit word, where LSB=100 mv. For example, if output voltage word is 0x00F0 (240d), actual voltage is 24.0 V.

Read Output Current

Read actual output current at I/O pin per individual channel. Value is signed binary 16 bit word, where LSB=3 mA. Read as 2's complement; Current source is positive, Current sink is negative. For example, if output voltage word is 0x0064 (100d), actual current is (current source) 300mA. For negative (current sink), (-) 300 mA would read as 0xFF9C (-100d).

Reset Over-Current

Write integer "1" to reset all sixteen channels (per module). This register is used to reset disabled channel(s) set to tri-state following an over-current condition. When reset process is complete, processor will write a "0" back to the *Reset Over-Current* register. Card will respond to a Reset command after one second.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESET OVER-CURRENT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	D=DATA BIT

Status Indications

The following status conditions can be monitored:

Fault: When the test circuit does not agree with the data read or data write, a fault status bit will be set within three seconds. A fault bit will remain latched until read.

Over-current: If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs.

Max High Threshold: If the signal exceeds this threshold, status is indicated (bit is set) within 500µs.

Min Low Threshold: If the signal falls below this threshold, status is indicated (bit is set) within 500µs.

Lo-Hi Transition: If a Lo to High transition is sensed, status is indicated (bit is set) within 40µs.

Hi-Low Transition: If a High to Low transition is sensed, status is indicated (bit is set) within 40µs.

Mid-Range: When the signal is in-between the Upper and Lower thresholds, status is indicated (bit set) within 500µs.

When status is "indicated," or bit is "set," bit value is logic "1." Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Max Hi Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Min Lo Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Mid-Range	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Interrupt Enable

To enable interrupts, set bit to '1' for the corresponding channel to be monitored. Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Max Hi Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Min Lo Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Mid-Range Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Interrupt Vectors

The Interrupt Vector Registers store the vectors for the specific interrupts generated by the module. When an interrupt is enabled and occurs, the contents of the corresponding Interrupt Vector register is the value that is reported to the user:

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Interrupt Vector BIT	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
Max Hi Threshold Interrupt Vector	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
Max Lo Threshold Interrupt Vector	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
Mid Range Threshold Interrupt Vector	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
Over-current Interrupt Vector	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
Interrupt Vector Lo-Hi Transition	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
Interrupt Vector Hi-Lo Transition	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding "latching" – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are "latching"; as defined, any noted transitional change on any channel will "latch" the entire Status Register.
- Once latched, there will be no further state change "sensed" by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will "unlatch" that particular status register (doesn't necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will "latch" the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read "until cleared".

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern ("loop to clear") - this would also be similar to an Interrupt Service Routine (ISR) "loop to clear" function.

    Ex: Running the 'loop to clear' on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are "cleared" and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

  The ISR is typically a software (SW) handling branch (part of host application software) structured to "loop to read and clear" the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should "read" the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were "latched" – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively "re-arm" for the next transition to occur.

  Ex: The ISR should have the 'loop to clear' – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also "latch" the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

I/O Discrete (Module K6) – Addendum A (PWM Enhanced Function)

Description

A new feature (termed “PWM/Timer Mode”) for the K6 (ver. 4) (**GEN3 and higher platforms only**) has been implemented (applies to platforms with DOM code 1327 (year-week) and higher - **PWM support presently applies only to K6 version 4 (rev D) with K6 FPGA rev 5 or later (may be queried from card)**). This new feature will provide an ‘automatic’ signal output (pulse train), based upon a programmable period and “on-time”. The PWM control capability will allow the user/programmer to initialize/trigger/control automatic pulse train generation from the K6 channel(s) which greatly reduces software control overhead.

The purpose of this enhanced function addendum is to provide detailed information to understand and utilize the new enhanced function proposed expressly for the K6 module discrete I/O output channel operation. The new function is termed “PWM/Timer Mode” and the definition and operation is contained within this document.

Features

- Programmable PWM/Timer period (sets total pulse period)
- Programmable PWM/Timer pulse width (sets pulse on-time)
- Programmable PWM/Timer polarity (on-time “high” or “low” definition)
- Programmable PWM/Timer mode select (feature “ON” or “OFF”)
- Programmable PWM/Timer mode enable (trigger)

Operational Control Registers:

By default, the card is powered-up in the “normal” mode (meaning standard operation of all channels). Reference the Specification/Operation Manual of the appropriate platforms.

Note: It is recommended that ‘default’ operational parameters are not ‘relied’ upon power-up and any/all functional parameters/settings are initialized.

Note: Function register offsets provided are for VME 16-bit data addressing. For cPCI/PCI/PCIe/SRIO 32-bit addressing, multiply the noted listed/defined register offsets by 2.

Operational notes/considerations:

High or Low side drive modes is recommended (with appropriate internal or external pull down/up respectively) if precise timing is required or for relatively short duration pulses <100 usec.

Push-pull mode may be utilized, however, due to implementation of a non-driven safety period required to preclude conflicting push/pull drive (break-before-make), the output is left “un-driven” for a period of approximately 80 usec. on each (H-L) or (L-H) transition.

For any drive mode (low-side, high-side (w/ appropriate pull-up/down) or push-pull); when the polarity bit is set to “0” (default) the pulse width will be defined as low-going. When the polarity bit is set to “1” the pulse width will be defined as high-going. This function is also related to “PWM/Timer Period and Pulse Width”. (Reference figure (1.), Timing Diagram).

If an internal or external *pull-up* is present while programmed for push-pull mode, pulse timing changes, due to the @ 80 usec. transitional safety timing buffer, will result in an increased pulse period duration of @ 160 usec. for high-going polarity (1) pulses and a decreased @ 160 usec. duration for low-going polarity (0) pulses. Conversely, if an internal/external *pull-down* is present, polarity (1) pulses will be decreased in duration by @ 160 usec. and polarity (1) pulse periods will be increased in duration by @ 160 usec.

Note: If push-pull mode is utilized and no internal/external pull up/down is present, the transition edges may appear "distorted" due to the lack of drive during the non-driven safety period. If the pulse width setting approaches the transition buffer (80 usec. non-driven safety period) time there may be irregular output of the pulses. For these settings, the high or low side drive mode/configuration is recommended.

Note: BIT fault reporting may appear under certain conditions when operating in the PWM/Timer output mode and the pulse output timing results in the set output state target not being met for the BIT trigger timing duration. This should be considered normal and the BIT status ignored or masked. Alternatively, the BIT status may be suppressed by setting the output state selection to the opposite sate of the I/O format configuration (e.g. Set the output state "High" for Low-Side configuration' or vice versa).

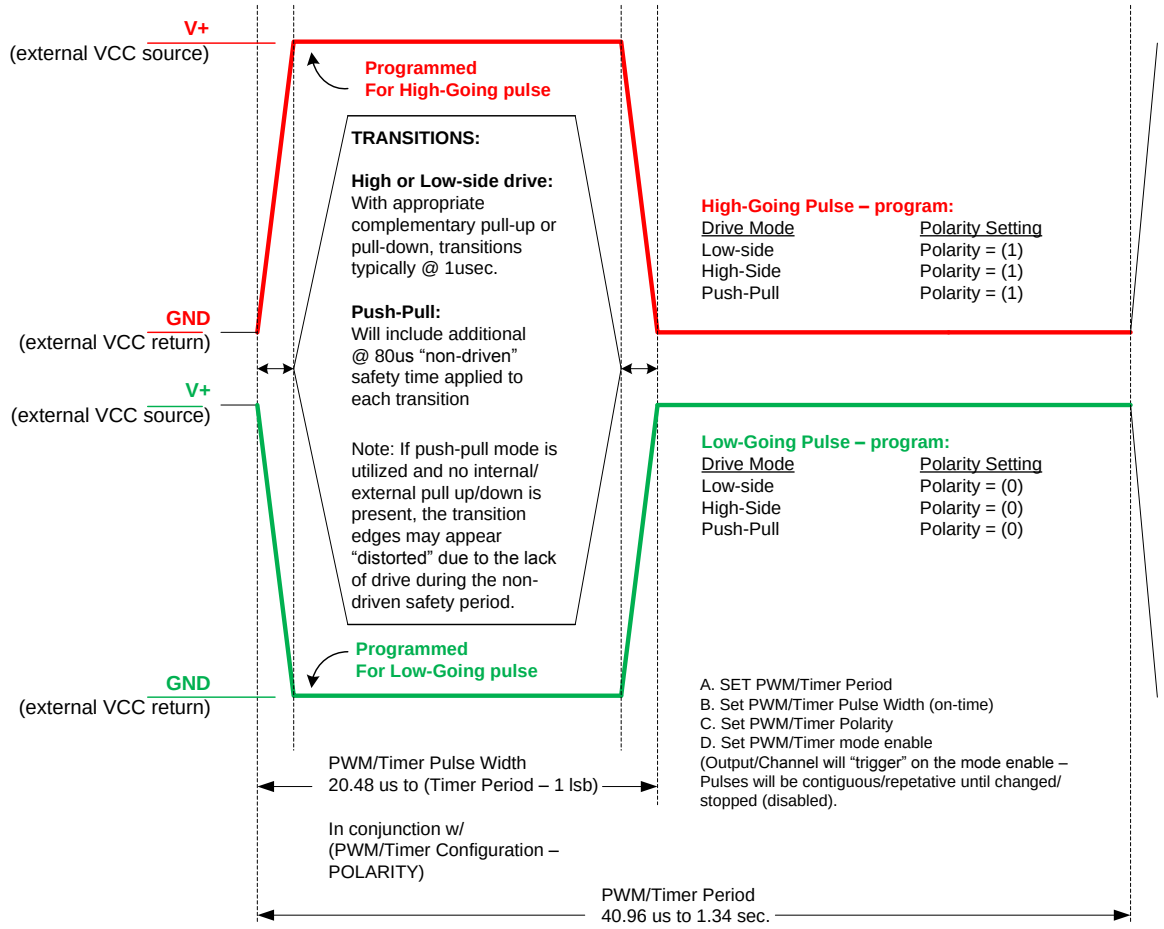


Figure 1. (Timing Diagram)

PWM/Timer Period

Initialize this register with the required full signal period. LSB is 20.48 usec. Range is 0x0002 to 0xFFFF (40.96 usec to 1.34 sec.). (see figure 1. Timing Diagram).

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PWM/Timer Period, CHx	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Register Offset	Description	Type	Power On / Reset Default	Remarks
0x0200	Timer Period, CH1	W/R	0x0000	
0x0202	Timer Period, CH2	W/R	0x0000	
0x0204	Timer Period, CH3	W/R	0x0000	
0x0206	Timer Period, CH4	W/R	0x0000	
0x0208	Timer Period, CH5	W/R	0x0000	
0x020A	Timer Period, CH6	W/R	0x0000	
0x020C	Timer Period, CH7	W/R	0x0000	
0x020E	Timer Period, CH8	W/R	0x0000	
0x0210	Timer Period, CH9	W/R	0x0000	
0x0212	Timer Period, CH10	W/R	0x0000	
0x0214	Timer Period, CH11	W/R	0x0000	
0x0216	Timer Period, CH12	W/R	0x0000	
0x0218	Timer Period, CH13	W/R	0x0000	
0x021A	Timer Period, CH14	W/R	0x0000	
0x021C	Timer Period, CH15	W/R	0x0000	
0x021E	Timer Period, CH16	W/R	0x0000	

PWM/TIMER Pulse Width

Sets the pulse width (on-time) of the PWM signal period. LSB is 20.48 usec.

Range is 0x0001 to (***Timer Period*** set – 1).

This function is also related to “PWM/Timer Period and Configuration (Polarity)”. (See figure 1. Timing Diagram).

REGISTER BIT MAP

	D1	D1	D1	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PWM/Timer Pulse Width, CHx	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Register Offset	Description	Type	Power On / Reset Default	Remarks
0x01A0	PWM/TIMER Pulse Width, CH1	W/R	0x0000	
0x01A2	PWM/TIMER Pulse Width, CH2	W/R	0x0000	
0x01A4	PWM/TIMER Pulse Width, CH3	W/R	0x0000	
0x01A6	PWM/TIMER Pulse Width, CH4	W/R	0x0000	
0x01A8	PWM/TIMER Pulse Width, CH5	W/R	0x0000	
0x01AA	PWM/TIMER Pulse Width, CH6	W/R	0x0000	
0x01AC	PWM/TIMER Pulse Width, CH7	W/R	0x0000	
0x01AE	PWM/TIMER Pulse Width, CH8	W/R	0x0000	
0x01B0	PWM/TIMER Pulse Width, CH9	W/R	0x0000	
0x01B2	PWM/TIMER Pulse Width, CH10	W/R	0x0000	
0x01B4	PWM/TIMER Pulse Width, CH11	W/R	0x0000	
0x01B6	PWM/TIMER Pulse Width, CH12	W/R	0x0000	
0x01B8	PWM/TIMER Pulse Width, CH13	W/R	0x0000	
0x01BA	PWM/TIMER Pulse Width, CH14	W/R	0x0000	
0x01BC	PWM/TIMER Pulse Width, CH15	W/R	0x0000	
0x01BE	PWM/TIMER Pulse Width, CH16	W/R	0x0000	

PWM/TIMER Configuration (Polarity)

Sets the polarity of the pulse width (on-time) of the PWM signal period. When the polarity bit is set to “0” (default), low side, high side (w/ appropriate pull-down) and push-pull modes, the pulse width will be defined as low-going. When the polarity bit is set to “1” , high side, low side (w/ appropriate pull-up) and push-pull modes, the pulse width will be defined as high-going.

This function is also related to “PWM/Timer Period and Pulse Width”. (See figure 1. Timing Diagram).

REGISTER BIT MAP

													Reserved	Reserved	Reserved	Polarity
	D1	D1	D1	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PWM/Timer Configuration	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D

Register Offset	Description	Type	Power On / Reset Default	Remarks
0x01C0	PWM/Timer Config. (Polarity), CH1	W/R	0x0000	
0x01C2	PWM/Timer Config. (Polarity), CH2	W/R	0x0000	
0x01C4	PWM/Timer Config. (Polarity), CH3	W/R	0x0000	
0x01C6	PWM/Timer Config. (Polarity), CH4	W/R	0x0000	
0x01C8	PWM/Timer Config. (Polarity), CH5	W/R	0x0000	
0x01CA	PWM/Timer Config. (Polarity), CH6	W/R	0x0000	
0x01CC	PWM/Timer Config. (Polarity), CH7	W/R	0x0000	
0x01CE	PWM/Timer Config. (Polarity), CH8	W/R	0x0000	
0x01D0	PWM/Timer Config. (Polarity), CH9	W/R	0x0000	
0x01D2	PWM/Timer Config. (Polarity), CH10	W/R	0x0000	
0x01D4	PWM/Timer Config. (Polarity), CH11	W/R	0x0000	
0x01D6	PWM/Timer Config. (Polarity), CH12	W/R	0x0000	
0x01D8	PWM/Timer Config. (Polarity), CH13	W/R	0x0000	
0x01DA	PWM/Timer Config. (Polarity), CH14	W/R	0x0000	
0x01DC	PWM/Timer Config. (Polarity), CH15	W/R	0x0000	
0x01DE	PWM/Timer Config. (Polarity), CH16	W/R	0x0000	

PWM/TIMER Mode Select

Sets output channel mode operation – either standard (responds to the standard ‘write output’ control) or PWM/Timer mode ‘automatic’ pulse output based on PWM/Timer initialization registers. Bit mapped per channel. When channel bit is set to “0” (default), the “respective channel will respond to ‘standard’ write output control. When channel bit is set to “1”, the respective channel will respond to PWM/Timer control pattern programmed accordingly.

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PWM/Timer Mode	Ch.16	Ch.15	Ch.1	Ch.1	Ch.1	Ch.1	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Register Offset	Description	Type	Power On / Reset Default	Remarks
0x01E0	PWM/Timer Mode Select	W/R	0x0000	

PWM/TIMER Mode Enable

Enables (triggers) the start or disables of output channel PWM/Timer mode operation. Bit mapped per channel. When channel bit is set to "1", the "respective channel will respond and start/continue output based on the programmed PWM/Timer pattern. When channel bit is set to "0", the respective channel will stop outputting the PWM/Timer control pattern (clean stop at the end of the period). May be used to 'synchronize' the start of multiple channels if desired.

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PWM/Timer Mode	Ch.16	Ch.15	Ch.1	Ch.1	Ch.1	Ch.1	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Register Offset	Description	Type	Power On / Reset Default	Remarks
0x01E2	PWM/Timer Mode Enable	W/R	0x0000	

Register Summary

Reference the Specification/Operation Manual (for the specific GEN3 or greater board support platform) for general operation and basic register function/offset guidelines – this document acts as an adendum where identified for the PWM/Timer additional functional operation. Note: register offsets provided are VME 16-bit addressed; for cPCI/PCI/PCIe/SRIO 32-bit addressing, multiply offsets by 2.

Register Offset	Description	Type	Power On / Reset Default	Remarks
0x0200 – 0x021E	PWM/Timer Period	R/W	0x0000	Individual channel registers Sets the PWM/Timer period
0x01A0 – 0x01BE	PWM/Timer Period Pulse Width (on-time)	R/W	0x0000	Individual channel registers Sets the PWM/Timer period 'on-time'
0x01C0 – 0x01DE	PWM/Timer Polarity	R/W	0x0000	Individual channel registers Defines the PWM/Timer period 'on-time' polarity
0x01E0	PWM/Timer mode select	W/R	0x0000	Bit-mapped per channel Sets either 'standard' write mode or PWM/Timer output control
0x01E2	PWM/Timer mode enable (trigger)	W/R	0x0000	Bit mapped per channel Starts/Stops the PWM/Timer pulse train

Operational Notes (General)

Recommended Initialization/Programming sequence:

1. Set PWM/Timer Period
2. Set PWM/Timer Pulse Width (on-time)
3. Set PWM/Timer Polarity
4. Set PWM/Timer mode select
5. Set PWM/Timer mode enable

The new function will allow for run-time PWM/Timer period and pulse width changes if desired. If used in this manner, ensure that the new programmed period and pulse width settings are within the respective ranges. For example, if changing to a smaller period, ensure the pulse width is changed first so that the new value does not exceed the new period time base programmed. If changing to a larger pulse width, ensure the time period is not exceeded. PWM/Timer Period and Pulse Width are 'buffered', meaning that run time programming changes can be effectively managed and will take effect at the end of the previous/current programmed period.

DISCRETE (MODULE K6 VER. 4) VME MODULE MEMORY REGISTER MAP

000	Write Output	Ch.01-16	R/W	072	Max High Threshold	Ch.12	R/W	140	Voltage Reading	Ch.01	R
002	Read I/O	Ch.01-16	R	074	Upper Threshold	Ch.12	R/W	142	Voltage Reading	Ch.02	R
				076	Lower Threshold	Ch.12	R/W	144	Voltage Reading	Ch.03	R
004	Max High Threshol	Ch.01	R/W	078	Min Low Threshold	Ch.12	R/W	146	Voltage Reading	Ch.04	R
006	Upper Threshold	Ch.01	R/W	07A	De-bounce time	Ch.12	R/W	148	Voltage Reading	Ch.05	R
008	Lower Threshold	Ch.01	R/W	07C	Max High Threshold	Ch.13	R/W	14A	Voltage Reading	Ch.06	R
00A	Min Low Threshold	Ch.01	R/W	07E	Upper Threshold	Ch.13	R/W	14C	Voltage Reading	Ch.07	R
00C	De-bounce time	Ch.01	R/W	080	Lower Threshold	Ch.13	R/W	14E	Voltage Reading	Ch.08	R
00E	Max High Threshold	Ch.02	R/W	082	Min Low Threshold	Ch.13	R/W	150	Voltage Reading	Ch.09	R
010	Upper Threshold	Ch.02	R/W	084	De-bounce time	Ch.13	R/W	152	Voltage Reading	Ch.10	R
012	Lower Threshold	Ch.02	R/W	086	Max High Threshold	Ch.14	R/W	154	Voltage Reading	Ch.11	R
014	Min Low Threshold	Ch.02	R/W	088	Upper Threshold	Ch.14	R/W	156	Voltage Reading	Ch.12	R
016	De-bounce time	Ch.02	R/W	08A	Lower Threshold	Ch.14	R/W	158	Voltage Reading	Ch.13	R
018	Max High Threshold	Ch.03	R/W	08C	Min Low Threshold	Ch.14	R/W	15A	Voltage Reading	Ch.14	R
01A	Upper Threshold	Ch.03	R/W	08E	De-bounce time	Ch.14	R/W	15C	Voltage Reading	Ch.15	R
01C	Lower Threshold	Ch.03	R/W	090	Max High Threshold	Ch.15	R/W	15E	Voltage Reading	Ch.16	R
01E	Min Low Threshold	Ch.03	R/W	092	Upper Threshold	Ch.15	R/W				
020	De-bounce time	Ch.03	R/W	094	Lower Threshold	Ch.15	R/W	160	Current Reading	Ch.01	R
022	Max High Threshold	Ch.04	R/W	096	Min Low Threshold	Ch.15	R/W	162	Current Reading	Ch.02	R
024	Upper Threshold	Ch.04	R/W	098	De-bounce time	Ch.15	R/W	164	Current Reading	Ch.03	R
026	Lower Threshold	Ch.04	R/W	09A	Max High Threshold	Ch.16	R/W	166	Current Reading	Ch.04	R
028	Min Low Threshold	Ch.04	R/W	09C	Upper Threshold	Ch.16	R/W	168	Current Reading	Ch.05	R
02A	De-bounce time	Ch.04	R/W	09E	Lower Threshold	Ch.16	R/W	16A	Current Reading	Ch.06	R
02C	Max High Threshold	Ch.05	R/W	0A0	Min Low Threshold	Ch.16	R/W	16C	Current Reading	Ch.07	R
02E	Upper Threshold	Ch.05	R/W	0A2	De-bounce time	Ch.16	R/W	16E	Current Reading	Ch.08	R
030	Lower Threshold	Ch.05	R/W					170	Current Reading	Ch.09	R
032	Min Low Threshold	Ch.05	R/W	0A4	Input/Output Format	Ch.01-08	R/W	172	Current Reading	Ch.10	R
034	De-bounce time	Ch.05	R/W	0A6	Input/Output Format	Ch.09-16	R/W	174	Current Reading	Ch.11	R
036	Max High Threshold	Ch.06	R/W					176	Current Reading	Ch.12	R
038	Upper Threshold	Ch.06	R/W	0A8	Current For Sink/Source, Bank 1	Ch.01-04	R/W	178	Current Reading	Ch.13	R
03A	Lower Threshold	Ch.06	R/W	0AA	Current For Sink/Source, Bank 2	Ch.05-08	R/W	17A	Current Reading	Ch.14	R
03C	Min Low Threshold	Ch.06	R/W	0AC	Current For Sink/Source, Bank 3	Ch.09-12	R/W	17C	Current Reading	Ch.15	R
03E	De-bounce time	Ch.06	R/W	0AE	Current For Sink/Source, Bank 4	Ch.13-16	R/W	17E	Current Reading	Ch.16	R
040	Max High Threshold	Ch.07	R/W								
042	Upper Threshold	Ch.07	R/W	0B0	Pull Up/Down Current Config	Ch.01-16	R/W	3E0	BIT Interrupt Vector	Ch.01-16	R/W
044	Lower Threshold	Ch.07	R/W	0B2	Current Share Config	Ch.01-16	R/W	3E2	Max Hi Threshold Interrupt Vector		R/W
046	Min Low Threshold	Ch.07	R/W	0B4	Vcc Value, Bank 1	Ch.01-04	R	3E4	Min Low Threshold Interrupt Vector		R/W
048	De-bounce time	Ch.07	R/W	0B6	Vcc Value, Bank 2	Ch.05-08	R	3E6	Mid Range Threshold Interrupt Vector		R/W
04A	Max High Threshold	Ch.08	R/W	0B8	Vcc Value, Bank 3	Ch.09-12	R	3C2	Over-current Interrupt Vector		R/W
04C	Upper Threshold	Ch.08	R/W	0BA	Vcc Value, Bank 4	Ch.13-16	R	3C4	Low-Hi Transition Interrupt Vector		R/W
04E	Lower Threshold	Ch.08	R/W	0BC	Reset Over-Current	Ch.01-16	R/W	3C6	Hi-Low Transition Interrupt Vector		R/W
050	Min Low Threshold	Ch.08	R/W								
052	De-bounce time	Ch.08	R/W	0D0	Status Fault	Ch.01-16	R	3B4	Module Design Version		R
054	Max High Threshold	Ch.09	R/W	0D4	Status Over-Current	Ch.01-16	R	3B6	Module Design Revision		R
056	Upper Threshold	Ch.09	R/W	0D6	Status Max Hi Threshold	Ch.01-16	R	3B8	Module DSP		R
058	Lower Threshold	Ch.09	R/W	0D8	Status Min Lo Threshold	Ch.01-16	R	3BA	Module FPGA		R
05A	Min Low Threshold	Ch.09	R/W	0DA	Status Mid Range	Ch.01-16	R	3BC	Module ID		R
05C	De-bounce time	Ch.09	R/W	0DC	Status Lo-Hi Transition	Ch.01-16	R				
05E	Max High Threshold	Ch.10	R/W	0DE	Status Hi-Lo Transition	Ch.01-16	R				
060	Upper Threshold	Ch.10	R/W								
062	Lower Threshold	Ch.10	R/W	0E8	Interrupt Fault Enable	Ch.01-16	R/W				
064	Min Low Threshold	Ch.10	R/W	0EC	Interrupt Over-Current Enable	Ch.01-16	R/W				
066	De-bounce time	Ch.10	R/W	0EE	Interrupt Max Hi Threshold Enable	Ch.01-16	R/W				
068	Max High Threshold	Ch.11	R/W	0F0	Interrupt Min Lo Threshold Enable	Ch.01-16	R/W				

06A	Upper Threshold	Ch.11	R/W	0F2	Interrupt Mid-Range Fault Enable	Ch.01-16	R/W			
06C	Lower Threshold	Ch.11	R/W	0F4	Interrupt Lo-Hi Transition Enable	Ch.01-16	R/W			
06E	Min Low Threshold	Ch.11	R/W	0F6	Interrupt Hi-Lo Transition Enable	Ch.01-16	R/W			
070	De-bounce time	Ch.11	R/W							

Note: Highlighted functionality available on K6 ver. 4 or later.

I/O DISCRETE (MODULE K7)

Description

Each module provides 16 isolated channels. Each channel is independently programmable and may be used for input voltage measurements or as a bi-directional switch. Programmed as voltage input, a channel can be used to measure differential bipolar input voltages of up to ±80V. Programmed as a switch and with the switch closed, both the current through, and voltage across the switch may be monitored.

The K7 Module includes diode clamping on each channel. Clamping is useful for inductive loads, such as relays and short circuit protection. Channel I/O signals are individually isolated from each other, from system power and ground.

Features

- Programmable for Input voltage or switch closure for each channel
- Continuous background built-in-test (BIT) (during normal operation, status provided for channel health and operation feedback)
- Ability to read switch I/O voltage and current
- Ability to handle switch closure currents of up to 600ma DC
- Automatic switch over-current protection @ 600ma
- Supports 'dual turn-on' (series channel output) applications (e.g. dual series 'key' missile launch control)
- Clean, bounce-free switching

Principles of Operation

Each module incorporates 16 independently programmable channels. All 16 channels have I/O connections that are available through the front panel connector (12 channels are available via rear connector). Each channel consists of two bipolar I/O pins. All 16 channels are galvanically isolated from each other and from system ground. Each channel's two-wire connection can function as an isolated voltage input or as an isolated bi-directional switch. When programmed to function as a bi-directional switch, a channel can control valves mechanical relays, indicators, etc. without concern about grounding. This module provides an automatic background built-in-test (BIT) for each channel. The BIT functions are always enabled and continually check that each channel is functioning properly.

Standard input operation is used for voltage sensing and measures both AC and DC input voltages. When operating as a switch, measurements for both voltage across and current through the switch closure are available. *Current* and *Voltage* measurements are available as both instantaneous and averaged (RMS).

Four input voltage threshold levels (Max High, Upper, Lower, Min Low) are programmed to user defined high and low voltage levels. All four of the threshold levels must be set for each Input or Output channel and are used to validate BIT testing. Threshold crossing may be programmed to generated interrupts on a change of state.

The module design utilizes state of the art galvanic isolation that is superior to alternatives such as optocoupler devices. The galvanic isolation eliminates typical optocoupler design concerns such as uncertain current transfer ratios, nonlinear transfer functions and temperature/lifetime degradation effects.

Continuous Background Built-in-Test (BIT)

BIT is always enabled, and continually checks the health of each channel.This is accomplished by internal test circuitry that is incorporated into each 16-channel module. The test circuit is sequentially connected across each channel and checks that the commanded mode (input or switch closure) is correctly set, and depending upon the configuration, verifies that the channel data agrees with the test data or a possible fault is detected. Additionally, each output is continually checked for over-current. Over-current is controlled by firmware and set by design at 600ma.

Input/Switch Interface

The channel contains a both an isolated differential amplifier and a dual N-Channel MOSFET, configured as isolated Solid State Relay (SSR). The channel can be configured ether for voltage measurement or switch closure. In voltage mode, an isolated differential amplifier measures the voltage between the channels two I/O pins. When programmed as a switch the SSR is energized, and both AC and DC current can flow through the channels I/O pins. The MOSFET presents a low ~.5 Ω on impedance. The K7 module contains circuitry to measure the current through the SSR and the voltage present on the I/O pins.

Switch Control

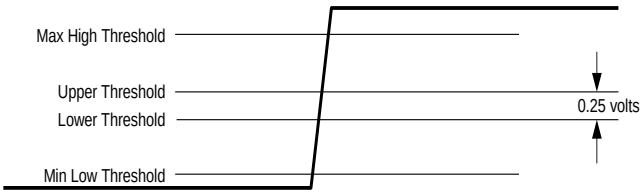
Each individual channel may be programmed for either input or switch closed. When set to '1' the I/O pin pair is configured as closed switch. Each bit corresponds to one of 16 channels (See Register Bit Map.)

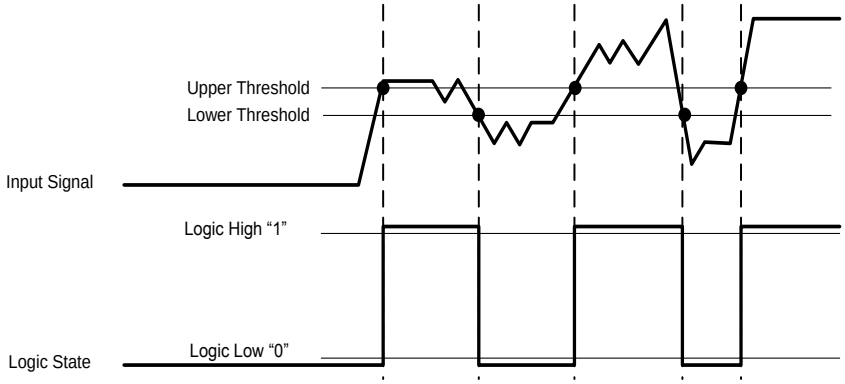
REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
Switch Control	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Threshold Programming

There are four threshold levels (*Max High, Upper, Lower, Min Low*) together they offer maximum user programming flexibility. All four threshold levels must be programmed. The Threshold logic in the K7 module measures the input RMS voltage value. The averaged RMS value is absolute value, and the threshold logic works with DC or AC input voltages. The threshold programming values are represented as an unsigned binary.
The threshold levels will define the logic states. For proper operation, the threshold values should be programmed where: **Max High Threshold > Upper Threshold > Lower Threshold > Min Low Threshold.**

Program Upper and Lower Thresholds, keeping the 0.25V min. differential in mind, and then add de-bounce time as required. When the input signal exceeds the Upper Threshold, logic level high "1" is maintained until the input signal falls below the Lower Threshold. Conversely, when the input signal falls below the Lower Threshold, logic level low "0" is maintained until the input signal rises above the Upper Threshold.





When the input signal exceeds the Upper Threshold, a logic high "1" is maintained until the input signal falls below the Lower Threshold. Conversely, the same is true as the signal changes from low to high, or high to low.

Max High Threshold

Maximum High Threshold is programmable per channel from 0Vrms to 80Vrms, with binary 10-bit word resolution (LSB=163mv). This assumes that the programmed level is the minimum voltage used to indicate a Max High Threshold. If a signal is greater than the Max High Threshold value, a flag is set in the *Max High Threshold Status register*. The Max High Threshold register may be used to monitor any type of high signal voltage condition or threshold such as a "Short to +V" as it applies to input measurement as well as contact sensing applications.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
							83.456	41.728	20.864	10.432	5.216	2.608	1.304	.652	.326	.163	value in Vrms
MAX HIGH THRESHOLD	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Upper Threshold

Upper Threshold is programmable per channel from 0Vrms to 80Vrms, with binary 10-bit word resolution (LSB=163mv). A signal is considered logic High ("1") when its value exceeds the Upper threshold and does not consequently fall below the Lower threshold in less than the programmed De-bounce time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
							83.456	41.728	20.864	10.432	5.216	2.608	1.304	.652	.326	.163	value in Vrms
UPPER THRESHOLD	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Lower Threshold

Lower Threshold is programmable per channel from 0Vrms to 80Vrms, with binary 10-bit word resolution (LSB=163mv). A signal is considered logic Low ("0") when its value falls below the Lower threshold and does not consequently rise above the Upper Threshold in less than the programmed de-bounce time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
							83.456	41.728	20.864	10.432	5.216	2.608	1.304	.652	.326	.163	value in Vrms
LOWER THRESHOLD	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

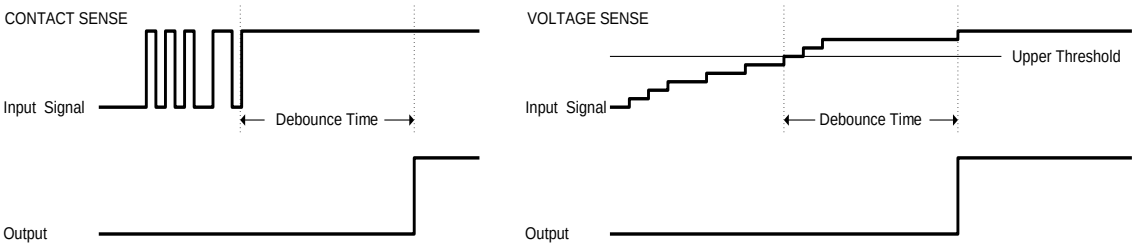
Min Low Threshold

Minimum Low Threshold is programmable per channel 0Vrms to 80Vrms, with binary 10-bit word resolution (LSB=163mv). This assumes that the programmed level is the maximum voltage used to indicate a Min Low Threshold. If a signal is less than the Min Low Threshold value, a flag is set in the *Min Low Threshold Status register*. The Min Low Threshold register may be used to monitor any type of low signal voltage condition or threshold such as a "Short to Ground" as it applies to input measurement as well as contact sensing applications.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
							83.456	41.728	20.864	10.432	5.216	2.608	1.304	.652	.326	.163	value in Vrms
MIN LOW THRESHOLD	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

De-Bounce Time

For contact sensing, de-bounce time is much like a glitch filter. Signal pulse widths less than the de-bounce time are filtered or ignored. Once a signal level is stable for a period longer than the de-bounce time (See Upper and Lower Threshold described above), a logic transition is validated. For voltage sensing, the input signal level must exceed its associated threshold for a time greater than the de-bounce time for the logic transition to be validated (See Upper and Lower Threshold described above). Once valid, the interrupt transition registers channel flag is set and the output logic changes state. To utilize these features, enter required de-bounce time into the appropriate channel registers. Enter time in 20.48 μs increments, up to (approx) 1.34 seconds. (LSB = approximately 20 μs). Value is 15 bits (MSB = don't care). De-bounce defaults to "0" upon reset. Enter a value of "0" to disable de-bounce filtering.



REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	~656	~328	~164	82	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.020	Approximate value in mS (LSB~**20.48** µS)
DE-BOUNCE TIME	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Read I/O

Independent of channel configuration (Voltage input or switch closure), read logic state High (“1”) or Low (“0”) as defined by channel threshold values. Each bit of 16-bit binary word corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Read Output Voltage (Actual)

Read actual output voltage at I/O pin per individual channel. Value is a signed binary 10 bit word, where LSB = 163mV. Data is read as 2’s complement number. **For example**, if output voltage word is 0x00F0 (240d), actual voltage is 39.12V. For negative voltage, 0x2F0 (-14d), actual voltage -2.283V

2F0 = {1, 0F0}

0F0 (2s complement) =0X000E (14d)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Output Voltage (signed)	**0**	**0**	**0**	**0**	**0**	**0**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Read Output Voltage (Averaged)

Read the averaged RMS value of the output voltage at I/O pin per individual channel. The Value is an unsigned binary 10 bit word, where LSB=163mV. **For example**, if output voltage word is 0x00F0 (240d), actual voltage is 39.12V.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
							83.456	41.728	20.864	10.432	5.216	2.608	1.304	.652	.326	.163	Value in Vrms
Output Voltage (averaged)	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Read Switch Current (Actual)

Read actual current through the I/O pins at each channel. Value is signed binary 10 bit word, where LSB=3mA. Read as 2’s complement; Current source is positive, Current sink is negative. **For example**, if output voltage word is 0x0064 (100d), actual current is (current source) 300mA. For negative (current sink), (-) 300mA would read as 0x39C (-100d)

39C = {1, 19C}

19C (2s complement) =0X0064 (100d)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Switch Current (signed)	**0**	**0**	**0**	**0**	**0**	**0**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Read Switch Current (Average)

Read averaged RMS current through the I/O pins at each channel. Value is signed binary 10 bit word, where LSB=3mA. Read as 2's complement; Current source is positive, Current sink is negative. **For example**, if output voltage word is 0x0064 (100d), actual current is (current source) 300mA. For negative (current sink), (-) 300mA would read as 0xFF9C (-100d).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Switch Current (averaged)	**0**	**0**	**0**	**0**	**0**	**0**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Reset Over-Current

There is only one Reset Over-Current register. Writing an integer "1" resets all sixteen channels. This register is used to reset disabled channel(s) that were tripped (high impedance state) following an over-current condition. Over-current condition is set at 600mA. Once the reset process is completes, processor will write a "0" back to the *Reset Over-Current* register. Card will respond to the reset command after one second.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
RESET OVER-CURRENT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	D=DATA BIT

Status Indications

The following status conditions can be monitored:

- **Fault:** When the test circuit does not agree with the data read or data write a fault status bit will be set within 3 seconds. A fault bit will remain latched until read.
- **Over-Current:** If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs
- **Max High Threshold:** If the signal exceeds this threshold, status is indicated (bit is set) within 500µs
- **Min Low Threshold:** If the signal falls below this threshold, status is indicated (bit is set) within 500µs
- **Lo-Hi Transition:** If a Lo to High transition is sensed, status is indicated (bit is set) within 40µs
- **Hi-Low Transition:** If a High to Low transition is sensed, status is indicated (bit is set) within 40µs
- **Mid-Range:** When the signal is in between the Upper and Lower thresholds, status is indicated (bit set) within 500µs

When status is "indicated," or bit is "set," bit value is logic "1." Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Max Hi Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Min Lo Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Mid-Range	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Interrupt Enable

To enable interrupts, set bit to '1' for the corresponding channel to be monitored. Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Max Hi Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Min Lo Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Mid-Range Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Interrupt Vectors

The Interrupt Vector Registers store the vectors for the specific interrupts generated by the module. When an interrupt is enabled and occurs, the contents of the corresponding Interrupt Vector register is the value that is reported to the user:

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Interrupt Vector BIT	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
Max Hi Threshold Interrupt Vector	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
Max Lo Threshold Interrupt Vector	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
Mid Range Threshold Interrupt Vector	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
Over-current Interrupt Vector	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
Interrupt Vector Lo-Hi Transition	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
Interrupt Vector Hi-Lo Transition	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding “latching” – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are “latching”; as defined, any noted transitional change on any channel will “latch” the entire Status Register.
- Once latched, there will be no further state change “sensed” by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will “unlatch” that particular status register (doesn’t necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will “latch” the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read “until cleared”.

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern (“loop to clear”) - this would also be similar to an Interrupt Service Routine (ISR) “loop to clear” function.

    Ex: Running the ‘loop to clear’ on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are “cleared” and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

  The ISR is typically a software (SW) handling branch (part of host application software) structured to “loop to read and clear” the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should “read” the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were “latched” – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively “re-arm” for the next transition to occur.

  Ex: The ISR should have the ‘loop to clear’ – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also “latch” the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

DISCRETE (MODULE K7) VME MODULE MEMORY REGISTER MAP

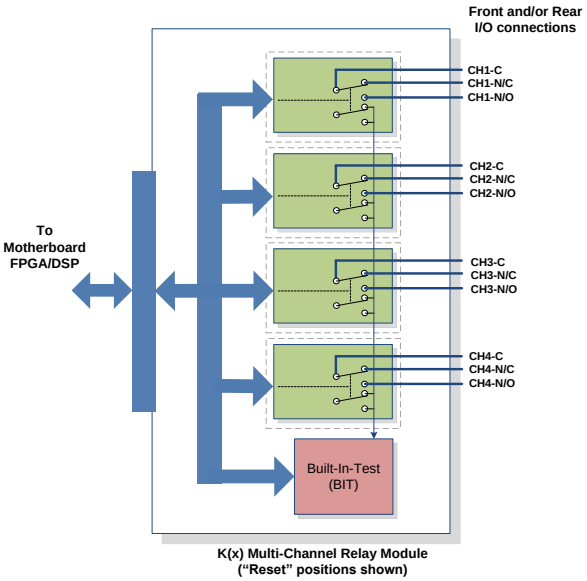
Module length (size) = 400h

000	Switch Control	Ch.01-16	R/W	07C	Max High Threshold	Ch.13	R/W	140	Voltage Reading (Averaged)	Ch.01	R
002	Read I/O	Ch.01-16	R	07E	Upper Threshold	Ch.13	R/W	142	Voltage Reading (Averaged)	Ch.02	R
				080	Lower Threshold	Ch.13	R/W	144	Voltage Reading (Averaged)	Ch.03	R
004	Max High Threshold	Ch.01	R/W	082	Min Low Threshold	Ch.13	R/W	146	Voltage Reading (Averaged)	Ch.04	R
006	Upper Threshold	Ch.01	R/W	084	De-bounce Time	Ch.13	R/W	148	Voltage Reading (Averaged)	Ch.05	R
008	Lower Threshold	Ch.01	R/W	086	Max High Threshold	Ch.14	R/W	14A	Voltage Reading (Averaged)	Ch.06	R
00A	Min Low Threshold	Ch.01	R/W	088	Upper Threshold	Ch.14	R/W	14C	Voltage Reading (Averaged)	Ch.07	R
00C	De-bounce Time	Ch.01	R/W	08A	Lower Threshold	Ch.14	R/W	14E	Voltage Reading (Averaged)	Ch.08	R
00E	Max High Threshold	Ch.02	R/W	08C	Min Low Threshold	Ch.14	R/W	150	Voltage Reading (Averaged)	Ch.09	R
010	Upper Threshold	Ch.02	R/W	08E	De-bounce Time	Ch.14	R/W	152	Voltage Reading (Averaged)	Ch.10	R
012	Lower Threshold	Ch.02	R/W	090	Max High Threshold	Ch.15	R/W	154	Voltage Reading (Averaged)	Ch.11	R
014	Min Low Threshold	Ch.02	R/W	092	Upper Threshold	Ch.15	R/W	156	Voltage Reading (Averaged)	Ch.12	R
016	De-bounce Time	Ch.02	R/W	094	Lower Threshold	Ch.15	R/W	158	Voltage Reading (Averaged)	Ch.13	R
018	Max High Threshold	Ch.03	R/W	096	Min Low Threshold	Ch.15	R/W	15A	Voltage Reading (Averaged)	Ch.14	R
01A	Upper Threshold	Ch.03	R/W	098	De-bounce Time	Ch.15	R/W	15C	Voltage Reading (Averaged)	Ch.15	R
01C	Lower Threshold	Ch.03	R/W	09A	Max High Threshold	Ch.16	R/W	15E	Voltage Reading (Averaged)	Ch.16	R
01E	Min Low Threshold	Ch.03	R/W	09C	Upper Threshold	Ch.16	R/W				
020	De-bounce Time	Ch.03	R/W	09E	Lower Threshold	Ch.16	R/W	160	Current Reading (Averaged)	Ch.01	R
022	Max High Threshold	Ch.04	R/W	0A0	Min Low Threshold	Ch.16	R/W	162	Current Reading (Averaged)	Ch.02	R
024	Upper Threshold	Ch.04	R/W	0A2	De-bounce Time	Ch.16	R/W	164	Current Reading (Averaged)	Ch.03	R
026	Lower Threshold	Ch.04	R/W					166	Current Reading (Averaged)	Ch.04	R
028	Min Low Threshold	Ch.04	R/W	0BC	Reset Over-Current	Ch.01-16	R/W	168	Current Reading (Averaged)	Ch.05	R
02A	De-bounce Time	Ch.04	R/W					16A	Current Reading (Averaged)	Ch.06	R
02C	Max High Threshold	Ch.05	R/W	0D0	Status Fault	Ch.01-16	R	16C	Current Reading (Averaged)	Ch.07	R
02E	Upper Threshold	Ch.05	R/W	0D4	Status Over-Current	Ch.01-16	R	16E	Current Reading (Averaged)	Ch.08	R
030	Lower Threshold	Ch.05	R/W	0D6	Status Max Hi Threshold	Ch.01-16	R	170	Current Reading (Averaged)	Ch.09	R
032	Min Low Threshold	Ch.05	R/W	0D8	Status Min Lo Threshold	Ch.01-16	R	172	Current Reading (Averaged)	Ch.10	R
034	De-bounce Time	Ch.05	R/W	0DA	Status Mid Range	Ch.01-16	R	174	Current Reading (Averaged)	Ch.11	R
036	Max High Threshold	Ch.06	R/W	0DC	Status Lo-Hi Transition	Ch.01-16	R	176	Current Reading (Averaged)	Ch.12	R
038	Upper Threshold	Ch.06	R/W	0DE	Status Hi-Lo Transition	Ch.01-16	R	178	Current Reading (Averaged)	Ch.13	R
03A	Lower Threshold	Ch.06	R/W					17A	Current Reading (Averaged)	Ch.14	R
03C	Min Low Threshold	Ch.06	R/W	0E8	Interrupt Fault Enable	Ch.01-16	R/W	17C	Current Reading (Averaged)	Ch.15	R
03E	De-bounce Time	Ch.06	R/W	0EC	Interrupt Over-Current Enable	Ch.01-16	R/W	17E	Current Reading (Averaged)	Ch.16	R
040	Max High Threshold	Ch.07	R/W	0EE	Interrupt Max Hi Threshold Enable	Ch.01-16	R/W				
042	Upper Threshold	Ch.07	R/W	0F0	Interrupt Min Lo Threshold Enable	Ch.01-16	R/W				
044	Lower Threshold	Ch.07	R/W	0F2	Interrupt Mid-Range Fault Enable	Ch.01-16	R/W				
046	Min Low Threshold	Ch.07	R/W	0F4	Interrupt Lo-Hi Transition Enable	Ch.01-16	R/W				
048	De-bounce Time	Ch.07	R/W	0F6	Interrupt Hi-Lo Transition Enable	Ch.01-16	R/W				
04A	Max High Threshold	Ch.08	R/W								
04C	Upper Threshold	Ch.08	R/W	100	Voltage Reading (Sampled)	Ch.01	R				
04E	Lower Threshold	Ch.08	R/W	102	Voltage Reading (Sampled)	Ch.02	R				
050	Min Low Threshold	Ch.08	R/W	104	Voltage Reading (Sampled)	Ch.03	R				
052	De-bounce Time	Ch.08	R/W	106	Voltage Reading (Sampled)	Ch.04	R				
054	Max High Threshold	Ch.09	R/W	108	Voltage Reading (Sampled)	Ch.05	R				
056	Upper Threshold	Ch.09	R/W	10A	Voltage Reading (Sampled)	Ch.06	R				
058	Lower Threshold	Ch.09	R/W	10C	Voltage Reading (Sampled)	Ch.07	R				
05A	Min Low Threshold	Ch.09	R/W	10E	Voltage Reading (Sampled)	Ch.08	R				
05C	De-bounce Time	Ch.09	R/W	110	Voltage Reading (Sampled)	Ch.09	R	3A8	(Reserved)		R/W
05E	Max High Threshold	Ch.10	R/W	112	Voltage Reading (Sampled)	Ch.10	R	3AA	(Reserved)		R/W
060	Upper Threshold	Ch.10	R/W	114	Voltage Reading (Sampled)	Ch.11	R	3AE	(Reserved)		R/W
062	Lower Threshold	Ch.10	R/W	116	Voltage Reading (Sampled)	Ch.12	R				
064	Min Low Threshold	Ch.10	R/W	118	Voltage Reading (Sampled)	Ch.13	R	3B2	(Reserved)		R/W
066	De-bounce Time	Ch.10	R/W	11A	Voltage Reading (Sampled)	Ch.14	R	3B4	Module Design Version		R
068	Max High Threshold	Ch.11	R/W	11C	Voltage Reading (Sampled)	Ch.15	R	3B6	Module Design Revision		R
06A	Upper Threshold	Ch.11	R/W	11E	Voltage Reading (Sampled)	Ch.16	R	3B8	DSP Version		R
06C	Lower Threshold	Ch.11	R/W					3BA	FPGA Version		R

06E	Min Low Threshold	Ch.11	R/W	120	Current Reading (Sampled)	Ch.01	R	3BC	Module ID	R
070	De-bounce Time	Ch.11	R/W	122	Current Reading (Sampled)	Ch.02	R			
072	Max High Threshold	Ch.12	R/W	124	Current Reading (Sampled)	Ch.03	R	3C2	Over-current Interrupt Vector	R/W
074	Upper Threshold	Ch.12	R/W	126	Current Reading (Sampled)	Ch.04	R	3C4	Low-Hi Transition Interrupt Vector	R/W
076	Lower Threshold	Ch.12	R/W	128	Current Reading (Sampled)	Ch.05	R	3C6	Hi-Low Transition Interrupt Vector	R/W
078	Min Low Threshold	Ch.12	R/W	12A	Current Reading (Sampled)	Ch.06	R			
07A	De-bounce Time	Ch.12	R/W	12C	Current Reading (Sampled)	Ch.07	R			
				12E	Current Reading (Sampled)	Ch.08	R	3E0	BIT Interrupt Vector Ch.01-16	R/W
				130	Current Reading (Sampled)	Ch.09	R	3E2	Max Hi Threshold Interrupt Vector	R/W
				132	Current Reading (Sampled)	Ch.10	R	3E4	Min Low Threshold Interrupt Vector	R/W
				134	Current Reading (Sampled)	Ch.11	R	3E6	Mid Range Threshold Interrupt Vector	R/W
				136	Current Reading (Sampled)	Ch.12	R			
				138	Current Reading (Sampled)	Ch.13	R			
				13A	Current Reading (Sampled)	Ch.14	R			
				13C	Current Reading (Sampled)	Ch.15	R			
				13E	Current Reading (Sampled)	Ch.16	R			

I/O RELAY (MODULE KN, KL)

Principle of Operation



This module provides four individual single pole user DPDT Form C (changeover / break-before-make type) relay I/O channels. The 2nd set of pole contacts is used for Built-In-Test (BIT). Each channel has a common input terminal (C), a normally closed output terminal (N/C) and a normally open (N/O) output terminal. The channel is commanded to energize or de-energize the relays (close or open) so that the signal provided on (C) may be switched/directed to either the (N/C) or (N/O) terminals. Interrupts can be enabled/configured for each channel to indicate if a BIT fault (state of secondary set of contacts does not match command) occurs. Internal de-bounce circuits for each channel provide the required time delay to eliminate false signals resulting from contact bounce commonly experienced with mechanical relays and switches. The **KN** implements "non-latching" type relays. The relays utilized on the KN module power-on default remain de-energized or in the "reset position" until commanded to the "set" position. The contacts will then remain in the "set" position until commanded to the "reset" position or if power is removed from the card/module. The **KL** implements "latching" type relays. The relays on the **KL** module utilize magnetic latching to assure that once a relay channel is 'set' or 'reset' (even if power is removed from the card/module), the channel will remain at the last commanded position. The secondary set of contacts on each relay channel is utilized for BIT purposes and is continually scanned in comparison to commanded "set" (closed) or "reset" (open) conditions. Data is double-buffered for immediate availability.

Automatic Background Built-In Test (BIT) Diagnostic Capability

The module contains automatic background BIT testing that verifies channel processing from a secondary set of contacts (data read compared to write logic), and tests for relay state. Any discrepancy (or fault) triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card.

Write Output

Write a logic level High ("1") (set/closed) or Low ("0") (reset/open) to associated channel bit, in 16-bit binary word, to toggle/command between the "set" or "reset" of the channel respectively.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	x	x	x	x	x	x	x	x	x	x	x	x	4	3	2	1	Channel
WRITE OUTPUT	0	0	0	0	0	0	0	0	0	0	0	0	D	D	D	D	D=DATA BIT

Read State

Read logic state High ("0") or Low ("1") as defined by relay state "OPEN" (reset) or "CLOSED" (set) respectively.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	0	0	0	0	0	0	0	0	0	0	0	0	D	D	D	D	D=DATA BIT

Status, BIT Fault

BIT Fault: The secondary set of contacts on each relay channel is utilized for BIT purposes and is continually scanned in comparison to commanded “set” (closed) or “reset” (open) conditions. “1” indicates FAIL/FAULT, “0” indicates PASS/No Fault. A fault will be indicated within 10 ms. A fault is latched until read.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	x	x	x	x	x	x	x	x	x	x	x	x	4	3	2	1	Channel
Status, BIT Fault	0	0	0	0	0	0	0	0	0	0	0	0	D	D	D	D	D=DATA BIT

Interrupt Enable, BIT Fault

To enable interrupts, set bit to ‘1’ for the corresponding channel to be monitored. Reading will reset (or unlatch) Status Register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	x	x	x	x	x	x	x	x	x	x	x	x	4	3	2	1	Channel
Interrupt Enable, BIT	0	0	0	0	0	0	0	0	0	0	0	0	D	D	D	D	D=DATA BIT

Interrupt Vector, BIT Fault

The Interrupt Vector Registers store the vectors for the specific interrupts generated by the module. When any channel interrupt is enabled and occurs, the contents of the corresponding Interrupt Vector register is the value that is reported to the user.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Vector, Interrupt	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding “latching” – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are “latching”; as defined, any noted transitional change on any channel will “latch” the entire Status Register.
- Once latched, there will be no further state change “sensed” by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will “unlatch” that particular status register (doesn’t necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will “latch” the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read “until cleared”.

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern (“loop to clear”) - this would also be similar to an Interrupt Service Routine (ISR) “loop to clear” function.

    Ex: Running the ‘loop to clear’ on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are “cleared” and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

  The ISR is typically a software (SW) handling branch (part of host application software) structured to “loop to read and clear” the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should “read” the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were “latched” – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively “re-arm” for the next transition to occur.

  Ex: The ISR should have the ‘loop to clear’ – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also “latch” the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

I/O RELAY (MODULE KN, KL) VME MEMORY MAP

(module length 0x400)

000	Write Output, Ch.1-4	R/W	0D0	Status, BIT Fault Ch.1-4	R	3B4	Module Design Version	R
002	Read State, Ch.1-4	R				3B6	Module Design Revision	R
						3B8	Module DSP	R
						3BA	Module FPGA	R
						3BC	Module ID	R
			0E8	BIT Fault, Intrpt. Enable Ch.1-4	R/W	3E0	Vector, BIT Interrupt	R/W

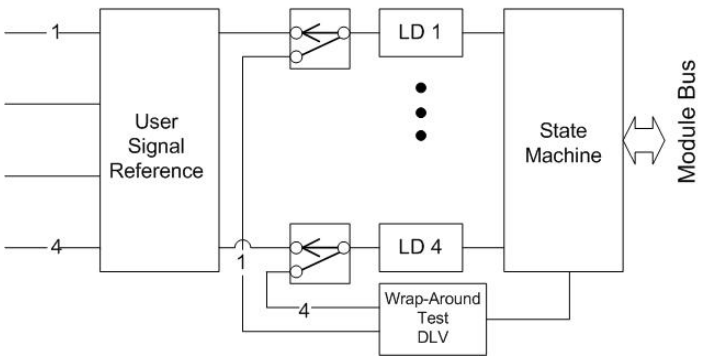
LVDT MEASUREMENT (MODULE L*)

*Indicates wide selection. (See part number designation.)

Principle of Operation (LVDT)

The LVDT Module provides four isolated measurement channels, programmable with 2, 3 and 4 wire interface capability. Typically the primary is excited by an AC source, causing a magnetic flux to be generated within the transducer. Voltages are induced in the two secondaries, with the magnitude varying with the position of the core. Usually, the secondaries are connected in series opposition, causing a net output voltage of zero when the core is at the electrical center. When the core is displaced in either direction from center the voltage increases linearly either in phase or out of phase with the excitation depending on the direction.

LVDT Module Block Diagram



Interfacing LVDT to Converter

Two common connection methods are:

1. Primary as reference (two-wire system)
2. Derived reference (three/four-wire LVDT)

2-Wire System

This method of connection converts the widest range of LVDT sensors and is the most sensitive to excitation voltage variations, temperature and phase shift effects. This system solves the identity V / Vexc.

3/4-Wire System

The LVDT is again excited from the primary side, but the converter reference is the sum of A + B that has constant amplitude for changing core displacement. This system is insensitive to temperature effects, phase shifts and oscillator instability and solves the identity (A-B) / (A+B).

Built-In Test (BIT) / Diagnostic Capability

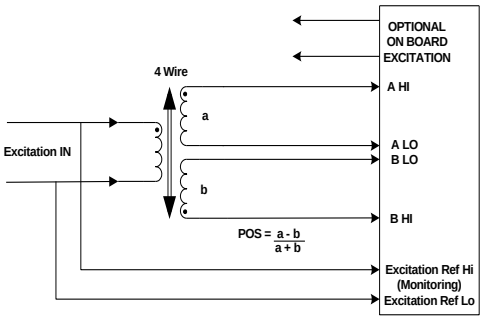
This board incorporates major diagnostics that offer substantial improvements to system reliability because the user is alerted to channel malfunction. This approach reduces bus traffic, because the Status Registers need not be constantly polled. Three different tests (one on-line and two off-line) can be selected.

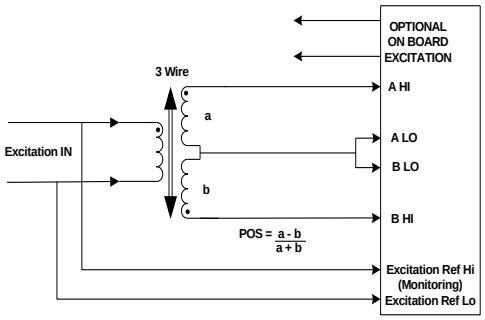
The On-line D2 Test initiates automatic background BIT testing (on-line). Each channel is checked over the programmed signal range to a measuring accuracy of 0.1% FS, and each Signal and Excitation is monitored. Any failure triggers an Interrupt (if enabled) and the results are available in registers. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 1 second, to verify that background bit testing is activated. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled.

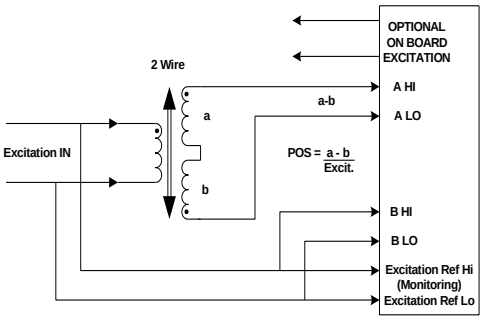
The Off-line D3 Test, if enabled, starts an initiated BIT Test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and measures multiple voltages to a test accuracy of 0.1%FS (offline). External excitation is not required. Any failure triggers an interrupt (if enabled) and results can be read from registers. The testing requires no external programming and can be initiated or terminated.

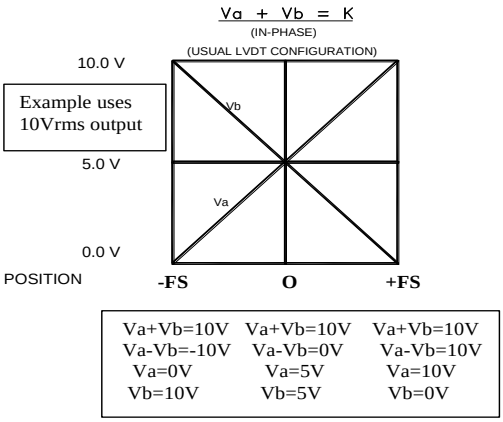
The Off-line D0 Test is used to check the card and the system interface. All channels are disconnected from the outside world (offline), allowing user to write any number of input positions to the card and then read the data from the interface. External excitation is not required.

Various LVDT Configurations









2-wire LVDT Connections:

Connect A–B LVDT output to Signal A and the Excitation to Signal B inputs. Excitation should also be connected to the Excitation input to enable card to sense and report any excitation loss.

3/4-wire LVDT Connections:

Connect A and B LVDT outputs to Signal A and B inputs. Excitation is not used, but should be connected to enable card to sense and report any excitation loss.

Position Data

Data Hi Type: 16-bit two's complement

Data Hi & Lo Type: 24-bit two's complement

Range: 0 to FFFF

Read/Write: R

Read Position Data: Reads the Position Data Register corresponding to a given channel.

Data Format (2-wire): The output data is A / B and represents %FS. Format is two's complement. Max. positive excursion is 7FFF, 0 = 0, and max. negative excursion is 8000.

Data format (3/4-wire): The output data is (A-B) / (A+B) and represents %FS. Format is two's complement. Max. positive excursion is 7FFF, 0 = 0, and max. negative excursion is 8000.

Bandwidth (BW)

The bandwidth (BW) for each channel is individually programmable (when Bandwidth Select Register is set for "manual" mode). When operating in "manual mode" (please see/note Bandwidth Selection register description), write desired BW as unsigned integer, between 6 and 1280 (in 2 Hz increments), to associated channel register. All values greater than 1280 will be processed as 1280Hz. All values less than 6 will be processed as 6 Hz.

Example: BW of 40 Hz = 028h.When the bandwidth select register is set for "automatic mode", the automatic bandwidth (as calculated and set by the card algorithm) can be read.

Bandwidth Select

BW Select register sets the "Automatic" or "Manual" Bandwidth control. This register is bitmapped per channel; (i.e. D0 = CH1, D1 = CH2, etc.). "1" indicates user wants automatic bandwidth. "0" indicates user wants manual control.

The Automatic BW feature, when enabled, reads the input reference frequency and automatically adjusts the BW to approximately 1/10 of the carrier frequency. This Auto BW range will be a minimum of 10 Hz with a maximum of 100 Hz.

When in "Manual BW" mode, the user can enter the BW between a range of 6 Hz and 1280 Hz, in 2 Hz increments.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BANDWIDTH SELECT	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	D=DATA BIT

Active Channels

Type: binary word

Range: N/A

Read/Write: R/W

Initialized Value: N/A

Set the bit corresponding to each channel to be monitored during BIT testing in the *Active Channel* register. Set bit to "1" for active channels and clear bit to "0" for those not used. **NOTE:** Omitting this step will produce false alarms, because unused channels will set faults.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ACTIVE CHANNEL	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL ENABLE BIT

Latch (Track/Hold)

Type: 16-bit unsigned integer

Range: 0 or 2

Read/Write: R

Initialized Value: 0

Writing the integer 2 to the *Latch* register will cause all the channels to be latched. Reading a particular channel will disengage the latch for that channel. Writing a 0 to this register will disengage latch on all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TRACK/HOLD	D	D	D	D	D	D	D	D	D	D	D	D	Ch4	Ch3	Ch2	Ch1	D=DATA BIT

Test (D2) Verify

Card will write 55h at *Test (D2) Verification* register when (D2) is enabled, approximately every one second. User can clear to 00h and then read again, after approximately one second, to verify that background bit testing is activated.

Test Enable

Set bit to enable associated Built-In Self Test D3, D2, or D0.

Write “1” to D2 to initiate automatic background BIT testing. Card will (every 1 second) write 55h at *Test (D2) verify* register when D2 is enabled. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 1 second, to verify that background bit testing is activated. D3 test cycle is completed within 45 seconds and results can be read from the associated status registers when D3 changes from “1” to “0”. Any failure triggers an Interrupt (if enabled). All testing requires no external programming and is initiated by writing “1” or terminated by writing “0”.

The on-line (D2) Test initiates automatic background BIT testing. Each channel is checked every 2.77° to a testing accuracy of 0.05°, and each Signal and Excitation is always monitored. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled via the bus.

The off-line (D3) Test initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different positions to a test accuracy of 0.05°. Results can be read from registers and external excitation is not required. Any failure triggers an Interrupt (if enabled). The testing requires no external programming, and can be initiated or stopped via the bus.

The off-line (D0) Test is used to check the card and the SYSTEM interface. All channels are disconnected from the outside world, allowing the user to write any number of input positions to the card and then to read the data from the interface. External excitation is not required.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TEST ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	**D3**	**D2**	X	**D0**

Test Position

Type: 16-bit unsigned integer

Range: 0 to 359.9945 degrees

Read/Write: W

Initialized Value: 8.33%

Enter the D0 test position as per table.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	approximate value
TEST POSITION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT (Degrees)

2-Wire/4-Wire Select

Type: binary word

Range: N/A

Read/Write: R/W

Initialized Value: N/A

Individually configure each channel for input signal measurement format:

- 4-Wire=01
- 2-Wire=10

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
LVDT2W/LVDT4W	X	X	X	X	X	X	X	X	CH4		CH3		CH2		CH1		CHANNEL BIT

Input Reference Frequency Measurement

Each individual channel input excitation frequency is measured and the value reported to a corresponding read register. The input excitation frequency is reported to a resolution of 0.01 Hz. The output is in integer decimal format.

For example, if channel 1 input excitation is 400 Hz, the output measurement word from the corresponding register would be 40,000.

Input Signal Voltage (V_{L-L}) Measurement

Each individual channel input signal voltage "V_{L-L}" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format.

For example, if channel 1 input signal voltage is 11.8 VRMS, the output measurement word from the corresponding register would be 1180.

Input Reference Voltage (VREF) Measurement

Each individual channel input signal voltage "VREF" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format.

For example, if channel 1 input signal voltage is 11.8 VRMS, the output measurement word from the corresponding register would be 1180.

Signal Loss Threshold

Each individual channel input signal voltage "V_{L-L}" is measured and the value reported to a corresponding read register. The signal loss detection circuitry can be tailored to report a signal loss (at SIG Status register) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format.

For example, if channel 1 input signal loss voltage threshold is to be 7 VRMS, the programmed word to the corresponding register would be 700 (2BCh).

Reference Loss Threshold

Each individual channel input excitation voltage "VREF" is measured and the value reported to a corresponding read register. The excitation loss detection circuitry can be tailored to report a excitation loss (at REF Status register) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format.

For example, if channel 1 input excitation loss voltage threshold is to be 20 VRMS, the programmed word to the corresponding register would be 2000 (7D0h).

Signal Status

Type: binary word

Range: N/A

Read/Write: R

Initialized Value: 0

Check the corresponding bit for a channel's Signal Status. A Signal input loss to that channel will trigger a bit failure (=1) on a per channel basis. Passing status (=0). Signal Loss is indicated after 2 seconds. Signal input monitoring is disabled during D3 or D0 Test. Any Signal Status failure, transient or intermittent, will latch the *Signal Status* register. Reading any status bit will unlatch the entire register. Signal Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Reference Status

Type: binary word

Range: N/A

Read/Write: R

Initialized Value: 0

Check the corresponding bit for a channel's Reference (Excitation) Status. An Excitation input loss to that channel will trigger a bit failure (=1) on a per channel basis. Passing status (=0). Signal and/or Excitation Loss is indicated after 2 seconds. Signal and Excitation input monitoring is disabled during D3 or D0 Test. Any Excitation Status failure, transient or intermittent, will latch the *Reference Status* register. Reading any status bit will unlatch the entire register. Excitation Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
REFERNCE STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Signal Status Interrupt Enable

Type: binary word

Range: N/A

Read/Write: R/W

Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal loss will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the *Signal Status Interrupt Vector.*

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

Reference Status Interrupt Enable

Type: binary word

Range: N/A

Read/Write: R/W

Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, an excitation input loss will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the *Reference Status Interrupt Vector.*

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
REFERENCE STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

BIT Status Interrupt Enable

Range: 0 to 15

Read/Write: R/W

Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 0 to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS INTR ENA	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

OSC (Onboard) Excitation Set Frequency

Type: 16-bit unsigned integer

Range: 47 to 10,000 Hz

Read/Write: R/W

Initialized Value: N/A

Program Reference Frequency, where LSB is 0.01 Hz. **For example**: To program 400 Hz, 400 x 100= 40,000, which equals 0x9C40. In this example, 0x0000 would be programmed in the *Reference Frequency High* register, and 0x9C40 would be programmed in the *Reference Frequency Low* register. To program 10,000 Hz, 10,000 x 100= 1,000,000, which equals 0xF4240. In this example, 0x000F would be programmed in the *Reference Frequency High* register, and 0x4240 would be programmed in the *Reference Frequency Low* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	327.68	163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	0.01	approximate value
REF FREQUENCY LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)
REGISTER	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
	0	0	0	0	0	0	0	0	0	0	0	0	5242.88	2621.44	1310.72	655.36	approximate value
REF FREQUENCY HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

OSC (Onboard) Excitation Set Voltage

Type: 16-bit unsigned integer

Range: 2.0 to 28.0 VRMS, or 115 VRMS

Read/Write: R/W

Initialized Value: N/A

Program Reference Voltage, where LSB is 0.01 VRMS. **For example**: To program 26.1 VRMS, 26.1 x 100= 2610, which equals 0xA32. In this example, 0x0000 would be programmed in the *Reference Voltage High* register, and 0x0xA32 would be programmed in the *Reference Voltage Low* register. To program 115 VRMS, 115 x 100= 11,500, which equals 0x2CEC. In this example, 0x0000 would be programmed in the *Reference Voltage High* register, and 0x2CEC would be programmed in the *Reference Voltage Low* register. **Note**: *Reference Voltage High* register always remains at 0x0000.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	81.92	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	0.01	approximate value
REF VOLTAGE LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (V)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	approximate value
REF VOLTAGE HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (V)

Interrupt Vector

Write 16-bit integer (0-255). Used for failure reports. The Interrupt Vector Registers store the vectors for the specific interrupts generated by the module. If the same vector is loaded into each register, the same interrupt routine will be invoked by all interrupts. If unique vectors are loaded into the registers, a different Interrupt Service Routine can be invoked by each interrupt.

- The Signal Loss interrupt vector will be serviced when the Signal Loss status is set and the interrupt has been enabled.
- The Excitation Loss interrupt vector will be serviced when the Excitation Loss status is set and the interrupt has been enabled.
- The BIT interrupt vector will be serviced when the Bit (failure) status is set and the interrupt has been enabled.
- The Lock Loss interrupt vector will be serviced when the Lock Loss status is set and the interrupt has been enabled.
- The Position Δ interrupt vector will be serviced when the Position Δ status is set and the interrupt has been enabled.

LVDT FIFO Buffer Operational Description

LVDT Data:

The available data in the FIFO buffer can be retrieved in the following registers one “WORD” (16 bits) at a time. The data is presented in 16-bit unsigned integer format.

Description	L(R)VDT Data (16-bit hex)
Data ch1-4	Data Range: (0x0000-0xFFFF)

Words in FIFO:

This is a counter that reports the number of data in WORD (2 byte) stored in the FIFO buffer. Every time a read operation is made to the L(R)VDT Data memory address, its corresponding “Words in FIFO” counter will be decremented by one. The maximum number of words that can be stored in the FIFO is 65,535 (0xFFFF).

Description	Words in FIFO (16-bit hex)
Words in ch1-4	Data Range: (0x0000-0xFFFF)

FIFO Status:

The FIFO status register indicates the current condition of the FIFO buffer. B0-B4 is used to show the different condition of the buffer.

B0 = Empty. When “Words In FIFO” register is zero, B0 = 1; otherwise B0 =0.

B1 = Low Limit. When “Words In FIFO” register” < “Low-Threshold”, B1= 1; otherwise B1 =0.

B2 = High Limit. When “Words In FIFO” register” > “Hi-Threshold”, B2=1; otherwise B2 =0.

B3 = FIFO Full. When “Words In FIFO” register” = 65535, B3=1; otherwise B3 =0.

B4 = Sample Done. When “Words In FIFO” register = “Size”, B4=1; otherwise B4 =0.

Description	FIFO Status (16-bit hex)
Status in ch1-4	Data Range: B0-B4

Pending (To be determined)

Description	FIFO Status (16-bit hex)
Status in ch1-4	Data Range: 0x0-0xFFFF

Hi-Threshold:

The Hi-threshold level is used to set or reset the high limit bit (B2) of the individual channel status register in the memory location. When the "Words in FIFO" counter is greater than or equal to the value stored in the hi-threshold register, the high limit bit (B2) of the channel status register will be set. When the "Words in FIFO" counter is less than or equal to the value stored in the hi-threshold, the high limit bit (B2) of the channel status register will be reset.

Set = "logical 1"

Reset = "logical 0"

Description	Hi-Threshold (16-bit hex)
Hi-Threshold in ch1-4	Data Range: (0x0000-0xFFFF)

Low-Threshold:

The low-threshold level is used to set or reset the low limit bit (B1) of the individual channel status register in the memory location. When the "Words in FIFO" counter is greater than or equal to the value stored in the low-threshold, the low limit bit (B1) of the channel status register will be reset. When the "Words in FIFO" counter is less than or equal to the value stored in the low-threshold, the low limit bit (B1) of the channel status register will be set.

Set = "logical 1"

Reset = "logical 0"

Description	Low-Threshold (16-bit hex)
Low-Threshold in ch1-4	Data Range: (0x0000-0xFFFF)

Delay:

Set the number of delay samples before the actual FIFO data collection begins. The data collected during the delay period will be discarded.

Description	Delay (16-bit hex)
Delay in ch1-4	Data Range: (0x0000-0xFFFF)

Size:

Set the size of the FIFO buffer. The largest size that a FIFO buffer can be is 65,535(0xFFFF)

Description	Size (16-bit hex)
Size in ch1-4	Data Range: (0x0000-0xFFFF)

Sample Rate:

The sample rate sets the sampling rate for the FIFO buffer. The rate is based on the product of 5.12 μs x Sample Rate. **For example**, if the rate is set to 2, the FIFO buffer will be sampling at 5.12 μs * 2 = 10.24 μs.

Description	Sample Rate (16-bit hex)
Rate in ch1-4	Data Range: (0x0000-0xFFFF)

Clear FIFO:

Whenever the Clear memory is set or reset for the individual channel, it initializes the "Words in FIFO" to zero. A read to the "L(R)VDT Data" register gives aged data.

Description	Clear FIFO (16-bit hex)
Clear in ch1-4	Data Range: (0x0000-0xFFFF)

Buffer Data Type:

Different types of data format can be stored in the FIFO buffer and their formats are defined by the Buffer Control Register. The following bit mask defines the type/format of data that will be put into the FIFO buffer.

B0 = Data (16-bit Hi). 16-bit resolution data.

B1 = Data (8-bit Lo). Combine with B0 to form a 24-bit resolution.

B2 = Filtered Data (16-bit Hi). Filtered 16-bit resolution data.

B3 = Filtered Data (8-bit Lo). Combine with B2 to form filtered 24-bit resolution.

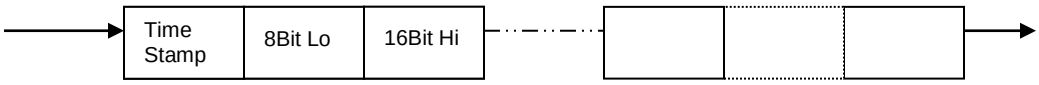
B4 = Time Stamp. An integer counter that counts from 0 to 65,535 and wraps around when it overflows.

B5 = Reserved

B6 = Reserved

B7 = Reserved

Note: Each data format (B0 – B4) requires one word of storage space from the FIFO buffer. **For example**, if B0, B1 and B4 are set (0x13) and the Size register is set to 1, a FIFO write will put 3 words of data to the FIFO memory spaces. Since the maximum physical size of FIFO is 65,535 for each channel, the value in the Size and Buffer Control register could cause an overflow to the FIFO buffer. When an overflow condition occurs, any un-stored data will be lost.



Description	Buffer Ctrl.(16-bit hex)
Buf. Ctrl. in ch1-4	Data Range: b0-b4

Trigger Mode:

The FIFO can be started/triggered by different sources.

B0-B1 = Source Select (choose one only)

- 0x0 = Ext. Trigger 2
- 0x1 = Ext. Trigger 1
- 0x2 = Software Trigger

B3 = Reserved

B4-B7 = Trigger Type (Choose one only)

- 0x10 = Negative Slope
- 0x20 = Trigger Pulse Enable
- 0x40 = Trigger Pulse/Trigger Enable Select
- 0x80 = Trigger Clear

Description	Trigger Ctrl.(16-bit hex)
Trigger Ctrl. in ch1-4	Data Range: B0-B7

Register Write	Trig Source	Slope
0x20	Ext Trigger 2	Positive
0x21	Ext Trigger 1	Positive
0x22	SW Trigger	Positive (don't care)
0x30	Ext Trigger 2	Negative
0x31	Ext Trigger 1	Negative
0x32	SW Trigger	Negative (don't care)
0x40	Initiate	
0x80	Stop (Clear Trigger)	

Software Trigger:

Software trigger is used to kick start the FIFO buffer and the collection of data. In order to use this operation, the "Trigger Ctrl" register must be set up properly. Setting or resetting the "Software Trigger" will start FIFO data collection for ALL channels.

Description	Software Trigger (16-bit hex)
Software Trigger	Data Range: 0x0-0xFFFF

Status, BIT Fail

Type: binary word

Range: 0 to 15

Read/Write: R

Initialized Value: 0

BIT status is part of background testing and the status register may be checked or polled at any given time. BIT status reports correct operation (with specification) for channel accuracy. Any failure of frequency, amplitude of DC offset will trigger a bit failure (=1) on a per channel basis. Passing status (=0). Status is latched; reading register unlatches BIT status. BIT is operating at all times and cannot be enabled or disabled using the General use Test Enable register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding “latching” – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are “latching”; as defined, any noted transitional change on any channel will “latch” the entire Status Register.
- Once latched, there will be no further state change “sensed” by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will “unlatch” that particular status register (doesn’t necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will “latch” the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read “until cleared”.

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- Power-up
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern (“loop to clear”) - this would also be similar to an Interrupt Service Routine (ISR) “loop to clear” function.

    Ex: Running the ‘loop to clear’ on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are “cleared” and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- Interrupt Software Routine (ISR)

  The ISR is typically a software (SW) handling branch (part of host application software) structured to “loop to read and clear” the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should “read” the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were “latched” – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively “re-arm” for the next transition to occur.

  Ex: The ISR should have the ‘loop to clear’ – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

Notes:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also “latch” the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

LVDT (MODULE L) VME MEMORY MAP

Module Length = 400h

000	Position CH 1 Data Lo	R	088	CH1 REF Loss Threshold	W/R	330	CH2 Data Buffer HI Threshold	W/R
002	Position CH 1 Data Hi	R	08A	CH2 REF Loss Threshold	W/R	332	CH2 Data Buffer Lo Threshold	W/R
004	Position CH 2 Data Lo	R	08C	CH3 REF Loss Threshold	W/R	334	CH2 Buffer Delay Sample	W/R
006	Position CH 2 Data Hi	R	08E	CH4 REF Loss Threshold	W/R	336	CH2 Buffer # of Samples	W/R
008	Position CH 3 Data Lo	R				338	CH2 Buffer Sample Rate	W/R
00A	Position CH 3 Data Hi	R	0A0	LVDT1 Scale	W/R	33A	CH2 Clear FIFO	W/R
00C	Position CH 4 Data Lo	R	0A2	LVDT2 Scale	W/R	33C	CH2 Buffer Data Type	W/R
00E	Position CH 4 Data Hi	R	0A4	LVDT3 Scale	W/R	33E	CH2 Buffer Trigger Mode	W/R
			0A6	LVDT4 Scale	W/R			
020	CH1 Bandwidth	W/R				340	CH3 Data Buffer HI Threshold	W/R
022	CH2 Bandwidth	W/R	0E8	SIG Status Ch.1-4	R	342	CH3 Data Buffer Lo Threshold	W/R
024	CH3 Bandwidth	W/R	0EA	REF Status Ch.1-4	R	344	CH3 Buffer Delay Sample	W/R
026	CH4 Bandwidth	W/R	0F2	SIG Status Interrupt Enable Ch.1-4	W/R	346	CH3 Buffer # of Samples	W/R
028	Bandwidth Select	W/R	0F4	REF Status Interrupt Enable Ch.1-4	W/R	348	CH3 Buffer Sample Rate	W/R
02E	LD Active Channels	W/R	0F6	BIT Status Interrupt Enable Ch.1-4	W/R	34A	CH3 Clear FIFO	W/R
030	LVDT Track / Hold	W/R				34C	CH3 Buffer Data Type	W/R
032	D2 Test Verify	W/R	100	OSC Set Freq Lo	W/R	34E	CH3 Buffer Trigger Mode	W/R
034	Test Enable	W/R	102	OSC Set Freq HI	W/R			
038	Test Position	W/R	104	OSC Set Volt Lo	W/R	350	CH4 Data Buffer HI Threshold	W/R
03C	LVDT2W/LVDT4W	W/R	106	OSC Set Volt Hi	W/R	352	CH4 Data Buffer Lo Threshold	W/R
						354	CH4 Buffer Delay Sample	W/R
050	CH1 Frequency LO	R	300	FIFO Buffer Data CH1	R	356	CH4 Buffer # of Samples	W/R
052	CH1 Frequency HI	R	302	FIFO Buffer Data CH2	R	358	CH4 Buffer Sample Rate	W/R
054	CH2 Frequency LO	R	304	FIFO Buffer Data CH3	R	35A	CH4 Clear FIFO	W/R
056	CH2 Frequency HI	R	306	FIFO Buffer Data CH4	R	35C	CH4 Buffer Data Type	W/R
058	CH3 Frequency LO	R				35E	CH4 Buffer Trigger Mode	W/R
05A	CH3 Frequency HI	R	308	FIFO Words CH1	R			
05C	CH4 Frequency LO	R	30A	FIFO Words CH2	R	360	Software Trigger	W/R
05E	CH4 Frequency HI	R	30C	FIFO Words CH3	R	380	BIT Status (CH1-4)	W/R
			30E	FIFO Words CH4	R			
060	CH1 V_{L-L} (A+B Magnitude)	R				3B4	Module Design Version	R
062	CH2 V_{L-L} (A+B Magnitude)	R	310	FIFO Status CH1	R	3B6	Module Design Revision	R
064	CH3 V_{L-L} (A+B Magnitude)	R	312	FIFO Status CH2	R	3B8	Module DSP Rev	R
066	CH4 V_{L-L} (A+B Magnitude)	R	314	FIFO Status CH3	R	3BA	Module FPGA Rev	R
			316	FIFO Status CH4	R	3BC	Module ID	R
068	CH1 Measured VREF	R						
06A	CH2 Measured VREF	R	320	CH1 Data Buffer HI Threshold	W/R	3E0	Vector Signal Loss	W/R
06C	CH3 Measured VREF	R	322	CH1 Data Buffer Lo Threshold	W/R	3E2	Vector REF Loss	W/R
06E	CH4 Measured VREF	R	324	CH1 Buffer Delay Sample	W/R	3E4	Vector BIT Fail	W/R
			326	CH1 Buffer # of Samples	W/R	3E6	Vector Lock Loss	W/R
080	CH1 Signal Loss Threshold	W/R	328	CH1 Buffer Sample Rate	W/R	3E8	Vector Position Δ	W/R
082	CH2 Signal Loss Threshold	W/R	32A	CH1 Clear FIFO	W/R			
084	CH3 Signal Loss Threshold	W/R	32C	CH1 Buffer Data Type	W/R			
086	CH4 Signal Loss Threshold	W/R	32E	CH1 Buffer Trigger Mode	W/R			

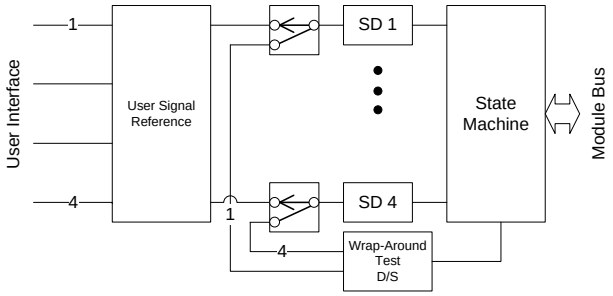
SYNCHRO/RESOLVER MEASUREMENT (MODULE S*)

S/D (Module S*)

*Indicates wide selection and optional 5VA reference supply
(See part number designation)

Principle of Operation

SD Module Block Diagram



The Synchro/Resolver Module provides four programmable isolated measurement channels. It features 16-bit resolution (with up to 24-bit resolution for the two-speed configuration), and a single speed accuracy of 1 arc-min. For two speed applications, the overall accuracy is calculated by dividing the accuracy of the fine channel (1 arc-min) by the gear ratio. This S/D measurement design has the capability to automatically shift to higher bandwidths when high acceleration events are encountered. There is no data latency. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 190 RPS, at 16-bit resolution. Both a software and hardware LATCH feature is provided to permit the user to read all channels at the same time. Reading will unlatch that channel. The angle alert monitors each channel for the programmed angle difference and sets an interrupt, if enabled, as soon as that threshold is reached. Thus, no polling of the angle registers is required until an angle has reached the specified difference. The use of Type II servo loop processing techniques enables tracking up to the specified rate, at full accuracy. A step input will not cause any hang-up condition. Intermediate transparent latches, on all angle and velocity outputs, assure that valid data is always available. Our synthetic reference compensates for ±60° phase shifts, thus eliminating the need for individual compensation networks.

Built-In Test (BIT) / Diagnostic capability

This board incorporates major diagnostics that offer substantial improvements to system reliability because the user is alerted to channel malfunction. This approach reduces bus traffic, because the Status Registers need not be constantly polled. Three different tests (one on-line and two off-line) can be selected.

The on-line (D2) Test initiates automatic background BIT testing. Each channel is checked every 5° to a testing accuracy of 0.05° and each Signal and Reference is always monitored. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 1 second, to verify that background bit testing is activated. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled.

The off-line (D3) Test initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. Results can be read from registers and external reference is not required. Any failure triggers an Interrupt (if enabled). The testing requires no external programming, and can be initiated or stopped.

The off-line (D0) Test is used to check the card and the system interface. All channels are disconnected from the outside world, allowing the user to write any angle to all channels on the card and then to read the data from the interface. External reference is not required.

Data

Data Hi Type: 16-bit unsigned integer
Data Hi & Lo Type: 24-bit unsigned integer (Multi-Speed Applications)
Range: 0 to 359.9945 degrees
Read/Write: R

For Single Speed (Ratio=1) applications, read *Data High* register of that channel. For Multi-Speed applications, read *Data High* register of the even channel (2 or 4) for that pair where 16-bit resolution is required. LSB is approximately 0.0055 degrees.

For Multi-Speed requirements, better than 16-bit resolution is available by utilizing *Data High* and *Data Low* registers combined to determine measured angle with up to 24-bit resolution. First read *Data Low* word, then *Data High* word. *Data Low* word, when read, latches the data high word. *Data High* word, when read, unlatches data. LSB is dependant upon Ratio. A gear ratio of 256 provides for a 24-bit resolution, a ratio of 128 provides for a 23-bit resolution, and so on. The N-speed information (Multi-Speed, Fine) from the synchro should be connected to the even channel of that pair. The pairs are defined as Ch.1 & 2 and Ch.3 & 4. **NOTE:** Per bit angle values in below table are approximate.

DATA HIGH REGISTER																**DATA LOW REGISTER**															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
180	90	45	22.5	11.2	5.62	2.81	1.40	0.703	0.352	0.176	0.088	0.044	0.022	0.011	0.0055	0.00274	0.00137	0.00068	0.00034	0.00017	0.00008	0.00004	0.00002	X	X	X	X	X	X	X	X
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	X	X	X	X	X	X	X	X

Velocity

Type: Two 16-bit two's complement words
Range: 0x7FFF maximum CW rotation to 0x8000 maximum CCW
Read/Write: R
Initialized Value: N/A

Read Velocity Registers of each channel as a two's complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

- When max. velocity is set to 190.7348 rps, an actual speed of 10 rps CW would be read as 06B5h.
- When max. velocity is set to 190.7348 rps, an actual speed of -10 rps CCW would be read as F94Bh.
- When max. velocity is set to 63.5783 rps, an actual speed of 10 rps CW would be read as 1421h.
- When max. velocity is set to 63.5783 rps an actual speed of -10 rps CCW would be read as EBDFh.

To convert a velocity word to rps: **Velocity in rps = Maximum x Output / Full Scale**

Example: If Velocity Output were EBDFh, and maximum velocity were 63.5783 RPS, then

Velocity in rps = 63.5783 x EBDFh / 32,768 = 63.5783 x -5153 / 32,768 = -10 rps

REGISTER	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
VELOCITY High (VEL HI)	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT, 2's Complement
REGISTER	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	FUNCTION
VELOCITY Lo (VEL Lo)	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT, 2's Complement

Bandwidth (BW)

The bandwidth for each channel is individually programmable, between 6 and 1280 (in 2 Hz increments), when Bandwidth Select Register is set for "manual" mode. When operating in "manual mode" (please see/note Bandwidth Selection register description), write desired BW as unsigned integer to associated channel register. All values greater than 1280 will be processed as 1280Hz. All values less than 6 will be processed as 6 Hz. **Example:** BW of 40 Hz = 028h. When the bandwidth select register is set for "automatic mode", the automatic bandwidth (as calculated and set by the card algorithm) can be read. The minimum BW is 10 Hz, and the maximum BW is 100 Hz.

Bandwidth Select

BW Select register sets “Automatic” or “Manual” Bandwidth control. This register is bitmapped per channel; (i.e. D0 = CH1, D1 = CH2, etc.). “1” indicates automatic bandwidth. “0” indicates manual control.

~~The Automatic BW feature, when enabled, reads the input reference frequency and automatically adjusts the BW to approximately 1/10 of the carrier frequency. This Auto BW range will be a minimum of 10 Hz with a maximum of 100 Hz.~~

Note

12/17/14: Due to user feedback received from the field regarding the Automatic Bandwidth setting, NAI advises that only Manual Bandwidth be used until further notice. We are working towards clarification of this and will update this section when it has been accomplished. For questions, please contact NAI Support.

When in “Manual BW” mode, the user can enter the BW between a range of 6 Hz and 1280 Hz, in 2 Hz increments.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	Ch4	Ch3	Ch2	Ch1	FUNCTION
BANDWIDTH SELECT	X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D	D=DATA BIT

Ratio

Type: 16-bit unsigned integer
Range: 1 to 256
Read/Write: R/W
Initialized Value: 1 (Single-Speed)

Enter the desired ratio, as an integer number, in the *Ratio* Register corresponding to the pair of channels to be used for a two-speed, or multi-speed configuration. **Example**, 36:1 = integer 36. Default is for single speed applications where Ratio = 1.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RATIO	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

Active Channels

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Set the bit corresponding to each channel to be monitored during BIT testing in the *Active Channel* register. Set bit to “1” for active channels and clear bit to “0” for those not used. Omitting this step will produce false alarms, because unused channels will set faults.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ACTIVE CHANNEL	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL ENABLE BIT

Latch (Track/Hold)

Type: 16-bit unsigned integer
Range: 0 or 2
Read/Write: R/W
Initialized Value: 0

Writing the integer “2” to the *Latch* register will cause all the S/D channels to be latched. Reading a particular channel will disengage the latch for that channel. Writing a “0” to this register will disengage latch on all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
LATCH	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Test (D2) Verify

Card will write 55h at *Test (D2) Verification* register when (D2) is enabled, approximately every one second. User can clear to 00h and then read again, after approximately one second, to verify that background bit testing is activated.

Test Enable

Set bit to enable associated Built-In Self Test D3, D2, or D0.

Write "1" to D2 to initiate automatic background BIT testing. Card will (every 1 second) write 55h at *Test (D2) verifiy* register when D2 is enabled. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 1 second, to verify that background bit testing is activated. D3 test cycle is completed within 45 seconds and results can be read from the associated status registers when D3 changes from "1" to "0". Any failure triggers an Interrupt (if enabled). All testing requires no external programming and is initiated by writing "1" or terminated by writing "0".

The (D2) Test initiates automatic background BIT testing. Each channel is checked every 5° to a testing accuracy of 0.05° and each Signal and Reference is always monitored. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled.

The (D3) Test initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. Results can be read from registers and external reference is not required. Any failure triggers an Interrupt (if enabled). The testing requires no external programming, and can be initiated or stopped.

The (D0) Test is used to check the card and the interface. All channels are disconnected from the outside world, allowing the user to write any angle to all channels on the card and then to read the data from the interface. External reference is not required.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0

Test Angle

Type: 16-bit unsigned integer
Range: 0 to 359.9945 degrees
Read/Write: W
Initialized Value: 30°

Enter the D0 test angle as per table.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	approximate value
TEST ANGLE	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT (Degrees)

Synchro/Resolver Select

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Individually configure each channel for input signal measurement format:

- Synchro=11
- Resolver=00.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SYNCHRO / RESOLVER	X	X	X	X	X	X	X	X	**CH4**		**CH3**		**CH2**		**CH1**		CHANNEL BIT

Angle Δ

Type: 16-bit unsigned integer
Range: 0.05 to 180 degrees
Read/Write: R/W
Initialized Value: 0

Enter the minimum differential angle to associated channel *Angle Δ* register required to trigger an angle change alert. See Angle Δ Alert register description for details. MSB=180°; minimum differential is 0.05°.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	approximate value
ANGLE Δ	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Degrees)

Angle Δ INIT

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Used in conjunction with *Angle Δ* and *Angle Δ Alert* registers. Set the bit corresponding to each channel to be monitored for angle change alert which is reported in the S/D angle change status register. Set bit to "1" for monitoring channels and clear bit to "0" for those not used.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL ENABLE BIT

Input Reference Frequency Measurement

Each individual channel input reference frequency is measured and the value is reported to a corresponding read register. The input reference frequency is reported to a resolution of 0.01 Hz. The output is in integer decimal format. **For example**, if channel 1 input reference is 400 Hz, the output measurement word from the corresponding register would be 40,000.

Input Signal Voltage (V_{L-L}) Measurement

Each individual channel input signal voltage "V_{L-L}" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input signal voltage is 11.8 VRMS, the output measurement word from the corresponding register would be 1180.

Input Reference Voltage (VREF) Measurement

Each individual channel input reference voltage "VREF" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input signal voltage is 11.8 VRMS, the output measurement word from the corresponding register would be 1180.

A & B Resolution

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Individually configure encoder output resolution or commutation for each channel.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
A & B RESOLUTION	**D**	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	D=DATABIT
Integer 0	**0**													**0**	**0**	**0**	16 bit Encoder Resolution
Integer 1	**0**													**0**	**0**	**1**	15 bit Encoder Resolution
Integer 2	**0**													**0**	**1**	**0**	14 bit Encoder Resolution
Integer 3	**0**													**0**	**1**	**1**	13 bit Encoder Resolution
Integer 4	**0**													**1**	**0**	**0**	12 bit Encoder Resolution
Integer 32768	**1**													**0**	**0**	**0**	4 Pole Commutation
Integer 32769	**1**													**0**	**0**	**1**	6 Pole Commutation
Integer 32770	**1**													**0**	**1**	**0**	8 Pole Commutation

Signal Loss Threshold

Each individual channel input signal voltage “VL-L” is measured and the value reported to a corresponding read register. The signal loss detection circuitry can be tailored to report a signal loss (at SIG Status register) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format**. For example**, if channel 1 input signal loss voltage threshold is to be 7 VRMS, the programmed word to the corresponding register would be 700 (2BCh).

Reference Loss Threshold

Each individual channel input reference voltage “VREF” is measured and the value reported to a corresponding read register. The reference loss detection circuitry can be tailored to report a reference loss (at REF Status register) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format. **For example**, if channel 1 input reference loss voltage threshold is to be 20 VRMS, the programmed word to the corresponding register would be 2000 (7D0h).

Velocity Scale

Type: 16-bit unsigned integer
Range: 11.9209 rps to 190.7348 rps
Read/Write: R/W
Initialized Value: N/A

The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (rps). The scale factor is: **4096 (190.7348 rps / max rps),** where the max rps is selected by the user to achieve the maximum resolution for a desired RPS. Enter the scale factor as an integer to the corresponding *Velocity Scale* register for that particular channel.

To scale the Max Velocity word for 190.7348 rps, set Velocity Scale Factor = 4096 □max velocity word of +32,767 (7FFFh) being 190.7348 rps for CW rotation, and -32,768 (8000h) being 190.7348 rps for CCW rotation). Scaling affects only the Velocity output word and not the dynamic performance.

Examples:

- To get a maximum velocity word (32,767) @ 190.7348 rps, Scale Factor = 4096 (190.7348 / 190.7348) = 4096 = 1000h; this is a velocity resolution of: (190.7348 rps/32,767) x 360°/rps = 2.0955 °/sec (factory default)
- To get a maximum velocity word (32,767) @ 63.5783 rps, Scale Factor = 4096(190.7348/63.5783) = 12,288 = 3000h; this is a velocity resolution of: (63.5783 rps / 32,767) x 360°/rps = 0.6985 °/sec
- To get a maximum velocity word (32,767) @ 11.9209 rps, Scale Factor = 4096(190.7348/11.9209) = 65,520 = FFF0h; this is a velocity resolution of: (11.9209 rps / 32,767) x 360°/rps = 0.1310 °/sec (lowest setting)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VELOCITY SCALE	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Signal Status

Type: binary word
Range: N/A
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Signal Status. A Signal input loss to that channel will trigger a bit failure (=1) on a per channel basis. Passing status (=0). Signal Loss is indicated after 2 seconds. Signal input monitoring is disabled during D3 or D0 Test. Any Signal Status failure, transient or intermittent, will latch the *Signal Status* register. Reading any status bit will unlatch the entire register. Signal Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Signal Loss Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	CHANNEL STATUS BIT

Reference Status

Type: binary word
Range: N/A
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Reference Status. A Reference input loss to that channel will trigger a bit failure (=1) on a per channel basis. Passing status (=0). Signal and/or Reference Loss is indicated after 2 seconds. Signal and Reference input monitoring is disabled during D3 or D0 Test. Any Reference Status failure, transient or intermittent, will latch the *Reference Status* register. Reading any status bit will unlatch the entire register. Reference Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Reference Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
REFERENCE STATUS	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	CHANNEL STATUS BIT

S/D Lock Loss Status (Two Speed Lock-Loss)

Type: binary word
Range: N/A
Read/Write: R
Initialized Value: N/A

When two Synchros are geared to each other in order to achieve higher accuracy, either electrically or mechanically, the misalignment of the Coarse and Fine Synchros must not exceed 90°/gear ratio or the digital angle output may not be valid. Should this problem occur within a given channel pair, the corresponding bit in *Two-Speed Lock-Loss* register will be set to "1".

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
S/D LOCK STATUS	X	X	X	X	X	X	X	X	X	X	X	X	3,4	X	1,2	X	CHANNEL PAIR

S/D Angle Change Status (Angle Δ Alert)

Type: binary word
Range: 0 to 15
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Angle Δ Alert Status. Angle Δ Alert Status Data bit (Ch.n, where n is 1 to 4) is set to "1" and indicates that the angle position of that channel has exceeded the minimum differential angle specified in the *Angle Δ* register. Status is latched. Reading any status bit will unlatch the entire register. Angle Change Alert part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Angle Δ Alert Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE Δ ALERT	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	CHANNEL STATUS BIT

Signal Status Interrupt Enable

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal input loss will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Signal Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	INTERRUPT ENABLE

Reference Status Interrupt Enable

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a reference input loss will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Reference Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
REFERENCE STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	INTERRUPT ENABLE

BIT Status Interrupt Enable

Range: 0 to 15
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 0 to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	INTERRUPT ENABLE

S/D Lock Loss Status Interrupt Enable

Type: binary word
Range: N/A
Read/Write: R
Initialized Value: N/A

When two Synchros are geared to each other in order to achieve higher accuracy, either electrically or mechanically, the misalignment of the Coarse and Fine Synchros must not exceed 90°/gear ratio or the digital angle output may not be valid. Should this problem, which is defined as lock-loss, occur within a given channel pair, the corresponding bit in the *Two-Speed Lock-Loss* register will be set to "0".

Set the bit to enable interrupts for the corresponding channel. When enabled by writing a "1" in the corresponding channel pair, a "Lock Loss" status will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the S/D Lock Loss Interrupt Vector.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
S/D LOCK LOSS INTR ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	**3,4**	X	**1,2**	X	CHANNEL PAIR

S/D Angle Change (Angle Δ Alert) Interrupt Enable

Type: binary word
Range: 0 to 15
Read/Write: R/W
Initialized Value: 0
Set the bit to enable interrupts for the corresponding channel. When enabled, an angle Δ alert will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Angle Δ Alert Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE Δ INTR ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

OSC (Optional Onboard Reference Supply) Set Frequency

Type: 16-bit unsigned integer
Range: 47 to 10,000 Hz
Read/Write: R/W
Initialized Value: N/A
Program Reference Frequency, where LSB is 0.01 Hz**. For example**: To program 400 Hz, 400 x 100= 40,000, which equals 0x9C40. In this example, 0x0000 would be programmed in the *Reference Frequency High* register, and 0x9C40 would be programmed in the *Reference Frequency Low* register. To program 10,000 Hz, 10,000 x 100= 1,000,000, which equals 0xF4240. In this example, 0x000F would be programmed in the *Reference Frequency High* register, and 0x4240 would be programmed in the *Reference Frequency Low* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	327.68	163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	0.01	approximate value
REF FREQUENCY LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	0	0	0	0	0	0	5242.88	2621.44	1310.72	655.36	approximate value
REF FREQUENCY HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

OSC (Optional Onboard Reference Supply) Set Voltage

Type: 16-bit unsigned integer
Range: 2.0 to 28.0 VRMS, or 115 VRMS
Read/Write: R/W
Initialized Value: N/A
Program Reference Voltage, where LSB is 0.01 VRMS**. For example**: To program 26.1 VRMS, 26.1 x 100= 2610, which equals 0xA32. In this example, 0x0000 would be programmed in the *Reference Voltage High* register, and 0x0xA32 would be programmed in the *Reference Voltage Low* register. To program 115 VRMS, 115 x 100= 11,500, which equals 0x2CEC. In this example, 0x0000 would be programmed in the *Reference Voltage High* register, and 0x2CEC would be programmed in the *Reference Voltage Low* register. **Note**: *Reference Voltage High* register always remains at 0x0000.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	81.92	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	0.01	approximate value
REF VOLTAGE LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (V)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	approximate value
REF VOLTAGE HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (V)

Interrupt Vector

Write 16-bit integer (0-255). Used for failure reports.

The Interrupt Vector Registers store the vectors for the specific interrupts generated by the module. If the same vector is loaded into each register, the same interrupt routine will be invoked by all interrupts. If unique vectors are loaded into the registers, a different Interrupt Service Routine (ISR) can be invoked by each interrupt.

- The Signal Loss interrupt vector will be serviced when the Signal Loss status is set and the interrupt has been enabled.
- The Reference Loss interrupt vector will be serviced when the Reference Loss status is set and the interrupt has been enabled.
- The BIT interrupt vector will be serviced when the Bit (failure) status is set and the interrupt has been enabled.
- The Lock Loss interrupt vector will be serviced when the Lock Loss status is set and the interrupt has been enabled.
- The Angle Δ interrupt vector will be serviced when the Angle Δ status is set and the interrupt has been enabled.

S/D FIFO Buffer Operational Description

S/D Data:

The available data in the FIFO buffer can be retrieved in the following registers one "WORD" (16bits) at a time. The data is presented in 16-bit unsigned integer format.

Description	S/D Data (16-bit hex)
Data Ch1-4	Data Range: (0x0000-0xFFFF)

Words in FIFO (Count):

This is a counter that reports the number of data in WORD (2 byte) stored in the FIFO buffer. Every time a read operation is made to the S/D Data memory address, its corresponding "Words in FIFO" counter will be decremented by one. The maximum number of words that can be stored in the FIFO is 65,535 (0xFFFF).

Description	Words in FIFO (16-bit hex)
Words in Ch1-4	Data Range: (0x0000-0xFFFF)

FIFO Status:

The FIFO status register indicates the current condition of the FIFO buffer. B0-B4 is used to show the different condition of the buffer.
B0 = Empty. When "Words In FIFO" register is zero, B0 = 1; otherwise B0 =0.
B1 = Low Limit. When "Words In FIFO" register" < "Low-Threshold", B1= 1; otherwise B1 =0.
B2 = High Limit. When "Words In FIFO" register" > "Hi-Threshold", B2=1; otherwise B2 =0.
B3 = FIFO Full. When "Words In FIFO" register" = 65,535; B3=1; otherwise B3 =0.
B4 = Sample Done. When "Words In FIFO" register = "Size", B4=1; otherwise B4 =0.

Description	FIFO Status (16-bit hex)
Status in Ch1-4	Data Range: B0-B4

Hi-Threshold:

The Hi-threshold level is used to set or reset the high limit bit (B2) of the individual channel status register in the memory location. When the "Words in FIFO" counter is greater than the value stored in the hi-threshold register, the high limit bit (B2) of the channel status register will be set. When the "Words in FIFO" counter is less than or equal to the value stored in the hi-threshold, the high limit bit (B2) of the channel status register will be reset.

Set = "logic 1"
Reset = "logic 0"

Description	Hi-Threshold (16-bit hex)
Hi-Threshold in Ch1-4	Data Range: (0x0000-0xFFFF)

Low-Threshold:

The low-threshold level is used to set or reset the low limit bit (B1) of the individual channel status register in the memory location. When the "Words in FIFO" counter is greater than or equal to the value stored in the low-threshold, the low limit bit (B1) of the channel status register will be reset. When the "Words in FIFO" counter is less than the value stored in the low-threshold, the low limit bit (B1) of the channel status register will be set.

Set = "logical 1"
Reset = "logical 0"

Description	Low-Threshold (16-bit hex)
Low-Threshold in Ch1-4	Data Range: (0x0000-0xFFFF)

Delay:

Set the number of delay samples before the actual FIFO data collection begins. The data collected during the delay period will be discarded.

Description	Delay (16-bit hex)
Delay in Ch1-4	Data Range: (0x0000-0xFFFF)

Size:

Set the size of the FIFO buffer. The largest size that a FIFO buffer can be is 65,535 (0xFFFF).

Description	Size (16-bit hex)
Size in Ch1-4	Data Range: (0x0000-0xFFFF)

Sample Rate:

The sample rate sets the sampling rate for the FIFO buffer. The rate is based on the product of 10.24 μs x Sample Rate. For **example**, if the rate is set to 2, the FIFO buffer will be sampling at 10.24μs * 2 = 20.48 μs.

Description	Sample Rate (16-bit hex)
Rate in Ch1-4	Data Range: (0x0000-0xFFFF)

Clear FIFO:

Whenever the clear memory is set or reset for the individual channel, it initializes the "Words in FIFO" to zero. A read to the "S/D Data" register gives aged data.

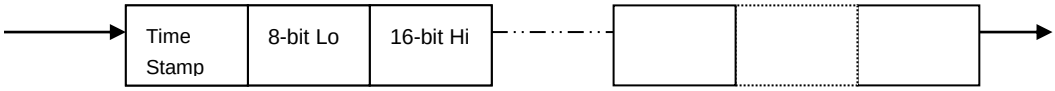
Description	Clear FIFO (16-bit hex)
Clear in Ch1-4	Data Range: (0x0000-0xFFFF)

Buffer Data Type:

Different types of data format can be stored in the FIFO buffer, and their formats are defined by the *Buffer Data Type Register*. The following bit map defines the type/format of data that will be put into the FIFO buffer.

B0 = Data (16-bit Hi). 16-bit resolution data.
B1 = Data (8-bit Lo). Combine with B0 to form a 24-bit resolution.
B2 = Filtered Data (16-bit Hi). Filtered 16-bit resolution data.
B3 = Filtered Data (8-bit Lo). Combine with B2 to form filtered 24-bit resolution.
B4 = Time Stamp. An integer counter that counts from 0 to 65,535 and wraps around when it overflows.
B5 = Reserved
B6 = Reserved
B7 = Reserved

Note: Each data format (B0 – B4) requires one word of storage space from the FIFO buffer. **For example**, if B0, B1 and B4 are set (0x13) and the Size register is set to 1, a FIFO write will put 3 words of data to the FIFO memory spaces. Since the maximum physical size of FIFO is 65,535 for each channel, the value in the Size and Buffer Control register could cause an overflow to the FIFO buffer. When an overflow condition occurs, any un-stored data will be lost.



Description	Buffer Ctrl.(16-bit hex)
Buf. Ctrl. in ch1-4	Data Range: B0-B4

Trigger Mode:

The FIFO can be started/triggered by different sources.
B0-B1 = Source Select (choose one only)
0x0 = Ext. Trigger 2
0x1 = Ext. Trigger 1
0x2 = Software Trigger
B3 = Reserved
B4-B7 = Trigger Type (Choose one only)
0x10 = Negative Slope
0x20 = Trigger Pulse Enable
0x40 = Trigger Pulse/Trigger Enable Select
0x80 = Trigger Clear

Register Write	Trig Source	Slope
0x20	Ext Trigger 2	Positive
0x21	Ext Trigger 1	Positive
0x22	SW Trigger	Positive (don't care)
0x30	Ext Trigger 2	Negative
0x31	Ext Trigger 1	Negative
0x32	SW Trigger	Negative (don't care)
0x40	Initiate	
0x80	Stop (Clear Trigger)	

Description	Trigger Ctrl.(16-bit hex)
Trigger Ctrl. in Ch1-4	Data Range: B0-B7

Interrupt:

Pending (To be determined)

Description	FIFO Status (16-bit hex)
Status in Ch1-4	Data Range: 0x0-0xFFFF

Software Trigger:

Software trigger is used to start the FIFO buffer and the collection of data. In order to use this operation, the "Trigger Ctrl" register must be set up accordingly. Setting or resetting the "Software Trigger" will start FIFO data collection for ALL channels.

Description	Software Trigger (16-bit hex)
Software Trigger	Data Range: 0x0-0xFFFF

Status, BIT Fail

Type: binary word
Range: 0 to 15
Read/Write: R

Initialized Value: 0

BIT status is part of background testing and the status register may be checked or polled at any given time. BIT status reports correct operation (with specification) for channel accuracy to programmed values. Any failure of frequency, amplitude of DC offset will trigger a bit failure (=1) on a per channel basis. Passing status (=0). Status is latched; reading register unlatches BIT status. BIT is operating at all times and cannot be enabled or disabled using the General use Test Enable register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding “latching” – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are “latching”; as defined, any noted transitional change on any channel will “latch” the entire Status Register.
- Once latched, there will be no further state change “sensed” by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will “unlatch” that particular status register (doesn’t necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will “latch” the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read “until cleared”.

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- Power-up
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern (“loop to clear”) - this would also be similar to an Interrupt Service Routine (ISR) “loop to clear” function.

    Ex: Running the ‘loop to clear’ on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are “cleared” and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- Interrupt Software Routine (ISR)

  The ISR is typically a software (SW) handling branch (part of host application software) structured to “loop to read and clear” the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should “read” the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were “latched” – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively “re-arm” for the next transition to occur.

  Ex: The ISR should have the ‘loop to clear’ – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also “latch” the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

S/D (MODULES S*) VME MEMORY MAP

000	SD1 Data Lo	R	068	SD1 Measured VREF		R	320	CH1 Data Buffer Hi Threshold	W/R
002	SD1 Data Hi	R	06A	SD2 Measured VREF		R	322	CH1 Data Buffer Lo Threshold	W/R
004	SD2 Data Lo	R	06C	SD3 Measured VREF		R	324	CH1 Buffer Delay Sample	W/R
006	SD2 Data Hi	R	06E	SD4 Measured VREF		R	326	CH1 Buffer # of Samples	W/R
008	SD3 Data Lo	R					328	CH1 Buffer Sample Rate	W/R
00A	SD3 Data Hi	R	070	SD1 Encoder Resolution		W/R	32A	CH1 Clear FIFO	W/R
00C	SD4 Data Lo	R	072	SD2 Encoder Resolution		W/R	32C	CH1 Buffer Data Type	W/R
00E	SD4 Data Hi	R	074	SD3 Encoder Resolution		W/R	32E	CH1 Buffer Trigger Mode	W/R
			076	SD4 Encoder Resolution		W/R			
010	SD1 VEL Lo	R	080	SD1 Signal Loss Threshold		W/R	330	CH2 Data Buffer Hi Threshold	W/R
012	SD1 VEL Hi	R	082	SD2 Signal Loss Threshold		W/R	332	CH2 Data Buffer Lo Threshold	W/R
014	SD2 VEL Lo	R	084	SD3 Signal Loss Threshold		W/R	334	CH2 Buffer Delay Sample	W/R
016	SD2 VEL Hi	R	086	SD4 Signal Loss Threshold		W/R	336	CH2 Buffer # of Samples	W/R
018	SD3 VEL Lo	R	088	SD1 REF Loss Threshold		W/R	338	CH2 Buffer Sample Rate	W/R
01A	SD3 VEL Hi	R	08A	SD2 REF Loss Threshold		W/R	33A	CH2 Clear FIFO	W/R
01C	SD4 VEL Lo	R	08C	SD3 REF Loss Threshold		W/R	33C	CH2 Buffer Data Type	W/R
01E	SD4 VEL Hi	R	08E	SD4 REF Loss Threshold		W/R	33E	CH2 Buffer Trigger Mode	W/R
020	SD1 Bandwidth	W/R	0A8	SD1 VEL SCALE		W/R	340	CH3 Data Buffer Hi Threshold	W/R
022	SD2 Bandwidth	W/R	0AA	SD2 VEL SCALE		W/R	342	CH3 Data Buffer Lo Threshold	W/R
024	SD3 Bandwidth	W/R	0AC	SD3 VEL SCALE		W/R	344	CH3 Buffer Delay Sample	W/R
026	SD4 Bandwidth	W/R	0AE	SD4 VEL SCALE		W/R	346	CH3 Buffer # of Samples	W/R
028	Bandwidth Select	W/R					348	CH3 Buffer Sample Rate	W/R
			0E8	SIG Status	CH1-4	R	34A	CH3 Clear FIFO	W/R
02A	SD Ratio ½	W/R	0EA	REF Status	CH1-4	R	34C	CH3 Buffer Data Type	W/R
02C	SD Ratio ¾	W/R	0EE	SD Lock Status	CH1-4	R	34E	CH3 Buffer Trigger Mode	W/R
02E	SD Active Channels	W/R	0F0	SD Angle Δ Status	CH1-4	R			
030	SD Track / Hold	W/R					350	CH4 Data Buffer Hi Threshold	W/R
032	D2 Test Verify	W/R	0F2	SIG Status Interrupt Enable	CH1-4	W/R	352	CH4 Data Buffer Lo Threshold	W/R
034	Test Enable	W/R	0F4	REF Status Interrupt Enable	CH1-4	W/R	354	CH4 Buffer Delay Sample	W/R
036	Test Angle	W/R	0F6	BIT Status Interrupt Enable	CH1-4	W/R	356	CH4 Buffer # of Samples	W/R
03C	SD SYN/RSL SELECT	W/R	0F8	SD Lock Status Interrupt Enable	CH1-4	W/R	358	CH4 Buffer Sample Rate	W/R
			0FA	SD Angle Δ Interrupt Enable	CH1-4	W/R	35A	CH4 Clear FIFO	W/R
040	SD1 Angle Δ	W/R					35C	CH4 Buffer Data Type	W/R
042	SD2 Angle Δ	W/R	100	OSC Set Freq Lo		W/R	35E	CH4 Buffer Trigger Mode	W/R
044	SD3 Angle Δ	W/R	102	OSC Set Freq Hi		W/R			
046	SD4 Angle Δ	W/R	104	OSC Set Volt Lo		W/R	360	Software Trigger	W/R
048	Angle Δ Enable	W/R	106	OSC Set Volt Hi		W/R	380	BIT Status (CH1-4)	W/R
050	SD1Measured Ref Freq Lo	R	300	FIFO Buffer Data	CH1	R	3B4	Module Design Version	R
052	SD1Measured Ref Freq Hi	R	302	FIFO Buffer Data	CH2	R	3B6	Module Design Revision	R
054	SD2 Measured Ref Freq Li	R	304	FIFO Buffer Data	CH3	R	3B8	Module DSP Rev	R
056	SD2 Measured Ref Freq Hi	R	306	FIFO Buffer Data	CH4	R	3BA	Module FPGA Rev	R
058	SD3 Measured Ref Freq Lo	R	308	FIFO Buffer Count	CH1	R	3BC	Module ID	R
05A	SD3 Measured Ref Freq Hi	R	30A	FIFO Buffer Count	CH2	R			
05C	SD4 Measured Ref Freq Lo	R	30C	FIFO Buffer Count	CH3	R	3E0	Vector Signal Loss	W/R
05E	SD4 Measured Ref Freq Hi	R	30E	FIFO Buffer Count	CH4	R	3E2	Vector REF Loss	W/R
							3E4	Vector BIT Fail	W/R
060	SD1 Measured V_{L-L}	R	310	FIFO Status	CH1	R	3E6	Vector Lock Loss	W/R
062	SD2 Measured V_{L-L}	R	312	FIFO Status	CH2	R	3E8	Vector Angle Δ	W/R
064	SD3 Measured V_{L-L}	R	314	FIFO Status	CH3	R			
066	SD4 Measured V_{L-L}	R	316	FIFO Status	CH4	R			

D/S THREE CHANNEL (MODULE 6*)

(*See part number designation)

Principle of Operation

This new Digital-to-Synchro/Resolver (D/S) module features a solid state design that eliminates the need for external transformers. This design is an isolated three channel synchro or resolver format, 0.25 VA design. All outputs are short circuit protected and any leg can be grounded without affecting performance. Any channel can be programmed for rotation, either continuous or with start/stop angles.

New features in this module now include a wrap capability for measuring each channel's commanded output angle and carrier frequency. The module's extensive programmability now includes optional format selections (synchro or resolver). A background calibration feature (pending), that is totally transparent to the operation of the channels, constantly adjusts outputs for all load and environmental conditions. Each channel can be programmed for a different output voltage, which can be programmed for either ratio-metric or absolute (fixed) output. Module power ON/OFF capability provided for shutting down channels.

Built-In Test (BIT) / Diagnostic Capability

Two different tests (one on-line and one off-line) can be selected:

The on-line (D2) Test initiates automatic background BIT testing that checks the output accuracy of each channel by comparing the measured output angle to the commanded angle. Each channel is individually checked to an accuracy of 0.2° and each D/S Signal output and Reference input is continually monitored. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 0.1 seconds, to verify that background bit testing is activated. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. **The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card,** and can be enabled or disabled.

The off-line (D3) Test initiates a BIT test that generates and tests 24 different angles to a test accuracy of 0.2°. Results can be read from registers. External reference is required and outputs must be on. Any failure triggers an Interrupt (if enabled). Testing requires no external programming, and can be initiated or stopped at any time.

CAUTION: Outputs must be ON and Reference supplied during this test and therefore active. Check connected loads for possible interaction.

* See Note 7 in *Part Number Designation* for detailed parameter characteristics

Wrap S/D Angle Read

Read individual channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Wrap S/D Data (°) Hi	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Wrap S/D Data (°) Lo	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X

Input Reference Voltage Measurement

Each individual channel input signal voltage "VREF" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input REF voltage is 26.0 VRMS, the output measurement word from the corresponding register would be 2600.

Input Signal Voltage (V_{L-L}) Measurement

Each individual channel output signal voltage "V_{L-L}" is measured and the value reported to a corresponding read register. The output voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 output signal voltage is 11.8 VRMS, the output measurement word from the corresponding register would be 1180.

Signal Loss Threshold

Each individual channel output signal voltage "V_{L-L}" is measured and the value reported to a corresponding read register. The signal loss detection circuitry can be tailored to report a signal loss (at Signal Loss Status register) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format. For example, if channel 1 signal loss voltage threshold is to be 7 VRMS, the programmed word to the corresponding register would be 700 (2BCh).

Reference Loss Threshold

Each individual channel input reference voltage "VREF" is measured and the value reported to a corresponding read register. The reference loss detection circuitry can be tailored to report a reference loss (at Reference Loss Status register) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format. For example, if channel 1 input reference loss voltage threshold is to be 20 VRMS, the programmed word to the corresponding register would be 2000 (7D0h).

D/S Channel Frequency

Each individual channel Reference Frequency is measured and the value reported to a corresponding read register. The input reference frequency is reported to a resolution of 1 Hz. The output is in integer decimal format. For example, if channel 1 input excitation is 400 Hz, the output measurement word from the corresponding register would be 400.

D/S Status, Signal Loss

Type: binary word

Range: N/A

Read/Write: R

Initialized Value: 0

Check the corresponding bit for a channel's Signal Status. A Signal input loss to that channel will trigger a bit failure (=1) on a per channel basis; Passing status (=0). Signal Loss is indicated after 2 seconds. Signal input monitoring is disabled during D3 or D0 Test. Any Signal Status failure, transient or intermittent, will latch the *Signal Status* register. Reading any status bit will unlatch the entire register. Signal Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Open Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Status, Signal Loss	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1	Channel Status BIT

D/S Write Angle – Single Speed

For single-speed applications (Ratio=1), write an "up to" 24-bit integer to the corresponding channel *D/S Data Register.* (ex. 330° (in 16bit resolution) = EAABh written to Data Hi register only); 330° (in 24bit resolution) = EAAAAB – note that "EAAA" is written to Data Hi register and "AB00" is written to Data Lo register).

WORD = (Angle ÷ (360/2^{24})).

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Write Data (°) Hi	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
D/S Write Data (°) Lo	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X

Note: Writing to an Input Angle Register will stop any rotation initiated on that channel

D/S Write Angle – Two Speed

The module can automatically simulate two-speed applications (applies only to multiple channel modules). Write an “up to” 24-bit integer to the corresponding channel *D/S Write Angle Register* to the coarse (channel 1) channel. By entering a ratio in the *D/S Ratio 1/2 register*, the fine (channel 2) channel will automatically output a signal proportional to the programmed coarse channel times the ratio programmed.

D/S Stop Angle

Write the desired stop angle to appropriate channel Stop Angle Register. Write a 16-bit integer (or 16-bit 2’s complement integer) to the corresponding channel *D/S Data Register.* (ex. 330° = EAABh).

WORD = (Angle ÷ (360/2^{16})).

Note: Writing to an Input Angle Register will stop any rotation initiated on that channel

D/S Rotation

Each channel may be configured for either start/stop or continuous rotation for applications that require it. In start/stop mode, the user can program a rotational velocity and a stop angle. When triggered, either via a software command or external pulse (selectable trigger mode), the output signal will start at the current position and simulate rotation at the specified rotation rate and stop at the programmed stop angle. Re-initiating the trigger will repeat the rotation. In continuous mode, the user will program a rotation rate and trigger the start of the rotation either via software command or external trigger. Stopping rotation can be accomplished by either issuing a stop rotation command or setting a commanded angle. Clockwise or counter-clockwise rotation is accomplished by setting either a positive or negative 2’s complement word in the velocity register.

D/S Rotation Rate

Write to the corresponding *Rotation Rate Registers (Hi and Lo)* a 2’s complement number representing the desired rotation rate, LSB = 0.015°/sec.

Ex: 12 RPS = (12 x 360°/0.015° = 288000 = 46500h), -12 RPS = (-12 x 360°/0.015° = -288000 = B9B00h)

Step size is 16 bits (0.0055°) for up to 1.5 RPS, and then linearly decreases to 12 bits (0.088°) at 13.6 RPS.

D/S Rotation Mode, Continuous or Start/Stop

For continuous rotation, set the corresponding channel bit to "0" in the *Rotation Mode Register*. For rotation to cease at a designated stop angle, set the bit to "1". For 2-speed applications, only the odd (coarse) channel needs to be programmed (CH1).

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Rotation Mode	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

Start Rotation

First set the *Rotation Rate* and *Rotation Mode* Registers for each channel that is to rotate. Then, to start rotation for the corresponding channel, write a “1” to the corresponding channel *D/S Start Rotation* register.

Stop Rotation

To stop rotation for the corresponding channel, write a “1” to the corresponding channel *D/S Stop Rotation* register. Channel will remain at the stopped angle until new input angles are set, or rotation is again initiated. Note: An in-process rotation can also be stopped by commanding a new angle (*D/S Write Angle*).

D/S Rotation Status

Check the corresponding bit of the *D/S Rotation Status Register* for status of rotation (Done or Not Done) for each channel. A "1" means Rotation Done (output is static), "0" means Rotation Not Done (output is rotating) on channel. Rotation monitoring is always enabled.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Rotation Status	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Set Reference Voltage

Set required input reference voltage "VREF" to a corresponding register. The input voltage is set with a resolution of 10 mv rms. The setting is in integer decimal format. For example, if channel 1 expected input REF voltage is 26.0 VRMS, the set word to the corresponding register would be 2600.

D/S Set Signal Voltage

Set required output signal voltage "VL-L" to a corresponding register. The output voltage is set with a resolution of 10 mv rms. The setting is in integer decimal format. For example, if channel 1 Signal (VL-L) voltage is to be 11.8 VRMS, the set word to the corresponding register would be 1180.

D/S Test Enable

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X

Set bit to enable associated Built-In Self Test D2 or D3.

The on-line (D2) Test - Writing "1" to the D2 bit of the *D/S Test Enable Register* initiates status reporting of the automatic background BIT testing that checks the output accuracy of each channel by comparing the measured output angle to the commanded angle. The status bits will be set to indicate an accuracy (0.2º) problem and the results can be read from *D/S Status Registers* within 2 seconds and if enabled, an interrupt will be generated (See *Interrupt Register*). Writing a "0" deactivates the status reporting. The testing is totally transparent to the user, requires no external programming, and has no effect on the standard operation of this card. **Note: Outputs must be ON and Reference supplied for test to function.** Card will write 55h (every 0.1 seconds) to the *D/S Test (D2) Verify Register* when D2 is enabled. User can periodically clear to 00h and then read the *D/S Test (D2) Verify Register* again, after 0.1 seconds, to verify that BIT Testing is activated. This test continuously sequences between the channels on the card with each output being measured for approximately 180mSec. If the measured angle has an error greater the 0.2º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.2º during a test cycle, the test cycle will not generally indicate an error.

In addition, each D/S Reference input and signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *D/S Signal* and *D/S Reference Status Registers*.

The off-line (D3) Test - Writing "1" to the D3 bit of the *D/S Test Enable Register* initiates a BIT Test that generates and tests 24 different angles to an accuracy of 0.2°. External reference is required and outputs must be ON. The D/S Status bits will be set to indicate an accuracy problem. Results are available in the *D/S Test Status Registers* and if enabled, an interrupt will be generated (See *Interrupt Register*). Test cycle takes about 30 seconds and the D3 bit changes from "1" to "0" when test is complete. The testing requires no external programming, and can be terminated at any time by writing a "0" to the D3 bit of the *D/S Test Enable Register*.



CAUTION: Outputs must be ON and Reference must be supplied during this test. The outputs are therefore active. Check connected loads for possible interaction.

Test (D2) Verify

Card will write 55h at *Test (D2) Verification* register when (D2) is enabled, approximately every one second. User can clear to 00h and then read again, after approximately one second, to verify that background bit testing is activated.

D/S Ratio 1/2

Set desired ratio between coarse (channel 1) and fine (channel 2) channels. Enter the desired ratio, as an integer number, in the D/S Ratio Register corresponding to the pair of channels to be used as a two-speed channel. Example: Single speed = 1; 36:1 = integer 36. (Ratio range from 1 to 255). By entering a ratio in the *D/S Ratio 1/2 register*, the fine (channel 2) channel will automatically output a signal proportional to the programmed coarse channel times the ratio programmed.

D/S Output Mode

The D/S Output Mode register is utilized for selecting either ratio-metric or absolute (fixed) mode voltages. Ratio-metric Mode, when selected, will cause the output signal voltage of the channel to vary with the input Reference Voltage. Fixed Mode, when selected, will cause the output signal voltage of the channel NOT to vary with the input Reference Voltage. Set corresponding channel bit to “0” for Ratio-metric Mode. Set corresponding channel bit to “1” for Fixed Mode.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Output Mode	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Synchro / Resolver Select

When required, write a “11” or “00” (Synchro = 11; Resolver = 00) to each corresponding channel bit pair, representing a channel commanded output format, of the *Synchro/Resolver Register*.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5 D4		CH2 D2		CH1 D0	
D/S Synchro / Resolver Select	X	X	X	X	X	X	X	X	X	X	D4	D5	D3	D2	D1	D0

D/S Trigger Source Select

Internal = “0x29”; External = “0x28”

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Trigger Source Select	X	X	X	X	X	X	X	X	X	X	**D**	X	D	X	X	**D**

D/S Trigger Slope Select

For positive slope, set the corresponding channel bit to "0" in the Trigger Slope Select Mode Register. For negative slope, set the bit to “1”.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Trigger Slope Select	X	X	X	X	X	X	X	X	X	X	**D**	X	**D**	X	X	**D**

D/S Module Power Enable

The *D/S Module Power Enable* Register is utilized for module channel output/power control.

To power/enable all channels, use D0 bit. Write D0 to 0x0001 to enable power-on all channels. Write 0x0000 to disable power-on to all channels

To control each channel power output individually, ensure that D0 (all channel control bit) is set to 0. To enable individual channel (output "on") set the corresponding bit to "1". To disable individual channel (output "Off") set the corresponding bit to "0".

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Module Power Enable	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1	X	X	X	All CH

Command word	Module/Channel Power Action
0x0000	ALL channels power OFF
0x0001	ALL channels power ON
0x0010	Channel 1 ON (only)
0x0020	Channel 2 ON (only)
0x0030	Channels 1&2 ON (ch 3 OFF)
0x0040	Channels 3 ON (only)
0x0050	Channels 1&3 ON (ch 2 OFF)
0x0060	Channels 2&3 ON (ch 1 OFF)
0x0070	Channels 1&2&3 ON

D/S Active Channels

Set the bit, corresponding to each channel to be monitored during BIT testing, in the Active Channel Register for the particular D/S channel. "1" = Active; "0" = not used.

IMPORTANT - Omitting this step will produce false alarms because unused channels will set faults.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Active Channels	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Status, Reference Loss

This register checks each active channel for the status of the excitation input.

1 = Reference signal loss (LOS: loss of signal)

0 = Reference signal detected at programmed threshold (See Signal Loss Threshold)

Channels that are inactive are also set to "0". (Reference loss is detected after 2 seconds). Reference monitoring is always enabled. Any D/S reference loss detection, transient or intermittent, will latch the *D/S Reference Status Register*. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, Reference Loss	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Status, Phase Lock Loss

Check the corresponding bit of the *D/S Phase Lock Loss* Register for status of the phase lock between the reference input and signal output for each active channel. A "1" means Phase Lock Loss has occurred, "0" means Phase Lock OK on active channels. Channels that are inactive are also set to "0". (Phase Lock loss is detected after 2 seconds). Phase Lock monitoring is always enabled. Any D/S Phase Lock Loss status failure, transient or intermittent, will latch the *D/S Phase Lock Loss Status Register*. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, Phase Lock Loss	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

D/S Set Phase Offset

The phase of each individual channel may be offset from Reference. The phase may be adjusted at a resolution of 0.1 deg / bit. Program the desired lead or lag in integer as a 2's complement word format. For example, if channel 1 output signal is to lead the reference signal by 1.6 degrees, program the corresponding channel phase register to 16 (10h). If channel 1 output signal is to lag the reference signal by 1.6 degrees, program the corresponding channel phase register to -16 (FFF0h). Phase shift range is -90 <= x <= 90.

D/S Status, BIT Test

Check the corresponding bit of the *D/S BIT Test Status* Register for status of BIT (Test-Accuracy) Testing for each "active" channel. A "1" means Accuracy Failed; "0" means Accuracy OK. Channels that are "inactive" are also set to "0". The status bits will be set to indicate an accuracy (0.2º) problem and the results can be read from D/S Status Registers within 2 seconds and, if enabled, an interrupt will be generated (See Interrupt Register).

This test continuously sequences between the channels on the card with each output being measured for approximately 180mSec. If the measured angle has an error greater the 0.2º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.2º during a test cycle, the test cycle will not generally indicate an error.

D/S channels, by default, are set for monitoring the channel background BIT (Built-In-Test) status reporting; "ON" or "ACTIVE". The front panel BIT LED illuminates (Red) if any channel reports a BIT fault. For BIT status to work properly on an "active" channel, the D/S channel must have a valid Reference source applied and the D/S channel power set to "ON" (so there is a valid signal being generated). If channels are not being used, it is recommended that the channel BIT status report be turned off (or set INACTIVE). However, it should be noted that the channel BIT status register latches the contents of a failure until read. Simply setting the channel "INACTIVE" will not clear the BIT status register or extinguish the front panel BIT fault LED if a fault was previously detected.

The *D/S BIT Test Status* register should be queried (read) to insure the register is unlatched which will enable the BIT status register to be re-written during next status update (which, when the channel is set INACTIVE, should clear the fault). Once this is done, the front panel BIT LED will extinguish – as long as the channels that are active are working properly and the channels not being utilized are set INACTIVE.

Note: When *D/S Wrap Select External/Internal* register is set for "external", the BIT wrap will be read from the external amplifier wrap input signals (See pin-out). Also, the BIT tolerance will be adjusted for the amplifier accuracy specification.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Status, BIT Test	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

Reference Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a reference input loss (D/S Status, Reference) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Reference Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reference Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

Signal Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal input loss (D/S Status, Signal Loss) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Signal Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Signal Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

BIT Test Fail Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a BIT Test Failure (D/S Status, BIT Test) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the BIT Test Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Test Fail Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

Phase Lock Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a Phase Lock Loss (D/S Status, Phase Lock Loss) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Phase Lock Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Phase Lock Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

OSC (Optional Onboard Reference Supply) Set Frequency

Type: 16-bit unsigned integer

Range: 47 to 10,000 Hz

Read/Write: R/W

Initialized Value: N/A

Program Reference Frequency, where LSB is 0.01 Hz. For example: To program 400 Hz, 400 x 100= 40,000, which equals 0x9C40. In this example, 0x0000 would be programmed in the *Reference Frequency High* register, and 0x9C40 would be programmed in the *Reference Frequency Low* register. To program 10,000 Hz, 10,000 x 100= 1,000,000, which equals 0xF4240. In this example, 0x000F would be programmed in the *Reference Frequency High* register, and 0x4240 would be programmed in the *Reference Frequency Low* register.

Note: This function register only applies if the platform supports the optional On-Board Reference Supply and the board is actually populated with the "optional" on-board Reference Supply. The optional On-Board Reference Supply does not occupy a physical module slot position.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	327.68	163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	0.01	approximate value
REF FREQUENCY LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	0	0	0	0	0	0	5242.88	2621.44	1310.72	655.36	approximate value
REF FREQUENCY HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

OSC (Optional Onboard Reference Supply) Set Voltage

Type: 16-bit unsigned integer

Range: 2.0 to 28.0 VRMS, or 115 VRMS

Read/Write: R/W

Initialized Value: N/A

Program Reference Voltage, where LSB is 0.01 VRMS. For example: To program 26.1 VRMS, 26.1 x 100= 2610, which equals 0xA32. In this example, 0x0000 would be programmed in the *Reference Voltage High* register, and 0x0xA32 would be programmed in the *Reference Voltage Low* register. To program 115 VRMS, 115 x 100= 11,500, which equals 0x2CEC. In this example, 0x0000 would be programmed in the *Reference Voltage High* register, and 0x2CEC would be programmed in the *Reference Voltage Low* register. Note: *Reference Voltage High* register always remains at 0x0000.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	81.92	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	0.01	approximate value
REF VOLTAGE LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (V)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	approximate value
REF VOLTAGE HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (V)

Interrupt Vector

Write 16-bit integer (0-255). Used for failure reports.

The Interrupt Vector Registers store the vectors for the specific interrupts generated by the module. If the same vector is loaded into each register, the same interrupt routine will be invoked by all interrupts. If unique vectors are loaded into the registers, a different Interrupt Service Routine (ISR) can be invoked by each interrupt.

The *Signal Loss* interrupt vector will be serviced when the *Signal Loss* status is set and the interrupt has been enabled.

The *Reference Loss* interrupt vector will be serviced when the *Reference Loss* status is set and the interrupt has been enabled.

The *BIT* interrupt vector will be serviced when the *Bit (failure)* status is set and the interrupt has been enabled.

The *Lock Loss* interrupt vector will be serviced when the *Lock Loss* status is set and the interrupt has been enabled.

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding "latching" – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are "latching"; as defined, any noted transitional change on any channel will "latch" the entire Status Register.
- Once latched, there will be no further state change "sensed" by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will "unlatch" that particular status register (doesn't necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will "latch" the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read "until cleared".

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern ("loop to clear") - this would also be similar to an Interrupt Service Routine (ISR) "loop to clear" function.

    Ex: Running the 'loop to clear' on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are "cleared" and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

  The ISR is typically a software (SW) handling branch (part of host application software) structured to "loop to read and clear" the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should "read" the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were "latched" – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively "re-arm" for the next transition to occur.

  Ex: The ISR should have the 'loop to clear' – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

Notes:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also "latch" the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

D/S 3 CHANNEL (6*) VME MODULE MEMORY MAP

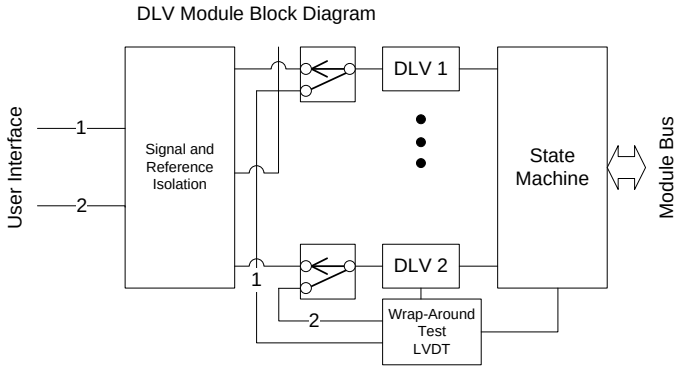
Module Length = 400h

000	Wrap S/D Angle Lo	CH1	R	080	D/S Set Rotation Rate Lo	CH1	W/R	0E6	D/S Reference Status		R
002	Wrap S/D Angle Hi	CH1	R	082	D/S Set Rotation Rate Hi	CH1	W/R	0E8	D/S Phase Lock Status		R
004	Wrap S/D Angle Lo	CH2	R	084	D/S Set Rotation Rate Lo	CH2	W/R	0F4	D/S Set Phase Offset	CH1	W/R
006	Wrap S/D Angle Hi	CH2	R	086	D/S Set Rotation Rate Hi	CH2	W/R	0F6	D/S Set Phase Offset	CH2	W/R
008	Wrap S/D Angle Lo	CH3	R	088	D/S Set Rotation Rate Lo	CH3	W/R	0F8	D/S Set Phase Offset	CH3	W/R
00A	Wrap S/D Angle Hi	CH3	R	08A	D/S Set Rotation Rate Hi	CH3	W/R	0FA	D/S Rotation Status		R
032	REF Voltage (meas.)	CH1	R	0A0	D/S Set Reference Volt Lo	CH1	W/R	198	OSC Set Voltage Lo		W/R
034	REF Voltage (meas.)	CH2	R	0A2	D/S Set Reference Volt Hi	CH1	W/R	19A	OSC Set Voltage Hi		W/R
036	REF Voltage (meas.)	CH3	R	0A4	D/S Set Reference Volt Lo	CH2	W/R	19C	OSC Set Frequency Lo		W/R
038	Signal Voltage (meas.)	CH1	R	0A6	D/S Set Reference Volt Hi	CH2	W/R	19E	OSC Set Frequency HI		W/R
03A	Signal Voltage (meas.)	CH2	R	0A8	D/S Set Reference Volt Lo	CH3	W/R	1D0	D/S Start Rotation		W
03C	Signal Voltage (meas.)	CH3	R	0AA	D/S Set Reference Volt Hi	CH3	W/R	1D2	D/S Stop Rotation		W
040	Signal Loss Threshold	CH1	W/R	0B0	D/S Set Signal Volt Lo	CH1	W/R	380	D/S Status, BIT Test		R
042	Signal Loss Threshold	CH2	W/R	0B2	D/S Set Signal Volt Hi	CH1	W/R	382	D/S Reference Loss Interrupt Enable		W/R
044	Signal Loss Threshold	CH3	W/R	0B4	D/S Set Signal Volt Lo	CH2	W/R	384	D/S Signal Loss Interrupt Enable		W/R
046	REF Loss Threshold	CH1	W/R	0B6	D/S Set Signal Volt Hi	CH2	W/R	386	D/S BIT FAIL Interrupt Enable		W/R
048	REF Loss Threshold	CH2	W/R	0B8	D/S Set Signal Volt Lo	CH3	W/R	388	D/S Phase Lock Loss Interrupt Enable		W/R
04A	REF Loss Threshold	CH3	W/R	0BA	D/S Set Signal Volt Hi	CH3	W/R				
								3E0	Vector Interrupt BIT Fail		W/R
04C	Channel 1 Frequency (meas.)		R	0C0	D/S Test Enable		W/R	3E2	Vector Interrupt Signal Loss		W/R
04E	Channel 2 Frequency (meas.)		R	0C2	D/S Ratio (CH1/2)		W/R	3E4	Vector Interrupt REF Loss		W/R
050	Channel 3 Frequency (meas.)		R	0C4	D2 Test Verify		W/R	3E6	Vector Interrupt Phase Lock Loss		W/R
058	Status, Signal Loss		R	0C6	D/S Output Mode		W/R				
								3B4	Module Design Version		R
060	D/S Write Angle Lo	CH1	W/R	0C8	D/S Rotation Mode		W/R	3B6	Module Design Revision		R
062	D/S Write Angle Hi	CH1	W/R	0CC	D/S SYN/RSL Select		W/R	3B8	Module DSP Revision		R
064	D/S Write Angle Lo	CH2	W/R					3BA	Module FPGA Revision		R
066	D/S Write Angle Hi	CH2	W/R	0D0	D/S Trigger Source Select	CH1	W/R	3BC	Module ID Revision		R
068	D/S Write Angle Lo	CH3	W/R	0D2	D/S Trigger Source Select	CH2	W/R				
06A	D/S Write Angle Hi	CH3	W/R	0D4	D/S Trigger Source Select	CH3	W/R				
072	D/S Stop Angle	CH1	W/R	0D6	D/S Trigger Slope Select		W/R				
074	D/S Stop Angle	CH2	W/R	0E0	D/S Module Power Enable		W/R				
076	D/S Stop Angle	CH3	W/R	0E4	D/S Active Channel Select		W/R				

DLV 3 CHANNEL (MODULE 5*)

(*See part number designation)

Principle of Operation



This Digital-to-LVDT/RVDT (DLV) Simulation Module offers three, 2-wire or 3/4-wire "Programmable" LVDT/RVDT outputs with wrap-around self test. This card can be programmed and re-programmed in the field for any excitation and signal voltage between 2.0 and 28 volts. Operating frequency between 47 Hz and 10 KHz can be specified (See part number). One excitation input is supplied for each output. The output format can be programmed to simulate either two-wire or three/four-wire LVDT's. The transformation ratio (TR), same for each pair of outputs, sets the maximum output voltage with relation to the excitation voltage (TR = Max Output Voltage/Excitation Voltage). Use of a ratiometric design eliminates errors caused by excitation voltage variations; however, an absolute output (one that does not vary with excitation) can be programmed.

New features include a wrap for measuring, of each channel, the output position, current and carrier frequency (Pending). A background calibration feature (pending) will constantly adjust the outputs for load and environmental condition.

Built-in Test/Diagnostic Capability

Extensive Built-In-Test (BIT) diagnostics are implemented which include continuous transparent background accuracy testing as well as user-invoked testing. Two different tests (one on-line and one off-line) can be selected:

The on-line (D2) Test initiates automatic background BIT testing (on-line) that checks the output accuracy of each channel by comparing the measured output position to the commanded position. This test continuously checks each channel individually over the programmed signal range to an accuracy of 0.2% FS. Each DLV Signal output and Excitation input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in registers. User can periodically clear to 00h and then read *Test (D2) verification register* again, after 30 seconds, to verify that background bit testing is activated. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled.

The off-line (D3) Test initiates a BIT Test that generates and tests 20 different positions to an accuracy of 0.2%. External excitation is required and outputs must be ON. The DLV Status bits will be set to indicate an accuracy problem. Results are available in the *DLV Test Status Registers* and if enabled, an interrupt will be generated. The testing requires no external programming and can be initiated or terminated at any time.

CAUTION: Outputs must be ON and Excitation supplied during this test and therefore active. Check connected loads for possible interaction.

Wrap LVDT Position (Read)

Wrap-around positions are read from the *Wrap-around Channel Registers*. Each enabled DLV channel is measured and can be read from the corresponding *Wrap-around Channel Register*. The generated result is a 16-bit binary word (or 16-bit 2's complement word) that represents position. The data is available at any time.

Note: In 3/4-wire mode, only channels 1A, 2A need to be read.

DLV Channel Excitation Voltage

Each individual channel input Excitation voltage "VEXC" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format.

For example, if channel 1 input signal voltage is 11.8 VRMS, the output measurement word from the corresponding register would be 1180.

DLV Channel Signal Voltage

Each individual channel output signal voltage "VL-L" is measured and the value reported to a corresponding read register. The output voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. **For example,** if channel 1 output signal voltage is 11.8 VRMS, the output measurement word from the corresponding register would be 1180.

Signal Loss Threshold

Each individual channel output signal voltage "VL-L" is measured and the value reported to a corresponding read register. The signal loss detection circuitry can be tailored to report a signal loss (at SIG Status register Ch.1-4) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format. **For example**, if channel 1 signal loss voltage threshold is to be 7 VRMS, the programmed word to the corresponding register would be 700 (2BCh).

Excitation Loss Threshold

Each individual channel input excitation voltage "VEXC" is measured and the value reported to a corresponding read register. The excitation loss detection circuitry can be tailored to report a excitation loss (at EXC Status Ch.1-4) at a user defined threshold. This threshold can be set to a resolution of 10 mv rms. Program the threshold by writing the value of the voltage threshold in integer decimal format. **For example**, if channel 1 input excitation loss voltage threshold is to be 20 VRMS, the programmed word to the corresponding register would be 2000 (7D0h).

DLV Write Position

Enter the position as a 2's complement number in the corresponding Position Ch. Data Register within the range of -1.00 < Position < (+1.00 – LSB). Factory default: POSITION = 0

Calculate using: register value = POSITION * 32768

Example: For a POSITION = -0.5 -> register value = -0.5 * 32768 = -16384 (0xC000)

Example: For a POSITION = 0.75 -> register value = 0.75 * 32768 = 24576 (0x6000)

The Output voltages in 3/4-wire mode are related to the position by:

Va = Excitation Voltage * TR * [Position/2 + 0.5]

Vb = Excitation Voltage * TR * [1 – (Position/2 + 0.5)]

The Output voltage in 2-wire mode is related to the position by:

V = Excitation Input * TR * Position

DLV Response / Filter Time

(Pending)

Status, Signal Loss

Type: binary word

Range: N/A

Read/Write: R

Initialized Value: 0

Check the corresponding bit for a channel's Signal Status. A Signal input loss to that channel will trigger a bit failure (=1) on a per channel basis. Passing status (=0). Signal Loss is indicated after 2 seconds. Signal input monitoring is disabled during D3 or D0 Test. Any Signal Status failure, transient or intermittent, will latch the Signal Status register. Reading any status bit will unlatch the entire register. Signal Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the *Open Status Interrupt Vector* in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS	X	X	X	X	X	X	X	X	X	X	X	X	X	**Ch3**	**Ch2**	**Ch1**	CHANNEL STATUS BIT

DLV Channel Frequency

Each individual channel excitation frequency is measured and the value reported to a corresponding read register. The input excitation frequency is reported to a resolution of 1 Hz. The output is in integer decimal format. **For example**, if channel 1 input excitation is 400 Hz, the output measurement word from the corresponding register would be 400.

DLV Set Channel Excitation Voltage

Set expected channel input Reference voltage "VREF" to a corresponding register. The input voltage is set with a resolution of 10 mv rms. The setting is in integer decimal format. **For example**, if channel 1 expected input REF voltage is 26.0 VRMS, the set word to the corresponding register would be 2600.

DLV Set Channel Signal Voltage

Set expected channel output signal voltage "VL-L" to a corresponding register. The output voltage is set with a resolution of 10 mv rms. The setting is in integer decimal format. **For example**, if channel 1 Signal (VL-L) voltage is to be 11.8 VRMS, the set word to the corresponding register would be 1180.

DLV Test Enable

Set bit to enable associated Built-In Self Test D2 or D3.

The on-line (D2) Test - Writing "1" to the D2 bit of the *DLV Test Enable Register* initiates status reporting of the automatic background BIT testing that checks the output accuracy of each channel by comparing the measured output position to the commanded position. The status bits will be set to indicate an accuracy (0.2% FS) problem and the results can be read from DLV Status Registers within 2 seconds and if enabled, an interrupt will be generated (See Interrupt Register). Writing a "0" deactivates the status reporting. The testing is totally transparent to the user, requires no external programming, and has no effect on the standard operation of this card. **Note**: Outputs must be ON and Excitation supplied for test to function. Card will write 55h (every 0.1 seconds) to the DLV Test (D2) Verify Register when D2 is enabled. User can periodically clear to 00h and then read the *DLV Test (D2) Verify Register* again, after 0.1 seconds, to verify that BIT Testing is activated. This test continuously sequences between the channels on the card with each output being measured for approximately 180mSec. If the measured position has an error greater the 0.2% FS, a flag will be set in the appropriate register. If the input position is stepped more than 0.2% FS during a test cycle, the test cycle will not generally indicate an error.

In addition, each DLV Excitation input and signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *DLV Signal* and *DLV Excitation Status Registers.*

The off-line (D3) Test - Writing "1" to the D3 bit of the *DLV Test Enable Register* initiates a BIT Test that generates and tests 72 different positions to an accuracy of 0.2% FS. External excitation is required and outputs must be ON. The DLV Status bits will be set to indicate an accuracy problem. Results are available in the *DLV Test Status Registers* and if enabled, an interrupt will be generated (See *Interrupt Register*). Test cycle takes about 30 seconds and the D3 bit changes from "1" to "0" when test is complete. The testing requires no external programming, and can be terminated at any time by writing a "0" to the D3 bit of the *DLV Test Enable Register.*

CAUTION: Outputs must be ON and Excitation must be supplied during this test. Output is therefore active. Check connected loads for possible interaction.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X

Test (D2) Verify

Card will write 55h at *Test (D2) Verification* register when (D2) is enabled, approximately every one second. User can clear to 00h and then read again, after approximately one second, to verify that background bit testing is activated.

DLV Output Mode

The DLV Output Mode register is utilized for selecting either ratio-metric or absolute (fixed) mode voltages. Ratio-metric Mode, when selected, will cause the output signal voltage of the channel to vary with the input Excitation. Fixed Mode, when selected, will set the output to a required magnitude that will not vary with excitation input and set in the DLV Signal Voltage register regardless of the actual input excitation voltage applied. Set register to "0" for Ratio-metric Mode. Set register to "1" for Fixed Mode.

DLV 2-wire or 3/4-Wire Select

Where applicable, write an "01" or "10" (4-Wire = 01; 2-Wire = 10) to each corresponding channel bit pair, representing a channel commanded output format, of the *DLV 2-Wire or 3/4 Wire Select Register.*

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	CH3		CH2 D2		CH1 D0	
DLV 2-Wire or 3/4 –Wire Select	X	X	X	X	X	X	X	X	X	X	D5	D4	D3	D2	D1	D0

DLV Module Power Enable

The *DLV Module Power Enable* register is utilized for module channel output/power control.
To power/enable all channels, use D0 bit. Write D0 to 0x0001 to enable power-on all channels. Write 0x0000 to disable power-on to all channels
To control each channel power output individually, ensure that D0 (all channel control bit) is set to 0. To enable individual channel (output "on") set the corresponding bit to "1". To disable individual channel (output "Off") set the corresponding bit to "0".

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Module Power Enable	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1	X	X	X	All CH

Command word	Module/Channel Power Action
0x0000	ALL channels power OFF
0x0001	ALL channels power ON
0x0010	Channel 1 ON (only)
0x0020	Channel 2 ON (only)
0x0030	Channels 1&2 ON (ch 3 OFF)
0x0040	Channels 3 ON (only)
0x0050	Channels 1&3 ON (ch 2 OFF)
0x0060	Channels 2&3 ON (ch 1 OFF)
0x0070	Channels 1&2&3 ON

DLV Current

(Pending)

Each individual channel current output is measured and the value reported to a corresponding read register. The output current being delivered is reported to a resolution of 0.1 mA rms. The output is in integer decimal format. **For example**, if channel 1 output current delivered is 100 mA rms, the output measurement word from the corresponding register would be 1000.

DLV Active Channels

Allows the *BIT Test Status* register to be updated. For BIT status to work properly on an "active" channel, the DLV channel must have a valid Reference source applied and the DLV channel power set to "ON" (so there is a valid signal being generated). If channels are not being used, it is recommended that the channel BIT status report be turned off (or set "Inactive"). Set the bit, corresponding to each channel to be monitored during BIT testing, in the *Active Channel Register* for the particular DLV channel. "1" = Active; "0" = not used.

IMPORTANT: Omitting this step will produce false alarms because unused channels will set faults.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Active Channels	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

DLV Status, Excitation

This register checks each active channel for the status of the excitation input.

1 = Reference signal loss (LOS: loss of signal)

0 = Reference signal detected at programmed threshold (See Excitation Loss Threshold)

Channels that are inactive are also set to “0”. (Excitation loss is detected after 2 seconds). Excitation monitoring is always enabled. Any DLV excitation status failure, transient or intermittent, will latch the DLV Excitation Status Register. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DLV Status, Excitation	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

DLV Status, Phase Lock Loss

Check the corresponding bit of the *DLV Phase Lock Loss Register* for status of the phase lock between the excitation input and signal output for each active channel. A ”0” means In-Phase, “1” means Phase Lock Loss on active channels. Channels that are inactive are also set to “0”. (Phase Lock loss is detected after 2 seconds). Phase Lock monitoring is always enabled. Any DLV Phase Lock Loss status failure, transient or intermittent, will latch the *DLV Phase Lock Loss Status Register*. Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DLV Status, Phase Lock Loss	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

DLV Set Phase Offset

The phase of each individual channel signal may be offset from the Reference signal. The phase may be adjusted at a resolution of 0.1 deg. (LSB). Program the desired lead or lag in integer as a 2’s complement word format. For example, if channel 1 output signal is to lead the reference signal by 1.6 degrees, program the corresponding channel phase register to 16 (10h). If channel 1 output signal is to lag the reference signal by 1.6 degrees, program the corresponding channel phase register to -16 (FFF0h). Phase shift range is -90 <= x <= 90.

DLV Current Threshold

(Pending)

OSC (Onboard) Excitation Set Frequency

Type: 16-bit unsigned integer

Range: 47 to 10,000 Hz

Read/Write: R/W

Initialized Value: N/A

Program Reference Frequency, where LSB is 0.01 Hz. **For example**: To program 400 Hz, 400 x 100= 40,000, which equals 0x9C40. In this example, 0x0000 would be programmed in the *Reference Frequency High* register, and 0x9C40 would be programmed in the *Reference Frequency Low* register. To program 10,000 Hz, 10,000 x 100= 1,000,000, which equals 0xF4240. In this example, 0x000F would be programmed in the *Reference Frequency High* register, and 0x4240 would be programmed in the *Reference Frequency Low* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	327.68	163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	0.01	approximate value
REF FREQUENCY LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	0	0	0	0	0	0	5242.88	2621.44	1310.72	655.36	approximate value
REF FREQUENCY HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

OSC (Onboard) Excitation Set Voltage

Type: 16-bit unsigned integer

Range: 2.0 to 28.0 VRMS, or 115 VRMS

Read/Write: R/W

Initialized Value: N/A

Program Reference Voltage, where LSB is 0.01 VRMS. **For example**: To program 26.1 VRMS, 26.1 x 100= 2610, which equals 0xA32. In this example, 0x0000 would be programmed in the *Reference Voltage High* register, and 0x0xA32 would be programmed in the *Reference Voltage Low* register. To program 115 VRMS, 115 x 100= 11,500, which equals 0x2CEC. In this example, 0x0000 would be programmed in the *Reference Voltage High* register, and 0x2CEC would be programmed in the *Reference Voltage Low* register. **Note**: *Reference Voltage High* register always remains at 0x0000.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	81.92	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	0.01	approximate value
REF VOLTAGE LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (V)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	approximate value
REF VOLTAGE HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (V)

DLV Status, BIT Test

Check the corresponding bit of the *DLV BIT Test Status Register* for status of BIT (Test-Accuracy) Testing for each active channel. A ”1” means Accuracy Failed; “0” means Accuracy OK. Accuracy defaulted to 0.2% FS output as compared to commanded position. Channels that are inactive are also set to “0”. The status bits will be set to indicate an accuracy (0.2% FS) problem and the results can be read from *DLV Status Registers* within 2 seconds and if enabled, an interrupt will be generated (See *Interrupt Register)*.

Note: D/L channels, by default, are set for monitoring the channel background BIT (Built-In-Test) status reporting; “ON” or “ACTIVE”. The front panel BIT LED illuminates (Red) if any channel reports a BIT fault. For BIT status to work properly on an “active” channel, the D/L channel must have a valid Reference source applied and the D/L channel power set to “ON” (so there is a valid signal being generated). If channels are not being used, it is recommended that the channel BIT status report be turned off (or set INACTIVE). However, it should be noted that the channel BIT status register latches the contents of a failure until read. Simply setting the channel “INACTIVE” will not clear the BIT status register or extinguish the front panel BIT fault LED if a fault was previously detected.

This test continuously sequences between the channels on the card with each output being measured for approximately 180mSec. If the measured position has an error greater the 0.2% FS, a flag will be set in the appropriate register. If the input position is stepped more then 0.2% FS during a test cycle, the test cycle will not generally indicate an error. Any DLV test status failure, transient or intermittent, will latch the *DLV Test Status Register.* Reading will unlatch register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DLV Status, BIT Test	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

Excitation Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a excitation input loss (DLV Status, Excitation) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Excitation Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Excitation Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

Signal Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal input loss (DLV Status, Signal Loss) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Signal Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Signal Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

BIT Test Fail Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a BIT Test Failure (DLV Status, BIT Test) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the BIT Test Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Test Fail Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

Phase Lock Loss Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a Phase Lock Loss (DLV Status, Phase Lock Loss) will trigger an interrupt. Default is “0” to disable interrupt on all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Phase Lock Loss Interrupt Vector.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Phase Lock Loss Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	CH3	CH2	CH1

Interrupt Vector

Write 16-bit integer (0-255). Used for failure reports.

The *Interrupt Vector Registers* store the vectors for the specific interrupts generated by the module. If the same vector is loaded into each register, the same interrupt routine will be invoked by all interrupts. If unique vectors are loaded into the registers, a different Interrupt Service Routine (ISR) can be invoked by each interrupt.

- The Signal Loss interrupt vector will be serviced when the Signal Loss status is set and the interrupt has been enabled.
- The Reference Loss interrupt vector will be serviced when the Reference Loss status is set and the interrupt has been enabled.
- The BIT interrupt vector will be serviced when the Bit (failure) status is set and the interrupt has been enabled.
- The Lock Loss interrupt vector will be serviced when the Lock Loss status is set and the interrupt has been enabled.

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding "latching" – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are "latching"; as defined, any noted transitional change on any channel will "latch" the entire Status Register.
- Once latched, there will be no further state change "sensed" by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will "unlatch" that particular status register (doesn't necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will "latch" the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read "until cleared".

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern ("loop to clear") - this would also be similar to an Interrupt Service Routine (ISR) "loop to clear" function.

    Ex: Running the 'loop to clear' on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are "cleared" and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

  The ISR is typically a software (SW) handling branch (part of host application software) structured to "loop to read and clear" the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should "read" the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were "latched" – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively "re-arm" for the next transition to occur.

  Ex: The ISR should have the 'loop to clear' – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also "latch" the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

3 CH DLV (5*) (VME) MODULE MEMORY MAP

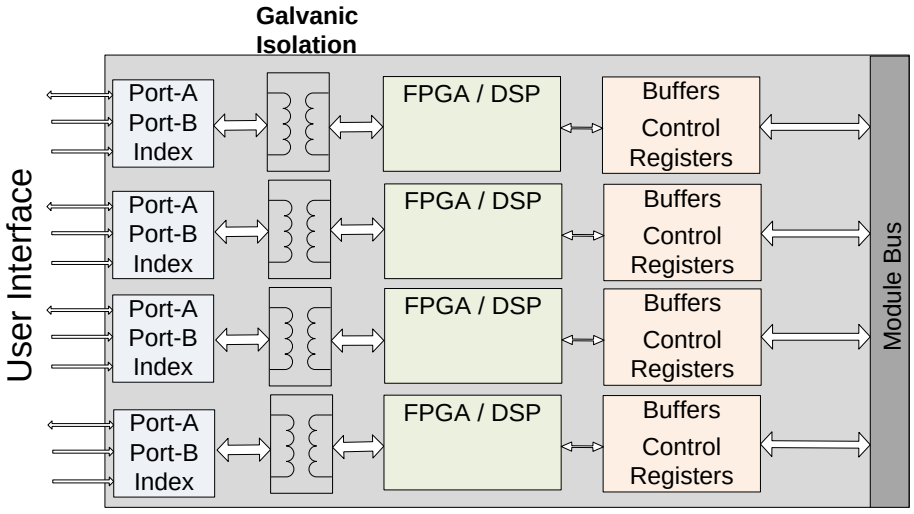
000	Wrap LVDT Position Lo	CH1	R	0A0	DLV Set Excitation Volt Lo	CH1	W/R	180	DLV Write Position Lo	CH1	W/R
002	Wrap LVDT Position Hi	CH1	R	0A2	DLV Set Excitation Volt Hi	CH1	W/R	182	DLV Write Position Hi	CH1	W/R
004	Wrap LVDT Position Lo	CH2	R	0A4	DLV Set Excitation Volt Lo	CH2	W/R	184	DLV Write Position Lo	CH2	W/R
006	Wrap LVDT Position Hi	CH2	R	0A6	DLV Set Excitation Volt Hi	CH2	W/R	186	DLV Write Position Hi	CH2	W/R
008	Wrap LVDT Position Lo	CH3	R	0A8	DLV Set Excitation Volt Lo	CH3	W/R	188	DLV Write Position Lo	CH3	W/R
00A	Wrap LVDT Position Hi	CH3	R	0AA	DLV Set Excitation Volt Hi	CH3	W/R	18A	DLV Write Position Hi	CH3	W/R
								198	OSC Set Voltage Lo		W/R
032	Wrap Excitation Voltage	CH1	R	0B0	DLV Set Signal Volt Lo	CH1	W/R	19A	OSC Set Voltage Hi		W/R
034	Wrap Excitation Voltage	CH2	R	0B2	DLV Set Signal Volt Hi	CH1	W/R	19C	OSC Set Frequency Lo		W/R
036	Wrap Excitation Voltage	CH3	R	0B4	DLV Set Signal Volt Lo	CH2	W/R	19E	OSC Set Frequency HI		W/R
				0B6	DLV Set Signal Volt Hi	CH2	W/R				
038	Wrap S/D Signal Voltage	CH1	R	0B8	DLV Set Signal Volt Lo	CH3	W/R	380	DLV Status, BIT Test		R
03A	Wrap S/D Signal Voltage	CH2	R	0BA	DLV Set Signal Volt Hi	CH3	W/R	382	DLV Reference Loss Interrupt Enable		W/R
03C	Wrap S/D Signal Voltage	CH3	R					384	DLV Signal Loss Interrupt Enable		W/R
				0C0	DLV Test Enable		W/R	386	DLV BIT FAIL Interrupt Enable		W/R
040	Wrap Signal Loss Threshold	CH1	W/R	0C4	D2 Test Verify		W/R	388	DLV Phase Lock Loss Interrupt Enable		W/R
042	Wrap Signal Loss Threshold	CH2	W/R	0C6	DLV Output Mode		W/R				
044	Wrap Signal Loss Threshold	CH3	W/R	0CC	DLV 2-W/4-W Select		W/R	3E0	Vector Interrupt BIT Fail		W/R
								3E2	Vector Interrupt REF Loss		W/R
046	Wrap Excitation Loss Threshold	CH1	W/R	0E0	DLV Module Power Enable		W/R	3E4	Vector Interrupt Signal Loss		W/R
048	Wrap Excitation Loss Threshold	CH2	W/R	0E4	DLV Active Channel Select		W/R	3E6	Vector Interrupt Phase Lock Loss		W/R
04A	Wrap Excitation Loss Threshold	CH3	W/R								
				0E6	DLV Excitation Status		R	3B4	Module Design Version		R
04C	Channel 1 Frequency		R	0E8	DLV Phase Lock Status		R	3B6	Module Design Revision		R
04E	Channel 2 Frequency		R	0F4	DLV Set Phase Offset	CH1	W/R	3B8	Module DSP Revision		R
050	Channel 3 Frequency		R	0F6	DLV Set Phase Offset	CH2	W/R	3BA	Module FPGA Revision		R
058	Status, Signal Loss		R	0F8	DLV Set Phase Offset	CH3	W/R	3BC	Module ID Revision		R

SSI / ENCODER / QUADRATURE COUNTER (MODULE E7)

Principles of Operation

Each module incorporates four (4) independent isolated programmable encoder/counter I/O channels. These encoder/counter channels can interface directly to independent industrial encoders without any concern about groundings. Each channel is programmable as an SSI interface controller, an SSI "Listen Only" mode receiver, an incremental encoder reader or a general purpose counter.

- When programmed in the SSI controller mode, the channel will output a clock to the encoder and will receive the encoder positional data signal. The SSI controller has a programmable clock rate.
- When programmed in the SSI "Listen Only" mode, the channel will accept both the clock and positional data signal as inputs. The data word can be programmed in binary or gray codes with parity.



SSI & Quadrature Encoder Module Block Diagram

- When programmed as a Quadrature encoder counter, the channel can accept an index pulse in conjunction with the A and B signal inputs.
- When programmed as an incremental encoder, sub-programming options include pre-loadable up/down counters and 1x, 2x or 4x input format.
- When programmed as a general purpose counter, the channels are pre-loadable and can be controlled as an UP or DOWN counter which can be fed via a programmable internal clock source or an external signal trigger.

The module provides an automatic background Built-In-Test (BIT) for each channel. BIT is always enabled and continually checks that each channel is functional. This capability is accomplished by Test Circuits that are dedicated for each of the channels. The Test Circuits are continuously monitoring each channel for comparison, voltage and current limit comparisons. Depending upon configuration, the Input data or Output logic of the operational channel and Test Circuit must agree or a fault is indicated with the results available in the associated status registers. Additional testing is provided to check for over-current condition. Four threshold levels (Max High, Upper, Lower, Min Low) are programmed to user defined high and low voltage levels. All four threshold levels must be set for each Input or Output channel to validate BIT testing. Interrupts can also be generated on a change of state or transition.

Channel Inputs

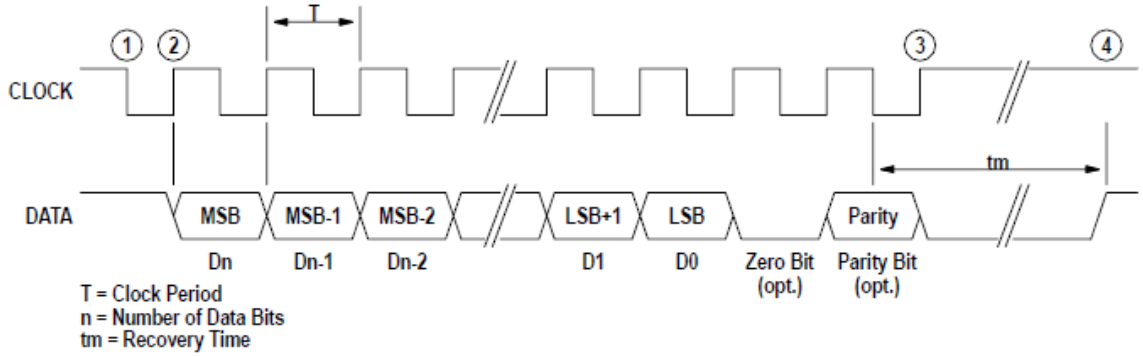
Channel Mode	Channel A	Channel B	Index
SSI (Standard)	Clock (Out)	Data (In)	N/u
SS (Listen Only)	Clock (In)	Data (In)	N/u
Timer Mode	N/u	N/u	Control (In)
Direction Count	Counter (In)	Counter Direction (In)	Control (In)
Up/Down Count	Count (Up)	Count (Down)	Control (In)
Quadrature	Input A	Input B	

Note: In SSI standard mode, the hardware permits any channel (A, B, or INDEX) to source the SSI clock. All RS485 transceivers are supplied the internally generated SSI clock signal. However each transceiver has a unique driver enable control bit, and only one (de) enable bit should be set at a time. If Channel B is assigned for SSI Data input (as indicated in the above table), then Channel A or the Index could be used to supply the SSI clock.

SSI Mode

Description

The Synchronous Serial Interface (SSI) is based on two differential signal lines, CLOCK and DATA. The CLOCK line is an input, the DATA line is an output of the absolute encoder.



SSI Timing Example

When not transmitting, the clock and data lines are high. To read out the positional data of an absolute encoder, the controller transmits a pulse train on the CLOCK line. The first falling edge of CLOCK latches the positional data of the absolute encoder. At the first rising edge of CLOCK “the absolute encoder presents the most significant bit on the DATA line. On each subsequent rising edge in the CLOCK pulse train the next bit in order is transmitted to the controller.

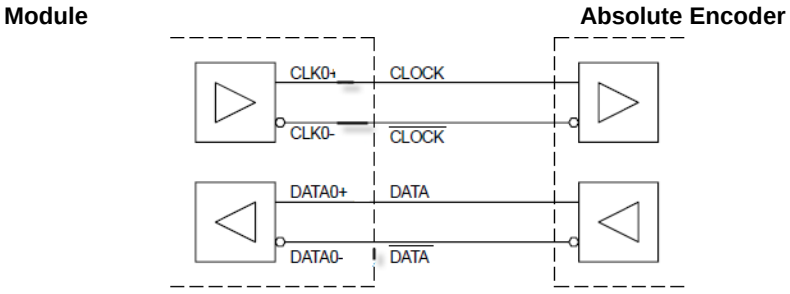
In addition to the data bits the absolute encoder can transmit a parity bit for error detection. As an option a zero bit can be placed between the data and the parity bit. After all bits are transmitted #, the absolute encoder holds the data line low for 10-30µs (recovery time tm). After that the absolute encoder is ready for a new transmission $. A new transmission must not be started before $.

The maximum achievable baud rate depends on the cable length. Cables are assumed to be twisted pair and screened.

Cable Length (m)	Baud Rate (kHz)
< 50	< 400
< 100	< 300
< 200	< 200
< 400	<100

Standard SSI Interface Controller Mode

In this mode A Module channel operates as a standard SSI interface controller. The SSI clock is an output and data signal is an input to the module:



This mode is enabled when the Interface Control in the Global Control Register is set to “01” and the MODE bit in the Control Register is set to (0).

Register	Symbol	Setting
Global Control Register	ICx	“01”
Control register 0	MODE (bit 8)	“0”

SSI Standard Mode Selection

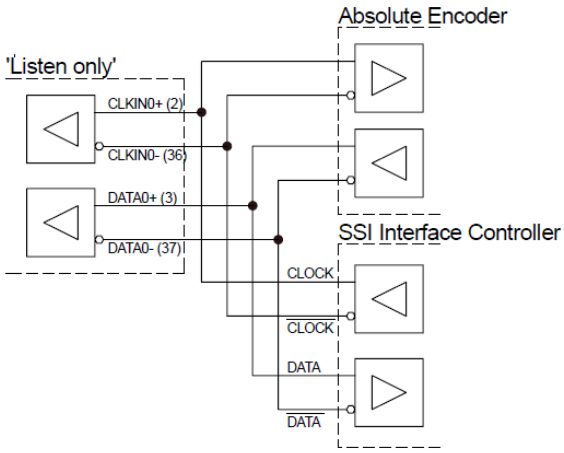
In the Control Register the SSI interface must be set up, conforming to the settings required of the connected absolute encoder:

Register	Symbol	Setting
Control Register 0	BC	BC Number of Data Bits
	ZB	Additional Zero Bit
	PAR	Parity Detection
	CR	Clock Rate
	Dwell	Number of Idled Clock Cycles Between SSI Read Cycles

A data transfer is initiated by a write to the data register. The SSI interface controller then generates a clock burst, on which the absolute encoder returns its positional data. The SSI Controller receives this data, processes it (parity check, gray- to binary code conversion) and indicates the end of the data transfer with the de-assertion of the **busy** bit. If enabled, an interrupt is asserted and the positional data can then be read in the Data Register. In this mode the read error status bit is always read zero (0).

Wiring Example: Channel 0, SSI Interface Controller Mode. This mode is enabled when the Interface Control in the Global Control Register is set to (01) and the MODE bit in the Control Register is set to (0).

Listen Only Mode



This mode is enabled when the Interface Control in the Global Control Register is set to (01) and the MODE bit in the Control Register is set to 1.

Register	Symbol	Setting
Global Control Register	ICx	01
Control Register 0	MODE	1

SSI Listen Only Mode Selection

In the Control Register the SSI interface must be set up, conforming to the settings required of the observed SSI interface:

Register	Symbol	Setting
Control Register X	BC	BC Number of Data Bits
	ZB	Additional Zero Bit
	PAR	Parity Detection
	CR	-
	Dwell	-

The clock rate setting in the Control Register is “don’t care”; the clock rate of the observed SSI interface will be detected automatically. After the Control Register is set up, the channel listens (indicated by Busy = 1).

A data transfer is initiated by the observed SSI interface. The positional data will be received and processed (parity check, gray- to binary code conversion) and the end of the data transfer is indicated with the de-assertion of the Busy bit. If enabled, an interrupt is asserted and the positional data can be read in the Data Register. Reading the Data Register will set the Busy bit to 1 and the channel is listening again.

Note: In this mode the clock rate setting in the Control Register is ignored; the Clock Rate will be detected automatically. Writes to the Data Register are also ignored for channels in this mode.

In case of a partial transmission a read error will be issued in the Status Register. To detect read errors, the width of the first SSI clock pulse is measured to detect the clock rate. This clock rate is multiplied by 4 and used as the initial value for a watchdog timer. Every new received bit resets the watchdog timer, until either the programmed data word length is reached (successful read) or a timeout occurs (read error).

In case of a timeout the Read Error bit is set to (1). Depending on the BREAK setting in the Control Register the channel ignores a read error and continues listening or it stops to listen. Reasons for a read error are:

- The number of data bits set in the control register does not match the actual size of the received transmission.
- Only a partial transmission was monitored (this could happen when the mode is switched and a transmission is in progress on the observed SSI interface).
- In the case that a SSI communication is in progress when the mode is switched to 'Listen only' a read error will be issued for the first reading.

Parity

Parity is the sum of data bits in the SSI word, with the bits high (1).

Sum of Input Bits	Even Parity (Par_oe = 0)	Odd Parity (Par_oe = 1)
Even Number of 1's	Parity Bit S/b = 1	Parity Bit S/b = 0
Odd Number of 1's	Parity Bit S/b = 0	Parity Bit S/b = 1

	Standard SSI Interface Mode	'Listen only' Mode
Control Register	Control Register SSI Bits Fully Used. Bit 14 (MODE) is set to '0'	Clock Rate Setting in Control Register is 'Don't Care'. Bit 14 (MODE) is Set to '1'
Status Register	**Status Register** Busy bit = '1' during transmission	Busy bit = '1' While Channel is Listening
Read Error Bit	Read Error Bit is Always .0.	Read Error Bit is Set to .1. on a Erroneous Transmission
Connections	Connect External SSI Data Outputs to Module 'DATA' Inputs. Connect External SSI Clock Inputs to Module PMC117 'CLK OUT' Outputs.	Connect External SSI Data to Module 'DATA' Inputs. Connect External SSI Clock to Module 'CLK IN' Inputs.
Data Transfer Start	Data Transfer is Initiated by a Write to the Data Register or a Multiple Channel Read	Data Transfer is Initiated by External SSI Interface Controller

Register access definitions: r=read, w=write, r/c=clear (0) on read action; n/u=not used

Control Register 0

During a transmission the parity error bit is not valid. The parity error status is updated only if the parity enable bit of the corresponding channel is set to “1”. Otherwise the parity status is read as “0”.

Bit	Symbol	Description	Access	Reset Value
[15:11]	-	N/u	r	0
[10]	-	EX_NML 0 = Normal Clock Mode. SSI data from the encoder transitions on the rising edge of the SSI_CLK and is sampled by this module on the falling edge of the SSI_CLK. 1 = Exchanged SSI data from the encoder transitions on the falling edge of the SSI_CLK and this module clocks the data in on the rising edge of the clock.	r/w	
[9]	Break	Break on Read Error (Listen Only) 1 = The Channel Stops to Listen On Read Errors 0 = Read Errors Are Ignored and the Channel Resumes to Listen	r/w	
[8]	Mode	1 = SSI Listen only 0 = Standard Mode	r/w	0
[7]	ZB	1 = Zero Bit Mode 0 = No Zero Bit	r/w	0
[6]	Par_Oe	1 = Odd Parity 0 = Even Parity	r/w	0
[5]	Par_En	Encoder with Parity - If Encoder Provides a Parity Bit: 1 = Detect Parity Errors 0 = Do Not Detect Parity Errors / No Parity Bit	r/w	0
[4:0]	BC[4:0]	Number of Data Bits Bits are used to program the number of bits of the serial Valid range ^1d to ^d31.	r/w	0

Control Register 1

Bit	Symbol	Description	Access	Reset Value
[15:11]	-	N/u	r	0
[10:6]	Dwell [4:0]	Number of bit cycle that the clock idles for after a SSI read.	r/w	0
[5:0]	CR[5:0]	Clock Rate for encoder serial clock speed The clock can be programmed in steps of 1µs in the range of 1 to 32. A value of 0 for the clock rate will stop the operation of the SSI interface. The .Listen only. Mode will ignore the Clock Rate setting; in this mode the Clock Rate will be detected automatically.		

SSI Received Data High

Bit	Symbol	Description	Access	Reset Value
[15:0]	-	Received SSI data register H [32:16]	r	0

SSI Received Data Low

Bit	Symbol	Description	Access	Reset Value
[15:0]	-	Received SSI Data Register H [15:0]	r	0

SSI Received ZB, Parity

Bit	Symbol	Description	Access	Reset Value
[15:2]	-	N/u	r	0
[1]		Received Zero Bit (Should be Zero)	r	0
[0]		Received Parity Bit	r	0

SSI Status

Bit	Symbol	Description	Access	Reset Value
[15:6]	-	N/u	r	0
[5]	EXTRA	EXTRA Valid Only in 'Listen Only' Mode. 1= Indicates More Falling Edges of the SSI Clock Than Programmed for the (BC) Value	r/c	0
[4]	WD_E	Watch Dog Error Valid Only in 'Listen Only' Mode. 1 = SSI Qatch Dog Timer Error. This bit is set if the watch dog timer times out. (SSI_CLK) stalls before the (BC) number of bits are received	r/c	0
[3]	Busy	Busy Bit In Standard SSI Interface Controller Mode Busy Bit = '1' Indicates a Transmission in Progress. (Busy bit sourced from the baud rate generator) In 'Listen Only' Mode Busy Bit is set '1' when a transmission is in progress (Busy bit is sourced from the SSI watch dog timer)	r	0
[2]	P-Error	Encoder With Parity - If Encoder Provides a Parity Bit: 1 = Detect Parity Errors 0 = Do Not Detect Parity Errors / No Parity Bit	r/c	0
[1]	Ov	Overflow	r/c	0
[0]	N-Data	New Data	r/c	

Counter Modes

Counter Match Register

Every time the counter matches the counter compare

Register value, bit 18 (MAT) of the status register is set to ’1’ and, if enabled, an interrupt is generated.

Match Data High [31:16]

Bit	Symbol	Description	Access	Reset Value
[15:0]	-	Match Data [31..16]	r/w	0

Match Data Low [15:0]

Bit	Symbol	Description	Access	Reset Value
[15:0]	-	Match Data [15..0]	r/w	0

Counter Preload Register

The value of this register can be loaded into the counter by:

- Setting bit 1 (LCNT) of the Counter Command Register low.
- An impulse on the I-input when the ’Load on I’-mode is active.
- Automatically in the ’Divide-by-N’-mode every time the counter creates a borrow or a carry.
- Reference modes.

Counter Preload High [31:16]

Bit	Symbol	Description	Access	Reset Value
[15:0]	-	Counter Preload Data [31..16]	r/w	0

Counter Preload Low [15:0]

Bit	Symbol	Description	Access	Reset Value
[15:0]	-	Counter Preload Data [15..0]	r/w	0

Counter Latch Register

The counter latch register is used to store the current value of the counter when a Latch on I event occurs. The status of the counter latch register is available in the Counter Status register (DRL, and OVFL bits). This register is reset on power up or by setting the ICx[1] bit to zero, in the global control register (low). Note: setting ICx[1] bit to zero will also reset the counter, and the counter status register (added DOM 3/14 and later).

Counter Latch High [31:16]

Bit	Symbol	Description	Access	Reset Value
[15:0]	-	Counter Latch Data [31..16]	r	0

Counter Latch Low [15:0]

Bit	Symbol	Description	Access	Reset Value
[15:0]	-	Counter Latch Data [15..0]	r	0

Counter Control Register

Bit	Symbol	Description	Access	Reset Value
[15:13]	-	N/u	r/w	0
[12:10]	ICM[2:0]	Index Control Mode	r/w	0
[9:7]	POL[2:0]	A,B,I Polarity	r/w	0
[6:5]	SCM[1:0]	Special Count Mode	r/w	0
[4:3]	CLKDIV[1:0]	Internal Clock Prescaler	r/w	0
[2:0]	CIM[2:0]	Counter Input Mode	r/w	0

Index Control Modes (ICM)

The Index Control Mode determines how events on the I-input are interpreted. With the exception of the 'Gate on I' mode, all modes react on a level change on the I-input. Due to the digital input filtering, a change in the input level is only detected, when the input line is stable for at least 100ns.

ICM[2:0]		POL = 0	POL = 1
000	Ignore I-Input	Rising Edge	Falling Edge
001	Load On I	Rising Edge	Falling Edge
010	Latch On I	Level High	Level Low
011	Gate On I	Rising Edge	Falling Edge
100	Reset On I	Rising Edge	Falling Edge
101	Ignore I-Input	-	-
110	Ignore I-Input	-	-
111	Ignore I-Input	-	-

An interrupt can be generated on a control mode event. This is only available for the Load-, Latch-, Gate- and Reset on I modes.

Index Control Mode	Interrupt Generation
No Control Mode	No Interrupt
Load, Latch or Reset Modes	Control Mode Event
Gate Mode	Gate Closed

No I-Control

In this mode the I-input is ignored.

Load on I

An event on the I-input loads the counter with the content of the Counter Preload Register. If the 'Single Cycle' mode is active, the event on the I-input will start the counter. The counter can also be preloaded by writing '1' to the 'Load Counter' (LCNT) bit in the Counter Command Register. This control mode can be used to establish a known reference position in a mechanical system.

Latch on I

An event on the I-input loads and locks the Counter Latch Register with the counter value. This register remains latched until a new event I input event reloads this register. . When a 'Latch on I' event occurs while the Data Register Lock DRL bit is still active, the data in the Counter Latch register will be retained and the Data Register Lock Overflow (OVFL) will be set to indicate that last latch on I counter value was lost. This control mode can be used to capture a position in a mechanical system.

Gate on I

The signal level on the I-input enables or disables counting. Remember that in this mode the I-input is level sensitive.

I-Input	Counter
0	Disabled
1	Enabled

In this mode an interrupt is generated (if enabled) when the gate is being closed (I-Input transition from '1' to '0').

When a signal with constant frequency is connected to the A- and B-inputs, this control mode can be used for impulse width measurements.

Reset on I

An event on the I-input resets (clears) the counter. If the 'Single Cycle' mode is active, the event on the I-input starts the counter. The counter can also be reset by writing '1' to the 'Reset Counter' (RCNT) bit in the Counter Command Register. This control mode can be used to establish a known home or reference position in a mechanical system.

POL[2:0]

POL[2:0]	Input	POL = 0	POL = 1
POL[2]	A	Active High	Active Low
POL[1]	B	Rising Edge	Falling Edge
POL[0]	INDEX	Level High	Level Low

Special Count Mode

SCM[1:0]

SCM[1:0]	Mode
00	No special mode
01	Divide-by-N
10	Single Cycle

Special Count Modes

In normal operation, the counter is a cycling counter. Two additional special count modes are available. The Count Modes are available for every Input Mode.

Divide-by-N

The counter is enabled in the Control Register and will run until it is disabled. The counter is loaded with the content of the preload register every time the counters creates a borrow or a carry.

Single Cycle

The counter is enabled in the Control Register and will start on following events:

- A manual preload or reset in the Counter Command Register
- A manual counter preload in the Global Control Register
- A control mode event in .Load on I. or .Reset on I. mode

The counter will stop when it creates a borrow or a carry.

Internal Clock Prescaler

CLKDIV

CLKDIV[1:0]	Divide by	Clock Frequency
00	1	50 MHz
01	2	25 MHz
10	4	12.5 MHz
11	8	6.25 MHz

Counter Input Mode (CIM)

CIM[2:0]	Input Mode	Counter Input Source	A Input	B Input
000	Counter Disabled		-	-
001	Timer Mode Up	Internal Clock Prescaler	-	-
010	Timer Mode Down	Internal Clock Prescaler	-	-
011	Direction Count	Input A & Input B	Count	Count Direction Up/Down
100	Up/Down Count	Input A & Input B	Count Up	Count Down
101	Quadrature Count 1x	Input A & Input B	Quadrature A	Quadrature B
110	Quadrature Count 2x	Input A & Input B	Quadrature A	Quadrature B
111	Quadrature Count 4x	Input A & Input B	Quadrature A	Quadrature B

Counter Status Register

Bit	Symbol	Description	Access	Reset Value
[15:8]	-	N/u	r	0
[7]	SGL	Single Cycle Active In Single Cycle counting mode this bit is set to '1' when the counter is active. It is reset to '0', when the counter has counted down to zero	r	0
[6]	OVFL	Counter Latch Overflow When a Latch Mode event occurs while the Data Register Lock (DRL) is still active, the data in the Counter Latch Register will be retained and this bit will be set to indicate that data was lost This bit must be reset by writing a '1' to this bit.	r/w	0
[5]	DRL	Data Register Latch This bit is set to '1', when the Counter Latch Register is locked due to a 'Latch on I' or a Multiple Channel Read. This bit is cleared after a read access to the Counter Latch (High or Low) Register or by writing a '1' to this bit.	r/w	0
[4]	DIR	Count Direction This bit indicates the counting direction of the counter. '1' indicates up, '0' indicates down. In the 'Up/Down Count' mode this bit indicates the direction at the last count. In the 'Direction Count' mode this bit corresponds to the I-input	r	0
[3]	SGN	Sign The Sign bit is set to '1' when the counter overflows, and is set to '0' when the counter underflows. After reset or power-up this bit should be considered as "don't care" until the first Carry or Borrow occurred.	r	0
[2]	MAT	Match This bit is set to '1' when the counter value Matches the value of the Counter Compare Register. This bit must be reset by writing a '1' to this bit.	r/w	0
[1]	CRY	Carry This bit is set to '1' when the counter changes from 0xFFFFFFFF to 0x00000000. This bit must be reset by writing a '1' to this bit.	r/w	0
[0]	BOR	Borrow This bit is set to '1' when the counter changes from 0x00000000 to 0xFFFFFFFF. This bit must be reset by writing a '1' to this bit.	r/w	0

Timer Mode

In Timer mode the counter uses an internal clock pre-scaler as input

Direction Count

The counter acts as up/down counter. Counting pulses are generated when a transition from low to high of the A-input is detected. The B-input determines the count direction.

B Input	Count Direction
0	Down
1	Up

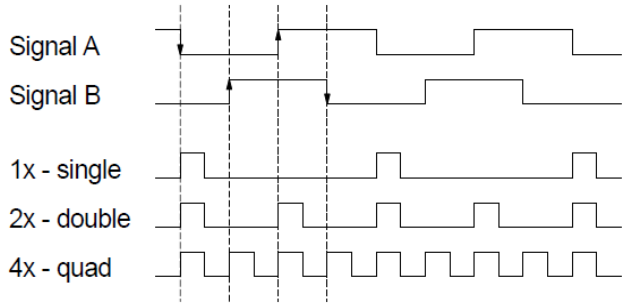
Up/Down Count

The counter acts as up-/down counter. Counting pulses are generated when a transition from low to high of either the A- or the B-input is detected. The A-input counts up, the B-input counts down. Simultaneous transitions on the A- and B-input do not generate a counting pulse.

Quadrature Mode

The counter acts as quadrature counter. A-input is quadrature input A, B-input is quadrature input B.

The quadrature inputs can be interpreted as 1x, 2x or 4x counting. 1x lets the counter count once for each full cycle of the quadrature inputs, 2x lets the counter count once for each half cycle of the quadrature inputs and 4x lets the counter count once for each quarter cycle of the quadrature inputs. The count direction (increase or decrease) is determined by the relative phase of the A- and B-signals.



Counter Command Register

Bit	Symbol	Description	Access	Reset Value
[15:2]	-	N/u	r	0
[1]	LCNT	Load Counter Write '1' to load the counter with the value of the Counter Preload Register.	w	0
[0]	RCNT	Reset Counter Write '1' to reset the counter.	w	0

Counter Command register bit, LCNT, and RCNT. Writing a one to these register bits either reset, or preloads the counter. Please note: use of these bits is exclusive.

Interval Timer

Bit	Symbol	Description	Access	Reset Value
[15:0]	ITPRE	Interval Timer Preload Register	r/w	0

Interval Timer Control

Bit	Symbol	Description	Access	Reset Value
[15:3]	-	N/c	r	0
[2:1]	ITDIV	Pre-Scale Value 00 25 MHz 40 ns 01 12.5 MHz 80 ns 10 6.25 MHz 160 ns 11 3.125 320 ns	r/w	00
[0]	ITEN	Interval Timer Enable '0' Disables the Interval Timer '1' Enables the Interval Timer	r/w	0

The interval timer is a 16-bit pre-loadable counter with a programmable clock rate. On activation the counter loads from the Interval Timer Preload Register and starts counting down. When the counter reaches zero, it generates an interrupt (if enabled), then is automatically preloaded again and continues counting. With the 16-bit preload register and the programmable clock interval, interval times up to 65ms are possible. Calculate the interval times using the following formula:

Interval Time = Value of Interval Timer Preload Register * Clock period

Interval Timer Clock Periods

The interval timer can be used as a reference timer in closed loop applications or as a trigger for a multiple channel read.

Global Control Registers

Global Control Register High

Bit	Symbol	Description	Access	Reset Value
[15]	-	N/u	r	0
[14]	MCRTR	**Multiple Channel Read Trigger** By writing 1 to this bit, a Multiple Channel Read is triggered.	w	0
[13]	MCRST	**Multiple Channel Read Status** This bit indicates pending Multiple Channel Read data When a SSI channel is enabled for Multiple Channel Read, it takes time for the conversion to complete. This bit indicates that the conversions of all enabled channels are complete. 1 = Multiple Channel Read Data is valid (for all enabled channels) 0 = The Data Registers of all enabled channels have been read out. To reset a multiple channel read sequence, write 1 to this bit[13]	r/w	0
[12]	ITRG	**Interval Timer as trigger for Multiple Channel Read** 1: Enable Interval Timer as trigger for multiple channel read 0: Disable Interval Timer as trigger for multiple channel read	r/w	0
[11:10]	-	N/u	r/w	0
[9]	MCHRD[4]	**Enable Multiple Channel Read Channel [4]** 1 = Enables Multi Channel Read 0 = Disables Multi Channel Read	r/w	0
[8]	MCHRD[3]	**Enable Multiple Channel Read Channel [3]**	r/w	0
[7]	MCHRD[2]	**Enable Multiple Channel Read Channel [2]**	r/w	0
[6]	MCHRD[1]	**Enable Multiple Channel Read Channel [1]**	r/w	0
[5:4]	-	N/u		
[3]	Prl[4]	**Manual Counter Preload Channel [4]** Writing a 1 issues a preload of the corresponding counter with the value of the Counter Preload Register. This preload method is only possible for channels in a .None Reference Mode. Before using this preload method, the corresponding Counter Preload Registers must be loaded with valid data	w	
[2]	Prl[3]	**Manual Counter Preload Channel [3]**	w	
[1]	Prl[2]	**Manual Counter Preload Channel [2]**	w	
[0]	Prl[1]	**Manual Counter Preload Channel [1]**	w	

Multiple Channel Read

Multi-channel read, is used to simultaneously latch the value of two or more counter channels, or read simultaneously the position of two or more SSI encoder channels. The Multiple Channel Read function is enabled through the Global Control Register. A Multiple Channel Read is triggered by writing '1' to the MCRTR-bit, or alternatively by setting the ITRG bit and enabling the interval timer. When setting the ITRG bit, a Multi–Channel read cycle is triggered each time the interval timer reaches terminal count. To become part of a Multi-channel read group, the MCHRD bit(s) needs to be set '1' for the associated channel.

For Counter modes when using the Multiple Channel Read function, the Multi–Channel read latches the value of the counters that are programmed to be part for the Multi-channel read group. The latched value of counter is available immediately after the trigger occurs.

For SSI modes a Multiple Channel Read trigger starts a conversion for the SSI channels that are part of the group. SSI channels need time for the conversion to complete. To indicate that the data for all the SSI channels that are part of the group is available, the MCRST bit in the Global Control Register is set to '1'. The MCRST remains set, until cleared by writing the MCRST bit with a '1'.

The Multiple Channel Read MCRST bit may also be programmed to generate an interrupt.

Multi-channel read Data Availability

SSI Mode
MCRST = '0' SSI conversion is in process, or hasn't been triggered. New data is not available. MCRST is cleared by writing a '1', to MCRST bit
MCRST = '1' SSI conversion for channels that are part of the group is complete

Example: Channels 1-3 are configured for SSI mode, channels 4-6 are configured for counter mode. Channels 1, 4 and 6 are enabled for Multiple Channel Read. A write to the MCRTR bit starts the Multiple Channel Read. Channel 1 starts a conversion and the counter value of channels 4 and 6 are latched. The latched counter value for the enabled counter channels is instantly available and can be read at once. The SSI data is not available until MCRST is set to '1'. The MCRST status is reset to '0' by writing a "1" to MCRST bit'.

Alternatively an interrupt can be set up for the SSI channel that takes the longest time to complete a conversion. If only counter channels use the multi-channel function, interrupts are not necessary because the counter data is instantly available on MCRTR trigger, or on the Interval Timer terminal count, which has an interrupt.

Global Control Register Low

Bit	Symbol	Description	Access	Reset Value
[15:13]	-	N/u	r/w	0
[12]	TEST_2	Test_2 1 = When set, the DOUT signal to the module (normally SSI Clock out is bypassed, and a internal nodes will by multiplexed on this pin. See Test_1 0 = Normal Mode	r/w	0
[11:10]	-	N/u	n/u	0
[9:8]	Test_Sel[1:0]	00 6.25 MHz 160 Ns 01 3.125 MHz 320 Ns 10 Interval Timer TC (Stretched to 500 Nsec) 11 Loop Back De-bounced CH1_INA to A_CH1_OUT		
[7:6]	IC4[1:0]	**Interface Control Channel 4** 00 Channel Disabled 01 SSI Mode 10 Counter Mode 11 Channel Disabled	r/w	0
[5:4]	IC3[1:0]	Interface Control Channel 3	r/w	0
[3:2]	IC2[1:0]	Interface Control Channel	r/w	0
[1:0]	IC1[1:0]	Interface Control Channel 1	r/w	0

Interrupt

Interrupt Vector Registers

Interrupt Assignment	VME Address
-Not Used-	03C0
SSI_CH_1 (n_Data)	03C2
SSI_CH_2 (n_Data)	03C4
SSI_CH_3 (n_Data)	03C6
SSI_CH_4 (n_Data)	03C8
Counter CH1_Match	03CA
Counter CH2_Match	03CC
Counter CH3_Match	03CE
Counter CH4_Match	03D0
Counter CH1 Index_Int	03D2
Counter CH2 Index_Int	03D4
Counter CH3 Index_Int	03D6
Counter CH4 Index_Int	03D8
Interval Timer (TC)	03DA
Multi_Cycle_Rd	03DC
-Not Used-	03DE

Interrupts generated from each subsystem, are encoded as indicated and passed through the MOD_BUS interrupt services to generate a vectored bus interrupt.

Interrupt Status

The interrupt status is read only. This status indicates the state of pending interrupts for this module.

Please Note; reading or writing to this register has no effect on the status of any interrupts. Interrupts must be cleared by reading the status at the subsystem level. As an example clearing the interrupt flag for SSI_CH1, the processor would read the SSI status register for CH1.

Bit	Symbol	Description	Access
[15]		-Not Used- (Read as Zero)	0
[14]	Multi_Cycle_Rd	Multi-Cycle Read Complete	r
[13]		-Not Used- (Read as Zero)	0
[12]		-Not Used- (Read as Zero)	0
[11]		-Not Used- (Read as Zero)	0
[10]		-Not Used- (Read as Zero)	0
[9]		-Not Used- (Read as Zero)	0
[8]	Match_CH4	Counter Match Interrupt – CH3	r
[7]	Match_CH3	Counter Match Interrupt – CH2	r
[6]	Match_CH2	Counter Match Interrupt – CH1	r
[5]	Match_CH1	Counter Match Interrupt – CH1	r
[4]	SSI_CH4	SSI Interrupts – CH4	r
[3]	SSI_CH3	SSI Interrupts – CH3	r
[2]	SSI_CH2	SSI Interrupts – CH2	r
[1]	SSI_CH1	SSI Interrupts – CH1	r
[0]		-Not Used- (Read as Zero)	

Interrupt Enable Register

The Interrupt mask register has the format as the table below. To enable an interrupt a (1) must be written to the corresponding bit in the mask register.

Bit	Symbol	Description	Access
[15]		-Not Used- (Read as Zero)	
[14]	Multi_Cycle_Rd	Multi-Cycle Read Complete	r/w
[13]	Interval Timer	Interval Timer TC	r/w
[12]	Cnt_Mde_Int_CH4	Index Control Mode Event – CH4	r/w
[11]	Cnt_Mde_Int_CH3	Index Control Mode Event – CH3	r/w
[10]	Cnt_Mde_Int_CH2	Index Control Mode Event – CH2	r/w
[9]	Cnt_Mde_Int_CH2	Index Control Mode Event – CH1	r/w
[8]	Match_CH4	Counter Match Interrupt – CH3	r/w
[7]	Match_CH3	Counter Match Interrupt – CH2	r/w
[6]	Match_CH2	Counter Match Interrupt – CH1	r/w
[5]	Match_CH1	Counter Match Interrupt – CH1	r/w
[4]	SSI_CH4	SSI Interrupts – CH4	r/w
[3]	SSI_CH3	SSI Interrupts – CH3	r/w
[2]	SSI_CH2	SSI Interrupts – CH2	r/w
[1]	SSI_CH1	SSI Interrupts – CH1	r/w
[0]		-Not Used- (Read as Zero)	

De-bounce, Digital Input Filter

De-bounce time can be utilized when channel is selected as an input to “filter” or “ignore” spurious initial transitions. Enter required de-bounce time into appropriate channel registers. Once a signal level is a logic voltage level period longer than the De-bounce time, a logic transition is validated. Signal pulse widths less than de-bounce time are filtered. Once valid, the transition status register flag is set for the channel and the output logic changes state. Enter a value of 0 to disable de-bounce filtering.

De-bounce resolution= 20 ns x 2. This results in a minimum resolution of 40 ns (de-bounce LSB=0) and a maximum filter value of (65,534 * 20E-9) or 1.311 msec.

De-bounce Register High [15:0]

Bit	Symbol	Description	Access	Reset Value
[15:0]	Cnt[15:0]	De-bounce Period [15:0]	r/w	0

De-bounce Register Low [0]

Bit	Symbol	Description	Access	Reset Value
[15:1]	-	N/u	r/w	0
[0]		Bypass 0 = De-bounce Circuit Bypassed (Disabled) 1= The Input Signal is Filtered According to the Filter Counter Value	r/w	0

CPLD (Module Configuration Registers)

CPLD Register High

Bit	Symbol	Description	Access	Reset Value
[15:13]	-	N/u	r/w	0
[12]	Test_1	Test 1 = Connects R0_A (the LTC2854 receiver output) directly to DI_IDX, the transmit data pin of the Index CHannel). This is useful for verification of input signal level and DAC offset voltage settings. 0 = Normal mode DI_IDX is connect to the DIN from the Module FPGA (Across the isolation barrier)	r/w	0
[11]	Ctrl_H_Idx	INDEX Channel Control H 1 = Disables a by-pass switch, and inserts additional 7.5k in series with the RS485 transceiver 0 = Enables the by-pass an connects the transceiver directly to the connector pins. (see text)	r/w	0
[10]	Ctrl_l_Idx	INDEX Channel Control L 1 = Disables a by-pass switch, and inserts additional 7.5k in series with the RS485 transceiver 0 = Enables the by-pass and connects the transceiver directly to the connector pins. (see text)	r/w	0
[9]	De_Idx	Driver Enable INDX 1 = De enables the driver. 0 = Force the driver outputs into a high impedance.	R/w	0
[8]	Te_Idx	Termination Enable INDX 0 = Disables 120 ohm termination (useful for multi-drop) 1 = Enables termination resistor	r/w	0
[7]	Ctrl_H_B	B Channel Control H	r/w	0
[6]	Ctrl_H_B	B Channel Control L	r/w	0
[5]	De_B	Driver Enable CH_B	r/w	0
[4]	Te_B	Termination Enable CH_B	r/w	0
[3]	Ctrl_H_A	A Channel Control H	r/w	0
[2]	Ctrl_l_A	A Channel Control H	r/w	0
[1]	De_A	Driver Enable CH_A	r/w	0
[0]	Te_A	Termination Enable CH_A	r/w	0

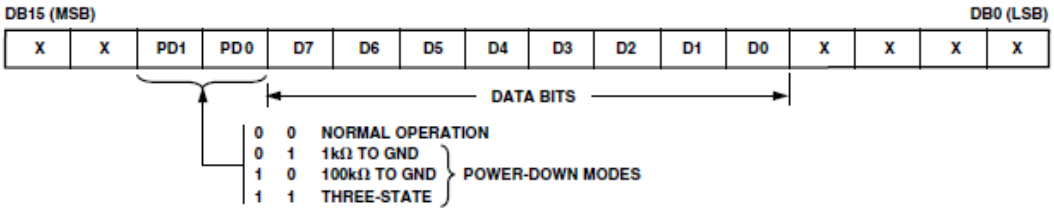
Note: The driver enable (de) bit must be set to enable its associated RS485 transmitter. Currently there is only one operational mode where the RS485 transmitter needs to be enabled. This would be the SSI Normal mode. In this mode the module supplies a burst clock signal used to read back data from an external encoder. In this SSI normal mode, the SSI output clock signal is available for all channels (A, B, and INDEX). The (de) bit should only be set for the l channel supplying the clock signal, for all other channels the (de) bit should be zero. When the de bit is zero the transmitter +, - outputs are high impedance.

In addition, when a channel is in receiver mode (typical operation mode) the (de) bit is zero (0), and the (te) bit is set (1). Although it is possible to set the Driver enable and Termination enable bit on, there operation should be considered mutually exclusive. The 120 ohm termination should be enable when the channel is in receive mode, and disabled for transmit.

CPLD Register Low

Bit	Symbol	Description	Access	Reset Value
[15:14]	X	n/u	r/w	0
[13]	PD1		r/w	
[12]	PD0		r/w	
[11:4]	Data[7:0]	DAC output voltage / DAC	r/w	
[3:0]	X	n/u	r/w	0

The CPLD register low is used the set the DAC off set voltage



The CPLD register low is used the set the DAC off set voltage.

Operating in single ended mode requires that the (-) module input pins are switched to ground. When a channel is set for single ended operation, this register is used to set the input threshold voltage for the single ended inputs.

Each cannel has a single 8 bit DAC that sets the threshold voltage for all three input pins (INDX, A, and B). For correct operation, single end or differential IO must be selected on a channel basis. For correct operation for either differential or single ended modes, the DAC input signals PD [1:0] bits must be set to [00].

In single ended mode the input threshold voltage maybe adjusted from 0v to 3.75v. The threshold voltage is adjusted, by writing register bits [11:4], DAC data [7:0]. Each single binary step equals a threshold voltage of .0147V. When operating in differential mode, the bit [11:4], DAC data [7:0] must be set to zero.

In order to operate in single ended mode several switches must also be correctly set;

the (ctrl_l_idx. ctrl_l_B, ctrl_l_A) bits in the CPLD register High must be set (1). Setting these bits isolates the DAC voltage output from the grounded (-) input pins. Setting the (ctrl_l_idx. ctrl_l_B, ctrl_l_A) bits insert in a series a 7.5K resistor between the grounded input pins and the voltage output of the DAC.

The termination enables (te_idx te_b, and te_a) bits must be zero. There is no differential termination in single ended mode.

Differential (DE) / Single-Ended (SE) Selection

Bit	Symbol	Description	Access	Reset Value
[15:1]	-	n/u (reserved, always returns 0)	r	0
[0]	Diff_se	Diff_se 1 = sets single ended mode by grounding the ALO, BLO and INDEX pin. 0 = Default; Differential Input Mode	r/w	0

The (diff_se) bit selects single end operational mode. Setting this bit (1), switches the inverting (-) input pins (A, B, and INDX) to the channel's isolated ground. This provides a ground return, and a ground reference for single ended signals.

CPLD Status

Bit	Symbol	Description	Access	Reset Value
[15:8]	-	N/u	r	0
[7:6]	-	Always High (1)	r	1
[5]	-	Always Zero (0)	r	0
[4]	Err_idx	ERR_INDEX 1= Error On Received Index Pulse. A one indicates a difference on the LT2854 received data and the AM28LV32E receivers for more than 1usec. 0 = Normal Operation	r	0
[3]	Err_b	ERR_CHB 1= Error On Received Index Pulse. A one indicates a difference on the LT2854 received data and the AM28LV32E receivers for more than 1usec. 0 = Normal Operation	r	0
[2]	Err_a	ERR_CHA 1= Error On Received Index Pulse. A one indicates a difference on the LT2854 received data and the AM28LV32E receivers for more than 1usec. 0 = Normal Operation	r	0
[1]	-	Always Zero (0)	r	0
[0]	-	Always Zero (1)	r	0

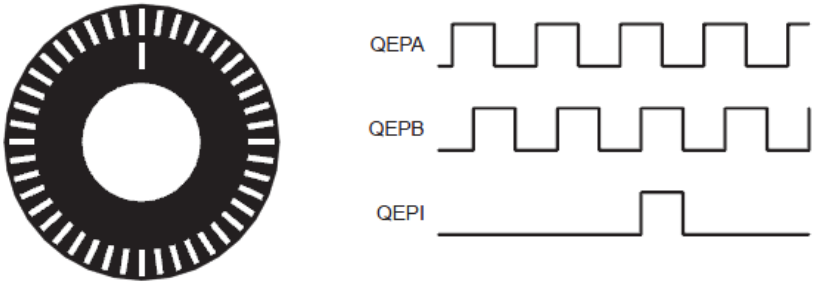
Appendix A – Quadrature (A-Quad-B) Discussion

Quadrature Count

The quadrature encoder module is used for direct interface with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine for use in a motion and position-control system.

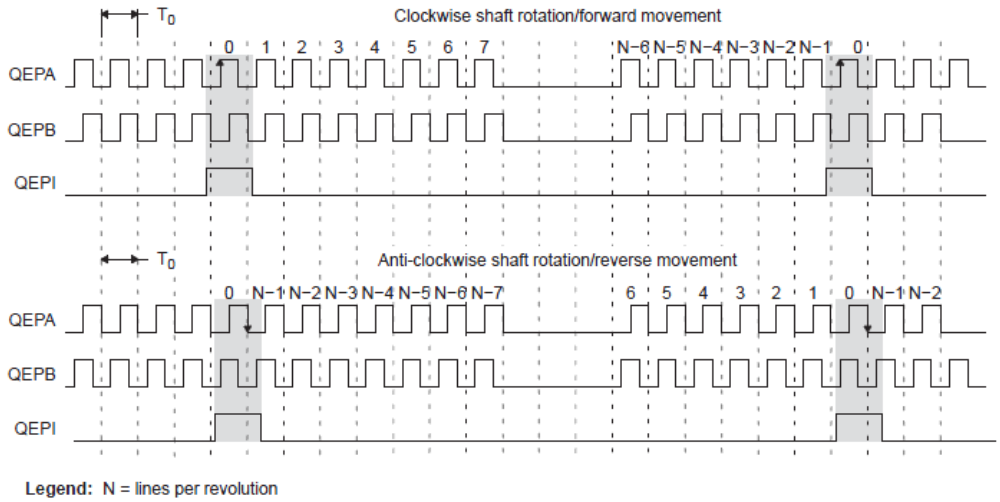
A single track of slots patterns the periphery of an incremental encoder disk, as shown in Figure 1. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark / light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: IDDX), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position, and zero reference.

Figure 1. Optical Encoder Disk



To derive direction information, the lines on the disk are read out by two different photo-elements that "look" at the disk pattern with a mechanical shift of 1/4 the pitch of a line pair between them. This shift is realized with a reticle or mask that restricts the view of the photo-element to the desired part of the disk lines. As the disk rotates, the two photo-elements generate signals that are shifted 90 out of phase from each other. These are commonly called the quadrature QEPA and QEPB signals. The clockwise direction for most encoders is defined as the QEPA channel going positive before the QEPB channel and vise versa as shown in Figure 2.

Figure 2. QEP Encoder Output Signal for Forward/Reverse Movement

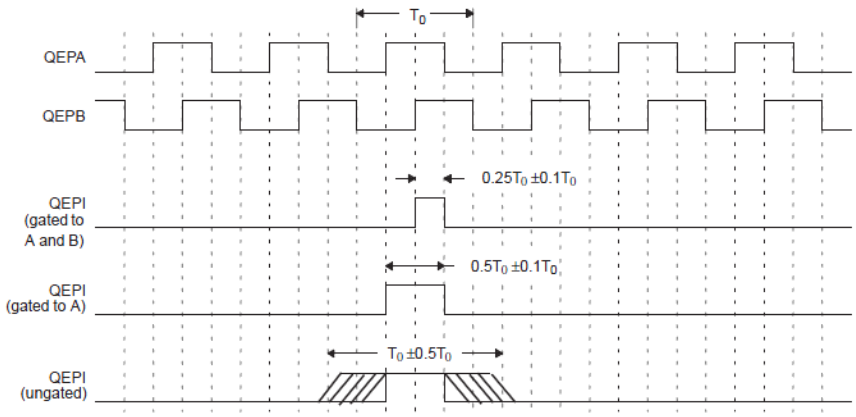


Legend: N = lines per revolution

The encoder wheel typically makes one revolution for every revolution of the motor or the wheel may be at a geared rotation ratio with respect to the motor. Therefore, the frequency of the digital signal coming from the QEPA and QEPB outputs varies proportionally with the velocity of the motor. For example, a 2000-line encoder directly coupled to a motor running at 5000 revolutions per minute (rpm) results in a frequency of 166.6 KHz, so by measuring the frequency of either the QEPA or QEPB output, the processor can determine the velocity of the motor.

Quadrature encoders from different manufacturers come with two forms of index pulse (gated index pulse or un-gated index pulse) as shown in Figure 3. A nonstandard form of index pulse is un-gated. In the un-gated configuration, the index edges are not necessarily coincident with A and B signals. The gated index pulse is aligned to any of the four quadrature edges and width of the index pulse and can be equal to a quarter, half, or full period of the quadrature signal.

Figure 3. Index Pulse Example



Some typical applications of shaft encoders include robotics and even computer input in the form of a mouse. Inside your mouse you can see where the mouse ball spins a pair of axles (a left/right, and an up/down axle). These axles are connected to optical shaft encoders that effectively tell the computer how fast and in what direction the mouse is moving.

General Issues:

Estimating velocity from a digital position sensor is a cost-effective strategy in motor control. Two different first order approximations for velocity may be written as:

$$v(k) \approx \frac{x(k) - x(k-1)}{T} = \frac{\Delta X}{T}$$

$$v(k) \approx \frac{X}{t(k) - t(k-1)} = \frac{X}{\Delta T}$$

Where:

v(k): Velocity at time instant k
x(k): Position at time instant k
x(k-1): Position at time instant k-1
T: Fixed unit time or inverse of velocity calculation rate
ΔX: Incremental position movement in unit time
t(k): Time instant "k"
t(k-1): Time instant "k-1"
X: Fixed unit position
ΔT: Incremental time elapsed for unit position movement.

Equation 1 is the conventional approach to velocity estimation and it requires a time base to provide unit time event for velocity calculation. Unit time is basically the inverse of the velocity calculation rate.

The encoder count (position) is read once during each unit time event. The quantity [x(k) - x(k-1)] is formed by subtracting the previous reading from the current reading. Then the velocity estimate is computed by multiplying by the known constant 1/T (where T is the constant time between unit time events and is known in advance).

Estimation based on **Equation 1** has an inherent accuracy limit directly related to the resolution of the position sensor and the unit time period T. For example, consider a 500-line per revolution quadrature encoder with a velocity calculation rate of 400 Hz. When used for position the quadrature encoder gives a four-fold increase in resolution, in this case, 2000 counts per revolution. The minimum rotation that can be detected is therefore 0.0005 revolutions, which gives a velocity resolution of 12 rpm when sampled at 400 Hz. While this resolution may be satisfactory at moderate or high speeds, e.g. 1% error at 1200 rpm, it would clearly prove inadequate at low speeds. In fact, at speeds below 12 rpm, the speed estimate would erroneously be zero much of the time.

At low speed, **Equation 2** provides a more accurate approach. It requires a position sensor that outputs a fixed interval pulse train, such as the aforementioned quadrature encoder. The width of each pulse is defined by motor speed for a given sensor resolution. **Equation 2** can be used to calculate motor speed by measuring the elapsed time between successive quadrature pulse edges. However, this method suffers from the opposite limitation, as does **Equation 1.** A combination of relatively large motor speeds and high sensor resolution makes the time interval Δ**T** small, and thus more greatly influenced by the timer resolution. This can introduce considerable error into high-speed estimates.

For systems with a large speed range (that is, speed estimation is needed at both low and high speeds), one approach is to use **Equation 2** at low speed and have the DSP software switch over to **Equation 1** when the motor speed rises above some specified threshold.

Appendix B – Operation Mode Signal Details

Mode of Operation: 422 (Differential) 485 (Differential)
Input
Receiver Input Levels: -10V to +10V
Receiver Input Sensitivity: ±200mV
Input Resistance: 120Ω or >12kΩ (Each channel incorporates a 120 Ω termination resistor that can be programmed on a channel by channel basis)
Read Delay: 300 ns
De-Bounce: Programmable per bit from 0 to 343 s. LSB= programmable.
Output
Driver Output Voltage: -0.25V to +5V max.
Driver Output Signal Level ±2V ±1.5V (Loaded minimum)
Driver Output Signal Level ±5V (Unloaded maximum)
Driver Load Impedance: 100Ω 54Ω

Mode of Operation: 422 (Differential) 485 (Differential)
Input
Receiver Input Levels: 10V to +10V
Receiver Input Sensitivity: ±200mV
Input Resistance: 120Ω or >12kΩ (Each channel incorporates a 120 Ω termination resistor that can be programmed on a channel by channel basis)
Read Delay: 300 ns
De-Bounce: Programmable per bit from 0 to 343 s. LSB= programmable.
Output
Driver Output Voltage: -0.25V to +5V max.
Driver Output Signal Level ±2V ±1.5V (Loaded minimum)
Driver Output Signal Level ±5V (Unloaded maximum)
Driver Load Impedance: 100Ω 54Ω

Mode of Operation: 24V
Input
Receiver Input Levels:
Receiver Input Sensitivity:
Input Resistance:
Read Delay: 300 ns
De-Bounce: Programmable per bit from 0 to 343 s. LSB= programmable.
Output
Driver Output Voltage:
Driver Output Signal Level
Driver Output Signal Level

Mode of Operation: +- 5V
Input
Receiver Input Levels:
Receiver Input Sensitivity:
Input Resistance:
Read Delay: 300 ns
De-Bounce: Programmable per bit from 0 to 343 s. LSB= programmable.
Output
Driver Output Voltage:
Driver Output Signal Level
Driver Output Signal Level

Mode of Operation: +- 15V
Input
Receiver Input Levels:
Receiver Input Sensitivity:
Input Resistance:
Read Delay: 300 ns
De-Bounce: Programmable per bit from 0 to 343 s. LSB= programmable.
Output
Driver Output Voltage:
Driver Output Signal Level
Driver Output Signal Level

FOUR CHANNEL SSI/ENCODER (MODULE E7) VME MEMORY MAP

Module Length = 400h

000	SSI Control Register 0	Ch1	R/W	0A6	Counter Preload Low	Ch3	R/W	1A0	IN_A De-bounce High	Ch3	R/W
002	SSI Control Register 1	Ch1	R/W	0AA	Counter Control Register	Ch3	R/W	1A2	IN_A De-bounce Low	Ch3	R/W
008	SSI Received Data High	Ch1	R	0AC	Counter Command Reg.	Ch3	W	1A8	IN_B De-bounce High	Ch3	R/W
00A	SSI Received Data Low	Ch1	R	0AE	Counter Status Register	Ch3	R/W	1AA	IN_B De-bounce Low	Ch3	R/W
00C	SSI Received ZB, Parity	Ch1	R	0B4	Actual Counter Value High	Ch3	R	1B0	IN_INDX De-bounce High	Ch3	R/W
00E	SSI Status	Ch1	R/W	0B6	Actual Counter Value Low	Ch3	R	1B2	IN_INDX De-bounce Low	Ch3	R/W
01C	SSI Received High	Ch1	R	0BC	Counter Latch High	Ch3	R				
01E	SSI Received Low	Ch1	R	0BE	Counter Latch Low	Ch3	R	1C0	IN_A De-bounce High	Ch4	R/W
020	Match Data High	Ch1	R/W					1C2	IN_A De-bounce Low	Ch4	R/W
022	Match Data Low	Ch1	R/W	0C0	SSI Control Register 0	Ch4	R/W	1C8	IN_B De-bounce High	Ch4	R/W
024	Counter Preload High	Ch1	R/W	0C2	SSI Control Register 1	Ch4	R/W	1CA	IN_B De-bounce Low	Ch4	R/W
026	Counter Preload Low	Ch1	R/W	0C8	SSI Received Data High	Ch4	R	1D0	IN_INDX De-bounce High	Ch4	R/W
02A	Counter Control Register	Ch1	R/W	0CA	SSI Received Data Low	Ch4	R	1D2	IN_INDX De-bounce Low	Ch4	R/W
02C	Counter Command Register	Ch1	W	0CC	SSI Received ZB, Parity	Ch4	R				
02E	Counter Status Register	Ch1	R/W	0CE	SSI Status	Ch4	R/W	1E0	CPLD configuration H	Ch1	R/W
034	Actual Counter Value High	Ch1	R	0DC	SSI Received High	Ch4	R	1E2	CPLD configuration L	Ch1	R/W
036	Actual Counter Value Low	Ch1	R	0DE	SSI Received Low	Ch4	R	1E4	CPLD Status	Ch1	R/W
03C	Counter Latch High	Ch1	R	0E0	Match Data High	Ch4	R/W	1E6	DIFF/SE interface select	Ch1	R/W
03E	Counter Latch Low	Ch1	R	0E2	Match Data Low	Ch4	R/W	1E8	CPLD configuration H	Ch2	R/W
				0E4	Counter Preload High	Ch4	R/W	1EA	CPLD configuration L	Ch2	R/W
040	SSI Control Register 0	Ch2	R/W	0E6	Counter Preload Low	Ch4	R/W	1EC	CPLD Status	Ch2	R/W
042	SSI Control Register 1	Ch2	R/W	0EA	Counter Control Register	Ch4	R/W	1EE	DIFF/SE interface select	Ch2	R/W
048	SSI Received Data High	Ch2	R	0EC	Counter Command reg.	Ch4	W	1F0	CPLD configuration H	Ch3	R/W
04A	SSI Received Data Low	Ch2	R	0EE	Counter Status Register	Ch4	R/W	1F2	CPLD configuration L	Ch3	R/W
04C	SSI Received ZB, Parity	Ch2	R	0F4	Actual Counter Value High	Ch4	R	1F4	CPLD Status	Ch3	R/W
04E	SSI Status	Ch2	R/W	0F6	Actual Counter Value Low	Ch4	R	1F6	DIFF/SE interface select	Ch3	R/W
05C	SSI Received High	Ch2	R	0FC	Counter Latch High	Ch4	R	1F8	CPLD configuration H	Ch4	R/W
05E	SSI Received Low	Ch2	R	0FE	Counter Latch Low	Ch4	R	1FA	CPLD configuration L	Ch4	R/W
060	Match Data High	Ch2	R/W					1FC	CPLD Status	Ch4	R/W
062	Match Data Low	Ch2	R/W	120	Interval Timer Preload		R/W	1FE	DIFF/SE interface select	Ch4	R/W
064	Counter Preload High	Ch2	R/W	122	Interval Timer Control		R/W	03C2	SSI Interrupt Vector	Ch1	R/W
066	Counter Preload Low	Ch2	R/W	138	Interval Timer Data Register		R	03C4	SSI Interrupt Vector	Ch2	R/W
06A	Counter Control Register	Ch2	R/W	140	Global Control Register High		R/W	03C6	SSI Interrupt Vector	Ch3	R/W
06C	Counter Command Register	Ch2	W	142	Global Control Register Low		R/W	03C8	SSI Interrupt Vector	Ch4	R/W
06E	Counter Status Register	Ch2	R/W	144	Interrupt Enable Register		R/W	03CA	Counter Match Interrupt Vector	Ch1	R/W
074	Actual Counter Value High	Ch2	R	148	Interrupt Status Register		R	03CC	Counter Match Interrupt Vector	Ch2	R/W
076	Actual Counter Value Low	Ch2	R	15E	Test Register		R	03CE	Counter Match Interrupt Vector	Ch3	R/W
07C	Counter Latch High	Ch2	R					03D0	Counter Match Interrupt Vector	Ch4	R/W
07E	Counter Latch Low	Ch2	R	160	IN_A De-bounce High	Ch1	R/W	03D2	Counter Match Interrupt Vector	Ch1	R/W
				162	IN_A De-bounce Low	Ch1	R/W	03D4	Counter Index Interrupt Vector	Ch2	R/W
080	SSI Control Register 0	Ch3	R/W	168	IN_B De-bounce High	Ch1	R/W	03D6	Counter Index Interrupt Vector	Ch3	R/W
082	SSI Control Register 1	Ch3	R/W	16A	IN_B De-bounce Low	Ch1	R/W	03D8	Counter Index Interrupt Vector	Ch4	R/W
088	SSI Received Data High	Ch3	R	170	IN_INDX De-bounce High	Ch1	R/W	03DA	Interval timer Interrupt Vector		R/W
08A	SSI Received Data Low	Ch3	R	172	IN_INDX De-bounce Low	Ch1	R/W	03DC	Multi Cycle Read Interrupt Vector		R/W
08C	SSI Received ZB, Parity	Ch3	R								
08E	SSI Status	Ch3	R/W	180	IN_A De-bounce High	Ch2	R/W	3B4	Design Version		R
09C	SSI Received High	Ch3	R	182	IN_A De-bounce Low	Ch2	R/W	3B6	Design Revision		R
09E	SSI Received Low	Ch3	R	188	IN_B De-bounce High	Ch2	R/W	3B8	DSP Version		R
0A0	Match Data High	Ch3	R/W	18A	IN_B De-bounce Low	Ch2	R/W	3BA	FPGA Version		R
0A2	Match Data Low	Ch3	R/W	190	IN_INDX De-bounce High	Ch2	R/W	3BC	Module ID		R
0A4	Counter Preload High	Ch3	R/W	192	IN_INDX De-bounce Low	Ch2	R/W				

ISOLATED ±15V DC/DC CONVERTER (MODULE V1, V2)

Description

The V1 module provides a single channel, isolated bipolar (+/-) 15V power source output. The V2 module provides two identical, individually programmable, fully isolated bipolar ±15VDC DC/DC converters. Each DC/DC converter can source and sink up to 450mA. Each converter can be used independently and features current output and voltage output monitoring, and a programmable current limit. Both converters are isolated and may be tied in series for applications requiring higher output voltages. For clarity, the two converters are referenced as channels 1 & 2.

Features:

- Programmable for output current limit
- Continuous Background Built in Testing (BIT) during normal operation, status provided for channel health and operation feedback.

Principles of Operation

The V1 incorporates a single programmable isolated converter output. The V2 module incorporates two independently programmable galvanically isolated DC/DC converters. Each converter has bipolar ±15VDC output and a separate ISO ground return. A single converter output may be used to supply +15VDC, and -15VDC, with each output supplying a different load current. Both converter outputs may be used together for applications requiring ±15VDC or 30VDC. Two converters may be tied in series to provide output voltages up to 60VDC. Power into the DC/DC converter is supplied through the ±12V power connections on the platform board. Please refer to the platform board documentation for I/O connections.

The V1 and/or V2 modules provide both continuous output voltage and output current monitoring. The output voltage and current values are provided separately for the (+) positive and (-) negative outputs. Each converter has a single programmable output current threshold. Exceeding the threshold for either the + or – outputs for longer than three seconds automatically triggers a fault and shuts down the converter. The default setting for the current threshold is set @ 450ma. This current threshold value may be reprogrammed by the user to a lower threshold value. Output is restored after a fault by removing the over current condition and clearing the fault flag(s).

This module provides an automatic background Built-In-Test (BIT) for each channel. The BIT functions are always enabled and continually checks that each channel is functional.

The module design utilizes state of the art galvanic isolation that is superior to alternatives such as optocoupler devices. The galvanic isolation eliminates typical optocoupler design concerns such as uncertain current transfer ratios, nonlinear transfer functions and temperature/lifetime degradation effects.

Continuous Background Built-in-Testing (BIT)

BIT is always enabled, and continually checks that each channel is functioning correctly. This capability is accomplished by internal test circuitry that is incorporated into the module. The BIT circuit is sequentially connected across each channel and checks that the commanded operation is correctly set. Dependent upon the configuration, BIT verifies that the output agrees with the test data, or a possible fault is indicated.

Registers

On/Off

The On/Off register turns on or off both of the DC/DC converters. When D0 or D1 is set, the associated converter is on. The module power on default is zero (0x0000) off. The state of the On/Off register is not affected by a fault condition, and it is not necessary to write to this register when recovering from a fault.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2	1	Channel
RESET OVER-CURRENT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D	D	D=DATA BIT

Current Limit Threshold

The Current limit threshold register sets the output current trip point for both the negative and positive outputs of bipolar power supply. When the current limit threshold value is exceeded for more than three second a fault condition is flagged and the DC/DC converter is shutdown. The current limit value is an unsigned 16-bit number where the LSB is 1mA. The user may reprogram the current limit threshold to a value lower than the 450mA.

The maximum current the DC/DC converter can supply is 450mA. On power up or system reset this register defaults to 450mA (0x01c2). Writing this register with a value greater than 450mA, results in the module using the default value of 450mA.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								256	128	64	32	16	8	4	2	1	value in mA
Threshold	0	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D=DATA BIT

Output Voltage (V+)

This register contains an averaged value for the positive + supply output voltage of the DC/DC converter. The Output Voltage (+) register is an unsigned 16-bit number where the LSB is 1mVDC.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	X	X	8196	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	value in mVDC
Output Voltage	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Output Voltage (V-)

This register contains an averaged value for the negative - supply output voltage of the DC/DC converter. The Output Voltage (-) register is an unsigned 16-bit number where the LSB is 1mVDC.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	X	X	8196	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	value in mVDC
Output Voltage	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Output Current (V+)

This register contains an averaged value for the positive + supply output current of the DC/DC converter. The Output Current (+) register is an unsigned 16-bit number where the LSB is 1mA.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	X	X	X	X	X	X	X	256	128	64	32	16	8	4	2	1	value in mA
Threshold	0	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D=DATA BIT

Output Current (V-)

This register contains an averaged value for the negative - supply output current of the DC/DC converter. The Output Current (+) register is an unsigned 16-bit number where the LSB is 1mA.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	X	X	X	X	X	X	X	256	128	64	32	16	8	4	2	1	value in mA
Threshold	0	0	0	0	0	0	0	D	D	D	D	D	D	D	D	D	D=DATA BIT

Fault

The Fault register is a read only register that contains two over current fault flags. One flag bit for each channel as indicated. The fault flag is set when the converter output current exceeds the programmed current threshold limit for more than three seconds. To recover from a fault the Fault register must be cleared and the condition that caused the excessive output current must be removed before the power supply will restart.

The Fault register is cleared by writing a 0x0001 to the Clear Fault register address.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	2	1	Channel
RESET OVER-CURRENT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D	D	D=DATA BIT

Clear Fault

The Clear Fault register is used to clear the over current fault flag bits. The Fault flags for both channels are cleared by writing a 0x0001 to this address. Reading this register location always returns zero (0x0000).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESET OVER-CURRENT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D	D=DATA BIT

Interrupt and Status Register Operation/Clarification

Unless otherwise specifically stated, the following represents a general operation/clarification note for the Interrupt operation and its associated/coinciding "latching" – type Status Register(s):

- An interrupt will be generated when the specific channel interrupt is enabled and there is a detection of the respective channel transition change in the appropriate channel of the corresponding Status Register.
- Status Register(s) are "latching"; as defined, any noted transitional change on any channel will "latch" the entire Status Register.
- Once latched, there will be no further state change "sensed" by the interrupt mechanism, hence, no further interrupts.
- The act of reading a Status Register will "unlatch" that particular status register (doesn't necessarily clear immediately, but will update and clear on the next internal loop cycle).
- Because transitional changes will "latch" the Status Register, and the interrupt mechanism uses the Status Register as its trigger, before an interrupt is generated and after an interrupt is generated, the Status Register must be read "until cleared".

The following is recommended for Interrupt and associated Status Register initialization and handling (assuming vectors and interrupt level (if appropriate) are being properly/appropriately initialized):

- **Power-up**
  - Perform normal initializations (card/channel initializations/interrupt vector/interrupt enable/ etc.).
  - Perform a software read loop (part of the host application software initialization routine(s)) on the specific Status Registers of concern ("loop to clear") - this would also be similar to an Interrupt Service Routine (ISR) "loop to clear" function.

    Ex: Running the 'loop to clear' on the appropriate Status Register(s) during the initialization (after I/O function is programmed) will ensure any spurious transitions detected on power-up are "cleared" and the channel(s) are primed and ready to trigger for interrupts.
  - <Signal transition occurs> - for the specific interrupt enabled channels
  - Initial interrupt should occur (if initialized/enabled)
- **Interrupt Software Routine (ISR)**

  The ISR is typically a software (SW) handling branch (part of host application software) structured to "loop to read and clear" the specific Status Register(s) associated with the interrupt type (i.e. H-L or L-H transition). The SW loop should "read" the Status Register until cleared (typically, this is 2 or 3 times) to ensure any other channel transitions are accounted for during the ISR process while the respective Status Register(s) were "latched" – the act of reading the Status Register(s) allows the channel(s) that set the transition/latch to clear and effectively "re-arm" for the next transition to occur.

  Ex: The ISR should have the 'loop to clear' – to ensure all transitions are accounted for – and the channel(s) are ready to trigger for next event.

NOTES:

- Any channel on the Status Register could latch the register regardless if the channel(s) interrupts are enabled or not.
- For Status Registers that are bit mapped for either input or output, programming outputs that change transitions will also "latch" the Status Register(s) – so, a subsequent read to the Status Register after the write operation should be performed to ensure the Status Register is unlatched, clear and ready to trigger on next event.

MODULE (V*), Dual ±15V DC/DC converter, VME MEMORY MAP

(Module size = 400h)

000	On_0ff		R/W
	(skipped)		
008	Current Threshold	Ch.01	R/W
00A	Current Threshold	Ch.02	R/W
00C	Output Current (V+)	Ch.01	R
00E	Output Current (V-)	Ch.01	R
010	Output Voltage (V+)	Ch.01	R
012	Output Voltage (V-)	Ch.01	R
024	Output Current (V+)	Ch.02	R
026	Output Current (V-)	Ch.02	R
028	Output Voltage (V+)	Ch.02	R
02A	Output Voltage (V-)	Ch.02	R
	(skipped)		
02C	Fault		R
02E	Clear Fault		R/W
	(skipped)		
3A8	(reserved)		
3AA	(reserved)		
3AE	(reserved)		
	(skipped)		
3B2	(reserved)		
3B4	Module Design Version		R
3B6	Module Design Revision		R
3B8	DSP Version		R
3BA	FPGA Version		R
3BC	Module ID		R

Note: For V1 module, only CH1 applies (where applicable).

REFERENCE (MODULE W*)

Reference (Module W*) - See part number designation)

Principle of Operation

When a secondary reference source is required, other than the optional on-board reference module (available on certain model boards, see part number), the W* Reference Module can be utilized to provide an AC signal source.

The single channel isolated AC output is programmable for full range voltage output from 2 to 115 VAC, and frequency from 47 Hz to 20 KHz (see detailed specification characteristics – operation must remain within the specified voltage/frequency/power limits.

Overcurrent protection is provided via a sensing circuit which provides automatic re-try for ten seconds before shutdown.

Suggested initialization is to program reference frequency first, reference voltage, and power on module. The three versions are:

Module Code	Output VL-L	Frequency Band
W1	2-115 VRMS	47 Hz - 20 KHz (within characterized limits – see specification)
W2	2-28 VRMS	47 Hz - 20 KHz (within characterized limits – see specification)
W3	28-115 VRMS	47 Hz - 20 KHz (within characterized limits – see specification)

Note: W1 utilizes mechanical relay for range switching. May not be suitable for some embedded system applications.

Reference Frequency

Type: 16-bit unsigned integer

Range: 47 to 10,000 Hz

Read/Write: R/W

Initialized Value: N/A

Program Reference Frequency, where LSB is 0.01 Hz. For example: To program 400 Hz, 400 x 100= 40,000, which equals 0x9C40. In this example, 0x0000 would be programmed in the *Reference Frequency High* register, and 0x9C40 would be programmed in the *Reference Frequency Low* register. To program 10,000 Hz, 10,000 x 100= 1,000,000 which equals 0xF4240. In this example, 0x000F would be programmed in the *Reference Frequency High* register, and 0x4240 would be programmed in the *Reference Frequency Low* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	327.68	163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	0.01	approximate value
REF FREQUENCY LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	0	0	0	0	0	0	5242.88	2621.44	1310.72	655.36	approximate value
REF FREQUENCY HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

Reference Voltage

Type: 16-bit unsigned integer
Range: 2.0 to 115.0 VRMS
Read/Write: R/W
Initialized Value: N/A

Program Reference Voltage, where LSB is 0.01 VRMS. For example: To program 26.1 VRMS, 26.1 x 100= 2610, which equals 0xA32. In this example, 0x0000 would be programmed in the *Reference Voltage High* register, and 0x0xA32 would be programmed in the *Reference Voltage Low* register. To program 115 VRMS, 115 x 100= 11,500 which equals 0x2CEC. In this example, 0x0000 would be programmed in the *Reference Voltage High* register, and 0x2CEC would be programmed in the *Reference Voltage Low* register. Note: *Reference Voltage High* register always remains at 0x0000.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	81.92	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	0.01	approximate value
REF VOLTAGE LO	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (V)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	approximate value
REF VOLTAGE HI	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (V)

Reference Module Power Enable

Type: 16-bit unsigned integer
Range: 0,1
Read/Write: R/W
Initialized Value: 0

The *Reference Module Power Enable* register is utilized for Reference module output/power control. Set the bit to enable the power output stage of the Reference module. "1" = Enable; "0" = Disabled. Initialized default is "0".

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Module Power Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D

Reference Overcurrent[1]

Type: 16-bit unsigned integer
Range: 0,1
Read/Write: R/W
Initialized Value: 0

The *Reference Overcurrent* register is utilized for status and re-set of the reference module overcurrent protection circuit. In normal operation, this register will be defaulted to "0". This is a status indication that the reference module is NOT in overcurrent condition. If the channel senses an over current condition, the module will automatically shut down and re-enable the output approximately every 1.3 seconds for a total of 10 seconds. After approximately 10 seconds, if the overcurrent condition has persisted, the output stage will be shut-down and the *Reference Overcurrent* register will be set to "1". To re-enable the output stage and re-engage the automatic 10 second overcurrent protection circuit, write a "0" to the *Reference Overcurrent* register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D/S Module Power Enable	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D

Note1: Reference Overcurrent feature added for DOM 8/2010 and later.

REFERENCE (MODULE W*) VME MEMORY MAP

100	Reference Frequency Lo	R/W
102	Reference Frequency HI	R/W
104	Reference Voltage Lo	R/W
106	Reference Voltage Hi	R/W
110	Reference Overcurrent[1]	R/W
3B4	Module Design Version	R
3B6	Module Design Revision	R
3B8	Module DSP	R
3BA	Module FPGA	R
3BC	Module ID	R
0E0	Power On	R/W

Note1: Reference over-current added for DOM 8/2010 and later.

MODULE IDENTIFICATION

Module Design Version

Type: ASCII character (in each upper and lower byte)

Range: N/A

Read/Write: R

Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1" are together 3120h.

Module Design Version																
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
ASCII "1"								ASCII " "								

Module Design Revision

Type: ASCII character (in each upper and lower byte)

Range: N/A

Read/Write: R

Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B" are together 4220h.

Module Design Revision																
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
ASCII "B"								ASCII " "								

Module DSP Revision

Type: binary word

Range: 1 to 65535

Read/Write: R

Initialized Value: N/A

Read register as 16 bit binary word to determine Module DSP revision. For example, 0x000B is revision 12.

Module DSP Revision																
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA Revision

Type: binary word

Range: 1 to 65535

Read/Write: R

Initialized Value: N/A

Read register as 16 bit binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

Module FPGA Revision																
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)

Range: N/A

Read/Write: R

Initialized Value: 4331h

Read register to determine Module ID in ASCII. For example, ASCII “C” in upper byte and ASCII “1” in lower byte, for Module “C1,” are together 4331h.

Module ID																
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D		D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
ASCII “C”								ASCII “1”								

GENERAL USE REGISTER MEMORY MAP

The registers of this memory map apply to the complete card.

Common User Register Memory Map (VME)

0000	Part number	R	0026	IP Address LO (Port A)	R	0050	(reserved)	R
0002	Serial number (LO)	R	0028	IP Submask HI (Port A)	R	0070	IP Address HI (Port B)	R
0004	Date Code	R	002A	IP Submask LO (Port A)	R	0072	IP Address LO (Port B)	R
0006	Revision Level, PCB	R	002C	IP Gateway HI (Port A)	R	0074	IP Submask HI (Port B)	R
0008	Revision Level, Interface DSP	R	002E	IP Gateway LO (Port A)	R	0076	IP Submask LO (Port B)	R
000A	Revision Level, Interface FPGA	R	0030	MAC Address HI (Port A)	R	0078	IP Gateway HI (Port B)	R
000C	Board Ready	R	0032	MAC Address MID (Port A)	R	007A	IP Gateway LO (Port B)	R
000E	Watchdog Timer	R/W	0034	MAC Address LO (Port A)	R	007C	MAC Address HI (Port B)	R
0010	Soft reset	R/W	0036	Status, TELNET	R	007E	MAC Address MID (Port B)	R
0012	(reserved) (latch A/Ds)	R	003C	Status, MAC Connect	R	0080	MAC Address LO (Port B)	R
0014	(reserved) (latch S/Ds)	R	003E	IPV6 Prefix (Port A)	R	0084	IPV6 Prefix (port B)	R
0016	(reserved) (number of modules)	R	0040	IPV6 Address 8 (Port A)	R	0086	IPV6 Address 8 (Port B)	R
0018	Version, Design	R	0042	IPV6 Address 7 (Port A)	R	0088	IPV6 Address 7 (Port B)	R
001A	Platform	R	0044	IPV6 Address 6 (Port A)	R	008A	IPV6 Address 6 (Port B)	R
001C	Model	R	0046	IPV6 Address 5 (Port A)	R	008C	IPV6 Address 5 (Port B)	R
001E	Generation	R	0048	IPV6 Address 4 (Port A)	R	008E	IPV6 Address 4 (Port B)	R
0020	(reserved) (special spec.)	R	004A	IPV6 Address 3 (Port A)	R	0090	IPV6 Address 3 (Port B)	R
0022	Interrupt Level	R/W	004C	IPV6 Address 2 (Port A)	R	0092	IPV6 Address 2 (Port B)	R
0024	IP Address HI (Port A)	R	004E	IPV6 Address 1 (Port A)	R	0094	IPV6 Address 1 (Port B)	R
						0096	Serial number (HI)	R
						01A0 – 01BE	Customer defined register allocation	W/R

Part Number

Type: unsigned integer word
Range: 0000h to FFFFh
Read/Write: R
Initialized Value: not applicable
This register contains the product part number. A unique 16-bit code is assigned to each part number.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PART NUMBER	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Serial Number

Type: unsigned integer word
Range: 0000h to FFFFh
Read/Write: R
Initialized Value: not applicable
This register contains the board serial number. As of date of manufacture (DOM) 7/2014: read as a (2)16-bit binary words (HI, LO concatenated).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SERIAL NUMBER	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Platform

Type: ASCII character (in each upper and lower byte)
Range: not applicable
Read/Write: R
Initialized Value: 3634h
The register holds the VME platform code “64” in ASCII. ASCII “6” is in upper byte and ASCII “4” is in lower byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PLATFORM	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “6”								ASCII “4”								

Model

Type: ASCII character (in each upper and lower byte)
Range: not applicable
Read/Write: R
Initialized Value: 4550h
This register holds product model code “E” in ASCII. ASCII “E” is in upper byte and ASCII “P” is in lower byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODEL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “E”								ASCII “P”								

Generation

Type: ASCII character (in each upper and lower byte)
Range: not applicable
Read/Write: R
Initialized Value: 3320h
This register holds product generation code “3” in ASCII. ASCII “3“ is in upper byte and ASCII “ ” is in lower byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
GENERATION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “3 ”								ASCII “ ”								

Special Spec

Type: ASCII character (in each upper and lower byte)
Range: not applicable
Read/Write: R
Initialized Value: 2020h
This register holds product special code in ASCII. ASCII “spaces” are used for none where ASCII “ “ is in upper byte and ASCII “ ” is in lower byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “ ”								ASCII “ ”								

Date Code

Address: 7F2h
Type: unsigned integer word
Range: 0000h to FFFFh
Read/Write: R
Initialized Value: not applicable
This register contains the date of manufacture. It is read as a four digit decimal number, where four digits represent YYWW (Year, Year, Week, Week). **For example**, 0126 converts to the 26th week of 2001.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
DATE CODE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A
Read register to determine Module ID in ASCII. There is one register for each module slot (1 through 3). **For example**, Module P1 register contents where slot is populated with module P1 would contain ASCII "P" in upper byte and ASCII "1" in lower byte, together 5031h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	Example ASCII "P"								ASCII "1"								

Revision Level, Interface FPGA

Type: unsigned integer word
Range: not applicable
Read/Write: R
Initialized Value: not applicable
Read register to determine VME hardware revision number.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PCB REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Revision Level, Interface DSP

Type: unsigned integer word
Range: 0 to 65535
Read/Write: R
Initialized Value: not applicable

Read register to determine module processor firmware revision number.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PROCESSOR REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Board Ready

Type: binary word
Range: not applicable
Read/Write: R
Initialized Value: not applicable

Poll register. Board is ready to be accessed **only after** you read "AA55" (depends on configuration; may be as much as 10 seconds). Following a soft reset, *Board Ready* continues to indicate 0xAA55 until approx 150ms have elapsed. After that time the card is undergoing reset and the register indicates 0x0000. Following a soft reset, wait 200ms before polling *Board Ready*. The register indicates 0xAA55 which is board ready. You may proceed with read/write/coding activity after that change.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BOARD READY	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Watchdog Timer

Type: binary word
Range: not applicable
Read/Write: R
Initialized Value: 0h

This register implements a *Watchdog timer*. When it detects that a value, or word, has been written to it, that word will be inverted within 70 µs. The inverted word remains until replaced by a new word. The user, after 70 µs, looks for the inverted word to confirm that the processor is operating.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
WATCHDOG TIMER	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Soft Reset

Type: unsigned integer
Range: 0 to 1
Read/Write: R
Initialized Value: 0

Level sensitive. Writing a "1" initiates and holds software in reset state. Then, writing "0" initiates reboot (depending upon configuration, takes up to 10 seconds). This function is equivalent to a power-on reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SOFT RESET	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D	D=DATA BIT

Interrupt Level

Type: unsigned integer
Range: 0 to 7
Read/Write: R
Initialized Value: 0h

This register is used to define the interrupt priority level. Enter 0 to disable interrupts. Enter in priority level 0 through 7 otherwise.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERRUPT LEVEL	X	X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D=DATA BIT

Design Version

The register holds product design version in ASCII. **For example**, design version 1 would be ASCII "1" is in upper byte and ASCII "space" in lower byte, together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
DESIGN VERSION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1 "								ASCII " "								

Customer Defined Register Allocation

Type: binary word
Range: not applicable
Read/Write: W/R
Initialized Value: 0h

Sixteen sequential register locations are allocated for "customer use" and are available for users to write/read data for any appropriate purpose. As an example, the registers may be used in an application where multiple application programs are accessing/controlling multiple serial channels simultaneously. Registers could be used for defining, "coordinating" (keeping track) of multiple program access or status; each application program can write/read to the bank of registers, to define, "set" and/or "determine, which serial ports are currently "in use". Then the application programs selects a defined port that is not being used and updates the register bank contents to let the next application programs know which serial ports are currently being used or are free.

Ethernet Configuration Registers

Applicable: (Port A and/or B); IP Address Hi/Lo (Port A and/or B), IP Submask HI/LO, IP Gateway Hi/Lo, MAC Address Hi/Mid/Lo and IPV6 support.

Type: unsigned integer word
Range: 0000h to FFFFh
Read/Write: R
Initialized Value: not applicable

This register contains the product part number. A unique 16-bit code is assigned to each part number.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PART NUMBER	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Warning: Applies to Dual Ethernet configurations

The second IP address cannot be on the Same Subnet as the First IP Address.

The mother board will not initialize addresses on the second Ethernet port if they are on the same subnet as the first Ethernet port.

Examples:

First Port (A) IP Address	First Port (A) Subnet Mask	Second Port (B) IP Address	Second Port (B) Subnet Mask	Result
192.168.1.5	255.255.255.0	192.168.2.5	255.255.255.0	Good
192.168.1.5	255.255.0.0	192.168.2.5	255.255.0.0	Conflict
192.168.1.5	255.255.0.0	192.168.2.5	255.255.255.0	Conflict
10.0.0.15	255.0.0.0	192.168.1.5	255.255.255.0	Good

ETHERNET

(For detailed supplement, please visit the NAI web-site specific product page and refer to:

NAI Ethernet Interface for Embedded IO Boards Specification

The Ethernet Interface Option allows communications and control access to all function modules either via the system BUS or Ethernet. The Ethernet Interface also provides a Web Server function for card/module functional access (on supported platforms) which provides a GUI (Graphical User Interface) for initial programming of the cards functions prior to writing specific, application dependent, API routines for the card functions. The card will respond to and support TCP/IP or UDP structured protocol(s). Every function that can be accessed via the system BUS can be accessed and commanded via the Ethernet Protocol Commands.

The default IP address: 192.168.4.42
The default subnet: 255.255.255.0
The default gateway: 192.168.4.1

(Note; actual 'as shipped' card Ethernet default IP addresses may vary based upon final ATP configuration(s).) Ethernet Port IP addresses may be field re-flashed to new default programmed addressed via use of the "***IP Configuring for Ethernet Supported Boards***" FLASH software support kit, available/documented from the specific product web page, through the card USB port.

Each physical Ethernet port on the card can support one TCP/IP port as "Port 23" and two UDP ports as "Port 1042 and 1043".

Ethernet Socket Protocol, Version 1

1. This messaging protocol applies only to card products.
2. Messaging is managed by the connected (client) computer. For version 1, the client computer will send a single message and wait for a reply from the card. Multiple cards may be managed from a single computer, subject to channel and computer capacity.
3. Both the message and reply will be in the following format:

Preamble 2 bytes Always 5A0F	Sequence # 2 bytes	Type Code 1 byte	Size 2 bytes	Payload (0..65526 bytes)	Post-amble 2 bytes Always F0A5

4. The Preamble and Postamble are fixed fields, intended to insure that messages are framed correctly. If either is missing the message should be ignored and the receiving device (card or computer) should either seek a new Preamble to re-establish sync, or break and re-establish the connection.
5. The Sequence Number is a field generated by the client computer. Its value is arbitrary, but it is nominally set to an incrementing value. It will be echoed in the reply message. Its purpose is to permit the client computer to transmit multiple messages without waiting for replies, using the sequence number to correlate the replies when they do arrive.
6. The Type Code specifies the purpose of the message, which also defines the content of the payload field.

   The following general rules were used to generate Type Codes:
   - MSB = 0 for write,1 for read (ignored for read or write-only Type Codes)
   - Codes 0x00-0x0f specify system or protocol-level functions
   - Codes 0x10-0x7f specify card communication functions
7. The Size field is the value of the whole framed message including Preamble, Sequence Number, to Post-amble. For example, the register read command: "5A 0F 04 D2 10 00 0C 00 03 BC F0 A5" there are twelve bytes so the length byte is set to 0x0C
8. When using port 23 for a TCP connection, the user can log into and out of the unit a maximum of 1000 times in 40 seconds. Exceeding this limit will cause the board to stop communicating via Ethernet for a time period up to 40 seconds. This limitation exists because every log out causes resources on the unit to linger for 40 seconds to catch any delayed packets (which is required for TCP). For reasons of performance speed, the unit is limited to approximately 1000 lingered sockets.

Type Codes Summary

Type Code	Mnemonic	Function	Comments
0x00	NOP	No operation	Size is zero, board always replies NOP; useful for low-level testing
0x01	LOG	Log in	Must be first message sent after connection is established. Payload is password. Board replies with a LOG message without the password payload, or breaks connection if password is incorrect. A LOG message with a zero payload sent by the client computer while a session in active will disconnect the session.
0x0d	FLSH	Re-flash device	Payload to be determined
0x0e	CINFOw	Communications information write	Reserved for setting communications-related parameters
0x8e	CINFOr	Communications information read	Reserved for retrieving communications-related settings or statistical data
0x0f	NAK	Negative ACK	Sent only by the card, to indicate that a message was received that could not be interpreted. The payload may or may not contain additional information, to be defined.
0x90	REGw (write)	Write to single location	Payload is a 24-bit address field followed by a 16-bit data field. The response is a zero-payload REGw message.[1]
0x10	REGr (read)	Read from single location	Payload is a 24-bit address field. The response is a REGr message with a payload containing a 24-bit address field and a 16-bit data field. [1]
0x91	BANKw (write)	Write to multiple locations	Payload is a 24-bit address field followed by a 16-bit count field and up to 1024 16-bit data fields. The data fields will be written into sequential card locations, beginning at the specified address. The response is a zero-payload BANKw message. [1]
0x11	BANKr (read)	Read from multiple locations	Payload is a 24-bit address field followed by a 16-bit count field. The response is a BANKr message with a payload containing a 24-bit address field followed by an 16-bit count field and up to 4095 16-bit data fields, read from sequential card locations, beginning at the specified address. [1]
0x92	MREGw (write)	Multiple write to a single location	Payload is a 24-bit address field followed by a 16-bit count field and up to 1024 16-bit data fields. The data field values will be repeatedly written into the specified card location. [1]
0x12	MREGr (read)	Multiple read from a single location	Payload is a 24-bit address field followed by a 16-bit count field. The response is a BANKr message with a payload containing a 24-bit address field followed by a 16-bit count field and up to 4095 16-bit data fields, repeatedly read from the specified card location. [1]
(other)	(TBD)	(TBD)	(available for expansion)

Note 1 - For PCI platforms, in order to compute the Ethernet register address, divide the PCI register address by 2. For VME platforms, the Ethernet register address is the same as the VME address.

Error Codes

In the event of an error, the board will send an error message. It will be in the same format as a standard reply with Type Code set to 0x02 and the payload will contain an Error Code.

0x00 – Null event (not usually sent)
0x01 – Malformed message error - (e.g. missing preamble/post-amble)
0x02 – Incoming message buffer overflow – message lost
0x03 – Port in use
0x04 – Value in Payload out of range
0x05 – Size value in Payload (e.g. size of bank read) is incorrect
0x10 – Unknown type code error
0x11 – Address out of range error
0x12 – Address fell on odd boundary (all SYSTEM addresses must end in even numbers)
0x80 – Disconnecting port deliberately

64EP3 CONNECTOR/PIN-OUT INFORMATION

Front and Rear Panel Connectors

Full user I/O is available through the J1-J6 front panel connectors when the card is configured with front panel I/O and through the user-defined rear I/O connectors P2 and P0 (VME64x). (See part number and pin-out information).

General Notes

This platform does NOT support an optional onboard AC reference source

⚠**DO NOT CONNECT TO ANY UNDESIGNATED, (N/C) PINS**

Trigger Input

Type	Front Panel I/O	Rear I/O
TRIG1+	J1-22	Not Avail.
TRIG1-	J1-44	Not Avail.
TRIG2+	J3-22	Not Avail.
TRIG2-	J3-44	Not Avail.

Note: Global trigger input functions are function module dependent

Front Panel System Ground

Front Panel: J1-J6 pin 23
J5, J6 pin 44

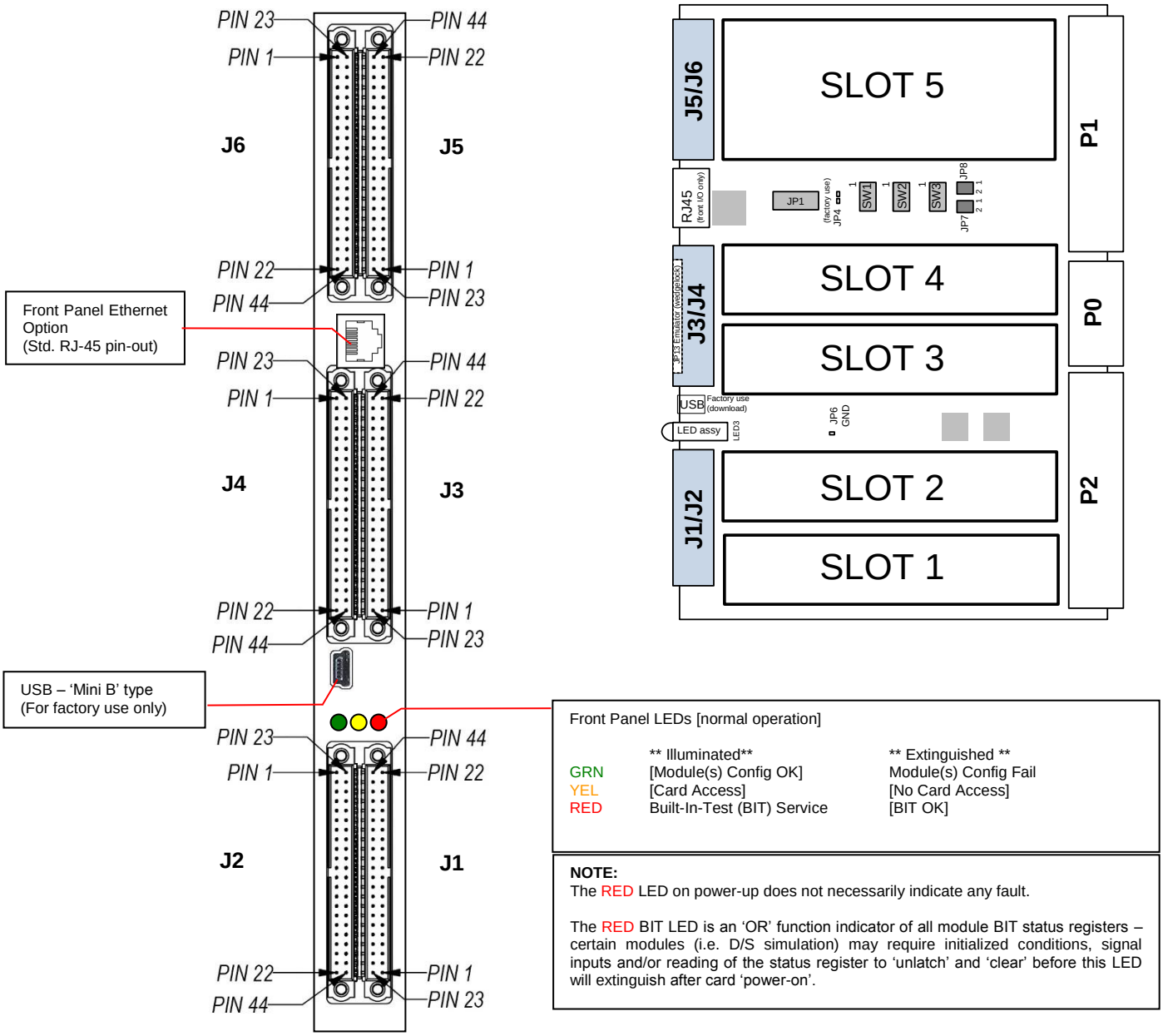
Front Panel Chassis Ground

Front Panel: J1-J6 pin 1
J5-J6 pin 22

Front Panel Connectors J1-J6:

44-pin male connectors, 2mm, Harwin P/N M80-5114422;
Mate kit: Harwin "Custom Hood Kit" part # M80C108448C (or equivalent). Includes connector, backshell, pins & jackscrews. This mating connector kit may be purchased separately under NAI P/N 05-0119 (contact factory).

Front Panel (J1-J6) (Connector Placement and Orientation):



Front Panel LEDs [normal operation]

	** Illuminated**	** Extinguished **
GRN	[Module(s) Config OK]	Module(s) Config Fail
YEL	[Card Access]	[No Card Access]
RED	Built-In-Test (BIT) Service	[BIT OK]

NOTE:
The RED LED on power-up does not necessarily indicate any fault.

The RED BIT LED is an 'OR' function indicator of all module BIT status registers – certain modules (i.e. D/S simulation) may require initialized conditions, signal inputs and/or reading of the status register to 'unlatch' and 'clear' before this LED will extinguish after card 'power-on'.

Slot 1 – Analog I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 1–J1)	Rear I/O P2	A/D (C*)	D/A (F*/J*)	D/A HI-V (J8)	D/A HI-CURR (F5)	RTD (G4)	Strain Gage (G5)	DC Power Supply (V1, V2)
J1-2	25A	IN1+	CH01 H	CH01 H	CH1-H	CH01 EX H	CH01 EX-H	-15V CH1
J1-24	26A	IN1-	CH01 L	CH01 L	CH1-L	CH01 EX L	CH01 EX-L	+15V CH1
J1-3	27A	IN2+	CH02 H		CH1-SNSH	CH01 Sig H	CH01 IN-H	RTN CH1
J1-25	28A	IN2-	CH02 L		CH1-SNSL	CH01 Sig L	CH01 IN-L	
J1-5	29A	IN3+	CH03 H			CH02 EX H	CH01 EX SNS-H	
J1-27	30A	IN3-	CH03 L			CH02 EX L	CH01 EX SNS-L	
J1-7	31A	IN4+	CH04 H	CH02 H	CH2-H	CH02 Sig H	CH02 EX-H	
J1-29	32A	IN4-	CH04 L	CH02 L	CH2-L	CH02 Sig L	CH02 EX-L	
J1-8	25C	IN5+	CH05 H		CH2-SNSH	CH03 EX H	CH02 IN-H	
J1-30	26C	IN5-	CH05 L		CH2-SNSL	CH03 EX L	CH02 IN-L	
J1-10	17D	AGND	N/C			CH03 Sig H	CH02 EX SNS-H	
J1-32	18D					CH03 Sig L	CH02 EX SNS-L	
J1-12	27C	IN6+	CH06 H	CH03 H	CH3-H	CH04 EX H	CH03 EX-H	
J1-34	28C	IN6-	CH06 L	CH03 L	CH3-L	CH04 EX L	CH03 EX-L	
J1-13	29C	IN7+	CH07 H		CH3-SNSH	CH04 Sig H	CH03 IN-H	
J1-35	30C	IN7-	CH07 L		CH3-SNSL	CH04 Sig L	CH03 IN-L	
J1-15	31C	IN8+	CH08 H			CH05 EX H	CH03 EX SNS-H	
J1-37	32C	IN8-	CH08 L			CH05 EX L	CH03 EX SNS-L	
J1-17	8A	IN9+	CH09 H	CH04 H	CH4-H	CH05 Sig H	CH04 EX-H	
J1-39	9A	IN9-	CH09 L	CH04 L	CH4-L	CH05 Sig L	CH04 EX-L	
J1-18	10A	IN10+	CH10 H		CH4-SNSH	CH06 EX H	CH04 IN-H	
J1-40	11A	IN10-	CH10 L		CH4-SNSL	CH06 EX L	CH04 IN-L	RTN CH2
J1-20	19D					CH06 Sig H	CH04 EX SNS-H	+15V CH2
J1-42	20D					CH06 Sig L	CH04 EX SNS-L	-15 CH2
J1-4								
J1-26								
J1-6								
J1-28								
J1-9								
J1-31								
J1-11								
J1-33								
J1-14								
J1-36								
J1-16								
J1-38								
J1-19								
J1-41								
J1-21								
J1-43								
J1-22		TRIGGER(1)+ 1						
J1-44		TRIGGER(1)- 1						

Note 1: [1]TRIG1 and TRIG2 are module function dependent

Slot 1 –Digital I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 1–J1)	Rear I/O P2	Differential (D8)	Discrete & TTL (K6/D7)	Isolated Discrete (K7)	Relay (KN / KL)
J1-2	25A	CH01 H	CH01	CH01-P	CH1-COM
J1-24	26A	CH01 L	CH02	CH01-N	CH1-COM
J1-3	27A	CH02 H	CH03	CH02-P	CH1-COM
J1-25	28A	CH02 L	CH04	CH02-N	CH1-COM
J1-5	29A	CH03 H	Vcc 1-4	CH03-P	CH1-NO
J1-27	30A	CH03 L	Gnd 1-4	CH03-N	CH1-NC
J1-7	31A	CH04 H	CH05	CH04-P	CH2-COM
J1-29	32A	CH04 L	CH06	CH04-N	CH2-COM
J1-8	25C	CH05 H	CH07	CH05-P	CH2-COM
J1-30	26C	CH05 L	CH08	CH05-N	CH2-COM
J1-10	17D	CH06 H	Vcc 5-8	CH06-P	CH2-NO
J1-32	18D	CH06 L	Gnd 5-8	CH06-N	CH2-NC
J1-12	27C	GND	CH09	CH07-P	CH3-COM
J1-34	28C	GND	CH10	CH07-N	CH3-COM
J1-13	29C	CH07 H	CH11	CH08-P	CH3-COM
J1-35	30C	CH07 L	CH12	CH08-N	CH3-COM
J1-15	31C	CH08 H	Vcc 9-12	CH09-P	CH3-NO
J1-37	32C	CH08 L	Gnd 9-12	CH09-N	CH3-NC
J1-17	8A	CH09 H	CH13	CH10-P	CH4-COM
J1-39	9A	CH09 L	CH14	CH10-N	CH4-COM
J1-18	10A	CH10 H	CH15	CH11-P	CH4-COM
J1-40	11A	CH10 L	CH16	CH11-N	CH4-COM
J1-20	19D	CH11 H	Vcc 13-16	CH12-P	CH4-NO
J1-42	20D	CH11 L	Gnd 13-16	CH12-N	CH4-NC
J1-4		CH12 H		CH13-P	
J1-26		CH12 L		CH13-N	
J1-6			Vcc 1-4		
J1-28			Gnd 1-4		
J1-9		CH13 H		CH14-P	
J1-31		CH13 L		CH14-N	
J1-11			Vcc-5-8		
J1-33			Gnd 5-8		
J1-14		CH14 H		CH15-P	
J1-36		CH14 L		CH15-N	
J1-16			Vcc 9-12		
J1-38			Gnd 9-12		
J1-19		CH15 H		CH16-P	
J1-41		CH15 L		CH16-N	
J1-21		CH16 H	Vcc 13-16		
J1-43		CH16 L	Gnd 13-16		
J1-22		TRIGGER(1)+ 1			
J1-44		TRIGGER(1)- 1			

Note 1: [1]TRIG1 and TRIG2 are module function dependent

Slot 1 – Motion Control I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 1–J1)	Rear I/O P2	Encoder (E7)	S/D (S*)	3 CH D/S (6*)	3CH DLV (5*)	LVDT (L*)	Reference (W*)
J1-2	25A	AHI-CH1	CH01 S1	CH01 S1	CH01 A Lo	CH01 A Lo	
J1-24	26A	ALO-CH1	CH01 S3	CH01 S3	CH01 A Hi	CH01 A Hi	
J1-3	27A	BHI-CH1	CH01 S2	CH01 S2	CH01 B Hi	CH01 B Hi	
J1-25	28A	BLO-CH1	CH01 S4	CH01 S4	CH01 B Lo	CH01 B Lo	
J1-5	29A	IDXHI-CH1	CH01 RH	CH01 RH	CH01 RH	CH01 RH	RHI-OUT
J1-27	30A	IDXLO-CH1	CH01 RL	CH01 RL	CH01 RL	CH01 RL	RLO-OUT
J1-7	31A	AHI-CH2	CH02 S1	CH02 S1	CH02 A Lo	CH02 A Lo	
J1-29	32A	ALO-CH2	CH02 S3	CH02 S3	CH02 A Hi	CH02 A Hi	
J1-8	25C	BHI-CH2	CH02 S2	CH02 S2	CH02 B Hi	CH02 B Hi	
J1-30	26C	BLO-CH2	CH02 S4	CH02 S4	CH02 B Lo	CH02 B Lo	
J1-10	17D	IDXHI-CH2	CH02 RH	CH02 RH	CH02 RH	CH02 RH	
J1-32	18D	IDXLO-CH2	CH02 RL	CH02 RL	CH02 RL	CH02 RL	
J1-12	27C	AHI-CH3	CH03 S1			CH03 A Lo	
J1-34	28C	ALO-CH3	CH03 S3			CH03 A Hi	
J1-13	29C	BHI-CH3	CH03 S2			CH03 B Hi	
J1-35	30C	BLO-CH3	CH03 S4			CH03 B Lo	
J1-15	31C	IDXHI-CH3	CH03 RH			CH03 RH	
J1-37	32C	IDXLO-CH3	CH03 RL			CH03 RL	
J1-17	8A	AHI-CH4	CH04 S1	CH03 S1	CH03 A Lo	CH04 A Lo	
J1-39	9A	ALO-CH4	CH04 S3	CH03 S3	CH03 A Hi	CH04 A Hi	
J1-18	10A	BHI-CH4	CH04 S2	CH03 S2	CH03 B Hi	CH04 B Hi	
J1-40	11A	BLO-CH4	CH04 S4	CH03 S4	CH03 B Lo	CH04 B Lo	
J1-20	19D	IDXHI-CH4	CH04 RH	CH03 RH	CH03 RH	CH04 RH	
J1-42	20D	IDXLO-CH4	CH04 RL	CH03 RL	CH03 RL	CH04 RL	
J1-4							
J1-26							
J1-6							
J1-28							
J1-9							
J1-31							
J1-11							
J1-33							
J1-14							
J1-36							
J1-16							
J1-38							
J1-19							
J1-41							
J1-21							
J1-43							
J1-22		TRIGGER(1)+ 1					
J1-44		TRIGGER(1)- 1					

Note 1: [1]TRIG1 and TRIG2 are module function dependent

Slot 1 – Communications I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 1–J1)	Rear I/O P2	ARINC 429/575 (A4)	CANBus (P6, PA)	RS232 (P8)	RS422/485 (P8/PC)	Paired Flow Control (CH1,2 & CH3,4) RS422/485 (P8/PC)	Paired Flow Control (CH1,2 Only) RS422/485 (P8/PC)	Paired Flow Control (CH3,4 Only) RS422/485 (P8/PC)	MIL-STD-1553 (N7, N8)
J1-2	25A	CH1-A	CANH-CH1	CH1 RXD	CH1 RXD-	CH1 RXD-	CH1 RXD-	CH1 RXD-	BUSAP-CH1
J1-24	26A	CH1-B	CANL-CH1		CH1 RXD+	CH1 RXD+	CH1 RXD+	CH1 RXD+	BUSAN-CH1
J1-3	27A			CH1 TXD	CH1 TXD-	CH1 TXD-	CH1 TXD-	CH1 TXD-	BUSBP-CH1
J1-25	28A				CH1 TXD+	CH1 TXD+	CH1 TXD+	CH1 TXD+	BUSBN-CH1
J1-5	29A	CH2-A		CH1 CTS	CH1 CLK+	CH1 CLK+	CH1 CLK+	CH1 CLK+	CH1-RT-ADDR0
J1-27	30A	CH2-B		CH1 RTS	CH1 CLK-	CH1 CLK-	CH1 CLK-	CH1 CLK-	CH1-RT-ADDR1
J1-7	31A		CANH-CH2	CH2 RXD	CH2 RXD-	CH1 CTS-	CH1 CTS-	CH2 RXD-	CH1-RT-ADDR2
J1-29	32A		CANL-CH2		CH2 RXD+	CH1 CTS+	CH1 CTS+	CH2 RXD+	CH1-RT-ADDR3
J1-8	25C	CH3-A		CH2 TXD	CH2 TXD-	CH1 RTS-	CH1 RTS-	CH2 TXD-	CH1-RT-ADDR4
J1-30	26C	CH3-B			CH2 TXD+	CH1 RTS+	CH1 RTS+	CH2 TXD+	CH1-RT-PARITY
J1-10	17D			CH2 CTS	CH2 CLK+	N/C	N/C	CH2 CLK+	CH1-STANDARD
J1-32	18D			CH2 RTS	CH2 CLK-	N/C	N/C	CH2 CLK-	CH1-MODE0
J1-12	27C	CH4-A	CANH-CH3	CH3 RXD	CH3 RXD-	CH3 RXD-	CH3 RXD-	CH3 RXD-	CH2-RT-ADDR0
J1-34	28C	CH4-B	CANL-CH3		CH3 RXD+	CH3 RXD+	CH3 RXD+	CH3 RXD+	CH2-RT-ADDR1
J1-13	29C			CH3 TXD	CH3 TXD-	CH3 TXD-	CH3 TXD-	CH3 TXD-	CH2-RT-ADDR2
J1-35	30C				CH3 TXD+	CH3 TXD+	CH3 TXD+	CH3 TXD+	CH2-RT-ADDR3
J1-15	31C	CH5-A		CH3 CTS	CH3 CLK+	CH3 CLK+	CH3 CLK+	CH3 CLK+	CH2-RT-ADDR4
J1-37	32C	CH5-B		CH3 RTS	CH3 CLK-	CH3 CLK-	CH3 CLK-	CH3 CLK-	CH2-RT-PARITY
J1-17	8A		CANH-CH4	CH4 RXD	CH4 RXD-	CH3 CTS-	CH4 RXD-	CH3 CTS-	CH2-STANDARD
J1-39	9A		CANL-CH4		CH4 RXD+	CH3 CTS+	CH4 RXD+	CH3 CTS+	CH2-MODE0
J1-18	10A	CH6-A		CH4 TXD	CH4 TXD-	CH3 RTS-	CH4 TXD-	CH3 RTS-	BUSAP-CH2
J1-40	11A	CH6-B			CH4 TXD+	CH3 RTS+	CH4 TXD+	CH3 RTS+	BUSAN-CH2
J1-20	19D			CH4 CTS	CH4 CLK+	N/C	CH4 CLK+	N/C	BUSBP-CH2
J1-42	20D			CH4 RTS	CH4 CLK-	N/C	CH4 CLK-	N/C	BUSBN-CH2
J1-4					CH1 CTS+				
J1-26					CH1 CTS-				
J1-6					CH1 RTS+				
J1-28					CH1 RTS-				
J1-9					CH2 CTS+				
J1-31					CH2 CTS-				
J1-11					CH2 RTS+				
J1-33					CH2 RTS-				
J1-14					CH3 CTS+				
J1-36					CH3 CTS-				
J1-16					CH3 RTS+				
J1-38					CH3 RTS-				
J1-19					CH4 CTS+				
J1-41					CH4 CTS-				
J1-21					CH4 RTS+				
J1-43					CH4 RTS-				
J1-22		TRIGGER(1)+ [1]							
J1-44		TRIGGER(1)- [1]							

Note 1: [1]TRIG1 and TRIG2 are module function dependent
N/C indicates “No Connection”

Slot 2 – Analog I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 2 – J2)	Rear I/O P2	A/D (C*)	D/A (F*/J*)	D/A HI-V (J8)	D/A HI-CURR (F5)	RTD (G4)	Strain Gage (G5)	DC Power Supply (V1, V2)
J2-2	12A	IN1+	CH01 H	CH01 H	CH1-H	CH01 EX H	CH01 EX-H	-15V CH1
J2-24	13A	IN1-	CH01 L	CH01 L	CH1-L	CH01 EX L	CH01 EX-L	+15V CH1
J2-3	14A	IN2+	CH02 H		CH1-SNSH	CH01 Sig H	CH01 IN-H	RTN CH1
J2-25	15A	IN2-	CH02 L		CH1-SNSL	CH01 Sig L	CH01 IN-L	
J2-5	16A	IN3+	CH03 H			CH02 EX H	CH01 EX SNS-H	
J2-27	17A	IN3-	CH03 L			CH02 EX L	CH01 EX SNS-L	
J2-7	18A	IN4+	CH04 H	CH02 H	CH2-H	CH02 Sig H	CH02 EX-H	
J2-29	19A	IN4-	CH04 L	CH02 L	CH2-L	CH02 Sig L	CH02 EX-L	
J2-8	20A	IN5+	CH05 H		CH2-SNSH	CH03 EX H	CH02 IN-H	
J2-30	21A	IN5-	CH05 L		CH2-SNSL	CH03 EX L	CH02 IN-L	
J2-10	21D	GND	N/C			CH03 Sig H	CH02 EX SNS-H	
J2-32	22D					CH03 Sig L	CH02 EX SNS-L	
J2-12	23A	IN6+	CH06 H	CH03 H	CH3-H	CH04 EX H	CH03 EX-H	
J2-34	24A	IN6-	CH06 L	CH03 L	CH3-L	CH04 EX L	CH03 EX-L	
J2-13	8C	IN7+	CH07 H		CH3-SNSH	CH04 Sig H	CH03 IN-H	
J2-35	9C	IN7-	CH07 L		CH3-SNSL	CH04 Sig L	CH03 IN-L	
J2-15	10C	IN8+	CH08 H			CH05 EX H	CH03 EX SNS-H	
J2-37	11C	IN8-	CH08 L			CH05 EX L	CH03 EX SNS-L	
J2-17	12C	IN9+	CH09 H	CH04 H	CH4-H	CH05 Sig H	CH04 EX-H	
J2-39	13C	IN9-	CH09 L	CH04 L	CH4-L	CH05 Sig L	CH04 EX-L	
J2-18	14C	IN10+	CH10 H		CH4-SNSH	CH06 EX H	CH04 IN-H	
J2-40	15C	IN10-	CH10 L		CH4-SNSL	CH06 EX L	CH04 IN-L	RTN CH2
J2-20	23D					CH06 Sig H	CH04 EX SNS-H	+15V CH2
J2-42	24D					CH06 Sig L	CH04 EX SNS-L	-15 CH2
J2-4								
J2-26								
J2-6								
J2-28								
J2-9								
J2-31								
J2-11								
J2-33								
J2-14								
J2-36								
J2-16								
J2-38								
J2-19								
J2-41								
J2-21								
J2-43								
J2-22		N/C						
J2-44		N/C						

N/C indicates “No Connection”

Slot 2 –Digital I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 2 – J2)	Rear I/O P2	Diff. (D8)	Discrete2 & TTL (K6/D7)	Isolated Discrete (K7)	Relay (KN / KL)
J2-2	12A	CH01 H	CH01	CH01-P	CH1-COM
J2-24	13A	CH01 L	CH02	CH01-N	CH1-COM
J2-3	14A	CH02 H	CH03	CH02-P	CH1-COM
J2-25	15A	CH02 L	CH04	CH02-N	CH1-COM
J2-5	16A	CH03 H	Vcc 1-4	CH03-P	CH1-NO
J2-27	17A	CH03 L	Gnd 1-4	CH03-N	CH1-NC
J2-7	18A	CH04 H	CH05	CH04-P	CH2-COM
J2-29	19A	CH04 L	CH06	CH04-N	CH2-COM
J2-8	20A	CH05 H	CH07	CH05-P	CH2-COM
J2-30	21A	CH05 L	CH08	CH05-N	CH2-COM
J2-10	21D	CH06 H	Vcc 5-8	CH06-P	CH2-NO
J2-32	22D	CH06 L	Gnd 5-8	CH06-N	CH2-NC
J2-12	23A	GND	CH09	CH07-P	CH3-COM
J2-34	24A	GND	CH10	CH07-N	CH3-COM
J2-13	8C	CH07 H	CH11	CH08-P	CH3-COM
J2-35	9C	CH07 L	CH12	CH08-N	CH3-COM
J2-15	10C	CH08 H	Vcc 9-12	CH09-P	CH3-NO
J2-37	11C	CH08 L	Gnd 9-12	CH09-N	CH3-NC
J2-17	12C	CH09 H	CH13	CH10-P	CH4-COM
J2-39	13C	CH09 L	CH14	CH10-N	CH4-COM
J2-18	14C	CH10 H	CH15	CH11-P	CH4-COM
J2-40	15C	CH10 L	CH16	CH11-N	CH4-COM
J2-20	23D	CH11 H	Vcc 13-16	CH12-P	CH4-NO
J2-42	24D	CH11 L	Gnd 13-16	CH12-N	CH4-NC
J2-4		CH12 H		CH13-P	
J2-26		CH12 L		CH13-N	
J2-6			Vcc 1-4		
J2-28			Gnd 1-4		
J2-9		CH13 H		CH14-P	
J2-31		CH13 L		CH14-N	
J2-11			Vcc-5-8		
J2-33			Gnd 5-8		
J2-14		CH14 H		CH15-P	
J2-36		CH14 L		CH15-N	
J2-16			Vcc 9-12		
J2-38			Gnd 9-12		
J2-19		CH15 H		CH16-P	
J2-41		CH15 L		CH16-N	
J2-21		CH16 H	Vcc 13-16		
J2-43		CH16 L	Gnd 13-16		
J2-22		N/C			
J2-44		N/C			

N/C indicates “No Connection”

Slot 2 – Motion Control I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 2 – J2)	Rear I/O P2	Encoder (E7)	S/D (S*)	3 CH D/S (6*)	3CH DLV (5*)	LVDT (L*)	Reference (W*)
J2-2	12A	AHI-CH1	CH01 S1	CH01 S1	CH01 A Lo	CH01 A Lo	
J2-24	13A	ALO-CH1	CH01 S3	CH01 S3	CH01 A Hi	CH01 A Hi	
J2-3	14A	BHI-CH1	CH01 S2	CH01 S2	CH01 B Hi	CH01 B Hi	
J2-25	15A	BLO-CH1	CH01 S4	CH01 S4	CH01 B Lo	CH01 B Lo	
J2-5	16A	IDXHI-CH1	CH01 RH	CH01 RH	CH01 RH	CH01 RH	RHI-OUT
J2-27	17A	IDXLO-CH1	CH01 RL	CH01 RL	CH01 RL	CH01 RL	RLO-OUT
J2-7	18A	AHI-CH2	CH02 S1	CH02 S1	CH02 A Lo	CH02 A Lo	
J2-29	19A	ALO-CH2	CH02 S3	CH02 S3	CH02 A Hi	CH02 A Hi	
J2-8	20A	BHI-CH2	CH02 S2	CH02 S2	CH02 B Hi	CH02 B Hi	
J2-30	21A	BLO-CH2	CH02 S4	CH02 S4	CH02 B Lo	CH02 B Lo	
J2-10	21D	IDXHI-CH2	CH02 RH	CH02 RH	CH02 RH	CH02 RH	
J2-32	22D	IDXLO-CH2	CH02 RL	CH02 RL	CH02 RL	CH02 RL	
J2-12	23A	AHI-CH3	CH03 S1			CH03 A Lo	
J2-34	24A	ALO-CH3	CH03 S3			CH03 A Hi	
J2-13	8C	BHI-CH3	CH03 S2			CH03 B Hi	
J2-35	9C	BLO-CH3	CH03 S4			CH03 B Lo	
J2-15	10C	IDXHI-CH3	CH03 RH			CH03 RH	
J2-37	11C	IDXLO-CH3	CH03 RL			CH03 RL	
J2-17	12C	AHI-CH4	CH04 S1	CH03 S1	CH03 A Lo	CH04 A Lo	
J2-39	13C	ALO-CH4	CH04 S3	CH03 S3	CH03 A Hi	CH04 A Hi	
J2-18	14C	BHI-CH4	CH04 S2	CH03 S2	CH03 B Hi	CH04 B Hi	
J2-40	15C	BLO-CH4	CH04 S4	CH03 S4	CH03 B Lo	CH04 B Lo	
J2-20	23D	IDXHI-CH4	CH04 RH	CH03 RH	CH03 RH	CH04 RH	
J2-42	24D	IDXLO-CH4	CH04 RL	CH03 RL	CH03 RL	CH04 RL	
J2-4							
J2-26							
J2-6							
J2-28							
J2-9							
J2-31							
J2-11							
J2-33							
J2-14							
J2-36							
J2-16							
J2-38							
J2-19							
J2-41							
J2-21							
J2-43							
J2-22		N/C					
J2-44		N/C					

N/C indicates “No Connection”

Slot 2 – Communications Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 2 – J2)	Rear I/O P2	ARINC 429/575 (A4)	CANBus (P6, PA)	RS232 (P8)	RS422/485 (P8/PC)	Paired Flow Control (CH1,2 & CH3,4) RS422/485 (P8/PC)	Paired Flow Control (CH1,2 Only) RS422/485 (P8/PC)	Paired Flow Control (CH3,4 Only) RS422/485 (P8/PC)	MIL-STD-1553 (N7, N8)
J2-2	12A	CH1-A	CANH-CH1	CH1 RXD	CH1 RXD-	CH1 RXD-	CH1 RXD-	CH1 RXD-	BUSAP-CH1
J2-24	13A	CH1-B	CANL-CH1		CH1 RXD+	CH1 RXD+	CH1 RXD+	CH1 RXD+	BUSAN-CH1
J2-3	14A			CH1 TXD	CH1 TXD-	CH1 TXD-	CH1 TXD-	CH1 TXD-	BUSBP-CH1
J2-25	15A				CH1 TXD+	CH1 TXD+	CH1 TXD+	CH1 TXD+	BUSBN-CH1
J2-5	16A	CH2-A		CH1 CTS	CH1 CLK+	CH1 CLK+	CH1 CLK+	CH1 CLK+	CH1-RT-ADDR0
J2-27	17A	CH2-B		CH1 RTS	CH1 CLK-	CH1 CLK-	CH1 CLK-	CH1 CLK-	CH1-RT-ADDR1
J2-7	18A		CANH-CH2	CH2 RXD	CH2 RXD-	CH1 CTS-	CH1 CTS-	CH2 RXD-	CH1-RT-ADDR2
J2-29	19A		CANL-CH2		CH2 RXD+	CH1 CTS+	CH1 CTS+	CH2 RXD+	CH1-RT-ADDR3
J2-8	20A	CH3-A		CH2 TXD	CH2 TXD-	CH1 RTS-	CH1 RTS-	CH2 TXD-	CH1-RT-ADDR4
J2-30	21A	CH3-B			CH2 TXD+	CH1 RTS+	CH1 RTS+	CH2 TXD+	CH1-RT-PARITY
J2-10	21D			CH2 CTS	CH2 CLK+	N/C	N/C	CH2 CLK+	CH1-STANDARD
J2-32	22D			CH2 RTS	CH2 CLK-	N/C	N/C	CH2 CLK-	CH1-MODE0
J2-12	23A	CH4-A	CANH-CH3	CH3 RXD	CH3 RXD-	CH3 RXD-	CH3 RXD-	CH3 RXD-	CH2-RT-ADDR0
J2-34	24A	CH4-B	CANL-CH3		CH3 RXD+	CH3 RXD+	CH3 RXD+	CH3 RXD+	CH2-RT-ADDR1
J2-13	8C			CH3 TXD	CH3 TXD-	CH3 TXD-	CH3 TXD-	CH3 TXD-	CH2-RT-ADDR2
J2-35	9C				CH3 TXD+	CH3 TXD+	CH3 TXD+	CH3 TXD+	CH2-RT-ADDR3
J2-15	10C	CH5-A		CH3 CTS	CH3 CLK+	CH3 CLK+	CH3 CLK+	CH3 CLK+	CH2-RT-ADDR4
J2-37	11C	CH5-B		CH3 RTS	CH3 CLK-	CH3 CLK-	CH3 CLK-	CH3 CLK-	CH2-RT-PARITY
J2-17	12C		CANH-CH4	CH4 RXD	CH4 RXD-	CH3 CTS-	CH4 RXD-	CH3 CTS-	CH2-STANDARD
J2-39	13C		CANL-CH4		CH4 RXD+	CH3 CTS+	CH4 RXD+	CH3 CTS+	CH2-MODE0
J2-18	14C	CH6-A		CH4 TXD	CH4 TXD-	CH3 RTS-	CH4 TXD-	CH3 RTS-	BUSAP-CH2
J2-40	15C	CH6-B			CH4 TXD+	CH3 RTS+	CH4 TXD+	CH3 RTS+	BUSAN-CH2
J2-20	23D			CH4 CTS	CH4 CLK+	N/C	CH4 CLK+	N/C	BUSBP-CH2
J2-42	24D			CH4 RTS	CH4 CLK-	N/C	CH4 CLK-	N/C	BUSBN-CH2
J2-4					CH1 CTS+				
J2-26					CH1 CTS-				
J2-6					CH1 RTS+				
J2-28					CH1 RTS-				
J2-9					CH2 CTS+				
J2-31					CH2 CTS-				
J2-11					CH2 RTS+				
J2-33					CH2 RTS-				
J2-14					CH3 CTS+				
J2-36					CH3 CTS-				
J2-16					CH3 RTS+				
J2-38					CH3 RTS-				
J2-19					CH4 CTS+				
J2-41					CH4 CTS-				
J2-21					CH4 RTS+				
J2-43					CH4 RTS-				
J2-22		N/C							
J2-44		N/C							

N/C indicates “No Connection”

Slot 3 – Analog I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 3 – J3)	Rear I/O P2	A/D (C*)	D/A (F*)	D/A HI-V (J8)	D/A HI-CURR (F5)	RTD (G4)	Strain Gage (G5)	DC Power Supply (V1, V2)
J3-2	16C	IN1+	CH01 H	CH01 H	CH1-H	CH01 EX H	CH01 EX-H	-15V CH1
J3-24	17C	IN1-	CH01 L	CH01 L	CH1-L	CH01 EX L	CH01 EX-L	+15V CH1
J3-3	18C	IN2+	CH02 H		CH1-SNSH	CH01 Sig H	CH01 IN-H	RTN CH1
J3-25	19C	IN2-	CH02 L		CH1-SNSL	CH01 Sig L	CH01 IN-L	
J3-5	20C	IN3+	CH03 H			CH02 EX H	CH01 EX SNS-H	
J3-27	21C	IN3-	CH03 L			CH02 EX L	CH01 EX SNS-L	
J3-7	23C	IN4+	CH04 H	CH02 H	CH2-H	CH02 Sig H	CH02 EX-H	
J3-29	24C	IN4-	CH04 L	CH02 L	CH2-L	CH02 Sig L	CH02 EX-L	
J3-8	1A	IN5+	CH05 H		CH2-SNSH	CH03 EX H	CH02 IN-H	
J3-30	2A	IN5-	CH05 L		CH2-SNSL	CH03 EX L	CH02 IN-L	
J3-10	25D	GND	N/C			CH03 Sig H	CH02 EX SNS-H	
J3-32	26D					CH03 Sig L	CH02 EX SNS-L	
J3-12	3A	IN6+	CH06 H	CH03 H	CH3-H	CH04 EX H	CH03 EX-H	
J3-34	4A	IN6-	CH06 L	CH03 L	CH3-L	CH04 EX L	CH03 EX-L	
J3-13	5A	IN7+	CH07 H		CH3-SNSH	CH04 Sig H	CH03 IN-H	
J3-35	6A	IN7-	CH07 L		CH3-SNSL	CH04 Sig L	CH03 IN-L	
J3-15	1C	IN8+	CH08 H			CH05 EX H	CH03 EX SNS-H	
J3-37	2C	IN8-	CH08 L			CH05 EX L	CH03 EX SNS-L	
J3-17	3C	IN9+	CH09 H	CH04 H	CH4-H	CH05 Sig H	CH04 EX-H	
J3-39	4C	IN9-	CH09 L	CH04 L	CH4-L	CH05 Sig L	CH04 EX-L	
J3-18	5C	IN10+	CH10 H		CH4-SNSH	CH06 EX H	CH04 IN-H	
J3-40	6C	IN10-	CH10 L		CH4-SNSL	CH06 EX L	CH04 IN-L	RTN CH2
J3-20	27D					CH06 Sig H	CH04 EX SNS-H	+15V CH2
J3-42	28D					CH06 Sig L	CH04 EX SNS-L	-15 CH2
J3-4								
J3-26								
J3-6								
J3-28								
J3-9								
J3-31								
J3-11								
J3-33								
J3-14								
J3-36								
J3-16								
J3-38								
J3-19								
J3-41								
J3-21								
J3-43								
J3-22		TRIGGER2(+)1						
J3-44		TRIGGER2(-)1						

N/C indicates “No Connection”

Slot 3 –Digital I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 3 – J3)	Rear I/O P2	Diff. (D8)	Discrete & TTL (K6/D7)	Isolated Discrete (K7)	Relay (KN / KL)
J3-2	16C	CH01 H	CH01	CH01-P	CH1-COM
J3-24	17C	CH01 L	CH02	CH01-N	CH1-COM
J3-3	18C	CH02 H	CH03	CH02-P	CH1-COM
J3-25	19C	CH02 L	CH04	CH02-N	CH1-COM
J3-5	20C	CH03 H	Vcc 1-4	CH03-P	CH1-NO
J3-27	21C	CH03 L	Gnd 1-4	CH03-N	CH1-NC
J3-7	23C	CH04 H	CH05	CH04-P	CH2-COM
J3-29	24C	CH04 L	CH06	CH04-N	CH2-COM
J3-8	1A	CH05 H	CH07	CH05-P	CH2-COM
J3-30	2A	CH05 L	CH08	CH05-N	CH2-COM
J3-10	25D	CH06 H	Vcc 5-8	CH06-P	CH2-NO
J3-32	26D	CH06 L	Gnd 5-8	CH06-N	CH2-NC
J3-12	3A	GND	CH09	CH07-P	CH3-COM
J3-34	4A	GND	CH10	CH07-N	CH3-COM
J3-13	5A	CH07 H	CH11	CH08-P	CH3-COM
J3-35	6A	CH07 L	CH12	CH08-N	CH3-COM
J3-15	1C	CH08 H	Vcc 9-12	CH09-P	CH3-NO
J3-37	2C	CH08 L	Gnd 9-12	CH09-N	CH3-NC
J3-17	3C	CH09 H	CH13	CH10-P	CH4-COM
J3-39	4C	CH09 L	CH14	CH10-N	CH4-COM
J3-18	5C	CH10 H	CH15	CH11-P	CH4-COM
J3-40	6C	CH10 L	CH16	CH11-N	CH4-COM
J3-20	27D	CH11 H	Vcc 13-16	CH12-P	CH4-NO
J3-42	28D	CH11 L	Gnd 13-16	CH12-N	CH4-NC
J3-4		CH12 H		CH13-P	
J3-26		CH12 L		CH13-N	
J3-6			Vcc 1-4		
J3-28			Gnd 1-4		
J3-9		CH13 H		CH14-P	
J3-31		CH13 L		CH14-N	
J3-11			Vcc-5-8		
J3-33			Gnd 5-8		
J3-14		CH14 H		CH15-P	
J3-36		CH14 L		CH15-N	
J3-16			Vcc 9-12		
J3-38			Gnd 9-12		
J3-19		CH15 H		CH16-P	
J3-41		CH15 L		CH16-N	
J3-21		CH16 H	Vcc 13-16		
J3-43		CH16 L	Gnd 13-16		
J3-22		TRIGGER2(+)1			
J3-44		TRIGGER2(-)1			

N/C indicates “No Connection”

Slot 3 – Motion Control I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 3–J3)	Rear I/O P2	Encoder (E7)	S/D (S*)	3 CH D/S (6*)	3CH DLV (5*)	LVDT (L*)	Reference (W*)
J3-2	16C	AHI-CH1	CH01 S1	CH01 S1	CH01 A Lo	CH01 A Lo	
J3-24	17C	ALO-CH1	CH01 S3	CH01 S3	CH01 A Hi	CH01 A Hi	
J3-3	18C	BHI-CH1	CH01 S2	CH01 S2	CH01 B Hi	CH01 B Hi	
J3-25	19C	BLO-CH1	CH01 S4	CH01 S4	CH01 B Lo	CH01 B Lo	
J3-5	20C	IDXHI-CH1	CH01 RH	CH01 RH	CH01 RH	CH01 RH	RHI-OUT
J3-27	21C	IDXLO-CH1	CH01 RL	CH01 RL	CH01 RL	CH01 RL	RLO-OUT
J3-7	23C	AHI-CH2	CH02 S1	CH02 S1	CH02 A Lo	CH02 A Lo	
J3-29	24C	ALO-CH2	CH02 S3	CH02 S3	CH02 A Hi	CH02 A Hi	
J3-8	1A	BHI-CH2	CH02 S2	CH02 S2	CH02 B Hi	CH02 B Hi	
J3-30	2A	BLO-CH2	CH02 S4	CH02 S4	CH02 B Lo	CH02 B Lo	
J3-10	25D	IDXHI-CH2	CH02 RH	CH02 RH	CH02 RH	CH02 RH	
J3-32	26D	IDXLO-CH2	CH02 RL	CH02 RL	CH02 RL	CH02 RL	
J3-12	3A	AHI-CH3	CH03 S1			CH03 A Lo	
J3-34	4A	ALO-CH3	CH03 S3			CH03 A Hi	
J3-13	5A	BHI-CH3	CH03 S2			CH03 B Hi	
J3-35	6A	BLO-CH3	CH03 S4			CH03 B Lo	
J3-15	1C	IDXHI-CH3	CH03 RH			CH03 RH	
J3-37	2C	IDXLO-CH3	CH03 RL			CH03 RL	
J3-17	3C	AHI-CH4	CH04 S1	CH03 S1	CH03 A Lo	CH04 A Lo	
J3-39	4C	ALO-CH4	CH04 S3	CH03 S3	CH03 A Hi	CH04 A Hi	
J3-18	5C	BHI-CH4	CH04 S2	CH03 S2	CH03 B Hi	CH04 B Hi	
J3-40	6C	BLO-CH4	CH04 S4	CH03 S4	CH03 B Lo	CH04 B Lo	
J3-20	27D	IDXHI-CH4	CH04 RH	CH03 RH	CH03 RH	CH04 RH	
J3-42	28D	IDXLO-CH4	CH04 RL	CH03 RL	CH03 RL	CH04 RL	
J3-4							
J3-26							
J3-6							
J3-28							
J3-9							
J3-31							
J3-11							
J3-33							
J3-14							
J3-36							
J3-16							
J3-38							
J3-19							
J3-41							
J3-21							
J3-43							
J3-22		TRIGGER2(+)1					
J3-44		TRIGGER2(-)1					

N/C indicates “No Connection”

Slot 3 – Communications Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 3 – J3)	Rear I/O P2	ARINC 429/575 (A4)	CANBus (P6)	RS232 (P8)	RS422/485 (P8/PC)	Paired Flow Control (CH1,2 & CH3,4) RS422/485 (P8/PC)	Paired Flow Control (CH1,2 Only) RS422/485 (P8/PC)	Paired Flow Control (CH3,4 Only) RS422/485 (P8/PC)	MIL-STD-1553 (N7, N8)
J3-2	16C	CH1-A	CANH-CH1	CH1 RXD	CH1 RXD-	CH1 RXD-	CH1 RXD-	CH1 RXD-	BUSAP-CH1
J3-24	17C	CH1-B	CANL-CH1		CH1 RXD+	CH1 RXD+	CH1 RXD+	CH1 RXD+	BUSAN-CH1
J3-3	18C			CH1 TXD	CH1 TXD-	CH1 TXD-	CH1 TXD-	CH1 TXD-	BUSBP-CH1
J3-25	19C				CH1 TXD+	CH1 TXD+	CH1 TXD+	CH1 TXD+	BUSBN-CH1
J3-5	20C	CH2-A		CH1 CTS	CH1 CLK+	CH1 CLK+	CH1 CLK+	CH1 CLK+	CH1-RT-ADDR0
J3-27	21C	CH2-B		CH1 RTS	CH1 CLK-	CH1 CLK-	CH1 CLK-	CH1 CLK-	CH1-RT-ADDR1
J3-7	23C		CANH-CH2	CH2 RXD	CH2 RXD-	CH1 CTS-	CH1 CTS-	CH2 RXD-	CH1-RT-ADDR2
J3-29	24C		CANL-CH2		CH2 RXD+	CH1 CTS+	CH1 CTS+	CH2 RXD+	CH1-RT-ADDR3
J3-8	1A	CH3-A		CH2 TXD	CH2 TXD-	CH1 RTS-	CH1 RTS-	CH2 TXD-	CH1-RT-ADDR4
J3-30	2A	CH3-B			CH2 TXD+	CH1 RTS+	CH1 RTS+	CH2 TXD+	CH1-RT-PARITY
J3-10	25D			CH2 CTS	CH2 CLK+	N/C	N/C	CH2 CLK+	CH1-STANDARD
J3-32	26D			CH2 RTS	CH2 CLK-	N/C	N/C	CH2 CLK-	CH1-MODE0
J3-12	3A	CH4-A	CANH-CH3	CH3 RXD	CH3 RXD-	CH3 RXD-	CH3 RXD-	CH3 RXD-	CH2-RT-ADDR0
J3-34	4A	CH4-B	CANL-CH3		CH3 RXD+	CH3 RXD+	CH3 RXD+	CH3 RXD+	CH2-RT-ADDR1
J3-13	5A			CH3 TXD	CH3 TXD-	CH3 TXD-	CH3 TXD-	CH3 TXD-	CH2-RT-ADDR2
J3-35	6A				CH3 TXD+	CH3 TXD+	CH3 TXD+	CH3 TXD+	CH2-RT-ADDR3
J3-15	1C	CH5-A		CH3 CTS	CH3 CLK+	CH3 CLK+	CH3 CLK+	CH3 CLK+	CH2-RT-ADDR4
J3-37	2C	CH5-B		CH3 RTS	CH3 CLK-	CH3 CLK-	CH3 CLK-	CH3 CLK-	CH2-RT-PARITY
J3-17	3C		CANH-CH4	CH4 RXD	CH4 RXD-	CH3 CTS-	CH4 RXD-	CH3 CTS-	CH2-STANDARD
J3-39	4C		CANL-CH4		CH4 RXD+	CH3 CTS+	CH4 RXD+	CH3 CTS+	CH2-MODE0
J3-18	5C	CH6-A		CH4 TXD	CH4 TXD-	CH3 RTS-	CH4 TXD-	CH3 RTS-	BUSAP-CH2
J3-40	6C	CH6-B			CH4 TXD+	CH3 RTS+	CH4 TXD+	CH3 RTS+	BUSAN-CH2
J3-20	27D			CH4 CTS	CH4 CLK+	N/C	CH4 CLK+	N/C	BUSBP-CH2
J3-42	28D			CH4 RTS	CH4 CLK-	N/C	CH4 CLK-	N/C	BUSBN-CH2
J3-4					CH1 CTS+				
J3-26					CH1 CTS-				
J3-6					CH1 RTS+				
J3-28					CH1 RTS-				
J3-9					CH2 CTS+				
J3-31					CH2 CTS-				
J3-11					CH2 RTS+				
J3-33					CH2 RTS-				
J3-14					CH3 CTS+				
J3-36					CH3 CTS-				
J3-16					CH3 RTS+				
J3-38					CH3 RTS-				
J3-19					CH4 CTS+				
J3-41					CH4 CTS-				
J3-21					CH4 RTS+				
J3-43					CH4 RTS-				
J3-22		TRIGGER2(+)1							
J3-44		TRIGGER2(-)1							

N/C indicates “No Connection”

Slot 4 – Analog I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 4 – J4)	Rear I/O P2	A/D (C*)	D/A (F*)	D/A HI-V (J8)	D/A HI-CURR (F5)	RTD (G4)	Strain Gage (G5)	DC Power Supply (V1, V2)
J4-2	7A	IN1+	CH01 H	CH01 H	CH1-H	CH01 EX H	CH01 EX-H	-15V CH1
J4-24	7C	IN1-	CH01 L	CH01 L	CH1-L	CH01 EX L	CH01 EX-L	+15V CH1
J4-3	22A	IN2+	CH02 H		CH1-SNSH	CH01 Sig H	CH01 IN-H	RTN CH1
J4-25	22C	IN2-	CH02 L		CH1-SNSL	CH01 Sig L	CH01 IN-L	
J4-5	1D	IN3+	CH03 H			CH02 EX H	CH01 EX SNS-H	
J4-27	2D	IN3-	CH03 L			CH02 EX L	CH01 EX SNS-L	
J4-7	3D	IN4+	CH04 H	CH02 H	CH2-H	CH02 Sig H	CH02 EX-H	
J4-29	4D	IN4-	CH04 L	CH02 L	CH2-L	CH02 Sig L	CH02 EX-L	
J4-8	5D	IN5+	CH05 H		CH2-SNSH	CH03 EX H	CH02 IN-H	
J4-30	6D	IN5-	CH05 L		CH2-SNSL	CH03 EX L	CH02 IN-L	
J4-10	29D	AGND	N/C			CH03 Sig H	CH02 EX SNS-H	
J4-32	30D					CH03 Sig L	CH02 EX SNS-L	
J4-12	7D	IN6+	CH06 H	CH03 H	CH3-H	CH04 EX H	CH03 EX-H	
J4-34	8D	IN6-	CH06 L	CH03 L	CH3-L	CH04 EX L	CH03 EX-L	
J4-13	9D	IN7+	CH07 H		CH3-SNSH	CH04 Sig H	CH03 IN-H	
J4-35	10D	IN7-	CH07 L		CH3-SNSL	CH04 Sig L	CH03 IN-L	
J4-15	11D	IN8+	CH08 H			CH05 EX H	CH03 EX SNS-H	
J4-37	12D	IN8-	CH08 L			CH05 EX L	CH03 EX SNS-L	
J4-17	13D	IN9+	CH09 H	CH04 H	CH4-H	CH05 Sig H	CH04 EX-H	
J4-39	14D	IN9-	CH09 L	CH04 L	CH4-L	CH05 Sig L	CH04 EX-L	
J4-18	15D	IN10+	CH10 H		CH4-SNSH	CH06 EX H	CH04 IN-H	
J4-40	16D	IN10-	CH10 L		CH4-SNSL	CH06 EX L	CH04 IN-L	RTN CH2
J4-20	29Z					CH06 Sig H	CH04 EX SNS-H	+15V CH2
J4-42	31Z					CH06 Sig L	CH04 EX SNS-L	-15 CH2
J4-4								
J4-26								
J4-6								
J4-28								
J4-9								
J4-31								
J4-11								
J4-33								
J4-14								
J4-36								
J4-16								
J4-38								
J4-19								
J4-41								
J4-21								
J4-43								
J4-22		N/C						
J4-44		N/C						

Note 1: [1]TRIG1 and TRIG2 are module function dependent
Note 2: [2] Discrete I/O Module (K6 only); additional VCC and GND pins are for higher current capability
N/C indicates "No Connection"

Slot 4 –Digital I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 4 – J4)	Rear I/O P2	Diff. (D8)	Discrete2 & TTL (K6/D7)	Isolated Discrete (K7)	Relay (KN / KL)
J4-2	7A	CH01 H	CH01	CH01-P	CH1-COM
J4-24	7C	CH01 L	CH02	CH01-N	CH1-COM
J4-3	22A	CH02 H	CH03	CH02-P	CH1-COM
J4-25	22C	CH02 L	CH04	CH02-N	CH1-COM
J4-5	1D	CH03 H	Vcc 1-4	CH03-P	CH1-NO
J4-27	2D	CH03 L	Gnd 1-4	CH03-N	CH1-NC
J4-7	3D	CH04 H	CH05	CH04-P	CH2-COM
J4-29	4D	CH04 L	CH06	CH04-N	CH2-COM
J4-8	5D	CH05 H	CH07	CH05-P	CH2-COM
J4-30	6D	CH05 L	CH08	CH05-N	CH2-COM
J4-10	29D	CH06 H	Vcc 5-8	CH06-P	CH2-NO
J4-32	30D	CH06 L	Gnd 5-8	CH06-N	CH2-NC
J4-12	7D	GND	CH09	CH07-P	CH3-COM
J4-34	8D	GND	CH10	CH07-N	CH3-COM
J4-13	9D	CH07 H	CH11	CH08-P	CH3-COM
J4-35	10D	CH07 L	CH12	CH08-N	CH3-COM
J4-15	11D	CH08 H	Vcc 9-12	CH09-P	CH3-NO
J4-37	12D	CH08 L	Gnd 9-12	CH09-N	CH3-NC
J4-17	13D	CH09 H	CH13	CH10-P	CH4-COM
J4-39	14D	CH09 L	CH14	CH10-N	CH4-COM
J4-18	15D	CH10 H	CH15	CH11-P	CH4-COM
J4-40	16D	CH10 L	CH16	CH11-N	CH4-COM
J4-20	29Z	CH11 H	Vcc 13-16	CH12-P	CH4-NO
J4-42	31Z	CH11 L	Gnd 13-16	CH12-N	CH4-NC
J4-4		CH12 H		CH13-P	
J4-26		CH12 L		CH13-N	
J4-6			Vcc 1-4		
J4-28			Gnd 1-4		
J4-9		CH13 H		CH14-P	
J4-31		CH13 L		CH14-N	
J4-11			Vcc-5-8		
J4-33			Gnd 5-8		
J4-14		CH14 H		CH15-P	
J4-36		CH14 L		CH15-N	
J4-16			Vcc 9-12		
J4-38			Gnd 9-12		
J4-19		CH15 H		CH16-P	
J4-41		CH15 L		CH16-N	
J4-21		CH16 H	Vcc 13-16		
J4-43		CH16 L	Gnd 13-16		
J4-22		N/C			
J4-44		N/C			

N/C indicates “No Connection”

Slot 4 – Motion Control I/O Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 4 – J4)	Rear I/O P2	Encoder (E7)	S/D (S*)	3 CH D/S (6*)	3CH DLV (5*)	LVDT (L*)	Reference (W*)
J4-2	7A	AHI-CH1	CH01 S1	CH01 S1	CH01 A Lo	CH01 A Lo	
J4-24	7C	ALO-CH1	CH01 S3	CH01 S3	CH01 A Hi	CH01 A Hi	
J4-3	22A	BHI-CH1	CH01 S2	CH01 S2	CH01 B Hi	CH01 B Hi	
J4-25	22C	BLO-CH1	CH01 S4	CH01 S4	CH01 B Lo	CH01 B Lo	
J4-5	1D	IDXHI-CH1	CH01 RH	CH01 RH	CH01 RH	CH01 RH	RHI-OUT
J4-27	2D	IDXLO-CH1	CH01 RL	CH01 RL	CH01 RL	CH01 RL	RLO-OUT
J4-7	3D	AHI-CH2	CH02 S1	CH02 S1	CH02 A Lo	CH02 A Lo	
J4-29	4D	ALO-CH2	CH02 S3	CH02 S3	CH02 A Hi	CH02 A Hi	
J4-8	5D	BHI-CH2	CH02 S2	CH02 S2	CH02 B Hi	CH02 B Hi	
J4-30	6D	BLO-CH2	CH02 S4	CH02 S4	CH02 B Lo	CH02 B Lo	
J4-10	29D	IDXHI-CH2	CH02 RH	CH02 RH	CH02 RH	CH02 RH	
J4-32	30D	IDXLO-CH2	CH02 RL	CH02 RL	CH02 RL	CH02 RL	
J4-12	7D	AHI-CH3	CH03 S1			CH03 A Lo	
J4-34	8D	ALO-CH3	CH03 S3			CH03 A Hi	
J4-13	9D	BHI-CH3	CH03 S2			CH03 B Hi	
J4-35	10D	BLO-CH3	CH03 S4			CH03 B Lo	
J4-15	11D	IDXHI-CH3	CH03 RH			CH03 RH	
J4-37	12D	IDXLO-CH3	CH03 RL			CH03 RL	
J4-17	13D	AHI-CH4	CH04 S1	CH03 S1	CH03 A Lo	CH04 A Lo	
J4-39	14D	ALO-CH4	CH04 S3	CH03 S3	CH03 A Hi	CH04 A Hi	
J4-18	15D	BHI-CH4	CH04 S2	CH03 S2	CH03 B Hi	CH04 B Hi	
J4-40	16D	BLO-CH4	CH04 S4	CH03 S4	CH03 B Lo	CH04 B Lo	
J4-20	29Z	IDXHI-CH4	CH04 RH	CH03 RH	CH03 RH	CH04 RH	
J4-42	31Z	IDXLO-CH4	CH04 RL	CH03 RL	CH03 RL	CH04 RL	
J4-4							
J4-26							
J4-6							
J4-28							
J4-9							
J4-31							
J4-11							
J4-33							
J4-14							
J4-36							
J4-16							
J4-38							
J4-19							
J4-41							
J4-21							
J4-43							
J4-22		N/C					
J4-44		N/C					

N/C indicates “No Connection”

Slot 4 – Communications Modules (User Defined I/O Pin-Outs)

Front I/O (Slot 4 – J4)	Rear I/O P2	ARINC 429/575 (A4)	CANBus (P6)	RS232 (P8)	RS422/485 (P8/PC)	Paired Flow Control (CH1,2 & CH3,4) RS422/485 (P8/PC)	Paired Flow Control (CH1,2 Only) RS422/485 (P8/PC)	Paired Flow Control (CH3,4 Only) RS422/485 (P8/PC)	MIL-STD-1553 (N7, N8)
J4-2	7A	CH1-A	CANH-CH1	CH1 RXD	CH1 RXD-	CH1 RXD-	CH1 RXD-	CH1 RXD-	BUSAP-CH1
J4-24	7C	CH1-B	CANL-CH1		CH1 RXD+	CH1 RXD+	CH1 RXD+	CH1 RXD+	BUSAN-CH1
J4-3	22A			CH1 TXD	CH1 TXD-	CH1 TXD-	CH1 TXD-	CH1 TXD-	BUSBP-CH1
J4-25	22C				CH1 TXD+	CH1 TXD+	CH1 TXD+	CH1 TXD+	BUSBN-CH1
J4-5	1D	CH2-A		CH1 CTS	CH1 CLK+	CH1 CLK+	CH1 CLK+	CH1 CLK+	CH1-RT-ADDR0
J4-27	2D	CH2-B		CH1 RTS	CH1 CLK-	CH1 CLK-	CH1 CLK-	CH1 CLK-	CH1-RT-ADDR1
J4-7	3D		CANH-CH2	CH2 RXD	CH2 RXD-	CH1 CTS-	CH1 CTS-	CH2 RXD-	CH1-RT-ADDR2
J4-29	4D		CANL-CH2		CH2 RXD+	CH1 CTS+	CH1 CTS+	CH2 RXD+	CH1-RT-ADDR3
J4-8	5D	CH3-A		CH2 TXD	CH2 TXD-	CH1 RTS-	CH1 RTS-	CH2 TXD-	CH1-RT-ADDR4
J4-30	6D	CH3-B			CH2 TXD+	CH1 RTS+	CH1 RTS+	CH2 TXD+	CH1-RT-PARITY
J4-10	29D			CH2 CTS	CH2 CLK+	N/C	N/C	CH2 CLK+	CH1-STANDARD
J4-32	30D			CH2 RTS	CH2 CLK-	N/C	N/C	CH2 CLK-	CH1-MODE0
J4-12	7D	CH4-A	CANH-CH3	CH3 RXD	CH3 RXD-	CH3 RXD-	CH3 RXD-	CH3 RXD-	CH2-RT-ADDR0
J4-34	8D	CH4-B	CANL-CH3		CH3 RXD+	CH3 RXD+	CH3 RXD+	CH3 RXD+	CH2-RT-ADDR1
J4-13	9D			CH3 TXD	CH3 TXD-	CH3 TXD-	CH3 TXD-	CH3 TXD-	CH2-RT-ADDR2
J4-35	10D				CH3 TXD+	CH3 TXD+	CH3 TXD+	CH3 TXD+	CH2-RT-ADDR3
J4-15	11D	CH5-A		CH3 CTS	CH3 CLK+	CH3 CLK+	CH3 CLK+	CH3 CLK+	CH2-RT-ADDR4
J4-37	12D	CH5-B		CH3 RTS	CH3 CLK-	CH3 CLK-	CH3 CLK-	CH3 CLK-	CH2-RT-PARITY
J4-17	13D		CANH-CH4	CH4 RXD	CH4 RXD-	CH3 CTS-	CH4 RXD-	CH3 CTS-	CH2-STANDARD
J4-39	14D		CANL-CH4		CH4 RXD+	CH3 CTS+	CH4 RXD+	CH3 CTS+	CH2-MODE0
J4-18	15D	CH6-A		CH4 TXD	CH4 TXD-	CH3 RTS-	CH4 TXD-	CH3 RTS-	BUSAP-CH2
J4-40	16D	CH6-B			CH4 TXD+	CH3 RTS+	CH4 TXD+	CH3 RTS+	BUSAN-CH2
J4-20	29Z			CH4 CTS	CH4 CLK+	N/C	CH4 CLK+	N/C	BUSBP-CH2
J4-42	31Z			CH4 RTS	CH4 CLK-	N/C	CH4 CLK-	N/C	BUSBN-CH2
J4-4					CH1 CTS+				
J4-26					CH1 CTS-				
J4-6					CH1 RTS+				
J4-28					CH1 RTS-				
J4-9					CH2 CTS+				
J4-31					CH2 CTS-				
J4-11					CH2 RTS+				
J4-33					CH2 RTS-				
J4-14					CH3 CTS+				
J4-36					CH3 CTS-				
J4-16					CH3 RTS+				
J4-38					CH3 RTS-				
J4-19					CH4 CTS+				
J4-41					CH4 CTS-				
J4-21					CH4 RTS+				
J4-43					CH4 RTS-				
J4-22		N/C							
J4-44		N/C							

Note 1: [1]TRIG1 and TRIG2 are module function dependent
N/C or 'open' indicates "No Connection"

Slot 5 – Processor Slot I/O Modules (User Defined I/O Pin-Outs)

Rear I/O (P2/P0)	Front I/O (Slot 5 – J5, J6)	U2
P0-A10	J5-12	DIFF-IOHI-CH1
P0-A9	J5-34	DIFF-IOLO-CH1
P0-A12	J5-13	DIFF-IOHI-CH2
P0-A11	J5-35	DIFF-IOLO-CH14
P0-A14	J5-14	DIFF-IOHI-CH3
P0-A13	J5-36	DIFF-IOLO-CH3
P0-A16	J5-15	DIFF-IOHI-CH4
P0-A15	J5-37	DIFF-IOLO-CH4
P0-A18	J5-18	DIFF-IOLO-CH5
P0-A17	J5-40	DIFF-IOHI-CH5
P0-B9	J5-19	DIFF-IOHI-CH6
P0-B8	J5-41	DIFF-IOLO-CH6
P0-B11	J5-20	DIFF-IOHI-CH7
P0-B10	J5-42	DIFF-IOLO-CH7
P0-B13	J5-21	N/C (Default) / DIFF-IOHI-CH8 (option)
P0-B12	J5-43	DIFF-IOLO-CH8
P0-B15	J5-16	DIFF-IOHI-CH9
P0-B14	J5-38	DIFF-IOLO-CH9
P0-B17	J5-17	DIFF-IOHI-CH10
P0-B16	J5-39	DIFF-IOLO-CH10
P0-B19	J6-12	DIFF-IOHI-CH11
P0-B18	J6-34	DIFF-IOLO-CH11
P0-C8	J6-13	USB-DP (Default) / DIFF-IOHI-CH12 (option)
P0-C7	J6-35	USB-PWR (Default) / DIFF-IOLOCH12 (option)
P0-C10	J6-14	USB-GND (Default) / DIFF-IOHI-CH13 (option)
P0-C9	J6-36	USB-DM (Default) / DIFF-IOLO-CH13 (option)
P0-C12	J6-15	SER-TXD (Default) / DIFF-IOHI-CH14 (option)
P0-C11	J6-37	SER-RXD (Default) / DIFF-IOLO-CH2 (option)
P0-C14	J6-18	DIFF-IOLO-CH15
P0-C13	J6-40	SER-GND (Default) / DIFF-IOHI-CH15 (option)
P0-C16	J6-19	DIFF-IOHI-CH16
P0-C15	J6-41	DIFF-IOLO-CH16
P0-C18	J6-20	DIFF-IOHI-CH17
P0-C17	J6-42	DIFF-IOLO-CH17
P0-D9	J6-21	TTL-IO-CH9
P0-D8	J6-43	TTL-IO-CH1
P0-D11	J6-16	DIFF-IOHI-CH19
P0-D10	J6-38	DIFF-IOLO-CH19
P0-D13	J6-17	DIFF-IOHI-CH20
P0-D12	J6-39	DIFF-IOLO-CH20
P0-D15	J5-2	TTL-IO-CH1
P0-D14	J5-24	TTL-IO-CH2
P0-D17	J5-3	TTL-IO-CH11
P0-D16	J5-25	TTL-IO-CH12
P0-D19	J5-4	TTL-IO-CH5
P0-D18	J5-26	TTL-IO-CH6
P0-E8	J5-5	TTL-VCC1
P0-E7	J5-27	GND
P0-E10	J5-8	GND
P0-E9	J5-30	TTL-VCC2
P0-E12	J5-9	DIFF-IOHI-CH18
P0-E11	J5-31	DIFF-IOLO-CH18
P0-E14	J5-10	TTL-IO-CH13
P0-E13	J5-32	TTL-IO-CH14
P0-E16	J5-11	TTL-IO-CH3
P0-E15	J5-33	TTL-IO-CH15
P0-E18	J5-6	TTL-IO-CH7

Rear I/O (P2/P0	Front I/O (Slot 5 – J5, J6)	U3
P0-A10		USB3-DM (not supported – for REF only)
P0-A9		USB3-DP (not supported – for REF only)
P0-A12		USB3-GND (not supported – for REF only)
P0-A11		USB3-PWR (not supported – for REF only)
P0-A14		
P0-A13		
P0-A16		
P0-A15		
P0-A18		
P0-A17		
P0-B9		
P0-B8		
P0-B11		
P0-B10		
P0-B13		SER0-RTS
P0-B12		
P0-B15		
P0-B14		
P0-B17		
P0-B16		
P0-B19		
P0-B18		
P0-C8		USB2-DP
P0-C7		USB2-PWR
P0-C10		USB2-GND
P0-C9		USB2-DM
P0-C12		SER0-TXD
P0-C11		SER0-RXD
P0-C14		
P0-C13		SER0-CTS
P0-C16		
P0-C15		
P0-C18		
P0-C17		
P0-D9		
P0-D8		
P0-D11		
P0-D10		
P0-D13		
P0-D12		
P0-D15		
P0-D14		
P0-D17		
P0-D16		
P0-D19		
P0-D18		
P0-E8		
P0-E7		
P0-E10		
P0-E9		
P0-E12		
P0-E11		
P0-E14		
P0-E13		
P0-E16		
P0-E15		
P0-E18		

Note: Front I/O pins are available for U2 processor module only. No Front I/O for U3 Processor module
N/C or 'open' indicates "No Connection"
U3 USB2 interface support-operation available / USB3 support (not available)
Optional U2 I/O pin assignments (contact factory)

Slot 5 – Processor Slot I/O Modules (User Defined I/O Pin-Outs) (Continued)

Rear I/O (P2/P0)	Front I/O (Slot 5 – J5, J6)	U2
P0-E17	J5-28	TTL-IO-CH8
P0-A8	J5-7	TTL-IO-CH4
P0-E19	J5-29	TTL-IO-CH17
P2-3Z	J6-2	TTL-IO-CH16
P2-1Z	J6-24	RX1
P2-7Z	J6-3	TTL-IO-CH19
P2-5Z	J6-25	TTL-IO-CH20
P2-11Z	J6-4	TTL-IO-CH21
P2-9Z	J6-26	TTL-IO-CH22
P2-15Z	J6-5	TTL-VCC3
P2-13Z	J6-27	GND
P2-19Z	J6-8	TX1
P2-17Z	J6-30	TTL-IO-CH18
P2-23Z	J6-9	SDAIN-CH1
P2-21Z	J6-31	SCLIN-CH1
P2-27Z	J6-10	TX2
P2-25Z	J6-32	RX2
P0-A19	J6-11	SDAIN-CH2
P0-C19	J6-33	SCLIN-CH2
P0-A7	J6-6	TTL-IO-CH23
P0-B7	J6-28	TTL-IO-CH24
P0-D7	J6-7	TX3
P0-C6	J6-29	RX3

Rear I/O (P2/P0)	Front I/O (Slot 5 – J5, J6)	U3
P0-E17		N/C
P0-A8		N/C
P0-E19		N/C
P2-3Z		N/C
P2-1Z		N/C
P2-7Z		N/C
P2-5Z		N/C
P2-11Z		N/C
P2-9Z		N/C
P2-15Z		N/C
P2-13Z		N/C
P2-19Z		N/C
P2-17Z		N/C
P2-23Z		N/C
P2-21Z		N/C
P2-27Z		N/C
P2-25Z		N/C
P0-A19		N/C
P0-C19		N/C
P0-A7		N/C
P0-B7		N/C
P0-D7		N/C
P0-C6		N/C

Note: Front I/O pins are available for U2 processor module only. No Front I/O for U3 Processor module
N/C indicates “No Connection”

Slot 5 – Option I/O Pin-Outs

U2 USB and serial connection may be optioned for USER I/O Signals. Please consult factory.

Rear I/O (P2/P0)	Front I/O (Slot 5 – J5, J6	U2 (Default)	U2 (Factory Option)
P0-B13	J5-21	N/C	DIFF-IOHI-CH8
P0-C8	J6-13	USB-DP	DIFF-IOHI-CH12
P0-C7	J6-35	USB-PWR	DIFF-IOLO-CH12
P0-C10	J6-14	USB-GND	DIFF-IOHI-CH13
P0-C9	J6-36	USB-DM	DIFF-IOLO-CH13
P0-C12	J6-15	SERIAL-TXD	DIFF-IOHI-CH14
P0-C11	J6-37	SERIAL-RXD	DIFF-IOLO-CH2
P0-C13	J6-40	SERIAL-GND	DIFF-IOHI-CH15

Optional U2 I/O pin assignments (contact factory)

Optional U2 JTAG Debug Header Connection

Please consult factory for options when using JTAG emulation with the U2 modules.
Note: Pin-out connections for JP13 and JP14 are identical.

JP13, JP14	Emulator Signal Assignment
1	TMS-IN
2	TCK-IN
3	TDI-IN
4	TDO-OUT
5	TRST-IN
6	EMU-OUT
7	N/C
8	N/C
9	3.3V
10	GND

With conduction-cooled boards, JTAG emulator connector JP13 is available for JTAG debug. JP13 is located in the front center of the 64EP3 board.

For air/ convection cooled boards JP14 is available for JTAG debug. However, front panel connectors J5 and J6 would not available. Default factory option will have JP14 mounted on underside of PC with access recess milled on front panel to allow full access of J5 and J6 I/O – will require additional front panel chassis side access (solder or back side of motherboard PCB) of approximately 0.050".

A JTAG debug emulation cable adapter is available from NAII to adapt wiring from JP13/JP14 connector header to the Analog Devices emulator pod socket header. Order NAII part # 07-0028

Ethernet Connections

Ethernet connections are available via the front panel RJ-45 connector and/or the P0 rear connector – specific Ethernet configuration is governed by Ethernet option selection in part number.

Ethernet (P0 Connector)

P0	Ethernet OPTION
A1	N/C
B1	N/C
C1	N/C
D1	N/C
E1	N/C
A2	ETH1-TP0 +
B2	ETH1-TP0 -
C2	GND
D2	ETH1-TP2 +
E2	ETH1-TP2 -
A3	ETH1-TP1 +
B3	ETH1-TP1 -
C3	GND
D3	ETH1-TP3 +
E3	ETH1-TP3 -
A4	ETH2-TP0+
B4	ETH2-TP0-
C4	GND
D4	ETH2-TP2+
E4	ETH2-TP2-
A5	ETH2-TP1+
B5	ETH2-TP1-
C5	GND
D5	ETH2-TP3+
E5	ETH2-TP3-
A6	N/C
B6	N/C
C6	N/C
D6	N/C
E6	N/C
Z1-Z19	**Ground (shield)**
F1-F19	**Ground (shield)**

Note: N/C indicates “No Connection”

Connector Signal/Pin-Out Notes

NAI Synchro/Resolver Naming Convention

Signal	Resolver	Synchro
S1	SIN(-)	X
S2	COS(+)	Z
S3	SIN(+)	Y
S4	COS(-)	No Connect

Pinout Notes

NOTES:

1. Isolated Discrete Module (K7)	For 'differential' A/D; "P" designation considered 'positive' input pin, "N" pin designation considered 'negative' input pin
2. Discrete I/O Module (K6)	All GND pins are common within the module; however, each pin should be individually wired for optimal power current distribution. I/O Module (K6) **–** VCC input for banks of four channels (i.e. VCC1 indicates VCC input for CH 1-4, VCC2 indicates input for CH 5-8, etc.) All GND pins are common within the module; however, each pin should be individually wired for optimal power current distribution.
3. TTL/DIFF I/O Modules (D7, D8)	I/O levels referenced to system power GND
4. D/A Module (F*/J*)	D/A (not including F5/J8) – All (-) signals are common within the module, isolated from all other modules and system GND.
5. D/A Module (F5)	Sense lines (SNSH/L) should be wired to respective CHx-H/L – connection at load is recommended for higher current applications, otherwise, wire at connector. Channel pairs (1,2 and 3,4) share a common return (L-pin)
6. Power Supply Module (V1, V2)	V1 is single channel (CH1 only); CH2 only available on V2
7. S/D	S4 connection for resolvers only (leave unconnected for synchro)

PART NUMBER DESIGNATION

64EP3 – XX XX XX XX XX X X X -XX

Slot # 1 2 3 4 5

MODULE (SLOT) DEFINITION

Reference the current "Available Function Modules" listing (i.e. Data Sheet/Specifications and/or Operations Manual). Enter Module Designation (i.e.C1) for each slot (1 through 4). Enter 'Z0' if slot is not populated Review the P/N Designation notes in the Operations Manual for valid combinations and application requirements as applied to specific modules/options selections.

MODULE (SLOT) 5 (PROCESSOR) DEFINITION

Enter processor module designation U2 or U3

(**Note:** For non-processor configurations see 64E3 multi-function card)

Module Type	Designation	Channel	Description
Processor	**U2**	--	ADI Blackfin BF533 processor module
Processor	**U3**	--	Freescale PowerPC MPC8536 processor module

MECHANICAL Note 3

F = Front panel and rear P2, P0 I/O
S = Front panel and rear P2 I/O only (No P0)
P = Blank panel with rear P2 & P0 I/O only
G = Blank panel with rear P2 I/O only (No P0)
W = P conduction cooled with wedgelocks
A = VME64 blank front panel with rear P2, P0 I/O only
R = VME64 blank front panel with rear P2 I/O only (No P0)
B = VME64 front panel and rear P2, P0 I/O
T = VME64 front panel and rear P2 I/O only (No P0)
D = VME64 blank front panel, with low profile extractors and rear P2, P0 I/O only

ENVIRONMENTAL

C = 0 TO 70 °C
E = -40 TO +85 °C
H = E with conformal coating
K = C with conformal coating

DUAL ETHERNET (MOTHERBOARD (MB) ONLY)

0 = No Ethernet
1 = MB port A to front panel connection
2 = MB port A to rear P0 connection
3 = MB port A to front and MB port B to P0 connection (2 ports)
4 = MB port A and port B to rear P0 connection (2 ports)

COMBINE W/ SLOT 5 ETHERNET OPTIONS

(Specific w/ module type Ethernet options only (i.e. U3)
A = MB Port A to front and U3 port A to P0
B = U3 Port A to P0 and MB port B to P0
C = U3 Port A to P0 and U3 port B to P0

SPECIAL OPTION CODE (OR LEAVE BLANK)

Part Number Notes

Note 1: Synchro/resolver four channel measurement module selection (field programmable SYN/RSL)
Specify the specific module code relating to the voltage and frequency applicable to the design requirements to assure that the correct parameters are set at the factory. For ranges other than those listed contact factory. There is a +10% tolerance on the upper limit, 0% on the lower limit (i.e. 115V +10%).

Module Code	Input voltage	Reference Voltage	Frequency Band	
SA	2-28 VL-L	2-115 Vrms	50 Hz - 400 Hz	All Input and Reference voltages are auto ranging
SB	2-28 VL-L	2-115 Vrms	400 Hz - 1 KHZ	All Input and Reference voltages are auto ranging
SC	2-28 VL-L	2-115 Vrms	1 KHz - 3 KHZ	All Input and Reference voltages are auto ranging
SD	2-28 VL-L	2-115 Vrms	3 KHz - 5 KHZ	All Input and Reference voltages are auto ranging
SE	2-28 VL-L	2-115 Vrms	5 KHz - 7 KHZ	All Input and Reference voltages are auto ranging
SF	2-28 VL-L	2-115 Vrms	7 KHz - 10 KHZ	All Input and Reference voltages are auto ranging
SG	2-28 VL-L	2-115 Vrms	10 KHz - 20 KHZ	All Input and Reference voltages are auto ranging
SH	90 VL-L	115 Vrms	50Hz - 400 Hz	
SJ	90 VL-L	115 Vrms	400 Hz - 1 KHZ	
SX	x	x	x	Special configurations, contact factory

Note 2:
Slot 1 can have Encoder outputs
Slot 2 can have Encoder outputs, but then slot 6 cannot be populated
Slot 3 cannot be populated with Encoder outputs
Slot 4 can have Encoders; but then no P0 Ethernet
Slot 5 can have Encoders; but then slot 3 cannot be populated and No P0 Ethernet
Slot 6 cannot be populated with Encoder Outputs

Note 3:
P0 connector is required for slots 3 and 6 module I/O for Rear Panel I/O. P0 is NOT required for slots 3 and 6 module I/O if using J1 and J2 Front Panel I/O

Note 4: LVDT/RVDT four channel measurement module selection
Specify the specific module code relating to the voltage and frequency applicable to the design requirements to assure that the correct parameters are set at the factory. For ranges other than those listed contact factory. There is a +10% tolerance on the upper limit, 0% on the lower limit (i.e. 115V +10%).

Module Code	Input Voltage	Reference Voltage	Frequency Band	
LB	2-28 VL-L	2-28 Vrms	400 Hz - 1 KHZ	All Input and Reference voltages are auto ranging
LC	2-28 VL-L	2-28 Vrms	1 KHZ - 3 KHZ	All Input and Reference voltages are auto ranging
LD	2-28 VL-L	2-28 Vrms	3 KHZ - 5 KHZ	All Input and Reference voltages are auto ranging
LE	2-28 VL-L	2-28 Vrms	5 KHZ - 7 KHZ	All Input and Reference voltages are auto ranging
LF	2-28 VL-L	2-28 Vrms	7 KHZ -10 KHZ	All Input and Reference voltages are auto ranging
LG	2-28 VL-L	2-28 Vrms	10 KHZ - 20 KHZ	All Input and Reference voltages are auto ranging
LX	x	x	x	Special configurations, contact factory

Note 5: Contact factory for availability (reserved)

Note 6:

Module Code	Output VL-L	Frequency Band
W1	2-115 Vrms	47 Hz - 10 KHz
W2	2-28 Vrms	47 Hz - 10 KHz
W3	28-115 Vrms	47 Hz - 10 KHz

Note: W1 utilizes a mechanical relay for voltage range switching. May not be suitable for embedded system applications.

Note 7: D(R)/S or LVDT Simulation module selection (Code Table(s) - (following pages))

MODULE CODE TABLES

3 Channel D/S Module Code Table

Code	Format	Output (V_{L-L}) *1 (VRMS)	Ref (V_{REF})*1 (VRMS)	Frequency*1 (Hz)	Max Load (VA)
60	SYN	2 - 11.8	2 – 28	360 – 1K	0.25
61	RSL	2 - 11.8	2 – 28	360 – 1K	0.25
62*	RSL	2 - 28	2 – 28	360 – 1K	0.25
63*	SYN	90	10 – 115	360 – 1K	0.25
64*	RSL	90	10 – 115	360 – 1K	0.25
65	SYN	11.8	2 – 28	47 - 400	0.25
66	RSL	2 - 11.8	2 – 28	47 - 400	0.25
67*	RSL	2 - 28	2 – 28	47 - 400	0.25
68*	SYN	90	10 – 115	47 - 400	0.25
69*	RSL	90	10 – 115	47 - 400	0.25
6A	RSL	2 - 11.8	2 – 28	1K – 3K	0.25
6B	RSL	2 - 11.8	2 – 28	3K – 5K	0.25
6C	RSL	2 - 11.8	2 – 28	5K – 7K	0.25
6D	RSL	2 - 11.8	2 – 28	7K – 10K	0.25
6E*	RSL	2 – 28	2 – 28	1K – 3K	0.25
6F*	RSL	2 – 28	2 – 28	3K – 5K	0.25
6G*	RSL	2 – 28	2 – 28	5K – 7K	0.25
6H*	RSL	2 – 28	2 – 28	7K – 10K	0.25
6J	SYN	2 - 11.8	2 – 28	1K – 3K	0.25
6K	SYN	2 - 11.8	2 – 28	3K – 5K	0.25
6L	SYN	2 - 11.8	2 – 28	5K – 7K	0.25
6M	SYN	2 - 11.8	2 – 28	7K – 10K	0.25
6N*	SYN	2 – 28	2 – 28	1K – 3K	0.25
6P*	SYN	2 – 28	2 – 28	3K – 5K	0.25
6Q*	SYN	2 – 28	2 – 28	5K – 7K	0.25
6R*	SYN	2 – 28	2 – 28	7K – 10K	0.25
6T*	SYN	2 – 11.8	10 – 115	47 - 400	0.25
6U*	SYN	2 – 11.8	10 – 115	360 – 1K	0.25

*Consult factory for availability

*1 There is a +10% tolerance on the range limits

3 Channel DLV Module Code Table

Code	Format	Output (V_{L-L}) (VRMS)	Ref (V_{REF})** (VRMS)	Frequency** (Hz)	Max Load (VA)
5A*	DLV	2 – 28	2-28	360 – 1K	0.1
5B*	DLV	2 – 28	2-28	47 - 400	0.1
5C*	DLV	2 – 28	2-28	1K – 3K	0.1
5D*	DLV	2 – 28	2-28	3K – 5K	0.1
5E*	DLV	2 – 28	2-28	5K – 7K	0.1
5F*	DLV	2 – 28	2-28	7K – 10K	0.1
5G	DLV	2 - 11.8	2-28	360 – 1K	0.1
5H	DLV	2 - 11.8	2-28	47 - 400	0.1
5J	DLV	2 - 11.8	2-28	1K – 3K	0.1
5K	DLV	2 - 11.8	2-28	3K – 5K	0.1
5L	DLV	2 - 11.8	2-28	5K – 7K	0.1
5M	DLV	2 - 11.8	2-28	7K – 10K	0.1

* Consult factory for availability.
** +10% tolerance on the range limits

REVISION PAGE

Revision	Description of Change	Engineer	Date
Preview	64C2; 64EP3; 64E3; 67C3; 68G5; 75C3; 75C5; 75C2; 75SBC4; 78CS2; 64C3; 78C2; 79C3; 75D4; 76C2; 76CS3; NIU1; 64C3; 64CS4; 64DP3:Updates to correct errors and changes in product descriptions	SL	05/08/17
2016-01-30-1712	64C2, VARIOUS:Update Gen 2/Gen3 Digital to Analog Module J8 specifications and description for specification changes and corrections.	AS	01/30/16
2015-11-18-0822	Incorporated the following in the 64C2, 64C3, 64CS4, 64E3, 64EP3, 67C3, 68C3, 75C2, 75C3, 75C5, 76C2, 76CS3, 78C2, 78Cs2, 79C3 and NIU1 Operations manual and specifications: updated D/A (F5) specifications; deleted AC Ref (W6, W7) specification; Added note to "OSC Set Frequency" register; added high power modules back to Available Functions Modules. Updated 67C3 Part Number Designation to correct error on front panel options.	AS	11/18/15
2015-07-14-1008	Delete -40 to +85 degree temperature option from manuals and part number designation datasheets. Affects all G5 and some G3 multifunction I/O and SBC products. Affects non-conformal coated option.	AS	07/14/15
2015-03-24-1613	Change the value of U3 clock speed from 1.25 GHz to 1.0 GHz in datasheet and operation manual.	AS	03/24/15
2014-12-19-0929	Added note to S-D Descriptions for Bandwidth. Select register	AS	12/19/14
2014-08-28-1708	ECO# C02636: 1. 75PPC1 SC1 pinout clarification; 2. 79C3 - added front panel I/O trigger reference designations/details 3. K9 description - pull-up/down "bank" designation correction.; 4. SIU33 HW manual - clarified power dissipation to 75W (max.) (pg. 6, specs/electrical) 5. All GEN2 and higher platforms - added high-word register(s) for accomodating 32-bit serial numbers	AS	08/28/14
2014-03-07-1610	VARIOUS: Document maintenance: 1. 75PPC1 I/O pinouts - front panel I/O pinout MOD2 corrected; From: J3 To: J4. 2. J5, J8 module spec output range clarified (J5 is +/-20V, J8 is +/-80V max ranges) (retro-clarification). 3. KA module spec/BIT availability/operation clarified.; 4. 73SD3 Spec/Manual updated to include BIT logic compatability function register. 5. L(R)VDT simulation modules (2-CH & 3-CH) - clarified phase offset control (removed previous "pending"). 6. Encoder (E7) module clarifications: A) Added "Counter Latch Register" function. B) Clarified "Latch on I" function. C) Clarified "Counter Status Register". 7. L(R)VDT (2-CH&3-CH) modules clarified: updated "Set Offset Phase" function (documented/removed "pending" status). 8. 75SD1 manual/specification update: removed reference of "Save" feature (retro-clarification). 9. Added G3 thermocouple measurerment module to spec, description and register maps - all "GEN3" platforms that support the function. 10. 75C5 - clarified P/N digit for bus master.	AS	03/07/14
2014-01-22-1153	ECO# C02392; Standard documentation maintenance: 1. Added sense line to 75DS2/64CS4 DLV 2-CH module pinouts (where applicable) 2. SIU6 Datasheet - clarified MIL-STD-461F test inclusion compliance 3. 76CS3 optional AC REF P/N clarification (W3 is 28-115 Vrms). 4. CANBus (P6 and PA) memory map inclusion of interrupt	AS	01/22/14

	vector registers 5. 79C3 (GEN3) inclusion of PC module. 6. SIU6 pinout correction: Pg. 21 J2-45 From: A-P2-E10 To: A-P0-E10; J2-66 From: A-P2-E13 To: A-P0-E13; Pg. 22 J3-57 From: A-P0-Z21 To: A-P2-Z21 7. General P8/PC module descriptions: clarified half duplex and extended mode RTS/CTS for front panel I/O (if platform supported) operation(s).; 75DS2 MB spec clarified (no +/-12V required for base MB (modules only). 8. Clarified applicable MFIO P/N designators for W1, W2, W3 frequency range (note to see spec for applicable Vout ranges).		
2013-07-24-1157	ECO C02212; 1. 75C3 - P/N designator - clarification of S/D encoder option configuration constraints. 2. LVDT (L*) VME memory map - add VLL (A+B magnitude) register offset locations. 3. 68RTC3 data sheet - Ethernet pinout referenced corrected to "VPX data plane P1" connector (column header).	AS	07/24/13
2013-07-01-1303	1) D8 (Diff I/O) module spec/memory map clarification - 11 CH w/ 16 CH available on supported platforms. 2) Interrupts w/use of latching registers operation/clarification - all modules w/ supporting functions. 3) NIU1 (data sheet/manual) clarification of mating connectors 4) H2 Ethernet Switch module control register/function additions. 5) K6 PWM function added - Gen3 platforms only. 6) E7 Description (clarifications) to the Multiple Channel Read function. Removed the FPGA resister map from the Interrupt Mapping. Changed and clarified the Interrupt status bits.; 7) DLV (2CH) code table correction. 8) Arinc A4 register naming sync with map. 9) D/S description - remove inferance of 2s complement convention for angle data. 10) 75C5 and 75D4 platforms - initial Agile release (generic volume) Ops Manual/Specifications and datasheet update. 11) H2 module update - description and control mapping. 12) DLV descriptions - clarified "phase lock" definition. 13) P4 ,K9 PCI/VME map update - pending PCI/VME for D6, P5	AS	07/01/13
2013-03-03-1422	ECO C02038; 1: D/S, DLV module code designation: Update AC Reference input voltage range specifications for D/S and D/L stimulus module/channels - LV (2-28 Vrms) REF input range from: 2-115 to: 2-28; HV (29-90 Vrms) REF input range from: 2-115 to: 10-115; added module types (1R, 1T, 3N, 3P, 6T, 6U). 2: K9, K6 module description - clarified principle of operation/block diagram. 3: NIU1 Description - correction to J2 Port 2 Ethernet connection pinouts. 4: Clarified NIU1 specification (base) power (from 5.1W to 3.3W) 5: 75SBC4 - clarified reference 'associated documents' are embedded within the specific BSP. 6: 65CS4 - pg. 12, clarified Input Ref Voltage Sim Command description - removed descriptor "Does not apply when Reference Source is Internal". 7: Added KN, KL relay module(s) specifications/description/register mapping to associated MFIO platforms. 8: Added K7 and V1, V2 module support details. 9: SIU6 HW manual Corrected J3-67 pinout from: A-P0-23Z to: A-P2-23Z (pg. 21). 10: 65CS4 ops manual updated.	AS	03/03/13
2012-12-20-1437	1. 64EP3, 64D3 Ops Manual(s) - clarified pinout(s) for MOD5 U3 and Ethernet keep-out. 2. Clarified 3-CH D/S and DLV module/channel power on command word	LB	12/20/12
2012-11-20-1039	1. NIU1 Operations Manual - Initial Agile release; 2. Gen3 module(s) minor format changes only; 3. 3 CH D/S and D/LV VME register maps updated for correct on-board volt/frequency locations; 4. Clarified D/A FIFO clock rate at 390.625 KHz only (removed 'pending', defined as 'not implemented); 5. E7 description - clarified counter pre-load "low" register; 6. 64EP3/75DP3 - Data sheet and P/N Designation U3 Gig-E rear port A clarification.	LB	11/20/12

2012-08-21-1358	1) 64EP3; Data Sheet / P/N Designation: Redefined/swapped Ethernet option (B) MB and U3 locations. 2) SIU6; HW Manual: Redefined/swapped Ethernet option (4) MB and U3 locations. 3) 76C2 Conn I/O Pinout - no content changes (Agile link only). 4) 67C3 Data Sheet/Spec/Manual: Added mech. option J and K; 67C3/68C3 P/N High Voltage operating warning note (P/N designation). 5) KA module correct/re-define discrete voltage thresholds from 100mV to 10mV lsb. Discrete I/O and A/D signal return references clarified (Description and Conn I/O Pinout sub-docs). 6) "C*" module VME memory map - added missing CH8 FIFO Buffer-Lo Threshold register. 7) P8-PC module description; removed reference to VME specific register reference, Interface Levels (Description sub-doc). 8) 75C3 - Added E7 to P/N Designation subdoc. 9) 44PA1 - Added mechanical options B4, B5. 10) C* module description paragraph restructured.	LB	08/21/12
2012-07-05-1724	1. Clarify MFIO card Ethernet protocol description 2. 64DP3 part number designation expanded for combination U3 and H2 Ethernet port configurations (manual, spec, datasheet) 3. CANBus (P6) module bit rate register programming example added (description section). 4. Corrected minor margin format mis-registrations (module specifications (C*, D7, F/J, K6). 5. RTD (G4) correct typo BIT INT enable register from E0 to E8 (VME, PCI x 2). 6. SIU6 HW manual, correct typo, debug/download mating connector from KMDLX-8P to KMDLAX-8P. 7. Corrected typo 75C3 connector/pin-out section Front Panel BIT LED call-out function.	AS	07/05/12
2012-03-19-1642	1. 64E(P)3 Maintenance Update; a. Module complement; b. GEN3 module support; c. IPV6 support details 2. Clarification on D/S 3CH memory map descriptions, 3. 79C3 MB power clarifications 4. 78C2 mechanical option clarification; E7 module clarification - DIFF/SE interface selection DocBuilder Updates:Multi-platform maintenace: 1. Addition of G4, G5, K7, V1/V2, PC module specification(s), descriptions, register map, pinouts as applicable. 2. Available module split for GEN3 platforms 3. IPV6 support details (where applicable) 3. Part number maintenance 64E3: NEW RELEASE	LB	03/19/12
2012-01-04-1645	Document clarifications:1. 75C3 OpsMans/Specs inclusuion of G5, K7, V1/V2; associated documentation, pinouts - where applicable.2. Clarified available (Aw/E) modules as/where applicable.3. Clarified L* register/descriptions where applicable.4. CANBus P6/PA split/clarifications.5. 79C3 I/O Conn updated for inboard J3 power header6. Clarified KA specification (VCCI/O definition)	LB	01/04/12
2011-11-11-0858	1. G4 Description sub-doc updated/clarified to reference (6) possible range(s).2. D/S 2CHI Specification sub-doc; corrected minor typo (KHz).3. K9 Specification sub-doc; output characteristics clarified - external VCC source required for high-side and push-pull drive capability.	LB	11/11/11
2011-10-24-1305	64C2, 64C3, 78C2:CLERICAL CHANGES, UPDATE FORMATTING OF DOCUMENTS 64EP3: RELEASE NEW PRODUCT 64DP3: RELEASE NEW PRODUCT 64CS4: REFORMATTING OF ALL DOCUMENTS 75C3: REFORMATTING OF ALL DOCUMENTS 75C2: REFORMATTING OF ALL DOCUMENTS 76C2: REFORMATTING OF ALL DOCUMENTS 79C3: REFORMATTING OF ALL DOCUMENTS 67C3: REFORMATTING OF ALL DOCUMENTS	LB	10/24/11

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