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XVME-682

VMEbus PC/AT Processor Module

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Chapter 1

MODULE DESCRIPTION

1.1 INTRODUCTION

The XVME-682 VMEbus PC/AT Processor Module is designed to combine the high-performance and ruggedized packaging of the VMEbus with the broad application software base of the IBM PC/AT standard. The module is fully AT-compatible, capable of running standard PC/AT software.

The XVME-682 is comprised of two VMEbus-compatible, 6U (double-high) cards: the CPU Module and the I/O Module. This unique two-card architecture is discussed later in this chapter.

The XVME-682 comes in four versions depending on the memory desired and the mounting locations of the boards relative to one another. The two memory and configuration options can be selected in any combination. This provides for four versions.

The memory options available on the XVME-682 are either 1 or 4M RAM.

The location option gives the user the ability to mount the CPU and I/O boards together or in non-adjacent VMEbus backplane slots. When together, the shared PC/AT signals are passed between the boards via a xx-pin connector. In the non-adjacent version, the PC/AT signals are routed via the VMEbus P2 backplane.

Table 1-1 below gives the configuration options, and their xycom designation.

Table 1-1 XVME-682 Versions

	RAM		CONNECTOR	
	1M	4M	LOCAL	P2
XVME-682/1	•		•	
XVME-682/2	•			•
XVME-682/3		•	•	
XVME-682/4		•		•

1.3 XVME-682 TWO-CARD ARCHITECTURE

1.3.1 The XVME-682 CPU Module

The XVME-682 CPU Module uses an 80286 microprocessor with software-selected speeds of 10, 8 or 6MHz. Memory is available as either 1 Mbyte or 4 Mbyte dual-ported RAM (with one wait state). Both the VMEbus and PC/AT interfaces reside on this board. Other XVME-682 CPU features include:

- An optional 80287 math co-processor
- Full IBM AT motherboard features
- VMEbus master, slave and interrupt handler interfaces
- A "Real Mode Window" which allows all VMEbus locations to be accessed while the processor is in "real mode"
- Control/Status registers
- Watch Dog Timer
- VMEbus "Slot 1" functions
- Three software-configurable ports (2 serial and 1 parallel)
- IBM PC/AT bus accessibility via VMEbus P2 connector or optional local connector

1.3.2 The XVME-682 I/O Module

The XVME-682 I/O Card provides the interface between the XVME-682 CPU card and the floppy disk, hard disk and graphics controller. Features on the XVME-682 I/O Module include:

- EGA, CGA, MDA, and Hercules graphics support
- 256K of video RAM
- IBM PC/AT-compatible Winchester and floppy disk controller
- Control of up to two Winchester-type hard disk drives
- Control of up to two floppy disk drives

1.3.3 XVME-682 Bus Signal Interfaces

The XVME-682 CPU and I/O boards are united via a local bus. This allows the CPU board to communicate directly with the graphics or disk-controller circuitry without tying up the VMEbus. VMEbus signals are carried by the P1 connector.

The XVME-682 I/O module requires the PC/XT bus for proper operation of its graphics controller circuitry. It also requires the full PC/AT bus for operation of the disk-controller circuitry.

The PC/XT bus is placed on Rows A & C of the VMEbus P2 backplane connector on all versions of the XVME-682. The remainder of the signals required for the PC/AT bus are placed either on the Row B of the VMEbus P2 backplane connector, or on a local connector (P3).

The XVME-682/1 and XVME-682/3 are designed to allow use of a 32-bit processor in the same backplane as the XVME-682. The tables in Appendix C describe the signals assigned for the various options of the XVME-682.

1.5 XVME-682 CPU MODULE OPERATIONAL DESCRIPTION

Figure 1-1 illustrates the functionality of the XVME-682 CPU card. A description of the components is given on the opposite page.

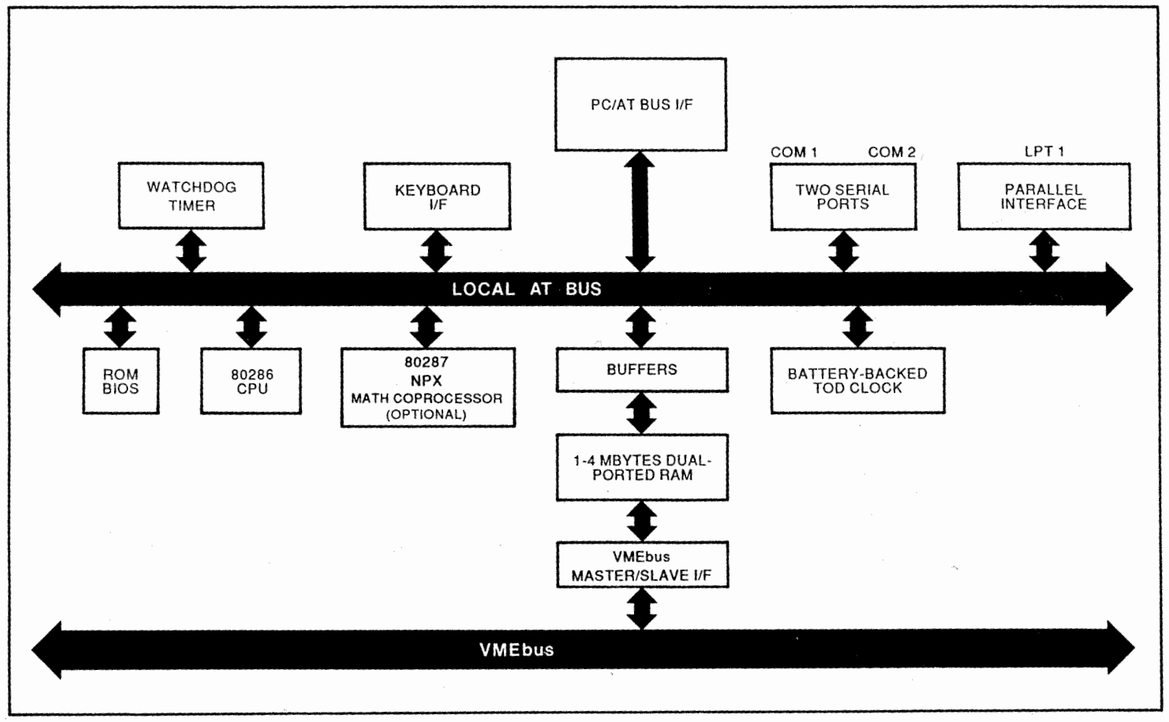


Figure 1-1 XVME-682 CPU Card Block Diagram

1.6 XVME-682 I/O MODULE OPERATIONAL DESCRIPTION

Figure 1-2 illustrates the functionality of the XVME-682 CPU card. A description of the components is given on the opposite page.

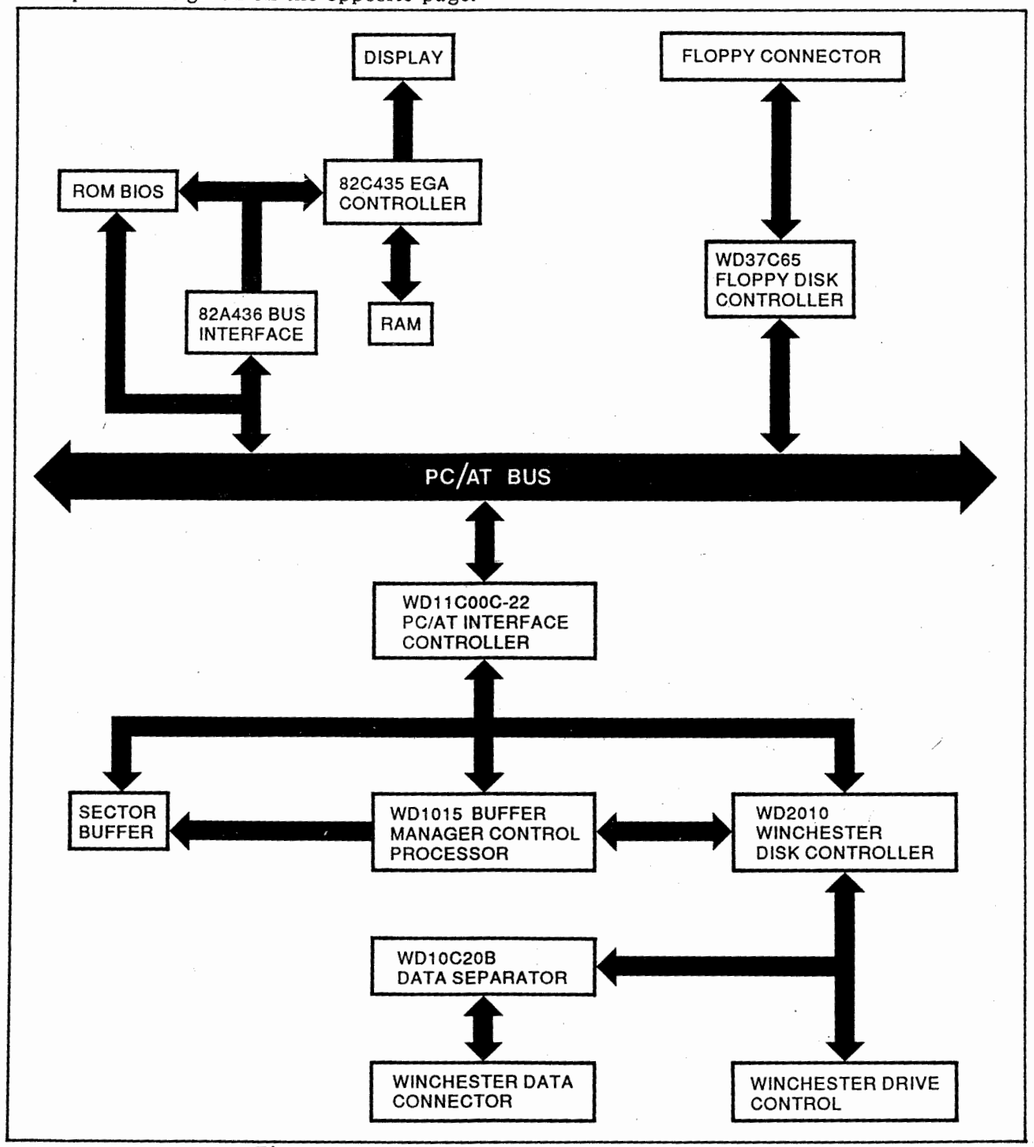


Figure 1-2 XVME-682 I/O Card Block Diagram

1.7 SPECIFICATIONS

Table 1-2 contains the functional specifications for the XVME-682.

Table 1-2 XVME-682 Module Specifications

SPECIFICATION	DESCRIPTION
Mechanical	
Processor	80286
Processor Speed	6, 8, or 10 MHz, software-selected
Math coprocessor (Optional)	80287
Coprocessor Speed	8 MHz
Resident Firmware	CPU Phoenix ROM BIOS PLUS I/O Phoenix EGA BIOS
Graphics Controller	EGA/CGA/MDA Hercules Monochrome
Floppy-disk Interface	SA450
Hard-disk Interface	ST506
On-board Memory	Dual-ported RAM: 1 or 4 MBytes EPROM on CPU module: 128 KBytes (2 sockets) EPROM on I/O module: 64 KBytes (1 socket)
Serial Ports (2)	8250/NS16450 compatible
Parallel Interface	Centronics compatible
Real Time Clock	Motorola 146818A compatible
Environmental	
Temperature	
Operating	0 to 65 C (32 to 149 F)
Non-operating	-40 to 85 C (-40 to 185 F)
Humidity	5 to 95% relative, non-condensing

Chapter 2

XVME-682 CPU MODULE CONFIGURATION

2.1 INTRODUCTION

This chapter provides the information necessary to configure and install the XVME-682 PC/AT CPU Module.

> **NOTE**
> The XVME-682 CPU and I/O modules obtain power from both the VMEbus P1 and P2 backplanes. Both backplanes must be installed for proper operation.

2.2 LOCATIONS OF COMPONENTS RELEVANT TO INSTALLATION

Jumpers and connector locations on the XVME-682 CPU are illustrated in Figure 2-2A for Revision Level A, Figure 2-2B for Revision Level B, and Figure 2-2C for Revision Level C. The board revision level is located on the back side of the module (see Appendix A).

Before modifying the jumpers on the XVME-682 the modules must be separated (see Figure 2-1 for screw locations). If you have an XVME-682/1 or XVME-682/3 (shared PC/AT signals passed through a local connector), remove the four screws and two standoffs holding the boards together and separate them (see Figure 2-1). **DO NOT** bend the circuit cards. The XVME-682/2 and XVME-682/4 boards should not be conncted.

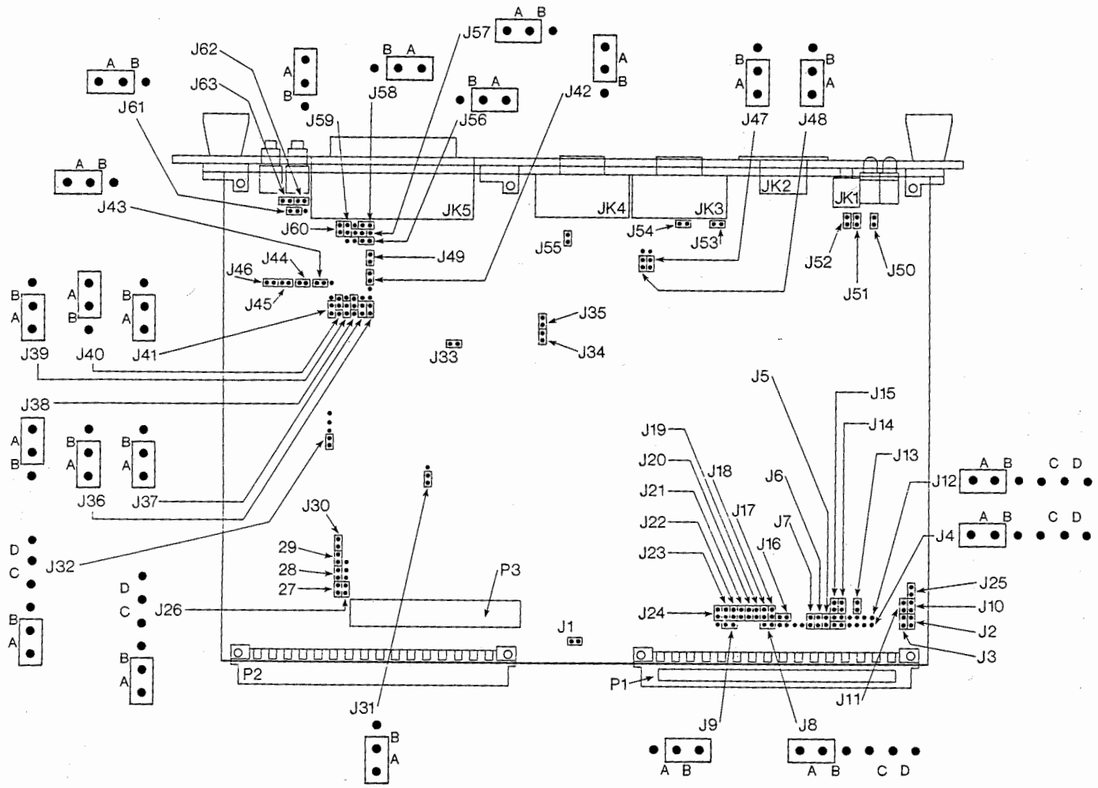


Figure 2-2A XVME-682 CPU Module Jumper and Connector Locations
(Artwork Revision A)

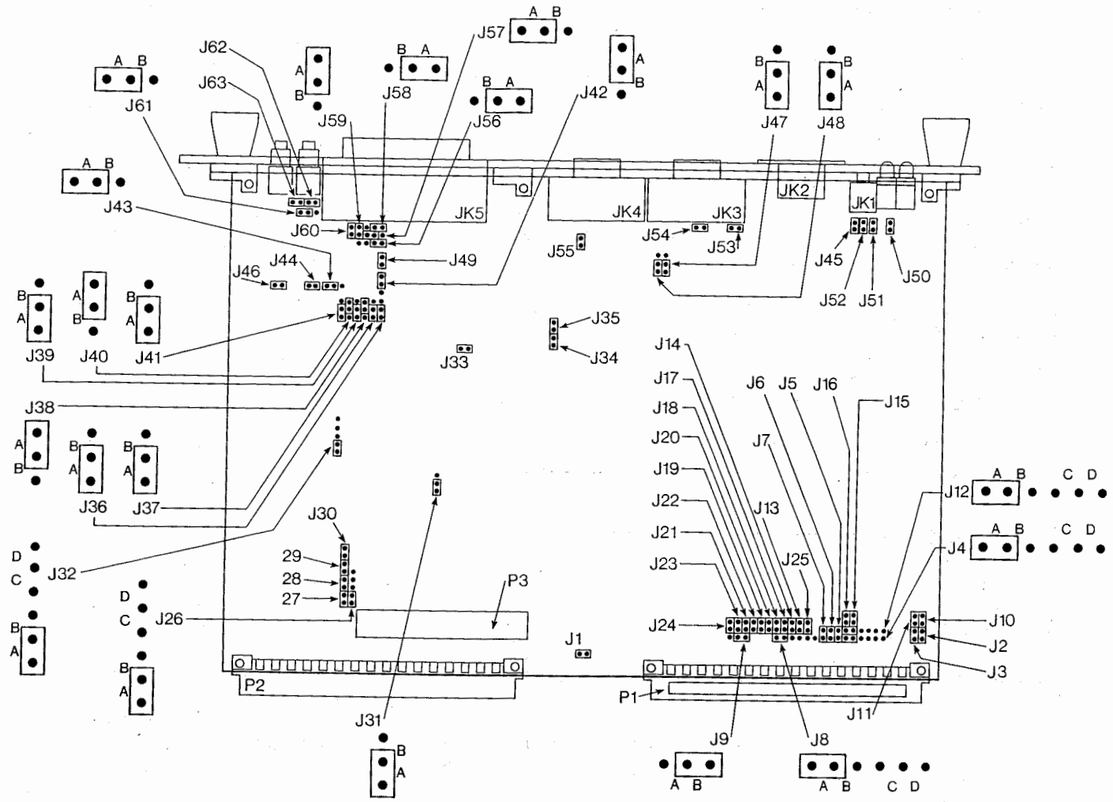


Figure 2-2C XVME-682 CPU Module Jumper and Connector Locations
(Artwork Revision C)

2.3.4 **VMEbus Interrupts** (J17, J18, J19, J21, J22, J23, J24)

The 80286 CPU chip can receive interrupts from all seven VMEbus interrupt levels. Each VMEbus interrupt level has a corresponding jumper to enable or disable its function. When the jumper is IN, the interrupt level is enabled. When the jumper is OUT, the interrupt level is disabled. Table 2-2 lists the seven jumpers corresponding to the seven VMEbus interrupt levels. The default is all except J20 are IN.

Table 2-2 VMEbus Interrupt Jumpers

JUMPER	VMEBUS INT LEVEL
J23	1
J22	2
J21	3
J24	4
J19	5
J18	6
J17	7

2.3.5 **Dual Port Interrupts** (J1)

Other VMEbus masters may interrupt the XVME-682 by reading any one of the lower 16 bytes of the module's dual-port RAM. Jumper J1 is used to enable and disable this type of interrupt. When J1 is IN, the dual-port interrupt is enabled. When the jumper is OUT, the interrupt is disabled. The default is IN.

2.3.6 **Auxiliary Non-Maskable Interrupts (ANMI)** (J50, J51, J52, J62)

Four Auxiliary Non-Maskable Interrupts (ANMI) have been added to the basic IBM AT architecture. They are: the Abort Button, the Watchdog Timer, SYSFAIL, and ACFAIL. Each of the four ANMIs is assigned to a jumper that can be used to permanently disable its function. When the jumper is IN, the ANMI source can generate an interrupt. When the jumper is OUT, the ANMI source may not generate an interrupt.

Table 2-3 lists the ANMIs and their corresponding jumpers. The default is all IN.

Table 2-3 Auxiliary Non-Maskable Interrupt Jumpers

JUMPER	ANMI SOURCE
J62	Abort Button
J51	ACFAIL
J52	SYSFAIL
J50	Watchdog Timer

2.3.9 **VMEbus Master Interface** (J54)

The VMEbus master interface allows the CPU chip to become a master or interrupt handler on the VMEbus. The master interface is invoked whenever the CPU chip has accessed the VMEbus standard address space, the short I/O space, or the IACK address space. VMEbus cycles may be terminated with BERR or DTACK. Jumper J54 is provided to disable the BERR NMI signal generation. When the jumper is IN, the BERR signal will generate an NMI. When it is out, the BERR signal will not generate an NMI. The default is IN.

2.3.10 **EPROM** (J47, J48)

Two jumpers define the type of EPROM at the odd byte location (U34) and the even byte location (U46). They are J47 and J48. Table 2-5 shows how these two jumpers are configured to select the type of EPROM on the XVME-682 CPU module. The default is J47A and J48B (256K EPROMs).

Table 2-5 EPROM Selection Jumpers

JUMPER		EPROM TYPE
J47	J48	
B	B	27512
A	B	27256
A	A	27128
A	A	2764

2.3.11 **VMEbus "Slot 1" Functions** (J5, J6, J9, J15, J34)

The XVME-682 can supply the VMEbus functions associated with Slot 1 (SYSRESET driver, IACK daisy chain driver, single-level arbiter, bus timeout, and SYSCLK driver). These functions are enabled and disabled as a group by jumpers J5, J6, J9, J15 & J34). Table 2-6 illustrates the configurations of these jumpers and their relationships to the Slot 1 functions. The default is all IN, with J9 set to A.

Table 2-6 Slot 1 Jumpers

JUMPER	ENABLED	DISABLED
J6	IN	OUT
J5	IN	OUT
J15	IN	OUT
J9	A	B
J34	IN	OUT

2.3.16 **AT Port Interrupt Levels** (J27, J28, J29, J30)

The 82C605 chip can interrupt the AT architecture on four levels. A jumper is provided for each level to enable and disable the interrupt on that particular level. When the jumper is IN, the interrupt is enabled. When OUT, the interrupt is disabled. Table 2-9 shows the corresponding jumpers and interrupt levels. The default is all IN.

Table 2-9 AT Port Interrupt Level Jumpers

JUMPER	INT LEVEL
J27	IRQ7
J30	IRQ5
J29	IRQ4
J28	IRQ3

2.3.17 **Serial Port Configuration** (J36, J37, J38, J39, J40, J41, J42, J43, J56, J57, J58, J59, J61)

Serial port #1 is RS-232 only (COM1 default configuration). Serial port #2 (COM2 default configuration) can be jumper-configured as either RS-232 or RS-422. Table 2-10 shows how the serial port configuration jumpers must be set for choosing the different port types for serial port #2. The default is RS-232.

> NOTE
> XVME-682 modules with Revision A artwork may only have the COM2 Port configured as RS-232.

Table 2-10 Serial Port Configuration Jumpers

	SETTINGS	
JUMPER	RS-232	RS-422
J36	B	A
J37	B	A
J38	A	B
J39	B	A
J40	A	B
J41	B	A
J42	A	B
J43	B	A
J56	B	A
J57	A	B
J58	B	A
J59	B	A
J61	B	A

2.5 XVME-682 CPU MODULE PINOUT DESCRIPTIONS

The following sections illustrate the signals passed by the ports and connectors on the XVME-682 CPU module.

2.5.1 COM1 and COM2

COM1 is labelled JK4 on the front panel, and COM2 is labelled as JK3. Both are 9 pin D-type connectors. COM1 is a dedicated RS-232 standard port, while COM2 can be configured to use either the RS-232 or RS-422 standards. The factory setting is both to RS-232. The RS-232 and RS-422 pinouts are given below.

Table 2-12 Serial RS-232

PIN	SIGNAL	PIN	SIGNAL
1	CD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	GND		

Table 2-13 Serial RS-422

PIN	SIGNAL	PIN	SIGNAL
1	TXD-	6	RXD-
2	TXD+	7	RXD+
3	RTS-	8	CTS+
4	RTS+	9	CTS-
5	GND		

Some earlier versions of the XVME-682 (Rev. A) can only have COM2 set to RS-232.

Chapter 3

XVME-682 I/O MODULE CONFIGURATION

3.1 INTRODUCTION

This chapter provides the information necessary to configure the XVME-682 I/O Module.

> **NOTE**
> The XVME-682 CPU and I/O modules obtain power from both the VMEbus P1 and P2 backplanes. Both backplanes must be installed for proper operation.

3.2 LOCATIONS OF COMPONENTS RELEVANT TO INSTALLATION

Jumpers, connectors and switch locations on the XVME-682 I/O module are illustrated in Figure 3-1A for Revision Level A, Figure 3-1B for Revision B, and Figure 3-1C for Revision Level C. Default jumper and switch settings are listed in APPENDIX A of this manual.

Before modifying the jumpers on the XVME-682 the modules must be separated (see Figure 2-1 for screw locations). If you have an XVME-682/1 or XVME-682/3 (shared PC/at signals passed through a local connector), remove the four screws and two standoffs holding the boards together and separate them (see Figure 2-1). **DO NOT** bend the circuit cards. The XVME-682/2 and XVME-682/4 boards should not be conncted.

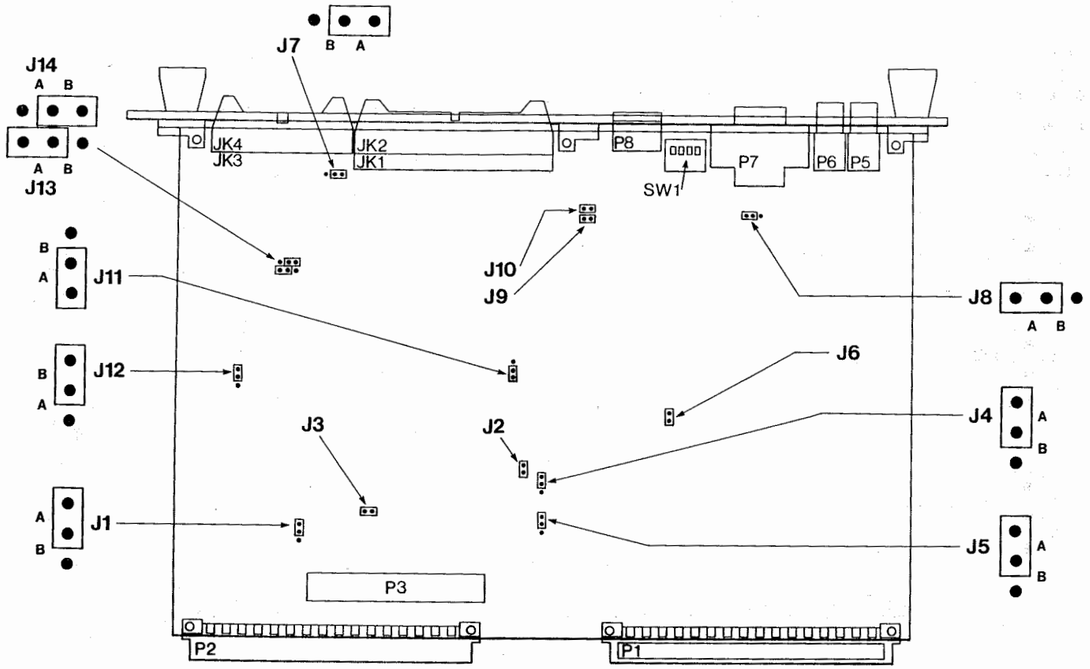


Figure 3-1B XVME-682 I/O Module Jumper, Connector and Switch Locations
(For Revision Level B)

3.3 JUMPERS

Prior to installing the XVME-682 I/O module, several jumper and switch options must be configured. The configurations of the jumpers and switches are dependent upon the module capabilities required for a particular application. Appendix B contains information depicting the default (shipped) configurations for each module version.

3.3.1 Floppy Drive Controller Address

Jumper J1 controls which address range the floppy drive controller will occupy. Setting J1 to A will use the secondary address of 372 to 377H. Setting it to B will use the primary address of 3F2 to 3F7H. PC/AT default is B.

3.3.2 Hard Drive Controller Address

Jumper J2 controls which address range the floppy drive controller will occupy. Setting J1 to A will use the secondary address of 170 to 177H. Setting it to B will use the primary address of 1F0 to 1F7H. PC/AT default is B.

3.3.3 Read Latch

Jumper J3 controls whether ornot the Status Read is latched. If the jumper is IN, the read is latched. The jumper OUT will mean the Status Read is not latched (this option is used with the Compaq 286). The PC/AT default is IN.

3.3.4 Hard Disk Drive

The J4A setting supports a 2-head, 612-cylinder hard-disk drive with standard system setup for 4-head, 306-cylinder drive. The J4B setting ties the firmware sensing bit "high" for hard-disk interface (PC/AT default).

3.3.5 Step Rate

J5A selects a 16 microsec. step rate instead of 35 microsec. step rate, while J5B ties the buffer manager control processor input "high" (PC/AT default).

3.3.6 Monitor Address

Jumnper J6 selects what address range the EGA Controller will use. If J6 is IN, the EGA controller I/O address is set to 2xxH. When OUT, the EGA controller I/O address set to 3xxH The PC/AT default is B.

3.4 MONITOR SELECTION SWITCH

The chipset used as a video controller in the XVME-682 allows for a Primary and Secondary video adapter. Switch 1 on the board controls whether one or two adapters and what type of displays will be used. Table 3-3 shows the various selection options for Switch 1.

Under most conditions, the XVME-682, an EGA-compatible board, will be the only (Primary) adapter. Therefore, one of the first six settings should be selected.

Table 3-2 Monitor Selection Switch Settings
(Switch 1)

SW1	SW2	SW3	SW4	PRIMARY DISPLAY TYPE	SECONDARY DISPLAY TYPE
ON	OFF	OFF	ON	EGA (40x25 res.)	MONO
OFF	OFF	OFF	ON	EGA (80x25 res.)	MONO
ON	ON	ON	OFF	EGA (Emulation Mode)	MONO
OFF	**ON**	**ON**	**OFF**	**EGA (High Res. Mode)**	**MONO**
ON	OFF	ON	OFF	EGA (Mono Mode)	CGA (40x25 res.)
OFF	OFF	ON	OFF	EGA (Mono Mode)	CGA (80x25 res.)
ON	ON	ON	ON	Mono	EGA (40x25)
OFF	ON	ON	ON	Mono	EGA (80x25)
ON	OFF	ON	ON	Mono	EGA (Emulation Mode)
OFF	OFF	ON	ON	Mono	EGA (High Res. Mode)
OFF	ON	ON	ON	CGA (40x25 res.)	EGA (Mono Mode)
OFF	ON	OFF	ON	CGA (80x25)	EGA (Mono Mode)

The default setting is shown in **bold.**

3.5.3 The Feature Connector and Video Jacks

The XVME-682 contains an EGA Feature Connector as part of the module. Table 3-5 describes the pinouts of P4, the 32-pin feature connector.

Table 3-5 Feature Connector

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	N/C
3	N/C	4	J18
5	J19	6	GSOUT
7	RSOUT	8	BSOUT
9	ATRS/L	10	BOUT
11	GOUT	12	G
13	RS	14	B
15	R	16	ROUT
17	FEAT1	18	BLANK
19	FEAT0	20	FC1
21	FC0	22	GS/I
23	BS/V	24	HIN
25	VIN	26	OSC 4Mhz clk)
27	INTERNL*	28	EXT OSC
29	VOUT	30	HOUT
31	GND	32	+5 VDC

There are also two video jacks labelled P5 and P6. These are standard video jacks that are available for use on the XVME-682. Currently, they are not connected to the circuitry on the card itself. The user can design a daughter to connect to the feature connector that would use these two jacks as outputs.

The connector labelled JK1 is the Hard Disk Control Connector. It is a 34-pin header.

Table 3-7 Hard Disk Control Connector

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	HHS3*
3	GND	4	HHS2*
5	GND	6	HWG*
7	GND	8	HSKCMPL*
9	GND	10	HTK000*
11	GND	12	HWFLT*
13	GND	14	HHS0*
15	GND	16	N/C
17	GND	18	HHS1*
19	GND	20	HINDEX*
21	GND	22	HDRDY*
23	GND	24	HSTEP*
25	GND	26	HDS1*
27	GND	28	HDS2*
29	GND	30	N/C
31	GND	32	N/C
33	GND	34	HDIRIN*

The connector labelled JK4 is the Hard Disk #1 Data Control Connector. It is a 20-pin header.

Table 3-8 Hard Disk #1 Data Connector

PIN	SIGNAL	PIN	SIGNAL
1	N/C	2	GND
3	N/C	4	GND
5	N/C	6	GND
7	N/C	8	GND
9	N/C	10	N/C
11	GND	12	GND
13	HWMFM1+	14	HWMFM1-
15	GND	16	GND
17	HRMFM1+	18	HRMFM1-
19	GND	20	GND

3.6 PC/AT INTERFACE CONNECTOR P2/P3

The XVME-682 is made in odd-numbered versions (XVME-682/1 & XVME-682/3) and even-numbered versions (XVME-682/2 & XVME-682/4). The even-numbered versions of the module cannot operate with a 32-bit processor sharing the same VMEbus backplane.

This is due to the fact that Row B of the VMEbus P2 connector is bussed to all cards on the backplane. Because the even-numbered XVME-682 versions use the P2 connector to send AT signals, they cannot share Row B with a 32-bit processor elsewhere on the backplane.

On all versions, the XT signals travel on the user-defined I/O pins on Rows A & C of the VMEbus P2 connector.

The pinouts for the XVME-682/2 & XVME-682/4 P2 connectors are as follows:

Table 3-10 PC/AT Interface Connector P2
(XVME-682/2 & XVME-682/4 Only)

PIN #	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
1	I/OCHCK	+5V	N/C
2	SD7	GND	IRQ9
3	SD6	MEMW*	DRQ2
4	SD5	SD8	N/C
5	SD4	SD9	SMEMW*
6	SD3	SD10	SMEMR*
7	SD2	SD11	IOW*
8	SD1	SD12	IOR*
9	SD0	SD13	DACK3*
10	IOCHRDY	SD14	DRQ3
11	AEN	SD15	DACK1*
12	SA19	GND	DRQ1
13	SA18	+5V	REFRESH*
14	SA17	MEMCS16*	CLK
15	SA16	IOCS16*	IRQ7
16	SA15	IRQ10	IRQ6
17	SA14	IRQ11	IRQ5
18	SA13	IRQ12	IRQ4
19	SA12	IRQ15	IRQ3
20	SA11	IRQ14	DACK2*

Table 3-11 PC/AT Interface Connector P2
(XVME-682/1 & XVME-682/3 Only)

PIN #	ROW A SIGNAL	ROW B SIGNAL	ROW C SIGNAL
1	I/O CHCK	+5V	N/C
2	SD7	GND	IRQ9
3	SD6	N/C	DRQ2
4	SD5	N/C	N/C
5	SD4	N/C	SMEMW*
6	SD3	N/C	SMEMR*
7	SD2	N/C	IOW*
8	SD1	N/C	IOR*
9	SD0	N/C	DACK3*
10	IOCHRDY	N/C	DRQ3
11	AEN	N/C	DACK1*
12	SA19	GND	DRQ1
13	SA18	+5V	REFRESH*
14	SA17	N/C	CLK
15	SA16	N/C	IRQ7
16	SA15	N/C	IRQ6
17	SA14	N/C	IRQ5
18	SA13	N/C	IRQ4
19	SA12	N/C	IRQ3
20	SA11	N/C	DACK2*
21	SA10	N/C	T/C
22	SA9	GND	BALE
23	SA8	N/C	OSC
24	SA7	N/C	SBHE
25	SA6	N/C	LA23
26	SA5	N/C	LA22
27	SA4	N/C	LA21
28	SA3	N/C	LA20
29	SA2	N/C	LA19
30	SA1	N/C	LA18
31	SA0	GND	LA17
32	GND	+5V	MEMR*

Chapter 4

INSTALLATION

4.1 INTRODUCTION

This chapter provides the information necessary to install the XVME-682 PC/AT Processor Module into the VMEbus backplane.

Xycom modules are designed to comply with all physical and electrical VMEbus backplane specifications. The XVME-682 is a double-high, two-board VMEbus module. As such, it requires two slots and both the P1 and P2 connections.

Prior to installing a module, you should determine and verify all relevant jumper configurations, and all connections to external devices or power supplies. Jumper configuration information for the CPU and I/O boards can be found in Chapters 2 and 3 respectively.

4.2 INSTALLATION

> **WARNING**
> Never attempt to install or remove any boards before turning off the power to the bus, and all related external power supplies.

1. Turn power to the VMEbus cardcage to **OFF** and disconnect the power cable.

2. Configure both the CPU and I/O cards for the particular application. All information on this is in Chapters 2 and 3.

> **CAUTION**
> DO NOT use excessive force or pressure to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide slots for possible damage or obstructions.

3. Install the XVME-682 into the cardcage by centering the board(s) on the plastic guides in the slots and pushing the cards slowly toward the rear of the chassis until the connectors engage (the cards should slide freely in the plastic guides).

4. Secure the board(s) to the chassis by tightening the two machine screws at the top and bottom of each board.

5. Attach the short ribbon cable provided to the rear of the VMEbus P2 backplane, connecting the slot containing the CPU module with the slot containing the I/O module.

6. Connect the disk drives to the front of the I/O module, in accordance with the Figure 4-2.

> **NOTE**
> Use Hard Drive Data 0 (JK4) when only one hard disk is used.

7. Connect all remaining peripherals (i.e., monitor, keyboard, printer, serial devices, or light pen) by inserting the each interface cable into the appropriate connector on the front of the I/O or CPU module. Use Figure 4-3 as a guide.

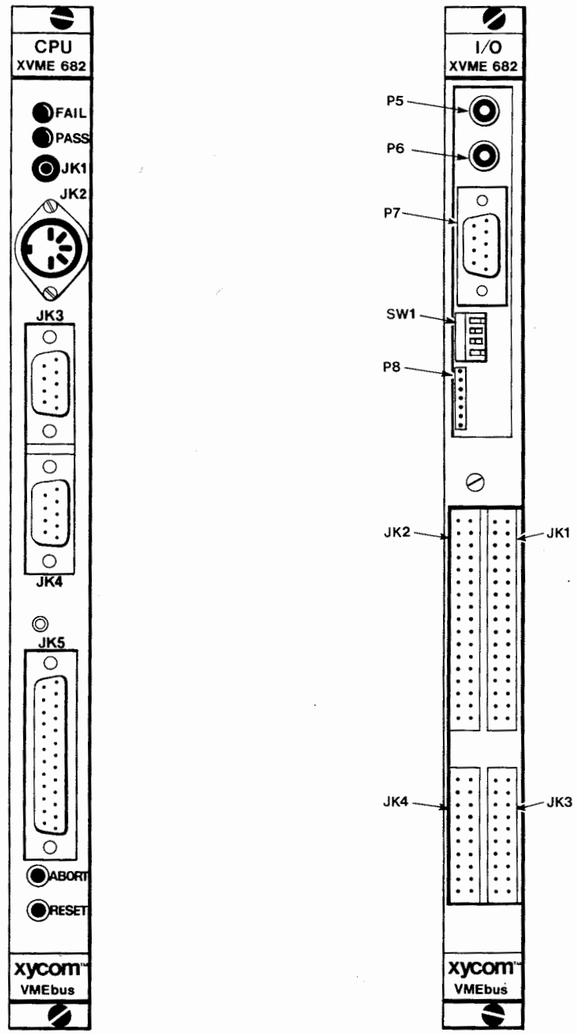


Figure 4-3 XVME-682 Front Panel

Assuming the steps in the previous sections of this chapter have been followed, the power to the VMEbus cardcage can now be turned to **ON**.

Chapter 5

XYCOM INDUSTRIAL COMPUTER BIOS

5.1 INTRODUCTION

The XVME-682 uses a complete Industrialized BIOS computer package which consists of three products from Phoenix Technologies. These products are the:

- Phoenix 80286 ROM BIOS PLUS
- Phoenix EGA BIOS
- Phoenix Utilities for 80286 ROM BIOS PLUS

5.2 CPU ROM BIOS PLUS

Two EPROMS on the XVME-682 contain the ROM BIOS PLUS firmware which controls many of the basic functions of the XVME-682 including disk I/O, serial and parallel ports, keyboard control, and power-up diagnostics. The ROM BIOS PLUS also contains a resident SETUP facility which is used for placing default system parameters in CMOS RAM.

The AT-compatible ROM BIOS PLUS supports all devices that IBM's BIOS supports as well as the following devices:

- 101/102-key keyboard
- 84-key keyboard
- System without keyboard
- 3.5 inch diskette drives (720 Kb and 1.44 Mb)
- 47 hard disk types

5.2.3 Hard Disk Drives Supported

Currently, 47 hard disk drive types can be selected for AT-Compatible systems. These hard disk selections are defined in Table 5-2.

> **NOTE**
> Prior to purchasing any of the drives in Table 2-2 it should be verified that it does contain an ST-506 interface provided for on the XVME-682 I/O Module.

Table 5-2 Hard Disk Drives Supported

#	DRIVE TYPE	CYLINDERS	HEADS	WRITE PRECOMP	LANDING ZONE	SECTORS
1	IBM 5.25" 10MB	306	4	128	305	17
2	IBM 5.25" 20MB Seagate ST-225 CDC Wren II 9415-5-25* Miniscribe 8438F	615	4	300	615 615	17
3	IBM 5.25" 30MB	615	6	300	615	17
4	IBM 5.25" 62MB	940	8	512	940	17
5	IBM 5.25" 46Mb	940	6	512	940	17
6	IBM 5.25" 20Mb Miniscribe MS 8425 Seagate ST4026** Tandon TM 262** Tandon TM 702AT**	615	4	-1	615	17
7	IBM 5.25" 30Mb	462	8	256	511	17
8	IBM 5.25" 30Mb	733	5	-1	733	17
9	IBM 5.25" 112Mb	900	15	-1	901	17
10	IBM 5.25" 20Mb	820	3	-1	820	17
11	IBM 5.25" 35Mb	855	5	-1	855	17
12	IBM 5.25" 49Mb	855	7	-1	855	17
13	IBM 5.25" 20Mb	306	8	128	319	17
14	IBM 5.25" 42Mb	733	7	-1	733	17
15	Available					
16	IBM 5.25" 20Mb	612	4	0	633	17
17	IBM 5.25" 40Mb	977	5	300	977	17
18	IBM 5.25" 56Mb	977	7	-1	977	17
19	IBM 5.25" 59Mb	1024	7	512	1023	17
20	IBM 5.25" 30Mb	733	5	300	732	17
21	IBM 5.25" 42Mb	733	7	300	732	17
22	IBM 5.25" 30Mb		5	300	733	17

5.3 ROM RESIDENT SETUP ROUTINE

SETUP is a program which resides in the ROM BIOS Plus EPROMS on the XVME-682 CPU module. It is used to write configuration information into battery-backed memory.

SETUP stores the following information in CMOS:

- Date and Time
- Diskette and Hard disk types
- Keyboard options (installed or not installed)
- Monitor type
- Processor speed
- Math coprocessor option (not accessible)
- Base memory size
- Extended memory size

5.3.1 When to Use SETUP

SETUP must be run by the user when:

- installing the system for the first time
- changing drives or monitor type
- changing system features (i.e. CPU speed)
- replacing the battery

5.3.2 Invoking the SETUP Routine

To invoke the ROM resident SETUP routine on the XVME-682 simply depress the "CTRL", "ALT", and "S" keys simultaneously on a PC/AT keyboard.

You may scroll through the available SETUP options by using the up-arrow and down-arrow keys on the PC/AT keyboard. Selections can be modified by manip-ulating the right-arrow and left-arrow keys. Memory size parameters are entered via the number keypad.

Chapter 6

PROGRAMMING

6.1 INTRODUCTION

The XVME-682 is fully PC/AT compatible. This means that it will run a wide range of standard software designed for the IBM PC/AT standard. Because the XVME-682 is designed to meet both the PC/AT and VMEbus standards, its programming capabilities exceed that of either a typical PC/AT or VMEbus processor.

This chapter provides information required to program the XVME-682 module. The presentation of this information will be as follows:

- Module memory map (as seen by the 80286 CPU)
- I/O port addresses, registers and descriptions
- Use of the VME master interface
- Use of the VME slave interface
- Interrupts

6.2 XVME-682 MODULE MEMORY MAP

Figures 6-1 and 6-2 show the XVME-682 Module memory maps as they would appear to the 80286 processor.

The XVME-682 dual-access memory appears as a contiguous 1 Mbyte (XVME-682/1/2) or 4 Mbyte (XVME-682/3/4) block to other processors residing on the VMEbus. Refer to section 2.4.9 for setting the address of dual access memory.

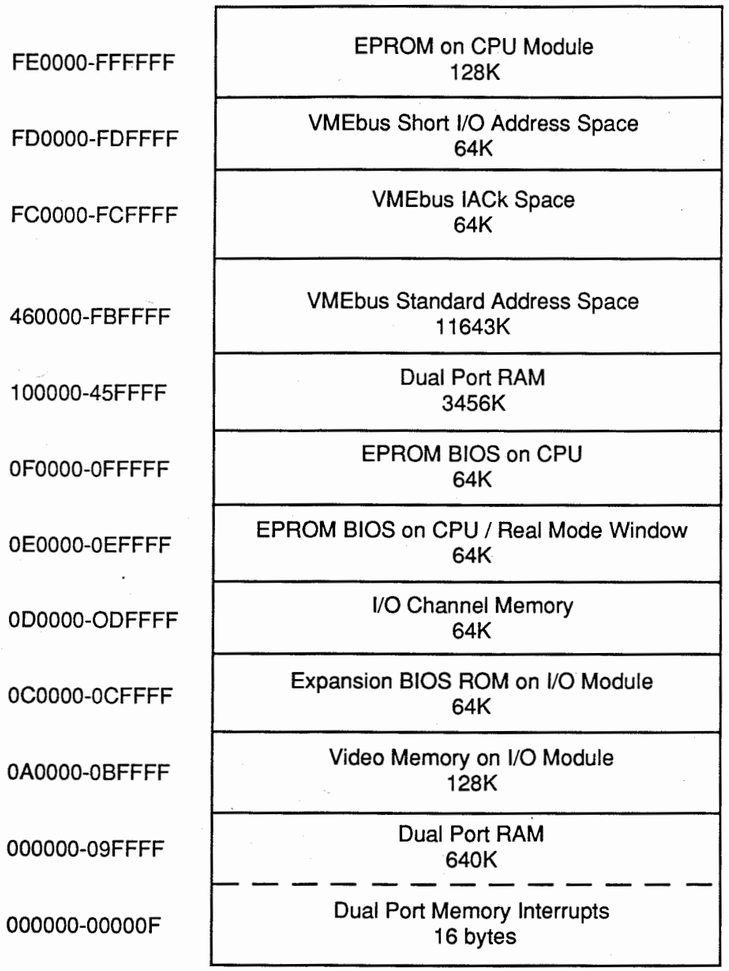


Figure 6-2 4 MB Memory Map (As Seen by the 80286 CPU)

6.2.5 VMEbus Short I/O Address Space

Any 80286 references to bytes in address space FD0000-FDFFFF will reference the VMEbus short I/O address space. The lower 16 bits of the 80286's address bus will be used to select a byte in the 64K short I/O space. Note that the 80286 must be in protected mode to access the short I/O in this fashion.

6.3 XVME-682 I/O PORT ADDRESSES

The XVME-682 I/O map contains all the I/O ports of the IBM AT architecture and some additions. Six extra I/O ports are defined at I/O address space 30-35H. These 8-bit I/O ports are mapped as follows:

I/O PORT ADDRESS	I/O PORT NAME	ACCESS
30H	CONREG	IN\OUT
31H	AUX_INT	IN ONLY
32H	STATUS_1	IN ONLY
33H	STATUS_2	IN ONLY
34H	VME_HI_ADD	OUT ONLY
35H	TRIG_WDT	IN\OUT

The following sections discuss these six I/O ports.

6.3.1 CONREG

This input\output port is the control register used to control many module functions. All bits of this port are set to zero when the module is reset. Its bits are defined as follows:

D0 = 0 The watchdog timer is disabled.
D0 = 1 The watchdog timer is enabled.

D1 = 0 The FAIL LED is on and the 682 is asserting SYSFAIL.
D1 = 1 The FAIL LED is off and the 682 is not asserting SYSFAIL.

D2 = 0 The PASS LED is off.
D2 = 1 The PASS LED is on.

D3 = 0 The VMEbus requester is to release the VMEbus.
D3 = 1 The VMEbus requester is to acquire the VMEbus.

D4 = 0 Auxiliary NMI sources are disabled.
D4 = 1 Auxiliary NMI sources are enabled.

6.3.4 STATUS_2

This input port is a status port, its bits are defined as follows:

D0-D3 Allows the 80286 to determine where the dual port RAM is mapped on the VMEbus.

D4=0 If the VMEbus requester has ownership of the VMEbus.
D4=1 If not.

D5=0 If VMEbus signal SYSFAIL is asserted.
D5=1 If not.

D6=0 If VMEbus signal ACFAIL is asserted.
D6=1 If not.

D7=0 If the watchdog timer has timed out.
D7=1 If not.

6.3.5 VME_HI_ADD

This output port is used to provide the upper 8 address bits when the VMEbus standard address space is accessed through the window.

6.3.6 TRIG_WDT

This port is used to trigger the watchdog timer. Inputs or outputs to this port will trigger the watchdog timer. No data is exchanged during these accesses. Refer to Section 6.5.3 for additional information on the watchdog timer.

Before accessing the Window in this mode, the upper 8 VMEbus address bits must be sent to register VME_HI_ADD. This defines which 64k byte block of the standard VMEbus address space will be accessed. Subsequent accesses to the window will use the 8 bits in VME_HI_ADD and the lower 16 bits of the CPU's address to form the 24 bit VMEbus address.

For example, to read word 123456H in the VMEbus standard address space, configure the window for VMEbus standard address space, output 12H to output port VME_HI_ADD (address 34H), and do a word read at address 0E3456H. The word returned will be from VMEbus address 123456H.

6.4.3 VMEbus IACK SPACE

When the Window is configured for the VMEbus IACK space, a byte read from the Window will cause the XVME-682 to perform a VMEbus IACK cycle. The data returned from the byte read will be the status ID vector returned from the responding interrupter. See Section 6.5 Interrupts.

The VMEbus interrupt level acknowledged depends on the window address read per the following:

WINDOW ADDRESS	VMEBUS INTERRUPT LEVEL
0E0003	1
0E0005	2
0E0007	3
0E0009	4
0E000B	5
0E000D	6
0E000F	7

6.4.4 EPROM

When the Window is configured for EPROM, the lower 64K bytes of the EPROM will appear in the Window. This is the mode selected after reset. This mode is compatible with the IBM PC/AT architecture.

6.5 INTERRUPTS

The XVME-682 is capable of generating interrupts on both the PC/ATbus and VMEbus structures. They are VMEbus and Dual Port Interrupt are generated on the VMEbus. On the PC/ATbus Auxiliary Non-Maskable Interrupts (the abort button, the watchdog timer, SYSFAIL, and ACFAIL) are generated on the PC/ATbus. The next sections will discuss how these interrupts are generated and handled.

The XVME-682 BIOS masks off interrupt levels 10, 11, 12, and 15 during its initialization phase. Before using VMEbus interrupts or Dual-Port memory interrupts, this mask must be changed. The following code will modify the mask in the 8259 Interrupt Controller located at I/O port address A1H:

```
IN A1,0A1H          ;get interrupt mask
AND A1, 01100011b ;enable IRQ 10, 11, 12, and 15
OUT 0A1H, A1        ;write out new mask
```

> **NOTE**
> A "0" in the interrupt mask location enables the interrupt, a "1" masks it.

6.5.1 VMEbus Interrupts

Each VMEbus interrupt line has a bit position in the AUX_INT input port. VMEbus interrupt level 7 corresponds to AUX_INT bit position 7, and so on through VMEbus interrupt level 1 which corresponds to AUX_INT bit position 1. When a particular bit in AUX_INT is set, the corresponding VMEbus interrupt is pending.

When the local 80286 processor receives an interrupt on IRQ10 - IRQ12 or IRQ15, the user program must read the AUX_INT port to determine the VMEbus interrupt level. The user program must perform a read in the VMEbus IACK space to obtain the vector and complete the VMEbus IACK cycle. Software should check to ensure the VMEbus interrupter has negated its interrupt before leaving the ISR (interrupt service routine).

Figure 6-3 shows how VMEbus interrupt levels (1-7) are handled on the XVME-682 CPU module.

When the local 80286 processor receives an interrupt on IRQ10 - IRQ12 or IRQ15, the user program must read the AUX_INT port to determine the VMEbus interrupt level. The user program must perform a read in the VMEbus IACK space to obtain the vector and complete the VMEbus IACK cycle. Software should check to ensure the VMEbus interrupter has negated its interrupt before leaving the ISR (interrupt service routine).

6.5.2 Dual-Port Interrupts

Another VMEbus master may interrupt the XVME-682 by reading any one of the lower 16 bytes of the module's dual port RAM. When this access occurs the dual port interrupt is latched and remains latched until bit 7 of CONREG is reset. The status of this interrupt is available in AUX_INT bit 0. When bit 0 is set the interrupt is pending. The dual port interrupt must be cleared by resetting bit 7 of CONREG.

A jumper is provided to enable\disable this interrupt, when J1 is IN the dual port interrupt is enabled, when OUT the interrupt is disabled. See Figure 6-3 for a diagram of the XVME-682 Auxiliary Maskable Interrupt Structure.

6.5.3 Auxiliary Non-Maskable Interrupts

Four non-maskable interrupts have been added to the basic IBM PC/AT architecture. These four auxiliary non maskable interrupts (ANMIs) are: the abort button, the watchdog timer, SYSFAIL, and ACFAIL. See Figure 6-4.

The IBM PC/AT architecture provides a mechanism to disable and enable NMIs. An output to port 70h with D7=0 will enable NMIs. An output to port 70h with D7=1 will disable NMIs. This same mechanism will enable and disable the ANMIs. All four ANMIs are implemented as latches.

When the interrupt event occurs, and is enabled, the latch will set. The latch remains set until the interrupt is disabled or a system reset occurs.

SYSFAIL, ACFAIL, and the abort button are all enabled by bit 4 of CONREG. If bit 4 is on, the occurrence of the interrupt event will set a latch, which remains set until bit 4 is reset. When the latch is set a NMI will occur if module NMI is enabled.

The state of these latches can be determined by checking input port STATUS_1. SYSFAIL latch is bit 2, ACFAIL latch is bit 1, and the abort button latch is bit 3. When these bits are high the corresponding latch is set.

The watchdog timer (WDT) ANMI is enabled by bit 0 of CONREG. The WDT has a timeout period of approximately 150 ms. If bit 0 of CONREG is set and the WDT expires, a latch will set and remain set until bit 0 of CONREG is reset. If the module NMI is enabled, the setting of this latch will generate a module ANMI.

The state of this latch is available in bit 7 as input port STATUS_2. When the latch is set, bit 7 will read 0, when the latch is reset, the bit will read 1.

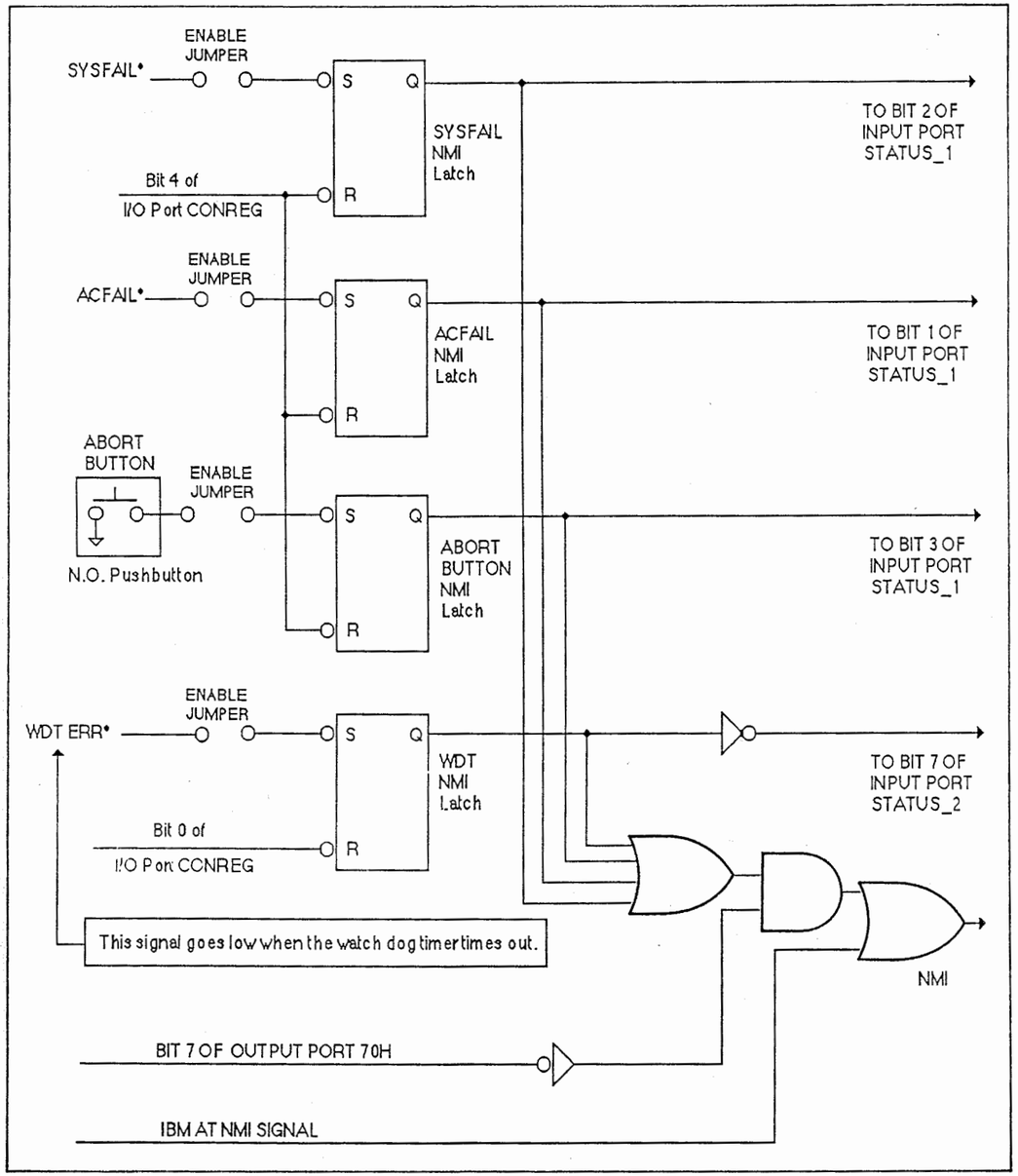


Figure 6-4 Auxiliary Non-maskable Interrupt Structure

6.7 BYTE SWAPPING

The VMEbus and PC/AT conventions differ in two important ways. The first is in how each addresses data bus bits. The second involves references to numeric variables longer than eight bits.

When comparing the way the VMEbus addresses data bus bits, relative to the way the PC/AT family addresses them, we find that the bytes are swapped as follows:

DATA BITS	VMEbus	PC/ATbus
D15-D08	Byte 0	Byte 1
D7-D0	Byte 1	Byte 0

When referring to a numeric variable longer than eight bits, the PC/AT stores the least significant byte (LSB) at the lower address while the VMEbus (Motorola type) requires that the most significant byte (MSB) be stored at the lowest address.

This problem concerns only numeric values. String-type variables are treated the same by both devices.

Xycom solved the data bus bit-swapping problem by connecting Byte 0 of the CPU to D15-D8 of the VMEbus, and Byte 1 of the CPU to D7-D0 of the VMEbus.

PC/AT DATA BUS	VME DATA BUS	BYTE
D7-D0	D15-D8	0
D15-D8	D7-D0	1

The second problem must be solved with software because the external hardware cannot distinguish between numeric and string-type variables. The programmer must be aware of the fact that whenever numerics are to be exchanged between the PC/AT and the Motorola-type devices on the VMEbus, data bytes must be swapped.

Example

PC/AT word = 1234

This word must be written to VMEbus (Motorola-type) devices as 3412

Appendix A

VMEbus CONNECTOR/PIN DESCRIPTION

Table A-1 J1 - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	1B:3	AC FAILURE: Open-collectors driven signal which indicates that the AC input to the power supply is no longer being provided, or that the required input voltage levels are not being met.
IACKIN*	1A:21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A:22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AM0-AM5	1A:23 1B:16,17, 18,19 1C:14	ADDRESS MODIFIER (bits 0-5): Three-state driven lines that provide additional information about the address bus, such as: size, cycle type, and/or DTB master identification.
AS*	1A:18	ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.
A01-A23	1A:24-30 1C:15-30 A24-A31 2B:4-11	ADDRESS BUS (bits 1-23): Three-state driven address lines that specify a memory address. ADDRESS BUS (bits 24-31): Three-state driven bus expansion address lines.

Table A-1 J1 - VMEbus Signal Identification cont.

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
D00-D15	1A:1-8 1C:1-8	DATA BUS (bits 0-15): Three-state driven, bi-directional data lines that provide a data path between the DTB master and slave.
GND	1A:9,11, 15,17,19, 1B:20,23, 1C:9 2B:2,12, 22,31	GROUND
IACK*	1A:20	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any master processing an interrupt request. It is routed via the backplane to slot 1, where it is looped-back to become slot 1 IACKIN* in order to start the interrupt acknowledge daisy-chain.
IRQ1*- IRQ7*	1B:24-30	INTERRUPT REQUEST (1-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	1C:13	LONGWORD: Three-state driven signal indicates that the current transfer is a 32-bit transfer.
(RESERVED)	2B:3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	1B:21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B:22	A reserved signal which will be used as the transmission line for serial communication bus messages.
SYSCLK	1A:10	SYSTEM CLOCK: A constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.

BACKPLANE CONNECTOR J1

The following table lists the P1 pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

Table A-2 J1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 V	+5 V STDBY	+12 V
32	+5 V	+5 V	+5 V

Appendix B

DEFAULT JUMPER CONFIGURATIONS

B.1 CPU MODULE DEFAULT JUMPER CONFIGURATIONS

The XVME-682 CPU module is shipped in the following jumper configurations

Table B-1 XVME-682 CPU Module Jumper Options

JUMPER	FUNCTION	DEFAULT
J1	Enables dual-port interrupt when installed	IN
J2	Reserved; must be installed for proper operation	IN
J3	Reserved; must be installed for proper operation	IN
J4	Defines VMEbus arbitration level in conjunction with J8 & J12	A
J5	Enables/disables VME "Slot 1" functions in conjunction with J6, J9, J15 & J34	IN
J6	Enables/disables VME "Slot 1" functions in conjunction with J5, J9, J15 & J34	IN
J7	Defines VMEbus address bits for slave interface in conjunction with J13, J14 & J25	OUT
J8	Defines VMEbus arbitration level in conjunction with J4 & J12	A
J9	Enables/disables VME "Slot 1" functions in conjunction with J5, J6, J15 & J34	A
J10	Reserved; must be installed for proper operation	IN

Table B-1 XVME-682 CPU Module Jumper Options cont.

JUMPER	FUNCTION	DEFAULT
J23	Enables VMEbus interrupt Level 1 when installed	IN
J24	Enables VMEbus interrupt Level 4 when installed	IN
J25	Defines VMEbus address bits for slave interface in conjunction with J7, J13, and J14	IN
J26 (cluster)	Defines which AT interrupt level is used as follows: J26A IRQ15 J26B IRQ12 J26C IRQ11 J26D IRQ10	A
J27	Enables AT interrupt level IRQ7 when installed	IN
J28	Enables AT interrupt level IRQ3 when installed	IN
J29	Enables AT interrupt level IRQ4 when installed	IN
J30	Enables AT interrupt level IRQ5 when installed	IN
J31	Reserved; must be installed for proper operation	A
J32 (cluster)	Selects which unit level (0-3) the port supplier chip is assigned to as follows: J32A 3 J32B 2 J32C 1 J32D 0	D

Table B-1 XVME-682 CPU Module Jumper Options cont.

JUMPER	FUNCTION	DEFAULT
J43	Part of serial port #2 (COM2) configuration block: either RS-232 or RS-422	B
J44	Enables on-board battery: IN = enabled OUT = disabled	OUT
J45	Enables the VMEbus slave interface when installed	IN
J46	Reserved; must be OUT for normal operation	OUT
J47	Defines EPROM type in conjunction with J48	A
J48	Defines EPROM type in conjunction with J47	B
J49	Reserved; must be OUT for normal operation	OUT
J50	Enables Watchdog Timer interrupts when installed	IN
J51	Enables ACFAIL interrupts when installed	IN
J52	Enables SYSFAIL interrupts when installed	IN
J53	Enables SYSRESET pushbutton on front panel when installed	IN
J54	Enables BERR signals when installed	IN
J55	Reserved; must be OUT for normal operation	OUT

B.2 I/O MODULE DEFAULT JUMPER CONFIGURATIONS

The XVME-682 I/O module is shipped in the following jumper configurations. Table B-2 lists the various jumpers on the XVME-682 I/O module and their uses.

Table B-2 XVME-682 I/O Module Jumper Options

JUMPER	FUNCTION	PC/AT DEFAULT
J1	I/O Address for Floppy Disk Controller: A = use secondary address (372-377H) B = use primary address (3F2-3F7H)	B
J2	I/O Address for Hard Disk Controller: IN = use secondary address of (170-177H) OUT = use primary address of (1F0-1F7H)	OUT
J3	Status Read IN = Status read is latched OUT = Status read is not latched. J3 is left OUT with the COMPAQ 286.	IN
J4	Hard Disk Drive Configuration A = Supports only 2-head, 612-cylinder hard-disk drive with standard system setup for 4-head, 306-cylinder drive. B = Supports any hard disk drive listed on BIOS hard drive table.	B
J5	Step rate A = Selects 16 microsec. step rate B = Selects 35 microsec. step rate	B
J6	EGA I/O Address IN = selects secondary address (2xxH) OUT = selects primary address (3xxH)	OUT

Appendix C

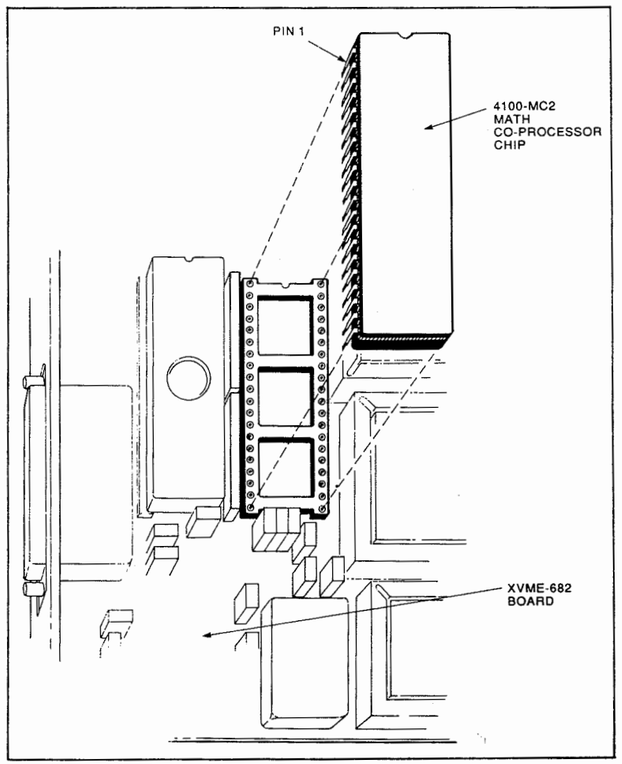
INSTALLATION OF OPTIONS

C.1 INTRODUCTION

This appendix will discuss the installation of the optional equipment that goes with the XVME-682 Processor Module.

C.2 MATH CO-PROCESSOR

Install the Math-Coprocessor as per the illustration below.

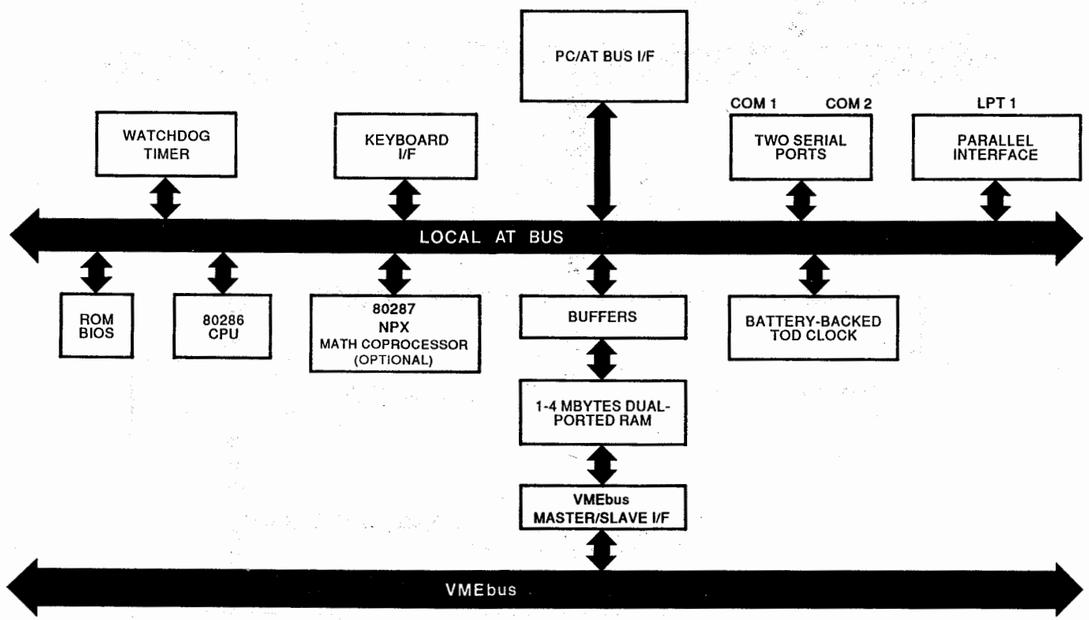


Appendix D

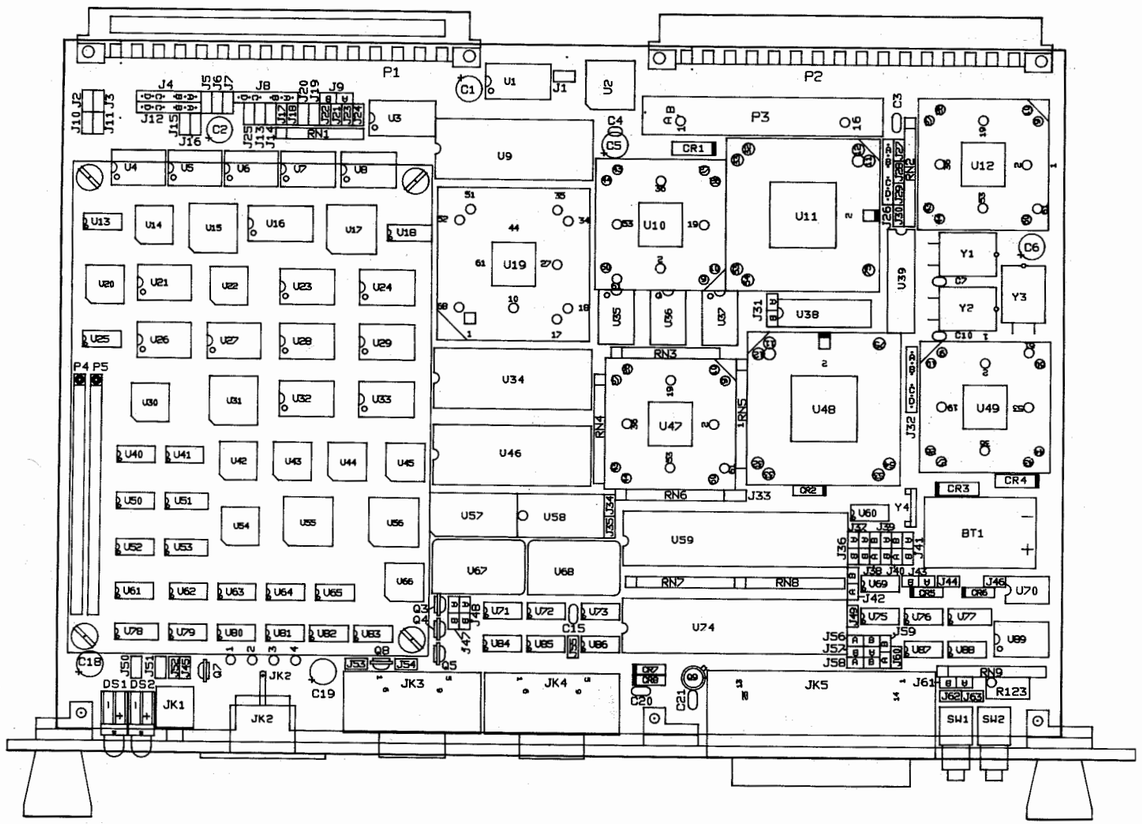
BLOCK DIAGRAMS, ASSEMBLY DRAWINGS, & SCHEMATICS

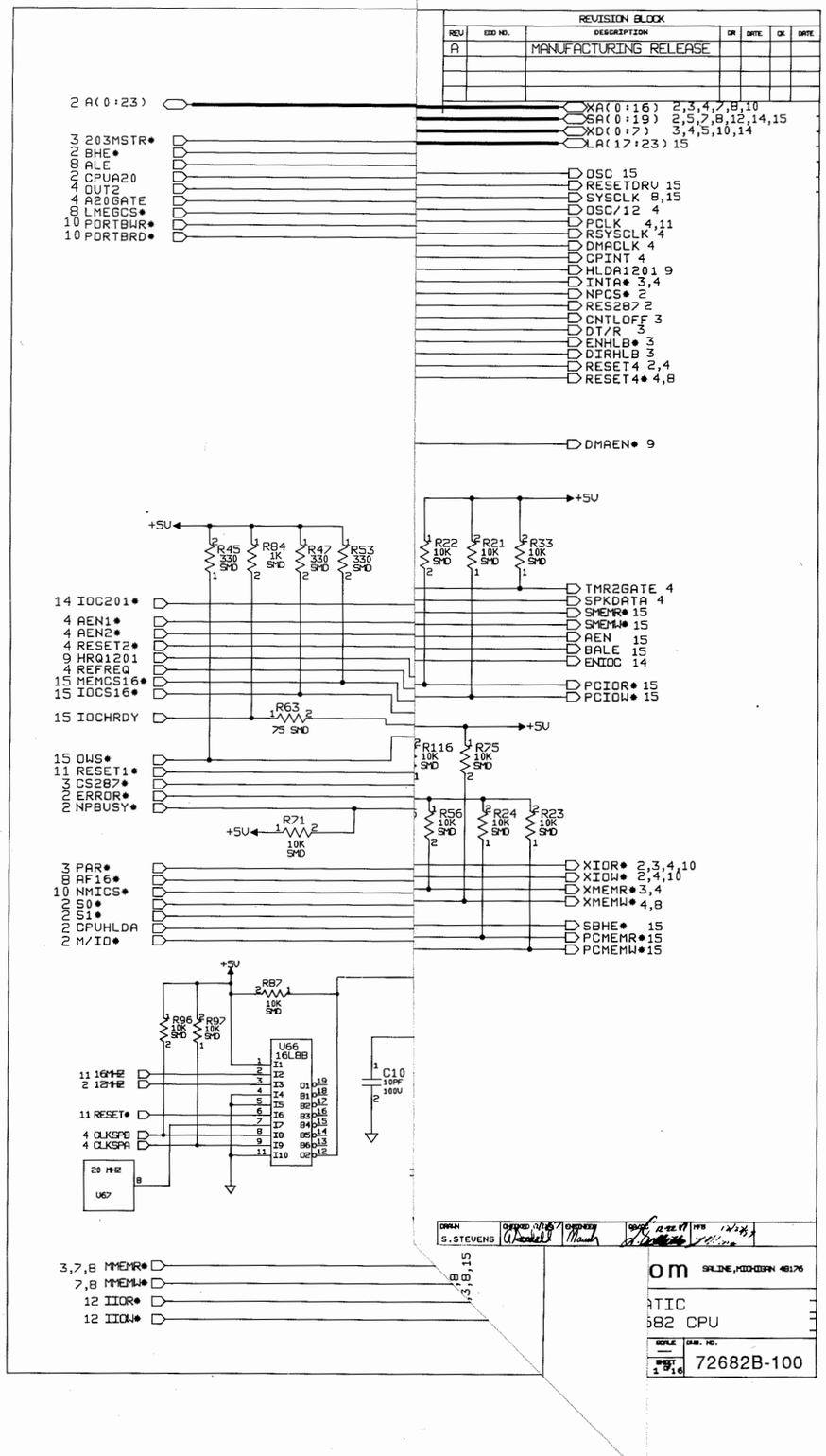
NOTE
These schematics and assembly drawings are for the Revision Level **C** artwork **ONLY.**

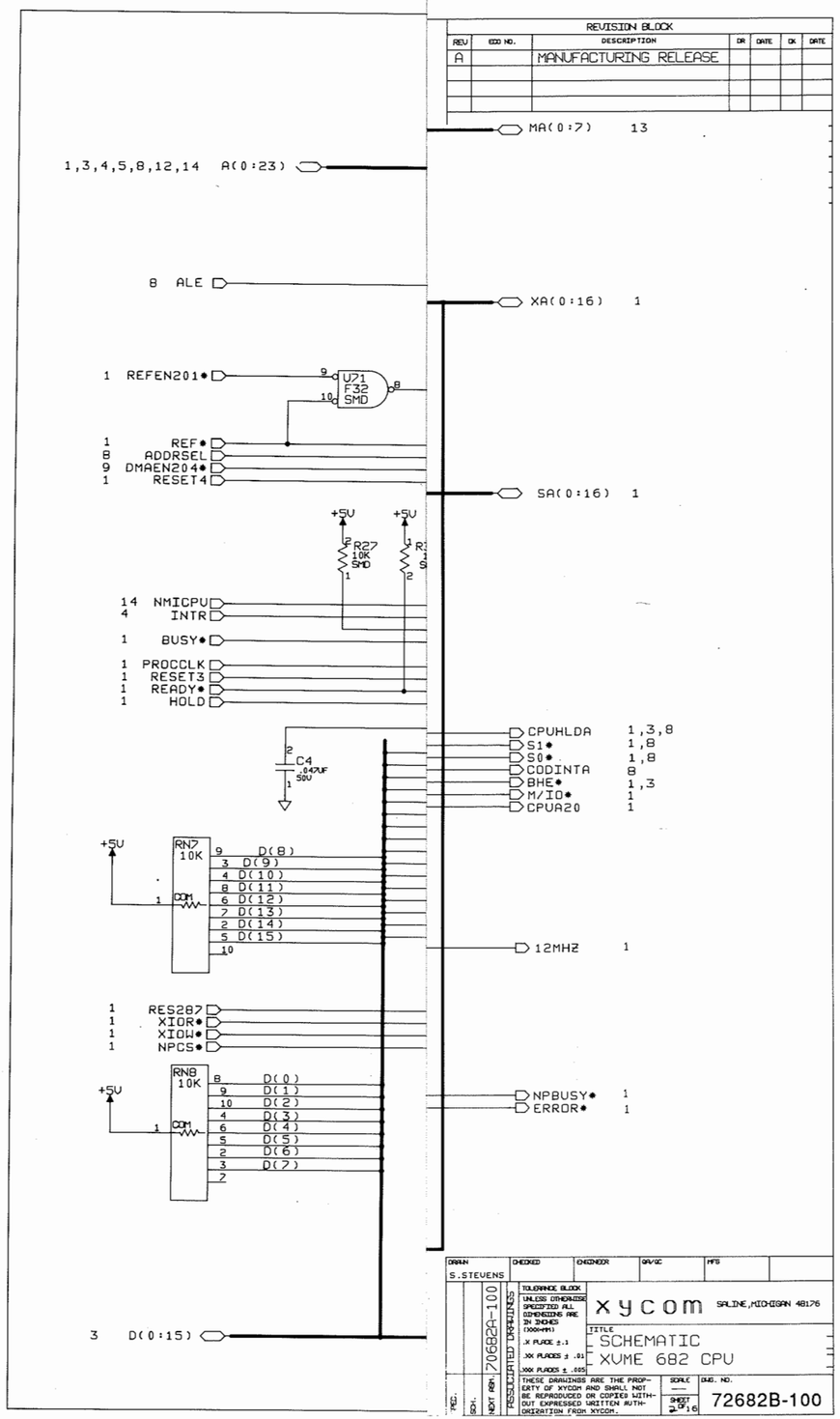
XVME-682 CPU BLOCK DIAGRAM

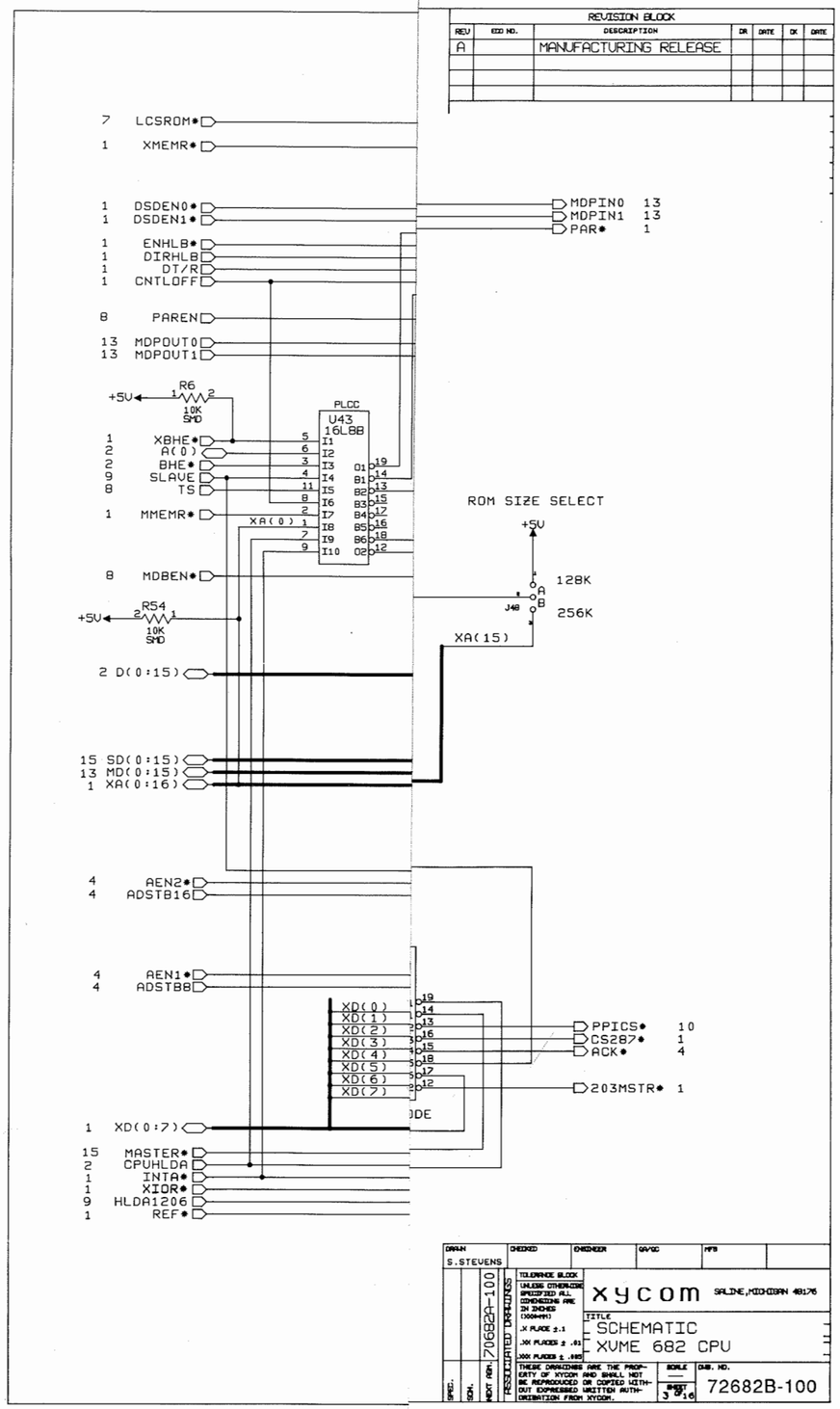


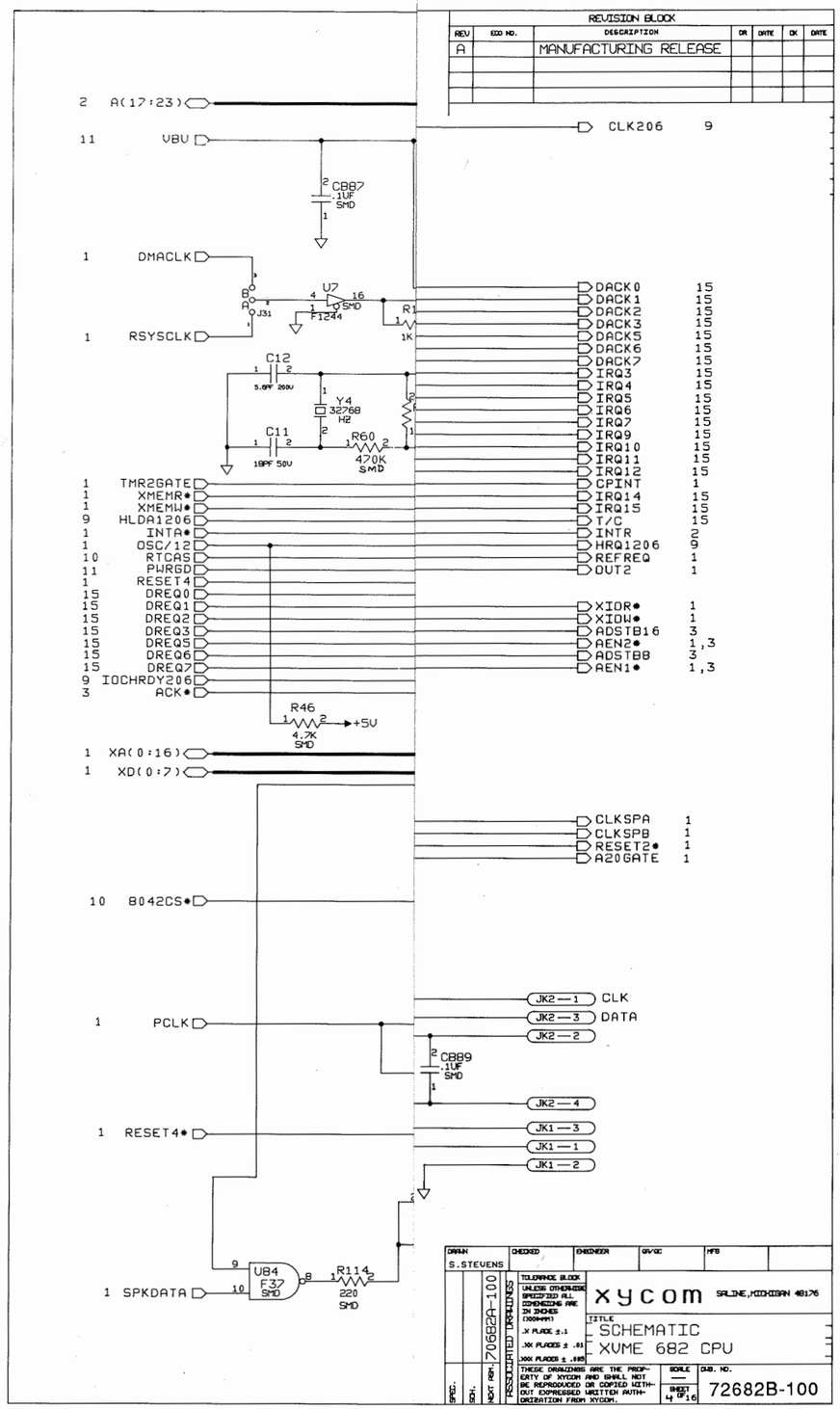
XVME-682 CPU ASSEMBLY DRAWING




REVISION BLOCK
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DESCRIPTION
DR
DATE
CK
DATE
A
MANUFACTURING RELEASE
2 A(0:23)
XA(0:16) 2,3,4,7,8,10
SA(0:19) 2,5,7,8,12,14,15
XD(0:7) 3,4,5,10,14
LA(17:23) 15
3 203MSTR*
2 BHE*
8 ALE
2 CPUA20
4 OUT2
4 A20GATE
8 LMEGCS*
10 PORTBWR*
10 PORTBRD*
OSC 15
RESETDRV 15
SYSCLK 8,15
OSC/12 4
PCLK 4,11
RSYSCLK 4
DMACLK 4
CPINT 4
HLDA1201 9
INTA* 3,4
NPCS* 2
RES287 2
CNTLOFF 3
DT/R 3
ENHLB* 3
DIRHLB 3
RESET4 2,4
RESET4* 4,8
DMAEN* 9
+5V
R45 330 SMD
R84 1K SMD
R47 330 SMD
R53 330 SMD
R22 10K SMD
R21 10K SMD
R33 10K SMD
14 IOC201*
4 AEN1*
4 AEN2*
4 RESET2*
9 HRQ1201
4 REFREQ
15 MEMCS16*
15 IOCS16*
TMR2GATE 4
SPKDATA 4
SMEMR* 15
SMEMW* 15
AEN 15
BALE 15
ENIOC 14
PCIOR* 15
PCIOW* 15
15 IOCHRDY
R63 75 SMD
15 OWS*
11 RESET1*
3 CS287*
2 ERROR*
2 NPBUSY*
R116 10K SMD
R75 10K SMD
R71 10K SMD
R56 10K SMD
R24 10K SMD
R23 10K SMD
3 PAR*
8 AF16*
10 NMICS*
2 S0*
2 S1*
2 CPUHLDA
2 M/IO*
XIOR* 2,3,4,10
XIOW* 2,4,10
XMEMR* 3,4
XMEMW* 4,8
SBHE* 15
PCMEMR* 15
PCMEMW* 15
R87 10K SMD
R96 10K SMD
R97 10K SMD
U66 16L8B
11 16M2
2 12M2
11 RESET*
4 CLKSPB
4 CLKSPA
C10 10PF 100V
20 MHZ
U67
3,7,8 MMEMR*
7,8 MMEMW*
12 IIOR*
12 IIOW*
3,8,15
DRAWN
S.STEVENS
SALINE,MICHIGAN 48176
ATIC
682 CPU
SCALE
DWG NO.
72682B-100
SHEET
1 OF 16


REVISION BLOCK
REV
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
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MANUFACTURING RELEASE
MA(0:7) 13
1,3,4,5,8,12,14 A(0:23)
8 ALE
XA(0:16) 1
1 REFEN201*
U71 F32 SMD
1 REF*
8 ADDRSEL
9 DMAEN204*
1 RESET4
SA(0:16) 1
+5V
R27 10K SMD
14 NMICPU
4 INTR
1 BUSY*
1 PROCCLK
1 RESET3
1 READY*
1 HOLD
CPUHLDA 1,3,8
S1* 1,8
S0* 1,8
CODINTA 8
BHE* 1,3
M/IO* 1
CPUA20 1
C4 .047UF 50V
RN7 10K
D(8)
D(9)
D(10)
D(11)
D(12)
D(13)
D(14)
D(15)
COM
12MHZ 1
1 RES287
1 XIOR*
1 XIOW*
1 NPCS*
RN8 10K
D(0)
D(1)
D(2)
D(3)
D(4)
D(5)
D(6)
D(7)
NPBUSY* 1
ERROR* 1
3 D(0:15)
DRAWN
S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XXX=MM)
.X PLACE ± .1
.XX PLACES ± .01
.XXX PLACES ± .005
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TITLE
SCHEMATIC
XVME 682 CPU
SCALE —
SHEET 2 OF 16
DWG. NO.
72682B-100
NEXT ASM.
72682A-100
ASSOCIATED DRAWINGS
MFG.
SCH.


REVISION BLOCK
REV | ECO NO. | DESCRIPTION | DR | DATE | CK | DATE
A | | MANUFACTURING RELEASE
7 LCSROM*
1 XMEMR*
1 DSDEN0*
1 DSDEN1*
MDPIN0 13
MDPIN1 13
PAR* 1
1 ENHLB*
1 DIRHLB
1 DT/R
1 CNTLOFF
8 PAREN
13 MDPOUT0
13 MDPOUT1
+5V
R6
10K
SMD
PLCC
U43
16L8B
1 XBHE*
2 A(0)
2 BHE*
9 SLAVE
8 TS
1 MMEMR*
XA(0)
8 MDBEN*
ROM SIZE SELECT
+5V
128K
256K
J48
XA(15)
R54
10K
SMD
2 D(0:15)
15 SD(0:15)
13 MD(0:15)
1 XA(0:16)
4 AEN2*
4 ADSTB16
4 AEN1*
4 ADSTB8
XD(0)
XD(1)
XD(2)
XD(3)
XD(4)
XD(5)
XD(6)
XD(7)
PPICS* 10
CS287* 1
ACK* 4
203MSTR* 1
1 XD(0:7)
15 MASTER*
2 CPUHLDA
1 INTA*
1 XIOR*
9 HLDA1206
1 REF*
DRAWN S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (3000MM)
.X PLACE ±.1
.XX PLACES ± .03
.XXX PLACES ± .005
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TITLE
SCHEMATIC
XVME 682 CPU
SIZE
DWG. NO.
72682B-100
SHEET 3 OF 16
NEXT ASSY. 72682A-100
GEN.
SPEC.
ASSOCIATED DRAWINGS


REVISION BLOCK
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ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
A
MANUFACTURING RELEASE
2 A(17:23)
11 VBU
CLK206 9
CB87 .1UF SMD
1 DMACLK
1 RSYSCLK
U7 F1244 SMD
J31
R1 1K
C12 5.6PF 250V
Y4 32768 HZ
C11 18PF 50V
R60 470K SMD
DACK0 15
DACK1 15
DACK2 15
DACK3 15
DACK5 15
DACK6 15
DACK7 15
IRQ3 15
IRQ4 15
IRQ5 15
IRQ6 15
IRQ7 15
IRQ9 15
IRQ10 15
IRQ11 15
IRQ12 15
1 TMR2GATE
1 XMEMR*
1 XMEMW*
9 HLDA1206
1 INTA*
1 OSC/12
10 RTCAS
11 PWRGD
1 RESET4
15 DREQ0
15 DREQ1
15 DREQ2
15 DREQ3
15 DREQ5
15 DREQ6
15 DREQ7
9 IOCHRDY206
3 ACK*
CPINT 1
IRQ14 15
IRQ15 15
T/C 15
INTR 2
HRQ1206 9
REFREQ 1
OUT2 1
XIOR* 1
XIOW* 1
ADSTB16 3
AEN2* 1,3
ADSTB8 3
AEN1* 1,3
R46 4.7K SMD
+5V
1 XA(0:16)
1 XD(0:7)
CLKSPA 1
CLKSPB 1
RESET2* 1
A20GATE 1
10 8042CS*
1 PCLK
CB89 .1UF SMD
JK2—1 CLK
JK2—3 DATA
JK2—2
JK2—4
1 RESET4*
JK1—3
JK1—1
JK1—2
1 SPKDATA
U84 F37 SMD
R114 220 SMD
DRAWN S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XXX=MM)
.X PLACE ±.1
.XX PLACES ± .01
.XXX PLACES ± .005
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TITLE
SCHEMATIC
XVME 682 CPU
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SCALE —
SHEET 4 OF 16
DWG. NO. 72682B-100
ASSOCIATED DRAWINGS
NEXT ASM. 72682A-100
ENG.
MFG.

REVISION BLOCK						
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A		MANUFACTURING RELEASE				

1 SA(1:16)

7 VMEEN*
8 SYSALE
9 SAE*
9 LEA*

U64 F04 SMD

U25 F30 SMD

2 A(17:23)

U25 F32 SMD

8 PROMADD*

7 MAS*
10 VHIADD*
1 XD(0:7)

13 MD(0:15)

9 VDEN*

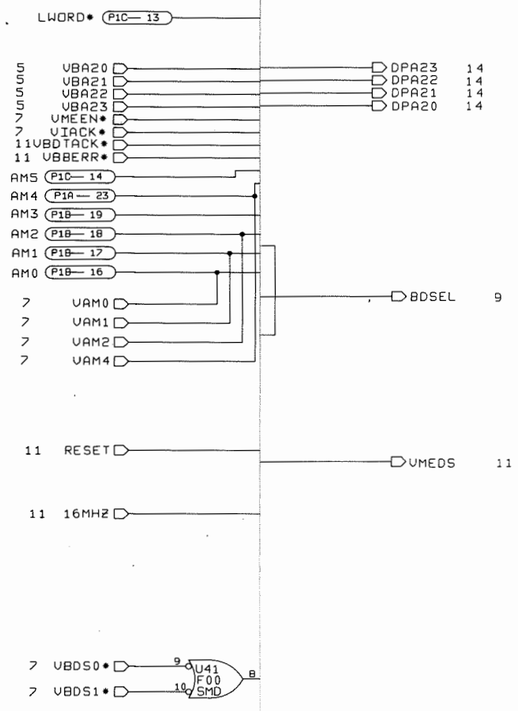
RN6 10K
+5V
COM
10
5 MD(0)
9 MD(1)
7 MD(2)
6 MD(3)
8 MD(4)
4 MD(5)
3 MD(6)
2 MD(7)

7 VDIR

6
6
6
6

DRAWN S.STEVENS	CHECKED	ENGINEER	QA/QC	MFG		
PUBLISHED DRAWING 72682A-100	TOLERANCE BLOCK UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XXX=MM) .X PLACE ±.1 .XX PLACES ± .01 .XXX PLACES ± .005	xycom SALINE,MICHIGAN 48176				
		TITLE SCHEMATIC XVME 682 CPU				
	THESE DRAWINGS ARE THE PROPERTY OF XYCOM AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT EXPRESSED WRITTEN AUTHORIZATION FROM XYCOM.	SCALE —	SIZE D	DWG. NO. 72682B-100		
		SHEET 5 OF 16				

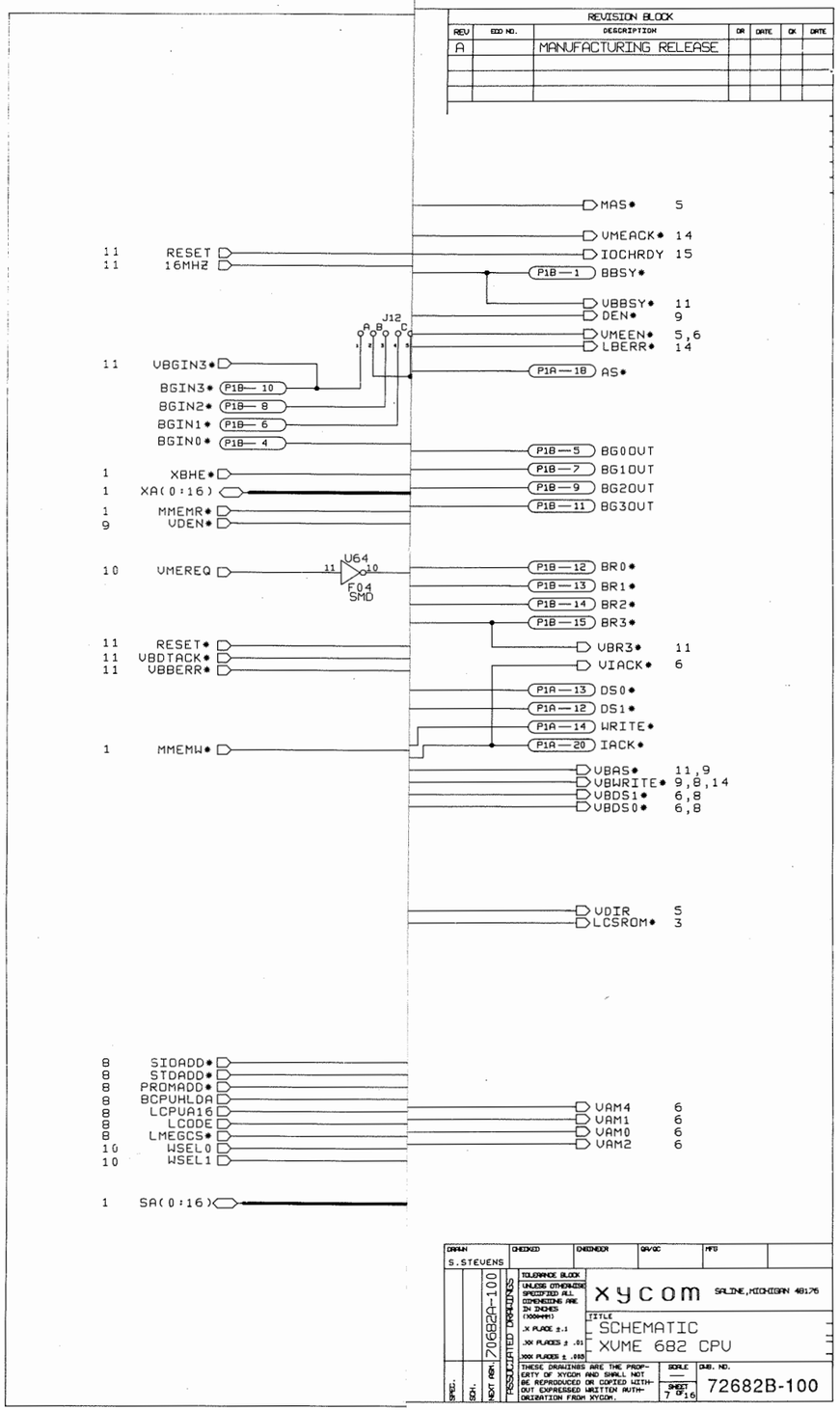
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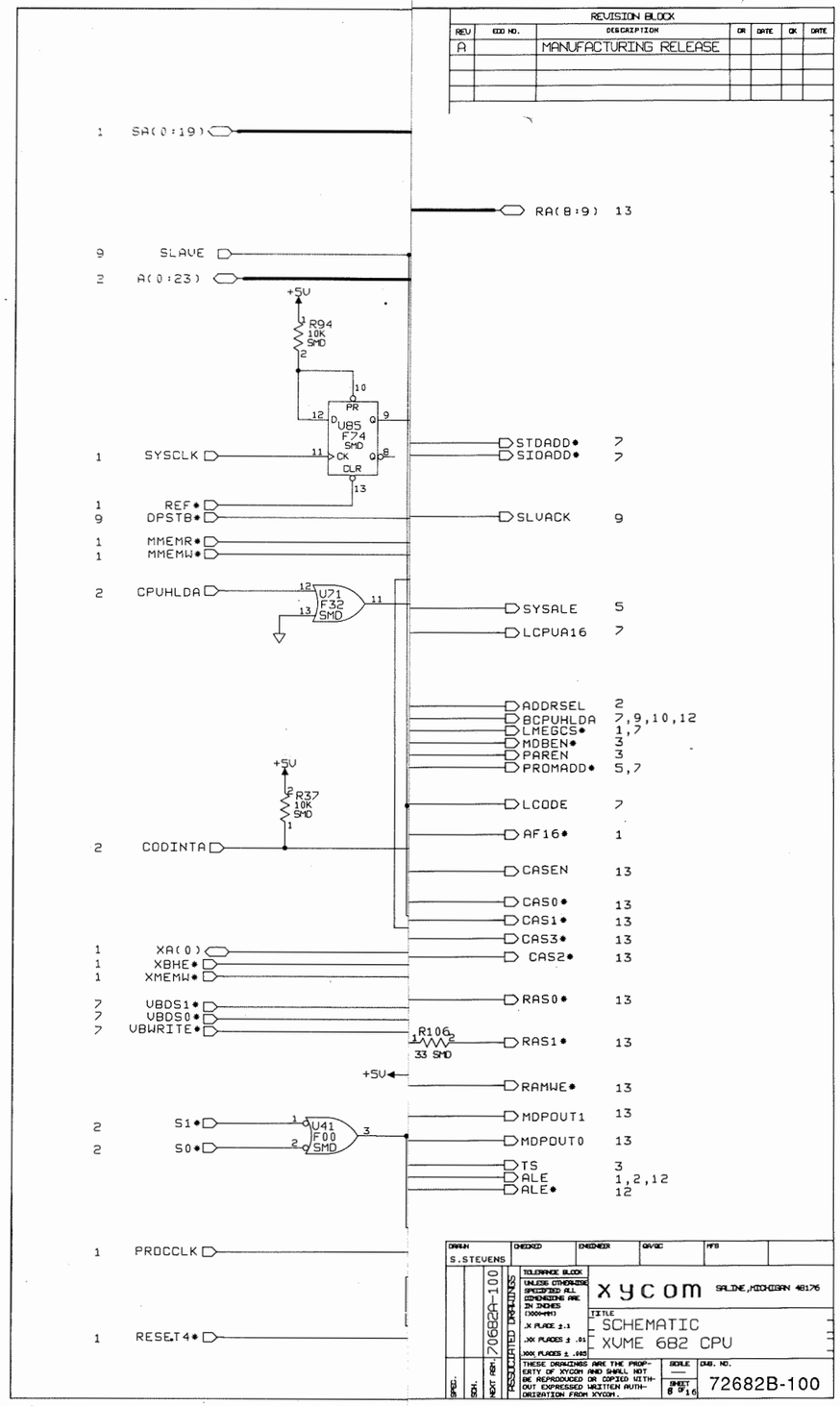


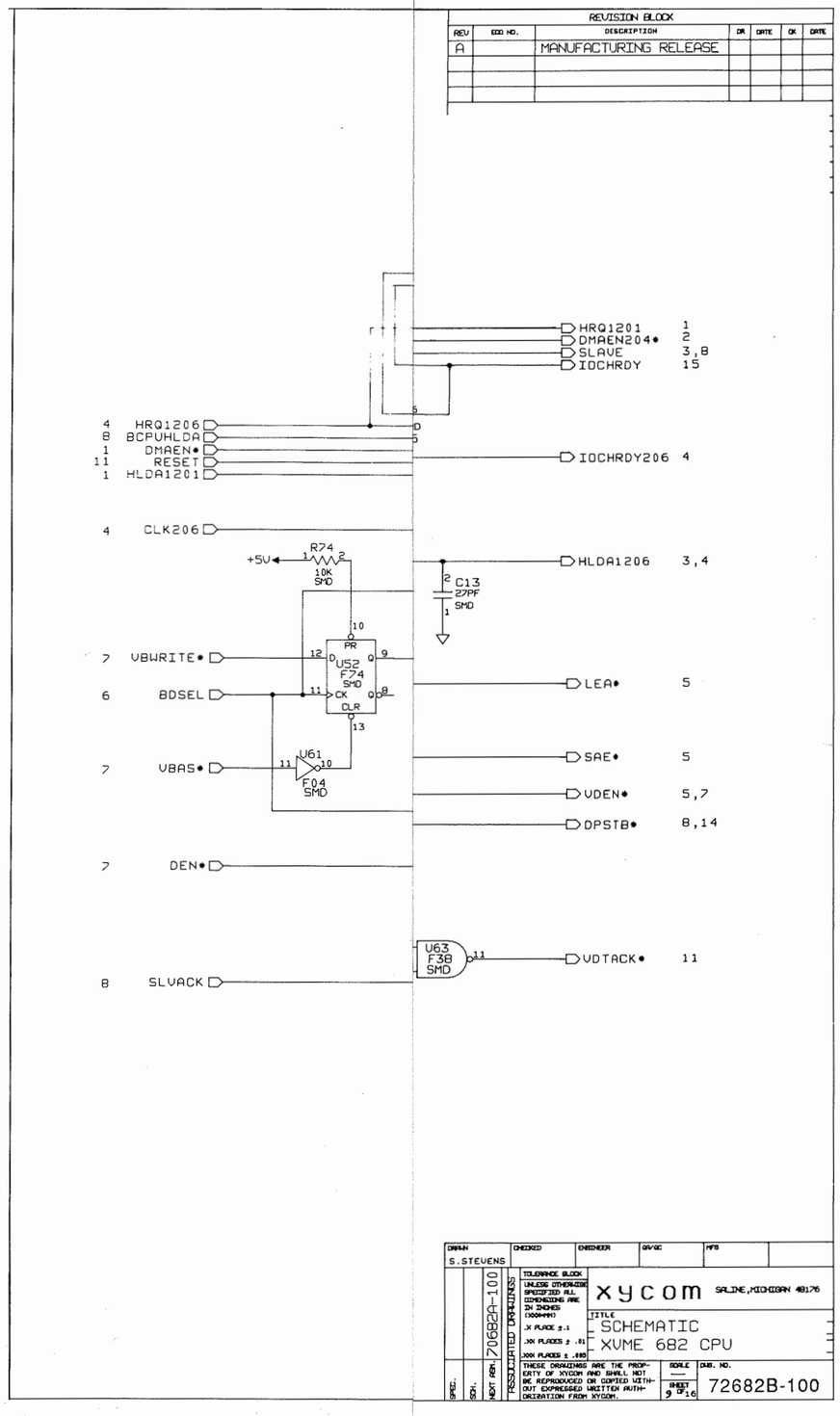
DRAWN	CHECKED	ENGINEER	QA/QC	MFG
S.STEVENS				

TOLERANCE BLOCK	xycom SALINE, MICHIGAN 48176
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (3000-MM)	TITLE SCHEMATIC XVME 682 CPU
.X PLACE ± .1	
.XX PLACES ± .03	
.XXX PLACES ± .005	
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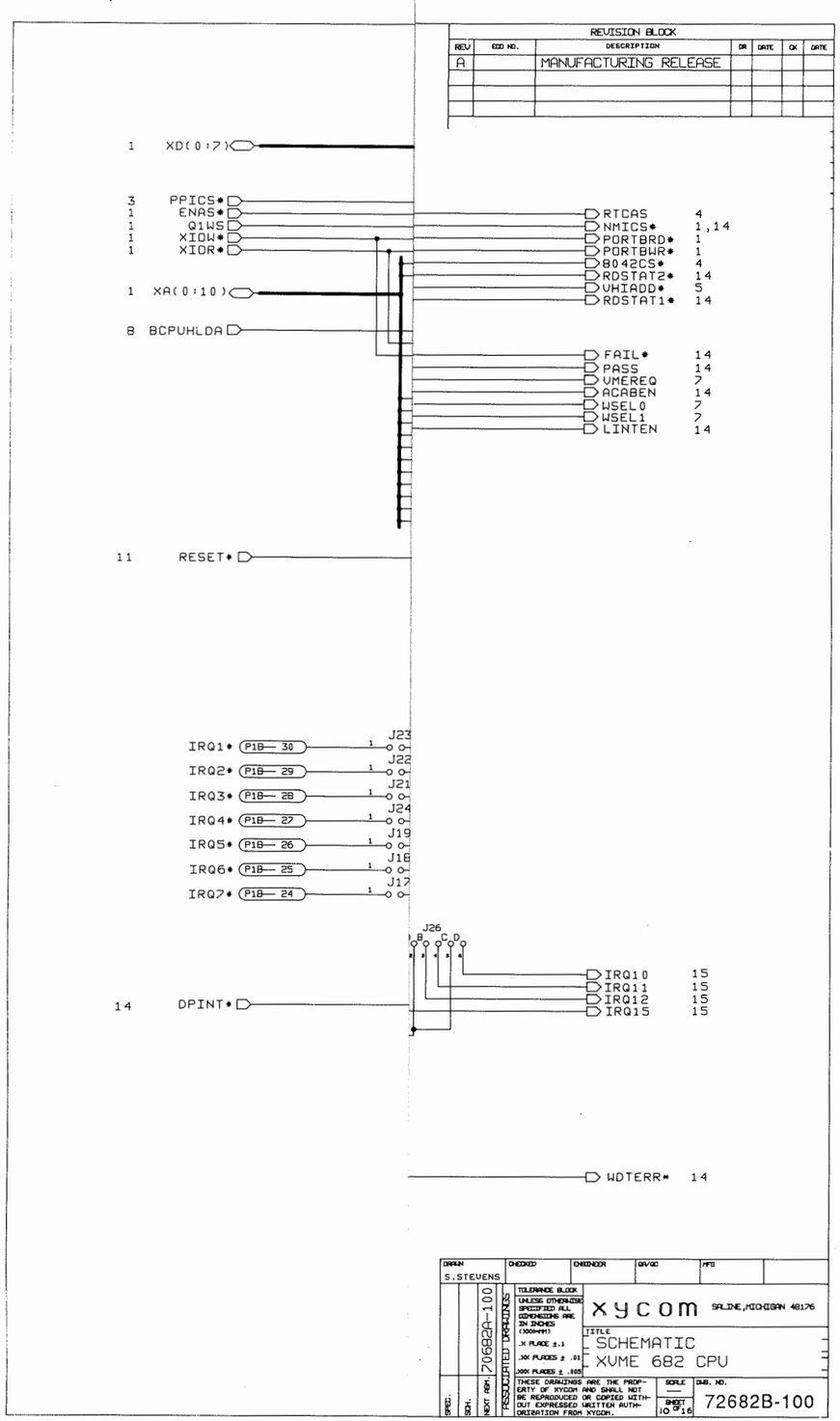
NEXT ASY. 72682A-100
ASSOCIATED DRAWINGS
SYSTEM
SCH.

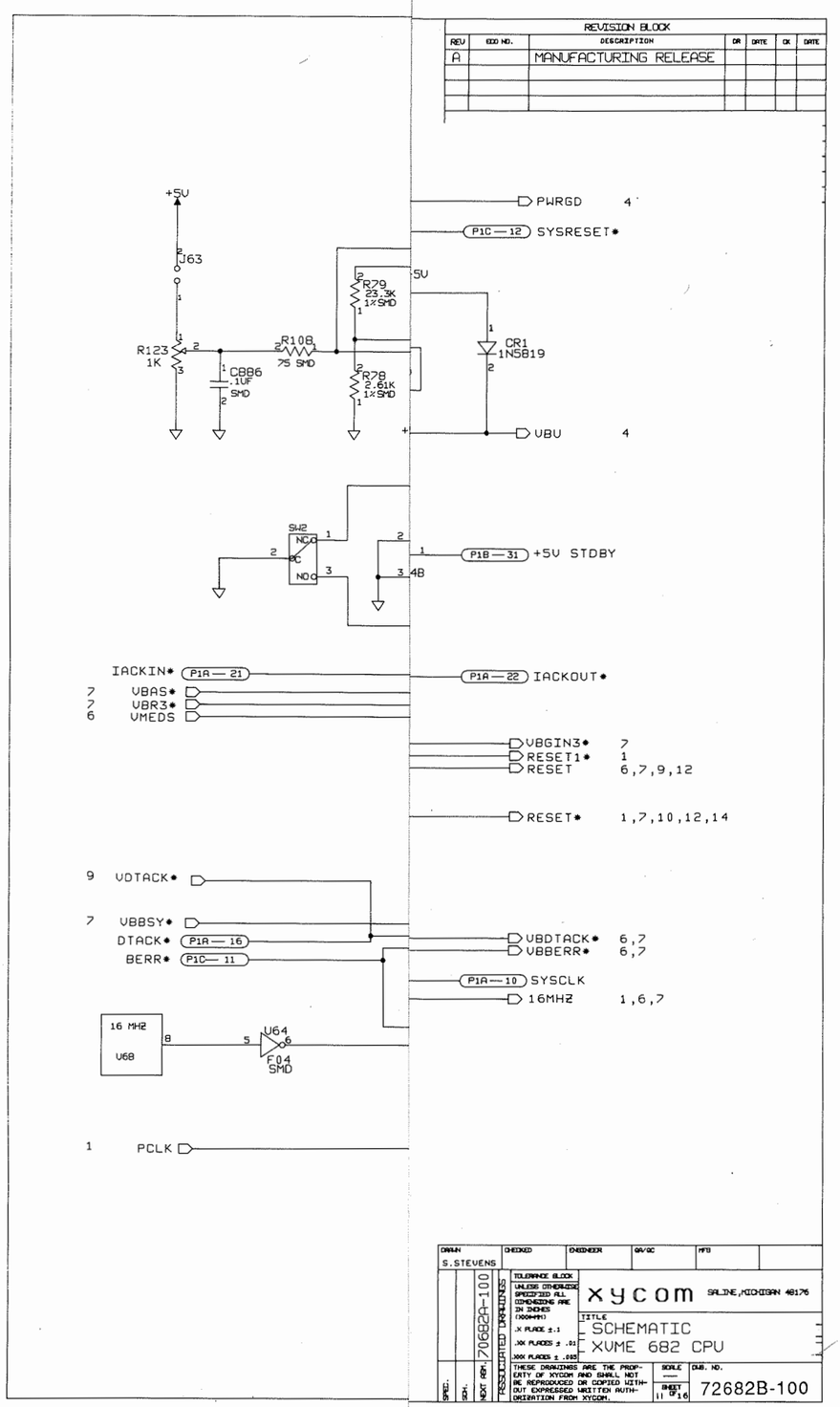

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MAS* 5
VMEACK* 14
IOCHRDY 15
BBSY*
VBBSY* 11
DEN* 9
VMEEN* 5,6
LBERR* 14
AS*
J12
A B C
11 VBGIN3*
BGIN3* P1B—10
BGIN2* P1B—8
BGIN1* P1B—6
BGIN0* P1B—4
BG0OUT P1B—5
BG1OUT P1B—7
BG2OUT P1B—9
BG3OUT P1B—11
1 XBHE*
1 XA(0:16)
1 MMEMR*
9 VDEN*
10 VMEREQ
U64
11 10
F04
SMD
BR0* P1B—12
BR1* P1B—13
BR2* P1B—14
BR3* P1B—15
11 RESET*
11 VBDTACK*
11 VBBERR*
VBR3* 11
VIACK* 6
DS0* P1A—13
DS1* P1A—12
WRITE* P1A—14
IACK* P1A—20
1 MMEMW*
VBAS* 11,9
VBWRITE* 9,8,14
VBDS1* 6,8
VBDS0* 6,8
VDIR 5
LCSROM* 3
8 SIOADD*
8 STDADD*
8 PROMADD*
8 BCPUHLDA
8 LCPUA16
8 LCODE
8 LMEGCS*
10 WSEL0
10 WSEL1
VAM4 6
VAM1 6
VAM0 6
VAM2 6
1 SA(0:16)
DRAWN S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XXmm)
.X PLACE ±.1
.XX PLACES ± .01
.XXX PLACES ± .005
THESE DRAWINGS ARE THE PROPERTY OF XYCOM AND SHALL NOT BE REPRODUCED OR COPIED WITHOUT EXPRESSED WRITTEN AUTHORIZATION FROM XYCOM.
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TITLE
SCHEMATIC
XVME 682 CPU
SCALE —
SHEET 7 OF 16
DWG. NO. 72682B-100
RESTRICTED DRAWINGS 72682A-100
SPEC. SCH. NOT MFR.

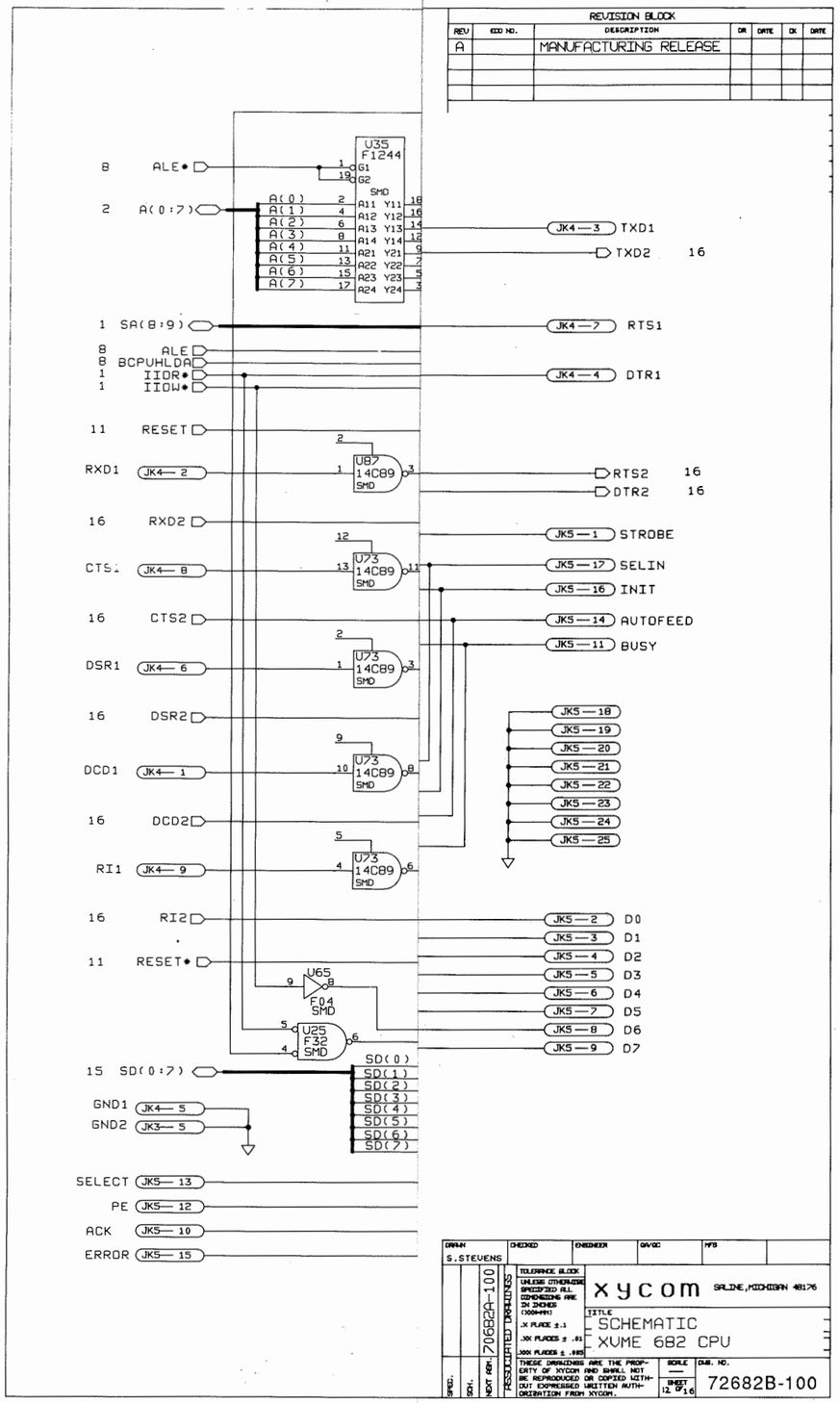

REVISION BLOCK
REV
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
A
MANUFACTURING RELEASE
1 SA(0:19)
RA(8:9) 13
9 SLAVE
2 A(0:23)
+5V
R94
10K
SMD
U85
F74
SMD
PR
D
Q
CK
CLR
1 SYSCLK
STDADD* 7
SIDADD* 7
1 REF*
9 DPSTB*
SLVACK 9
1 MMEMR*
1 MMEMW*
2 CPUHLDA
U71
F32
SMD
SYSALE 5
LCPUA16 7
ADDRSEL 2
BCPUHLDA 7,9,10,12
LMEGCS* 1,7
MDBEN* 3
PAREN 3
PROMADD* 5,7
LCODE 7
AF16* 1
CASEN 13
CAS0* 13
CAS1* 13
CAS3* 13
CAS2* 13
R37
10K
SMD
2 CODINTA
1 XA(0)
1 XBHE*
1 XMEMW*
7 VBDS1*
7 VBDS0*
7 VBWRITE*
RAS0* 13
R106
33 SMD
RAS1* 13
+5V
RAMWE* 13
MDPOUT1 13
MDPOUT0 13
2 S1*
2 S0*
U41
F00
SMD
TS 3
ALE 1,2,12
ALE* 12
1 PROCCLK
1 RESET4*
DRAWN
S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XXX=MM)
.X PLACE ± .1
.XX PLACES ± .01
.XXX PLACES ± .005
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TITLE
SCHEMATIC
XVME 682 CPU
SCALE —
DWG. NO.
72682B-100
SHEET 8 OF 16
SPEC.
SDV.
NEXT ASM.
72682A-100
ASSOCIATED DRAWINGS


REVISION BLOCK
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DR
DATE
CK
DATE
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MANUFACTURING RELEASE
HRQ1201 1
DMAEN204* 2
SLAVE 3,8
IOCHRDY 15
4 HRQ1206
8 BCPUHLDA
1 DMAEN*
11 RESET
1 HLDA1201
IOCHRDY206 4
4 CLK206
+5V
R74
10K
SMD
HLDA1206 3,4
C13
27PF
SMD
7 VBWRITE*
6 BDSEL
U52
F74
SMD
PR
CLR
LEA* 5
SAE* 5
7 VBAS*
U61
F04
SMD
VDEN* 5,7
DPSTB* 8,14
7 DEN*
U63
F38
SMD
VDTACK* 11
8 SLVACK
DRAWN
S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XXMM)
.X PLACE ±.1
.XX PLACES ± .01
.XXX PLACES ± .005
xycom SALINE,MICHIGAN 48176
TITLE
SCHEMATIC
XVME 682 CPU
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SCALE

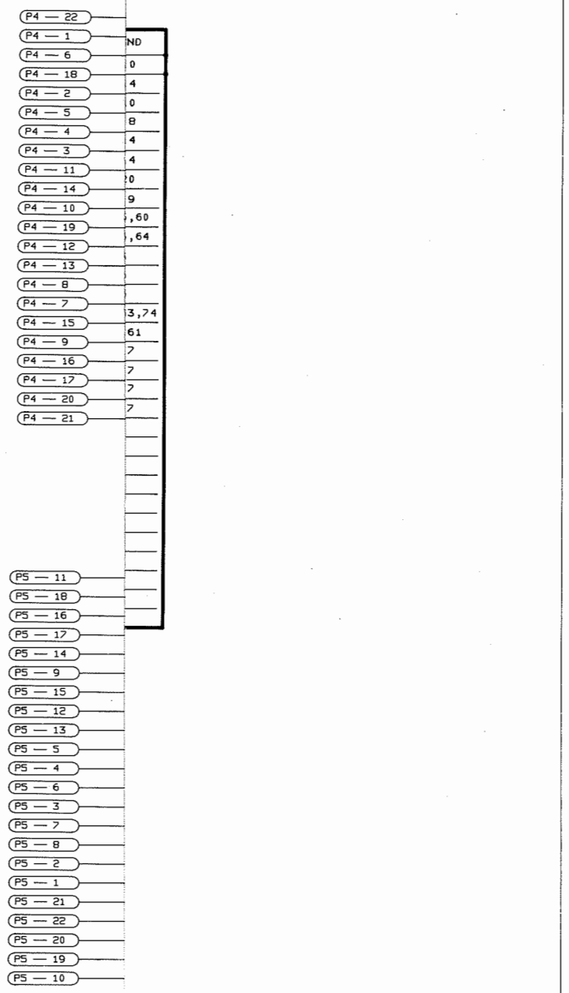
SHEET
9 OF 16
DWG. NO.
72682B-100
ASSOCIATED DRAWINGS
NEXT ASM
72682A-100
ASM.
SPEC.


REVISION BLOCK
REV
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
A
MANUFACTURING RELEASE
1 XD(0:7)
3 PPICS*
1 ENAS*
1 Q1WS
1 XIOW*
1 XIOR*
1 XA(0:10)
8 BCPUHLDA
11 RESET*
RTCAS 4
NMICS* 1,14
PORTBRD* 1
PORTBWR* 1
8042CS* 4
RDSTAT2* 14
VMIADD* 5
RDSTAT1* 14
FAIL* 14
PASS 14
VMEREQ 7
ACABEN 14
WSEL0 7
WSEL1 7
LINTEN 14
IRQ1* P1B-30 J23
IRQ2* P1B-29 J22
IRQ3* P1B-28 J21
IRQ4* P1B-27 J24
IRQ5* P1B-26 J19
IRQ6* P1B-25 J18
IRQ7* P1B-24 J17
J26
14 DPINT*
IRQ10 15
IRQ11 15
IRQ12 15
IRQ15 15
WDTERR* 14
DRAWN S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (1000=mm)
.X PLACE ±.1
.XX PLACES ± .01
.XXX PLACES ± .005
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TITLE
SCHEMATIC
XVME 682 CPU
SCALE —
SHEET 10 OF 16
DWG. NO.
72682B-100
ASSOCIATED DRAWINGS
72682A-100
NEXT ASSY.
USED
SPEC.


REVISION BLOCK
REV
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
A
MANUFACTURING RELEASE
+5V
J63
R123
1K
R108
75 SMD
C886
.1UF
SMD
R79
23.3K
1%SMD
R78
2.61K
1%SMD
CR1
1N5819
5V
PWRGD 4
P1C — 12 SYSRESET*
VBU 4
SW2
NC
C
NO
P1B — 31 +5V STDBY
4B
IACKIN* P1A — 21
P1A — 22 IACKOUT*
7 VBAS*
7 VBR3*
6 VMEDS
VBGIN3* 7
RESET1* 1
RESET 6,7,9,12
RESET* 1,7,10,12,14
9 VDTACK*
7 VBBSY*
DTACK* P1A — 16
BERR* P1C — 11
VBDTACK* 6,7
VBBERR* 6,7
P1A — 10 SYSCLK
16MHZ 1,6,7
16 MHZ
U68
U64
F04
SMD
1 PCLK
DRAWN
S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XXX=MM)
.X PLACE ± .1
.XX PLACES ± .01
.XXX PLACES ± .005
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ASSOCIATED DRAWINGS
706B2A-100
NEXT ASM.
SCH.
SPEC.
xycom SALINE, MICHIGAN 48176
TITLE
SCHEMATIC
XVME 682 CPU
SCALE
SHEET 11 OF 16
DWG. NO.
72682B-100


REVISION BLOCK
REV | ECO NO. | DESCRIPTION | DR | DATE | CK | DATE
A | | MANUFACTURING RELEASE
U35 F1244 SMD
ALE*
A(0:7)
SA(8:9)
ALE
BCPUHLDA
IIOR*
IIOW*
RESET
RXD1
RXD2
CTS1
CTS2
DSR1
DSR2
DCD1
DCD2
RI1
RI2
RESET*
SD(0:7)
GND1
GND2
U87 14C89 SMD
U73 14C89 SMD
U65 F04 SMD
U25 F32 SMD
JK4—3 TXD1
TXD2 16
JK4—7 RTS1
JK4—4 DTR1
RTS2 16
DTR2 16
JK5—1 STROBE
JK5—17 SELIN
JK5—16 INIT
JK5—14 AUTOFEED
JK5—11 BUSY
JK5—18
JK5—19
JK5—20
JK5—21
JK5—22
JK5—23
JK5—24
JK5—25
JK5—2 D0
JK5—3 D1
JK5—4 D2
JK5—5 D3
JK5—6 D4
JK5—7 D5
JK5—8 D6
JK5—9 D7
SELECT JK5—13
PE JK5—12
ACK JK5—10
ERROR JK5—15
DRAWN S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
.X PLACE ±.1
.XX PLACES ± .01
.XXX PLACES ± .005
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TITLE
SCHEMATIC
XVME 682 CPU
SCALE —
SHEET 12 OF 16
DWG. NO. 72682B-100
72682A-100
ASSOCIATED DRAWINGS
SPEC.
SCH.
NOT REL

REVISION BLOCK						
REV	ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
A		MANUFACTURING RELEASE				



DRAWN: S.STEVENS	CHECKED	ENGINEER	QA/QC	MFG	

TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (XXX=MM)
.X PLACE ± .1
.XX PLACES ± .01
.XXX PLACES ± .005

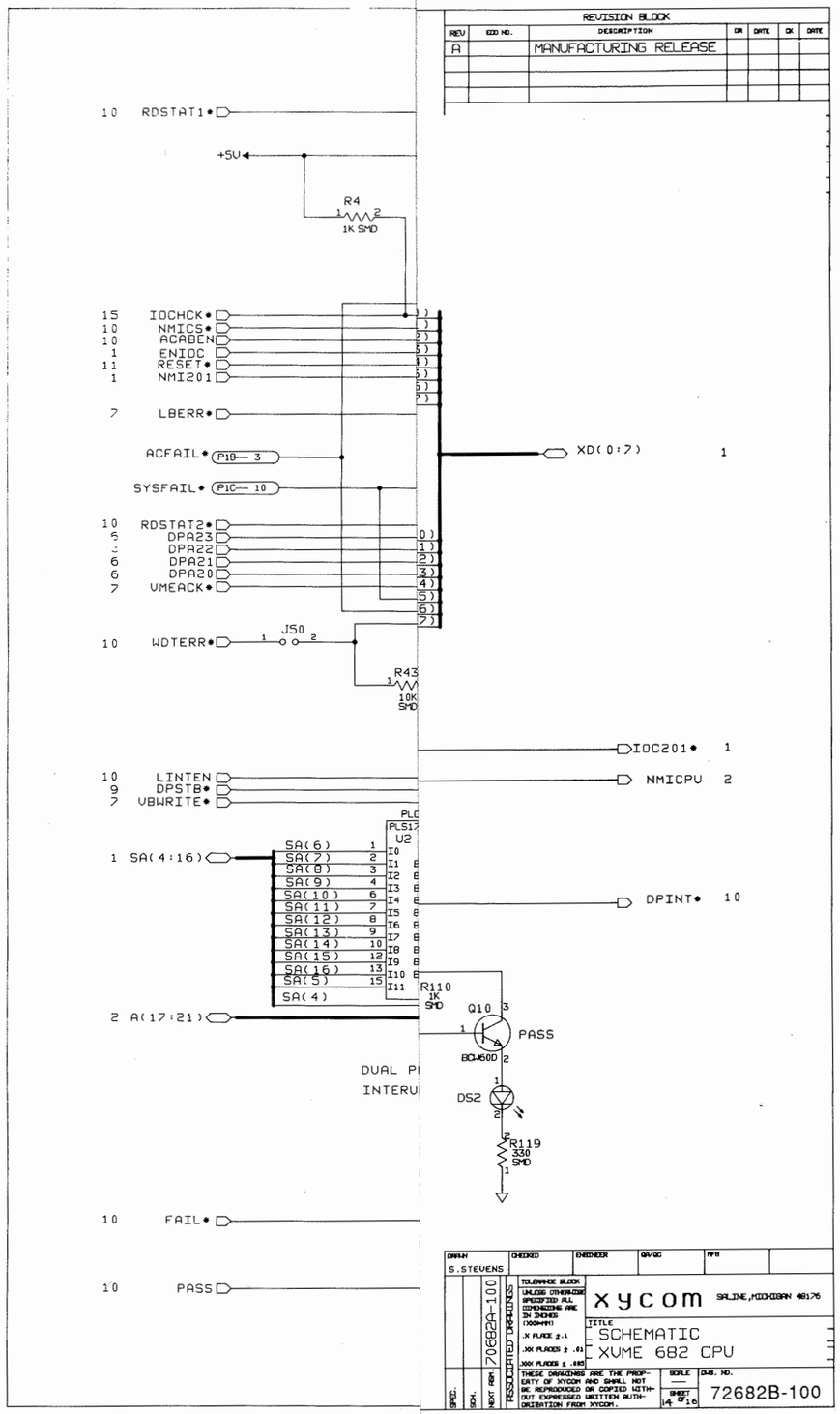
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TITLE
SCHEMATIC
XVME 682 CPU

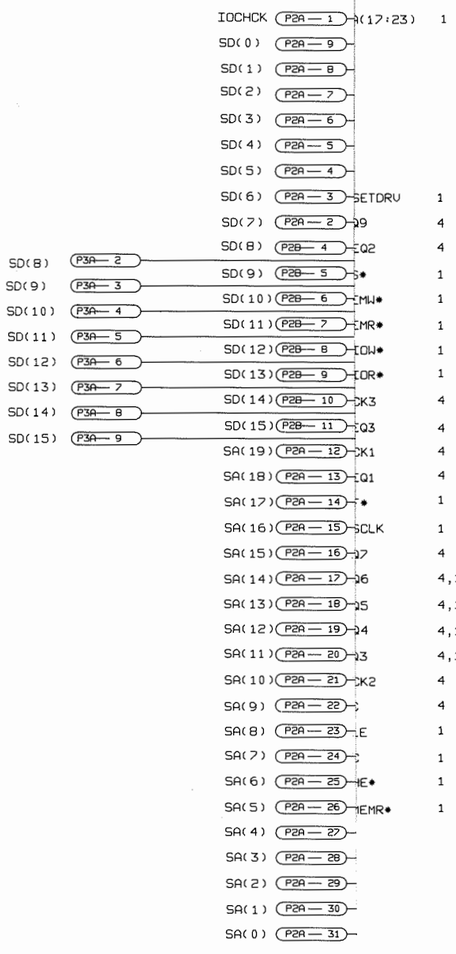
SIZE: D | SCH.: 7 | NEXT ASM.: 72682A-100 | RESTRICTED DRAWINGS

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SCALE: —
SHEET 13 OF 16
DWG. NO. 72682B-100


REVISION BLOCK
REV
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
A
MANUFACTURING RELEASE
10 RDSTAT1*
+5V
R4
1K SMD
15 IOCHCK*
10 NMICS*
10 ACABEN
1 ENIOC
11 RESET*
1 NMI201
7 LBERR*
ACFAIL* P1B-3
SYSFAIL* P1C-10
XD(0:7)
1
10 RDSTAT2*
DPA23
DPA22
DPA21
DPA20
7 VMEACK*
10 WDTERR*
JS0
R43
10K SMD
IOC201*
1
10 LINTEN
9 DPSTB*
7 VBWRITE*
NMICPU
2
1 SA(4:16)
SA(6)
SA(7)
SA(8)
SA(9)
SA(10)
SA(11)
SA(12)
SA(13)
SA(14)
SA(15)
SA(16)
SA(5)
SA(4)
DPINT*
10
R110
1K SMD
Q10
PASS
BCW60D
2 A(17:21)
DS2
R119
330 SMD
10 FAIL*
10 PASS
DRAWN
S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
xycom
SALINE, MICHIGAN 48176
TITLE
SCHEMATIC
XVME 682 CPU
SIZE
DWG. NO.
72682B-100
SHEET
4 OF 16
706822A-100
RESTRICTED DRAWINGS
NEXT ASM.
SCH.
BMED.

REVISION BLOCK						
REV	ECO NO.	DESCRIPTION	DR	DATE	CK	DATE
A		MANUFACTURING RELEASE				



DRAWN	CHECKED	ENGINEER	QA/QC	MFG	
S.STEVENS					

TOLERANCE BLOCK
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.X PLACE ±.1
.XX PLACES ± .01
.XXX PLACES ± .005

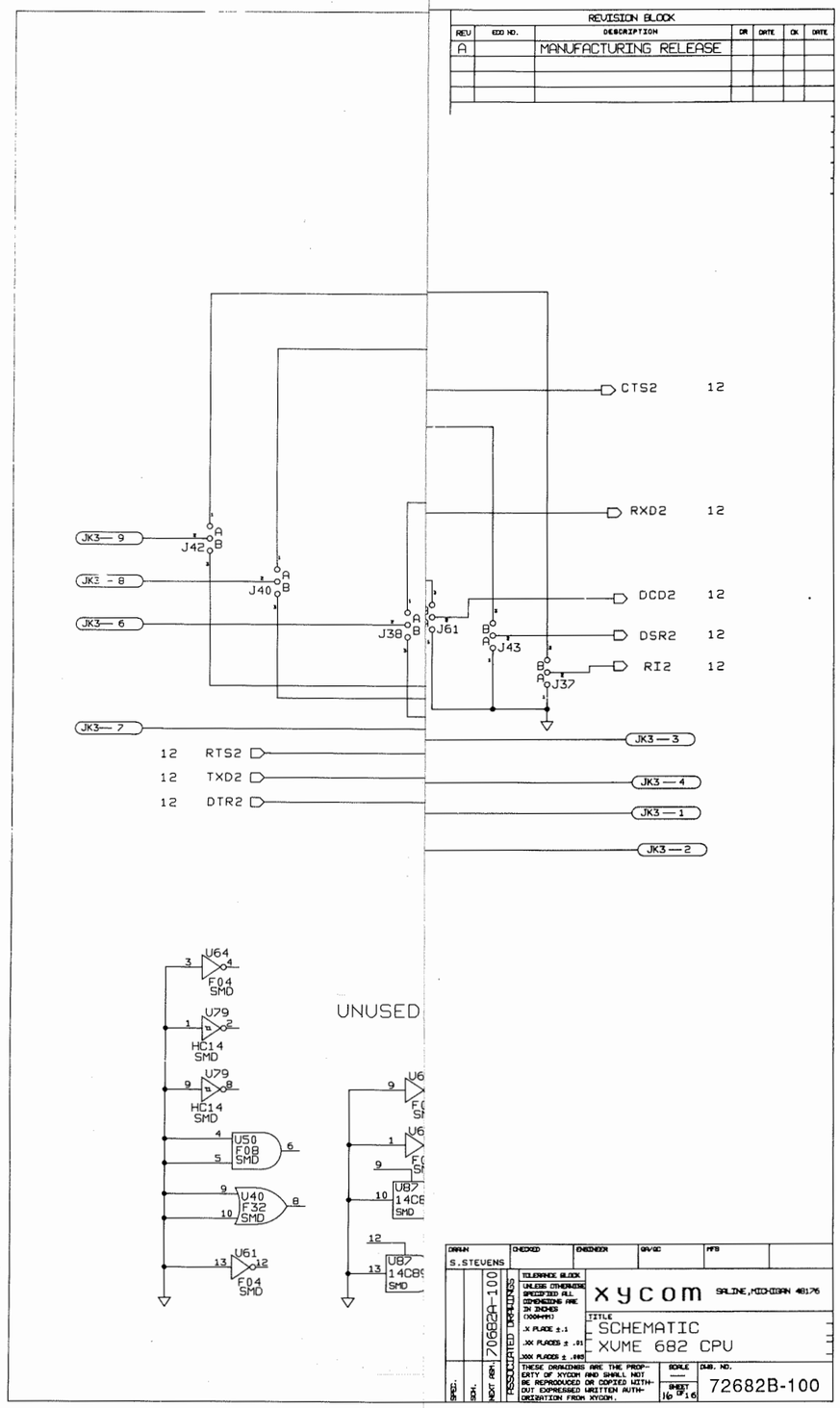
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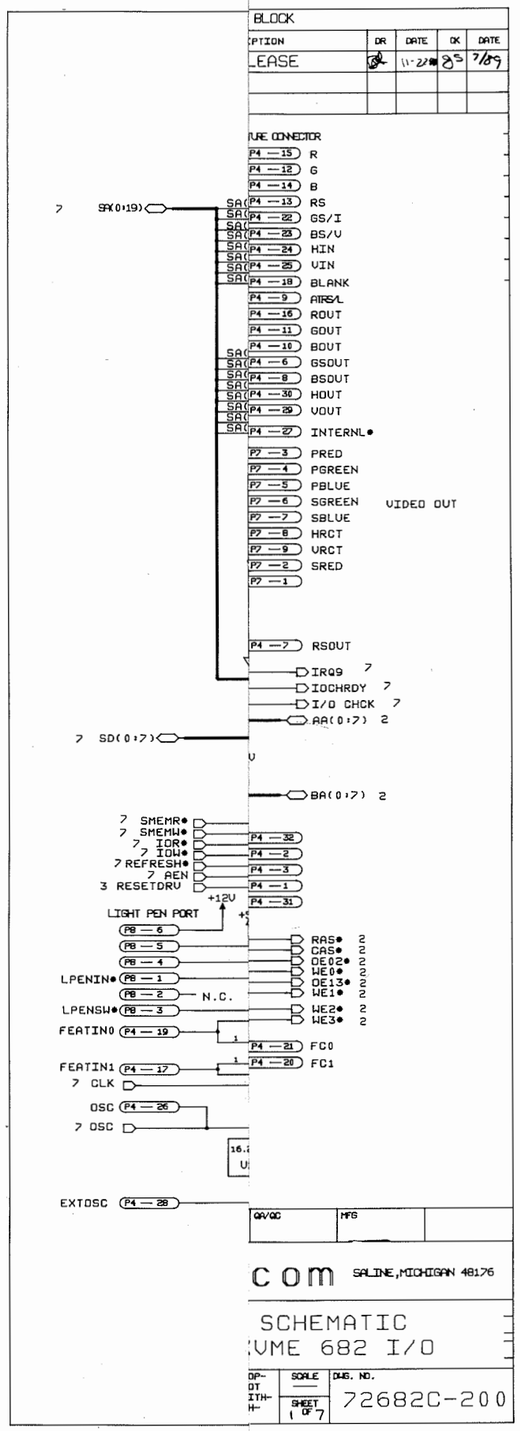
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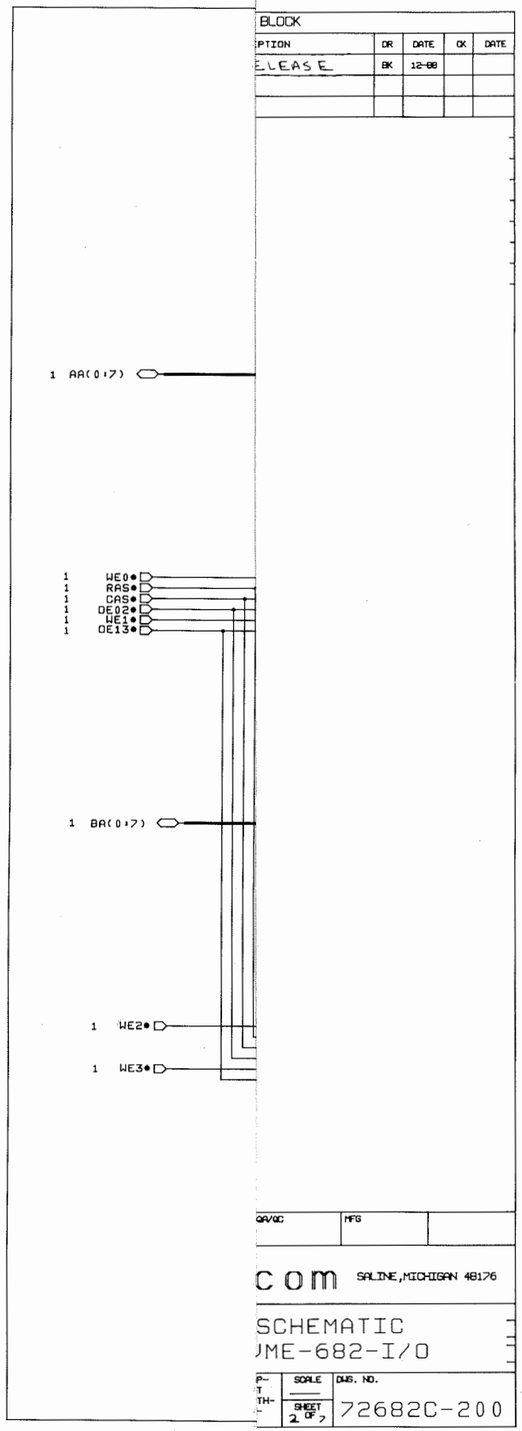
TITLE
SCHEMATIC
XVME 682 CPU

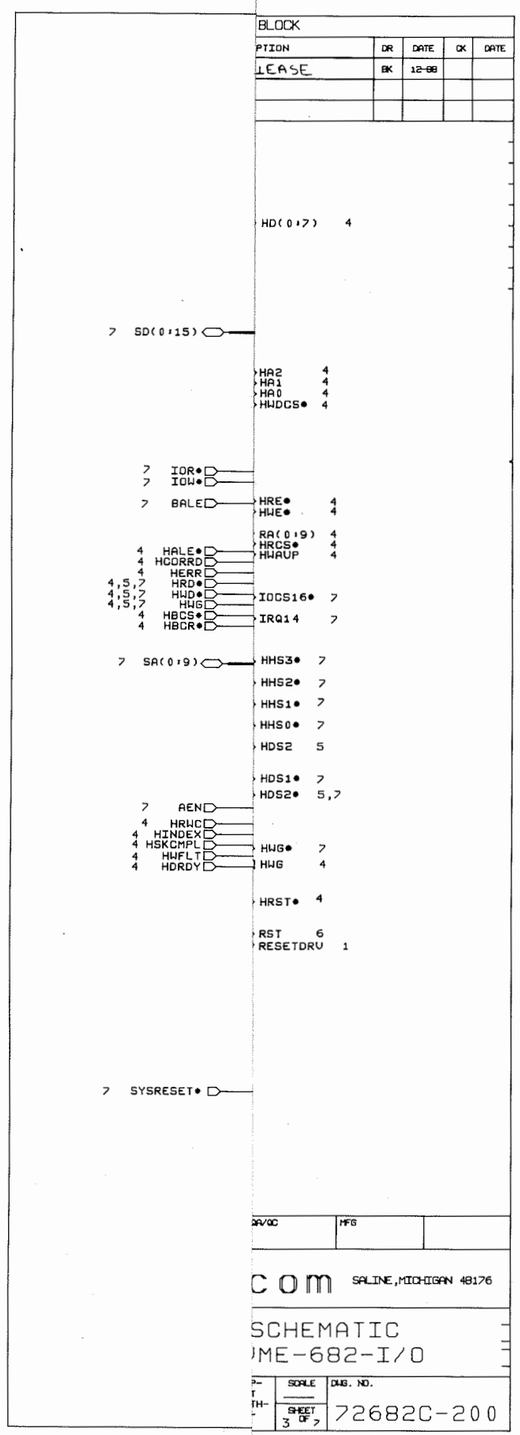
SIZE: D | DSH: 70682A-100 | NEXT ASH: | RESOLICITED DRAWINGS

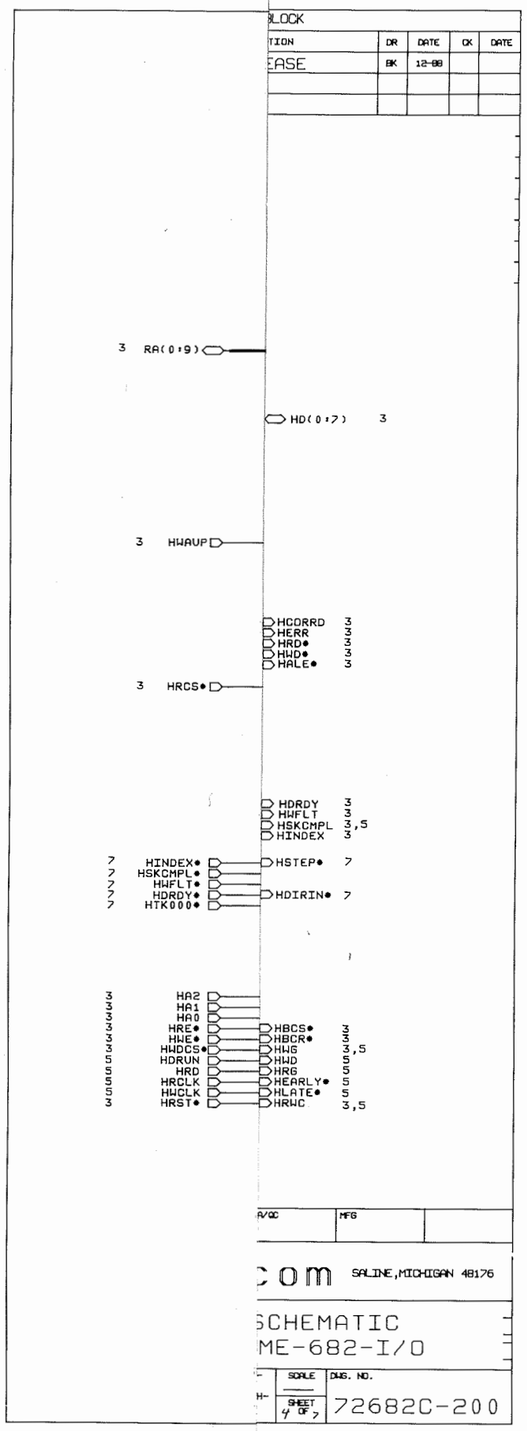
SCALE: —
SHEET 15 OF 16
DWG. NO. 72682B-100

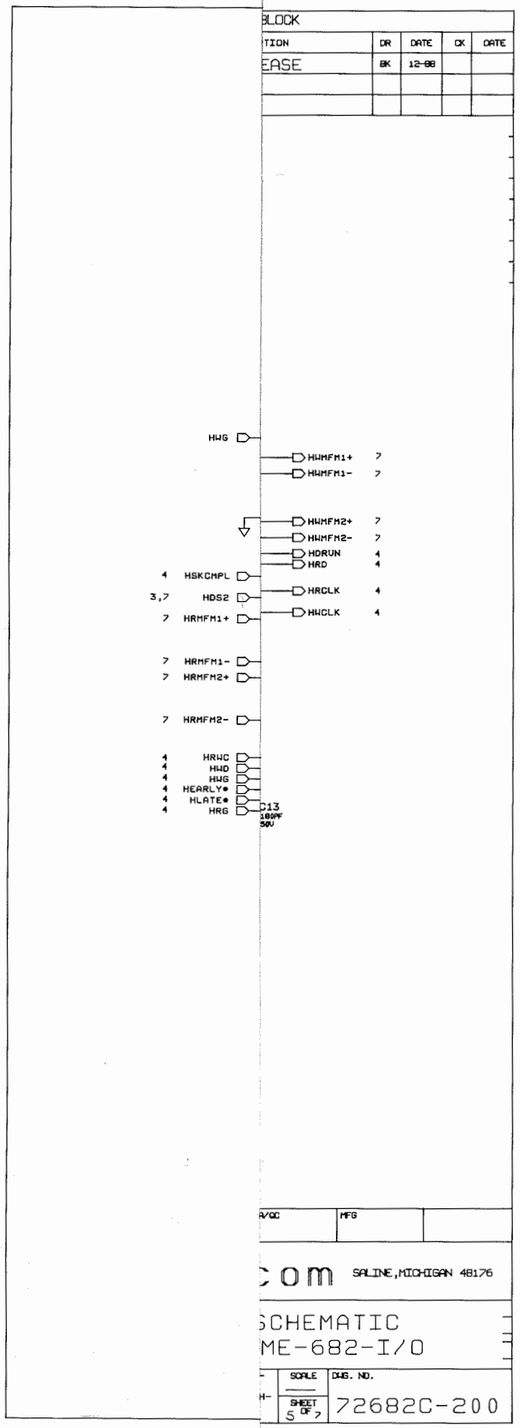

REVISION BLOCK
REV
ECO NO.
DESCRIPTION
DR
DATE
CK
DATE
A
MANUFACTURING RELEASE
CTS2 12
RXD2 12
DCD2 12
DSR2 12
RI2 12
JK3— 9
JK3 — 8
JK3— 6
JK3— 7
J42
J40
J38
J61
J43
J37
12 RTS2
12 TXD2
12 DTR2
JK3 — 3
JK3 — 4
JK3 — 1
JK3 — 2
U64
F04
SMD
U79
HC14
SMD
U50
F08
SMD
U40
F32
SMD
U61
F04
SMD
UNUSED
DRAWN
S.STEVENS
CHECKED
ENGINEER
QA/QC
MFG
TOLERANCE BLOCK
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES (MMM=M)
.X PLACE ±.1
.XX PLACES ± .01
.XXX PLACES ± .005
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SALINE, MICHIGAN 48176
TITLE
SCHEMATIC
XVME 682 CPU
SIZE
B
DWG NO.
72682B-100
SCALE
—
SHEET
16 OF 16
72682A-100
RESTRICTED DRAWINGS
DO NOT REPRODUCE

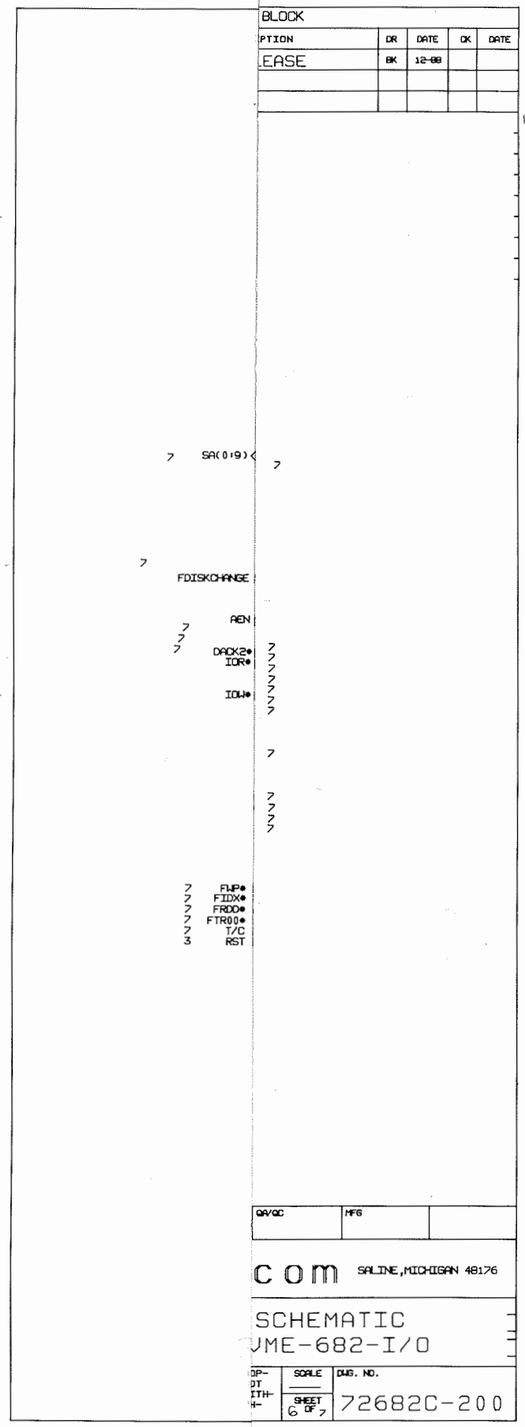

BLOCK
DR
DATE
CK
DATE
LEASE
URE CONNECTOR
P4 — 15 R
P4 — 12 G
P4 — 14 B
P4 — 13 RS
P4 — 22 GS/I
P4 — 23 BS/V
P4 — 24 HIN
P4 — 25 VIN
P4 — 18 BLANK
P4 — 9 AIRSL
P4 — 16 ROUT
P4 — 11 GOUT
P4 — 10 BOUT
P4 — 6 GSOUT
P4 — 8 BSOUT
P4 — 30 HOUT
P4 — 29 VOUT
P4 — 27 INTERNL•
P7 — 3 PRED
P7 — 4 PGREEN
P7 — 5 PBLUE
P7 — 6 SGREEN
VIDEO OUT
P7 — 7 SBLUE
P7 — 8 HRCT
P7 — 9 VRCT
P7 — 2 SRED
P7 — 1
P4 — 7 RSOUT
7 SA(0:19)
IRQ9 7
IOCHRDY 7
I/O CHCK 7
AA(0:7) 2
7 SD(0:7)
BA(0:7) 2
7 SMEMR•
7 SMEMW•
7 IOR•
7 IOW•
7 REFRESH•
7 AEN
3 RESETDRV
P4 — 32
P4 — 2
P4 — 3
P4 — 1
P4 — 31
+12V
LIGHT PEN PORT
P8 — 6
P8 — 5
P8 — 4
P8 — 1
P8 — 2
N.C.
P8 — 3
LPENIN•
LPENSW•
RAS• 2
CAS• 2
OE02• 2
WE0• 2
OE13• 2
WE1• 2
WE2• 2
WE3• 2
FEATIN0 P4 — 19
FEATIN1 P4 — 17
P4 — 21 FC0
P4 — 20 FC1
7 CLK
OSC P4 — 26
7 OSC
EXTOSC P4 — 28
QA/QC
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SCHEMATIC
VME 682 I/O
SCALE
DWG. NO.
72682C-200
SHEET
OF 7

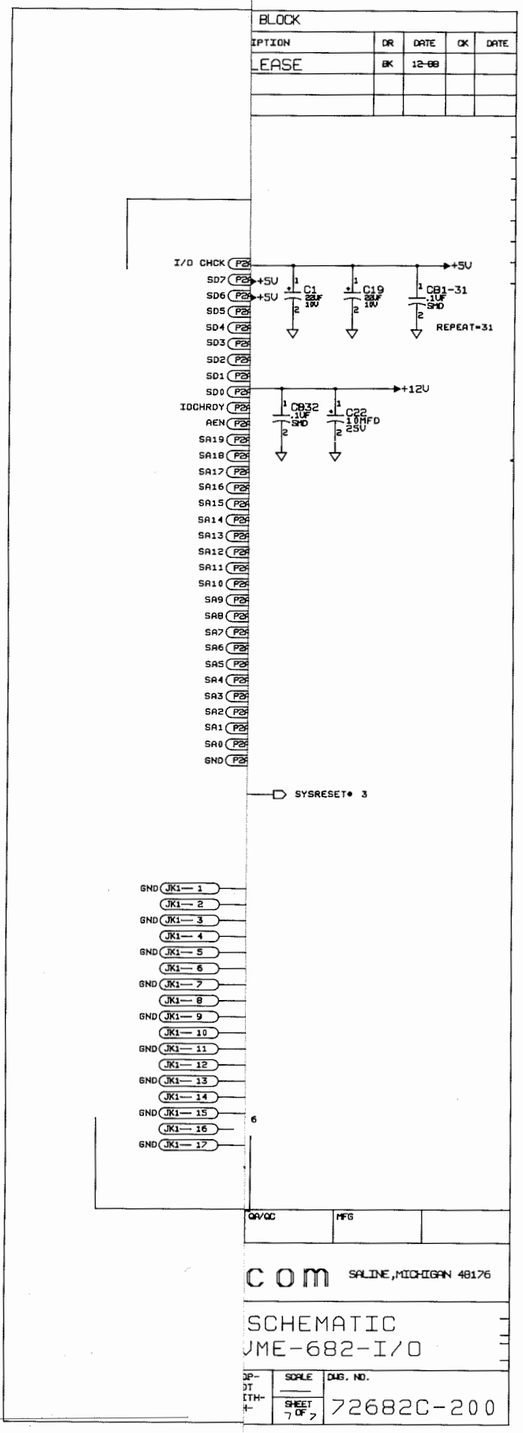

BLOCK
PTION
DR
DATE
CK
DATE
ELEASE
BK
12-88
1 AA(0:7)
1 WE0*
1 RAS*
1 CAS*
1 OE02*
1 WE1*
1 OE13*
1 BA(0:7)
1 WE2*
1 WE3*
QA/QC
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SALINE,MICHIGAN 48176
SCHEMATIC
JME-682-I/O
SCALE
SHEET 2 OF 7
DWG. NO.
72682C-200


BLOCK
PTION
DR
DATE
CK
DATE
LEASE
BK
12-88
HD(0:7) 4
7 SD(0:15)
HA2 4
HA1 4
HA0 4
HWDCS● 4
7 IOR●
7 IOW●
7 BALE
HRE● 4
HWE● 4
RA(0:9) 4
HRDS● 4
HWAUP 4
4 HALE●
4 HCORRD
4 HERR
4,5,7 HRD●
4,5,7 HWD●
4,5,7 HWG
4 HBCS●
4 HBDR●
IOCS16● 7
IRQ14 7
7 SA(0:9)
HHS3● 7
HHS2● 7
HHS1● 7
HHS0● 7
HDS2 5
HDS1● 7
HDS2● 5,7
7 AEN
4 HRWC
4 HINDEX
4 HSKCMPL
4 HWFLT
4 HDRDY
HWG● 7
HWG 4
HRST● 4
RST 6
RESETDRV 1
7 SYSRESET●
MFG
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SALINE,MICHIGAN 48176
SCHEMATIC
ME-682-I/O
SCALE
SHEET 3 OF 7
DWG. NO.
72682C-200


BLOCK
TION | DR | DATE | CK | DATE
EASE | BK | 12-88
3 RA(0:9)
HD(0:7) 3
3 HWAVP
HCORRD 3
HERR 3
HRD• 3
HWD• 3
HALE• 3
3 HRCS•
HDRDY 3
HWFLT 3
HSKCMPL 3,5
HINDEX 3
7 HINDEX• HSTEP• 7
7 HSKCMPL•
7 HWFLT•
7 HDRDY• HDIRIN• 7
7 HTK000•
3 HA2
3 HA1
3 HA0
3 HRE• HBCS• 3
3 HWE• HBCR• 3
3 HWDCS• HWS 3,5
5 HDRUN HWD 5
5 HRD HRG 5
5 HRCLK HEARLY• 5
5 HWCLK HLATE• 5
3 HRST• HRWC 3,5
A/QC | MFG
com SALINE,MICHIGAN 48176
SCHEMATIC
ME-682-I/O
SCALE | DWG. NO.
SHEET 4 OF 7 | 72682C-200


BLOCK
TION
DR
DATE
CK
DATE
EASE
BK
12-88
HWG
HWMFM1+ 7
HWMFM1- 7
HWMFM2+ 7
HWMFM2- 7
HDRUN 4
HRD 4
4 HSKCMPL
3,7 HDS2
7 HRMFM1+
HRCLK 4
HWCLK 4
7 HRMFM1-
7 HRMFM2+
7 HRMFM2-
4 HRWC
4 HWD
4 HWG
4 HEARLY*
4 HLATE*
4 HRG
C13
.10UF
50V
A/QC
MFG
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SCHEMATIC
ME-682-I/O
SCALE
DWG. NO.
SHEET 5 OF 7
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BLOCK
PTION
DR
DATE
CK
DATE
EASE
BK
12-88
SA(0:9)
FDISKCHANGE
AEN
DACK2*
IOR*
IOW*
FWP*
FIDX*
FRDD*
FTR00*
T/C
RST
QA/QC
MFG
com
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SCHEMATIC
VME-682-I/O
SCALE
DWG. NO.
SHEET 6 OF 7
72682C-200


BLOCK
IPTION
DR
DATE
CK
DATE
LEASE
BK
12-88
I/O CHCK
SD7
SD6
SD5
SD4
SD3
SD2
SD1
SD0
IOCHRDY
AEN
SA19
SA18
SA17
SA16
SA15
SA14
SA13
SA12
SA11
SA10
SA9
SA8
SA7
SA6
SA5
SA4
SA3
SA2
SA1
SA0
GND
+5V
+12V
C1
C19
C81-31
.1UF
SMD
REPEAT=31
C832
C22
18MFD
25V
SYSRESET* 3
JK1-- 1
JK1-- 2
JK1-- 3
JK1-- 4
JK1-- 5
JK1-- 6
JK1-- 7
JK1-- 8
JK1-- 9
JK1-- 10
JK1-- 11
JK1-- 12
JK1-- 13
JK1-- 14
JK1-- 15
JK1-- 16
JK1-- 17
6
QA/QC
MFG
com
SALINE,MICHIGAN 48176
SCHEMATIC
VME-682-I/O
SCALE
SHEET
7 OF 7
DWG. NO.
72682C-200

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