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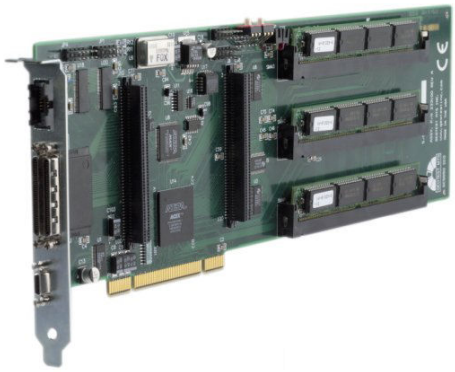
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Find the *Marvin Test Sets / Geotest GC5050* at our website: *Click HERE*

# GC5050

## DYNAMICALLY CONTROLLED HIGH SPEED DIGITAL I/O PCI CARD

- 32 bi-directional I/O pins (16 cards may be daisy-chained for a total of 512 pins)
- 3 MB or 12 MB of on-board memory
- External and programmable internal clock rates from 5 Hz to 50 MHz
- Dynamically controlled sequencer supports branching,looping, & subroutines
- Multiple I/O options: TTL, PECL, LVDS, and Programmable levels
- Includes a graphical vector development environment (DIOEasy) for generating,editing, capturing, and comparing complex digital patterns



## DESCRIPTION

The GC5050 is a high speed Dynamic Digital I/O card that provides capabilities comparable to high speed I/O products found in large functional test systems. The card shares an identical architecture with the GX5050, a 6U PXI card. Both have the ability to operate independently of the host computer when in the RUN mode.

## FEATURES

The GC5050 provides real-time digital stimulus and capture with 32 pins per card. Up to 16 cards can be daisy-chained for a total of up to 512 pins. The 32 pins can be configured as input or output groups of eight. The direction of each group can be changed dynamically with the sequencer, externally, or both. There is also a 16-bit external bus for triggering and synchronization with external events.

Clock and strobe signals are distributed to the cards via a daisy-chained ribbon cable. These signals can be generated internally or externally. The external control signals allow full synchronization with the unit under test (UUT) and minimize the initialization part of the test.

### Algorithmic Sequencer Technology (AST™)

An innovative, state-of-the-art algorithmic sequencer allows users to create loops and branches to manipulate the output vectors. All of the sequencer commands can be conditioned using the External Event bus and may be programmed using the Graphical Vector Editor using Windows® API commands or via a script language. This gives the GC5050 the capability to generate test vectors indefinitely at maximum test rates. Internal and external trigger and pause commands are available in several modes.

### On-Board Memory

The on-board memory is configurable from 3 MB or 12 MB and is user upgradeable. Separate memories are provided for output data, response data, and test step sequencing commands. The separate memory for response data lets the application read the activity on the UUT pins independent of the bi-directional mode. This is an important feature lacking in most high speed digital I/O applications.

### Compatibility

The GC5050 operates in any full size PCI slot that provides both 3.3 V and 5 V power supplies and are compatible with the Marvin Test Solutions GT50 and GT25 boards Test vectors. Additionally, firmware can be upgraded using the unique In-System-Programming front panel.

## I/O MODULES

The GC5050 offers a variety of I/O modules with input and output levels that meet the requirement of any digital test application, including TTL, PECL, ECL, Programmable Levels, LVDS, and custom modules. I/O module type and memory size must be specified at the time the GC5050 is ordered.

| I/O Modules | Channels | Levels |
|---|---|---|
| TTL | 32 | 5 V and 3.3 V logic |
| PECL | 32 | Positive ECL |
| LVDS | 32 | LVDS |
| Programmable Levels | 32 | 0.3 V to 9 V |

## CONFIGURATION

The GC5050 can be configured as a Master or as a Slave. The Master provides timing signals for up to 15 Slaves.

DIGITAL I/O


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# GC5050

## PROGRAMMING AND SOFTWARE

The board is supplied a 32-bit DLL driver. Various interface files provide access to the DLL from programming tools and languages such as ATEasy, LabVIEW, C/C++, Microsoft Visual Basic®, Delphi, and more. The available virtual panel can be used to interactively adjust and control the instrument from a window that displays the current instrument settings and measurements.

On-Line help file and PDF User's Guide provides documentation that includes instructions for installing, using and programming the board.

## APPLICATIONS

- Automatic Test Equipment (ATE)
- High-speed functional digital test
- Vector capture
- Hybrid and digital device test
- Memory testing
- Event sequencer, logic pattern capture

## SPECIFICATIONS

| TIMING | |
|---|---|
| Internal Test Clock | 5 Hz to 50 MHz |
| Resolution | 1 Hz or 0.01% (whichever is greater) |
| Auxiliary Internal Clock B | 1 MHz to 100 MHz |
| Resolution | 1 Hz or 0.2% (whichever is greater) |
| Internal Strobe | 10 to 25 ns before next clock |
| External Test Clock | 0 to 50 MHz |
| Skew | 3 ns max on the same card<br>5 ns max between cards |
| **I/O** | |
| The I/O levels are I/O module dependant. I/O modules support TTL, PECL, LVDS, and Programmable Levels | |
| Number of I/O Channels | 32 per Card |
| Direction | Input or Output per step (in groups of eight) |
| Memory | 256 Kb to1 Mb per I/O pin (UMbit optional) |
| Triggering | Software generated trigger<br>External Input trigger override<br>Conditional triggering (Conditioned by one or two sequential external events) |
| Pause | Software generated pause<br>External Input pause override<br>Conditional pause (Conditioned by an external event)<br>Sequencer Pause command |
| **EXTERNAL CONTROL AND STATUS** | |
| Output Enable | Tri-state control for groups of eight (8) I/O pins |
| External Clock Enable | Internal, external clock selection |
| Clock Output | The selected clock |
| External Strobe | The selected strobe |
| Pause | External pause override input |
| Trigger | External trigger override input |
| Run | Run indicator output |
| B Clock | Auxiliary clock output |
| $V_{CC}$ | +5 $V_{DC}$ output |
| **ENVIRONMENTAL** | |
| Operating Temperature | 0 °C to +50 °C |
| Storage Temperature | -20 °C to +70 °C |
| Vibration | 5 g @ 500 Hz |
| Shock | 10 g for 6 ms ½ sine |
| Size | Full size PCI slot |
| Weight | 1.2 lbs (520 g) |
| **CONNECTIONS** | |
| Timing | 68 position SCSI III Type |
| I/O Module | 68 position SCSI III Type |
| Control | 14 position SCSI III Type |

Note: Specifications are subject to change without notice



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# GC5050

## ORDERING INFORMATION

| | |
|---|---|
| **GC5050-256K** | Dynamic Digital I/O Master/Slave (PCI), 32 Channels up to 50 MHz w/256 Kb Channel Memory and a Mating Cable. Requires One GC59XX I/O Module |
| **GC5050-1M** | Dynamic Digital I/O Master/Slave (PCI), 32 Channels up to 50 MHz w/1 Mb Channel Memory and a Mating Cable. Requires One GC59XX I/O Module |
| **I/O MODULE (SELECT ONE)** | |
| **GC5910** | TTL I/O Module for GC5050 Boards, 32 TTL Channels at up to 50MHz |
| **GC5910-5V** | TTL I/O Module for GC5050 Boards, 32 5V TTL Channels at up to 50MHz |
| **GC5930** | Programmable Levels I/O Module for GC5050 boards, 32 channels at up to 50MHz |
| **GC5960** | LVDS I/O Module for GC5050 boards, 32 differential LVDS channels at up to 50MHz |
| **SOFTWARE** | |
| **DIOEasy** | Digital I/O control software including a vector generator and vector comparison |
| **DIOEasy-DS** | 2 days DIOEasy training at Marvin Test Solutions (Irvine, CA) for 1-3 persons. Call for larger groups. |
| **DIOEasy-DS2** | On-site, 2-days DIOEasy training seminars for 1-3 persons. Call for larger groups. |
| **ACCESSORY** | |
| **GT95014** | Connector Interface for GT5xxx/GX5xxx/GC5xxx, SCSI to 100 Mil Grid, Single Ended |
| **GT95015** | Connector Interface for all 5xxx/35xx, SCSI to 100 Mil Grid, Differential |
| **GT95020** | Connector I/F for 5xxx/35xx products, SCSI to 100 Mil Grid, Single Ended (both 68 & 14 pin) |
| **GT95021** | 2' shielded cable for 5xxx/35xx products (68 Pin) |
| **GT95022** | 3' shielded cable for 5xxx/35xx products (68 Pin) |
| **GT95022E** | 3' shielded cable for 5xxx/35xx products (68 Pin) not terminated one end |
| **GT95028** | 10' shielded cable for 5xxx/35xx products (68 Pin) |
| **GT95031** | 6' shielded cable for 5xxx/35xx products (68 Pin) |
| **GT95032** | 6" Shielded Cable for all 5xxx/35xx (68 Pin) |
| **GT95032-8** | 8" Shielded Cable for all 5xxx/35xx (68 Pin) |
| **GT95032-12** | 12" Shielded Cable for all 5xxx/35xx (68 Pin) |



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