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GTDIO

GT-DIO Product Family

GC5050

Dynamic Digital I/O PCI Card

User's Guide

Last Updated August 14, 2013

MARVIN TEST SOLUTIONS

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Chapter 1 - Introduction

About This User Guide

This User Guide provides information needed to install, configure, program and use Marvin Test Solutions' GC5050 digital I/O (DIO) boards. Supporting boards such as I/O modules, accessories and software are discussed in related User Guides.

Required User Knowledge and Skills

This User Guide assumes a general knowledge of PC-based computers and some knowledge of electronics.

Scope and Organization

The User Guide is organized as follows:

Chapter	Content
Chapter 1	**Introduction** – Introduces this User Guide.
Chapter 2	**Overview** – Summarizes DIO GC5050 family, board features, architecture, hardware and driver.
Chapter 3	**Installation and Setup** – Furnishes step-by-step directions for installing and setting up hardware and installing the driver.
Chapter 4	**Theory of Operation** – Provides a functional hardware description.
Appendix A	**Connectors** – Supplies connector definitions and pin assignments.
Appendix B	**Control Memory Command Micro Code** – Describes the control memory command code.
Appendix C	**Specifications** – Provides a summary of the GC5050's specifications.
Index	Provides a roadmap to important topics and concepts in this manual.

Related Documents

The following documents contain related information and are considered an integral part of this User Guide:

- DIO I/O Modules and Interface User Guide – Information about I/O Modules and supporting hardware.
- DIO Software User Guide and Programming Reference – Information about the DIO Driver, Panel and the ***DIOEasy*** Windows application.

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Style Conventions

Example	Description
Copy or Paste	Commands are indicated in bold type.
Shift+F1	Keys are often used in combination. The example to the left instructs the user to hold down the shift key while pressing the FI key at the same time. When key combination instructions are separated by commas (such as ALT+D, A), hold the ALT key while pressing D, then press A.
Direction Keys	Refer to the up arrow (↑), down arrow (↓), right arrow (→), and left arrow (←) keys.
cd **bold**	Bolded text must be entered from the keyboard exactly as shown.
cd *directory name*	Italicized text is a placeholder for variables or other items the user must define and enter from the keyboard.
`examples`	Examples and source code are indicated in Courier, a fixed pitch font.
0x*hexnumber*	An integer in hexadecimal notation, for example, 0x10A equals 266 in decimal.

Definitions

The following table defines terms commonly used in this document:

Term	Definition
DIO	Digital Input/Output (I/O).
DIO board	Generically, any of Marvin Test Solutions' digital Input/Output circuit boards in any board family. The context could restrict it to the GC5050 family.
GC5050 domain	A system based on GC5050 Master & Slave boards. These include I/O Module daughter boards, and associated cables and software.
Master board	Refers specifically to the G05050 DIO circuit board when used as a Master.
Slave or GC5050 board	Refers specifically to the GC5050 DIO circuit board when used as a Slave.
I/O User Guide	The *DIO I/O Modules and Interface User Guide*
Step	One in a sequence of test intervals. DIO boards run through a programmed sequence of steps.
Software User Guide (or variants)	The *DIO Software User Guide and Programming Reference* provided with GC5050 DIO boards.
Testware	Test software. It includes test vectors loaded and run on the DIO system, as well as driver commands used to load the boards and read results.
Vector or Test vector	A sequence of stimuli applied to the pins of a unit under test.
VHD connector	Very High Density. Used to describe a SCSI 3 type connector with very small pin spacing.

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Chapter 2 - Overview

Introduction

The GC5050 provide real-time digital stimulus and capture with 32 pins per card. Up to 16 cards can be daisy chained for a total of 512 pins. The 32 pins can be configured as input or output in groups of eight. The direction of each group may be changed dynamically within the sequencer, externally, or both.

Clock and strobe signals are distributed to the cards via a daisy-chained ribbon cable. These signals can be generated internally or externally. The external control signals allow full synchronization with the unit under test (UUT) and minimize the initialization part of the test. The algorithmic sequencer lets you create loops and branches to manipulate the output vectors. All of the sequencer commands can be conditioned by using the external event bus. This gives the GC5050 the capability to generate test vectors indefinitely at maximum test rates. Internal and external trigger and pause commands are available in several modes. The on-board memory is configurable from 768KB to 12MB and is user upgradeable. Separate memories are provided for output data, response data, and test step sequencing commands. The separate memory for response data lets the application read the activity on the UUT pins independent of the bi-directional mode. This important feature is lacking in most other high-speed digital I/O cards.

Marvin Test Solutions' DIO is a family of high-speed, programmable, dynamic Digital Input and Output (I/O) boards. These boards perform high-speed automated functional testing, device testing, simulation and data acquisition. The DIO family provides real-time digital pattern capture and generation with 32 channels per card and up to 8 cards or 256 channels.

The DIO family uses common software development tools to develop test vector files. The test vector files contain digital patterns sent to or received from the Unit Under Test (UUT) and specific pre-defined setting for each board in the setting.

Using ***DIOEasy*** or DIO driver functions, the development of vector files can be done without using the actual hardware**.** Vector file verification requires the DIO be installed and properly configured.

Marvin Test Solutions bundles ***DIOEasy*** with all DIO products. ***DIOEasy***, Marvin Test Solutions' vector development and analysis software, allows manual control of the DIO hardware using the built-in DIO Virtual Instrument Panel. The DIO driver permits control of the DIO family from common software development tools such as Marvin Test Solutions' ***ATEasy***, Microsoft Visual Basic, Microsoft Visual C++, Borland C++, Borland Delphi and more.

DIOEasy, a Windows application used to develop digital vectors and does not require any programming experience or knowledge to operate.

Computer Bus Interface

The DIO Driver accesses Master, Slave and carrier boards through the computer's bus (Figure 2-1). The driver can accommodate up to 16 masters (from either family) and each master can have up to 7 DIO slave boards. ISA based DIOs and carrier boards have switches to set their base address to identify by the driver where PCI and PXI boards are using the physical slot number they are installed in to identify by the driver. PXI and PCI boards Master and Slave numbers are set through selector switches located on the front.

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DIO Domains

A DIO domain has one Master DIO board and up to seven DIO Slave boards. A DIO *domain* comprise of Master, its Slaves, Carriers and related modules. Figure 2-1 shows two domains from two different families on a PC bus.

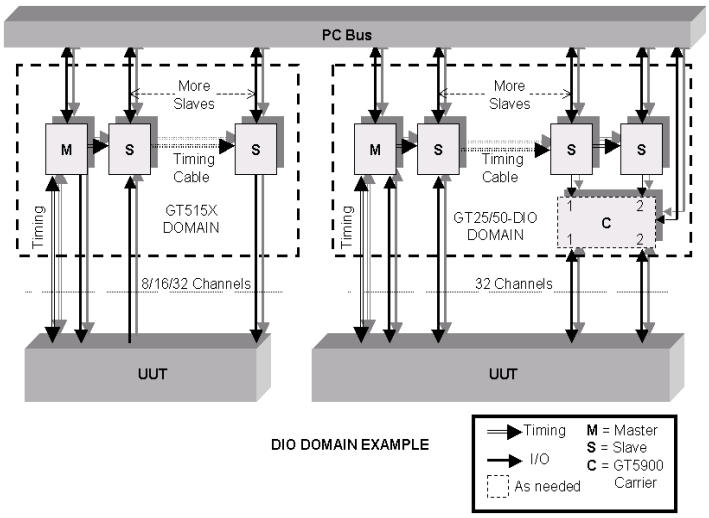


Figure 2-1: Two Different DIO Domains on One PC Bus

Domains are internally synchronized and controlled through a Timing cable binding the Master's Timing connector to all domain Slave boards. To synchronize a domain with a UUT, you need to synchronize the Master board's Timing signals using the Master's Timing connector.

Masters and slaves within a domain must be members of the same product family. Each Slave adds 32 additional UUT I/O channels. Up to seven slaves can be added to a domain.

Full domain containing eight DIO boards provide up to 256 UUT I/O channels (256 channels *wide*). Because the driver supports 16 masters, up to 16 domains of mixed types can, in principle, share a computer bus. The number of master/slaves depends on the DIO Bus type (ISA, PXI, PCI), and the number of available free bus slots in your system.

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GC5050 Architecture and Capabilities

The following are key GC5050 characteristics and architecture:

- The GC5050 is a **Plug and Play (PnP)** board. The operating system (Windows 9x, Me, Windows 2000 or XP) automatically identify and arbitrate resource requirements as well as notify the user that a new board was found and automatically install the driver for it.
- A DIO domain, when in RUN mode, operates independently of the host computer.
- Each GC5050 DIO board supports a maximum clock frequency of up to 50MHz per channel for all channels (total of 1.6GB of data per second for 256 channels).
- A GC5050 (Master) board controls the timing of a DIO domain and can be synchronized to a UUT.
- Multiple Master boards are used to synchronize mutually asynchronous UUT elements.
- Each GC5050 Slave board adds 32 UUT channels. Up to seven Slave boards can be added to make a total of 256-channel domain.
- DIO boards can support different interfaces (that is different voltage levels) by mounting different I/O Modules (see the *I/O Modules and Interface User Guide*).
- Every GC5050 board, Master or Slave, require an I/O Module daughter card.
- Channel direction is controlled in-groups of eight. Direction can be set while in RUN mode for each step, input or output as defined in the loaded vector.
- GC5050 output channels can be enabled or disabled dynamically by external lines in groups of eight. Disabled channels on output boards are in Tri-State. This is useful for connecting to a user bus. Disabling the outputs has no effect if the board is set up for input.
- Configuration of board memories can vary within a domain. The board with the smallest step capacity limits the available number of vector steps (depth).
- Each Master has a 16-bit external event bus. This bus is used for triggering and synchronization with external events.
- There are three registers A, B and C that can be loaded and compared against external events on the External Event line.
- Triggers can be generated by external events on the Timing connector External Event lines. Event and Mask registers are used to determine both the triggering event and the masking bits to be ignored. These use the D Event and D Mask registers and T Event and T Mask registers.
- External triggering can be initiated on sequential or concurrent events by using both D and T event registers to define events.
- The test sequence (vector) can be paused on external events unconditionally or conditionally. P Event and P Mask registers hold the condition and bits that generate a conditional pause.
- An X Register is used to emulate an external event condition under program control for purposes of test program verification. The register is loaded through the computer bus.
- A DIO domain can be set to have internal or external clock, in order to synchronize with the user UUT.
- A DIO domain clock source (internal or external), active when outputting data, can be programmatically delayed by 0-25 nSec (increments of 5nSec).
- A DIO domain Strobe source (internal or external), active when inputting data, can be programmatically delayed by 0-63.75 nSec (increments of 0.25nSec).
- All boards Firmware, GC5050 and I/O Modules, can be upgraded through the DIO driver.

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- The GC5050 is compatible with Marvin Test Solutions' GT50 and GT25 boards. Test vectors developed for these products also work with the GC5050.

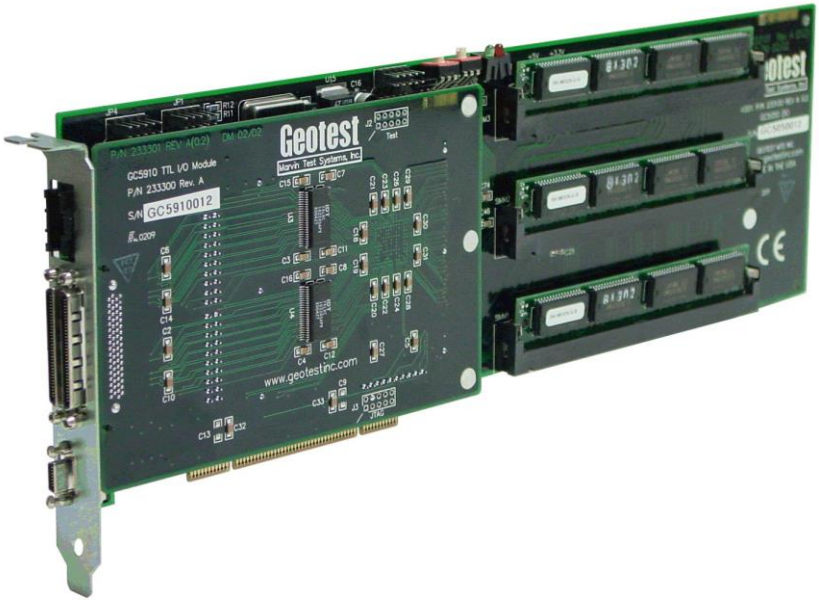


Figure 2-2: C5050 -Complete View

GX5050 Models and Accessories

Name/	**Description**
DIO board	Digital input/output and domain timing and control.
I/O Module, TTL (GC5050 require one I/O module option)	I/O Interface, TTL
I/O Module, Programmable (GC5050 require one I/O module option)	I/O Interface, Programmable Levels
I/O Module, PECL (GC5050 require one I/O module option)	I/O Interface, PECL
I/O Module, LVDS (GC5050 require one I/O module option)	I/O Interface, LVDS (differential)
Connector Interface for GC5050, SCSI to 100 Mil Grid, Single Ended	UUT I/O Interface
Connector Interface for GC5050, SCSI to 100 Mil Grid, Differential	UUT I/O Interface
Connector I/F for GC5050, SCSI to 100 Mil Grid, Single Ended (both 64 & 14 pin)	UUT I/O Interface
2' shielded cable for GC5050 (68 Pin)	UUT I/O Cable
3' shielded cable for GC5050 (68 Pin)	UUT I/O Cable
6' shielded cable for GC5050 (68 Pin)	UUT I/O Cable
10' shielded cable for GC5050 (68 Pin)	UUT I/O Cable
Timing ribbon cable, 2 to 16 20-pin connectors	Connects Timing connector to Master and slaves.

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Chapter 3 - Installation and Setup

Getting Started

This section includes general hardware installation procedures for the GX5290 board and installation instructions for the GTDIO software. Before proceeding, please refer to the appropriate chapter to become familiar with the board being installed.

To Find Information on…	**Refer to…**
GTDIO Software Installation	This Chapter
Hardware/Board Installation	This Chapter
Using the GTDIO Panel	This chapter and the DIO Software User's Guide
Using DIOEasy	DIO Software User's Guide
Programming the Board	DIO Software User's Guide and the DIO Programmer's Reference manuals

Packing List

Check the package against the packing list and your purchase order and make certain all purchased items are included. A DIO board package includes required items and may include options and accessories listed below:

Part Name/Description	**Part Function**	**Part Number**
DIO board	Digital input/output and domain timing and control.	GC5050
I/O Module, TTL (GC5050 require one I/O module option)	I/O Interface, TTL	GC5910
I/O Module, Programmable (GC5050 require one I/O module option)	I/O Interface, Programmable Levels	GC5930
I/O Module, PECL (GC5050 require one I/O module option)	I/O Interface, PECL	GC5940
I/O Module, LVDS (GC5050 require one I/O module option)	I/O Interface, LVDS (differential)	GC5960
Connector Interface for GC5050, SCSI to 100 Mil Grid, Single Ended	UUT I/O Interface	GT95014
Connector Interface for GC5050, SCSI to 100 Mil Grid, Differential	UUT I/O Interface	GT95015
Connector I/F for GC5050, SCSI to 100 Mil Grid, Single Ended (both 64 & 14 pin)	UUT I/O Interface	GT95020
2' shielded cable for GC5050 (68 Pin)	UUT I/O Cable	GT95021
3' shielded cable for GC5050 (68 Pin)	UUT I/O Cable	GT95022
6' shielded cable for GC5050 (68 Pin)	UUT I/O Cable	GT95031
10' shielded cable for GC5050 (68 Pin)	UUT I/O Cable	GT95028
Timing ribbon cable, 2 to 16 20-pin connectors	Connects Timing connector to Master and slaves.	GT95009/10/11

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Unpacking and Inspection

After removing the board from the shipping carton:

 **Caution -** Static sensitive devices are present. Ground yourself to discharge static.

1. Remove the board from the static bag by handling only the metal portions.
2. Be sure to check the contents of the shipping carton to verify that all of the items found in it match the packing list.
3. Inspect the board for possible damage. If there is any sign of damage, return the board to Marvin Test Solutions immediately. Please refer to the warranty information at the beginning of the manual.
4. Return the board to its anti-static bag until ready for installation and setup.

System Requirements

All GX5290 instrument boards are designed for use with a 3U or 6U cPCI or PXI compatible chassis. The software is compatible with any computer system running Windows 98, Windows Me, Windows 2000, Windows XP, Windows VISTA (32 bit) operating systems.

Each board requires one unoccupied 3U PXI bus slot.

Installation of the GTDIO Software

Before installing the board it is recommended to install the software as described in this section:

1. Insert the Marvin Test Solutions CD-ROM and locate the **GTDIO.EXE** setup program. If you computer's Auto Run is configured, when inserting the CD a browser will show several options, select the Marvin Test Solutions Files option, then locate the setup file. If Auto Run is not configured you can open the Windows explorer and locate the setup files (usually located under \Files\Setup folder). You can also download the file from Marvin Test Solutions web site (www.MarvinTest.com).
2. Run the setup and follow the instruction on the Setup screen to install the software.

   Note: When installing under Windows 2000/XP/VISTA, you may be required to restart the setup after logging-in as a user with an Administrator privileges. This is required in-order to upgrade your system with newer Windows components and to install kernel-mode device drivers (HW.SYS and HWDEVICE.SYS) required by the GTDIO driver to access resources on your board.
3. The first setup screen to appear is the Welcome screen. Click **Next** to continue.
4. Enter the folder where software is to be installed. Either click **Browse** to set up a new folder, or click **Next** to accept the default entry of `C:\Program Files\Marvin Test Solutions\GTDIO`.
5. Select the type of Setup you wish and click **Next.** You can choose between **Typical**, **Run-Time** and **Custom** setups. **Typical** setup type installs all files. **Run-Time** setup type will install only the files required for controlling the board either from its driver or from its virtual panel. **Custom** setup type lets you select from the available components.

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The program will now start its installation. During the installation, Setup may upgrade some of the Windows shared components and files. The Setup may ask you to reboot after it complete if some of the components it replaced where used by another application during the installation – do so before attempting to use the software.

You can now continue with the installation to install the board. After the board installation is complete you can test your installation by starting a panel program that let you control the board interactively. The panel program can be started by selecting it from the Start, Programs, GTDIO menu located in the Windows Taskbar.

Overview of the GTDIO Software

Once the software installed, the following tools and software components are available:

- **PXI/PCI Explorer applet** – use to configure the PXI chassis, controllers and devices. This is required for accurate identification of your PXI instruments later on when installed in your system. The applet configuration is saved to PXISYS.ini and PXIeSYS.ini that are used by Marvin Test Solutions instruments, the VISA provider and VISA based instruments drivers. In addition, the applet can be used to assign chassis numbers, Legacy Slot numbers and instruments alias names.

  VISA is a standard maintained by the VXI Plug & Play System Alliance and the PXI Systems Alliance organizations (http://www.vxipnp.org/, http://www.pxisa.org/). VISA provides a standard way for instrument manufacturers and users to write and use instruments drivers. The VISA resource managers such as National Instruments **Measurement & Automation** (NI-MAX) can display and configure instruments and their address (similar to Marvin Test Solutions' PXI/PCI Explorer).

- **GTDIO Panel** – use to configure, control and display the board settings.
- **DIOEasy** – Windows application for creating and analyzing vector files used by DIO boards.
- **GTDIO driver** – a DLL (GTDIO32.DLL) located in the Windows System folder used to program and control the board.
- **Programming files and examples** – interface files and libraries for various programming tools, see later in this chapter for a complete list of files, programming languages and development tools supported by the driver.
- **Documentation** – On-Line help and User's Guide.

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Configuring Your PXI System using the PXI/PCI Explorer

To configure your PXI/PCI system using the **PXI/PCI Explorer** applet follow these steps:

1. **Start the PXI/PCI Explorer applet**. The applet can be start from the Windows Control Panel or from the Windows Start Menu, **Marvin Test Solutions**, **HW**, **PXI/PCI Explorer**.
2. **Identify Chassis and Controllers**. After the PXI/PCI Explorer started it will scan your system for changes and will display the current configuration. The PXI/PCI Explorer automatically detects systems that have Marvin Test Solutions controllers and chassis. In addition, the applet detects PXI-MXI-3/4 extenders in your system (manufactured by National Instruments). If your chassis is not shown in the explorer main window, use the Identify Chassis/Controller commands to identify your system. Chassis and Controller manufacturers should provide INI and driver files for their chassis and controllers to be used by these commands.
3. **Change chassis numbers, PXI devices Legacy Slot numbering and PXI devices Alias names.** These are optional steps to be performed if you would like your chassis to have different numbers. Legacy slots numbers are used by older Marvin Test Solutions or VISA drivers. Alias names can provide a way to address a PXI device using your logical name (e.g. "DIO1"). For more information regarding these numbers see the **DioSetupInitialization** and **DioSetupInitializationVisa** functions in the DIO Programming User's Guide.
4. **Save you work**. PXI Explorer saves the configuration to the following files located in the Windows folder: PXISYS.ini, PXIeSYS.ini and GxPxiSys.ini. Click on the **Save** button to save you changes. The PXI/Explorer prompt you to save the changes if changes were made or detected (an asterisk sign ' *' in the caption indicated changes).

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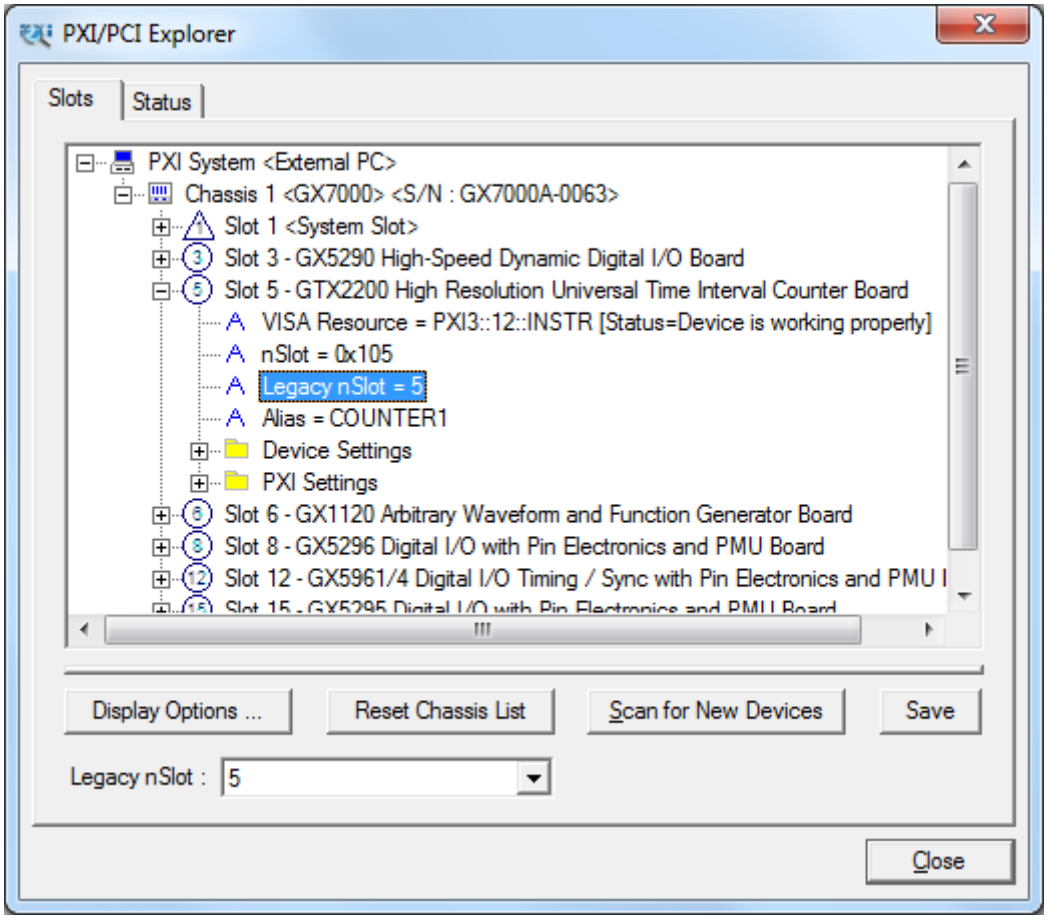


Figure 3-1: PXI/PCI Explorer

Board Installation

Before you Begin

- Install the GTDIO software as described in the prior section.
- Configure your PXI/PC system using **PXI/PCI Explorer** as described in the prior section.
- Verify that all the components listed in the packing list (see previous paragraph) are present.

Electric Static Discharge (ESD) Precautions

To reduce the risk of damage to the board, the following precautions should be observed:

- Leave the board in the anti-static bags until installation requires removal. The anti-static bag protects the board from harmful static electricity.
- Save the anti-static bag in case the board is removed from the computer in the future.
- Carefully unpack and install the board. Do not drop or handle the board roughly.

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- Handle the board by the edges. Avoid contact with any components on the circuit board.

Caution - Do not insert or remove any board while the computer is on. Turn off the power from the PXI chassis before installation.

Board Selector Switch Settings

A DIO domain has a Master and Slave boards. In order to configure a DIO domain, each board needs to have a unique number so it can be identify by the software as part of the specified domain, i.e. all Slave boards that belongs to the same Master are in the same domain.

Master — The selector switch designated as "Master" sets the Master domain that the board belongs to. The adjacent selector switch (designated as "Slave") needs to be set to 0.

Slave — The selector switch designated as "Master" sets the Master domain that the Slave board belongs to. The selector switch designated as "Slave", select the Slave number in that domain and can be set to any number from 1 to 7 for a total of 7 Slaves (number 0 is saved for the Master).



Figure 3-2:Master and Slave Switch Selectors

Connecting Timing cable

Timing cable needs to be installed only if there is at least one Slave board. The Timing cable provides timing and control signals to the Master and Slaves boards in the DIO domain. The Timing connection is Daisy Chain arrangement, similar to SCSI or IDE buses. The Timing cable is a flat cable with 20-pin header connectors.

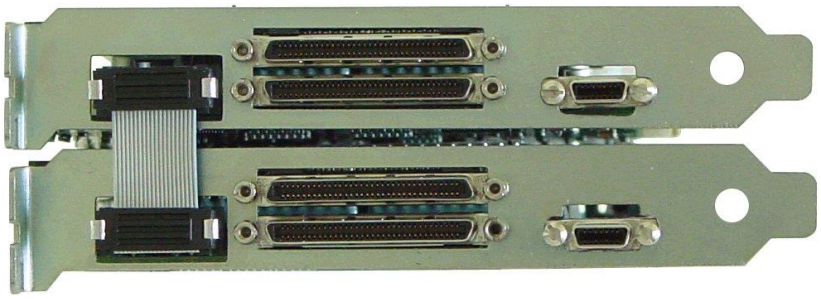


Figure 3-3: Timing Cable Interconnection

Installing Memory

The GC5050 is shipped with the memory configuration it has been ordered with. Skip this section if you are not adding or reconfiguring the memory of the GC5050.

This section covers SIMMs (single in-line memory modules) used for data and control memory functions.

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Note: DIO SIMM modules are specially made for Marvin Test Solutions in order to match the DIO's unparallel high performance stand-alone capabilities.

GC5050 DIO boards use three SIMMs (Figure 3-4)

- SIMM1 – is the Control Memory
- SIMM2 – is the Output Memory
- SIMM3 – is the Input Memory

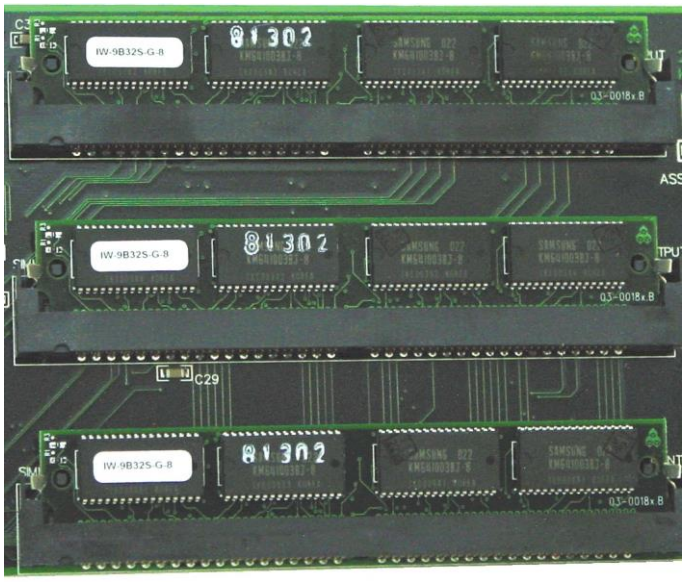


Figure 3-4: Memory and Sockets

When upgrading memory, all DIO SIMMs must have the same size and speed specifications.

Domain performance is limited by the slowest and smallest memory on any DIO board. Therefore, the user is urged to compare test requirements against DIO board memory capabilities and upgrade DIO boards as necessary. This must be done before installing boards.

The following procedure explains how to install SIMMs on a DIO board. This procedure must be implemented with the DIO board removed from the PCI chassis / PC and laying component side up on a suitable bench or work area. Observe safety and ESD precautions to avoid damage.

1. If populating memory with all new SIMMs, use Table 3-1.
2. Carefully set the SIMM over the socket to check orientation. Make certain the SIMM edge connector is aligned with the 72-pin socket. The off-center gap between pins should match. If necessary, rotate the SIMM to align with the socket.

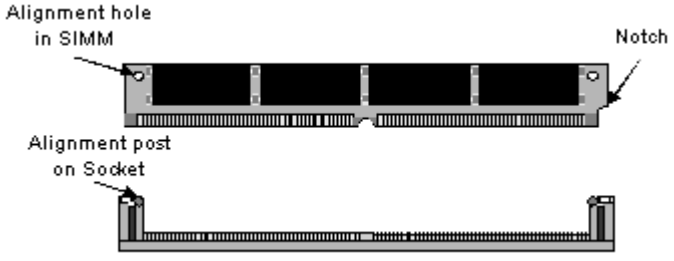


Figure 3-5: SIMM Module Installation

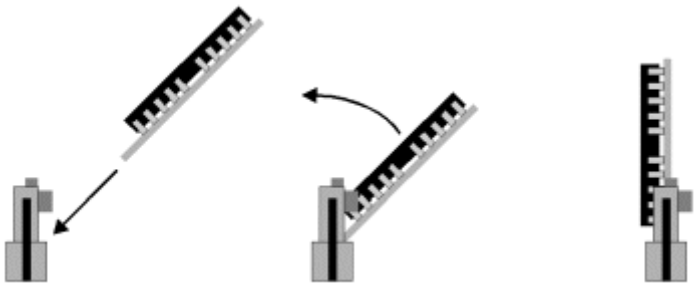


Figure 3-6: SIMM Module Installation

3. With the SIMM aligned and normal to the board, press firmly and rotate downward to a 45-degree angle until it snaps into place. When properly seated, the module "clicks" into place.

4. Assure that all SIMMs are seated correctly and that the metal locking tabs engage on both sides of the SIMM socket.

Notes: (1) Never force a SIMM into a socket. It is keyed with a notch in the lower right corner. This notch prevents incorrect orientation. If there is difficulty inserting a SIMM, check the alignment.

(2) Damage to SIMM modules and/or sockets may result if proper insertion guidelines are not observed.

(3) SIMMs are extremely sensitive to static electricity. Follow instructions near the beginning of this chapter under *Discharge Static Electricity Precautions*.

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GC5150 DIO memory options are listed in Table 3-1.

SIMM Part number	Memory Size & Speed
GC5006	256K, 50MHz
GC5001	1MB, 50MHz

Table 3-1: SIMM Options

Installing I/O Modules

The GC5050 is shipped with the I/O Module it has been ordered with. Skip this section unless installing or changing an I/O Module.

I/O Module daughter cards provide special interface functionality between DIO and a UUT, including signal level conversion and high drive power for cables. GC5050 DIO boards require an I/O Module to interface with a UUT. A user-selected module is factory installed and tested. For simple five-volt or 3.3Volt logic, use the GC5910 TTL I/O Module, which uses single-ended 3.3V logic. See the *DIO I/O Modules and Interface User Guide* for more information.

When a DIO board is ordered with an I/O Module, the module is factory installed and tested. Sometimes, however, it is necessary to change the I/O interface or replace one that has been damaged. An I/O Module can be ordered separately and includes mounting hardware.

To replace an I/O Module on a GC5050 do the following:

1. Disconnect the Timing Cable from the front plate.
2. Remove the GC5050 board out from the PC/PCI chassis.
3. If the GC5050 board is mounted on a GTXI PCI Carrier board (e.g. GT7720) dismount the GC5050 board from the Carrier board.
4. On the front plate remove the I/O connector screws.
5. Remove the middle plastic screw at the edge of the I/O Module.
6. Replace the I/O Module with the new one and press the two connectors, J9 and J10 in place.
7. Install the middle plastic screw at the edge of the I/O Module.
8. Install the screws of the I/O connector in the front panel.
9. If the GC5050 board was mounted on a GTXI PCI Carrier board (e.g. GT7720) assemble the GC5050 board on the Carrier board.
10. Reattached the Timing Cable See ***Connecting Timing cable*** above.

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Installing a Board

Install each of the boards as follows:

1. Turn off the PXI chassis and unplug the power cord.
2. Locate a PXI empty slot on the PXI chassis.
3. Place the module edges into the PXI chassis rails (top and bottom).
4. Carefully slide the PXI board to the rear of the chassis, make sure that the ejector handles are pushed **out** (as shown in Figure 3-7).

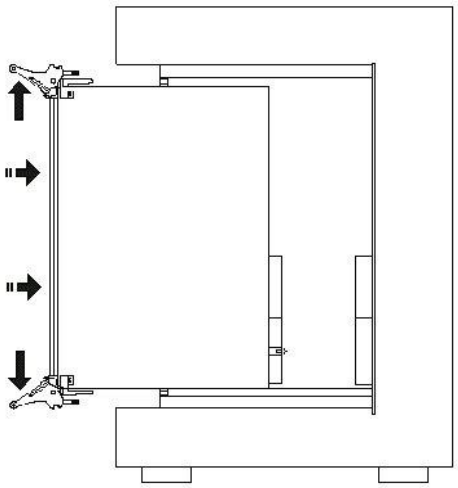


Figure 3-7: Ejector handles position during module insertion

5. After you feel resistance, push in the ejector handles as shown in Figure 3-8 to secure the module into the frame.

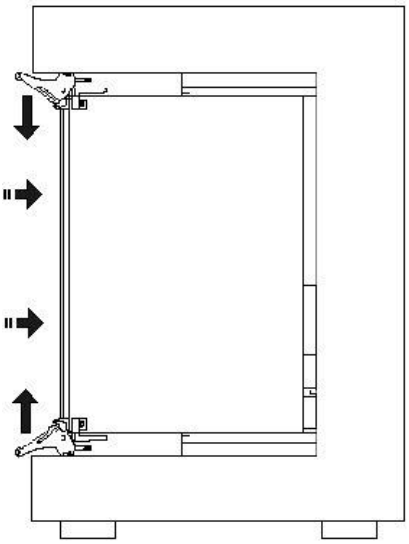


Figure 3-8: Ejector handles position after module insertion

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6. Tighten the module's front panel to the chassis to secure the module in.
7. Connect any necessary cables to the board.
8. Plug the power cord in and turn on the PXI chassis.

Plug & Play Driver Installation

Plug & Play operating systems such as Windows 9x, Me, Windows 2000 or XP (Not Windows NT) notify the user that a new board was found using the **New Hardware Found** wizard after restarting the system with the new board.

If another Marvin Test Solutions board software package was already installed, Windows will suggest using the driver information file: HW.INF. The file is located in your Program Files\Marvin Test Solutions\HW folder. Click **Next** to confirm and follow the instructions on the screen to complete the driver installation.

If the operating system was unable to find the driver (since the software driver was not installed prior to the board installation), you may install the software as described in the prior section, then click on the **Have Disk** button and browse to select the HW.INF file located in C:\Program File\Marvin Test Solutions\HW.

If you are unable to locate the driver click **Cancel** to the found New Hardware wizard and exit the New Hardware Found Wizard, install the DIO driver, reboot your computer and repeat this procedure.

The Windows Device Manager (open from the System applet from the Windows Control Panel) must display the proper board name before continuing to use the board software (no Yellow warning icon shown next to device). If the device is displayed with an error you can select it and press delete and then press F5 to rescan the system again and to start the New Hardware Found wizard.

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Removing a Board

Remove the board as follows:

1. Turn off the PXI chassis and unplug the power cord.
2. Locate a PXI slot on the PXI chassis.
3. Disconnect and remove any cables/connectors connected to the board.
4. Un-tighten the module's front panel screws to the chassis.
5. Push out the ejector handles and slide the PXI board away from the chassis.
6. Optionally - uninstall the software by running the setup again (or from the Windows Control Pane, Programs and Features or Add Remove Programs applet) and selecting Remove/Uninstall.

Verifying the Installation

To verify proper DIO board installation, install the software first, and then use the Panel to configure the driver and initialize the board. To access the Panel, GTDIO software must be installed. Run the panel by selecting **Marvin Test Solutions**, **GTDIO**, **DIO Panel** from the Windows Start menu.

Initializing DIO Boards

A DIO board installation is successful if the driver configuration database can be updated and all boards can be initialized.

When software installation is complete, do the following to configure and initialize the new boards.

1. Run PXI/PCI Explorer from the Windows Control Panel or from the Windows Start menu, Marvin Test Solutions, HW, PXI/PXI Explorer.
2. Make sure that your chassis is configured as described in configuring your PXI System using PXI/PCI Explorer. Locate your DIO board under PXI/PCI Explorer note the chassis number and the slot number it appears under.
3. Configure the DIO boards according to the procedure at **Chapter 3 - GTDIO Panel** in the **DIO Software User's Guide.**
4. Click **Initialize** to accept the domain configuration.
5. If the new DIO board(s) can be successfully configured and initialized, installation is successful, the memory density and number of SIMMs displays for each board.

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Chapter 4 - Theory of Operation

This chapter presents the theory of operation for the GC5050 boards, with an overview of operation and a simple description of operation for one channel (I/O pin). Other topics covered in this chapter are:

- Operation of clock (CLK) and strobe signals.
- Memory management.
- Program sequencer and command conditions.
- Basic states of operation internal and external trigger operation.
- Internal and external pause operation.

Architecture

The GC5050 can run at frequencies as high as 50MHz. Each board contains 32 I/O pins arranged in 4 groups of 8, each group having its own direction: input or output. The direction of each group can be changed for each and every step, either internally by command words or externally in an unsynchronized mode. Each GT-DIO board can be configured from 256K steps to 1M steps behind each I/O pin.

The GC5050 works as a state machine with three main states: **HALT**, **PAUSE** and **RUN**. One of the modules in the board is the sequencer. The sequencer interprets commands stored in a memory array and controls the states machine. Two other memory arrays hold the output data and the input data. The sequencer controls the address of the memory arrays and thereby controls the flow when the board is in the RUN state.

External control provides CLK, strobe and I/O pin direction from an external source. The combination of the external bi-directional control and external clocking, strobing, and triggering provides the capability to fully synchronize with UUTs and to minimize initialization procedures. The board sequencer permits the creation of conditional and unconditional loops and branches to manipulate the output vectors. This provides the capability to generate indefinite stimulus vectors at the maximum test rate.

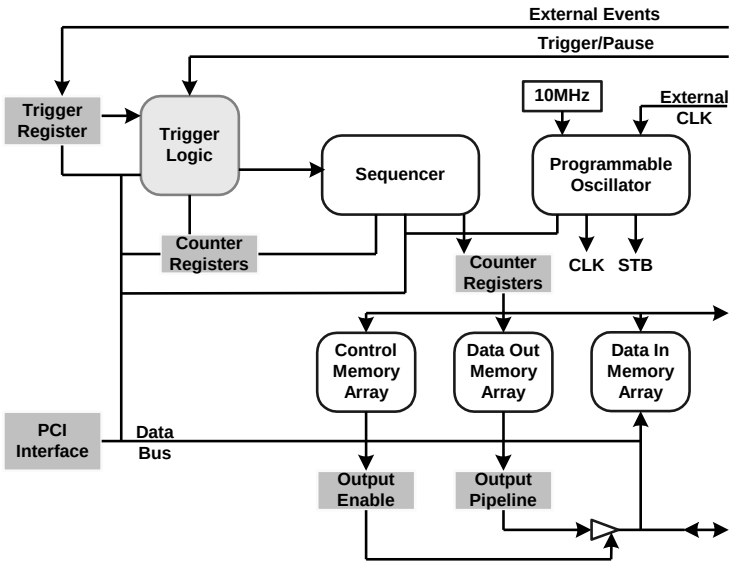


Figure 4-1: Architecture Diagram

Masters and Slaves

The DIO System is made up of Master and Slave(s) circuit boards. The Master board can be connected to a maximum of seven Slave boards. Each board must have an I/O Module.

All boards are (Master and Slaves) connected through a 20-pins timing ribbon cable. The timing cable distributes clock, control and status signals. The ribbon cable connected from J7 on a Master board to J7 on each of the other Slave boards. See "Chapter 3 -Setup and Installation" for more details about board installation.

I/O Pin

An I/O pin uses one channel. Up to eight boards can be used in one domain for a maximum of 256 pins (each board containing 32 I/O pins).

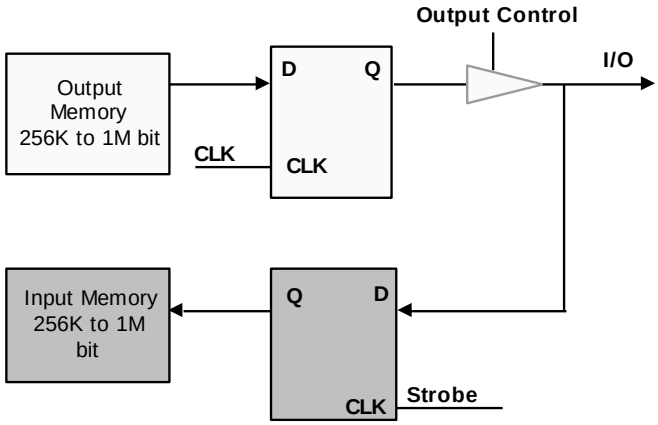


Figure 4-2: I/O Pin Block Diagram

Figure 4-3 is a simplified block diagram of a single I/O pin. This diagram shows how a single channel functions. Output data is stored in the output memory and is outputted from the board as a function of the CLK signal through an output buffer when enabled. When defining the channel a Input, the channel value is latched by the Strobe signal into the input buffer and stored in the input memory.

Note: Whenever a group of channels is defined as Output for a specified step, the value of that group step will be latched into the In Memory while running.

The direction of the I/O pins (input/output) depends on the output Control State. In addition, each output (driver) defined pin is also an input (receiver). The software can ignore the received data; however, its value in the input memory will be the same as the output value.

Clock and Strobe Signals

The clock (CLK) signal initiates each output vector. The rate of this signal can be programmed from 5Hz to 50MHz (depend on board configuration). Similarly, the strobe signal latches the input vector. All clock and strobe signals are distributed evenly to all DIOs (in the same Maser/Slave domain) through J7 using the timing cable.

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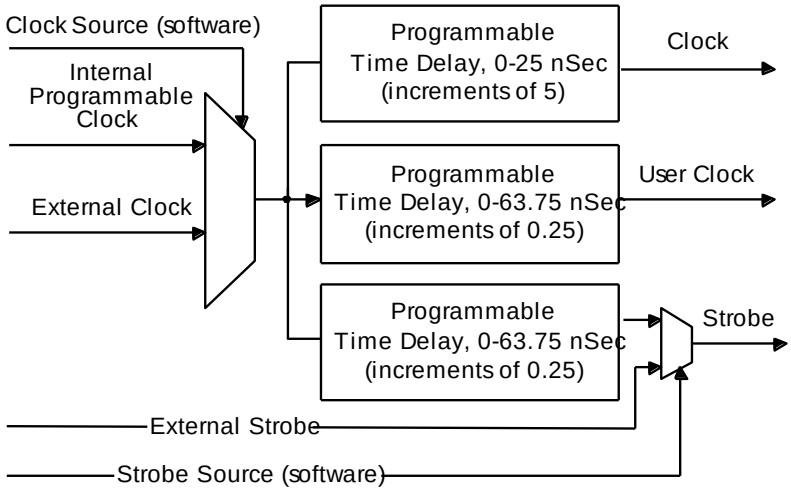


Figure 4-3: Clock Source Block Diagram

Timing board has the following clock source signals:

1. Internal Programmable Clock – programmable clock from 5Hz to 50MHz with increments of 1HZ. See *Specification* for details
2. External Clock – supplied by the user through J1 Timing Control, can be from 5Hz to 50MHz. See *Specification* for details.

There are three clock signals coming out of the Timing board:

Clock	The DIO sends output patterns to the IO Module connector on the rising edge of the Clock (CLK) signal. The Clock can have a delay of 0-25 nSec (with increments of 5) relative to the current clock source.
User Clock	This clock signal has the same source and frequency as the Clock but can have a different time delay. The User Clock can have a delay of 0-64 nSec (with increments of 0.25) relative to the current clock source.
Strobe	The DIO captures input patterns from the IO Module connector on the rising edge of Strobe (STB). When the Strobe source signal is internal, it has the same frequency as the Clock signal. The Strobe can have a delay of 0-64 nSec (with increments of 0.25) relative to the current clock source. The timing diagram in Figure 4-4 displays CLK and Strobe signals. The DIO board can be driven using either internal or external clock sources. In internal mode, Strobe occurs Ts nanoseconds before the next clock (CLK) signal (16 nSec default). Ts can be set from 0 – 25 nanoseconds before the CLK signal. In the external mode, Clock or Strobe signals are provided externally.

A timing diagram of the CLK and Strobe signals is shown in Figure 4-4.

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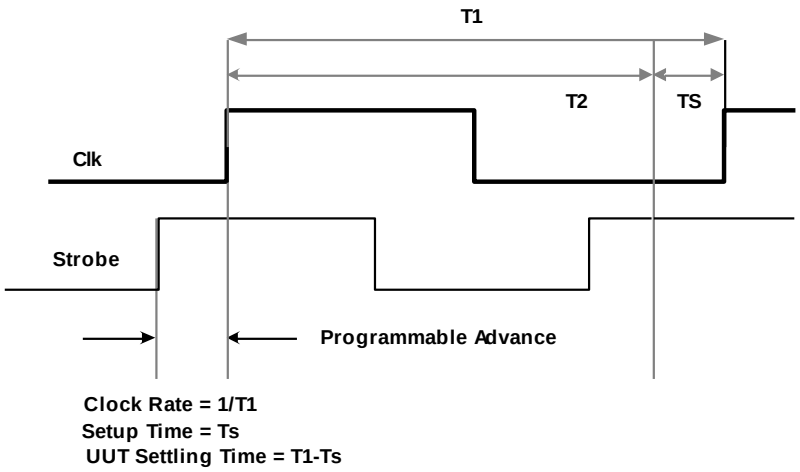


Figure 4-4: Signal Timing Diagram

GC5050 Memory Management

The GC5050 board has an independent memory for Input, Output and Control that can be configured with either 256K or 1M of memory steps behind each I/O pin. Control and I/O memory are managed as shown in the memory management block diagram (Figure 4-5).

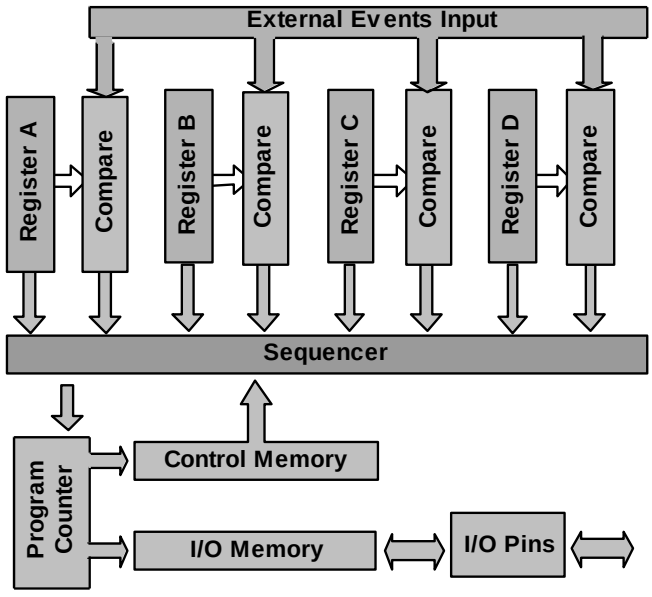


Figure 4-5: Memory Management Block Diagram

The CLK signal and the sequencer control the program counter. The program counter contains the address of the current control and I/O memory. After resetting, the program counter points to address zero and increments with the CLK signal towards address 1M.

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Program Sequencer

The sequencer (Figure 4-5) controls the program counter and is one of the most important blocks. The inputs to the sequencer are the control memory, 16 bit registers (A, B, C, D, P and T) and the 16-bit external events input lines (X register), through the comparators.

Every program step includes one command residing in the Control Memory. Sequencer commands allow you to control and manipulate the program counter. Each memory step can include only **one** sequencer command. Most of these commands can be conditioned.

Commands

Commands can be used to change the flow control of vectors by changing the value of the program counter while the program is running. Commands can be various types: loads registers or modify the next address provided by the program counter.

The following commands can be executed:

1. **NOP – No operation.** Go to the next step, the sequencer will not affect the program counter.
2. **Set register to X**. The sequencer will set register A, B, C, or D to a value given in the command. The value assigned to the command can be from 0 to 0xFFFF. If Register D is used, the 16 external event lines' values are assigned to Register D.
3. **Jump to Step X**. The sequencer enables you to program a jump to any location and it can be conditional or unconditional.
4. The jump command can be near or far. If the far jump command is used, the address can be anywhere in the 1M 20-bit steps; however, the command cannot be conditional. If the jump is near, the address is 17 bits, within the current 128K-memory page.
5. **Loop to Step X**. The sequencer enables you to perform a programmed number of jumps (a series of jumps) from the same address. This command can be conditional or unconditional. The jump is always to a near address, in the current 128K-memory page.
6. **Call subroutine at X**. The sequencer saves the address and allows you to perform a jump that remembers the location it jumped from (Y). It returns to Y+1 and can be conditional or unconditional. The address of the subroutine is a far address in eight step boundaries (0, 8, 16, etc.). One level can be used when calling a subroutine.
7. **Return.** The sequencer returns to the address following the last **Call** command. The command can be conditional or unconditional.
8. **Pause.** A pause in the program. The command can be conditional or unconditional.
9. **Halt.** End of the program.

Note: See Appendix B for more information on how to code and decode commands.

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Sequencer Command Table

#	COMMAND	PARAMETERS
1	NOP - Continue to next step.	
2	Set Register *R* to *V* Value. If *R* is D, the value is taken from External Event Lines.	*R* = A, B, C or D Registers $0 \le V \le$ 0xFFFF
3	Jump (FAR) to Step *X*.	$0 \le X \le$ 1M
4	Jump (NEAR) to Step *X* on Register *R* Condition (optional) or on External Event Line *B* (high or low) (optional).	*R* = A, B, C or D Registers $0 \le B \le 3$ *X* is the address in the current 128K page
5	Loop *N* Times to Step *X* on Register D Condition (optional).	*N* = A, B or C Registers *X* is the address in the current 128K page
6	Call Subroutine at Step *X* on Register *R* Condition (optional) or on External Event Line *B (*high or low) (optional).	*R* = A, B, C or D Registers $0 \le B \le 3$ $0 \le X \le$ 1M Step *X* must be divided by 8 (0, 8, 16, 24, etc.)
7	Return from Subroutine on Register *R* Condition (optional) or on External Event Line # *B* (optional).	*R* = A, B, C or D Registers $0 \le B \le 3$
8	Pause on Register *R* Condition (optional) or on External Event Line *B* (optional).	*R* = A, B, C or D Registers $0 \le B \le 3$
9	Halt	

Table 4-1: Sequencer Commands

Conditions

Conditions are a combination of comparisons of the external event input lines to a register. The external event input lines are compared with a 16-bit A, B, C or D register.

Conditions can be based on:

- The register equals the external event input lines.
- The register does not equal the external event input lines.
- The register is greater than the external event input lines.
- The register is less than the external event input lines.

Other available conditions are as follows (these conditions cannot be used with the loop command):

- Bit number 0, 1, 2, 3 in the external event line is high.
- Bit number 0, 1, 2, 3 in the external event line is low.

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GC5050 States

The GC5050 board functions in three basic operational states; **Halt**, **Pause** and **Run**.

Error! Reference source not found. is a block diagram showing the relationship of these operational states.

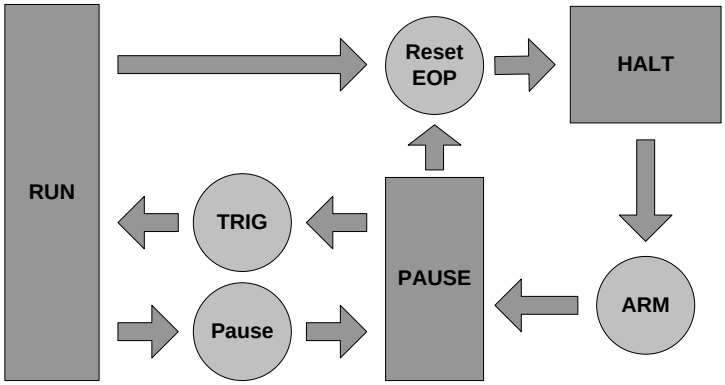


Figure 4-6: GC5050 Operational States

Halt State

The GC5050 board goes into a Halt state after a Reset signal and following the Halt command. All external event inputs as well as external control inputs are ignored following a Halt command. Following Reset, all I/O pin (channels) are in the receiving mode of operation. The program counter is zero, the frequency is set to an internal 5MHz, and the strobe timing is set to 5nSec.

Pause State

The board enters a Pause state from a Halt state with an ARM command sent by the PC bus, or from the Run state following the Pause command.

Run State

In the Run state, data is being output and input is being latched. The program counter holds the address of the current output and the address of the command to be decoded and executed by the sequencer. While executing the command, output pins send the data from the output memory located at the program counter address in the control memory and the input pins receive the data. The sequencer executing the command usually increments the programs counter by one unless the command changed the value of the program counter (for example, the Jump command) or the state of the machine was changed (for example, the Pause command). After changing the program counter value, the input data is stored in the input memory at the new program counter address.

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Trigger Command

The trigger command causes the board to change its state to the Run state and originates from the following sources:

- PC (software)
- External trigger control line
- External event lines (16 lines)

PC (Software) Trigger

The software trigger originates within the PC. The PC bus trigger command takes effect immediately and overrides other established trigger conditions.

External Trigger

External Trigger Control Line

External triggers originate from the external trigger line. Pulling this line to zero causes the board to change its state to RUN. The external trigger line overrides other trigger conditions set for the GT-DIO board.

External Event Lines

It is also possible to set a conditional trigger command, which is activated upon receiving external event input lines. This external event may be any expected value on all or part of the external event input lines. The 16 external event lines are ANDed with pre-defined masks and compared with pre-defined events in registers D and T. The external events trigger function is shown in Figure 4-7.

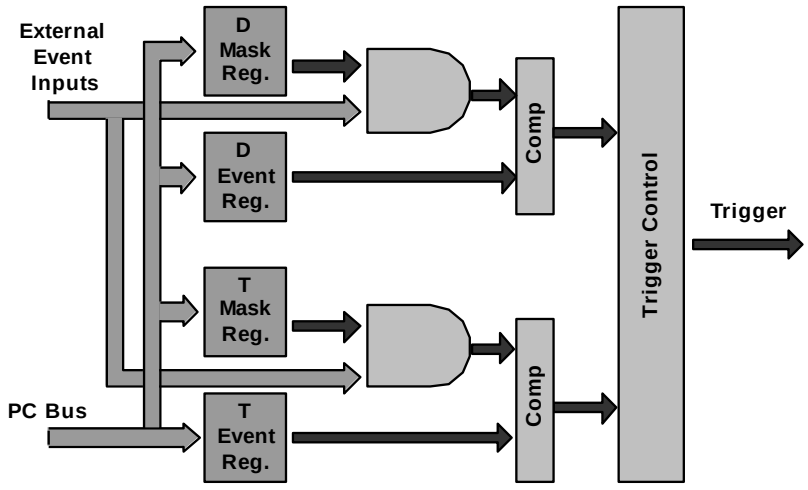


Figure 4-7: External Events Trigger Block Diagram

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The external events trigger can be set to one or two levels. In the one level mode, the trigger will be generated after the external condition has been met with the D or T event mask registers. In the two level mode, the board will wait for two sequential events to be met before issuing the trigger signal (D first, T second or opposite).

Pause Command

The pause command causes the board to change its state to the Pause state and originates from the following sources:

- External control line
- External events line
- Sequencer command

External Pause

External Pause Control Line

External pause originates from the external pause line. Pulling this line to zero will cause an immediate pause. The external pause overrides other pause conditions set to the GT-DIO board.

External Pause Event Lines

The P mask and event registers can be used to create conditional pauses that depend on external event lines. The 16 external event lines are ANDed with pre-defined masks and compared with pre-defined events in register P.

The external/internal events pause function in the board is shown in Figure 4-8:

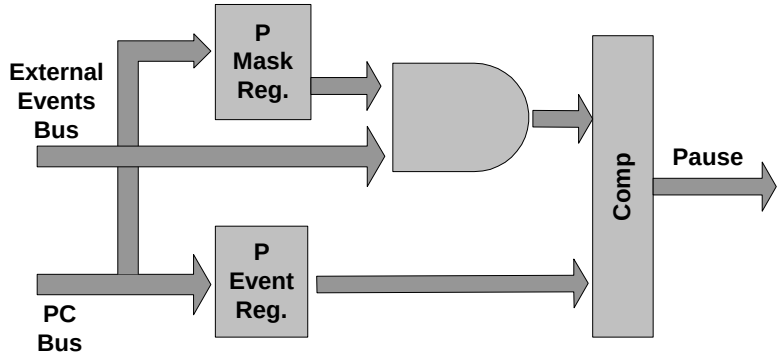


Figure 4-8: External Events Pause Block Diagram

Other Features of the GC5050 Board

X Register

The GC5050 board has a 16-bit register that can be set by software to simulate the external event lines.

B Clock Source

The GC5050 Board has another programmable clock that may be used externally. This clock can be programmed from 1MHz to 110MHz.

This clock CLKB is independent. It is not defined at power up and once programmed, it will not change (even by reset) until programmed to another value.

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Appendix A - Connectors and Cables

Overview

This section describes the DIO I/O and the Timing connectors and cables (see Figure A-1).

When a GC5050 is configured as Master all connectors can be used. When it configured as a Slave, the Timing connector should not be used because some of its signals are not connected In a DIO domain only the Master timing signal are connected and valid.

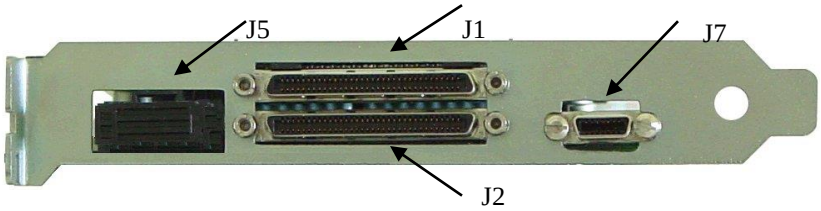


Figure A-1: GC5050 Panel Connectors for UUT Cables

DIO Connectors

The GC5050 has 4 connectors. All the connectors are available on the instrument's front panel.

The GC5050 has the following connectors:

Connector Name	Control signals	Connector Description
J1 I/O	UUT I/O signals	68 Pin VHD Connector
J2 Timing	UUT Timing Signals	68 Pin VHD Connector
J5 I/O	Timing Signals Daisy chained to additional slaves.	20 Pin High Density Connector
J7 Control	UUT Control Signals. Do not use on Slave.	14 Pin VHD Connector

Connectors J5 (UUT I/O Signals), and J2 (Timing Control Signals) are 68-pin VHD connectors. J7 is 20-pin high-density header that is used to Daisy-chained additional Slave DIOs to achieve a pattern that is wider than 32 channels.

Figure A-2 shows the layout of a 68-Pin VHD connectors used for UUT I/O and timing signals. The 68-pin male end plate connector has a shielded, double pin row receptacle. The connector mates with a UUT cable.

GC5050 68-Pin (VHD) Connector

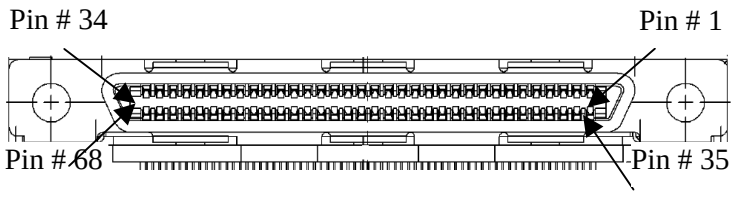


Figure A-2: GC5050 68-Pin (VHD) Connector

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J1 I/O Connector (68-Pin to UUT)

The following table defines the GC5050 DIO to UUT I/O signals. This interface uses a 68-pin VHD connector.

Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type
1	IO0+	I/O	18	IO17+	I/O	35	IO0-	I/O	52	IO17-	I/O
2	IO1+	I/O	19	IO18+	I/O	36	IO1-	I/O	53	IO18-	I/O
3	IO2+	I/O	20	IO19+	I/O	37	IO2-	I/O	54	IO19-	I/O
4	IO3+	I/O	21	IO20+	I/O	38	IO3-	I/O	55	IO20-	I/O
5	IO4+	I/O	22	IO21+	I/O	39	IO4-	I/O	56	IO21-	I/O
6	IO5+	I/O	23	IO22+	I/O	40	IO5-	I/O	57	IO22-	I/O
7	IO6+	I/O	24	IO23+	I/O	41	IO6-	I/O	58	IO23-	I/O
8	IO7+	I/O	25	IO24+	I/O	42	IO7-	I/O	59	IO24-	I/O
9	IO8+	I/O	26	IO25+	I/O	43	IO8-	I/O	60	IO25-	I/O
10	IO9+	I/O	27	IO26+	I/O	44	IO9-	I/O	61	IO26-	I/O
11	IO10+	I/O	28	IO27+	I/O	45	IO10-	I/O	62	IO27-	I/O
12	IO11+	I/O	29	IO28+	I/O	46	IO11-	I/O	63	IO28-	I/O
13	IO12+	I/O	30	IO29+	I/O	47	IO12-	I/O	64	IO29-	I/O
14	IO13+	I/O	31	IO30+	I/O	48	IO13-	I/O	65	IO30-	I/O
15	IO14+	I/O	32	IO31+	I/O	49	IO14-	I/O	66	IO31-	I/O
16	IO15+	I/O	33	MS		50	IO15-	I/O	67	MS	
17	IO16+	I/O	34	MS		51	IO16-	I/O	68	MS	

Table A-1: J5 68-Pin UUT I/O Data Connector.

Notes for Table A-1:

- Pin: Pin number
- I/O: Input or Output
- P: Power/GND
- IO0 – IO31: Differentially Coupled Data Lines. Non-differential I/O Modules, all IOx-(negated) lines are grounded.
- MS: I/O Module specific, See the "*PCI Bus I/O Modules and Interfaces User's Guide"* for complete pin listings for I/O modules.

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J2 - Timing Connector

This topic describes the GC5050's Timing connector J2. This 68-pin, very high-density (VHD) connector handles UUT timing and external event signals. It is used only on a Master.

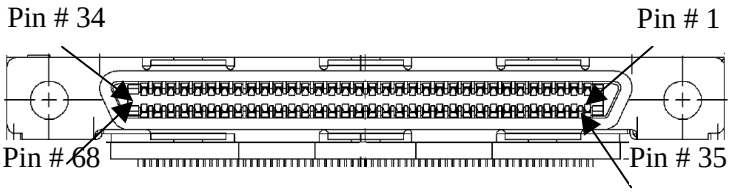


Figure A 3: Timing connector 68-Pin (VHD) Connector

The following table lists Timing signals:

Pin	Name	Function	Pin	Name	Function
1	EXT0	External event 0	18	ORUN	Output Run Indication
2	EXT1	External event 1	19	GND	
3	EXT2	External event 2	20	BCLK	Independent user defined programmable clock output
4	EXT3	External event 3	21	GND	
5	EXT4	External event 4	22	OCLK	User Clock Output
6	EXT5	External event 5	23	GND	
7	EXT6	External event 6	24	OSTB	Strobe Output
8	EXT7	External event 7	25	GND	
9	EXT8	External event 8	26	XTRIG	External Trigger (Overrides Run Command)
10	EXT9	External event 9	27	XPAUSE	External Pause (Overrides Pause Command)
11	EXT10	External event 10	28	XCLKEN	External Clock Enable
12	EXT11	External event 11	29	XSTBEN	External Strobe Enable
13	EXT12	External event 12	30	GND	
14	EXT13	External event 13	31	XCLK	External Clock Input
15	EXT14	External event 14	32	XSTB	External Strobe Input
16	EXT15	External event 15	33	VCC	
17	GND		34	GND	
35	GND		67	VCC	
66	GND		68	GND	

Table A-3: J2 68-pin Connector (timing) to UUT.
Unspecified pins are GND.

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J7 - Control Connector

This topic describes the GC5050's Control connector J7. This 14-pin, very high-density (VHD) connector handles UUT control signals.

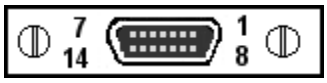


Figure A-4: GC5050 14-Pin Control Connector

The following table defines the GT5150 DIO to UUT control interface. This interface uses a 14-pin VHD connector.

Pin #	Function	Type	Pin #	Function	Type
1	GND	P	8	SDIN	IT
2	OEN0	OT	9	SSYNC	OT
3	OEN1	OT	10	JA	IT
4	OEN2	OT	11	XOE0	IT
5	OEN3	OT	12	XOE1	IT
6	SCLK	OT	13	XOE2	IT
7	SDOUT	OT	14	XOE3	IT

Table A-4: J7 14-Pin UUT Control Connector, J9.

Notes for Table A-4:

- IT : Input TTL level
- JA : Jump to a predefined address A Input. A low on this line will cause a jump to that address.
- OEN0-OEN3 : IOM generated Output Enables. A low on these lines specifies the I/O group currently enabled.
- OT : Output TTL level
- P : Power/GND
- SCLK, SDOUT, SDIN, SSYNC : Reserved, Should not be connected at any time
- XOE0-XOE3 : External Output Enable - input control for each I/O group. A low on these lines will disable the specific group output drivers.

J5 - Expansion Connector

J5 is an expansion connector between a domain master and one or more slaves. There are no signals available to the user, so signal and pin definitions are not shown.

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Appendix B - Control Memory Command

Overview

The information in this section describes the control memory command micro code. This information is useful when reading from and writing to the DIO board control memory. The control memory contains a 32-bit command for each step. Those commands serve as input to the on-board sequencer controlling the flow of the program counter and the direction of the I/O pins. See the *Commands* section in "Chapter 4 – Theory of Operation" for a complete and detailed list of commands and parameters.

Command Micro Code

The control memory consists of 32 bit commands. Each command is divided into six fields. A command layout diagram with the name of each field and position (bit number) is shown in Table B-1, followed by a definition of each command field in Table B-2.

Command Layout

BIT #	31 28	27 25	24 22	21 20	19 17	16 0
FIELD NAME	I/O Groups Control	Reserved (0)	Operation Code	Register	Condition	Address

Table B-1: Command Layout

COMMAND FIELD	DESCRIPTION
I/O Groups Control	These bits control the direction of the I/O bits 31-28 pin groups as described in Table B-3.
Reserved, bits 27-25	Reserved for future versions. Must be set to 0.
Operation Code, bits 24-22	These bits provide the command code as described in Table B-4.
Register, bits 21 and 20	SPECIFIES THE INTERNAL REGISTER USED WITH EITHER THE RELATED COMMAND OR THE EXTERNAL EVENT LINE NUMBER (0-3) CONDITIONS (SEE TABLE 4-1), AS DESCRIBED IN TABLE B-5.
Condition, bits 19-17	This field is the condition code for the related commands and the tree address MSBs for the JUMP FAR command (see Table 4-1). Condition codes are described in Table B-6.
Address, bits 16-0	THIS FIELD CONTAINS THE ADDRESS FOR BRANCH COMMANDS: **JUMP**, **LOOP**, **GOTO** AND **CALL**. WHEN THE OPERATIONS CODE IS SET TO THE SET COMMAND, THIS FIELD (BITS 0-15) IS USED AS DATA TO BE ASSIGNED TO A REGISTER.

Table B-2: Command Field Descriptions

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I/O Groups Control Field

I/O pins	Control word bit#	Control bit = 1	Control bit = 0
0-7	28	IN	OUT
8-15	29	IN	OUT
16-23	30	IN	OUT
23-32	31	IN	OUT

Table B-3: I/O Groups Control Field

Operation Code Field

Mnemonic	Additional fields	Value	Bit 24	Bit 23	Bit 22
NOP	None	0	0	0	0
JUMP FAR	Destination = Condition & Address	1	0	0	1
JUMP NEAR	Condition & Address	2	0	1	0
LOOP	Reg, Address & Condition	3	0	1	1
SET	Reg & Address	4	1	0	0
CALL	Condition & Address*	5	1	0	1
RETURN	Condition	6	1	1	0
PAUSE	Condition	7	1	1	1
HALT	Condition = 7	7	1	1	1

* Address in the CALL is divided by 8 (see Table 4-1).

Table B-4: Operation Code Field

Register Field

Register	External Event Line # B (Table B-6)	Bit 21	Bit 20
A	0	0	0
B	1	0	1
C	2	1	0
D	3	1	1

Table B-5: Register Field

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Condition Field

Condition	Bit 17-19	Bit 19	Bit 18	Bit 17
None	0	0	0	0
External event lines value > Register value	1	0	0	1
External event lines value < Register value	2	0	1	0
External event lines value = Register value	3	0	1	1
External event lines value <> Register value	4	1	0	0
External event line # B is Low*	5	1	0	1
External event line # B is High*	6	1	1	0
HALT when combined with PAUSE command	7	1	1	1

* *B* is determined by the Register field

Table B-6: Condition Field

Guidelines on How to Write Control Commands

When writing commands to a file or to the control memory, the following guidelines should be observed:

1. Commands other than NOP can reside every four steps. Micro code should be the same for all four steps except for I/O Groups Control direction and Operation Code. The Operation Code should be encoded only in the fourth step.
2. The direction can be changed at each step.
3. Control memory and output memory must be written to all boards, Master and Slave.

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Appendix C - Specifications

This section provides GC5050 DIO and Timing connector specifications.

GC5050 DIO Specifications

The following are specifications for GC5050 board:

Feature	Value
Timing	
Int. Test Clock	5Hz to 50MHz
Resolution, max	Greater of 1Hz or 0.2%
Int. B Block	1 to 120MHz
B Clock Resolution	0.2%
Internal Strobe Phase – Clock delay	4 - 18nS, 2nS steps
Ext.Test Clock	0 to 50MHz
Ext. Strobe	0 to 50MHz
Timing skew	3nS same card, 5nS between cards
Input/Output	
Data Direction control	Input or Output, fixed during execution
I/O channel width	32
Channels per board	8, 16 or 32 (programmable)
Output low level	See I/O Modules and Interface User Guide
Output high level	See I/O Modules and Interface User Guide
Source/Sink current	See I/O Modules and Interface User Guide
Input low level	See I/O Modules and Interface User Guide
Input high level	See I/O Modules and Interface User Guide
Memory depth, steps	256K to 1M
Trigger	Software, external override, or conditional
Pause	Software, external override, or conditional
External Status & Control	
Output Enable	Tri-state in 8-pin groups
Ext.Clock Enable	Internal, External and Select
Clock Output	As selected Test clock
External Strobe	As selected Input
External Event Bus	As selected 16 lines
Pause	As selected Override Input
Trigger	As selected Override Input
Run	As selected Indicator
B Clock	As selected Output
Power Requirements	
3.3V Typical Power (mA):	250
3.3V Maximum Power (mA):	600
5V Typical Power (A):	1.5
5V Maximum Power (A):	2.5
Environmental	
Operating Temp.	0 to 50°C

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Feature	Value
Storage Temperature	-20 to 70°C
Physical Properties	
Bus Interface	PCI
Dimensions	Full-Size PCI card
Weight	

Table C-1: GC5050 DIO Specifications

Timing Signals Specifications

The following are specifications for the Timing signals:

Parameter	Min	Typical	Max	Units
Internal Test Clock				
Freq. Range	5		50M	Hz
Resolution	The greater of 1 Hz or 0.2%.			
Internal B Clock				
Freq. Range	1		120	MHz
Resolution	The greater of 1 HZ or 0.2%.			
External Clock with Internal Strobe				
Freq. Range	0		50	MHz
Pulse width	8			ns
XCLK to OCLK delay	60		70	ns
XCLK to OSTB delay *	50		60	ns
Data setup time to XCLK **	12			ns
Data hold time to XCLK	5			ns
External Clock with External Strobe				
Freq. Range				
External Clock	0		50	MHz
External Strobe	0		50	MHz
Pulse width				
External Clock	8			ns
External Strobe	8			ns
XCLK to OCLK delay	50		60	ns
XSTB to OSTB delay	50		60	ns
Data setup time to XSTB **	12			ns
Data hold time to OSTB	5			ns
External Control Inputs				
Input Level High	2.0		5.1	V
Input Level Low	-0.1		0.8	V
Input Current High			10	mA
Input Current Low			10	mA
External Control Outputs				
Type	74FCT162245T			
Output Level High	2.4		2.4	V
Output Level Low		0.35	0.6	V
Output Current High			20	mA

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Parameter	Min	Typical	Max	Units
Output Current Low			20	mA

* Timing depends on the strobe delay setting and typically is XCLK to OCLK timing minus strobe delay setting.

** Setup time depends on the selected memory and is given for a typical configuration.

Table C-2: Timing connector Specifications

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