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GTDIO

GT-DIO Product Family

GX5280

Dynamic Digital I/O PXI Cards

User's Guide

Last Updated August 14, 2013

MARVIN TEST SOLUTIONS

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Chapter 1 - Introduction

About This User Guide

This User Guide provides information needed to install, configure, program and use Marvin Test Solutions' GX5280 digital I/O (DIO) boards. Supporting boards such as I/O modules, accessories and software are discussed in related User Guides.

Required User Knowledge and Skills

This User Guide assumes a general knowledge of PC-based computers and some knowledge of electronics.

Scope and Organization

The User Guide is organized as follows:

Chapter	Content
Chapter 1	**Introduction** – Introduces this User Guide.
Chapter 2	**Overview** – Summarizes DIO GX5280 family, board features, architecture, hardware and driver.
Chapter 3	**Installation and Setup** – Furnishes step-by-step directions for installing and setting up the software and hardware.
Chapter 4	**Theory of Operation** – Provides a functional hardware description.
Appendix A	**Connectors** – Supplies connector definitions and pin assignments.
Appendix B	**Specifications** – Provides a summary of the GX5280's specifications.
Index	Provides a roadmap to important topics and concepts in this manual.

Related Documents

The following documents contain related information and are considered an integral part of this User Guide:

- DIO Software User Guide – Information about Panel and the ***DIOEasy*** Windows application and introduction to programming the board.
- DIO Programming Reference – Reference information about the DIO Driver library functions (API) and the DIO script objects.

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Style Conventions

Example	Description
Copy or Paste	Commands are indicated in bold type.
Shift+F1	Keys are often used in combination. The example to the left instructs the user to hold down the shift key while pressing the FI key at the same time. When key combination instructions are separated by commas (such as ALT+D, A), hold the ALT key while pressing D, then press A.
Direction Keys	Refer to the up arrow (↑), down arrow (↓), right arrow (→), and left arrow (←) keys.
cd **bold**	Bolded text must be entered from the keyboard exactly as shown.
cd *directory name*	Italicized text is a placeholder for variables or other items the user must define and enter from the keyboard.
`examples`	Examples and source code are indicated in Courier, a fixed pitch font.
0x*hexnumber*	An integer in hexadecimal notation, for example, 0x10A equals 266 in decimal.

Definitions

The following table defines terms commonly used in this document:

Term	Definition
DIO	Digital Input/Output (I/O).
DIO board	Generically, any of Marvin Test Solutions' digital Input/Output circuit boards in any board family. The context could restrict it to the GX5280 family.
GX5280 domain	A system based on GX5280 Master & Slave boards. These include I/O Module daughter boards, and associated cables and software.
Master board	Refers specifically to the GX5280 DIO circuit board when used as a Master.
Slave or GX5280 board	Refers specifically to the GX5280 DIO circuit board when used as a Slave.
I/O User Guide	The *DIO I/O Modules and Interface User Guide*
Step	One in a sequence of test intervals. DIO boards run through a programmed sequence of steps.
Software User Guide (or variants)	The *DIO Software User Guide and Programming Reference* provided with GX5280 DIO boards.
Testware	Test software. It includes test vectors loaded and run on the DIO system, as well as driver commands used to load the boards and read results.
Vector or Test vector	A sequence of stimuli applied to the pins of a unit under test.
VHD connector	Very High Density. Used to describe a SCSI 3 type connector with very small pin spacing.

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Chapter 2 - Overview

Introduction

The GX5280 Series are high performance, cost-effective 3U PXI dynamic digital I/O boards with 32 TTL I/O channels and 32 LVDS I/O channels. The GX5280 Series offers an industry leading 512MB of on-board memory and allows test rates up to 200 MHz (GX5283 Only). The single board design supports both master and slave functionality without the use of add-on modules. Channels direction can be programmed on a per byte basis, i.e. Group 0 (channels 0 -7) can be set as output while Group 1 (channels 8 -15) can be set to be input etc. Output channels data is present on both LVDS and TTL Standard level I/O connectors. If the specified group is in input mode, the user can select (software) which input interface to activate, i.e. LVDS or level (one of 3.3. 1.8, 1.5, 2.5). The GX5280 Series utilize the PXI Local Bus to distribute signals across a domain.

All GX5280 cards offer programmable I/O width - trading vector width for vector depth. The GX5283 vector memory can be configured to support channel widths of 32, 16, 8, 4, 2 and 1 (single channel) with corresponding vector depths of 128M steps, 256M steps, 512M steps, 1G steps, 2G steps and 4G steps. The GX5282 vector memory can be configured to support channel widths of 32, 16, 8, 4, 2 and 1 (single channel) with corresponding vector depths of 64M steps 128M steps, 256M steps, 512M steps, 1G steps and 2G steps. The GX5281 vector memory can be configured to support channel widths of 32, 16, 8, 4, 2 and 1 (single channel) with corresponding vector depths of 32M steps 64M steps, 128M steps, 256M steps, 512M steps and 1G steps.

Marvin Test Solutions' DIO is a family of high-speed, programmable, dynamic Digital Input and Output (I/O) boards. These boards perform high-speed automated functional testing, device testing, simulation and data acquisition. The DIO family provides real-time digital pattern capture and generation with 32 channels per card and up to 16 cards or 512 channels.

The DIO family uses common software development tools to develop test vector files. The test vector files contain digital patterns sent to or received from the Unit Under Test (UUT) and specific pre-defined setting for each board in the setting.

Using ***DIOEasy*** or DIO driver functions, the development of vector files can be done without using the actual hardware**.** Vector file verification requires the DIO be installed and properly configured.

Marvin Test Solutions bundles ***DIOEasy*** with all DIO products. ***DIOEasy***, Marvin Test Solutions' vector development and analysis software, allows manual control of the DIO hardware using the built-in DIO Virtual Instrument Panel. The DIO driver permits control of the DIO family from common software development tools such as Marvin Test Solutions' ***ATEasy***, Microsoft Visual Basic, Microsoft Visual C++, Borland C++, Borland Delphi and more.

DIOEasy, a Windows application used to develop digital vectors and does not require any programming experience or knowledge to operate.

Computer Bus Interface

The DIO Driver accesses Master, Slave and carrier boards through the computer's bus (see Figure 2-1). The driver can accommodate up to 16 masters (from either family) and each master can have up to 7 DIO slave boards. ISA based DIOs and carrier boards have switches to set their base address to identify by the driver where PCI and PXI boards are using the physical slot number they are installed in to identify by the driver. PXI and PCI boards Master and Slave numbers are set through selector switches located on the front.

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DIO Domains

A DIO domain has one Master DIO board and up to 15 DIO Slave boards. A DIO *domain* comprise of Master, its Slaves, Carriers and related modules. Figure 2-1shows two domains from two different families on a PC bus.

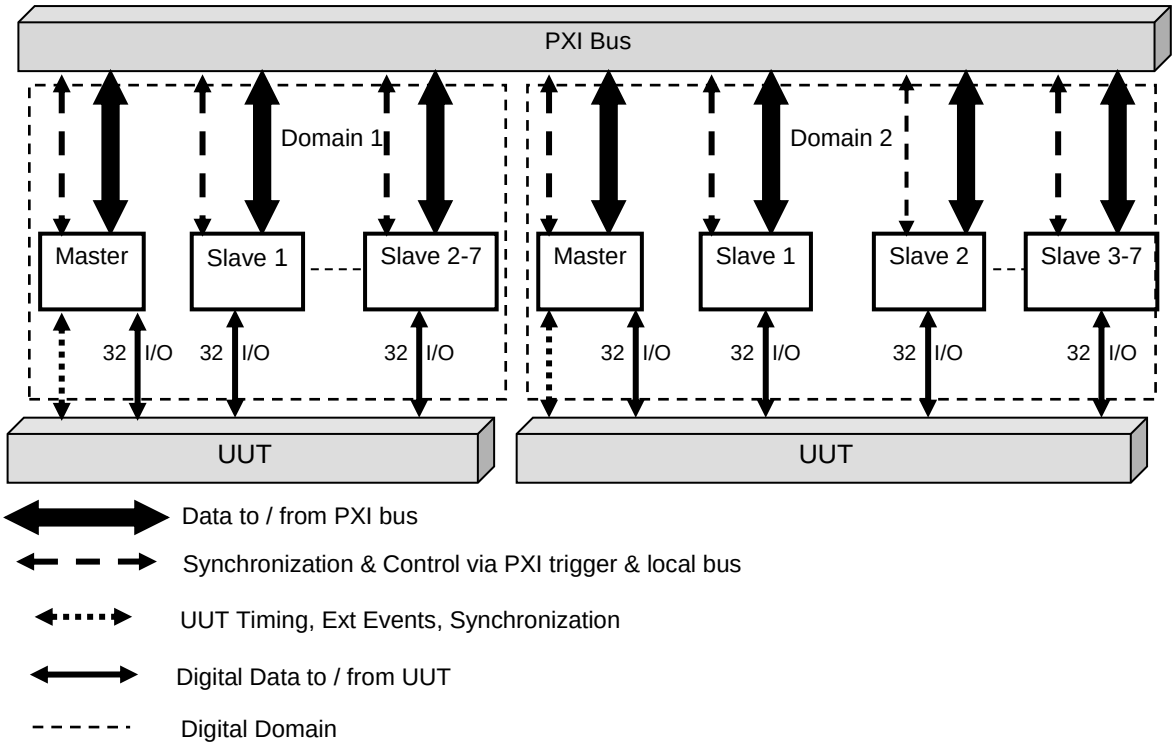


Figure 2-1: Two Different DIO Domains on One PC Bus

Domains are internally synchronized and controlled via the PXI local bus. To synchronize a domain with a UUT, you need to synchronize the Master board's Timing signals using the Master's Timing connector.

A full domain containing sixteen DIO boards provides up to 512 UUT I/O channels (512 channels *wide*). Because the driver supports 16 masters, up to 16 domains of mixed types can, in principle, be supported in a PXI system. The number of master/slaves depends on the number of available free PXI slots in your system.

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GX5280 Architecture and Capabilities

The following are key GX5280 characteristics and architecture:

- The GX5280 is a **Plug and Play (PnP)** board. The operating system (Windows 9x, Me, Windows 2000 or XP) automatically identify and arbitrate resource requirements as well as notify the user that a new board was found and automatically install the driver for it.
- DIO domain operates independently of the host computer when in RUN mode.
- Each GX5280 DIO board supports a maximum clock frequency of up to 200MHz (GX5283 Only) per channel for all channels.
- A GX5280 (Master) board controls the timing of its domain and can be synchronized to a UUT.
- Any GX5280 board can be transforms to be Master or Slave depends on the on-board switch settings (can only be done when the system is shutdown)
- Multiple Master boards are used to synchronize mutually asynchronous UUT elements.
- Each GX5280 Slave board adds 32 UUT channels. Up to 15 Slave boards can be added to make a total of 512 channel domain.
- Programmable channel's output enabled or disabled. Each channel can be enabled or disabled at any time through software control. Disabled channels in output mode are in Tri-State. This is useful for connecting to a user bus
- Each Master has a 16-bit external event bus. This bus is used for triggering and synchronization with external events.
- Multiple trigger sources are available: Programmed PXI Trigger line, Star Trigger, External Trigger, Internal trigger (software) or event driven trigger (generated by external events). All triggers sources can work in tandem.
- Event driven trigger can be generated by external events on the Timing connector External Event lines. Event and Mask registers are used to determine both the triggering event and the masking bits to be ignored. These use the D Event and D Mask registers and T Event and T Mask registers.
- External triggering can be initiated on sequential or concurrent events by using both D and T event registers to define events.
- Multiple pause sources are available: Programmed PXI Trigger line, External Pause, Internal pause (software) or event driven pause (generated by external events). All pause sources can work in tandem.
- The test sequence (vector) can be paused on external events unconditionally or conditionally. P Event and P Mask registers hold the condition and bits that generate a conditional pause.
- An X Register is used to emulate an External Event condition under program control for purposes of test program verification. The register is loaded through the computer bus.
- DIO domain can be set to have internal or external clock, in order to synchronize with the user UUT.
- DIO domain clock source (internal or external), active when outputting data, can be programmatically delayed by 0-24 nSec (increments of 4nSec).
- DIO domain Strobe source (internal or external), active when inputting data, can be programmatically delayed by 0-24 nSec (increments of 4nSec).
- All GX5280 Firmware can be upgraded through the DIO In-System- Programming (ISP).
- Direction can be programmed on a per byte basis, i.e. Group 0 (channels 0 -7) can be set as output while Group 1 (channels 8 -15) can be set to be input etc.

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- Programmable voltage level (applied for all 32 channels) in the TTL Standard connector.
- Dual Data I/O interface connectors providing dual output standards, LVDS and TTL Standard (3.3V, 2.5V, 1.8V or 1.5V), for each groups of channels when in Output mode.
- User programmable interface input selection, LVDS or TTL Standard (3.3V, 2.5V, 1.8V or 1.5V) for each groups of channels when in Input mode.
- User programmable PXI Star Trigger input state for Trigger and/or Pause.



Figure 2-2 GX5280: Complete View

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GX5280 Models and Accessories

The following GX5280 models are available:

- **GX5282** – 100 MHz Digital I/O Board with 512 MB of vector memory and LVDS levels.
- **GX5283** – 200 MHz Digital I/O Board with 512 MB of vector memory and LVDS levels.

The following GX5280 accessories are available:

- **GT95014** – Connector interface, SCSI to 100 Mil Grid, Single Ended I/F Board
- **GT95015** – Connector interface, SCSI to 100 Mil Grid, Differential I/F Board
- **GT95021** – 2’ shielded cable (68-pin SCSI)
- **GT95022** – 3’ Shielded cable (68-pin SCSI)
- **GT95028** – 10’ Shielded cable (68-pin SCSI)
- **GT95031** - 6’ Shielded cable (68-pin SCSI)

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Chapter 3 - Installation and Setup

Getting Started

This section includes general hardware installation procedures for the GX5280 board and installation instructions for the GTDIO software. Before proceeding, please refer to the appropriate chapter to become familiar with the board being installed.

To Find Information on…	**Refer to…**
GTDIO Software Installation	This Chapter
Hardware/Board Installation	This Chapter
Using the GTDIO Panel	This chapter and the DIO Software User's Guide
Using DIOEasy	DIO Software User's Guide
Programming the Board	DIO Software User's Guide and the DIO Programmer's Reference manuals

Packing List

Check the package against the packing list and your purchase order and make certain all purchased items are included. A DIO board package includes required items and may include options and accessories listed below:

Part Name/Description	**Part Function**	**Part Number**
DIO board	Digital input/output and domain timing and control.	GX5280
GTDIO software installation file (GTDIO.exe)	Installation of software driver, DIOEasy, examples on-line help and documentations (in PDF format) files.	N/A
Connector Interface for GX5280, SCSI to 100 Mil Grid, Single Ended	UUT I/O Interface	GT95014
Connector Interface for GX5280, SCSI to 100 Mil Grid, Differential	UUT I/O Interface	GT95015
2' shielded cable for GX5280 (68 Pin)	UUT I/O Cable	GT95021
3' shielded cable for GX5280 (68 Pin)	UUT I/O Cable	GT95022
6' shielded cable for GX5280 (68 Pin)	UUT I/O Cable	GT95031
10' shielded cable for GX5280 (68 Pin)	UUT I/O Cable	GT95028

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Unpacking and Inspection

After removing the board from the shipping carton:

 **Caution -** Static sensitive devices are present. Ground yourself to discharge static.

1. Remove the board from the static bag by handling only the metal portions.
2. Be sure to check the contents of the shipping carton to verify that all of the items found in it match the packing list.
3. Inspect the board for possible damage. If there is any sign of damage, return the board to Marvin Test Solutions immediately. Please refer to the warranty information at the beginning of the manual.
4. Return the board to its anti-static bag until ready for installation and setup.

System Requirements

All GX5280 instrument boards are designed for use with a 3U or 6U cPCI or PXI compatible chassis. The software is compatible with any computer system running Windows 98, Windows Me, Windows 2000, Windows XP, Windows VISTA (32 bit) operating systems.

Each board requires one unoccupied 3U PXI bus slot.

Installation of the GTDIO Software

Before installing the board it is recommended to install the software as described in this section:

1. Insert the Marvin Test Solutions CD-ROM and locate the **GTDIO.EXE** setup program. If you computer's Auto Run is configured, when inserting the CD a browser will show several options, select the Marvin Test Solutions Files option, then locate the setup file. If Auto Run is not configured you can open the Windows explorer and locate the setup files (usually located under \Files\Setup folder). You can also download the file from Marvin Test Solutions web site (www.MarvinTest.com).
2. Run the setup and follow the instruction on the Setup screen to install the software.

   Note: When installing under Windows 2000/XP/VISTA, you may be required to restart the setup after logging-in as a user with an Administrator privileges. This is required in-order to upgrade your system with newer Windows components and to install kernel-mode device drivers (HW.SYS and HWDEVICE.SYS) required by the GTDIO driver to access resources on your board.
3. The first setup screen to appear is the Welcome screen. Click **Next** to continue.
4. Enter the folder where software is to be installed. Either click **Browse** to set up a new folder, or click **Next** to accept the default entry of `C:\Program Files\Marvin Test Solutions\GTDIO`.
5. Select the type of Setup you wish and click **Next.** You can choose between **Typical**, **Run-Time** and **Custom** setups. **Typical** setup type installs all files. **Run-Time** setup type will install only the files required for controlling the board either from its driver or from its virtual panel. **Custom** setup type lets you select from the available components.

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The program will now start its installation. During the installation, Setup may upgrade some of the Windows shared components and files. The Setup may ask you to reboot after it complete if some of the components it replaced where used by another application during the installation – do so before attempting to use the software.

You can now continue with the installation to install the board. After the board installation is complete you can test your installation by starting a panel program that let you control the board interactively. The panel program can be started by selecting it from the Start, Programs, GTDIO menu located in the Windows Taskbar.

Overview of the GTDIO Software

Once the software installed, the following tools and software components are available:

- **PXI/PCI Explorer applet** – use to configure the PXI chassis, controllers and devices. This is required for accurate identification of your PXI instruments later on when installed in your system. The applet configuration is saved to PXISYS.ini and PXIeSYS.ini that are used by Marvin Test Solutions instruments, the VISA provider and VISA based instruments drivers. In addition, the applet can be used to assign chassis numbers, Legacy Slot numbers and instruments alias names.

  VISA is a standard maintained by the VXI Plug & Play System Alliance and the PXI Systems Alliance organizations (http://www.vxipnp.org/, http://www.pxisa.org/). VISA provides a standard way for instrument manufacturers and users to write and use instruments drivers. The VISA resource managers such as National Instruments **Measurement & Automation** (NI-MAX) can display and configure instruments and their address (similar to Marvin Test Solutions' PXI/PCI Explorer).

- **GTDIO Panel** – use to configure, control and display the board settings.
- **DIOEasy** – Windows application for creating and analyzing vector files used by DIO boards.
- **GTDIO driver** – a DLL (GTDIO32.DLL) located in the Windows System folder used to program and control the board.
- **Programming files and examples** – interface files and libraries for various programming tools, see later in this chapter for a complete list of files, programming languages and development tools supported by the driver.
- **Documentation** – On-Line help and User's Guide.

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Configuring Your PXI System using the PXI/PCI Explorer

To configure your PXI/PCI system using the **PXI/PCI Explorer** applet follow these steps:

1. **Start the PXI/PCI Explorer applet**. The applet can be start from the Windows Control Panel or from the Windows Start Menu, **Marvin Test Solutions**, **HW**, **PXI/PCI Explorer**.
2. **Identify Chassis and Controllers**. After the PXI/PCI Explorer started it will scan your system for changes and will display the current configuration. The PXI/PCI Explorer automatically detects systems that have Marvin Test Solutions controllers and chassis. In addition, the applet detects PXI-MXI-3/4 extenders in your system (manufactured by National Instruments). If your chassis is not shown in the explorer main window, use the Identify Chassis/Controller commands to identify your system. Chassis and Controller manufacturers should provide INI and driver files for their chassis and controllers to be used by these commands.
3. **Change chassis numbers, PXI devices Legacy Slot numbering and PXI devices Alias names.** These are optional steps to be performed if you would like your chassis to have different numbers. Legacy slots numbers are used by older Marvin Test Solutions or VISA drivers. Alias names can provide a way to address a PXI device using your logical name (e.g. "DIO1"). For more information regarding these numbers see the **DioSetupInitialization** and **DioSetupInitializationVisa** functions in the DIO Programming User's Guide.
4. **Save you work**. PXI Explorer saves the configuration to the following files located in the Windows folder: PXISYS.ini, PXIeSYS.ini and GxPxiSys.ini. Click on the **Save** button to save you changes. The PXI/Explorer prompt you to save the changes if changes were made or detected (an asterisk sign ' *' in the caption indicated changes).

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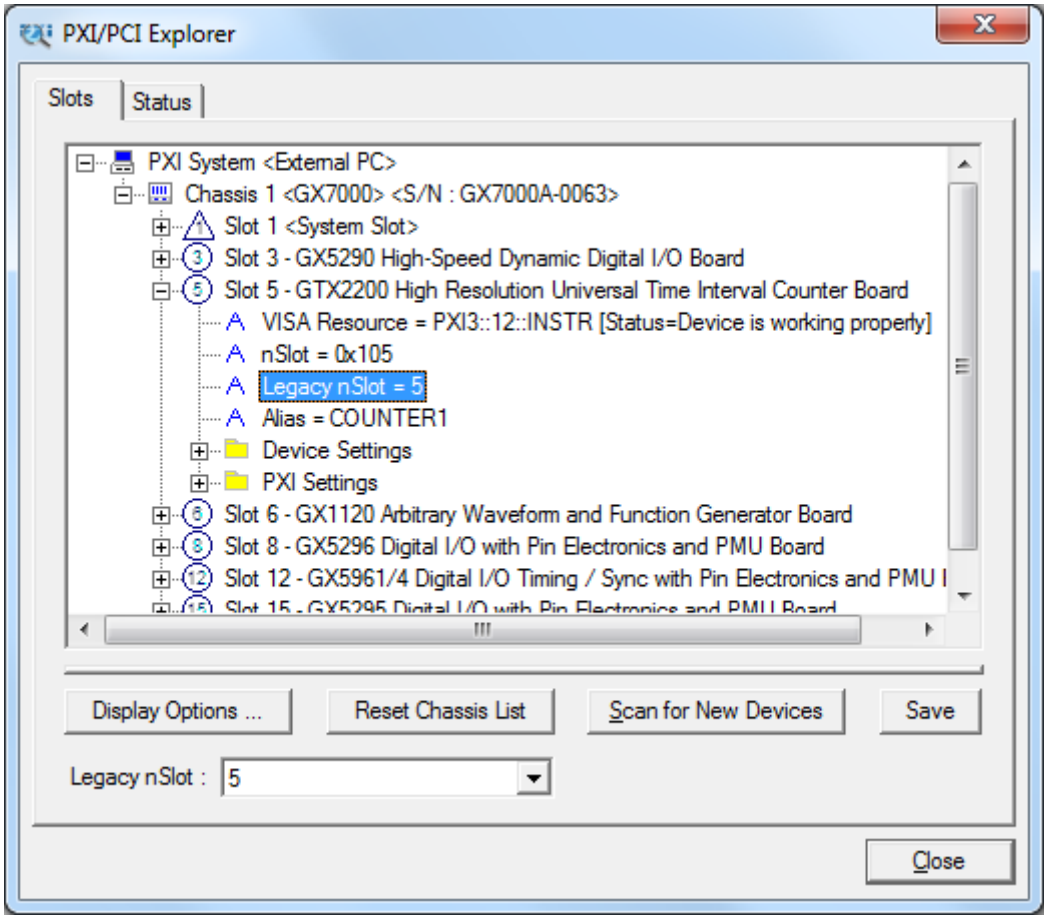


Figure 3-1: PXI/PCI Explorer

Board Installation

Before you Begin

- Install the GTDIO software as described in the prior section.
- Configure your PXI/PC system using **PXI/PCI Explorer** as described in the prior section.
- Verify that all the components listed in the packing list (see previous paragraph) are present.

Electric Static Discharge (ESD) Precautions

To reduce the risk of damage to the board, the following precautions should be observed:

- Leave the board in the anti-static bags until installation requires removal. The anti-static bag protects the board from harmful static electricity.
- Save the anti-static bag in case the board is removed from the computer in the future.
- Carefully unpack and install the board. Do not drop or handle the board roughly.

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- Handle the board by the edges. Avoid contact with any components on the circuit board.

Caution - Do not insert or remove any board while the computer is on. Turn off the power from the PXI chassis before installation.

Board Selector Switch Settings

Any DIO domain is based on a single Master board and additional Slaves boards. The slaves are basically an expansion of the number of channels in the domain. Each board needs to have a unique number so it can be identify by the software as part of the specified domain, i.e. all Slave boards that belongs to the same Master are in the same domain. You must setup the domain by setting the Master and Slave selectors as shown in Figure 3-2.

Master — The selector switch designated as "Master" sets the Master domain that the board belongs to. The adjacent selector switch (designated as "Slave") needs to be set to 0.

Slave — The selector switch designated as "Master" sets the Master domain that the Slave board belongs to. The selector switch designated as "Slave", select the Slave number in that domain and can be set to any number from 1 to 7 for a total of 7 Slaves (number 0 is saved for the Master).

1. Set unique board number for each new DIO board using the selector switch on the front.
2. Lay boards out in slot order with the master in the middle (the Master should have equal number of Slaves from both sides).

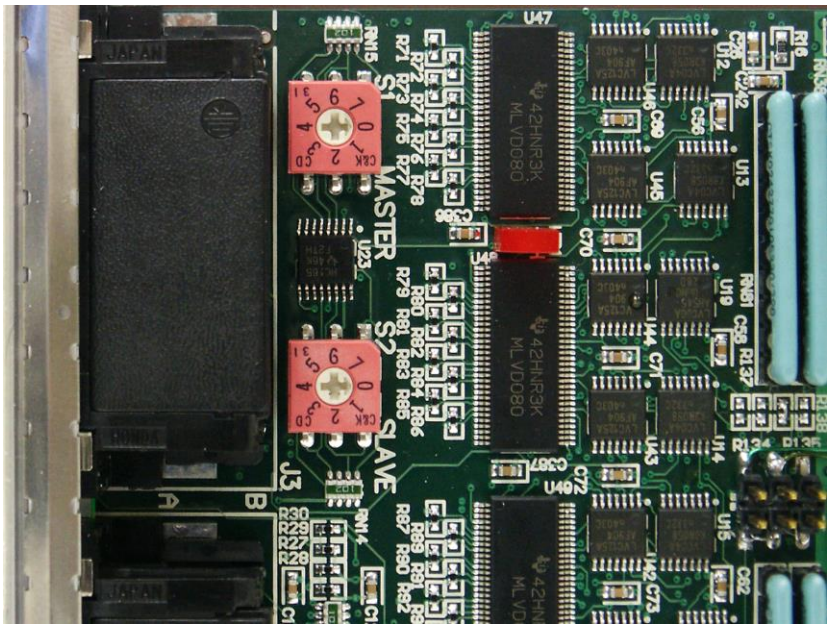


Figure 3-2: Master and Slave Switch Selectors

Installing a Board

Install each of the boards as follows:

1. Turn off the PXI chassis and unplug the power cord.
2. Locate a PXI empty slot on the PXI chassis.
3. Place the module edges into the PXI chassis rails (top and bottom).

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4. Carefully slide the PXI board to the rear of the chassis, make sure that the ejector handles are pushed **out** (as shown in Figure 3-3).

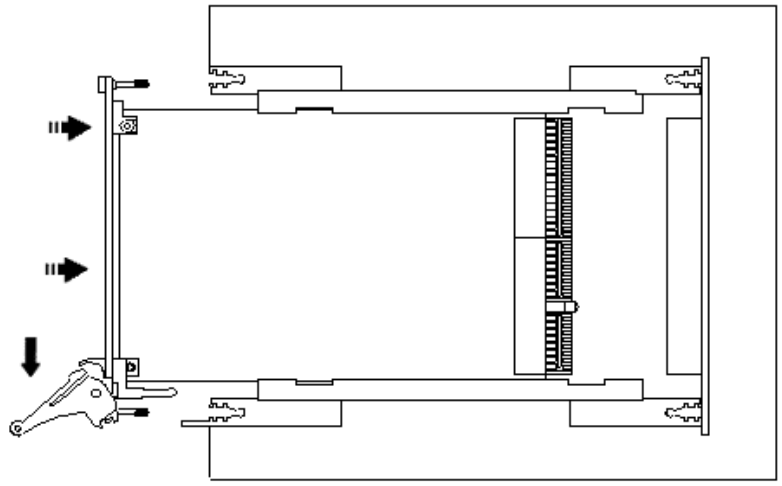


Figure 3-3: Ejector handles position during module insertion

5. After you feel resistance, push in the ejector handles as shown in Figure 3-4 to secure the module into the frame.

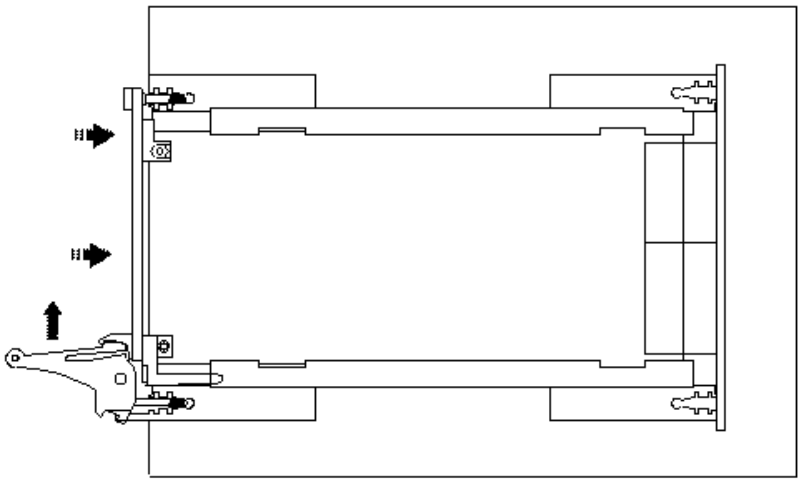


Figure 3-4: Ejector handles position after module insertion

6. Tighten the module's front panel to the chassis to secure the module in.
7. Connect any necessary cables to the board.
8. Plug the power cord in and turn on the PXI chassis.

Plug & Play Driver Installation

Plug & Play operating systems such as Windows 9x, Me, Windows 2000 or XP (Not Windows NT) notify the user that a new board was found using the **New Hardware Found** wizard after restarting the system with the new board.

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If another Marvin Test Solutions board software package was already installed, Windows will suggest using the driver information file: HW.INF. The file is located in your Program Files\Marvin Test Solutions\HW folder. Click **Next** to confirm and follow the instructions on the screen to complete the driver installation.

If the operating system was unable to find the driver (since the software driver was not installed prior to the board installation), you may install the software as described in the prior section, then click on the **Have Disk** button and browse to select the HW.INF file located in C:\Program File\Marvin Test Solutions\HW.

If you are unable to locate the driver click **Cancel** to the found New Hardware wizard and exit the New Hardware Found Wizard, install the DIO driver, reboot your computer and repeat this procedure.

The Windows Device Manager (open from the System applet from the Windows Control Panel) must display the proper board name before continuing to use the board software (no Yellow warning icon shown next to device). If the device is displayed with an error you can select it and press delete and then press F5 to rescan the system again and to start the New Hardware Found wizard.

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Removing a Board

Remove the board as follows:

1. Turn off the PXI chassis and unplug the power cord.
2. Locate a PXI slot on the PXI chassis.
3. Disconnect and remove any cables/connectors connected to the board.
4. Un-tighten the module's front panel screws to the chassis.
5. Push out the ejector handles and slide the PXI board away from the chassis.
6. Optionally - uninstall the software by running the setup again (or from the Windows Control Pane, Programs and Features or Add Remove Programs applet) and selecting Remove/Uninstall.

Verifying the Installation

To verify proper DIO board installation, install the software first, and then use the Panel to configure the driver and initialize the board. To access the Panel, GTDIO software must be installed. Run the panel by selecting **Marvin Test Solutions**, **GTDIO**, **DIO Panel** from the Windows Start menu.

Initializing DIO Boards

A DIO board installation is successful if the driver configuration database can be updated and all boards can be initialized.

When software installation is complete, do the following to configure and initialize the new boards.

1. Run PXI/PCI Explorer from the Windows Control Panel or from the Windows Start menu, Marvin Test Solutions, HW, PXI/PXI Explorer.
2. Make sure that your chassis is configured as described in configuring your PXI System using PXI/PCI Explorer. Locate your DIO board under PXI/PCI Explorer note the chassis number and the slot number it appears under.
3. Configure the DIO boards according to the procedure at **Chapter 3 - GTDIO Panel** in the **DIO Software User's Guide.**
4. Click **Initialize** to accept the domain configuration.
5. If the new DIO board(s) can be successfully configured and initialized, installation is successful, the memory density and number of SIMMs displays for each board.

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Chapter 4 - Theory of Operation

This chapter presents the theory of operation for the GX5280 boards, with an overview of operation and a simple description of operation for one channel (I/O pin). Other topics covered in this chapter are:

- Architecture Diagram.
- Operation of clock (CLK) and strobe signals.
- Memory management.
- Vector Program Control.
- Basic states of operation.
- Trigger operation.
- Pause operation.

Architecture

The GX5280 can run at frequencies as high as 200MHz (See specifications) feature three deep onboard memory options: 32, 64, or 128 Mbit/Channel. Each board contains 32 I/O pins arranged in 4 groups of 8, each group having its own direction either input or output applied to all steps in the group. The I/O stage can be software-configured to interface with a broad set of common logic families of 5,0 V, 3,3 V, 2,5 V and 1,8 V. as well as additional dedicated LVDS I/O stage connector. In addition the I/O voltage stage can be programmed with 10 mV resolution ranges from 1.4V to 3.6V. The programmed voltage level determines the logic high level for channels programmed to output mode and defines the threshold level for channels defined as input.

The GX5280 works as a complex programmable state machine with three main states: **HALT**, **PAUSE** and **RUN**. The central module of the board is the Vector Program Control. The Vector Program Control interprets predefined commands, controls the states machine and monitors the complex Trigger/Pause mechanism.

External control provides CLK, strobe and I/O pin direction from an external source. The combination of the external bi-directional control and external clocking, strobing, and triggering provides the capability to fully synchronize with UUTs and to minimize initialization procedures. The board sequencer permits the creation of conditional and unconditional loops and branches to manipulate the output vectors. This provides the capability to generate indefinite stimulus vectors at the maximum test rate.

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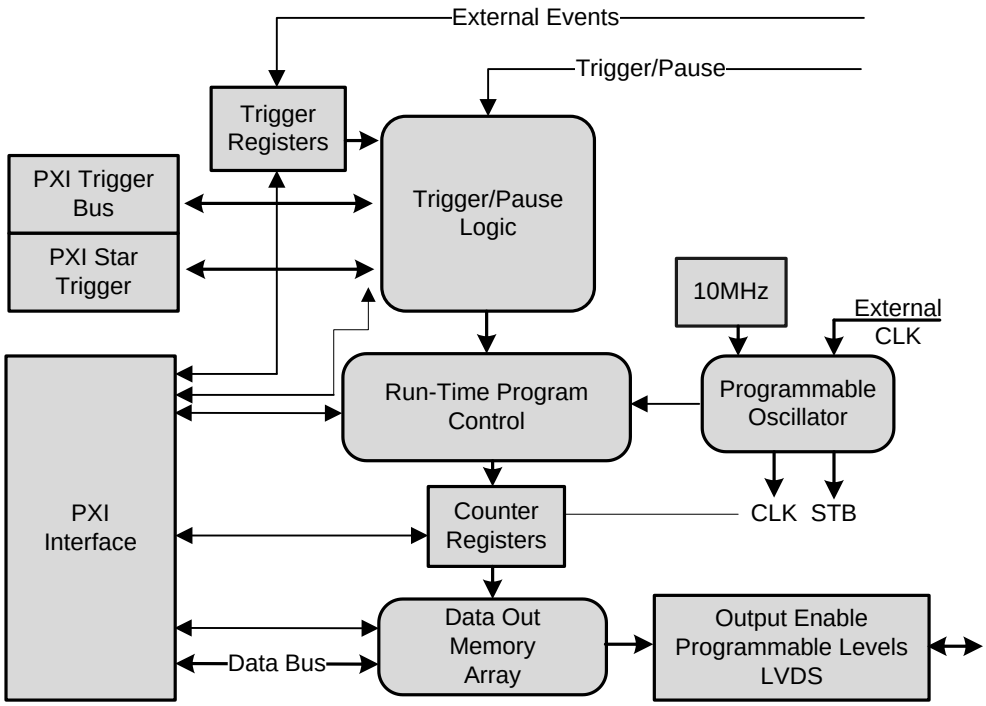


Figure 4-1: Architecture Diagram

Masters and Slaves

The DIO System (a DIO Domain) is made up of Master and Slave(s) circuit boards. The Master board can be connected to a maximum of 15 Slave boards expanding the number of channels in the domain. All external inputs, external clocks/strobes and controls are done primarily through the Master only.

The Master distributes clock, control and status signals to all the Slaves in the domain through the PXI Bus.

Any GX5280 board can be a Master or a Slave depends on the on-board switch settings (see Chapter 3). Although Master/Slave transformation can only be done when the system is shutdown.

I/O Channels

The operation of a GX5280 board is best understood by studying the operation of a single I/O channel.

Figure 4-2 displays a simplified block diagram of a single I/O channel. This diagram shows how one channel functions.

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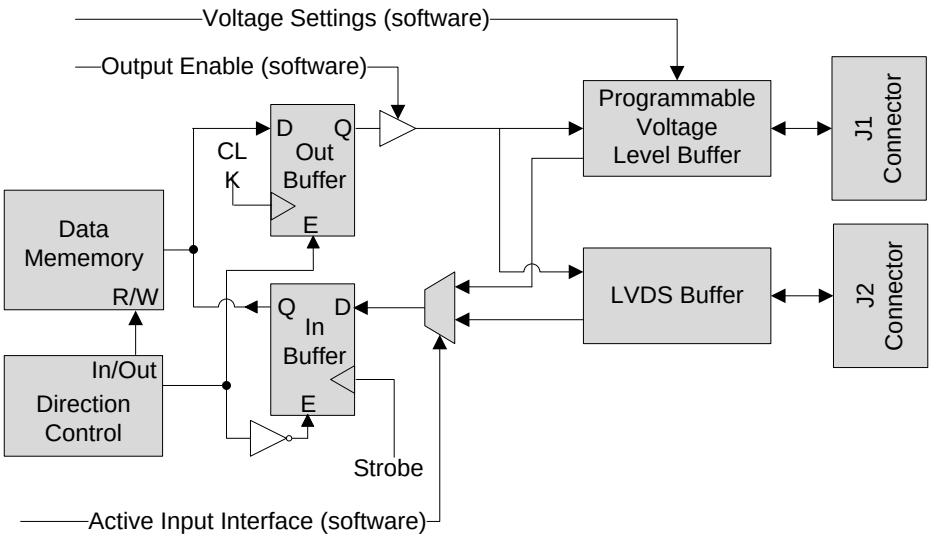


Figure 4-2: I/O Channel Block Diagram

Channel is set to be in output mode

The Channel's Direction control is set to output through software enabling the Out Buffer and disables the In Buffer. At the Out Buffer output there is an Output Enable Driver that is controlled by software. The output signal is then being fed into two buffers: Programmable Voltage Level Buffer and LVDS Buffer. Both buffers will output the signals to both J1 and J2 connectors. The out signal that goes through the Programmable Voltage Level Buffer its Output logic high voltage level can be programmed using software (see specification for details). Data is going to be latched to both J1 and J2 connectors on every rising Clock (when in RUN mode).

Channel is set to be in input mode

The Channel's Direction control is set to input through software enabling the In Buffer and disables the Out Buffer. The In Buffer input signal source can be programmed to be J1 or J2 input. If selecting the Programmable Voltage Level Buffer, the threshold can be programmed using software (see specification for details). Data is going to be latched into memory on every rising Strobe (when the DIO is in RUN mode).

Programmable Voltage Level Buffer and LVDS Buffer. Both buffers are outputting in tandem to both J1 and J2 connectors. The out signal that goes through the Programmable Voltage Level Buffer its Output logic high voltage level can be programmed using software (see specification for details). Data is going to be latched to both J1 and J2 connectors on every rising clock (when the DIO is in RUN mode).

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Clock and Strobe Signals

The clock (CLK) signal initiates each output vector. The rate of this signal can be programmed from 5Hz to 100MHz. Similarly, the strobe signal latches the input vector. All clock and strobe signals are distributed to all DIOs.

The GX5280's clock architecture provides the user with the flexibility to align signals between the DIO and the Unit Under Test (UUT) using delay settings. Figure 4-3 is a block diagram of the clock architecture which includes programmable delays for the DIO clock and strobe. The clock signal is used to output test vectors, and strobe (clock) data into the DIO's record memory. The basic architecture of the clock delay generator provides seven coarse delays in 4 ns steps. In addition a fine resolution delay (vernier) is available which provides a 0ns to 3ns delay in 250ps steps. Together, these elements provide delays in the range of 0ns to 27ns, with 250ps resolution for the data out and data input clocks.

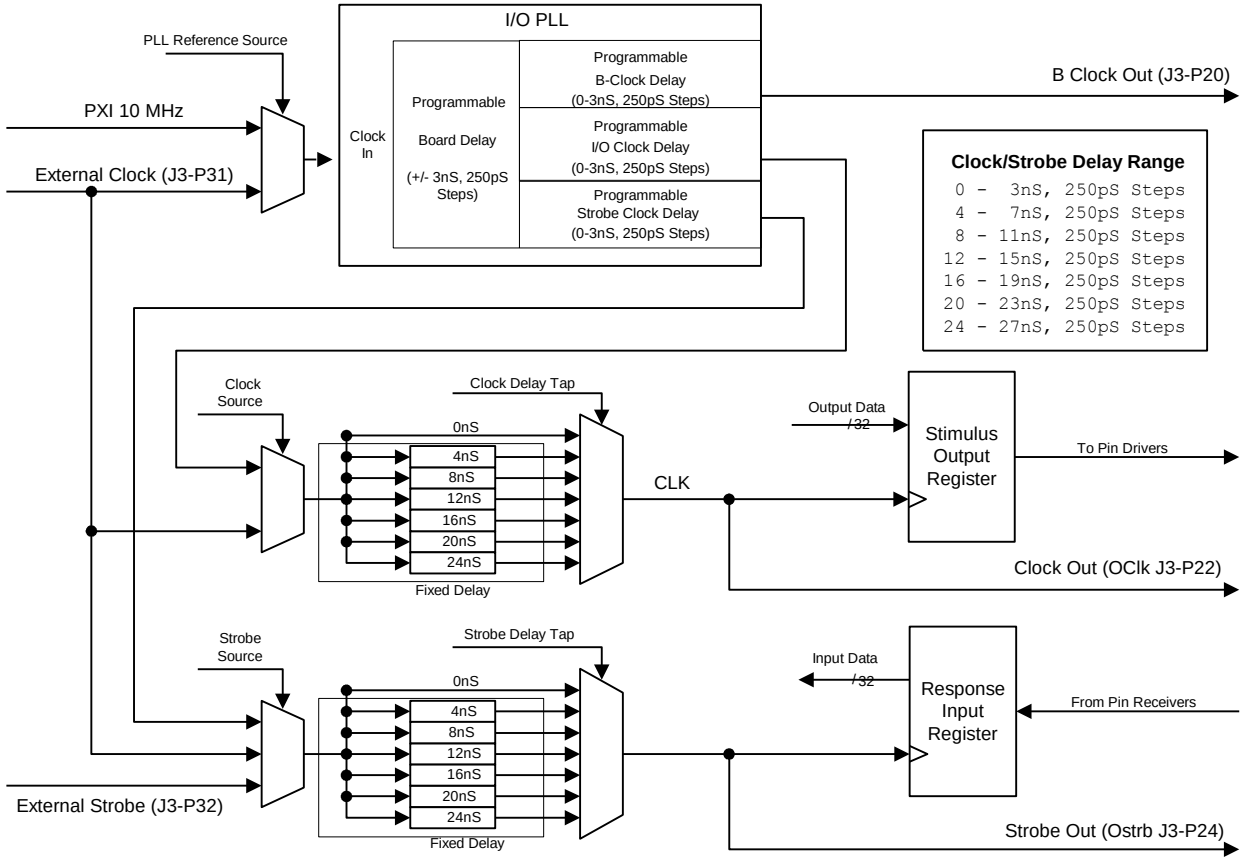


Figure 4-3: Clock Source Block Diagram

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Three clock signals are available for clocking input and output data:

O Clock	The DIO sends output patterns to the I/O connector on the rising edge of the Clock (OCLK) signal. The Clock can have a delay of 0-27 nSec (with increments of 250 pSec) relative to the Out clock source.
Out Clock	This clock signal has the same source and frequency as the Clock without time delay. This is only an internal signal.
Strobe	The DIO captures input patterns from the I/O connector on the rising edge of Strobe (STB). When the Strobe source signal is internal, it has the same frequency as the Clock signal. The Strobe Clock can have a delay of 0-27 nSec (with increments of 250 pSec) relative to the Out clock source. The timing diagram in Figure 4-4 displays Out CLK and Strobe signals. The DIO board can be driven using either internal or external clock sources. In internal mode, Strobe occurs Ts nanoseconds before the next clock (CLK) signal (8 nSec default). Ts can be set from 0 – 24 nanoseconds before the Out CLK signal. In the external mode, Clock or Strobe signals are provided externally.

A timing diagram of the CLK and Strobe signals is shown in Figure 4-4.

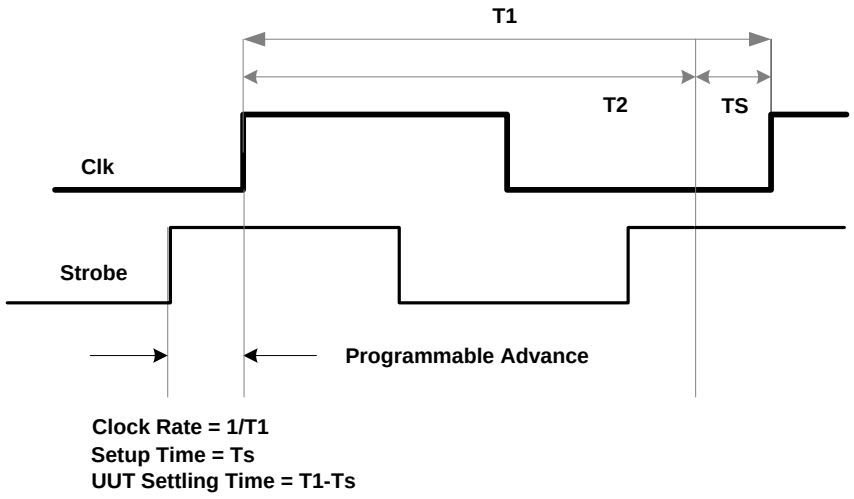


Figure 4-4: Signal Timing Diagram

Memory Management

The memory subsystem is composed of four blocks each of which can be separately configured as an input or an output. This configuration provides for presetting channels in groups of eight to either be input or output. All memories can be as large as 128Mb per channel with a sustained throughput of more than 100Mbits/Sec.

The memory subsystem is connected via the FPGA to the PXI bus at full bandwidth, for fast download or upload of vectors between the host computer and the GX5280.

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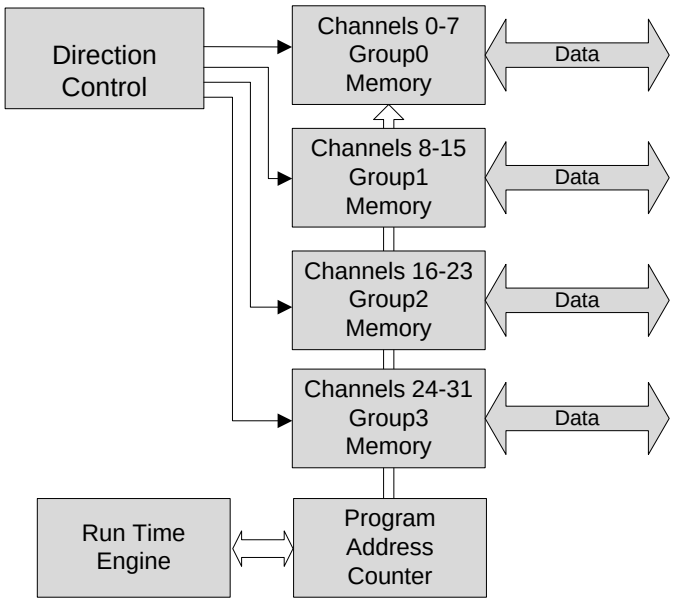


Figure 4-5: Memory Management Block Diagram

The Clock/Strobe signals and the Vector Program Control the program counter that contains the address of the current I/O memory. After resetting, the program counter points to address zero and increments with the Clock/Strobe signals signal towards the last memory address.

Vector Program Control

The Vector Program Control (Figure 4-6) is a high-speed Event Detection with Real-Time Response to those events unit controlling the program counter and the GX5280 state. The inputs to the Vector Program Control are:

- The 16-bit external events input lines or X register
- Trigger or Pause signals as processed by the Trigger/Pause logic.
- Software command control: Arm, Trigger, Pause, Halt, Step and Reset.
- External input lines: External Trigger, External Pause and External Jump.
- Predefined program commands to be processed in run time.

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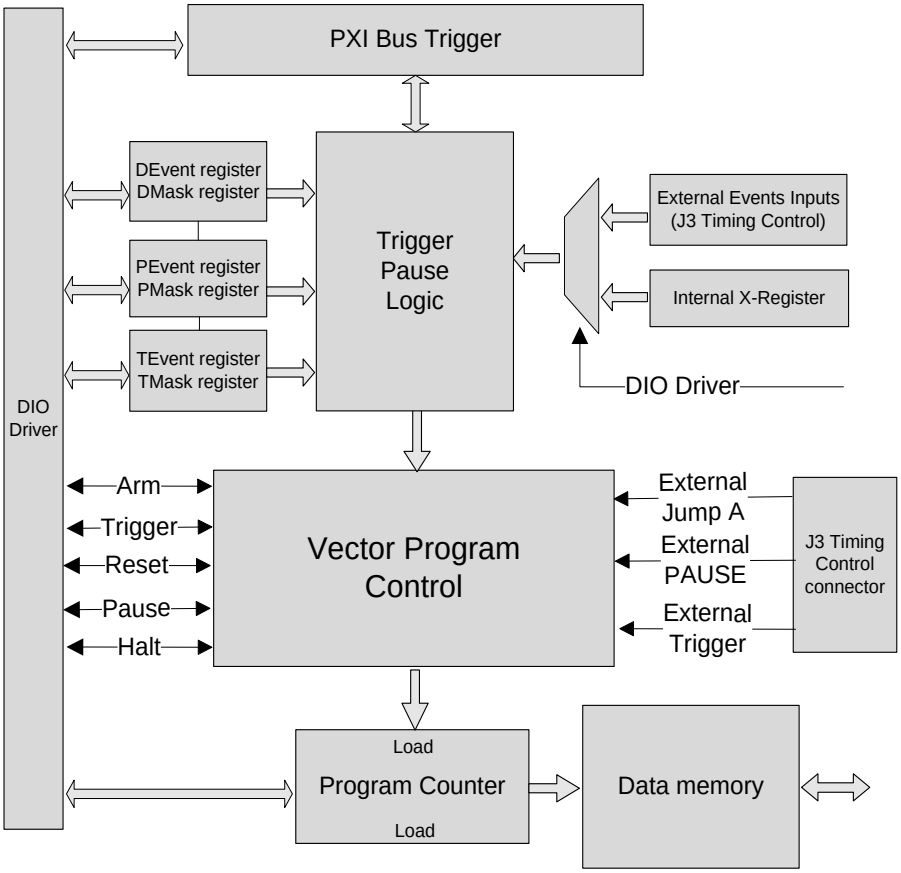


Figure 4-6: GX5280 Vector Program Control

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Vector Program Control States

The GX5280 Vector Program Control functions in three basic operational states; **Halt**, **Pause** and **Run**.

Figure 4-7 is a block diagram showing the relationship of these operational states.

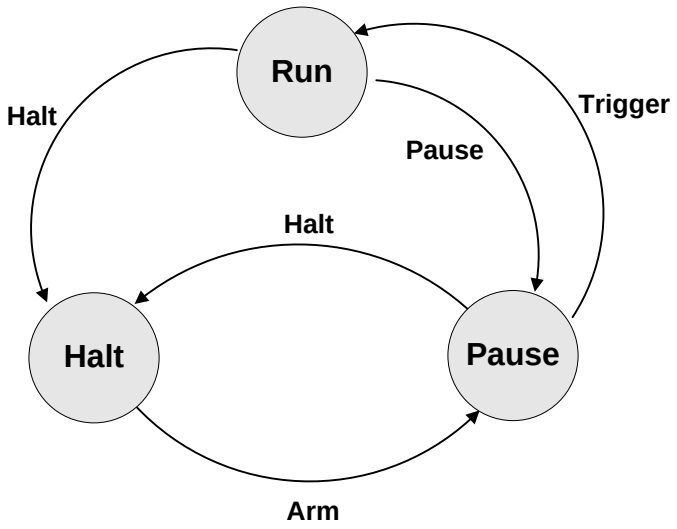


Figure 4-7: GX5280 Operational States

Halt State

The GX5280 Vector Program Control goes into a Halt state after a Reset signal and following the Halt command. All external event inputs as well as external control inputs are ignored following a Halt command. Following Reset, all I/O pin (channels) are in the receiving mode of operation. The program counter is zero, the frequency is set to an internal 10MHz, and the strobe timing is set to 5nSec.

Pause State

The Vector Program Control enters a Pause state from a Halt state with an ARM command sent by the PC bus, or from Run state following Pause command.

Run State

In the Run state, data is being output and input is being latched and the program counter holds the address of the current output. While running channels that are defined as output send the data from the memory located at the program counter address and the channels that are defined as input receive data.

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Trigger Command

The trigger command causes the board to change its state to the Run state and can be originate from the following sources:

- PC (software)
- External trigger control line
- External event lines (16 lines)
- PXI Trigger Bus Line.

PC (Software) Trigger

The software trigger originates within the PC. The PC bus trigger command takes effect immediately and overrides other established trigger conditions.

External Trigger

External Trigger Control Line

External triggers originate from the external trigger line. Pulling this line low causes the board to change its state to RUN. The external trigger line overrides other trigger conditions set for the GT-DIO board.

External Event Lines

It is also possible to set a conditional trigger command, which is activated upon receiving external event input lines. This external event may be any expected value on all or part of the external event input lines. The 16 external event lines are ANDed with pre-defined masks and compared with pre-defined events in registers D and T.

The external events trigger function is shown in Figure 4-8.

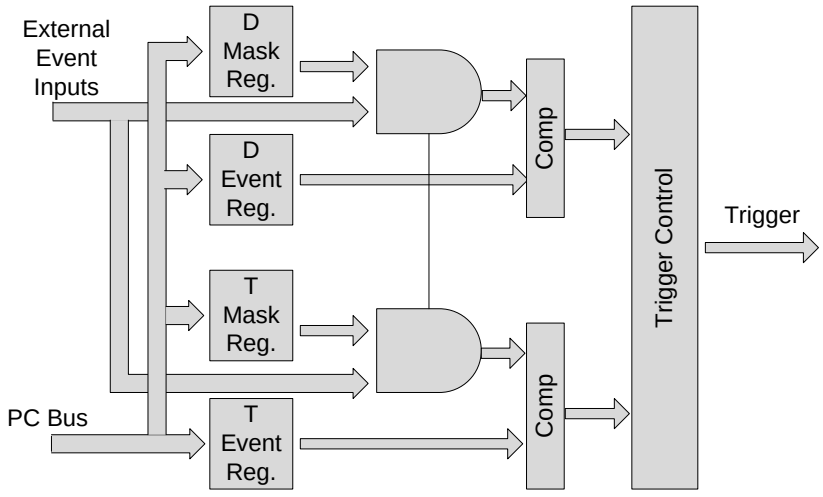


Figure 4-8: External Events Trigger Block Diagram

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The external events trigger can be set to one or two levels. In the one level mode, the trigger will be generated after the external condition has been met with the D or T event mask registers. In the two level mode, the board will wait for two sequential events to be met before issuing the trigger signal (D first, T second or opposite).

PXI Trigger Bus Line Trigger

Controlled by software the GX5280 can be programmed to trigger on any one of the PXI Trigger Bus Lines. The programmed selected PXI Trigger Bus Line can then be Enabled/Disabled through software control achieving additional control over the PXI Trigger Bus event.

Pause Command

The pause command causes the board to change its state to the Pause state and originates from the following sources:

- PC (Software).
- External control line
- External events line
- PXI Trigger Bus Line Pause

PC (Software) Pause

The software Pause originates within the PC. The PC bus Pause command takes effect immediately and overrides other established trigger conditions.

External Pause

External Pause Control Line

External pause originates from the external pause line. Pulling this line low will cause an immediate pause. The external pause overrides other pause conditions set to the GT-DIO board.

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External Pause Event Lines

The P mask and event registers can be used to create conditional pauses that depend on external event lines. The 16 external event lines are ANDed with pre-defined masks and compared with pre-defined events in register P.

The external/internal events pause function in the board is shown in Figure 4-9:

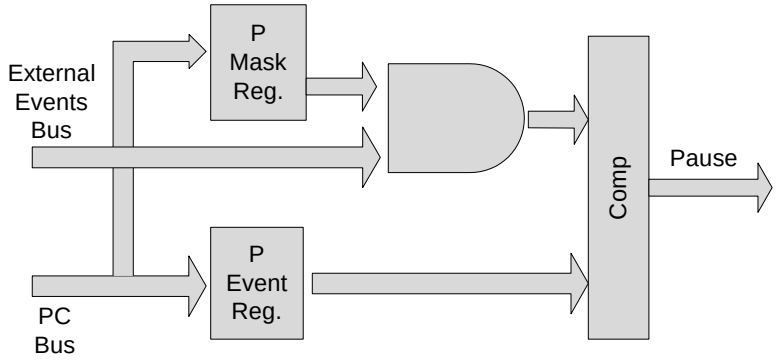


Figure 4-9: External Events Pause Block Diagram

PXI Trigger Bus Line Pause

Controlled by software the GX5280 can be programmed to Pause on any one of the PXI Trigger Bus Lines. The programmed selected PXI Trigger Bus Line can then be Enabled/Disabled through software control achieving additional control over the PXI Trigger Bus event.

Other Features of the GX5280 Board

X Register

The GX5280 board has a 16-bit register that can be set by software to simulate the external event lines.

B Clock Source

The GX5280 Board has another programmable clock that may be used externally. This clock can be programmed from 1MHz to 200MHz.

This clock CLKB is independent. It is not defined at power up and once programmed, it will not change (even by reset) until programmed to another value.

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Appendix A - Connectors and Cables

Overview

This section describes the DIO I/O and the Timing connectors and cables (see Figure A-1).

When a GX5280 is configured as Master all connectors can be used. When it configured as Slave J3 Timing and J4 Control connectors should not be used.

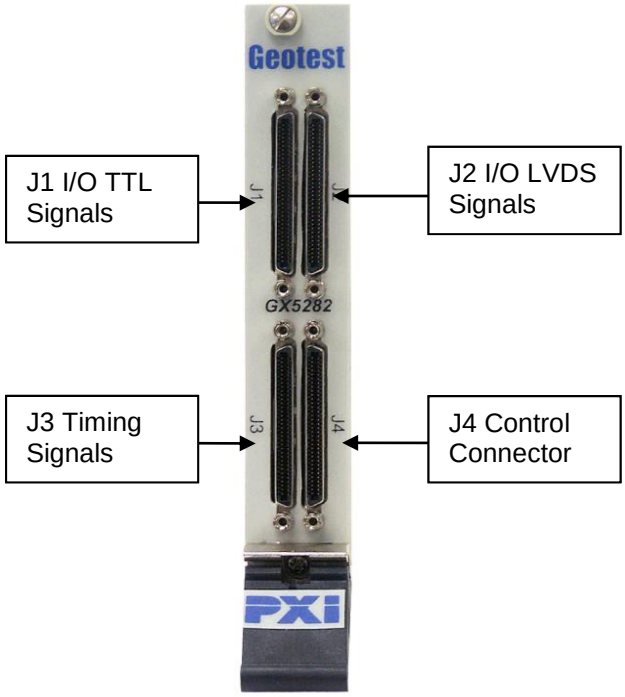


Figure A 1: GX5280 Panel Connectors for UUT Cables

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DIO Connectors

The GX5280 has 4 connectors. All the connectors are available on the instrument's front panel.

The GX5280 has the following connectors:

J1 I/O TTL Signals	Programmable TTL Level I/O Data Connector Signals.
J2 I/O LVDS Signals	LVDS I/O Data Signals.
J3 Timing	Timing Signals (do not use on Slave).
J4 Control	User Control Connector Signals (do not use on Slave).

Note: All connectors J1-J4 are 68-pin VHD connectors.

Figure A-2 shows the layout of 68-Pin VHD connectors. The 68-pin male end plate connector has a shielded, double pin row receptacle. The connector mates with a UUT cable.

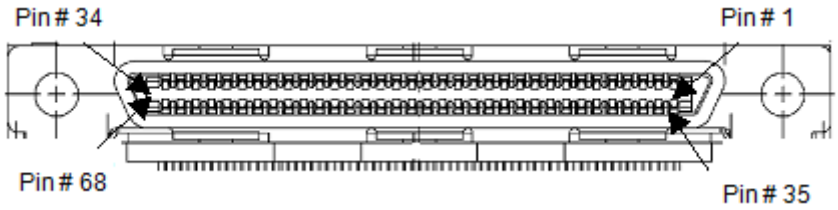


Figure A - 2: GX5280 68-Pin (VHD) Connector

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J1 I/O TTL Signals (68-Pin to UUT)

The following table defines the GX5280 DIO to I/O signals. This interface uses a 68-pin VHD connector.

Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type
1	IO0	I/O	18	IO17	I/O	35	GND	P	52	GND	P
2	IO1	I/O	19	IO18	I/O	36	GND	P	53	GND	P
3	IO2	I/O	20	IO19	I/O	37	GND	P	54	GND	P
4	IO3	I/O	21	IO20	I/O	38	GND	P	55	GND	P
5	IO4	I/O	22	IO21	I/O	39	GND	P	56	GND	P
6	IO5	I/O	23	IO22	I/O	40	GND	P	57	GND	P
7	IO6	I/O	24	IO23	I/O	41	GND	P	58	GND	P
8	IO7	I/O	25	IO24	I/O	42	GND	P	59	GND	P
9	IO8	I/O	26	IO25	I/O	43	GND	P	60	GND	P
10	IO9	I/O	27	IO26	I/O	44	GND	P	61	GND	P
11	IO10	I/O	28	IO27	I/O	45	GND	P	62	GND	P
12	IO11	I/O	29	IO28	I/O	46	GND	P	63	GND	P
13	IO12	I/O	30	IO29	I/O	47	GND	P	64	GND	P
14	IO13	I/O	31	IO30	I/O	48	GND	P	65	GND	P
15	IO14	I/O	32	IO31	I/O	49	GND	P	66	GND	P
16	IO15	I/O	33	VTH	P	50	GND	P	67	VTH	P
17	IO16	I/O	34	GND	P	51	GND	P	68	GND	P

Table A-1: 68-Pin I/O TTL Signals, J1.

Notes for Table A-1:

- Pin: Pin number
- I/O: Input or Output
- P: Power/GND
- IO0 – IO31: Single Ended Data Lines.
- VTH – Termination voltage for data and control signals.

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J2 I/O LVDS Signals (68-Pin to UUT)

The following table defines the GX5280 DIO to I/O signals. This interface uses a 68-pin VHD connector.

Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type
1	IO0+	I/O	18	IO17+	I/O	35	IO0-	I/O	52	IO17-	I/O
2	IO1+	I/O	19	IO18+	I/O	36	IO1-	I/O	53	IO18-	I/O
3	IO2+	I/O	20	IO19+	I/O	37	IO2-	I/O	54	IO19-	I/O
4	IO3+	I/O	21	IO20+	I/O	38	IO3-	I/O	55	IO20-	I/O
5	IO4+	I/O	22	IO21+	I/O	39	IO4-	I/O	56	IO21-	I/O
6	IO5+	I/O	23	IO22+	I/O	40	IO5-	I/O	57	IO22-	I/O
7	IO6+	I/O	24	IO23+	I/O	41	IO6-	I/O	58	IO23-	I/O
8	IO7+	I/O	25	IO24+	I/O	42	IO7-	I/O	59	IO24-	I/O
9	IO8+	I/O	26	IO25+	I/O	43	IO8-	I/O	60	IO25-	I/O
10	IO9+	I/O	27	IO26+	I/O	44	IO9-	I/O	61	IO26-	I/O
11	IO10+	I/O	28	IO27+	I/O	45	IO10-	I/O	62	IO27-	I/O
12	IO11+	I/O	29	IO28+	I/O	46	IO11-	I/O	63	IO28-	I/O
13	IO12+	I/O	30	IO29+	I/O	47	IO12-	I/O	64	IO29-	I/O
14	IO13+	I/O	31	IO30+	I/O	48	IO13-	I/O	65	IO30-	I/O
15	IO14+	I/O	32	IO31+	I/O	49	IO14-	I/O	66	IO31-	I/O
16	IO15+	I/O	33	VTH	P	50	IO15-	I/O	67	VTH	P
17	IO16+	I/O	34	GND	P	51	IO16-	I/O	68	GND	P

Table A-2: 68-Pin I/O LVDS Signals, J2.

Notes for Table A-2:

- Pin: Pin number
- I/O: Input or Output
- P: Power/GND
- IO0 – IO31: Differentially Coupled Data Lines.
- VTH – Termination voltage for data and control signals.

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J3 Timing Signals Connector

This topic describes the GX5280 Timing connector J3 timing and external event signals (used only on a Master). This interface uses a 68-pin VHD connector. The following table lists the Timing signals:

Pin	Name	Function	Pin	Name	Function
1	EXT0	Input External event 0	18	ORun	Output Run Indication
2	EXT1	Input External event 1	19	GND	
3	EXT2	Input External event 2	20	BClk	Independent output programmable clock output
4	EXT3	Input External event 3	21	GND	
5	EXT4	Input External event 4	22	OClk	User Output Clock
6	EXT5	Input External event 5	23	GND	
7	EXT6	Input External event 6	24	OStb	Strobe Output
8	EXT7	Input External event 7	25	GND	
9	EXT8	Input External event 8	26	XTrig	External Trigger Input (Overrides Run Command)
10	EXT9	Input External event 9	27	XPause	External Pause Input (Overrides Pause Command)
11	EXT10	Input External event 10	28	XClkEn	External Clock Enable Input
12	EXT11	Input External event 11	29	XStbEn	External Strobe Enable Input
13	EXT12	Input External event 12	30	EXCLKO	Output clock, distributes EXCLK to slaves (PCB revision D or later, otherwise GND).
14	EXT13	Input External event 13	31	XClk	External Clock Input
15	EXT14	Input External event 14	32	XStb	External Strobe Input
16	EXT15	Input External event 15	33	VTH	Termination voltage output for data and control signals
17	OArm	Output Arm Indication	34	GND	
35	GND		67	VTH	Termination voltage output for data and control signals
66	GND		68	GND	

Table A-3: 68-pin Connector J3 Timing UUT.
Unspecified pins are GND.

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J4 Control Connector

This topic describes the GX5280's Control connector J4 handles UUT control signals. This interface uses a 68-pin VHD connector.

The following table defines the DIO to UUT control interface.

Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type	Pin	Signal	Type
1	GND	P	18	GND	P	35	GND	P	52	GND	P
2	N/C	X	19	OEN0n	O	36	N/C	X	53	GND	P
3	GND	X	20	OEN1n	O	37	GND	X	54	GND	P
4	CLK_LVDS+	X	21	OEN2n	O	38	CLK_LVDS-	X	55	GND	P
5	GND	X	22	OEN3n	O	39	GND	X	56	GND	P
6	GND	P	23	CLK2O	P	40	GND	P	57	GND	P
7	N/C	X	24	XEN0n	I	41	N/C	X	58	GND	P
8	N/C	X	25	XEN1n	I	42	N/C	X	59	GND	P
9	N/C	X	26	XEN2n	I	43	N/C	X	60	GND	P
10	N/C	X	27	XEN3n	I	44	N/C	X	61	GND	P
11	GND	P	28	GND	P	45	GND	P	62	GND	P
12	N/C	X	29	N/C	I	46	N/C	X	63	GND	P
13	N/C	X	30	N/C	X	47	N/C	X	64	GND	P
14	N/C	X	31	5V	P	48	GND	P	65	GND	P
15	N/C	X	32	5V	P	49	GND	P	66	GND	P
16	EXCLK2	X	33	VTH	P	50	GND	P	67	VTH	P
17	EXCLK2O	X	34	GND	P	51	GND	P	68	GND	P

Table A-4: 68-Pin Control Connector Signals, J4.

Notes for Table A-4:

- I: Input
- O: Output
- P: Power/GND
- N/C: Reserved, do not use.
- OEN0-3n– Output Enable outputs. A low signal indicates output signal/signals in the indicated byte group is currently enabled (active low).
- XOE0-3n– External Output Enable inputs. A low signal disables the output drivers of the selected I/O group (active low).
- VTH – Termination voltage for data and control signals.
- CLK_LVDS+, CLK_LVDS-: LVDS clock positive and negative signals (PCB revision D or later, otherwise N/C).
- CLK2O – Output clock distributing external clocks or strobes to slaves (PCB revision D or later, otherwise N/C).
- EXCLK2 – External Clock input #2 (PCB revision D or later, otherwise N/C).
- EXCLK2O – Output clock, distributes EXCLK2 to slaves (PCB revision D or later, otherwise N/C).

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Caution - DO NOT CONNECT the GT95014 DIO Single Ended Interface Board to User connector J4 if the LVDS clock is enabled. The LVDS_N signal will get shorted to ground and device damage may result. Use the GT95015 DIO Differential Interface Board for all J4 functions if the LVDS clock is required.

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Appendix B - Specifications

This section provides GX5280 DIO and Timing connector specifications.

GX5280 DIO Specifications

The following are specifications for GX5280 board:

Feature	Value
Timing	
Internal Clock (PLL):	
Range	GX5281: 5 Hz (Min), 50 MHz (Max) GX5282: 5 Hz (Min), 100 MHz (Max) GX5283: 5 Hz (Min), 200 MHz (Max)
Resolution, max	Greater of 1Hz or 0.2%
Internal B Clock:	
Range	1 to 200MHz
Resolution	0.2%
Internal Strobe Phase – Clock delay	0 – 24nS in 4nS steps
Ext.Test Clock	0 to 50MHz
Ext. Strobe	0 to 50MHz
Timing skew	1nS same card, 1nS between cards
Clock In	
Direction	Input into Master board
Destinations	Reference clock (for the phase lock loop (PLL)) Sample clock
As Sample clock	
Frequency range	3.5 MHz to 50 MHz
As Reference Clock	
Reference clock frequency range	10 MHz ± 50 ppm
Input/Output	
Data Direction control	Input or Output, fixed during execution
I/O channel width	32
Channels per board	32
Memory depth, steps	GX5281: 32M GX5282: 64M GX5283: 128M

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Feature	Value
Trigger	Software, external override, or conditional
Pause	Software, external override, or conditional
External Status & Control	
Output Enable	Tri-state in 8-pin groups
External Clock Enable	Internal, External and Select
Clock Output	As selected clock
External Strobe	As selected Input
External Event Bus	As selected 16 lines
Pause	As selected Override Input
Trigger	As selected Override Input
Run	As selected Indicator
B Clock	As selected Output
Environmental	
Operating Temp.	0 to 50°C
Storage Temperature	-20 to 70°C
Physical Properties	
Bus Interface	Compact PCI/PXI
Dimensions	Single 3U Compact PCI slot; PXI compatible
Weight	200 gr.
Front Panel Connectors	
Label:	
J1	I/O TTL Signals, type 68-pin VHD connector
J2	I/O LVDS Signals, type 68-pin VHD connector
J3	Timing Signals, type 68-pin VHD connector
J4	Control Connector, type 68-pin VHD connector

Table C-1: GX5280 DIO Specifications

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