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GTDIO

GT-DIO Product Family

GT25/GT50

Dynamic Digital I/O ISA Cards

User's Guide

Last Updated August 14, 2013

MARVIN TEST SOLUTIONS

Safety and Handling

Each product shipped by Marvin Test Solutions is carefully inspected and tested prior to shipping. The shipping box provides protection during shipment, and can be used for storage of both the hardware and the software when they are not in use.

The circuit boards are extremely delicate and require care in handling and installation. Do not remove the boards from their protective plastic coverings or from the shipping box until you are ready to install the boards into your computer.

If a board is removed from the computer for any reason, be sure to store it in its original shipping box. Do not store boards on top of workbenches or other areas where they might be susceptible to damage or exposure to strong electromagnetic or electrostatic fields. Store circuit boards in protective anti-electrostatic wrapping and away from electromagnetic fields.

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Table of Contents

Safety and Handling ... iii
Warranty ... iii
If You Need Help ... iii
Disclaimer ... iii
Copyright ... iii
Trademarks ... iv
Chapter 1 - Introduction ... 1
About This User Guide ... 1
Required User Knowledge and Skills ... 1
Scope and Organization ... 1
Related Documents ... 1
Style Conventions ... 2
Definitions ... 2
Chapter 2 - Overview ... 3
What is DIO? ... 3
PC Bus Interface ... 4
DIO Domains ... 4
GT25/50-DIO Architecture and Capabilities ... 5
DIO Software Components ... 5
Supported Development Environments ... 6
Chapter 3 - Setup and Installation ... 7
Introduction ... 7
Caution ... 7
Discharge Static Electricity Precautions ... 7
Packing List ... 7
GTxx-DIO Master Board ... 7
GTxx-DIO Slave Board ... 8
Memory Options ... 8
System Requirements ... 9
Hardware ... 9
Installation Procedures ... 9
Introduction ... 9
Verify Terminator Jumpers ... 10
Setting the Base Address ... 10
Memory Installation or Upgrades ... 11

Installing the Timing Control Module 13
Board Installation Inside the PC 14
GTXI Installation 14
Getting Started with the GT-DIO Board 15
Chapter 4 - Theory of Operation 17
Architecture 17
Masters and Slaves 18
I/O Pin 18
Clock and Strobe Signals 19
GT-DIO Memory Management 20
Program Sequencer 20
Commands 21
Sequencer Command Table 22
Conditions 22
GT-DIO States 23
Halt State 23
Pause State 23
Run State 23
Trigger Command 24
PC (Software) Trigger 24
External Trigger 24
External Trigger Control Line 24
External Event Lines 24
Pause Command 25
External Pause 25
External Pause Control Line 25
External Pause Event Lines 25
Other Features of the GT-DIO Board 25
X Register 25
B Clock Source 26
Appendix A – Connectors & Cables 27
Overview 27
Input-Output Module Connector and Pin Assignments 28
Timing Module Connector and Pin Assignments 29
Appendix B – Control Memory Command 31
Overview 31
Command Micro Code 31

Command Layout....31
I/O Groups Control Field....32
Operation Code Field....32
Register Field....32
Command Field....33
Guidelines on How to Write Control Commands....33
Appendix C – Specifications....35
Overview....35
Timing Module Specifications....35
I/O Module Specifications....37
Index....39

Chapter 1 - Introduction

About This User Guide

This User Guide provides information needed to install, configure, program and use Marvin Test Solutions' GT25-DIO and GT50-DIO digital input/output (DIO) boards. Supporting boards, accessories and software are discussed in related User Guides.

Required User Knowledge and Skills

This User Guide assumes a general knowledge of PC-based computers, proficiency with a 32-bit Microsoft Windows operating system and some knowledge of electronics.

Scope and Organization

The User Guide is organized as follows:

Chapter	Content
Chapter 1	***Introduction.*** Introduces this DIO User Guide.
Chapter 2	***Overview***. Summarizes GT25/50-DIO family, board features, architecture, hardware and driver.
Chapter 3	***Installation and Setup.*** Furnishes step-by-step directions for installing and setting up hardware and installing the driver.
Chapter 4	***Theory of Operation.*** Furnishes a description of the functional hardware.
Appendix A	***Connectors and Cables.*** Defines connector and pin assignments.
Appendix B	***Control Memory Command.*** Describes the control memory command micro code.
Appendix C	***Specifications***. Summarizes GT25/50-DIO design requirements.
Index	Provides a roadmap to important topics and concepts in this manual.

Related Documents

The following documents contain related information and are considered an integral part of this User Guide:

DIO I/O Modules and Interfaces User Guide – Information about I/O Modules and supporting hardware.

DIO Software User Guide – Information about the DIO Driver, Panel and ***DIOEasy*** Windows application.

Style Conventions

Example	Description
Copy or **Paste**	Commands are indicated in bold type.
Shift+F1	Keys are often used in combination. The example to the left instructs the user to hold down the shift key while pressing the FI key at the same time. When key combination instructions are separated by commas (such as ALT+D, A), hold the ALT key while pressing D, then press A.
Direction Keys	Refer to the up arrow (↑), down arrow (↓), right arrow (→), and left arrow (←) keys.
cd bold	Bolded text must be entered from the keyboard exactly as shown.
cd *directory name*	Italicized text is a placeholder for variables or other items the user must define and enter from the keyboard.
`examples`	Examples and source code are indicated in Courier, a fixed pitch font.
0x*hexnumber*	An integer in hexadecimal notation, for example, 0x10A equals 266 in decimal.

Definitions

The following table defines terms commonly used in this document:

Term	Definition
DIO	Digital Input/Output (I/O).
DIO board	Generically, any of Marvin Test Solutions' digital Input/Output circuit boards in any board family. The context could restrict it to the GT25/50 family.
GT25/50-DIO domain	A system based on GT25-DIO and GT50-DIO DIO boards. These include I/O Module daughter boards as well as associated cables and software.
GT25/50	Refers to both the GT25-DIO and GT50-DIO circuit boards.
HD	High Density. Used to describe a small 50-pin connector used for GT25/50-DIO data.
Master or GT25/50-DIO board	Refers specifically to the GT25-50-DIO circuit board with timing board, unless otherwise specified.
I/O User Guide	The ***DIO I/O Modules and Interfaces User Guide***
Slave or GT25/50-DIO Slave board	Refers specifically to the GT25/50-DIO circuit board without timing board, unless otherwise specified.
Step	One in a sequence of test intervals. DIO boards run through a programmed sequence of steps.
Software User Guide (or variants)	The DIO *Software User Guide* provided with GT25/50-DIO boards.
Testware	Test software. It includes test vectors loaded and run on the DIO system, as well as driver commands used to load the boards and read results.
Vector or Test vector	A sequence of stimuli applied to the pins of a Unit Under Test (UUT).

Chapter 2 - Overview

What is DIO?

Marvin Test Solutions' DIO is a family of high-speed, programmable, dynamic Digital Input and Output (I/O) boards. These boards perform high-speed automated functional testing, device testing, simulation and data acquisition. The DIO family provides real-time digital pattern capture and generation, with 32 channels per card and up to 8 cards or 256 channels per system.

The DIO family uses common software development tools to develop test vector files. The test vector files contain digital patterns sent to or received from the Unit Under Test (UUT).

Development of the vector file may be independent of the hardware with ***DIOEasy***. Vector file verification requires the DIO be installed and properly configured.

Marvin Test Solutions bundles ***DIOEasy*** with all DIO products. ***DIOEasy***, Marvin Test Solutions' vector development and analysis software, allows manual control of the DIO hardware using the built-in DIO Virtual Instrument Panel. The DIO driver permits control of the DIO family from common software development tools such as ***ATEasy***, Visual Basic, C, C++, Pascal and more.

DIOEasy is a 32-bit Windows application not requiring any programming experience or knowledge.DIO Product Families

The DIO Driver and ***DIOEasy*** software control the DIO boards. Effective use of the driver requires an understanding of how DIO boards are used in a system and board capability.

Marvin Test Solutions offers two families of DIO boards:

- GT25/50-DIO series.
- GT515x (see the *DIO GT5150/5151 Dynamic Digital I/O User Guide*).

Common Elements

Both families use a *Master* DIO board to establish synchronization with the UUT and provide timing signals to the Master and other (Slave) boards. The DIO Master also has a Timing and Control Module. This module mounts on the Master. Signals from the timing module provide control and synchronization to the Master's I/O Module and up to seven Slave I/O Modules. Every DIO configuration needs at least one Master board and can control up to 256 digital input or output channels.

Both families support Slave boards, extending the number of UUT I/O channels while maintaining the same timing and pattern sequencing. However, the Slave boards must be of the same family as the Master board.

The Driver and ***DIOEasy*** application are common to both families.

GT25/50-DIO Series

The GT25/50-DIO has 32 channels of I/O. The direction of GT25/50 channels can be switched dynamically from Input to Output at each vector step (in groups of eight channels). The GT25/50 has only TTL levels but can support other levels using GT515x I/O modules mounted on a GT5900.

GT515x Series

The GT515x has 8, 16 or 32 channels (programmable width). Each channel can be preprogrammed as Input or as Output, although the direction applies to the entire board and cannot be changed dynamically (while the test vector is running). Memory depth of the GT515x increases proportionately as width is reduced (that is, 32Mbit per channel with a width of 32 channels, 64Mbit per channel with a width of 16 channels or 128Mbit per channel with a width of 8 channels). The GT515x can use a variety of I/O modules to interface with different UUTs. Those I/O modules expand the DIO abilities, including interfacing with different voltage levels, providing higher speed and comparing data on the fly.

The GT5900 is a carrier board for GT515x I/O modules. This board is used typically with the GT25/50 when special I/O modules are required. The GT5900 can carry two I/O modules or one I/O module and a Timing Control module.

The family architectures are different and so are their capabilities. Some driver functions are available only to a specific family while others will work with both families.

PC Bus Interface

The DIO Driver accesses Master, Slave and carrier boards through the computer's bus (Figure 2-1). The driver can accommodate up to 16 Masters (from either family). All DIO and carrier boards have switches used to assign I/O addresses. Each board must have a unique I/O address. Board addresses then are saved in a database through a driver library function call or the Panel's "**Configure!**" button.

DIO Domains

A DIO domain has one Master DIO board and up to seven Slave DIO boards. The Master, its Slaves, carriers and related modules comprise a DIO *domain*. Figure 2-1shows a domain from two different families on a PC bus.

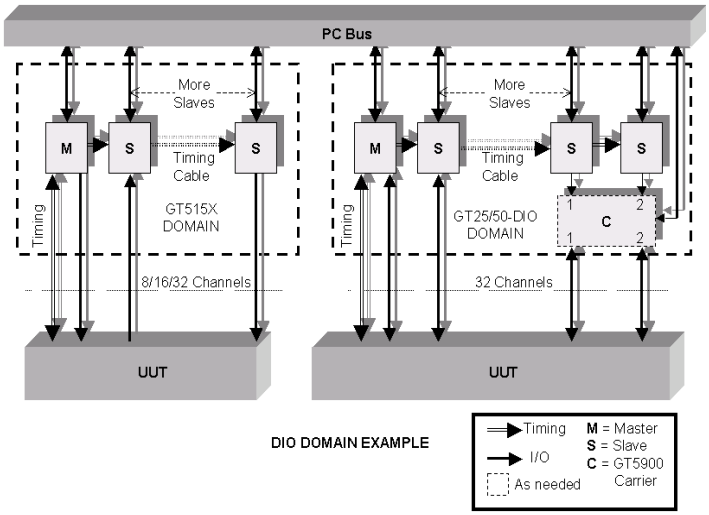


Figure 2-1: Two Different DIO Domains on One PC Bus

Domains are internally synchronized and controlled through a Timing cable binding the Master's Timing module to all domain Slave boards. To synchronize a domain with a UUT, you need to synchronize the Master board's Timing module.

Masters and Slaves within a domain must be members of the same product family. Each Slave adds 32 additional UUT I/O channels. Up to seven Slaves can be added to a domain.

A full domain, containing eight DIO boards, provides up to 256 UUT I/O channels (256 channels wide). Because the driver supports 16 Masters, up to 16 domains of mixed types can, in principle, share a PC bus. Realistically, only two DIO domains (16 cards, 512 channels) can exist in an industrial PC due to slot and I/O address limitations. Using Marvin Test Solutions' GTXI instrument control chassis (which can accommodate up to 52 instruments and has expanded I/O addressing), up to six DIO domains (48 boards, 1536 channels) can be used in a single system. The actual limit is subject to slot and possible I/O address availability. Each DIO Master board can serve an independent UUT time source.

A minimum DIO domain contains only a Master DIO board (32 digital channels).

GT25/50-DIO Architecture and Capabilities

The following are key GT25/50-DIO characteristics and architecture elements:

A GT25/50-DIO domain can contain one or more GT25/50 DIO boards.

A GT25/50-DIO Master board controls the timing of a DIO domain and can be synchronized to a UUT.

A Master board can be added to synchronize an additional asynchronous UUT element.

A GT25/50-DIO Slave board adds 32 UUT channels. Up to 7 Slave boards can be added for 256 channels.

DIO boards can support non-TTL interfaces by adding a GT5900 Carrier with appropriate I/O Modules mounted on it.

Channel direction is controlled in-groups of eight. Direction can be switched on the fly between input and output via program control.

Memory can differ among domain boards. The board with the lowest capacity memory limits available program steps (depth). The user must assure enough memory exists to run the vector file and acquire results.

Registers A, B, C, D, P and T can be loaded and compared against external events on the External Event line.

UUTs can generate triggers on External Event lines. D and T Event Registers can be compared after masking events with loadable D and T Mask Registers.

External triggering can be initiated on sequential or concurrent events using both D and T Event Registers to define the events.

The test program can be paused with or without conditions, based on external events. The P Event and P Mask Registers hold the condition and bits generating a conditional pause.

A more thorough discussion of board architecture, including a block diagram, is found in the *GT25/50-DIO and Digital Input/Output Board User Guide*.

DIO Software Components

DIO software is used by all DIO family boards and includes the modules described below.

Product	Description
Driver	A dynamic link library (DLL) providing Application Programming Interface (API) functions for configuring and controlling DIO boards. Some functions are product specific while others apply to the entire DIO family. Two versions are available: 16 bit and 32 bit.
Panel	A Windows application allowing you interactive control over DIO and carrier board setup and configuration. Can also be accessed from ***DIOEasy*** or a driver call.
DIOEasy	A 32-bit Windows application for generating, viewing and analyzing digital test vectors. Provides *Panel* accesses.
Sample files	Example code demonstrating Driver calls.
Help files	An interactive User Guide.

DIO testware can be developed on a PC using a development environment or ***DIOEasy*** with the DIO Driver. However, testing and testware validation requires DIO hardware.

DIOEasy offers a quick and simple way to generate and preview vectors, and to analyze returned data in a Graphical User Interface (GUI) environment. However, using the full power of DIO requires the driver and writing test programs.

Supported Development Environments

DIO test code can be written in a large number of 16 and 32-bit development environments. These include, but are not limited to, ***ATEasy***, Visual C++, Visual Basic, Borland C++ Builder and Delphi, as well as any programming language capable of loading and using Windows' DLLs.

Chapter 3 - Setup and Installation

Introduction

This chapter provides instructions on how to install the GT-DIO circuit board, the accompanying ***DIOEasy*** software and the GT-DIO driver. This chapter also contains sections explaining memory options, system requirements and how to configure GT-DIO circuit boards.

Caution

Discharge Static Electricity Precautions

To reduce the risk of damaging GTxx-DIO boards, the following precautions should be observed:



Caution - Static-sensitive devices are present. Ground yourself to discharge any static electricity charge.

- Wear a grounding strap.
- Leave the board in the anti-static bag before installation. The anti-static bag protects the board from harmful static electricity.
- Save the anti-static bag to store the board if it is removed from the computer.
- Handle the board only at the edges. Avoid touching components.
- Carefully unpack the board. Do not drop the board or handle it roughly. A hairline fracture can cause unreliable operation.

Packing List

Depending on what you ordered, the shipping kit may contain the following items:

GTxx-DIO Master Board

This includes:

- Input-Output Module GTxx-DIO board, with installed memory in groups of three SIMMs (see memory options listed in the next section), and one 50 pin flat cable with one installed connector and one uninstalled connector.

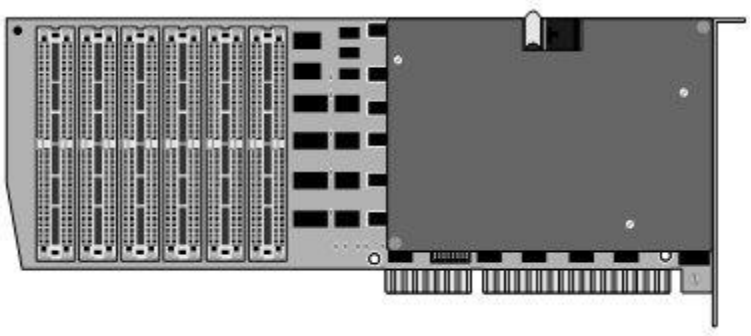


Figure 3-1: Master Circuit Board with Timing Control Module

- GTxx-TIM Timing Control Module (installed on I/O module) including one or two 20-pin flat cables with a number of pre-installed connectors depending upon the number of boards in the system. For example, if you have four boards, order one flat cable with five installed connectors. This flat cable may be used to daisy chain up to four boards. Two cables may be used to connect up to eight boards: one Master and seven Slaves.
- 1.44MB (3.5 inch) floppy disk containing ***DIOEasy*** software and GT-DIO driver.
- *GT-DIO / **DIOEasy** User's Guide*.

GTxx-DIO Slave Board

This includes:

- Input-Output Module GTxx-DIO board with installed memory in groups of three SIMMs (see memory options listed below), and one 50 pin flat cable with one installed connector.

Memory Options

Memory options for the GTxx-DIO circuit boards are as follows:

Board	Memory Option
GT-16K-15	16K Memory for up to 40MHz Applications
GT-16K-12	16K Memory for up to 50MHz Applications
GT-64K-30	64K Memory for up to 25MHz Applications
GT-64K-20	64K Memory for up to 35MHz Applications
GT-256K-25	256K Memory for up to 35MHz Applications
GT-256K-30	256K Memory for up to 25MHz Applications
GT-256K-12	256K Memory for up to 50 MHz Applications
GT-256K-10	256K Memory for up to 65MHz Applications

Table 3-1: Memory Options

Other memory options may be available when ordering. Memory is always supplied in groups of three SIMMs. Up to four groups or banks (12 SIMMs) may be installed on each board to provide up to 1M of steps per pin.

System Requirements

Hardware

The GTxx-DIO boards are installed in the expansion slots located inside the PC. IBM PC/AT compatible computers have two types of expansion slots: 8-bit with one card-edge receptacle and 16-bit with two card-edge receptacles. The GTxx-DIO boards require a 16-bit slot. Do not install the boards in special 32-bit memory expansion slots (such as VESA local bus).

Installation Procedures

Introduction

The GT-DIO System has two types of circuit boards:

- **Master** – The Master board can be connected to a maximum of seven Slave boards. Each Master board contains a Timing Module attached to an Input-Output Module.
- **Slave** – Each Slave board contains only an Input-Output Module.

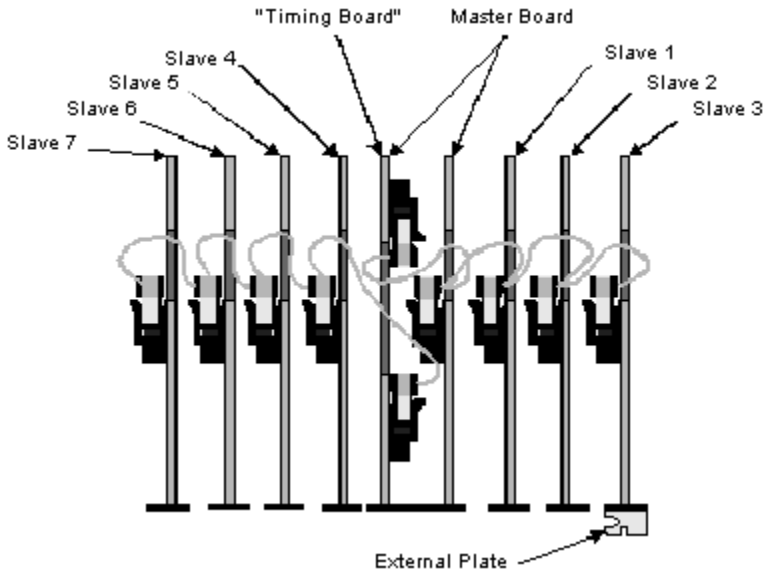


Figure 3-2: Master and Slave Input-Output Circuit Boards with Cable Attached

The following steps are required before the board(s) can be installed in the PC. Each one of these steps is explained in detail in a following section.

Verify the terminator jumpers are in place.

Set the base address.

If required, install or upgrade SIMM memory.

If required, install the Timing Control Module on the Master board.

Install the board inside the PC.

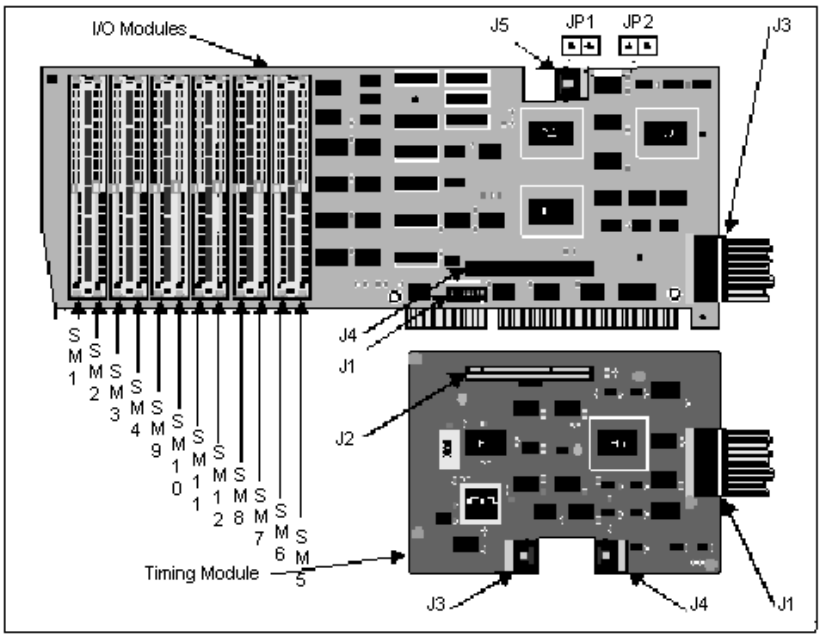


Figure 3-3: GTxx-DIO Boards Layout

Verify Terminator Jumpers

When installing, verify the terminator jumpers are installed, with JP1 and JP2 near J5, (see Figure 3-3). Only the last input-output Slave board in each daisy chain should have terminators installed (see Figure 3-2). If only the Master board is installed, then the jumpers should be installed on this board (see Figure 3-1).

Setting the Base Address

For each Master or Slave board, set the address by setting the Dip switch S1 on the I/O module (see **Error! Not a valid bookmark self-reference.**). Each board occupies four unique addresses in the PC I/O address space. For example, a system with a Master and a Slave board can be installed at 0x310 (hex 310) for the Master and 0x314 for the Slave. You must make sure no other board in the system uses this I/O space before setting the base address.

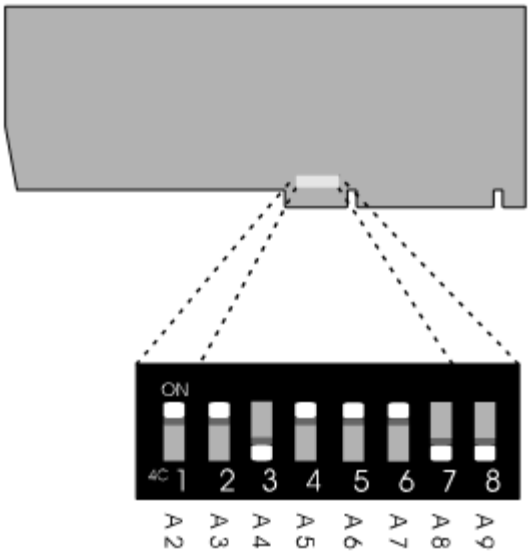


Figure 3-4: Input-Output Circuit Board Showing Switch S1 set to I/O Address 0x310.

The following table shows the value of each switch in S1 when set to the OFF position.

Switch #	Decimal	Hex
Switch 8	512	200
Switch 7	256	100
Switch 6	128	80
Switch 5	64	40
Switch 4	32	20
Switch 3	16	10
Switch 2	8	8
Switch 1	4	4

Table 3-2: Switch Values with Switch S1 in Off Position

For example, for address 0x310 (default) switches 8, 7, and 3 should be in the OFF position (0x200+0x100+0x0010).

Memory Installation or Upgrades

SIMMs (single in-line memory modules) are plug-in memory modules containing the chips required for input, output and control memory in the DIO system. A minimum of three SIMMs (one bank) is shipped pre-installed with each board to accommodate all three types of memory. Each memory type has specific sockets the SIMMs can be installed in, as listed in Table 3-3.

Memory Type	Reference Designators
Output	SM 1 - 4
Input	SM 9 – 12
Control	SM 5 - 8

Table 3-3: Memory Type and Sockets

The following table describes the appropriate SIMM sockets for each number of banks:

# Of Banks	# Of SIMMs	Socket
1	3	SM1, SM5, SM9
2	6	SM1, SM2, SM5,SM6, SM9, SM10
3	9	SM1, SM2, SM3, SM5, SM6, SM7, SM9, SM10, SM11
4	12	SM1, SM2, SM3, SM4, SM5, SM6, SM7, SM8, SM9, SM10, SM11, SM12

Table 3-4: SIMM Sockets

The board contains twelve sockets for SIMM installation and each socket is labeled (see Figure 3-3). Be sure to select the appropriate socket for the SIMM. Additional SIMM banks may be installed to upgrade memory, up to a total of four banks.

The following section explains how to install SIMMs memory on the GT-DIO board.

1. Select the appropriate SIMM socket (see Table 3-4).
2. Carefully set the SIMM (as shown in Figure 3-5) into the appropriate socket at a 45 degree angle using both hands, tilting upwards (refer to Figure 3-6).

   Do not force the SIMM into the socket. The SIMM module has a notch in the lower right corner. This notch prevents incorrect installation. If you are having difficulty installing the SIMM module, make sure you are not installing the module backwards.

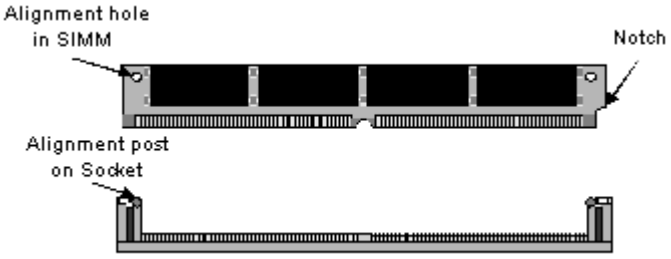


Figure 3-5: SIMM Module Installation

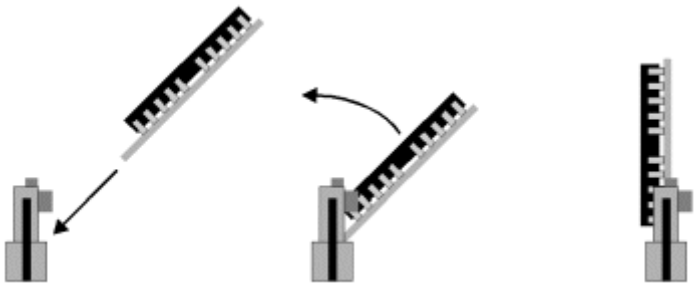


Figure 3-6: SIMM Module Installation – Side View

3. Confirm the module is centered and the module's connector pins are aligned with the socket connector pins.
4. Once the SIMM module is correctly seated, use both hands to push the module to an upright position to lock the module into the socket. Make sure both locking tabs are in place.

Note: Damage to the SIMM module and/or socket may result if proper insertion guidelines are not observed. SIMMs are extremely sensitive to static electricity. When installing SIMMs, follow the instructions at the beginning of this chapter under the *Caution* heading.

Installing the Timing Control Module

The Timing Control Module is usually pre-installed on the I/O module of the Master board (see Figure 3-1). The following installation procedures explain how to install the timing module in case it has not been installed already:

1. Connect the 20 pin flat cable to J3 on the Timing Control Module (see Figure 3-3).
2. Connect the other end of the 20 pin flat cable to J5 on the I/O module (see Figure 3-3).
3. Insert the plastic screws in the Timing Control Module (see Figure 3-7) and install the spacers (see Figure 3-8).
4. Connect J2 on the Timing Control Module to J4 on the I/O module, making sure that the screws are inserted properly in the I/O module (see Figure 3-3).
5. Place the nuts on the screws to connect both modules (see Figure 3-8).

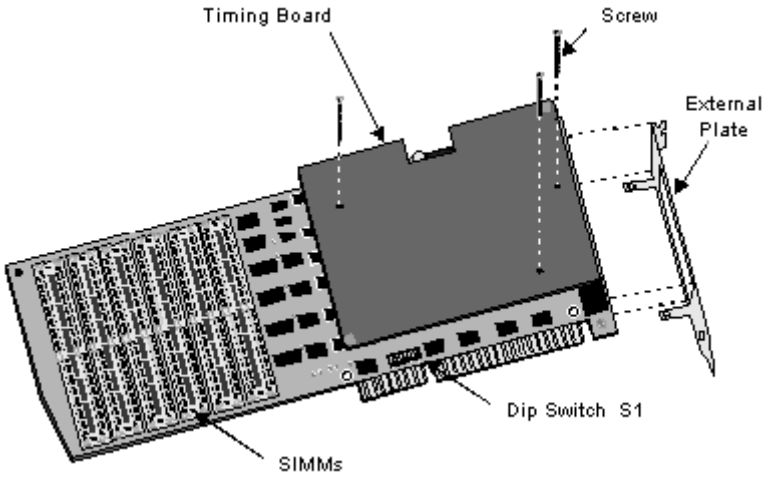


Figure 3-7: Timing Control Module Installation

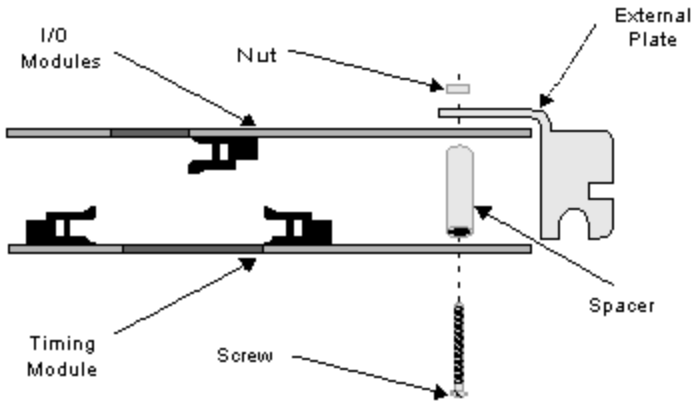


Figure 3-8: Timing Control Module Installation – Side View

Board Installation Inside the PC

Install the GTxx-DIO boards as follows:

1. Turn the PC off and unplug the power cord.
2. Remove the PC cover.
3. Locate a free 16-bit slot on the PC motherboard. Free slots must be available to accommodate the number of boards in the DIO system. If multiple boards are to be installed, the free slots must be continuous (one after the other) since the boards will be daisy-chained.
4. Each expansion slot has a rear panel opening at its end for mounting I/O connectors. Unused slots have a metal plate covering this opening. Remove the screw holding the plate and remove the cover plate. Save the screw.
5. Carefully insert the GTxx-DIO board into the expansion slot and fit the connector through the rear panel opening.
6. Insert the card edge into the motherboard card receptacle.
7. Use the screw from the cover plate to attach the mounting bracket to the rear panel, holding the board firmly in place.
8. Connect the 20-pin daisy chain flat cable to the other Slave board(s). If more than four boards are being installed, use two cables (see Figure 3-2).
9. Slide the PC cover back on and reattach it to the chassis.
10. Plug the power cord in and turn on the PC.

GTXI Installation

DIO broads may also be used in GTXI-700 or GT7700 chassis. However, the GTXI form factors and connectors are different than PC board slots. The DIO board is first configured and then mounted on a GTXI ISA carrier (GT7020) to adapt the DIO board for GTXI-based instrumentation.

DIO boards are configured as above for a PC installation with these exceptions:

After configuration, each DIO board is mounted on a carrier.

Each carrier’s offset address must be set before installing it in a GTXI slot.

The Timing cable is strung through carrier perforations before inserting the carrier into the GTXI chassis. There is no overhead access or clearance for connecting Timing cables into installed carriers.

Carriers are then inserted into GTXI-type chassis using special procedures. Refer to your GTXI documentation for further information on mounting ISA boards on GTXI carriers and configuring carrier board offset addresses.

Note: GTXI carrier boards (GT7020) should not be confused with GT5900 carrier boards used in PCs. These boards are physically and functionally very different.

Getting Started with the GT-DIO Board

When software installation is complete, a Program Manager group called ***DIOEasy*** appears on your screen.

1. Double-click on the **GT-DIO Panel** icon to activate the GT-DIO Virtual Front Panel.

Note: For proper operation of the software, a temporary directory should exist on the hard disk and a "SET TEMP= " command listed in your autoexec.bat file. Before proceeding, check this out and if it is missing, create a temporary directory and write an appropriate line in the autoexec.bat file. The temporary directory is used to store temporary files during ***DIOEasy*** operation. The temp directory and its drive should contain enough disk space for ***DIOEasy*** operation.

The GT-DIO panel window opens (see Figure 3-9).

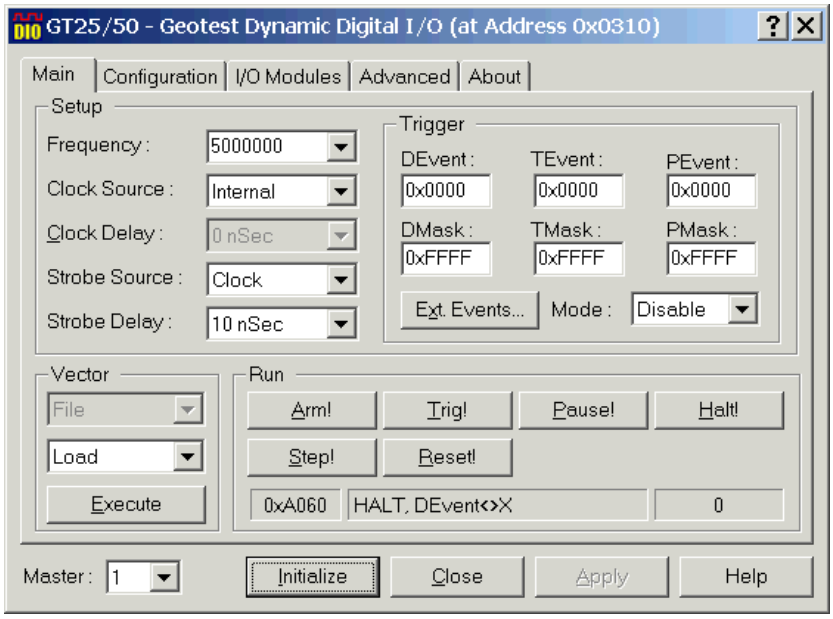


Figure 3-9: GT-DIO Panel Window

2. To configure the installed board(s), click **Configure ….** The DIO Configuration window opens, as shown in Figure 3-10.

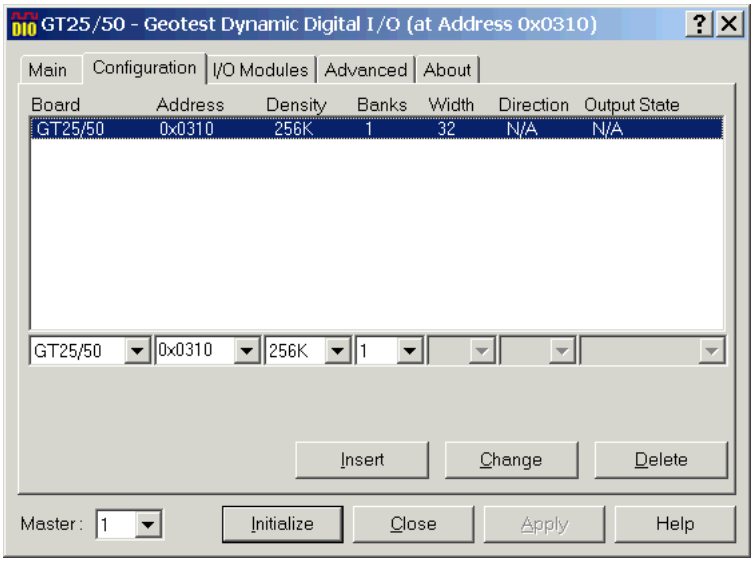


Figure 3-10: GT-DIO Panel Configuration Window

3. Insert the board(s) parameters in the configuration table (see Figure 3-10.) Beginning with the Master board, configure each installed board with the following steps:

   a. Type the base address.

   b. Select the density from the drop down combo box and type the number of banks installed (from 1 – 4). Click the mouse or use the Tab key to move the cursor from field to field.

   c. Click **Insert** to add the board(s) to the configuration table.

Note: The base address can be typed in two formats, hex and decimal. For example, the hex format would be typed as `0x310`.

---

4. Click the Close button (**X**) to close the DIO Configuration window.

5. Click **Initialize!** to accept the configuration (see Figure 3-9).

Chapter 4 - Theory of Operation

This chapter presents the theory of operation for the GT25/50-DIO circuit boards, with an overview of operation and a simple description of operation for one channel (I/O pin). Other topics covered in this chapter are:

- Operation of clock (CLK) and strobe signals.
- Memory management.
- Program sequencer and command conditions.
- Basic states of operation internal and external trigger operation.
- Internal and external pause operation.

Architecture

The GT-DIO supports up to 25MHz (GT25) or up to 50MHz (GT50) operation. Each board contains 32 I/O pins arranged in 4 groups of 8, each group having its own direction: input or output. The direction of each group can be changed for each and every step, either internally by command words or externally in an unsynchronized mode. Each GT-DIO board can be configured from 16K steps up to 1M behind each I/O pin.

The GT-DIO works as a state machine with three main states: **HALT**, **PAUSE** and **RUN**. One of the modules in the board is the sequencer. The sequencer interprets commands stored in the memory array and controls the states machine. Two other memory arrays hold the output data and the input data. The sequencer controls the address of the memory arrays and thereby controls the flow when the board is in the RUN state.

External control provides CLK, strobe and I/O pin direction from an external source. The combination of the external bi-directional control and external clocking, strobing, and triggering provides the capability to fully synchronize with UUTs and to minimize initialization procedures. The board sequencer permits the creation of conditional and unconditional loops and branches to manipulate the output vectors. This provides the capability to generate indefinite stimulus vectors at the maximum test rate.

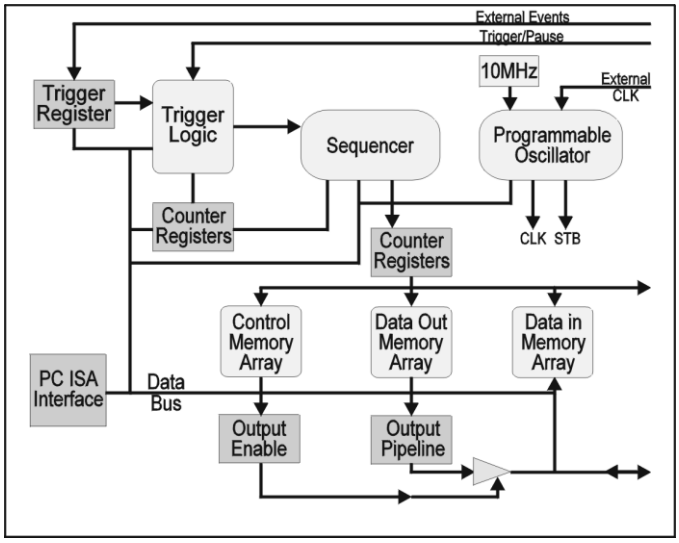


Figure 4-1: Architecture Diagram

Masters and Slaves

The Digital Input-Output System is made up of Master and Slave circuit boards. The Master board can be connected to a maximum of seven Slave boards. Each Master board contains a Timing Module attached to an Input-Output Module, while each Slave board contains only an Input-Output Module.

The Timing Module installed on the standard I/O board makes this board a Master. The other standard boards are Slave boards, which are piggybacked to the Master board with a supplied clock distribution ribbon cable connected from J3 on a Master board to J5 on each of the other Slave boards. See "Chapter 3 -Setup and Installation" for more details about board installation.

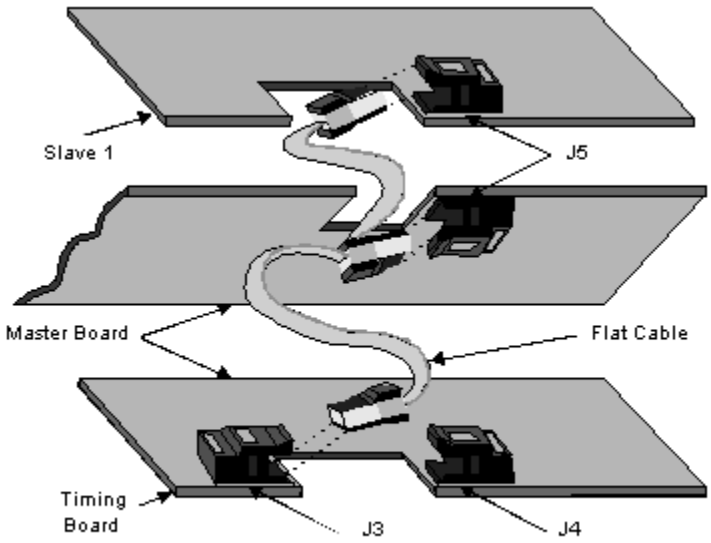


Figure 4-2: Typical DIO System

I/O Pin

An I/O pin uses one channel. Up to eight boards can be used in one system for a maximum of 256 pins (each board containing 32 I/O pins).

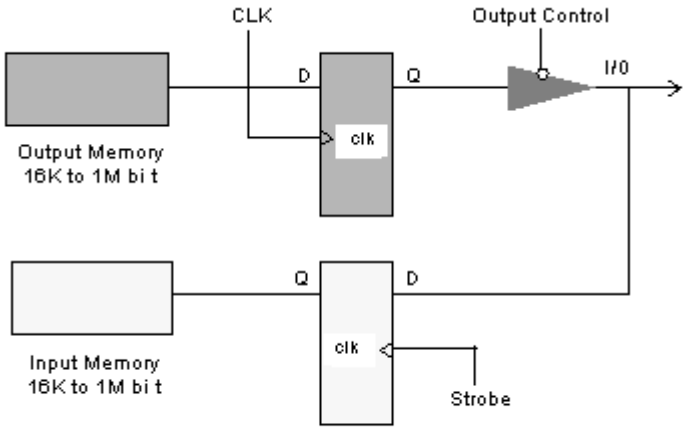


Figure 4-3: I/O Pin Block Diagram

Figure 4-3 is a simplified block diagram of a single I/O pin. This diagram shows how a single channel functions. Output data is stored in the output memory and is outputted from the board as a function of the CLK signal through an output buffer when enabled. In the other direction, the channel value is latched by the Strobe signal into the input buffer and stored in the input memory.

The direction of the I/O pins (input/output) depends on the output Control State. In addition, each output (driver) defined pin is also an input (receiver). The software can ignore the received data; however, its value in the input memory will be the same as the output value.

Clock and Strobe Signals

The clock (CLK) signal initiates each output vector. The rate of this signal can be programmed from 750Hz to either 50MHz or 25MHz, depending on the board configuration. Similarly, the strobe signal latches the input vector. A timing diagram of the CLK and Strobe signals is shown in Figure 4-4.

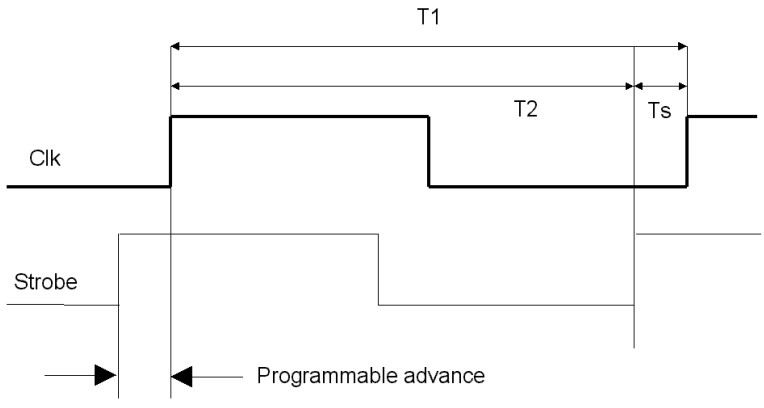


Figure 4-4: Signal Timing Diagram

The GT-DIO board can be driven using either internal or external clock source modes. In the internal mode, the Strobe signal occurs Ts (10nSec default) before the next CLK signal. The Strobe signal can be set to 5, 10, or 20nSec before the CLK signal. In the external mode, the Clock and Strobe signal can be provided externally and the timing is defined externally.

GT-DIO Memory Management

The GT-DIO board has an independent memory for input, output and control that can be configured with 16K to 1M of steps of memory behind each I/O pin. Control and I/O memory are managed as shown in the memory management block diagram (Figure 4-5).

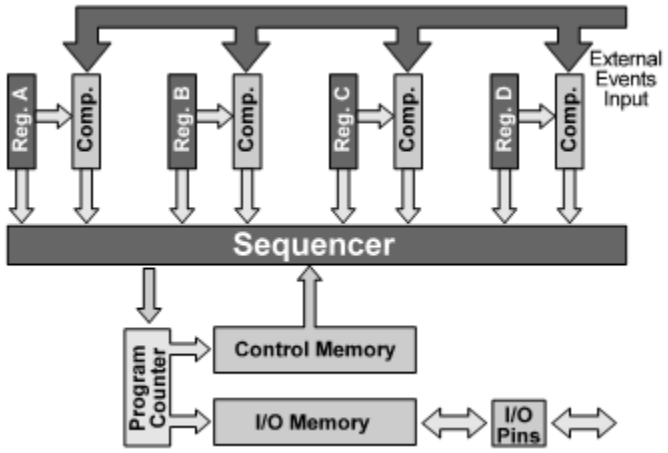


Figure 4-5: Memory Management Block Diagram

The CLK signal and the sequencer control the program counter. The program counter contains the address of the current control and I/O memory. After resetting, the program counter points to address zero and increments with the CLK signal towards address 1M. After reaching 1M, the counter starts again from zero and continues.

Program Sequencer

The sequencer (Figure 4-5) controls the program counter and is one of the most important blocks. The inputs to the sequencer are the control memory, 16 bit registers (A, B, C, D, P and T) and the 16 external events input lines, through the comparators.

Each program step includes one command residing in the control memory. Sequencer commands allow you to control and manipulate the program counter. Each memory step can include only **one** sequencer command. Most of these commands can be conditioned.

Commands

Commands can be used to change the flow control of vectors by changing the value of the program counter while the program is running. Commands can be various types: loads registers or modify the next address provided by the program counter.

The following commands can be executed:

1. **NOP – No operation.** Go to the next step, the sequencer will not affect the program counter.
2. **Set register to X**. The sequencer will set register A, B, C, or D to a value given in the command. The value assigned to the command can be from 0 to 64K. If Register D is used, the 16 external event lines' values are assigned to Register D.
3. **Jump to Step X**. The sequencer enables you to program a jump to any location and it can be conditional or unconditional.
4. The jump command can be near or far. If the far jump command is used, the address can be anywhere in the 1M 20-bit steps; however, the command cannot be conditional. If the jump is near, the address is 17 bits, 0 - 128K, within the current 128K-memory page.
5. **Loop to Step X**. The sequencer enables you to perform a programmed number of jumps (a series of jumps) from the same address. This command can be conditional or unconditional. The jump is always to the near address, between 0 - 128K, in the current 128K-memory page.
6. **Call subroutine at X**. The sequencer saves the address and allows you to perform a jump that remembers the location it jumped from (Y). It returns to Y+1 and can be conditional or unconditional. The address of the subroutine is a far address in eight step boundaries (0, 8, 16, etc.). One level can be used when calling a subroutine.
7. **Return.** The sequencer returns to the address following the last **Call** command. The command can be conditional or unconditional.
8. **Pause.** A pause in the program. The command can be conditional or unconditional.
9. **Halt.** End of the program.

Note: See Appendix B for more information on how to code and decode commands.

Sequencer Command Table

#	COMMAND	PARAMETERS
1	NOP - Continue to next step.	
2	Set Register *R* to *V* Value. If *R* is D, the value is taken from External Event Lines.	*R* = A, B, C or D Registers $0 \le V \le 64K$
3	Jump (FAR) to Step *X*.	$0 \le X \le 1M$
4	Jump (NEAR) to Step *X* on Register *R* Condition (optional) or on External Event Line *B* (high or low) (optional).	*R* = A, B, C or D Registers $0 \le B \le 3$ *X* is the address in the current 128K page
5	Loop *N* Times to Step *X* on Register D Condition (optional).	*N* = A, B or C Registers *X* is the address in the current 128K page
6	Call Subroutine at Step *X* on Register *R* Condition (optional) or on External Event Line *B (*high or low) (optional).	*R* = A, B, C or D Registers $0 \le B \le 3$ $0 \le X \le 1M$ Step *X* must be divided by 8 (0, 8, 16, 24, etc.)
7	Return from Subroutine on Register *R* Condition (optional) or on External Event Line # *B* (optional).	*R* = A, B, C or D Registers $0 \le B \le 3$
8	Pause on Register *R* Condition (optional) or on External Event Line *B* (optional).	*R* = A, B, C or D Registers $0 \le B \le 3$
9	Halt	

Table 4-1: Sequencer Commands

Conditions

Conditions are a combination of comparisons of the external event input lines to a register. The external event input lines are compared with a 16-bit A, B, C or D register.

Conditions can be based on:

- The register equals the external event input lines.
- The register does not equal the external event input lines.
- The register is greater than the external event input lines.
- The register is less than the external event input lines.

Other available conditions are as follows (these conditions cannot be used with the loop command):

- Bit number 0, 1, 2, 3 in the external event line is high.
- Bit number 0, 1, 2, 3 in the external event line is low.

GT-DIO States

The GT-DIO board functions in three basic operational states; **Halt**, **Pause** and **Run**.

Figure 4-6 is a block diagram showing the relationship of these operational states.

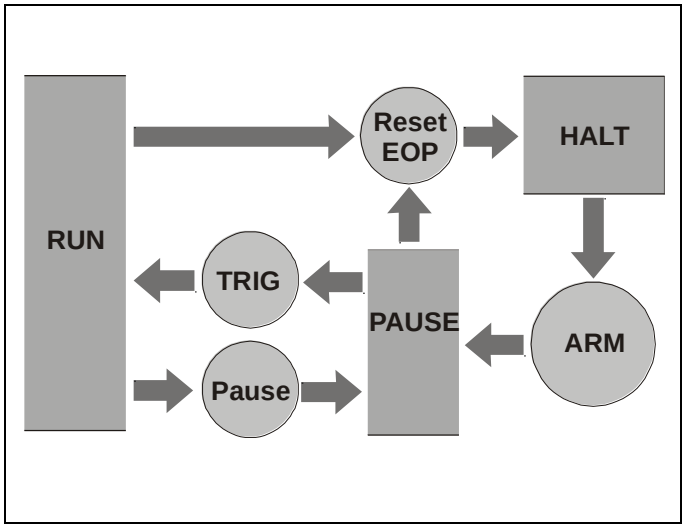


Figure 4-6: GT-DIO Operational States

Halt State

The GT-DIO board goes into a Halt state after a Reset signal and following the Halt command. All external event inputs as well as external control inputs are ignored following a Halt command. Following Reset, all I/O pin (channels) are in the receiving mode of operation. The program counter is zero, the frequency is set to an internal 5MHz, and the strobe timing is set to 5nSec.

Pause State

The board enters a Pause state from a Halt state with an ARM command sent by the PC bus, or from the Run state following the Pause command.

Run State

In the Run state, data is being output and input is being latched. The program counter holds the address of the current output and the address of the command to be decoded and executed by the sequencer. While executing the command, output pins send the data from the output memory located at the program counter address in the control memory and the input pins receive the data. The sequencer executing the command usually increments the programs counter by one unless the command changed the value of the program counter (for example, the Jump command) or the state of the machine was changed (for example, the Pause command). After changing the program counter value, the input data is stored in the input memory at the new program counter address.

Trigger Command

The trigger command causes the board to change its state to the Run state and originates from the following sources:

PC (software)

External trigger control line

External event lines (16 lines)

PC (Software) Trigger

The software trigger originates within the PC. The PC bus trigger command takes effect immediately and overrides other established trigger conditions.

External Trigger

External Trigger Control Line

External triggers originate from the external trigger line. Pulling this line to zero causes the board to change its state to Run. The external trigger line overrides other trigger conditions set for the GT-DIO board.

External Event Lines

It is also possible to set a conditional trigger command, which is activated upon receiving external event input lines. This external event may be any expected value on all or part of the external event input lines. The 16 external event lines are ANDed with pre-defined masks and compared with pre-defined events in registers D and T. The external events trigger function is shown in Figure 4-7.

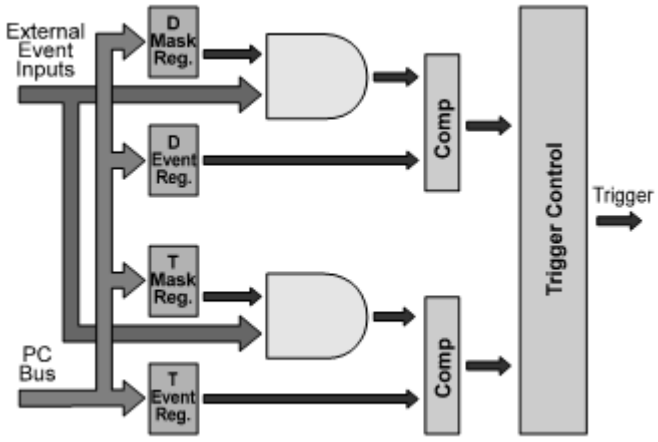


Figure 4-7: External Events Trigger Block Diagram

The external events trigger can be set to one or two levels. In the one level mode, the trigger will be generated after the external condition has been met with the D or T event mask registers. In the two level mode, the board will wait for two sequential events to be met before issuing the trigger signal (D first, T second or opposite).

Pause Command

The pause command causes the board to change its state to the Pause state and originates from the following sources:

- External control line
- External events line
- Sequencer command

External Pause

External Pause Control Line

External pause originates from the external pause line. Pulling this line to zero will cause an immediate pause. The external pause overrides other pause conditions set to the GT-DIO board.

External Pause Event Lines

The P mask and event registers can be used to create conditional pauses that depend on external event lines. The 16 external event lines are ANDed with pre-defined masks and compared with pre-defined events in register P.

The external/internal events pause function in the board is shown in Figure 4-8:

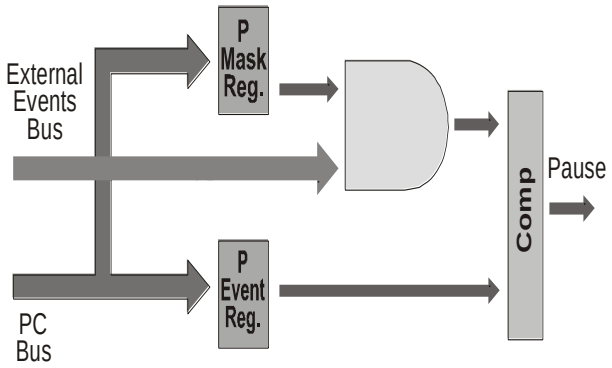


Figure 4-8: External Events Pause Block Diagram

Other Features of the GT-DIO Board

X Register

The GT-DIO board has a 16-bit register that can be set by software to simulate the external event lines.

B Clock Source

The GT-DIO Board has another programmable clock that may be used externally. This clock can be programmed from 350KHz to 110MHz.

This clock CLKB is independent. It is not defined at power up and once programmed, it will not change (even by reset) until programmed to another value.

Appendix A – Connectors & Cables

Overview

This section describes the I/O module and the timing module connectors and cables (see Figure A-1). Both boards come with a 50-position 25-mil grid flat ribbon cable with a double row receptacle.

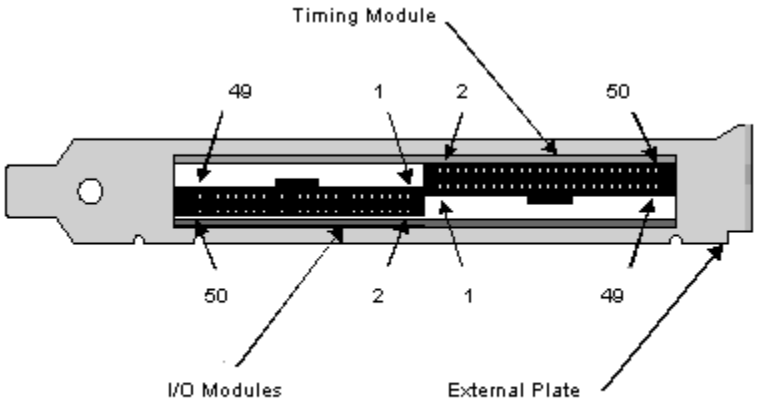


Figure A-1: Master Board Connectors

Input-Output Module Connector and Pin Assignments

The following functional groups are available: data input-output (I/O pins), output enable, and external output enable. Table A-1 describes the I/O module connector pin assignments, followed by a description of each pin group in Table A-2.

Pin	Name	Function	Pin	Name	Function
1	GND	Ground	2	IO0	I/O pin # 0
3	IO1	I/O pin # 1	4	IO2	I/O pin # 2
5	IO3	I/O pin # 3	6	GND	Ground
7	IO4	I/O pin # 4	8	IO5	I/O pin # 5
9	IO6	I/O pin # 6	10	IO7	I/O pin # 7
11	GND	Ground	12	IO8	I/O pin # 8
13	IO9	I/O pin # 9	14	IO10	I/O pin # 10
15	IO11	I/O pin # 11	16	GND	Ground
17	IO12	I/O pin # 12	18	IO13	I/O pin # 13
19	IO14	I/O pin # 14	20	IO15	I/O pin # 15
21	GND	Ground	22	IO16	I/O pin # 16
23	IO17	I/O pin # 17	24	IO18	I/O pin # 18
25	IO19	I/O pin # 19	26	GND	Ground
27	IO20	I/O pin # 20	28	IO21	I/O pin # 21
29	IO22	I/O pin # 22	30	IO23	I/O pin # 23
31	GND	Ground	32	IO24	I/O pin # 24
33	IO25	I/O pin # 25	34	IO26	I/O pin # 26
35	IO27	I/O pin # 27	36	GND	Ground
37	IO28	I/O pin # 28	38	IO29	I/O pin # 29
39	IO30	I/O pin # 30	40	IO31	I/O pin # 31
41	GND	Ground	42	OEO0	Output enable line # 0
43	OEO1	Output enable line # 1	44	OEO2	Output enable line # 2
45	OEO3	Output enable line # 3	46	GND	Ground
47	XOE0	Ext. output enable # 0	48	XOE1	Ext. output enable # 1
49	XOE2	Ext. output enable # 2	50	XOE3	Ext. output enable # 3

Table A-1: I/O Module Connector Pins

Name	I/O	Function
IOX	Input/ output	Input/output pin number. Data input-output lines. A 74FCT245 is used as a data driver.
OEOX	Output	Output enable lines for each I/O group (IO0-IO7 group 0, IO8-1015 group 1, etc.). A low on this output indicates that the specific group output drivers are enabled (the GT-DIO is driving data out). These lines are pulled up internally.
XOEX	Input	External outputs enable controls for each I/O pin group. A low on this input line forces the specific group to disable its output drivers. These lines are pulled up internally.

Table A-2: I/O Module Connector Pin Groups

Timing Module Connector and Pin Assignments

Table A-3 describes the timing connector pin assignments, followed by a description of each pin group in Table A-4.

Pin	Name	Function	Pin	Name	Function
1	GND	Ground	2	EXT0	External event line # 0 (LSB)
3	EXT1	External event line # 1	4	EXT2	External event line # 2
5	EXT3	External event line # 3	6	GND	Ground
7	EXT4	External event line # 4	8	EXT5	External event line # 5
9	EXT6	External event line # 6	10	EXT7	External event line # 7
11	GND	Ground	12	EXT8	External event line # 8
13	EXT9	External event line # 9	14	EXT10	External event line # 10
15	EXT11	External event line # 11	16	GND	Ground
17	EXT12	External event line # 12	18	EXT13	External event line # 13
19	EXT14	External event line # 14	20	EXT15	External event line # 15 (MSB)
21	GND	Ground	22		Spare
23		Spare	24	GND	Ground
25	XPAUSE	External override pause command	26	GND	Ground
27	XTRIG	External override run command	28	GND	Ground
29	ORUN	Run Indication	30	GND	Ground
31	XCLK	External Clock input	32	GND	Ground
33	XSTB	External Strobe input	34	GND	Ground
35	XCEN	External Clock Enable	36	GND	Ground
37		Spare	38	GND	Ground
39	OCLK	Clock Output	40	GND	Ground
41	OSTB	Strobe Output	42	GND	Ground
43		Spare	44	GND	Ground
45	BCLK	Spare B Clock	46	GND	Ground
47		Spare	48		Spare
49		Vcc (+5V)	50		Vcc (+5V)

Table A-3: Timing Module Connector Pins

Name	I/O	Function
EXT 1-16	Input	External event lines
XPAUSE	Input	When set to low, the board is forced to the PAUSE state. Only if the board is armed. If both (XTRIG and XPAUSE) are low and the board was armed, the board will toggle between the RUN state and the PAUSE state every clock cycle.
XTRIG	Input	When set to low, the board is forced to the RUN state. Only if the board is armed. If both (XTRIG and XPAUSE) are low and the board was armed, the board will toggle between the RUN state and the PAUSE state every clock cycle.
ORUN	Output	When low, the board is in the RUN state.
XCLK	Input	External clock
XSTB	Input	External strobe
XCEN	Input	External clock enable. When low, the board is forced to use the external clock. The external clock must be present before this line is set to low. If this line is set to low before arming the board, it may cause improper operation of the board.
OCLK	Output	Clock output
OSTB	Output	Strobe output
BCLK	Output	B clock output

Table A-4. Timing Module Connector Pin Groups

Appendix B – Control Memory Command

Overview

The information in this section describes the control memory command micro code. This information is useful when reading from and writing to the DIO board control memory. The control memory contains a 32-bit command for each step. Those commands serve as input to the on-board sequencer controlling the flow of the program counter and the direction of the I/O pins. See the *Commands* section in "Chapter 4 – Theory of Operation" for a complete and detailed list of commands and parameters.

Command Micro Code

The control memory consists of 32 bit commands. Each command is divided into six fields. A command layout diagram with the name of each field and position (bit number) is shown in Table B-1, followed by a definition of each command field in Table B-2.

Command Layout

BIT #	31 28	27 25	24 22	21 20	19 17	16 0
FIELD NAME	I/O Groups Control	Reserved (0)	Operation Code	Register	Condition	Address

Table B-1: Command Layout

COMMAND FIELD	DESCRIPTION
I/O Groups Control	These bits control the direction of the I/O bits 31-28 pin groups as described in Table B-3.
Reserved, bits 27-25	Reserved for future versions. Must be set to 0.
Operation Code, bits 24-22	These bits provide the command code as described in Table B-4.
Register, bits 21 and 20	SPECIFIES THE INTERNAL REGISTER USED WITH EITHER THE RELATED COMMAND OR THE EXTERNAL EVENT LINE NUMBER (0-3) CONDITIONS (SEE TABLE 4-1), AS DESCRIBED IN TABLE B-5.
Condition, bits 19-17	This field is the condition code for the related commands and the tree address MSBs for the JUMP FAR command (see Table 4-1). Condition codes are described in Table B-6.
Address, bits 16-0	THIS FIELD CONTAINS THE ADDRESS FOR BRANCH COMMANDS: **JUMP**, **LOOP**, **GOTO** AND **CALL**. WHEN THE OPERATIONS CODE IS SET TO THE SET COMMAND, THIS FIELD (BITS 0-15) IS USED AS DATA TO BE ASSIGNED TO A REGISTER.

Table B-2: Command Field Descriptions

I/O Groups Control Field

I/O pins	Control word bit	Direction for bit = 1	Direction for bit = 0
0-7	28	IN	OUT
8-15	29	IN	OUT
16-23	30	IN	OUT
23-32	31	IN	OUT

Table B-3: I/O Groups Control Field

Operation Code Field

Mnemonic	Additional fields	Value	Bit 24	Bit 23	Bit 22
NOP	None	0	0	0	0
JUMP FAR	Destination = Condition & Address	1	0	0	1
JUMP NEAR	Condition & Address	2	0	1	0
LOOP	Reg, Address & Condition	3	0	1	1
SET	Reg & Address	4	1	0	0
CALL	Condition & Address*	5	1	0	1
RETURN	Condition	6	1	1	0
PAUSE	Condition	7	1	1	1
HALT	Condition = 7	7	1	1	1

* Address in the CALL is divided by 8 (see Table 4-1).

Table B-4: Operation Code Field

Register Field

Register	External Event Line # B*	Bit 21	Bit 20
A	0	0	0
B	1	0	1
C	2	1	0
D	3	1	1

* See Table B-6

Table B-5: Register Field

Command Field

Condition	Bit 17-19	Bit 19	Bit 18	Bit 17
None	0	0	0	0
External event lines value > Register value	1	0	0	1
External event lines value < Register value	2	0	1	0
External event lines value = Register value	3	0	1	1
External event lines value <> Register value	4	1	0	0
External event line # B is Low*	5	1	0	1
External event line # B is High*	6	1	1	0
HALT when combined with PAUSE command	7	1	1	1

* *B* is determined by the Register field

Table B-6: Command XXX Field

Guidelines on How to Write Control Commands

When writing commands to a file or to the control memory, the following guidelines should be observed:

1. Commands other than NOP can reside every four steps. Micro code should be the same for all four steps except for I/O Groups Control direction and Operation Code. The Operation Code should be encoded only in the fourth step.
2. The direction can be changed at each step.
3. Control memory and output memory must be written to all boards, Master and Slave.

Appendix C – Specifications

Overview

This section describes the timing module and I/O module specifications. Table C-1 describes the timing module specifications pin assignments, followed by a description of the I/O module specifications in Table C-2:

Timing Module Specifications

Parameter	GT25 – Timing			GT50 - Timing			Units
	Min	Type	Max	Min	Type	Max	
Internal Test Clock							
Freq. Range	1000		25M	1000		50M	Hz
Resolution	The greater of 1 Hz or 0.2%.						
Internal B Clock							
Freq. Range	400K		100M	400K		100M	Hz
Resolution	The greater of 1 HZ or 0.2%.						
External Clock with Internal Strobe							
Freq. Range	0		25M	0		50M	Hz
Pulse width	15			10			nS
XCLK to OCLK delay	42	50	59	42	50	59	nS
XCLK to OSTB delay *	22		54	22		54	nS
Data setup time to OSTB **	8			6			nS
Data hold time to OSTB	3			3			nS
External Clock with External Strobe							
Freq. Range							
External Clock	0		25	0		33	MHz
External Strobe	0		25	0		33	MHz
Pulse width							
External Clock	15			10			nS
External Strobe	15			10			nS
XCLK to OCLK delay	13	17	22	13	17	22	nS
XCLK to OSTB delay	13	17	22	13	17	22	nS
Data setup time to OSTB **	8			6			
Data hold time to OSTB	3			3			

Parameter	GT25 – Timing			GT50 - Timing			Units
External Control Inputs							
Input Level High	2.0		5.1	2.0		5.1	V
Input Level Low	-0.1		0.8	-0.1		0.8	V
Input Current High			48			48	mA
Input Current Low			48			48	mA
External Control Outputs							
Type	74AS805						
Output Level High	2.4			2.4			V
Output Level Low		0.35	0.5	-0.1	0.35	0.5	V
Output Current High			48			48	mA
Output Current Low			48			48	mA
Physical							
Size	6,25”x4.2”						
Weight	100g						
Supply Current @ 5VDC		200	400		200	600	mA
Supply Current @ 12VDC		25	35		25	50	mA

Table C-1: Timing Module Specifications (Continues)

I/O Module Specifications

	Min	Type	Max	Units
Input/Output				
Channels Per Module	32 I/O			
Type	74FCT245			
Output level Low		0.3	0.55	V
Output level High	2.4	4.3		V
Source/Sink Current			-15/64	mA
Input level Low	-0.1		0.8	V
Input level High	2.0		5.1	V
Driver Enable Control				
Configuration Per Module	Four Groups of 8			
XOEN Input level Low	-0.1		0.8	V
XOEN Input level High	2.0		5.1	V
OEN Output level Low		0.35	0.5	V
OEN Output level High	2.4			V
OEN Source/Sink			-10/10	mA
Memory				
Types	In, Out, Control			
Depth*	16	64-256	1024	KB
Output Timing				
Output change from OCLK		12	18	nS
Skew (same module)		2	3	nS
Skew (other module)		4	5	nS
Input Timing				
Setup before OSTB (15nS Memory mdl.) Module)	10			nS
Setup before OSTB (20nS Memory mdl.))	15			nS
Setup before OSTB (30nS Memory Module)	20			nS
Physical				
Operating temperature	0		50	°C
Storage temperature	-20		70	°C
Size	13.2”x4.8” (Full Size AT Card)			
PC Slot Type	AT (16 Bit)			
Weight	475			g
Power 5VDC**		0.7	4.5	A

* Up to four memories bank on one GT-DIO I/O module. Each one can be 16KB, 64KB or 256KB.

** The maximum current occurs when running the vector at 35MHz with full memory configuration.

Table C-2: I/O Module Specifications (Continues)

Index

A

Abbreviations 2
Architecture 17

B

B Clock 26
Block Diagram 17
Board Installation 14

C

Clock and Strobe Signals 19
Clock B 26
Commands 21
Common Elements 3
Conditions 22
Connectors & Cables 27
Control Memory Command Micro Code 31
Conventions
  Style 2
Copyright iii

D

Definitions 2
DIO
  Definition 2
  DIO board
    Definition 2
  Domain overview 4
  Overview 3
  Product families 3
Discharge Static Electricity 7
Disclaimer iii
Domain
  Definition 2
  Overview 4

E

Electricity
  Discharge 7
External
  Event Lines 24
  Pause 25
  Trigger 24

G

Getting Started 15
GT25/50
  Architecture and Capabilities 5
  Definition 2
GT25/50-DIO Series 3
GT515x Series 3
GTXI Installation 14
Guidelines - Control Commands 33

H

Halt 23
Hardware 9
HD
  Definition 2
Help iii

I

I/O
  Connector 28
  Pin 18
  User Guide Definition 2
I/O Module
  Connector 28
  Pin Assignments 28
  Specifications 37
Installation 7
  GTXI 14
  Procedures 9
Installing Timing Module 13
Introduction 1

M

Masters and Slaves 18

Memory
Installation 11
Management 20
Options 8
Upgrades....11
Micro Code....31
O
Organization 1
Overview 3
P
Packing List....7
Pause
Command 25
State 23
PC Bus Interface
Overview 4
Precautions
Static Electricity 7
Program Sequencer....20
R
Related Documents....1
Requirements....9
Run State 23
S
Safety and Handling iii
Sequencer 20
Commands....22
Setting the Base Address 10
Setup....7
Slave
Definition....2
Software....6
Component Overview....5
Trigger 24
User Guide....2
Specifications 35
States 23
Static Electricity
Precautions 7
Step
Definition....2
Strobe Signals....19
System
Overview 3
Requirements....9, 14
T
Technical support iii
Testware
Definition....2
Theory of Operation 17
Timing
Connector 29
Module Pin Assignments....29
Module Specifications 35
Pin Assignments 29
Trademarks....iv
Trigger Command....24
U
Upgrades....11
User Knowledge and Skills 1
V
Vector
Definition....2
Verify Terminator Jumpers....10
W
Warranty.... iii
X
X Register....25

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