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Find the *Kontron / Thales / Matrix MD-CPUE100* at our website: *Click HERE*

MD-CPU100
MX-CPU100
MS-CPU100
MSX-CPU100

MC68000 CPU
12.5 MHz
512 KB or 1 MB DRAM

- 12.5 MHz MC68000 CPU
- Double-Height (6U) and Single-Height (3U) Board Sizes Available
- 512 KB or 1 MB of Zero-Wait-State Dual-Accessed DRAM with Express Memory Architecture
- Two 28-Pin EPROM Sockets
- 8 KB Local Battery-Backed SRAM
- Battery-Backed Time-of-Day Clock/Calendar
- Interrupt Handler for all Seven VMEbus IRQs
- VMEbus Mailbox Interrupt
- 64 Hz Time-Slice Interrupt
- Local Semaphore Interrupt
- Two Serial Ports
- Programmable Control and Status Registers
- System Controller Jumper Enabled
- Fair, ROR Requester
- Watchdog Timer with Software Enable
- Industrial and Extended Temperature Versions Available

Efficient CPU for Real-Time Environments

The CPU100 processor is tailored for high-end, 16-bit applications in both stand-alone and multiprocessing real-time environments. Standard features of the CPU100 include Board Control and Status Registers, MATRIX Corporation's Express Memory Architecture, multiple interrupt functions, and a complete serial I/O interface.

Express Memory Architecture

The CPU100 series utilizes MATRIX Corporation's unique Express Memory Architecture which increases memory performance by combining a queued refresh scheme with zero-wait-state processor operation. In this scheme, a refresh queuing circuit stores several refresh ticks and then bursts refresh packets to the memory array. By combining this refresh feature with an efficient VMEbus interface, the Express Memory Architecture cuts memory refresh overhead by 51% over standard memory architecture designs.

Board Control & Status Registers

The software-regulated Board Control and Status Registers (BCSRs) determine several functions of the CPU100. These BCSR functions include interrupt masking and source flagging, control of VMEbus arbitration techniques (ROR, Interrupt, and bus locking), and the VMEbus slave address. Consequently, the CPU100 efficiently handles interrupts, provides a flexible means of controlling the VMEbus resource, and eases board configuration handling.

Interrupt Features

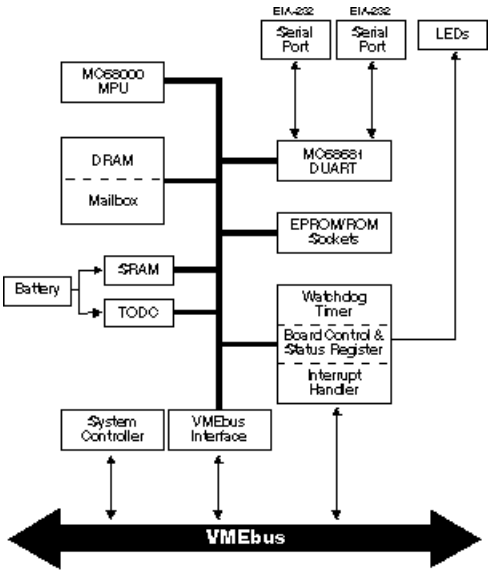
All CPU100 interrupt sources are software maskable. The CPU100 controls all internal I/O, utility sources, and VMEbus interrupt levels. An internally generated semaphore interrupt may be utilized for efficient task initialization or any other user-specific requirement.

Configurable I/O Ports

The CPU100 offers two serial ports. The first is an EIA-232 terminal and the second is an EIA-422 (DTE or DCE), or a full-featured EIA-232 (DTE or DCE). Both ports are routed to P2 and front panel DB-25 connectors for front or rear cabling schemes.

Software Support

Real-time operating systems are supported by MATRIX and third-party resources. Contact MATRIX for assistance with software selection.



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