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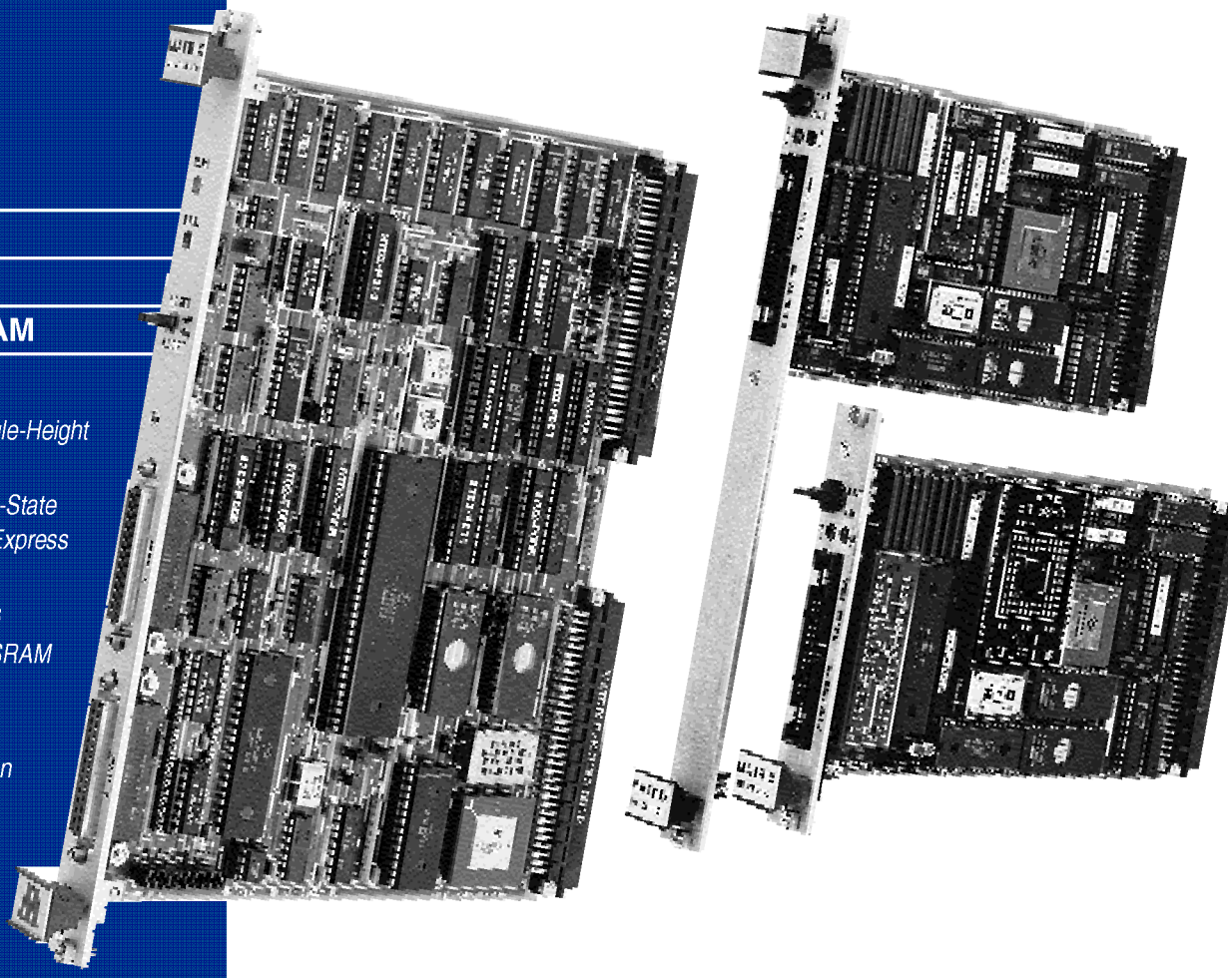
Find the *Kontron / Thales / Matrix MD-CPUE100* at our website: *Click HERE*

MD-CPU100
MX-CPU100
MS-CPU100
MSX-CPU100

MC68000 CPU

12.5 MHz

512 KB or 1 MB DRAM



- *12.5 MHz MC68000 CPU*
- *Double-Height (6U) and Single-Height (3U) Board Sizes Available*
- *512 KB or 1 MB of Zero-Wait-State Dual-Accessed DRAM with Express Memory Architecture*
- *Two 28-Pin EPROM Sockets*
- *8 KB Local Battery-Backed SRAM*
- *Battery-Backed Time-of-Day Clock/Calendar*
- *Interrupt Handler for all Seven VMEbus IRQs*
- *VMEbus Mailbox Interrupt*
- *64 Hz Time-Slice Interrupt*
- *Local Semaphore Interrupt*
- *Two Serial Ports*
- *Programmable Control and Status Registers*
- *System Controller Jumper Enabled*
- *Fair, ROR Requester*
- *Watchdog Timer with Software Enable*
- *Industrial and Extended Temperature Versions Available*

Efficient CPU for Real-Time Environments

The CPU100 processor is tailored for high-end, 16-bit applications in both stand-alone and multiprocessing real-time environments. Standard features of the CPU100 include Board Control and Status Registers, MATRIX Corporation's Express Memory Architecture, multiple interrupt functions, and a complete serial I/O interface.

Express Memory Architecture

The CPU100 series utilizes MATRIX Corporation's unique Express Memory Architecture which increases memory performance by combining a queued refresh scheme with zero-wait-state processor operation. In this scheme, a refresh queuing circuit stores several refresh ticks and then bursts refresh packets to the memory array. By combining this refresh feature with an efficient VMEbus interface, the Express Memory Architecture cuts memory refresh overhead by 51% over standard memory architecture designs.

Board Control & Status Registers

The software-regulated Board Control and Status Registers (BCSRs) determine several functions of the CPU100. These BCSR functions include interrupt masking and source flagging, control of VMEbus arbitration techniques (ROR, Interrupt, and bus locking), and the VMEbus slave address. Consequently, the CPU100 efficiently handles interrupts, provides a flexible means of controlling the VMEbus resource, and eases board configuration handling.

Interrupt Features

All CPU100 interrupt sources are software maskable. The CPU100 controls all internal I/O, utility sources, and VMEbus interrupt levels. An internally generated semaphore interrupt may be utilized for efficient task initialization or any other user-specific requirement.

Configurable I/O Ports

The CPU100 offers two serial ports. The first is an EIA-232 terminal and the second is an EIA-422 (DTE or DCE), or a full-featured EIA-232 (DTE or DCE). Both ports are routed to P2 and front panel DB-25 connectors for front or rear cabling schemes.

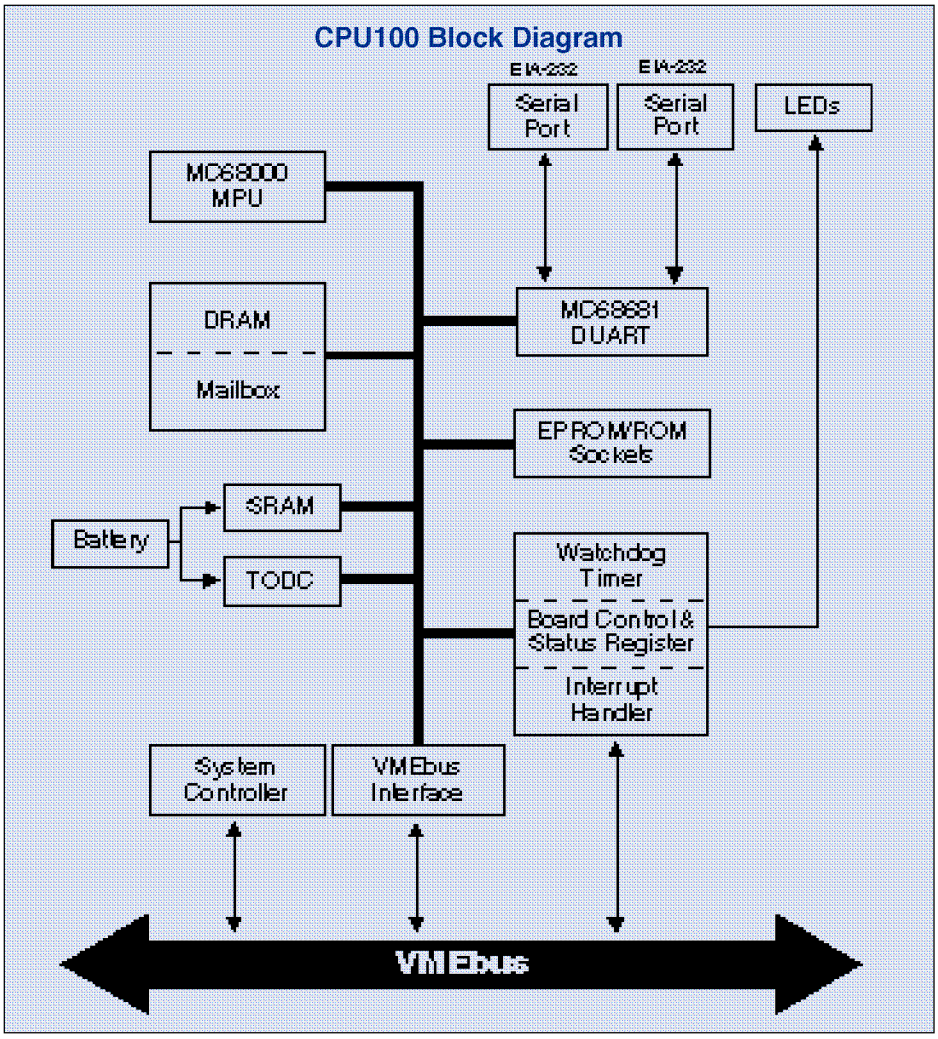
Software Support

Real-time operating systems are supported by MATRIX and third-party resources. Contact MATRIX for assistance with software selection.

MATRIX Corporation ▼ 1203 New Hope Road ▼ Raleigh, NC 27610 ▼ (800) 848-2330 ▼ FAX (919) 231-8001

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CPU100 Block Diagram



Ordering Information

M_-CPU10_-N-

Size & Environmental Class
- *6U Industrial ..... D*
- *6U Extended Temperature ..... X*
- *3U Industrial ..... S*
- *3U Extended Temperature ..... SX*

DRAM Memory
- *512 KB DRAM 5*
- *1 MB DRAM 1*

Serial Port B
- *EIA-232 ..... 2*
- *EIA-422 ..... 4*

Double-height (6U) front panel is available.

Associated Cables

Part Number	Description
6D25P-D25B	*For 6U board; 6-foot, 25 conductor cable with both pin and socket D-25 serial port connectors. One cable is needed for each serial port.*
6V50-D25B-B	*For 6U board; 6-foot, 50 conductor cable with dual pin and socket D-25 serial port connectors.*
6RCMS100-B-B	*For 3U board; 6-foot, 40 conductor cable with dual pin and socket D-25 serial port connectors.*

Specifications

Standard Compliance	ANSI/IEEE 1014-1987
Processor	MC68000 @ 12.5 MHz
VMEbus Interface	MA24/16, MD16/8 SA24, SD16/8, RMW, SADO
Serial Ports	One EIA-232 One 232/422
Maximum Baud Rate	Port A-38.4 Kbaud async Port B-614.4 Kbaud sync, 38.4 Kbaud async
Counter/Timers	One programmable, 16 bits One selectable (64 Hz, 1 Hz, 1/minute, 1/hour)
Interrupt Lines/Levels	18/7
Power Requirements	+5V @ 2.0A typical ±12V @ 20 mA maximum
Relative Humidity	0 to 95%, noncondensing
Storage Temperature	-40° to +85°C
Operating Temperature:	
MD-CPU100 (6U Industrial)	0° to +70°C
MX-CPU100 (6U Ext. Temp.)	-40° to +85°C
MS-CPU100 (3U Industrial)	0° to +70°C
MSX-CPU100 (3U Ext. Temp.)	-40° to +85°C

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