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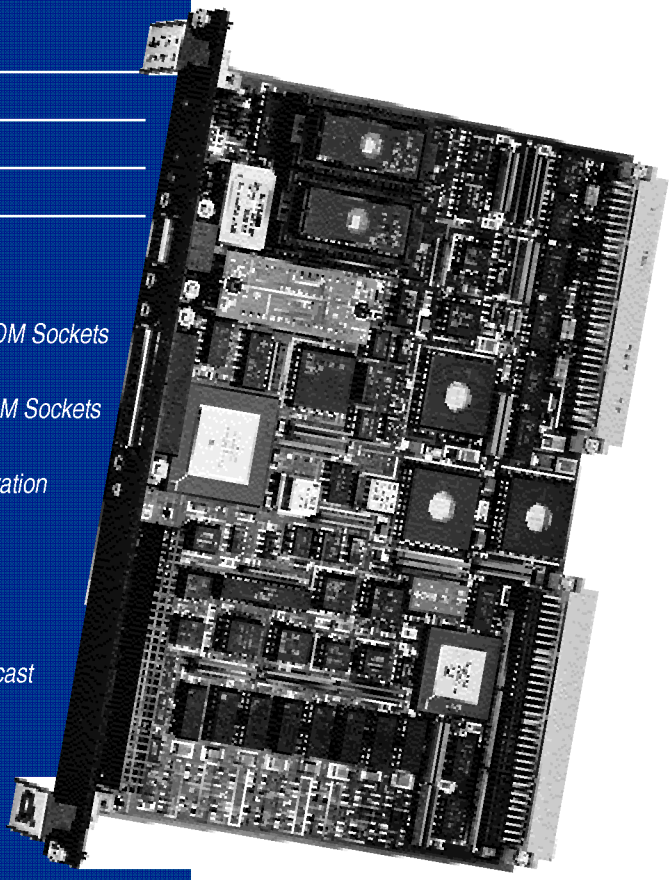
Find the *Kontron / Thales / Matrix MD-CPUE100* at our website: *Click HERE*

MD-CPUE100

MC68HC000 CPU

AUI Ethernet Interface

Four Serial Ports



- *MC68HC000 at 12.5 MHz*
- *512 KB, 1, 2, or 4 MB DRAM*
- *Two 32-pin EPROM/Flash EPROM Sockets Support up to 1 MB Devices*
- *Two 32-pin Battery-Backed SRAM Sockets Support up to 512K x 8 Devices*
- *512 bytes EEPROM for Configuration Data*
- *IEEE 802.3 Ethernet Controller (DP8390):*
  - *On-board DMA*
  - *Physical, Multicast, and Broadcast Modes*
  - *Network Statistics Counters*
  - *16 byte FIFO with Programmable Thresholds*
- *Four Serial Ports*
- *Low Power, 5V-Only Operation*
- *Battery-Backed Clock/Calendar*
- *Interrupt Handler for all Seven VMEbus IRQs*
- *Two 16-Bit Programmable Timers*
- *Watchdog Timer with Software Enable*
- *System Controller Jumper Enabled*
- *Front Panel Status LEDs*
- *Programmable Control and Status Registers*

SBC for Node Controllers

MATRIX Corporation offers a single-board computer (SBC) with an on-board Ethernet interface intended for network-distributed real-time control applications and embedded communication systems. The MD-CPUE100 can be a stand-alone processor within a VMEbus system, or it can act as a gateway to other VMEbus processors. This single-slot solution offers a high degree of integration with memory and interface combinations that normally require multiple-board assemblies.

Efficient, High-Speed Communication

The Ethernet Controller provides all the Media Access Control layer functions required for packet transfers in accordance with the IEEE 802.3 standard. The on-board FIFO and DMA form an efficient data management scheme for handling local DMA transfers to the on-board memory. Four serial communication ports provide either EIA-232 or TTL interfaces. One EIA-232 serial port is available via the front panel for easy connection to a debug/maintenance terminal.

Flexible Memory Configurations

Memory configurations on the CPUE100 allow the user to select various combinations of DRAM, SRAM, and EPROM. Byte parity is optional on the zero wait state DRAM and provides an interrupt for error correction. The MD-CPUE100 supports UV, 5V Flash, and 12V Flash EPROMs and allows in-socket programming of Flash EPROM devices.

Other Features

Control and status registers program VMEbus slave address map, interrupt control, and other on-board functions. The MD-CPUE100's Interrupt Handler supports all seven VMEbus IRQs, SYSFAIL, ACFAIL, and on-board interrupts. Two 16-bit timers can generate periodic interrupts, count the time between software-initiated events, or serve as additional baud rate generators for any of the serial ports. An on-board monitor resets the CPU during low DC voltage conditions.

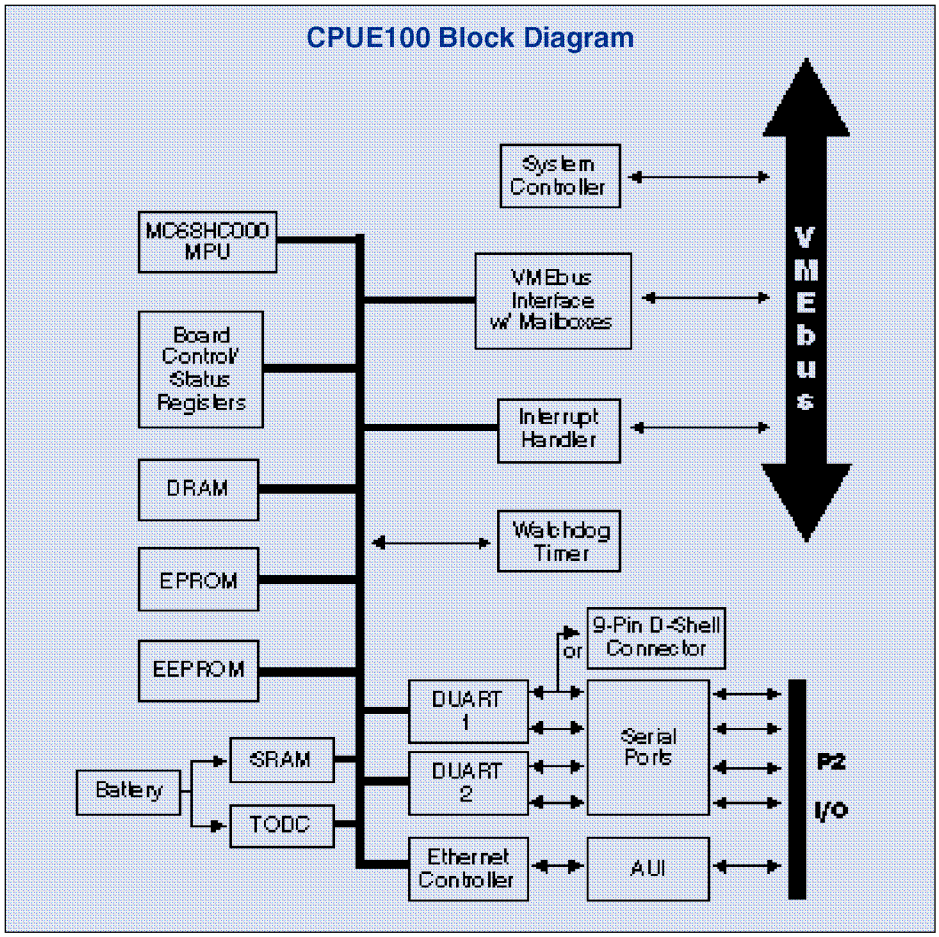
Software Support

Real-time operating systems are supported by MATRIX and third-party resources. Contact MATRIX for assistance with software selection.

MATRIX Corporation ▼ 1203 New Hope Road ▼ Raleigh, NC 27610 ▼ (800) 848-2330 ▼ FAX (919) 231-8001

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CPUE100 Block Diagram



Specifications

VMEbus Standard Compliance	ANSI/IEEE Std 1014-1987
VMEbus Interface	MA24/16, MD16/8, SA24/16, SD16/8, RMW, ADO
Microprocessor Unit (MPU)	MC68HC000 @ 12.5 MHz
Ethernet Standard Compliance	ANSI/IEEE Std 802.3-1985
Serial Ports	
Maximum Baud Rate	38.4 Kbaud
Front Panel Interface (Port 1A)	EIA-232, DCE
P2 (Ports 1A, 1B, 2A, 2B)	EIA-232 or TTL, DCE
On-Board Memory	
DRAM	512 KB, 1 MB, 2 MB, or 4 MB
EPROM Sockets	Two 32-pin
SRAM Sockets	Two 32-pin
TODC Accuracy	±26 sec/month maximum
Power Requirements	5V @ 1.4A typical +12V (if used, current requirements are determined by the 12V Flash EPROMs and the external Ethernet transceiver)
Standby Power (On-Board Lithium battery)	
Battery Life	>10 years typical
Relative Humidity	0 to 95%, noncondensing
Storage Temperature	-40° to +85°C
Operating Temperature:	
MD-CPUE100 (Industrial)	0° to +70°C

Ordering Information

MD-CPUE10 _-N

Environmental Class
- *Industrial* ..... *D*

DRAM Memory
- *512 KB DRAM* *5*
- *1 MB DRAM* *1*
- *2 MB DRAM* *2*
- *4 MB DRAM* *4*

Serial Port Interface (P2)
- *TTL* ..... *T*
- *EIA-232* *2*

DRAM Byte Parity
- *No Parity* ..... *N*
- *Parity* ..... *P*

SRAM Memory
- *No SRAM installed* ..... *N*
- *32 KB SRAM* *3*
- *64 KB SRAM* *6*
- *128 KB SRAM* *1*
- *256 KB SRAM* *2*
- *512 KB SRAM* *5*
- *1 MB SRAM* ..... *M*

See page 75 for Ethernet Accessories.

Associated Cables

Part Number	Description
V64-CPUE100	*2-foot Ethernet drop cable and 6-foot serial port connector cable.*
6D09P-D25P	*6-foot, nine conductor cable with D-9 connector mating to the CPUE100 and a D-25 connector provided for the user.*

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