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CIO-DAS1401/12,
CIO-DAS1402/12,
CIO-DAS1402/16

Data Acquisition & Control Boards

User's Manual



Revision 7
November, 2000

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1 INTRODUCTION

The installation and operation of all three of the CIO-DAS1400 series boards is very similar. Throughout this manual we use CIO-DAS1400 as a generic designation for the CIO-DAS1401/12, CIO-DAS1402/12 and CIO-DAS1402/16. When required due to the differences in the boards, the specific board name is used.

The CIO-DAS1400 is easy to use. This manual will help you quickly and easily setup, install and test your board. If you are unfamiliar or uncomfortable with board installation, please refer to your computer's documentation.

We recommend you perform the software installation described in section 2 prior to installing the board. InstaCal™ will show you how to set the switches and jumpers on the board before installing the board.

2 SOFTWARE INSTALLATION

The board has a variety of switches and jumpers to set before installing the board in your computer. By far the simplest way to configure your board is to use the InstaCal™ program provided as part of your software package. InstaCal™ will show you all available options, how to configure the various switches and jumpers to match your application requirements, and will create a configuration file that your application software (and the Universal Library) will refer to so the software you use will automatically know the exact configuration of the board.

Please refer to the Software Installation Manual regarding the installation and operation of InstaCal™. The following hard copy information is provided as a matter of completeness, and will allow you to set the hardware configuration of the board if you do not have immediate access to InstaCal™ and/or your computer.

3 HARDWARE INSTALLATION

You must set switches and jumpers before installing the board in your computer. The simplest way to configure your board is to use the InstaCal™ program provided as part of your software package.

The following information is provided to allow you to set the hardware configuration of the CIO-DAS1400 board if you do not have immediate access to InstaCal™ and/or your computer.

3.1 BASE ADDRESS SWITCHES

Unless there is already a board in your system using address 300 hex (768 decimal), leave the switches as they are set at the factory.

In the example shown in Figure 3-1, the CIO-DAS1400 is set at base address 300 hex.

Note: Wait State Enable is typically not required. Leave the WAIT EN switch in the UP (not enabled) position.

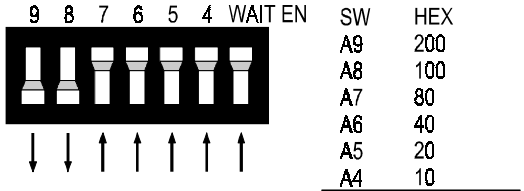
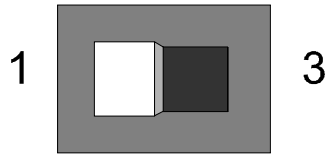


Figure 3-1. Base Address Switches

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3.2 DMA LEVEL SELECT

DMA level 1 or 3 may be selected. The default level is level 1 (Figure 3-2). There are other boards that use DMA levels. Some network boards do and so do some IEEE-488 interface boards. Check to see if you have other boards in your computer that use DMA channels 1 or 3.



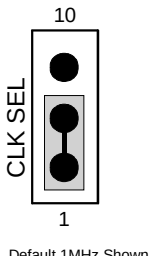
DMA LEVEL SELECT - DMA Level 1 is selected.

Figure 3-2. DMA Level Select Switch

3.3 1/10 MHz XTAL JUMPER

The 1/10 MHz (1 or 10 MHz) XTAL jumper selects the frequency of the square wave used as a clock by the A/D pacer circuitry. This pacer circuitry controls the sample timing of the A/D. The output driving the A/D converter is also available at the CTR 2 output pin on the main connector.

To maintain full compatibility with the original DAS-16, the CIO-DAS1400 required a 1 MHz crystal oscillator. When MetraByte redesigned the DAS-16 and added the faster 10MHz crystal, a jumper was provided to maintain compatibility with older software. The CIO-DAS1400 has the jumper because the DAS-16 has the jumper. For older software, the jumper must be in the 1 MHz position. If you are not concerned with compatibility with older software, use the 10MHz position.

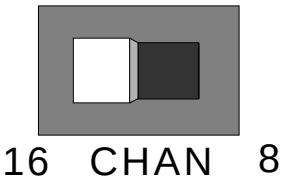


The CIO-DAS1400 is shipped with the jumper in the 1 MHz position (see Figure 3-3).

Figure 3-3 Clock Select Jumper

3.4 8/16 CHANNEL SELECT

The Analog inputs of the CIO-DAS1400 can be configured for eight differential or 16 single-ended inputs. Use the single-ended input mode if you have more than eight, low-noise analog inputs to sample. Using the differential input mode allows up to 10 volts of common mode noise rejection..



16/8 CHANNEL SELECT SWITCH

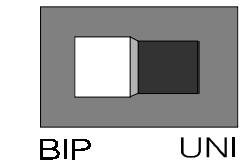
16 Channel differential-input mode shown

The CIO-DAS1400 comes from the factory configured for 16 single-ended inputs and the 8/16 switch is in the position shown in Figure 3-4. Set it for the type (or number) of inputs you require. On the CIO-DAS1402/16, this switch is located under the metal shield. If you need access to this switch, this shield may be removed by removing the two screws on the back of the CIO-DAS1402/16.

Figure 3-4. 8/16 Channel Select Switch

3.5 BIPOLAR/UNIPOLAR MODE SELECTION

The Bipolar or Unipolar configuration of the A/D converter is set by a switch. This switch is shown in Figure 3-5.. The switch controls all A/D channels. Although you cannot mix bipolar and unipolar channels, you can measure a unipolar input in the bipolar mode. (e.g., you can monitor a 0 to 5V input with a ±5 V channel). On the CIO-DAS1402/16, this switch is located under the metal shield. If you need access to this switch, this shield may be removed by removing the two screws on the back of the CIO-DAS1402/16.



BIP = Bipolar (+/-X) Ranges Selected
UNI = Unipolar (0-X) Ranges Selected

Figure 3-5. Bipolar/Unipolar Select Switch

Input amplifier gain is controlled by a software-programmed register located at BASE + B hex (11 decimal). Refer to the Register Architecture section for details on this register.

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3.6 PACER EDGE SELECT

The original Keithley MetraByte DAS-1600 was designed such that A/D conversion was initiated on the falling (trailing) edge of the convert signal from the internal pacer. Neither the original DAS-16, nor any of the other DAS-16 derivations convert on the falling edge. We are not aware of any A/D board that uses the falling edge to initiate the A/D conversion.

When using the falling edge to start the conversion, the A/D may be falsely triggered by 8254 pacer clock initialization glitching (easy to avoid but a real possibility in the DAS-1600). Converting on the falling edge mode also may lead to timing differences if the CIO-DAS1400 board is being used as a replacement for an older DAS16 series board.

Because using the falling edge trigger is undesirable, the CIO-DAS1400 has a jumper which allows you choose which edge of the internal pacer signal starts the A/D conversion. The jumper has no effect on an external pacer signal (EXTCLOCK). The only reason we supply you the option of a falling edge trigger is to provide complete compatibility for those who have developed software for a DAS-1600 using the AS-1600 drivers, AND, when using the CIO-DAS1400 with that software you observe sample timing differences.

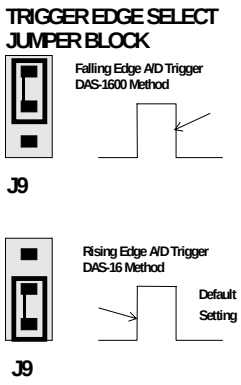


Figure 3-6. Pacer Edge Select

The CIO-DAS1400 is shipped with the jumper in the rising (leading) edge position. Figure 3-6 shows the edge selection options. For compatibility with all third party packages, with all DAS-16 software and with CIO-DAS1400 software, leave this jumper in the rising edge position.

3.7 AUXILIARY TRIGGER

There is a position for a header connector at the rear of the CIO-DAS1400. This connector provides the same function as that found on the DAS-1600.

The A/D trigger signal may come from this connector, if installed. A jumper controls which pin the trigger signal comes in from. We do not install this connector (nor is it installed on the DAS-1600).

3.8 BURST MODE GENERATOR

The burst mode generator is a clock signal that paces the A/D at the maximum multi-channel sample rate, then periodically performs additional maximum-rate scans. In this way, the channel-to-channel skew (time between successive samples in a scan) are minimized without taking a large number of undesired samples (see Figure 3-7).

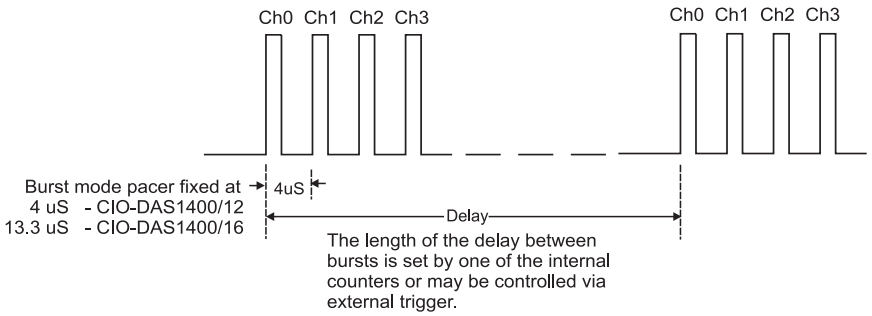


Figure 3-7. Burst Mode Generator Timing

The CIO-DAS1400 burst mode generator takes advantage of the fast A/D. The burst mode skew is 4.0 ms between channels for the CIO-DAS1400/12. It is 13.3 ms for the CIO-DAS1402/16.

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4 CONNECTOR PINOUTS

The CIO-DAS1400 analog connector is a 37-pin, “D”-connector accessible from the rear of the PC on the expansion back plate. The signals available are identical to the DAS-16, or optionally, an additional signal, SS&H OUT (Simultaneous Sample & Hold), is available at pin 26.

The connector accepts female 37D type connectors, such as on the C73FF-2, a two-foot cable. If frequent changes to signal connections or signal conditioning is required, we strongly recommend purchasing the CIO-MINI37 screw terminal board and the mating C37FF-2 cable.

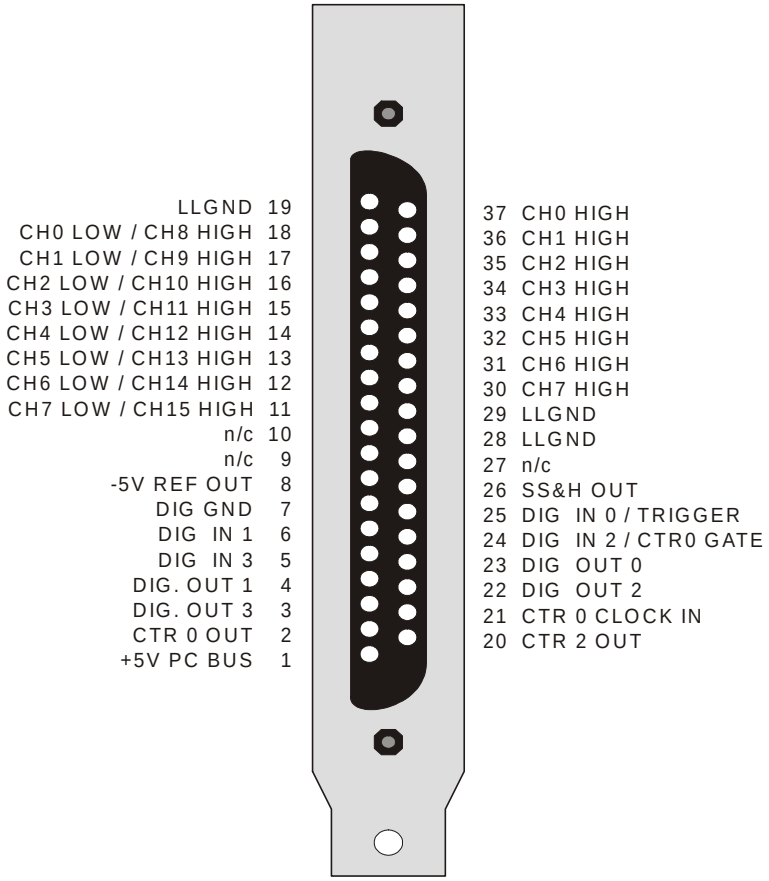


Figure 4-1. CIO-DAS1400 Analog Signal Connector

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5.1 ANALOG INPUTS

Analog signal connection is one of the most challenging aspects of applying a data acquisition board. If you are an electrical engineer you may wish to skip this section, but for many PC data acquisition users, the best way to connect your analog inputs may not be obvious. While complete coverage of this topic is beyond the scope of this manual, the following section provides some explanations and helpful hints regarding analog input connections. This section is included to help you achieve the optimum performance from your CIO-DAS1400 series board.

Before making connections, you should have a basic understanding of Single-Ended/Differential inputs and signal grounding/isolation. If you are already familiar with these topics, skip to the next section.

The CIO-DAS1400 provides either 8 differential or 16 single-ended input channels. Single-ended and differential inputs are described in the following section.

5.1.1 Single-Ended Inputs

A single-ended input measures the voltage between the input signal and ground. In single-ended mode, the CIO-DAS1400 measures the voltage between the input channel and LLGND. The single-ended input configuration requires only one physical connection (wire) per channel and allows the CIO-DAS1400 to monitor more channels than the 2-wire differential configuration using the same connector and onboard multiplexor. However, since the CIO-DAS1400 is measuring the input voltage relative to its own low level ground, single-ended inputs are more susceptible to both EMI (electro-magnetic interference) and any ground noise at the signal source. Figure 5-1 shows the single-ended input configuration

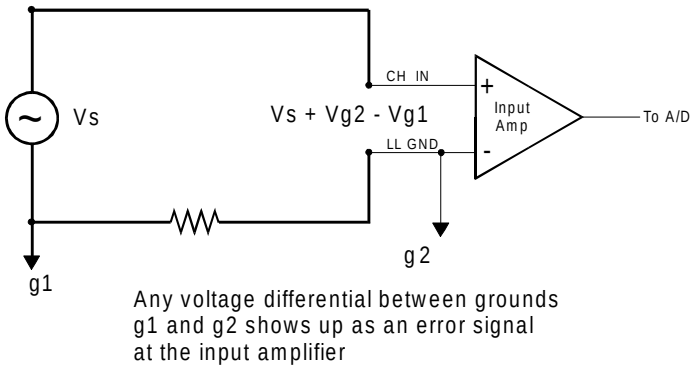


Figure 5-1. Single-Ended Input Configration

5.1.2 Differential Inputs

Differential inputs measure the voltage between two distinct input signals. Within a certain range (referred to as the common mode range), the measurement is almost independent of signal source to CIO-DAS1400 ground variations. A differential input is also much more immune to EMI than a single-ended one. Most EMI noise induced in one lead is also induced in the other, the input only measures the difference between the two leads, and the EMI common to both is ignored. This effect is a major reason there is twisted pair wire as the twisting assures that both wires are subject to virtually identical external influence. Figure 5-2 shows a typical differential input configuration.

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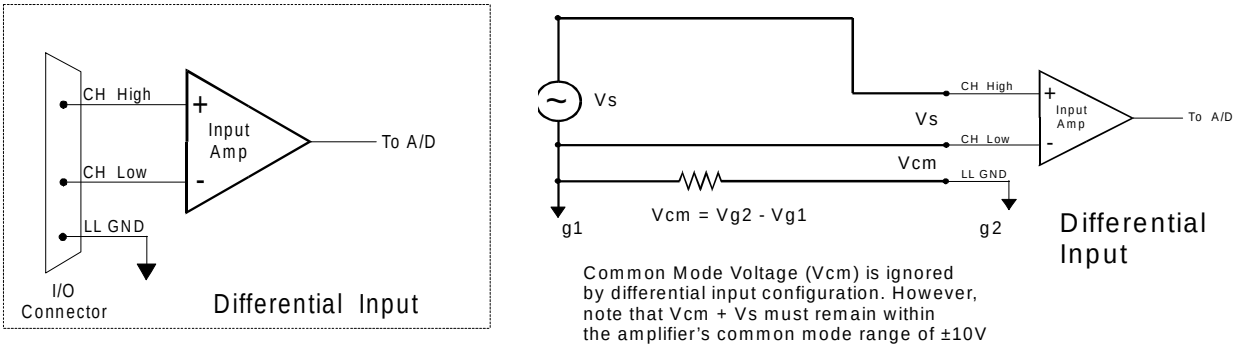


Figure 5-2. Differential Input - Common Mode Voltage Rejection

Before moving on to the discussion of grounding and isolation, it is important to explain the concepts of common mode, and common mode range (CM Range). Common mode voltage is depicted in the diagram above as Vcm. Though differential inputs measure the voltage between two signals, without (almost) respect to the either signal's voltages relative to ground, there is a limit to how far away from ground either signal can go. Though the CIO-DAS1400 has differential inputs, it will not measure the difference between 100V and 101V as 1 Volt (in fact the 100V would destroy the circuit!). This limitation or common mode range is depicted graphically in Figure 5-3. The CIO-DAS1400 common mode range is +/- 10 Volts. Even in differential mode, no input signal can be measured if it is more than 10V from the board's low level ground (LLGND).

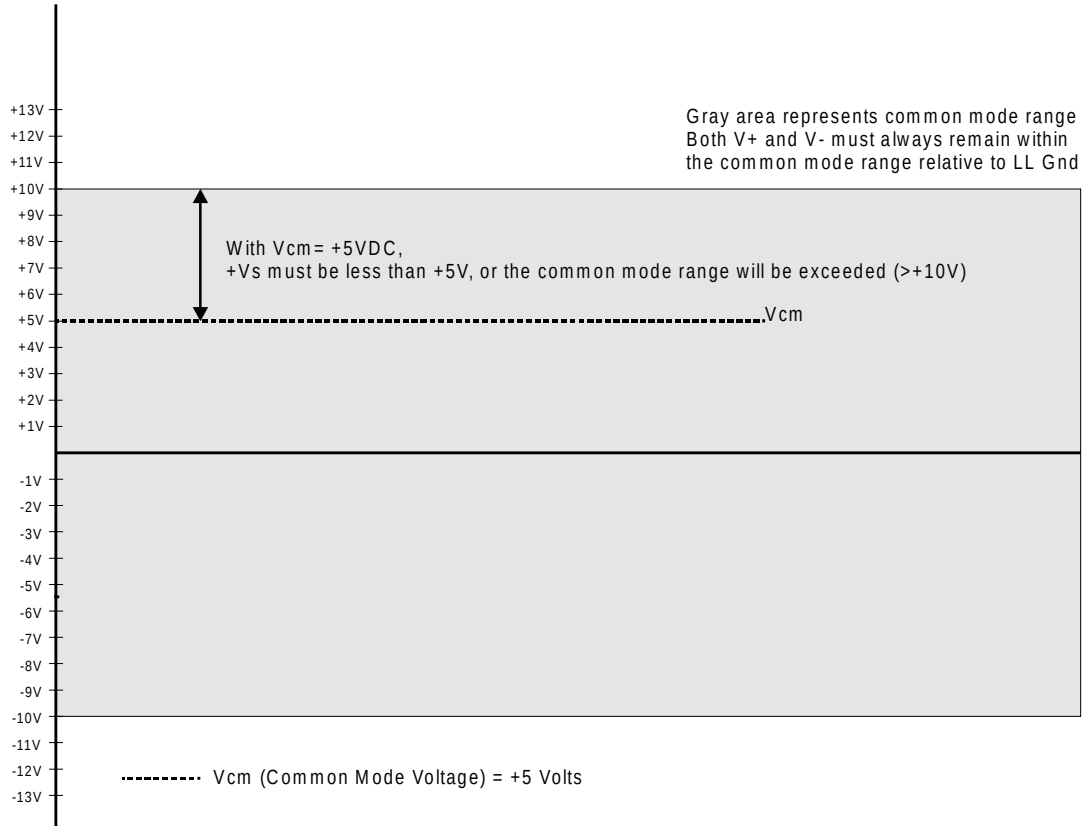


Figure 5-3. Common Mode Voltage Range Values

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5.2 SYSTEM GROUNDS and ISOLATION

There are three possibilities when connecting a signal source to the CIO-DAS1400 board:

The CIO-DAS1400 and the signal source may have the same (or common) ground. This signal source can be connected directly to the board.

The CIO-DAS1400 and the signal source may have an offset voltage between their grounds (AC and/or DC). This offset is commonly referred to as a common mode voltage. Depending on the magnitude of this voltage, it may or may not be possible to connect the board directly to your signal source. We will address this topic further in a later section.

The CIO-DAS1400 and the signal source may have isolated grounds. This signal source can be connected directly to the board.

5.2.1 Ground Testing

Perform the following test: Using a battery powered voltmeter*, measure the voltage between the ground signal at your signal source and at your PC. Place one voltmeter probe on the PC ground and the other on the signal source ground. Measure both the AC and DC Voltages.

*If you do not have access to a voltmeter, skip the test and read the following three sections. You may be able to identify your system type from the descriptions provided.

If both AC and DC readings are 0.00 volts, you may have a system with common grounds. However, since voltmeters will average out high frequency signals, there is no guarantee. Please refer to the section below titled Common Grounds.

If you measure reasonably stable AC and DC voltages, your system has an offset voltage between the grounds. This offset is referred to as a Common Mode Voltage. Read and observe the following warning, then proceed to the section describing Common Mode systems.

WARNING
An offset voltage greater than 30 volts can cause injury or death. It may also only damage board and computer circuitry. Use extreme care. If either the AC or DC voltage is greater than 10 volts, do not connect a CIO-DAS1400 series board to this signal source. You are beyond the board's usable common mode range and will need to either adjust your grounding system or add special signal isolation conditioning in order to take useful measurements.

If you cannot obtain a reasonably stable DC voltage measurement between the grounds, or the voltage drifts considerably, the two grounds are most likely isolated. To check for isolation, change your voltmeter to a resistance scale and measure the resistance between the two grounds. Turn both systems OFF prior to taking this resistance measurement. If the measured resistance is more than 100 Kohm, it's a fairly safe bet that your system has electrically isolated grounds.

5.2.2 Systems with Common Grounds

In the simplest (but perhaps least likely) case, your signal source will have the same ground as the CIO-DAS1400. This would typically occur when providing power or excitation to your signal source directly from the board. There may be other common ground configurations, but it is important to note that any voltage between the CIO-DAS1400 ground and your signal ground is a potential error voltage if you set up your system based on a common ground assumption.

As a safe rule of thumb, if your signal source or sensor is not connected directly to an LLGND pin on your board, it's best to assume that you do not have a common ground even if your voltmeter measured 0.0 Volts. Configure your system as if there is ground offset voltage between the source and the CIO-DAS1400. This is especially true if you are using either the CIO-DAS1402/16 or the CIO-DAS1402/12 at high gains, since ground potentials in the sub-millivolt range will be large enough to cause A/D errors, yet will not likely be measured by your handheld voltmeter.

5.2.3 Systems with Common Mode (Ground-Offset) Voltages

The most frequently encountered grounding scenario involves grounds that are loosely connected, but have AC and/or DC offset voltages between the board and the signal source ground. This offset voltage may be AC, DC, or both and may be caused by a number of things including EMI pickup or resistive voltage drops in ground wiring and connections.

5.2.4 Small Common Mode Voltages

If the voltage between the signal source ground and board ground is small, the combination of the ground voltage and input signal will not exceed the CIO-DAS1400's +/-10V common mode range, (i.e. the voltage between grounds, added to the maximum input voltage,

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stays within +/-10V), This input is compatible with the CIO-DAS1400 and the system may be connected without additional signal conditioning. Fortunately, most systems fall in this category and have a small voltage differential between grounds.

5.2.5 Large Common Mode Voltages

If the ground differential is large enough, the board's +/- 10V common mode range will be exceeded (i.e. the voltage between CIO-DAS1400 and signal source grounds, added to the maximum input voltage you're trying to measure exceeds +/-10V). In this case the CIO-DAS1400 cannot be directly connected to the signal source. You must change your system grounding configuration or add isolation signal conditioning. (Please look at our ISO-RACK and ISO-5B-series products to add electrical isolation, or give our technical support group a call to discuss other options).

CAUTION

Do not rely on the earth prong of a 120VAC for signal ground connections. Different ground plugs may have large and potentially even dangerous voltage differentials. Remember that the ground pins on 120VAC outlets on different sides of the room may only be connected in the basement. This leaves the possibility that the "ground" pins may have a significant voltage differential (especially if the two 120 VAC outlets happen to be on different phases!)

5.2.6 Isolated Grounds Exist

Some signal sources may be electrically isolated from the CIO-DAS1400. Figure 5-4 shows a typical isolated ground system. These signal sources are often battery powered. Isolated ground systems provide excellent performance, but require some extra care during connections to assure optimum performance is obtained. Please refer to the following sections for further details.

5.3 WIRING CONFIGURATIONS

Combining all the grounding and input type possibilities provides us with the following potential connection configurations. The combinations along with our recommendations on usage are shown in Table 5-1 below.

Table 5-1. Recommended Input Configurations

GROUND CATEGORY	INPUT CONFIGURATION	OUR VIEW
Common Ground	Single-Ended Inputs	Recommended
Common Ground	Differential Inputs	Acceptable
Common Mode Voltage < +/-10V	Single-Ended Inputs	Not Recommended
Common Mode Voltage < +/-10V	Differential Inputs	Recommended
Common Mode Voltage > +/- 10V	Single-Ended Inputs	Unacceptable without adding Isolation
Common Mode Voltage > +/-10V	Differential Inputs	Unacceptable without adding Isolation
Already Isolated Grounds	Single-ended Inputs	Acceptable
Already Isolated Grounds	Differential Inputs	Recommended

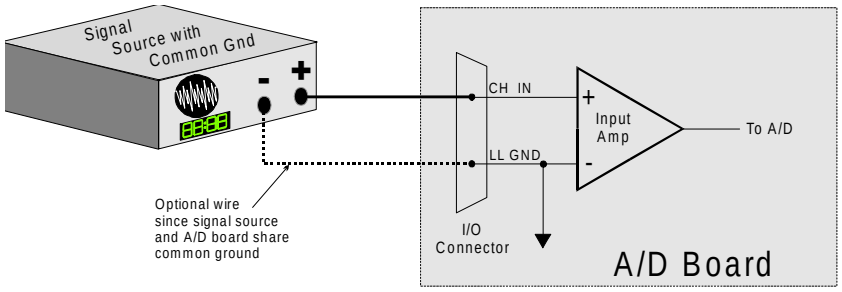
The following sections show recommended input wiring schemes for each of the eight possible input configuration/grounding combinations.

5.3.1 Common Ground / Single-Ended Inputs

Single-ended is the recommended configuration for common ground connections. However, if some of your inputs are common ground and some are not, we recommend you use the differential mode. There is no performance penalty (other than loss of channels) for

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using a differential input to measure a common ground signal source. However the reverse is not true. Figure 5-4 is a connection diagram for a common ground / single-ended input system.

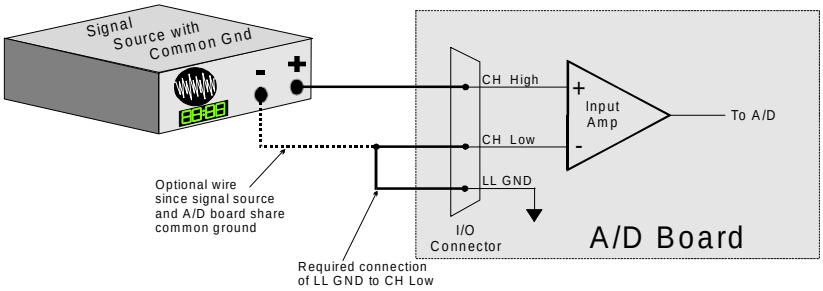


Signal source and A/D board
sharing common ground connected
to single-ended input.

Figure 5-4. Single-Ended, Common Ground

5.3.2 Common Ground / Differential Inputs

The use of differential inputs to monitor a signal source with a common ground is a acceptable configuration though it requires more wiring and offers fewer channels than selecting a single-ended configuration. Figure 5-5 shows the recommended connections in this configuration.



Signal source and A/D board
sharing common ground connected

Figure 5-5. Differential Input, Sharing Common Ground

5.3.3 Common Mode Voltage Less Than +/-10V / Single-Ended Inputs

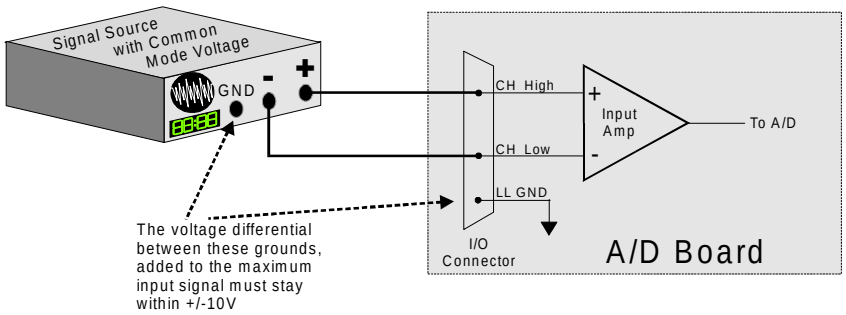
This is not a recommended configuration. In fact, the phrase common mode has no meaning in a single-ended system and this case would be better described as a system with offset grounds. Anyway, you are welcome to try this configuration, no system damage should occur and depending on the overall accuracy you require, you may receive acceptable results.

5.3.4 Common Mode Voltage, Less than +/-10V / Differential Inputs

Systems with varying ground potentials should always be monitored in the differential mode. Care is required to assure that the sum of the input signal and the ground differential (referred to as the common mode voltage) does not exceed the common mode range of the A/D board (+/-10V on the CIO-DAS1400). Figure 5-6 shows recommended connections in this configuration

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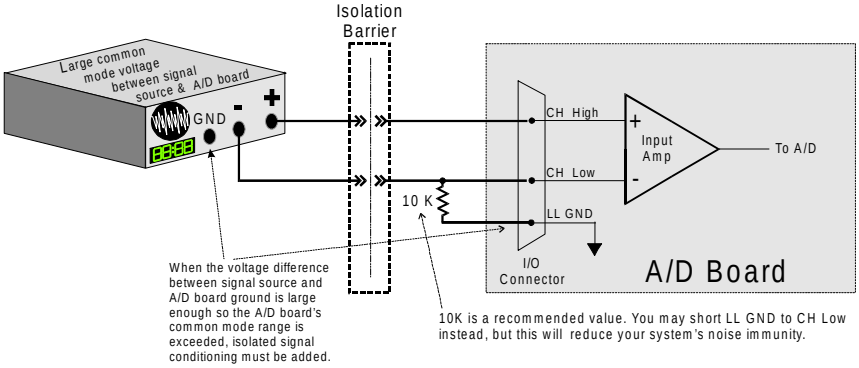


Signal source and A/D board with common mode voltage connected to a differential input.

Figure 5-6. Differential Input, Maximum Common Mode Voltage Requirement

5.3.5 Common Mode Voltage, Greater Than +/-10V

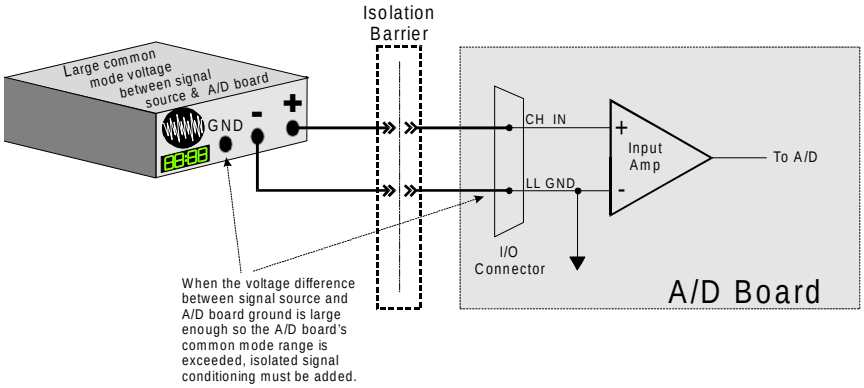
The CIO-DAS1400 will not directly monitor signals with common mode voltages greater than +/-10V. You will either need to alter the system ground configuration to reduce the overall common mode voltage, or add isolated signal conditioning between the source and your board . See Figures 5-7 and 5-8.



System with a Large Common Mode Voltage, Connected to a Differential Input

Figure 5-7. Common Mode Voltage Greater Than +/-10V, Differential Input

.



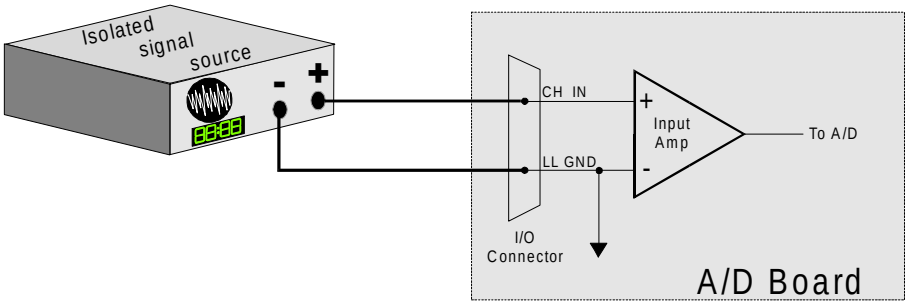
System with a Large Common Mode Voltage, Connected to a Single-Ended Input

Figure 5-8. Common Mode Voltage Greater Than +/-10V, Single-Ended Input w/Isolation Barrier

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5.3.6 Isolated Grounds / Single-Ended Inputs

Single-ended inputs can be used to monitor isolated inputs, though the use of the differential mode will increase you system's noise immunity. The diagram below shows the recommended connections is this configuration.

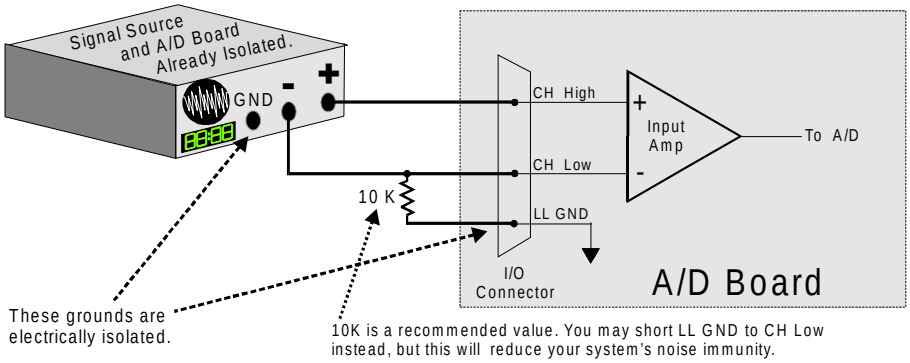


Isolated Signal Source
Connected to a Single-Ended Input

Figure 5-9. Isolated Ground - Single-Ended input

5.3.7 Isolated Grounds / Differential Inputs

Optimum performance with isolated signal sources is assured with the use of the differential input setting. The diagram below shows the recommend connections is this configuration.



Already isolated signal source
and A/D board connected to
a differential input.

Figure 5-10. Isolated Grounds - Differential Input

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6 REGISTER ARCHITECTURE

6.1 INTRODUCTION

There are three ways to generate software for CIO-DAS1400 series boards. These are:
Writing custom software using our Universal Library package.
Using a fully integrated software package (e.g. SoftWire).
Doing direct register-level programming.

CUSTOM SOFTWARE UTILIZING THE UNIVERSAL LIBRARY
Most customers write custom software using Measurement Computing's Universal Library. The Universal Library takes care of all the board I/O commands and lets you concentrate on the application part of the software. For additional information regarding using the Universal Library, please refer to the documentation supplied with the Universal Library

FULLY INTEGRATED SOFTWARE PACKAGES (e.g. SoftWire)
Many customers also take advantage of the power and simplicity offered by one of the high-level data acquisition packages. Please refer to the package's documentation for setup and usage details.

DIRECT REGISTER-LEVEL PROGRAMMING
Though uncommon, some applications may not allow the use of our Universal Library and a high-level package may not be available. For this case, a detailed register mapping for experienced programmers follows.

6.2 CONTROL & DATA REGISTERS

The CIO-DAS1400 is controlled and monitored by reading and writing 24 I/O addresses. The first address is referred to as the BASE ADDRESS (BADR) and is set by a bank of switches on the board. All other addresses are located at the BASE ADDRESS plus a specified offset. In particular, the main analog I/O functions are controlled by the I/O addressees from BADR to BADR +F hex and BADR +404 hex through BADR +407 hex. Although registers are easy to read and write to, unless there is a specific reason to write your program at the register lever, we highly recommend you use our Universal Library.

The method of programming required to set/read bits from bytes is beyond the scope of this manual. The remainder of this chapter is included for those experienced programmers who wish to write their own registe level programs.

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The registers and their functions are listed in Table 6-1. Each register has eight bits for either a byte of data or individual bit functions.

Table 6-1. Register Addresses and Functions

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D Data (Least significant four bits)	Start A/D Conversion
BASE + 1	A/D Data (Most significant byte)	None
BASE + 2	Channel MUX	Channel MUX / FIFO reset
BASE + 3	Digital 4-Bit Input	Digital 4-Bit Output
BASE + 4	None	None
BASE + 5	None	None
BASE + 6	None	None
BASE + 7	None	None
BASE + 8	Status EOC, UNI/BIP etc.	Clear Interrupt
BASE + 9	DMA, Interrupt & Trigger Control	Set DMA, INT etc
BASE + Ah	none	Burst Length/pacer clk cntrl
BASE + Bh	PGA gain	PGA Control/DT reset
BASE + Ch	Counter 0 Data	Counter 0 Data
BASE + Dh	CTR 1 Data - A/D Pacer Clock	CTR 1 Data - A/D Pacer
BASE + Eh	CTR 2 Data - A/D Pacer Clock	CTR 2 Data - A/D Pacer
BASE + Fh	None. No read back on 8254	Pacer Clock Control (8254)
BASE + 400h	None	None
BASE + 401h	None	None
BASE + 402h	None	None
BASE + 403h	None	None
BASE + 404h	None	Conversion Enable/Disable
BASE + 405h	None	Burst Mode Enable/Disable
BASE + 406h	None	DAS 1400 Enable/Disable
BASE + 407h	Status of extended features	None

6.2.1 A/D Data & Channel Registers (CIO-DAS140#/12

Base Address +0

7	6	5	4	3	2	1	0
A/D 3	A/D 2	A/D 1	A/D 0 LSB	CH3	CH2	CH1	CH0

This register is read/write.

READ
On read, it contains two types of data. The least significant four digits of the analog input data and the channel number from which the current data was taken.

These four bits of analog input data must be combined with the eight bits of analog input data in BASE + 1, forming a complete 12-bit number. The data is in the format 0 = minus full scale. 4095 = +FS.

The channel number is binary. If the current channel were five, then bits CH2 and CH0 would be high, CH3 and CH1 would be low.

WRITE
Writing any data to the register causes an immediate A/D conversion.

BASE ADDRESS +1

7	6	5	4	3	2	1	0
A/D 11	A/D 10	A/D 9	A/D 8	A/D 7	A/D 6	A/D 5	A/D 4

MSB
This register is read-only.

On read, the most significant A/D byte is read.

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6.2.2 A/D Data & Channel Registers (CIO-DAS1402/16)

BASE ADDRESS

7	6	5	4	3	2	1	0
A/D 7	A/D 6	A/D 5	A/D 4	A/D 3	A/D 2	A/D 1	A/D 0 LSB

This register is read/write.

READ
On read, it contains the least significant eight digits of the analog input data.

These eight bits of analog input data are combined with the eight bits of analog input data in BASE + 1, forming a complete 16-bit number. The data is in the format 0 = minus full scale. 65,535 = +FS.

WRITE
Writing any data to the register causes an immediate A/D conversion.

BASE ADDRESS +1

7	6	5	4	3	2	1	0
A/D 15 MSB	A/D 14	A/D 13	A/D 12	A/D 11	A/D 10	A/D 9	A/D 8

This register is read-only. On read, the most significant A/D byte is read.

6.2.3 Channel MUX Scan Limits Register

BASE ADDRESS +2

7	6	5	4	3	2	1	0
CH H3	CH H2	CH H1	CH H0	CH L3	CH L2	CH L1	CH L0

This register is read and write.

READ
The current channel scan limits are read as one byte. The high channel number scan limit is in the most significant four bits. The low channel scan limit is in the least significant four bits.

WRITE
The channel scan limits desired are written as one byte. The high channel number scan limit is in the most significant four bits. The low channel scan limit is in the least significant four bits.

NOTE
Every write to this register sets the current A/D channel MUX setting to the number in bits 0-3 and resets the FIFO. See BASE + 8.

6.2.4 Four-Bit Digital I/O Registers

BASE ADDRESS +3 (when read)

7	6	5	4	3	2	1	0
1	1	0	0	DI3	DI2, CTR0 GATE	DI1	DI0, TRIG

READ
The signals present at the inputs are read as one byte, the most significant four bits of which are always zero. Pins 25 (digital input 0) and 24 (digital input 2) digital inputs have two functions each.

The TRIG function of digital input 0 may be used to hold off the first sample of an A/D set by holding it low (0V) until you are ready to take samples, which are then paced by the 8254. It can also be used as the source of an external start conversion pulse, synchronizing A/D conversions to some external event.

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BASE ADDRESS +3 (when written to)

7	6	5	4	3	2	1	0
X	X	X	X	DO3	DO2	DO1	DO0

WRITE
The upper four bits are ignored. The lower four bits are latched TTL outputs. Once written, the state of the inputs cannot be read back because a read back would read the separate digital input lines (see above).

NOTE
Since the digital inputs have multiple functions, use the digital input lines 0-3 with care when you are also using the A/D converter.

The digital outputs are also used by the CIO-EXP32, 32-channel analog multiplexer/amplifier.

6.2.5 Status Registers

BASE ADDRESS + 8

7	6	5	4	3	2	1	0
EOC	U/B	MUX	INT	CH3	CH2	CH1	CH0

This register is read-mostly, one-function-write.

READ

EOC = 1, the A/D converter is busy. EOC = 0, it is free.

U/B = 1, the amplifier is in Unipolar mode. U/B = 0, is bipolar.

MUX = 1, Channels are configured 16, single-ended. MUX = 0, 8 differential.

INT = 1, an interrupt has been received. INT = 0, ready to receive an interrupt. An interrupt service routine must clear this bit after each interrupt.

CH3, CH2, CH1 & CH0 are bits in a binary number between 0 and 15 indicating the MUX channel currently selected. It is valid only when EOC = 0. The channel MUX increments shortly after EOC = 1 so may be in a state of transition when EOC = 1.

WRITE
A write of any data to this register sets the INT bit to 0.

6.2.6 DMA, Interrupt & Trigger Control

BASE ADDRESS + 9

7	6	5	4	3	2	1	0
INTE	IR2	IR1	IR0	X	DMA	TS1	TS0

This register is read and write.

READ
INTE = 1, interrupts are enabled. An interrupt generated will be placed on the PC bus interrupt level selected by IR4, IR2, and IR1. INTE = 0, interrupts are disabled.

IR2, IR1, IR0 are bits in a binary number between 0 and 7 which map interrupts onto the PC bus interrupt levels 2 - 7. Interrupts 0 and 1 can not be asserted by the CIO-DAS1400.

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Table 6-2. Interrupt Coding

IR2	IR1	IR0	INTERRUPT LEVEL
0	0	0	None
0	0	1	None
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

DMA = 1, DMA transfers are enabled.
DMA = 0, DMA transfers are disabled.
Note that this bit only allows the CIO-DAS1400 to assert a DMA request to the PC on the DMA request level selected by the DMA switch on the CIO-DAS1400. Before this bit is set to 1, the PC's 8237 (or appropriate) DMA controller chip must be set up.

TS1 & TS0 control the source of the A/D start conversion trigger according to table 6-3 below.

Table 6-3. Trigger Source TS0 and TS1 Control Codes

TS1	TS0	
0	X	Software triggered A/D only
1	0	Start on rising edge (Digital input 0, Pin 25)
1	1	Start on Pacer Clock Pulse (CTR 2 OUT, no external access)

6.2.7 Pacer Clock Control Register

BASE ADDRESS + A hex

7	6	5	4	3	2	1	0
BL3	BL2	BL1	BL0	X	X	CTR0	TRIG0

This register is write-only.

BL3 - BL0 = BURST LENGTH. Nibble determines number of conversions per trigger when in burst mode. One to sixteen samples (single ended) or eight samples (differential) in a burst. When the CIO-DAS1400 is not in burst mode these bits have no function.

CTR0 = 1. When CTR0 = 1, an onboard 100KHz clock signal is ANDed with the COUNTER 0 CLOCK INPUT (pin 21). A high on pin 21 will allow pulses from the onboard source into the 8254 Counter 0 input. (This input has a pull-up resistor on it, so no connection is necessary to use the onboard clock as a pacer clock.

CTR0 = 0. When CTR0 = 0, the input to 8254 Counter 0 is entirely dependent on pulses at pin 21, COUNTER 0 CLOCK INPUT.

TRIG0 = 1. When TRIG0 = 1 external gating of the pacer clock at pin 25 is enabled. Pin 25 going high will start A/D conversions. The input at pin 25 is connected to a pull-up resistor and will remain high unless pulled low externally.

TRIG0 = 0. When TRIG0 = 0, the gating of the pacer clock at pin 25 is disabled. The gates of counter 1 & 2 are held high, preventing external control of the pacer gate.

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Figure 6-1 may help you understand these registers.

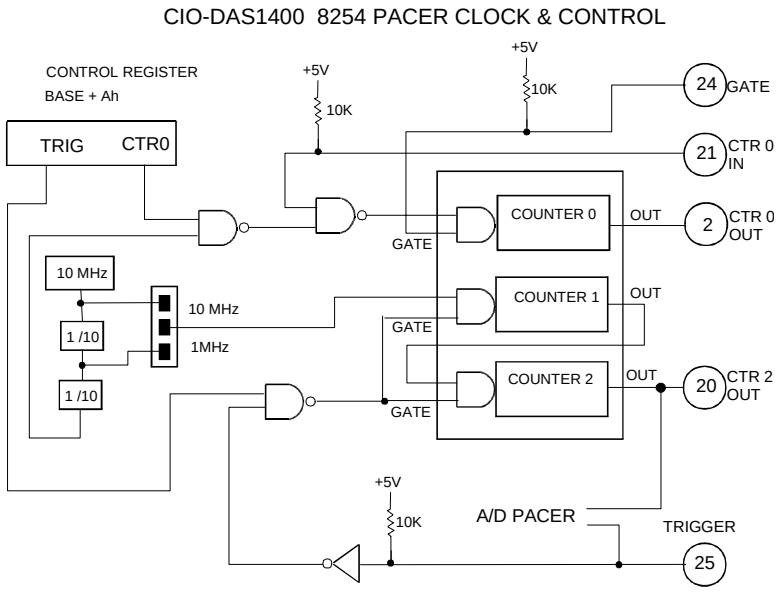


Figure 6-1. Pacer and Counter Block Diagram

6.2.8 Programmable Gain Control Register / Burst Rate

BASE ADDRESS + B hex

7	6	5	4	3	2	1	0
X	X	X	X	X	X	G1	G0

BURST RATE is fixed at: CIO-DAS1400/12 = 4ms (250 kHz) between burst samples. CIO-DAS1402/16 = 13.3ms (~75 kHz) between burst samples.

The MetraByte DAS-1600 manual lists this register as containing the control bits of a settable burst rate. Although the bits are described in detail, no amount of writing to them will cause a change in the burst rate. The MetraByte catalog lists the burst rate as fixed at 10ms and we found this to be consistent with the board's operation. The MetraByte manual appears to be in error.

Given the nature and purpose of burst mode, a rate fixed at the maximum possible is the best choice.

PROGRAMMABLE GAIN CONTROL: Range and gain is controlled by bits G1 and G0. The codes have different meaning for each board in the DAS1400 family.

Table 6-4. Range Control Codes

BOARD	CODE	BIPOLAR RANGE	UNIPOLAR RANGE
CIO-DAS1401/12	0	+/-10V	0-10V
	1	+/-1V	0-1V
	2	+/-0.1V	0-0.1V
	3	+/-0.01V	0-0.01V
CIO-DAS1402/12 and CIO-DAS1402/16	0	+/-10V	0-10V
	1	+/-5V	0-5V
	2	+/-2.5V	0-2.5V
	3	+/-1.25V	0-1.25V

The range, unipolar or bipolar is controlled by a switch. If your application is served better by programmable ranges, please consider the CIO-DAS16/Jr or CIO-DAS16/330 boards.

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6.2.9 Pacer Clock Data & Control Registers

8254 COUNTER 0 DATA
BASE ADDRESS +C hex

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 1 DATA
BASE ADDRESS +D hex

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 2 DATA
BASE ADDRESS +E hex

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

The three 8254 counter/timer data registers are read/write. Because each counter can count as high as 64,535, it is clear that loading or reading the counter data is a multi-step process. The operation of the 8254 is explained in Intel's 8254 data sheet.

8254 COUNTER CONTROL
BASE ADDRESS +F hex

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

This register controls the operation and loading/reading of the counters. The configuration of the 8254 codes which control the 8254 chip is explained in the Intel 8254 data sheet.

6.2.10 Convert Disable Register

BASE ADDRESS +404 hex

7	6	5	4	3	2	1	0
T	T	T	T	T	T	T	T

WRITE ONLY. Writing a 0 to this register enables triggering of the A/D converter if the DAS1400 mode is enabled. On power-up or reset this register is reset to conversion triggers enabled. Writing a 40 hex to this register disables A/D conversions.

6.2.11 Burst Mode Enable Register

BASE ADDRESS +405 hex

7	6	5	4	3	2	1	0
B	B	B	B	B	B	B	B

WRITE ONLY. Burst mode enable. Writing 40 hex to this register enables the burst trigger. Writing 0 to this register disables burst trigger. On power-up or reset the burst trigger is disabled.

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6.2.12 DAS1400 Mode Enable Register

BASE ADDRESS +406 hex

7	6	5	4	3	2	1	0
M	M	M	M	M	M	M	M

WRITE ONLY. DAS1400 mode enable. Writing 40 hex to this register enables the DAS1400 functions. Writing 0 to this register disables DAS1400 functions. On power-up or reset the DAS1400 functions are disabled.

6.2.13 Burst Status Register

BASE ADDRESS + 407 hex

7	6	5	4	3	2	1	0
0	BME	ME	CD	0	0	WS	CLK

READ ONLY. This register provides status on:

a. The Clock Select switch and Wait State switch.
b. The DAS1400 enable, Conversion Disable and Burst Mode Enable bits.

The register defaults to 000100XX on power-up or reset, which corresponds to the programmable bit default settings plus the state of the switches. The bit assignments are as follows.

BME 1 = Burst Mode Enabled, 0 = disabled.
ME 1 = DAS1400 Mode Enabled, 0 = disabled.
CD 1 = Conversions allowed, 0 = conversions disabled.
WS 1 = Wait State Enabled, 0 = No wait state.
CLK 1 = 10 MHz clock selected, 0 = 1 MHz clock selected.

7 CALIBRATION AND TEST

Every board is fully tested and calibrated before shipment. For normal environments, a calibration interval of six months to one year is recommended. If frequent variations in temperature or humidity are common, recalibrate at least every three months. It takes less than 20 minutes to calibrate the CIO-DAS1400 series board.

7.1 REQUIRED EQUIPMENT

Ideally, you will need a precision voltage source, or a non precision source and a 4½ digit digital voltmeter (5 ½ digit for the CIO-DAS-1402/16), and a few pieces of wire.

You do not need an extender card to calibrate the board but you do need to remove the cover from your computer so trim pots can be adjusted during calibration.
NOTE: Use the plastic screwdriver supplied with your board for adjusting the trim pots, so that if the screwdriver is dropped into the PC, it won't cause a short circuit.

7.2 CALIBRATING THE A/D CONVERTERS

The A/D is calibrated by applying a known voltage to an analog input channel and adjusting trim pots for offset and gain. There are three trim pots requiring adjustment to calibrate the analog input section of the board. There are also three pots associated with each of the analog output channels. The entire procedure is described in detail in the InstaCal™, calibration routine.

The board should be calibrated for the range you intend to use it in. When the range is changed, slight variation in Zero and Full Scale may result. These variations can be measured and removed in software if necessary.

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8.1 VOLTAGE DIVIDERS

If you need to measure a signal whos span is greater than the input span of an analog or digital input, use a voltage divider to drop the voltage of the input signal to fall within the range values of the analog or digital input.

A voltage divider takes advantage of Ohm's law, which states,

Voltage = Current * Resistance (V = I * R)

and Kirkoff's voltage law which states,

The sum of the voltage drops around a circuit will be equal to the voltage drop across the entire circuit.

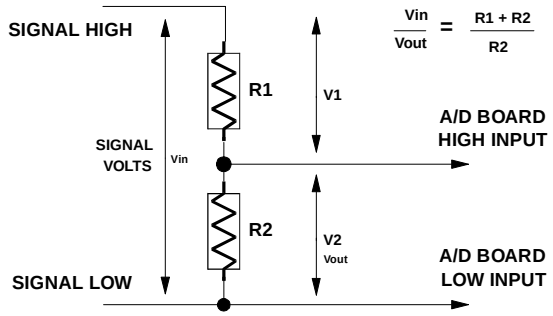
Thus, any variation in the voltage drop for the circuit as a whole will have a proportional variation in all the voltage drops in the circuit.

In a voltage divider, the voltage across one of the resistors in a circuit is proportional to the voltage across the total resistance in the circuit.

The object in using a voltage divider is to choose two resistors with the proper proportions relative to the full scale of the analog or digital input and the maximum signal voltage.

The action of dropping the voltage proportionally is often called attenuation. The formula for attenuation is:

SIMPLE VOLTAGE DIVIDER



$$\text{Attenuation} = \frac{R1 + R2}{R2}$$

The variable Attenuation is the proportional difference between the signal voltage max and the full scale of the analog input.

$$2 = \frac{10K + 10K}{10K}$$

For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the attenuation is 2:1 or just 2.

$$R1 = (A-1) * R2$$

For a given attenuation, pick a suitable resistor and call it R2, the use this formula to calculate R1.

Digital inputs often require the use of voltage dividers. For example, suppose you wish to measure a digital signal that is at 0 volts when OFF and 24 volts when ON. You cannot connect such a high voltage directly to the CIO-AD digital inputs. The voltage must be dropped to 5 volts maximum when ON. The attenuation must be 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 10K. Remember that a TTL input is 'ON' when the input voltage is greater than 2.5 volts.

$$R1 = (4.8- 1) * 10K$$
$$R1 = 38 \text{ Kohms}$$
$$4.8 = \frac{38K + 10K}{10K}$$

IMPORTANT NOTE: The resistors, R1 and R2, are going to dissipate all the power in the divider circuit according to the equation Current = Voltage / Resistance, and Power = Current squared * Resistance ($W = I^2R$). The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit.

For attenuation of 5:1 or less, no resistor should be less than 10K.

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For attenuation greater than 5:1, no resistor should be less than 1K.

The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. The CIO-TERMINAL is a 16" by 4" screw terminal board with two 37 pin D type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you may complete with the proper value components for your application.

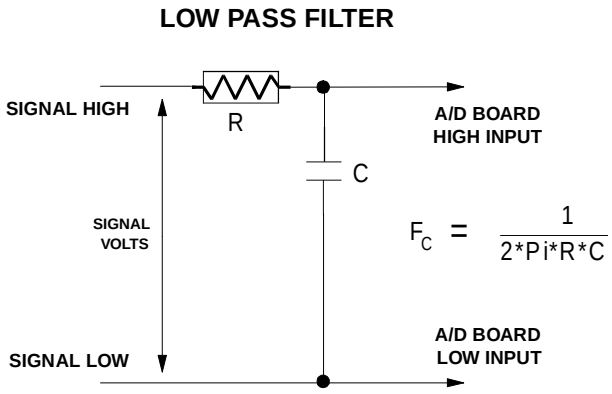
8.2 LOW-PASS FILTERS

A low-pass filter is placed on the signal wires between a signal and an A/D board. It attenuates frequencies greater than the cut-off frequency, preventing them from entering the A/D board's analog or digital inputs.

The key term in a low-pass filter circuit is cut-off frequency. The cut-off frequency is that frequency above which no variation of voltage with respect to time can enter the board's input circuit. For example, if a low-pass filter had a cut off frequency of 30 Hz, the kind of interference associated with line voltage (60 Hz) would be filtered out but a signal of 25 Hz would pass.

In a digital circuit, a low-pass filter can be used to filter an input from pushing a momentary contact switch.

A low-pass filter may be constructed from one resistor (R) and one capacitor (C). The cut-off frequency is determined by the formula:



$$Fc = \frac{1}{2 * p * R * C}$$

$$R = \frac{1}{2 * p * C * Fc}$$

Where: p = 3.14...
R is Ohms
C is Farads
Fc is Hz (cycles per second)

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9.1 CIO-DAS1401/12 and CIO-DAS1402/12

Analog Input Section

A/D converter type	ADS7800 successive-approximation
Resolution	12 bits (1 in 4096)
Programmable ranges	
CIO-DAS1401/12	±10V, ±1V, ±0.1V, ±0.01V, 0 to 10V, 0 to 1V, 0 to 0.1V, 0 to 0.01V
CIO-DAS1402/12	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D pacing	Programmable: external source (Din0, positive edge) or internal counter (positive or negative edge, jumper selectable) or software polled
Burstmode	4 µs
Data transfer	From 512 sample FIFO via interrupt, DMA or software-polled
Polarity	Unipolar/Bipolar, switch-selectable
Number of channels	8 differential or 16 single-ended, switch-selectable
Interrupts	2 to 7
Interrupt enable	Programmable
Interrupt sources	End-of-conversion, terminal count (DMA)
DMA	Channel 1 or 3
Trigger sources	External hardware/software (DIn0)
A/D conversion time	3.3 µs
Throughput	160 kHz
Differential Linearity error	±1 LSB
Integral Linearity error	±1 LSB
No missing codes guaranteed	12 bits
Gain drift (A/D specs)	±30 ppm/°C
Zero drift (A/D specs)	±10 ppm/°C
Input leakage current	250 nA max
Input impedance	10 MegOhms min
Absolute maximum input voltage	±35V

Digital Input / Output

Digital Type	
Output	74LS197
Input	74LS244
Configuration	4 fixed inputs, 4 fixed outputs
Number of channels	8
Output High	2.7 volts min @ -0.4mA
Output Low	0.5 volts max @ 8mA
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min

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Counter Section

Counter type 82C54

Configuration 3 down-counters, 16 bits each

Counter 0 - Independent, user configurable

Source: Programmable - Internal 100kHz or external (CTR0 Clock In)

Gate: External (DIn2)

Output: Available at user connector (CTR0 Out)

Counter 1 - ADC Pacer Lower Divider

Source: 1 or 10 MHz oscillator (jumper selectable)

Gate: Tied to Counter 2 gate, programmable source.

Output: Chained to Counter 2 Clock.

Counter 2 - ADC Pacer Upper Divider

Source: Counter 1 Output.

Gate: Tied to Counter 1 gate, programmable source.

Output: ADC Pacer clock, hard-wired to user connector, Ctr2 out

Clock input frequency	10 Mhz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	-20 to 70°C
Humidity	0 to 90% non-condensing

Power Consumption

+5 1.4A typical, 2.1A max

9.2 CIO-DAS1402/16

Analog Input Section

A/D converter type	ADS7805 successive approximation
Resolution	16 bits (1 in 65,536)
Programmable ranges	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D pacing	Programmable: external source (Din0, positive edge) or internal counter (positive or negative edge, jumper-selectable) or software-polled
Burstmode	13.3µs
Data transfer	From 512 sample FIFO via interrupt, DMA, or software-polled
Polarity	Unipolar/Bipolar, switch-selectable
Number of channels	8 differential or 16 single-ended, switch-selectable
Interrupts	2 to 7
Interrupt enable	Programmable
Interrupt sources	End-of-conversion, terminal count (DMA)
DMA	Channel 1 or 3
Trigger sources	External hardware/software (DIn0)
A/D conversion time	10 µs
Throughput	100 kHz
Absolute Accuracy	Adjustable to ±0.0015% of FS
Differential Linearity error (Bipolar)	±1 LSB

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Integral Linearity error (Bipolar)	±1.5 LSB
No missing codes guaranteed	16 bits
Gain drift (A/D specs)	±7 ppm/°C
Zero drift (A/D specs)	±2 ppm/°C
Input leakage current	250 nA max
Input impedance	10 MegOhms min
Absolute maximum input voltage	±35V

Digital Input / Output

Digital Type	
Output	74LS197
Input	74LS244
Configuration	4 fixed input, 4 fixed output
Number of channels	8
Output High	2.7 volts @ -0.4 mA min
Output Low	0.5 volts @ 8 mA max
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min

Counter Section

Counter type 82C54

Configuration 3 down counters, 16 bits each

Counter 0 - Independent, user configurable
- Source: Programmable - Internal 100 kHz or external (CTR0 Clock In)
- Gate: External (DIn2)
- Output: Available at user connector (CTR0 Out)

Counter 1 - ADC Pacer Lower Divider
- Source: 1 or 10 MHz oscillator (jumper-selectable)
- Gate: Tied to Counter 2 gate, programmable source.
- Output: Chained to Counter 2 Clock.

Counter 2 - ADC Pacer Upper Divider
- Source: Counter 1 Output.
- Gate: Tied to Counter 1 gate, programmable source.
- Output: ADC Pacer clock, hard-wired to user connector, Ctr2 out.

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	-20 to 70°C
Humidity	0 to 90% non-condensing

Power Consumption

+5V	1.4A typical, 2.1A max

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EC Declaration of Conformity

We, Measurement Computing Corp., declare under sole responsibility that the product:

Part Number	Description
CIO-DAS1400 series	ISA Bus, analog and digital I/O boards

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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