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Find the *Measurement Computing CIO-DAS1402/16* at our website: *Click HERE*

SPECIFICATIONS

CIO-DAS1401/12
CIO-DAS1402/12
CIO-DAS1402/16

Analog Input & Digital I/O



Revision 7, November, 2000

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CIO-DAS1401/12 and CIO-DAS1402/12

Analog Input Section

A/D converter type	ADS7800 successive-approximation
Resolution	12 bits (1 in 4096)
Programmable ranges	
CIO-DAS1401/12	±10V, ±1V, ±0.1V, ±0.01V, 0 to 10V, 0 to 1V, 0 to 0.1V, 0 to 0.01V
CIO-DAS1402/12	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D pacing	Programmable: external source (Din0, positive edge) or internal counter (positive or negative edge, jumper selectable) or software polled
Burstmode	4 µs
Data transfer	From 512 sample FIFO via interrupt, DMA or software-polled
Polarity	Unipolar/Bipolar, switch-selectable
Number of channels	8 differential or 16 single-ended, switch-selectable
Interrupts	2 to 7
Interrupt enable	Programmable
Interrupt sources	End-of-conversion, terminal count (DMA)
DMA	Channel 1 or 3
Trigger sources	External hardware/software (DIn0)
A/D conversion time	3.3 µs
Throughput	160 kHz
Differential Linearity error	±1 LSB
Integral Linearity error	±1 LSB
No missing codes guaranteed	12 bits
Gain drift (A/D specs)	±30 ppm/°C
Zero drift (A/D specs)	±10 ppm/°C
Input leakage current	250 nA max
Input impedance	10 MegOhms min
Absolute maximum input voltage	±35V

Digital Input / Output

Digital Type	
Output	74LS197
Input	74LS244
Configuration	4 fixed inputs, 4 fixed outputs
Number of channels	8
Output High	2.7 volts min @ -0.4mA
Output Low	0.5 volts max @ 8mA
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min

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Counter Section

Counter type	82C54
Configuration	3 down-counters, 16 bits each

Counter 0 - Independent, user configurable

Source:	Programmable - Internal 100kHz or external (CTR0 Clock In)
Gate:	External (DIn2)
Output:	Available at user connector (CTR0 Out)

Counter 1 - ADC Pacer Lower Divider

Source:	1 or 10 MHz oscillator (jumper selectable)
Gate:	Tied to Counter 2 gate, programmable source.
Output: Chained to Counter 2 Clock.	

Counter 2 - ADC Pacer Upper Divider

Source:	Counter 1 Output.
Gate:	Tied to Counter 1 gate, programmable source.
Output:	ADC Pacer clock, hard-wired to user connector, Ctr2 out

Clock input frequency	10 Mhz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	-20 to 70°C
Humidity	0 to 90% non-condensing

Power Consumption

+5 1.4A typical, 2.1A max

CIO-DAS1402/16

Analog Input Section

A/D converter type	ADS7805 successive approximation
Resolution	16 bits (1 in 65,536)
Programmable ranges	±10V, ±5V, ±2.5V, ±1.25V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V
A/D pacing	Programmable: external source (Din0, positive edge) or internal counter (positive or negative edge, jumper-selectable) or software-polled
Burstmode	13.3 µs
Data transfer	From 512 sample FIFO via interrupt, DMA, or software-polled
Polarity	Unipolar/Bipolar, switch-selectable

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Number of channels	8 differential or 16 single-ended, switch-selectable
Interrupts	2 to 7
Interrupt enable	Programmable
Interrupt sources	End-of-conversion, terminal count (DMA)
DMA	Channel 1 or 3
Trigger sources	External hardware/software (DIn0)
A/D conversion time	10 µs
Throughput	100 kHz
Absolute Accuracy	Adjustable to ±0.0015% of FS
Differential Linearity error (Bipolar)	±1 LSB
Integral Linearity error (Bipolar)	±1.5 LSB
No missing codes guaranteed	16 bits
Gain drift (A/D specs)	±7 ppm/°C
Zero drift (A/D specs)	±2 ppm/°C
Input leakage current	250 nA max
Input impedance	10 MegOhms min
Absolute maximum input voltage	±35V

Digital Input / Output

Digital Type	
Output	74LS197
Input	74LS244
Configuration	4 fixed input, 4 fixed output
Number of channels	8
Output High	2.7 volts @ -0.4 mA min
Output Low	0.5 volts @ 8 mA max
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, -0.5 volts absolute min

Counter Section

Counter type	82C54
Configuration	3 down counters, 16 bits each
Counter 0 - Independent, user configurable	
Source:	Programmable - Internal 100 kHz or external (CTR0 Clock In)
Gate:	External (DIn2)
Output:	Available at user connector (CTR0 Out)
Counter 1 - ADC Pacer Lower Divider	
Source:	1 or 10 MHz oscillator (jumper-selectable)
Gate:	Tied to Counter 2 gate, programmable source.
Output:	Chained to Counter 2 Clock.
Counter 2 - ADC Pacer Upper Divider	
Source:	Counter 1 Output.
Gate:	Tied to Counter 1 gate, programmable source.
Output:	ADC Pacer clock, hard-wired to user connector, Ctr2 out.
Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min

Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Power Consumption

+5V	1.4A typical, 2.1A max

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	-20 to 70°C
Humidity	0 to 90% non-condensing

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