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FRONT PANEL DATA PORT PMC MODULE

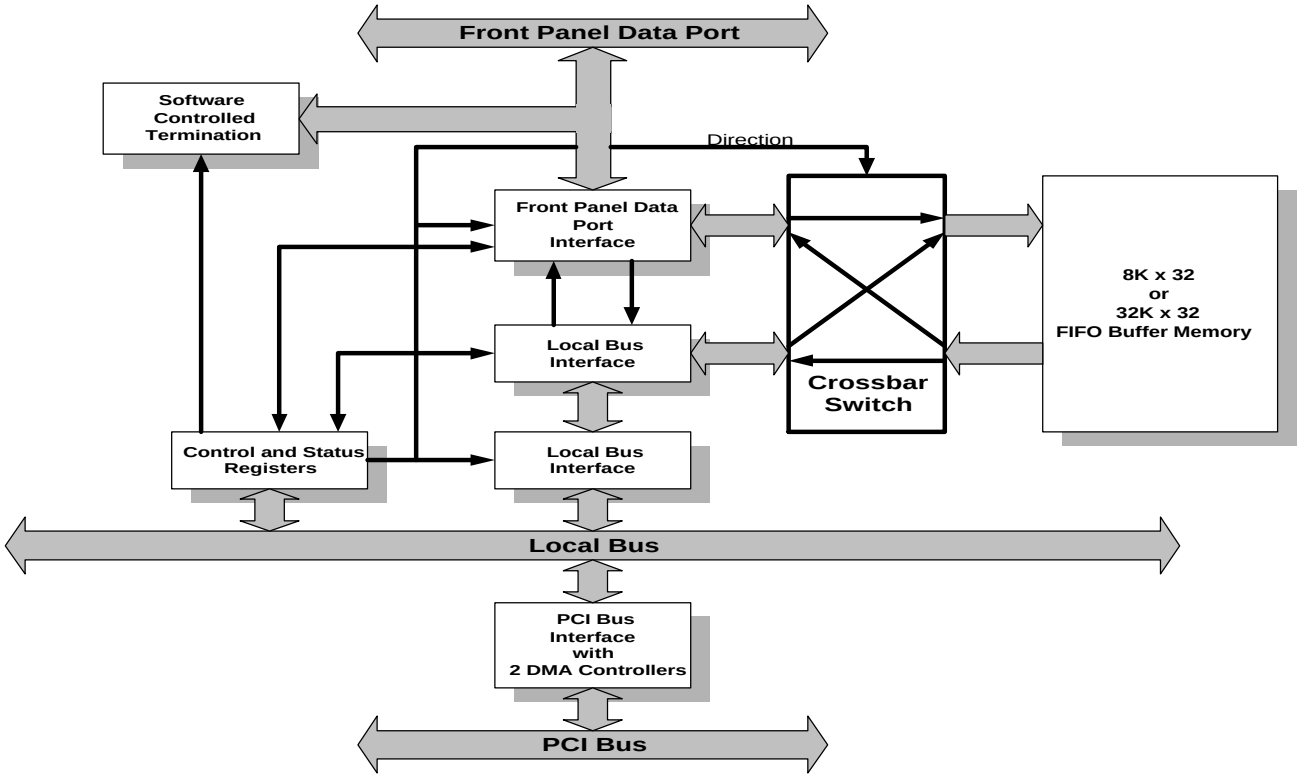
FPDP-PMC



FEATURES

* SINGLE WIDE PCI MEZZANINE CARD (PMC)
* FULLY FRONT PANEL DATA PORT INDUSTRY STANDARD COMPLIANT (FPDP) ANSI/VITA 17-1998
* PCI BUS REVISION 2.1 COMPLIANT
* MAX DATA RATE SUPPORTED: UP TO 160 MBYTES/SEC PECL, UP TO 80 MBYTES/SEC TTL
* TRANSMIT MASTER, RECEIVER MASTER OR RECEIVER MODE SOFTWARE SWITCHABLE "ON THE FLY"
* SUPPORTS ALL FOUR FPDP OPERATING MODES
* FLEXIBLE PCI INTERRUPTS TO SUPPORT "REAL TIME" OPERATION
* TWO DIRECT MEMORY ACCESS CONTROLLERS THAT SUPPORT DMA CHAINING FROM PCI MEMORY
* 3.3V OR 5V PCI OPERATION
* 8K x 32 or 32K x 32 FIFO MEMORY BUFFER DEPTH FACTORY CONFIGURED
* SOLARIS, VxWORKS, AND WINDOWS NT DRIVER SUPPORT

FPDP-PMC MODULE BLOCK DIAGRAM



ECHOTEK CORPORATION **555 SPARKMAN DRIVE #400** **HUNTSVILLE, AL 35816**
PHONE 256 721 1911 **FAX 256 721 9266** **E-MAIL: sales@echotek.com**

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FPDP-PMC MODULE

Overview

The Echotek Corporation FPDP-PMC is a single wide PCI Mezzanine Card which provides a high speed bidirectional parallel digital interface from the PCI Bus to the Front Panel Data Port (FPDP). The FPDP is a 32-data-bit-wide, 80 conductor bus with TTL control, data and clock, and one PECL clock. The TTL clock can operate the interface at data rates up to 80MBytes/Sec. (20 MHz). The PECL clock can operate the interface at data rates up to 160MBytes/Sec. (40 MHz). The PCI Bus Interface uses the PLX PCI9080 PCI interface chip, which has two Direct Memory Access Controllers that can be chained, using PCI memory. The Echotek Corporation FPDP-PMC was designed to ANSI/VITA 17-1998. The FPDP-PMC can be software configured and switched "on the fly" to be either a Transmitter Master, Receiver Master, or a Receiver.

FPDP Interface

The FPDP Interface uses the standard TTL Termination which can be enabled and disabled via software control. There are also three PECL Clock Termination schemes supplied; a custom termination which can be software controlled, and two standard terminations that are DIP switch controlled.

FPDP Modes of Operation

Besides the Transmitter Master, Receiver Master, and Receiver configurations, there are four modes of operation that apply to these configurations which are presented in the FPDP specification, and are supported by the Echotek FPDP-PMC: Un-Framed Data, Single Frame Data, Fixed Size Repeating Frame Data, and Dynamic Size Repeating Frame Data. The Dynamic Size Frame data mode is controlled by a small buffer which stores the frame size detected when the FPDP-PMC is a Receiver, or is used to generate a sync when the FPDP-PMC is a Transmitter Master. This allows software to monitor or control the frame size.

Programmable I/O Control

The (TTL) PIO1 and PIO2 signals of the FPDP are user definable. The Echotek FPDP-PMC permits the User to software control the direction and state of each independently.

PCI Interrupt Support

The Echotek FPDP-PMC implements a flexible Interrupt scheme for the implementation of "RealTime" data transfers. Buffer FIFO Flags such as Empty, Full, Almost Full, and Not Empty exist, as well as Frame Complete, Data Valid Complete, and Data Valid Active are available as Interrupt sources which are particularly suited for "RealTime" data transfer as well as the Programmable Count Interrupt. This source will cause a PCI interrupt when the number of samples input (Receiver or Receiver Master), or output (Transmit Master) is equal to the programmed count. This feature also allows the data throughput to be tuned to the system. To keep up with DMA transfers, an interrupt for each DMA Controller is also provided.

FPDP Buffer FIFO Memory

The FPDP-PMC uses a First In First Out (FIFO) Buffer to store input or output data. This memory can be factory configured to be 8Kx32 or 32Kx32. The design employs a unidirectional FIFO which is interfaced by a Crossbar switch. The Crossbar switch selects the FIFO Buffer to be an input or output, depending upon the configuration specified: transmitter or receiver.

PCI Interface

The PCI Interface is implemented via the PLX PCI9080 Interface chip, which provides two Direct Memory Access Controllers (DMACs). These DMACs can be chained, but only using PCI memory, as the FPDP-PMC has no Random Access Memory.

Support Software

The simple user interface driver supports Unframed Data, Single Frame Data, Fixed Size Repeating Frame Data, and Dynamic Size Repeating Frame Data. The mode and direction of data may only be changed by software control at the termination of the current frame. Data transfer can be controlled by interrupts or by polling and typical interrupts are DMA Done (Channel 0 or 1), PCI status, or Mailbox. Software is provided for PCI burst mode operation, direct driver programmability, and support is provided for the two programmable I/O lines. Drivers and test software are available for VxWorks, Solaris, and NT.

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Ordering Information

Model	Part Number	Ruggedization	Options
FPDP-PMC-32K	12-0031C/CC299	Commercial	32K FIFO's
FPDP-PMC-8K	12-0031C/CC304	Commercial	8K FIFO’s
FPDP-PMC-32K	12-0031C/CC508	Extended Temperature	32K FIFO’s

Ruggedization Levels	Operating Temp (°C)	Storage Temp (°C)	Vibration	Shock	Humidity	Notes
Commercial	0 to +55°C with 300ft./ min. airflow	-50 to +85°C	0.002g2/Hz from 10 to 2000Hz random and 2g sinusidal from 5 to 500 Hz	20g peak sawtooth, 11mS duration	Up to 95% RH	Commercial Grade, cooled by blown air, for use in benign environments and software development applications
Extended Temperature	-20 to +65°C with 300ft./ min. airflow	-50 to +85°C	0.002g2/Hz from 10 to 2000Hz random and 2g sinusidal from 5 to 500 Hz	20g peak sawtooth, 11mS duration	Up to 95% RH with varying temp., 10 cycles, 240 hrs.	Similar to standard but conformally coated and temperature characterized.

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