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PCI-DAS6402/16

Specifications



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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	AD976A, successive approximation ADC
Resolution	16 bits
Number of channels	64 single ended; 32 differential
Input ranges (SW programmable)	Bipolar: ±10 V, ±5 V, ±2.5 V, ±1.25 V Unipolar: 0 to 10 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V
Polarity	Unipolar/Bipolar, software selectable
A/D pacing (SW programmable)	Internal counter – ASIC
	External source (A/D external pacer)
	Software polled
Burst mode	Software selectable option, burst rate = 5 µS. Valid for a fixed input range only.
A/D gate sources	External digital (A/D Pacer Gate)
	External analog (Analog Trigger In)
A/D gating modes	External digital: Programmable, active high or active low, level, or edge
	External analog: Software-configurable for: ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window Trigger levels set by D/A OUT 0 and/or D/A OUT 1.
A/D trigger sources	External digital (A/D start trigger in and A/D stop trigger in)
	External analog (analog trigger in)
A/D triggering modes	External digital: Software-configurable for rising or falling edge.
	External analog: Software-configurable for positive or negative slope. Trigger levels set by D/A OUT 0 and/or D/A OUT 1.
	Pre-/post-trigger: Unlimited number of pre-trigger samples, 16 Meg post-trigger samples. Compatible with both digital and analog trigger options.
Data transfer	From 8k RAM buffer via DMA (demand or non-demand mode) using scatter gather.
	Programmed I/O
Configuration memory	8K words
Channel/gain queue	*Up to 8K elements. Programmable channel, gain, and offset.*
A/D conversion time	5 µS
Calibration	*Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.*

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Accuracy

200 kHz sampling rate, single channel operation and a 60 minute warm-up. Accuracies are listed for operational temperatures within ±2 ºC of internal calibration temperature. Calibrator test source high side tied to Channel 0 High and low side tied to Channel 0 Low. Low-level ground is tied to Channel 0 Low at the user connector.

Table 2. Absolute accuracy

Range	Absolute accuracy
±10.000 V	±3.0 LSB
±5.000 V	±3.0 LSB
±2.500 V	±4.5 LSB
±1.250 V	±4.5 LSB
0 V to +10.000 V	±3.0 LSB
0 V to +5.000 V	±3.0 LSB
0 V to +2.500 V	±4.5 LSB
0 V to +1.250 V	±4.5 LSB

Table 3. Accuracy components

Range	Gain error	Offset error	DLE	ILE
±10.00 V	±1.5 max	±1.5 max	±1.75 max	±2 max
±5.000 V	±1.5 max	±1.5 max	±1.75 max	±2 max
±2.500 V	±2.0 max	±2.5 max	±1.75 max	±2 max
±1.250 V	±2.0 max	±2.5 max	±1.75 max	±2 max
0 to +10.00 V	±1.5 max	±1.5 max	±1.75 max	±2 max
0 to +5.000 V	±1.5 max	±1.5 max	±1.75 max	±2 max
0 to +2.500 V	±1.5 max	±3.0 max	±1.75 max	±2 max
0 to +1.250 V	±1.5 max	±3.0 max	±1.75 max	±2 max

Each PCI-DAS6402/16 is tested at the factory to assure the board's overall error does not exceed accuracy limits described in Table 2 above.

As shown in Table 3, total analog input error is a combination of gain, offset, differential linearity and integral linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case errors are realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction.

System throughput

Table 4. System throughput specifications

Condition	Calibration coefficients	ADC rate (max)
1. Single channel, single input range.	Per specified range	200 kHz
2. Multiple channel, single input range	Per specified range	200 kHz
3. Single channel, multiple input ranges. All samples in unipolar OR bipolar mode.	Default to value for `cbAInScan()` range	200 kHz
4. Multiple channels, multiple input ranges. All samples in unipolar OR bipolar mode.	Default to value for `cbAInScan()` range	200 kHz
5. Multiple channels, multiple input ranges, switching Unipolar/bipolar mode	Default to value for `cbAInScan()` range	200 kHz
6. Multiple channel, single input range, switching Unipolar/bipolar mode.	Default to value for `cbAInScan()` range	200 kHz

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Note 1: For conditions 1-2 above, specified accuracy is maintained at rated throughput. Conditions 3-6 apply calibration coefficients which correspond to the range value selected in `cbAInScan()`. These coefficients remain unchanged throughout the scan. Errors of up to 25 counts may be incurred when switching gains while in bipolar or unipolar mode only (conditions 3 and 4). Errors of up to 100 counts may be incurred when mixing unipolar/bipolar modes (conditions 5 and 6).

Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the maximum rate. A full scale 100 Hz triangle wave is input on Channel 1; Channel 0 is tied to Analog Ground at the 100 pin user connector. The table below summarizes the influence of Channel 1 on Channel 0 with the effects of noise removed. The residue on Channel zero is described in LSBs.

Table 5. Crosstalk specifications

Condition	Crosstalk	Per channel rate	ADC rate
Same range to same range	3 LSB pk-pk	100 kHz	200 kHz
Any range to any range	6 LSB pk-pk	100 kHz	200 kHz

Analog input drift

Table 6. Analog input drift specifications

Analog input full-scale gain drift	0.25 LSB/°C max
Analog input zero drift	0.21 LSB/°C max
Overall analog input drift	0.46 LSB/°C max
Common mode range	±10 V
CMRR @ 60 Hz	-80 dB min
Input impedance	*10 MegOhm min*
Absolute maximum input voltage	▪ *Channel 0: ±15 V, power on or off* ▪ *Channels 1-63: –40 V to +55 V, power on or off*
Warm-up time	60 minutes

Noise performance

Table 7 below summarizes the noise performance for the PCI-DAS6402/16. Noise distribution is determined by gathering 50K samples with inputs tied to ground at the user connector.

Table 7. Board noise performance

Range	Standard Deviation	% within ±2 counts	% within ±1 count	MaxCounts	LSBrms*
±10.00 V	0.8	98%	78%	9	1.4
±5.000 V	0.8	98%	78%	9	1.4
±2.500 V	0.8	98%	78%	9	1.4
±1.250 V	0.9	97%	73%	10	1.5
0 to +10.00 V	0.9	97%	73%	10	1.5
0 to +5.000 V	0.9	97%	73%	10	1.5
0 to +2.500 V	0.9	97%	73%	10	1.5
0 to +1.250 V	1.0	95%	68%	11	1.7

* RMS noise is defined as the peak-to-peak bin spread divided by 6.6.

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Analog output

Table 8. Analog output specifications

A/D converter type	*AD669BR*
Resolution	*16-bits*
Number of Channels	*2*
Voltage ranges	±10 V, ±5 V, 0 to 10 V, 0 to 5 V. Each channel independently programmable.
Monotonicity	*Guaranteed monotonic over temperature*
Analog output full-scale gain drift	±0.55 LSB/°C
Analog output zero drift	10 V ranges: ±0.25 LSB/°C; 5 V ranges: ±0.45 LSB/°C
Overall analog output drift	10 V ranges: ±0.8 LSB/°C; 5 V ranges: ±1.0 LSB/°C
Slew rate	10 V Ranges: 5 V/µs; 5 V ranges: 2.5 V/µs;
Settling time	20 V step to .0008%:13 µs max; 10 V step to .0008%:6 µs typ
Current drive	±15 mA
Output short-circuit duration	*Indefinite @ 25 mA*
Output coupling	*DC*
Output impedance	0.1 ohms
Power up and reset	DACs cleared to 0 volts ±75 mV max

Accuracy

Table 9. Absolute accuracy specifications

Range	Absolute accuracy
±10.000 V	±4.0 LSB
±5.000 V	±4.0 LSB
0 to +10.000 V	±4.0 LSB
0 to +5.000 V	±4.0 LSB

Table 10. Typical accuracy specifications

Range	Typical accuracy
±10.000 V	±3.5 LSB
±5.000 V	±3.5 LSB
0 to +10.00 V	±3.5 LSB
0 to +5.000 V	±3.5 LSB

Accuracy components

Table 11. Accuracy component specifications

Range	Gain error (LSB)	Offset error (LSB)	DLE (LSB)	ILE (LSB)
±10.000 V	±2.0 max, ±1.5 typ	±2.0 max, ±1.0 typ	±1.0 max, ±0.5 typ	±1.0 max, ±0.5 typ
±5.000 V	±2.0 max, ±1.5 typ	±2.0 max, ±1.0 typ	±1.0 max, ±0.5 typ	±1.0 max, ±0.5 typ
0 to +10.00 V	±2.0 max, ±1.5 typ	±2.0 max, ±1.0 typ	±1.0 max, ±0.5 typ	±1.0 max, ±0.5 typ
0 to +5.000 V	±2.0 max, ±1.5 typ	±2.0 max, ±1.0 typ	±1.0 max, ±0.5 typ	±1.0 max, ±0.5 typ

Each PCI-DAS6402/16 is tested at the factory to assure the board's overall error does not exceed ±4.0 LSB.

Total analog output error is a combination of gain, offset, integral linearity, and differential linearity error. The theoretical worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are at their maximum level, and causing error in the same direction. Although an examination of the chart and a summation of the maximum theoretical errors shows that the board could theoretically exhibit a ±6.0 LSB error, our testing assures this error is never realized in a board that we ship.

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Typical accuracy is derived directly from the various component typical errors. This typical, maximum error calculation for the PCI-DAS6402/16 yields ±3.5 LSB. However, this again assumes that each of the errors contributes in the same direction and the ±3.5 LSB specification is quite conservative.

Analog output pacing and triggering

Table 12. Analog output pacing and triggering specifications

D/A pacing (SW programmable)	Internal counter – ASIC
	External source (D/A external pacer)
	Software paced
D/A gate sources (SW programmable)	▪ External digital (external D/A trigger/pacer gate) ▪ External analog (analog trigger in)
D/A gating modes	▪ External digital: Programmable, active high or active low, level or edge ▪ External analog: Software-configurable for above or below reference. Gating levels set by DAC0 or DAC1
D/A trigger sources	External digital (external D/A trigger/pacer gate)
	Software triggered
D/A triggering modes	External digital: Software-configurable for rising or falling edge.
Data transfer	▪ From 16k RAM buffer via DMA (demand or non-demand mode) using scatter gather. ▪ Programmed I/O ▪ Update DACs individually or simultaneously (SW selectable)
Throughput	100 kHz max per channel, 2 channels simultaneous

Digital input/output

Table 13. Digital input/output specifications (main connector)

Digital type (main connector)	Output: 74LS175
	Input: 74LS244
Configuration	4 inputs, 4 outputs (DIN0 through DIN3; DOUT0 to DOUT3)
Output high voltage (IOH = -0.4 mA)	*2.7 V min*
Output low voltage (IOL = 8 mA)	*0.5 V max*
Input high voltage	*2.0 V min, 7 volts absolute max*
Input low voltage	*0.8 V max, –0.5 volts absolute min*

Table 14. Digital input/output specifications (DIO connector)

Digital type (digital I/O connector)	82C55
Number of I/O	24 (FIRSTPORTA Bit 0 through FIRSTPORTC Bit 7)
Configuration	▪ 2 banks of 8 and 2 banks of 4 or ▪ 3 banks of 8 or ▪ 2 banks of 8 with handshake
Input high voltage	*2.0 V min, 5.5 V absolute max*
Input low voltage	*0.8 V max, –0.5 V absolute min*
Output high voltage (IOH = -2.5 mA)	*3.0 V min*
Output low voltage (IOL = 2.5 mA)	*0.4 V max*
Power-up / reset state	Input mode (high impedance)

Table 15. Simultaneous sample and hold specifications

SSH output	TTL-compatible output, HOLD is asserted from start of the conversion for Channel 0 through conversion of the last channel in the scan. Available at user connector (SSH OUT / D/A PACER OUT). This pin is software selectable as SSH OUT or D/A PACER OUT.
SSH polarity	HOLD high (default) or HOLD low, software selectable

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Interrupts

Table 16. Interrupt specifications

Interrupts	PCI INTA# - mapped to IRQn via PCI BIOS at boot-time	
Interrupt enable	Programmable through PLX9080	
ADC interrupt sources (sw programmable)	DAQ_ACTIVE:	Interrupt is generated when a DAQ sequence is active.
	DAQ_STOP:	Interrupt is generated when A/D Stop Trigger In is detected.
	DAQ_DONE:	Interrupt is generated when a DAQ sequence completes.
	DAQ_FIFO_1/4_FULL:	Interrupt is generated when ADC FIFO is ¼ full.
	DAQ_SINGLE:	Interrupt is generated after each conversion completes.
	DAQ_EOSCAN:	Interrupt is generated after the last channel is converted in multi-channel scans.
	DAQ_EOSEQ:	Interrupt is generated after each interval delay during multi-channel scans.
DAC interrupt sources (sw programmable)	DAC_ACTIVE:	Interrupt is generated when DAC waveform circuitry is active.
	DAC_DONE:	Interrupt is generated when a DAC sequence completes.
	DAC_FIFO_1/4_EMPTY:	Interrupt is generated DAC FIFO is ¼ empty.
	DAC_HIGH_CHANNEL:	Interrupt is generated when the DAC high channel output is updated.
	DAC_RETRANSMIT:	Interrupt is generated when the end of a waveform sequence has occurred in retransmit mode.
External interrupt	Interrupt is generated via edge-sensitive transition on the External Interrupt pin. Rising/falling edge polarity software selectable.	

Counters

Table 17. Counter specifications

User counter type	82C54
Configuration	One down counter, 16 bits. Counters 2 and 3 not used.
Counter 1 source	External from connector (CTR1 CLK)
Counter 1 gate	Available at connector (CTR1 GATE).
Counter 1 output	Available at connector (CTR1 OUT).
Clock input frequency	*10 MHz max*
High pulse width (clock input)	*30 nS min*
Low pulse width (clock input)	*50 nS min*
Gate width high	*50 nS min*
Gate width low	*50 nS min*
Input low voltage	*0.8 V max*
Input high voltage	*2.0 V min*
Output low voltage	*0.4 V max*
Output high voltage	*3.0 V min*

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Pacer

Table 18. Pacer specifications

ADC pacer type	ASIC
Configuration	1 down counter, 24 bits (1 scan interval, 1 sample interval)
ADC pacer Source	40 MHz
ADC pacer Gate	Internally controlled by software/hardware trigger.
ADC pacer Out	ADC pacer clock, available at user connector (A/D pacer out)
DAC Pacer type	ASIC
Configuration	1 down counter, 24 bits (1 scan interval, 1 sample interval)
DAC pacer source	40 MHz or 100 kHz internal source. Software selectable
DAC pacer gate	Internally controlled by software/hardware trigger.
DAC pacer out	DAC pacer clock. Available at connector. (SSH OUT / D/A PACER OUT). This pin is software selectable as SSH OUT or D/A PACER OUT.
Internal pacer crystal oscillator	40 MHz
Frequency accuracy	50 ppm

Power consumption

Table 19. Power consumption specifications

+5 V	2.9A typical, 3.3 max

Environmental

Table 20. Environmental specifications

Operating temperature range	0 to 70 °C
Storage temperature range	-40 to 100 °C
Humidity	0 to 95% non-condensing

Mechanical

Table 21. Mechanical specifications

Card dimensions	312 mm (L) x 100.6 mm (W) x 16 mm (H)

Main connector and pin out

Table 22. Main connector specifications

Connector type	100-pin high-density unshielded Robinson Nugent
Compatible cables	C100FF-x cable (x = length in feet)
Compatible accessory products	BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50

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Table 23. 32-channel differential mode pin out

Pin	Signal name	Pin	Signal name
1	LLGND	51	LLGND
2	CH0 HI	52	CH16 HI
3	CH0 LO	53	CH16 LO
4	CH1 HI	54	CH17 HI
5	CH1 LO	55	CH17 LO
6	CH2 HI	56	CH18 HI
7	CH2 LO	57	CH18 LO
8	CH3HI	58	CH19 HI
9	CH3 LO	59	CH19 LO
10	CH4 HI	60	CH20 HI
11	CH4 LO	61	CH20 LO
12	CH5 HI	62	CH21 HI
13	CH5 LO	63	CH21 LO
14	CH6 HI	64	CH22 HI
15	CH6 LO	65	CH22 LO
16	CH7 HI	66	CH23 HI
17	CH7 LO	67	CH23 LO
18	LLGND	68	LLGND
19	CH8 HI	69	CH24 HI
20	CH8 LO	70	CH24 LO
21	CH9 HI	71	CH25 HI
22	CH9 LO	72	CH25 LO
23	CH10 HI	73	CH26 HI
24	CH10 LO	74	CH26 LO
25	CH11 HI	75	CH27 HI
26	CH11 LO	76	CH27 LO
27	CH12 HI	77	CH28 HI
28	CH12 LO	78	CH28 LO
29	CH13 HI	79	CH29 HI
30	CH13 LO	80	CH29 LO
31	CH14 HI	81	CH30 HI
32	CH14 LO	82	CH30 LO
33	CH15 HI	83	CH31 HI
34	CH15 LO	84	CH31 LO
35	D/A GND 0	85	DOUT0
36	D/A OUT 0	86	DOUT1
37	D/A GND 1	87	DOUT2
38	D/A OUT 1	88	DOUT3
39	CTR1 CLK	89	GND
40	CTR1 GATE	90	+12V
41	CTR1 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	ANALOG TRIGGER IN	93	DIN2
44	DIN0	94	DIN3
45	A/D START TRIGGER IN	95	A/D INTERNALPACER OUTPUT
46	DIN1	96	D/A EXTERNAL PACER INPUT
47	A/D STOP TRIGGER IN	97	EXTERNAL D/A TRIGGER/PACER GATE
48	PC +5V	98	A/D PACER GATE
49	SSH OUT / D/A PACER OUT	99	EXTERNAL INTERRUPT
50	GND	100	GND

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Table 24. 64-channel single-ended mode pin out

Pin	Signal name	Pin	Signal name
1	LLGND	51	LLGND
2	CH0 IN	52	CH16 IN
3	CH32 IN	53	CH48 IN
4	CH1 IN	54	CH17 IN
5	CH33 IN	55	CH49 IN
6	CH2 IN	56	CH18 IN
7	CH34 IN	57	CH50 IN
8	CH3 IN	58	CH19 IN
9	CH35 IN	59	CH51 IN
10	CH4 IN	60	CH20 IN
11	CH36 IN	61	CH52 IN
12	CH5 IN	62	CH21 IN
13	CH37 IN	63	CH53 IN
14	CH6 IN	64	CH22 IN
15	CH38 IN	65	CH54 IN
16	CH7 IN	66	CH23 IN
17	CH39 IN	67	CH55 IN
18	LLGND	68	LLGND
19	CH8 IN	69	CH24 IN
20	CH40 IN	70	CH56 IN
21	CH9 IN	71	CH25 IN
22	CH41 IN	72	CH57 IN
23	CH10 IN	73	CH26 IN
24	CH42 IN	74	CH58 IN
25	CH11 IN	75	CH27 IN
26	CH43 IN	76	CH59 IN
27	CH12 IN	77	CH28 IN
28	CH44 IN	78	CH60 IN
29	CH13 IN	79	CH29 IN
30	CH45 IN	80	CH61 IN
31	CH14 IN	81	CH30 IN
32	CH46 IN	82	CH62 IN
33	CH15 IN	83	CH31 IN
34	CH47 IN	84	CH63 IN
35	D/A GND 0	85	DOUT0
36	D/A OUT 0	86	DOUT1
37	D/A GND 1	87	DOUT2
38	D/A OUT 1	88	DOUT3
39	CTR1 CLK	89	GND
40	CTR1 GATE	90	+12V
41	CTR1 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	ANALOG TRIGGER IN	93	DIN2
44	DIN0	94	DIN3
45	A/D START TRIGGER IN	95	A/D INTERNALPACER OUTPUT
46	DIN1	96	D/A EXTERNAL PACER INPUT
47	A/D STOP TRIGGER IN	97	EXTERNAL D/A TRIGGER/PACER GATE
48	PC +5V	98	A/D PACER GATE
49	SSH OUT / D/A PACER OUT	99	EXTERNAL INTERRUPT
50	GND	100	GND

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Auxiliary DIO connector and pin out

Table 25. DIO connector specifications

Connector type	40-pin header connector
Compatible cables	▪ C40FF-x (x = length in feet) ▪ C40-37F-x (x = length in feet) ▪ BP40-37 (translates to a standard CIO-DIO24 type)
Compatible accessory products with the C40FF-x cable	CIO-MINI40
Compatible accessory products with the C40-37F-x cable or with the BP40-37 and the C37FF-x or C37FFS-x cable	CIO-MINI37 SCB-37 CIO-ERB24 CIO-ERB08 SSR-RACK24 SSR-RACK08

Table 26. Digital I/O connector pin out

Pin	Signal name	Pin	Signal name
1	NC	2	PC +5V
3	NC	4	DGND
5	FIRSTPORTB Bit 7	6	FIRSTPORTC Bit 7
7	FIRSTPORTB Bit 6	8	FIRSTPORTC Bit 6
9	FIRSTPORTB Bit 5	10	FIRSTPORTC Bit 5
11	FIRSTPORTB Bit 4	12	FIRSTPORTC Bit 4
13	FIRSTPORTB Bit 3	14	FIRSTPORTC Bit 3
15	FIRSTPORTB Bit 2	16	FIRSTPORTC Bit 2
17	FIRSTPORTB Bit 1	18	FIRSTPORTC Bit 1
19	FIRSTPORTB Bit 0	20	FIRSTPORTC Bit 0
21	DGND	22	FIRSTPORTA Bit 7
23	NC	24	FIRSTPORTA Bit 6
25	DGND	26	FIRSTPORTA Bit 5
27	NC	28	FIRSTPORTA Bit 4
29	DGND	30	FIRSTPORTA Bit 3
31	NC	32	FIRSTPORTA Bit 2
33	DGND	34	FIRSTPORTA Bit 1
35	PC +5V	36	FIRSTPORTA Bit 0
37	DGND	38	NC
39	NC	40	NC

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