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CIO-DAC02/16

DUAL ANALOG OUTPUTS

User's Manual



Revision 5
October, 2000

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MEGA-FIFO, the CIO prefix to data acquisition board model numbers, the PCM prefix to data acquisition board model numbers, PCM-DAS08, PCM-D24C3, PCM-DAC02, PCM-COM422, PCM-COM485, PCM-DMM, PCM-DAS16D/12, PCM-DAS16S/12, PCM-DAS16D/16, PCM-DAS16S/16, PCI-DAS6402/16, Universal Library, *Insta*Cal, *Harsh Environment Warranty* and Measurement Computing Corporation are registered trademarks of Measurement Computing Corporation.

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1 INTRODUCTION

The CIO-DAC02/16 is a dual-channel analog output board having 16 bits of resolution. One of six output voltage ranges can be individually selected for each channel. Individual or simultaneous output updates are jumper-selectable.

2 SOFTWARE INSTALLATION

The board has a variety of switches and jumpers to set before installing the board in your computer. By far the simplest way to configure your board is to use the *Insta*Cal™ program provided as part of your software package. *Insta*Cal™ will show you all available options, how to configure the various switches and jumpers (as applicable) to match your application requirements, and will create a configuration file that your application software (and the Universal Library) will refer to so the software you use will automatically know the exact configuration of the board.

Please refer to the *Extended Software Installation Manual* regarding the installation and operation of *Insta*Cal™. The following hard copy information is provided as a matter of completeness, and will allow you to set the hardware configuration of the board if you do not have immediate access to *Insta*Cal™ and/or your computer.

3 HARDWARE INSTALLATION

The CIO-DAC02/16 has one bank of address switches, two range switches and one jumper block which must be set before installing the board in your computer. The calibration and test program, InstaCal, included with the CIO-DAC02/16 will show how these switches are to be set and may be run before you open your computer.

The factory defaults are:

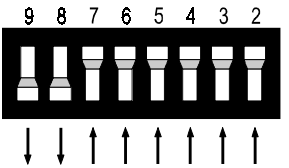
Base Address	300h (768 decimal)
Output 1 (Ch 0) Range	±5 Volts
Output 2 (Ch 1) Range	±5 Volts
UPDATE/XFER jumper	UPDATE (individual update of DACs)

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3.1 BASE ADDRESS

Unless there is already a board in your system which uses address 300 hex (768 decimal), leave the switches as they are set at the factory. Refer to Table 3-1 for PC I/O addresses.

In the example shown in Figure 3-1, the CIO-DAC02/16 is set for base address 300 hex (768 decimal).



SW	HEX
A9	200
A8	100
A7	80
A6	40
A5	20
A4	10
A3	08
A2	04

BASE ADDRESS SWITCH - Address 300H shown here.

Figure 3-1. Base Address Switches

Table 3-1. PC I/O Addresses

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA#1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

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3.2 SIMULTANEOUS TRANSFER JUMPER

Analog outputs can be jumpered so that new output data for one (or both) DACs is held in the registers until any register is read. With this jumper in the XFER position, when any register from BASE +0 to BASE +3 is read, both DACs are updated simultaneously with data TRANSFERRED from the four registers.



JUMPER BLOCK - The jumper block is in the Individual-Update position.

Figure 3-2 to the right shows the jumper block in the individual UPDATE (default) position.

Figure 3-2. Simultaneous Transfer Jumper

Simultaneous transfer is useful if a system requires that a zero voltage be applied from the CIO-DAC02/16 outputs at power up and reset.

The CIO-DAC02/16 outputs are set to 0 volts at power-up and reset but the data in the data registers is not necessarily zero. To avoid a random value being output, use simultaneous update mode and initialize all registers with appropriate values before updating any channel.

3.3 VOLTAGE RANGE SWITCHES

The D/A converters on the CIO-DAC02/16 output a voltage according to the equation:

Unipolar
Volts Out = (V_{FS}/ 65536) x Digital Value

Bipolar
Volts Out = (V_{FS}/ 65536) x Digital Value − (0.5 x V_{FS})

For example, in the 0 to 10V range with an output value of 50350:

Volts Out = (10/65536) * 50350 = 7.6828 volts

Two banks of DIP switches located upper left and right on the CIO-DAC02/16 are used to set the voltage output range of the two DACs. The range of each DACs is set according to the following switch settings Figure . Holding the board as it would sit in the computer expansion slot, U means switch is UP, D means switch is DOWN.

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Use Switch bank S1 to select the output range of Channel 0.

Use Switch bank S2 to select the output range of Channel 1.

Table 3-2. Range Selection Switch Positions

RANGE	1	**2**	**3**	**4**	**5**
±10V	D	U	D	U	D
±5V	D	U	D	D	U
±2.5V	D	U	D	D	D
0 to 10V	U	D	U	U	D
0 to 5V	U	D	U	D	U
0 to 2.5V	U	D	U	D	D

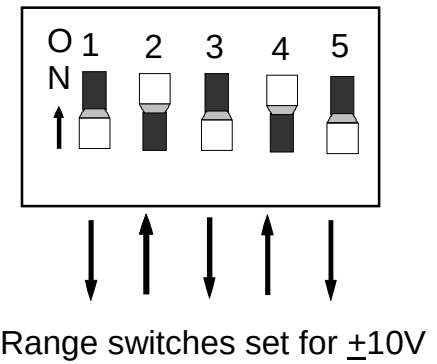


Figure 3-3. Range Switch Block - ±10V Example Shown

3.4 INSTALLING THE CIO-DAC02/16 IN THE COMPUTER

1. Turn the power off.

2. Remove the cover of your computer. Be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

3. Locate an empty expansion slot in your computer.

4. Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DAC02/16.

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4 CONNECTOR DIAGRAM

The CIO-DAC02/16 signal connector is a 25-pin, D-type female connector accessible from the rear of the PC through the expansion backplate (Figure 4-1).

Use the C25FM-# cable with the CIO-MINI25 screw terminal board for easy signal connection.

As an alternative to a cable, you may bring field signals to the 25-pin connector with a DMCON-25 male connector kit available from Measurement Computing Corp.

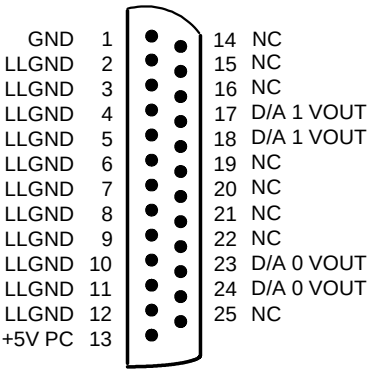


Figure 4-1. 25-Pin Connector Pin out

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5 DATA REGISTERS

The CIO-DAC02/16 has four analog-output data registers. There are two for each channel, one for the lower eight bits and one for the upper eight bits. The first address (BASE ADDRESS) is determined by setting a bank of DIP switches on the board.

The information presented in this chapter is intended for experienced programmers. If you are not familiar with register manipulation, we encourage you to use the Universal Library.

To write to or read from a register in decimal or HEX, the following weights apply:

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

The registers and their function are listed on Table 5-1.

Table 5-1. Data Registers

ADDRESS	WRITE FUNCTION	READ FUNCTION
BASE + 0	D/A 0 Least Significant Byte	Initiate simultaneous update.
BASE + 1	D/A 0 Most Significant Byte	Initiate simultaneous update.
BASE + 2	D/A 1 Least Significant Byte	Initiate simultaneous update.
BASE + 3	D/A 1 Most Significant Byte	Initiate simultaneous update.

The bits of the registers are labeled as follows:

BASE + 0 and BASE +2 (LEAST SIGNIFICANT BYTE)

7	6	5	4	3	2	1	0
DA9	DA10	DA11	DA12	DA13	DA14	DA15	DA16 (LSB)

BASE + 1 and BASE +3 (MOST SIGNIFICANT BYTE)

7	6	5	4	3	2	1	0
DA1 (MSB)	DA2	DA3	DA4	DA5	DA6	DA7	DA8

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6 SPECIFICATIONS

POWER CONSUMPTION

+ 5V Supply	400 mA Typical / 675 mA Max.
+ 12V Supply	None
- 12V Supply	None

ANALOG OUTPUTS

Outputs	2
Resolution	16 Bits (1 in 65536 parts)
Type	AD660BN
Output Ranges	±10, ±5, ±2.5, 0 to 10, 0 to 5, 0 to 2.5
Latches	Double-Buffered
Update	Individual or Simultaneous (Jumper Select)
Power Up/Reset	DAC Output forced to 0 Volts
Offset Error	Adjustable to 0
Gain Error	Adjustable to 0
Differential Linearity	± 1 LSB Max.
Integral Non linearity	± 1 LSB Max.
Monotonicity	Guaranteed to 15 bits over temp range
Gain Drift	± 15 ppm/C Max
Bipolar Offset Drift	± 5 ppm/C Max
Unipolar Offset Drift	± 3 ppm/C Max
Slew Rate	2.8V/µs Typical
Settling Time	
20 Volt Step to 0.0008%	12 µs typical, 19 µs max
10 Volt Step to 0.0008%	6 µs typical, 9 µs max
Current Drive	± 5 mA Min
Output Resistance (Op27)	0.1 Ohm Max
Output Short Circuit Duration	40 mA Min Continuous

ENVIRONMENTAL

Operating Temperature	0 to 70 Deg. C
Storage Temperature	–40 to +100 Deg. C
Humidity	0 to 90% Non-condensing

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EC Declaration of Conformity

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Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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