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# CIO-DAC02

# Dual Channel 12-Bit Analog Output User's Manual




Revision 4
October, 2000

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# TABLE OF CONTENTS

**1: INSTALLATION** . . . . . 1
*1.1 SOFTWARE* . . . . . 1
*1.2 HARDWARE* . . . . . 1
*1.3 BASE ADDRESS* . . . . . 2
*1.4 WAIT STATE JUMPER* . . . . . 3
*1.5 VOLTAGE REFERENCE JUMPERS* . . . . . 3
*1.6 INSTALLING BOARD IN THE COMPUTER* . . . . . 4
**2: SIGNAL CONNECTION** . . . . . 4
*2.1 CONNECTOR DIAGRAM - CIO-DAC02* . . . . . 4
*2.2 ANALOG OUTPUTS* . . . . . 5
*2.3 4-20 mA OUTPUTS* . . . . . 6
**3: DIRECT REGISTER PROGRAMMING** . . . . . 7
*3.1 INTRODUCTION AND EXAMPLE* . . . . . 7
*3.2 D/A CODING* . . . . . 8
**4: SPECIFICATIONS** . . . . . 9

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# 1: INSTALLATION

## 1.1 SOFTWARE

Before you open your computer and install the board, install and run *Insta*Cal, the installation, calibration and test utility included with your board. *Insta*Cal will guide you through switch and jumper settings for your board. Detailed information regarding these settings can be found below. Refer to the *Extended Software Installation* manual for *Insta*Cal installation instructions.

## 1.2 HARDWARE

The CIO-DAC02 (Figure 1-1) has one bank of switches and two jumper blocks which must be set before installing the board in your computer.

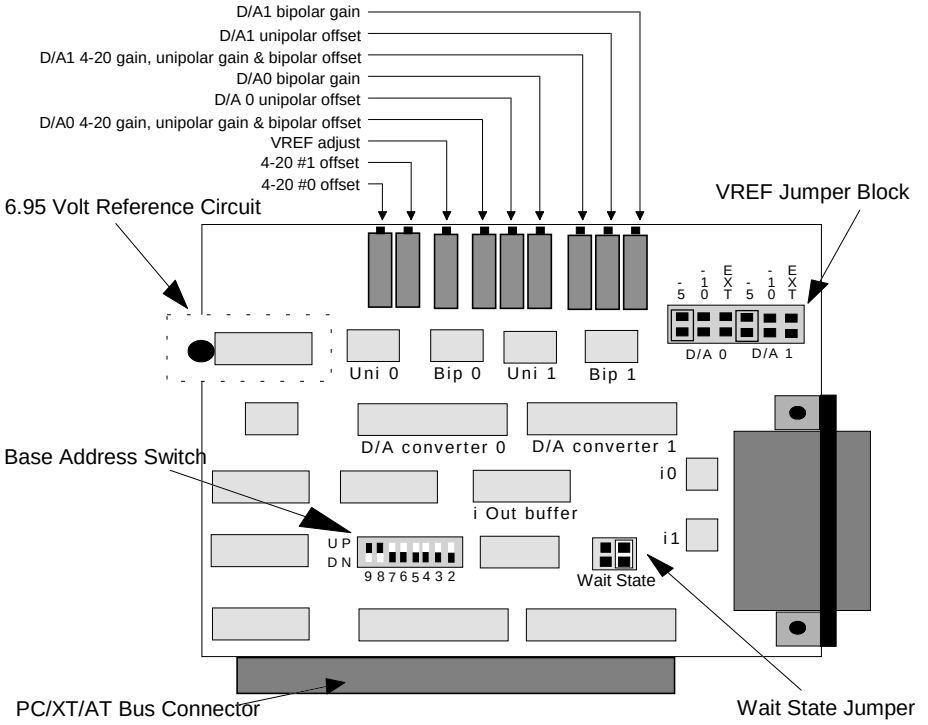



Figure 1-1. Board Layout - CIO-DAC02



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## 1.3 BASE ADDRESS

Unless there is already a board in your system that uses address 300 hex (768 decimal), leave the switches as they were set at the factory. In the example shown in Figure 1-2, the board is set for base address 300 hex (768 decimal).

Table 1-1 lists PC I/O addresses.

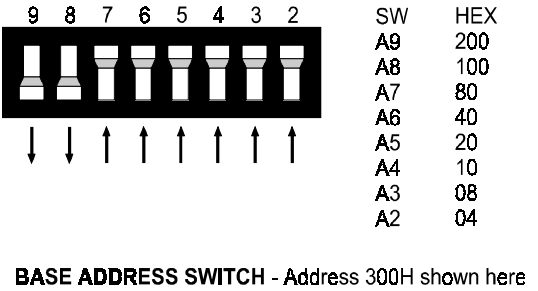



Figure 1-2. Base Address Switches

Table 1-1. I/O Addresses

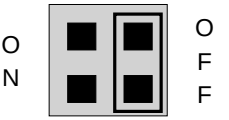
| HEX RANGE | FUNCTION | HEX RANGE | FUNCTION |
|---|---|---|---|
| 000-00F | 8237 DMA #1 | 2C0-2CF | EGA |
| 020-021 | 8259 PIC #1 | 2D0-2DF | EGA |
| 040-043 | 8253 TIMER | 2E0-2E7 | GPIB (AT) |
| 060-063 | 8255 PPI (XT) | 2E8-2EF | SERIAL PORT |
| 060-064 | 8742 CONTROLLER (AT) | 2F8-2FF | SERIAL PORT |
| 070-071 | CMOS RAM & NMI MASK | 300-30F | PROTOTYPE CARD |
| 080-08F | DMA PAGE REGISTERS | 310-31F | PROTOTYPE CARD |
| 0A0-0A1 | 8259 PIC #2 | 320-32F | HARD DISK (XT) |
| 0A0-0AF | NMI MASK (XT) | 378-37F | PARALLEL PRINTER |
| 0C0-0DF | 8237 #2 (AT) | 380-38F | SDLC |
| 0F0-0FF | 80287 NUMERIC CO-P (AT) | 3A0-3AF | SDLC |
| 1F0-1FF | HARD DISK (AT) | 3B0-3BB | MDA |
| 200-20F | GAME CONTROL | 3BC-3BF | PARALLEL PRINTER |
| 210-21F | EXPANSION UNIT (XT) | 3C0-3CF | EGA |
| 238-23B | BUS MOUSE | 3D0-3DF | CGA |
| 23C-23F | ALT BUS MOUSE | 3E8-3EF | SERIAL PORT |
| 270-27F | PARALLEL PRINTER | 3F0-3F7 | FLOPPY DISK |
| 2B0-2BF | EGA | 3F8-3FF | SERIAL PORT |



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## 1.4 WAIT STATE JUMPER

The wait state generator is only active when the CIO-DAC02 is being accessed. In general, the PC is not slowed down by using the wait state. Normally, a wait state is not required.




**WAIT STATE JUMPER - No wait state is selected here. Place jumper on the two leftmost pins for a wait state.**

Figure 1-3. Wait-State Jumper

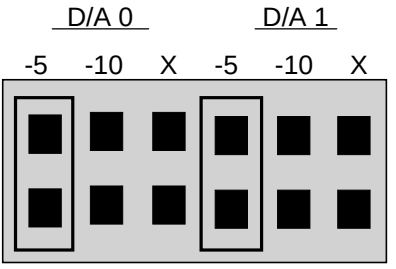
## 1.5 VOLTAGE REFERENCE JUMPERS

The output voltage of the D/A converters is determined by the value of the reference voltage (VREF) and the digital code written to the DACs (see *Analog Output* section below). The VREF signal must be supplied to each D/A or no voltage output will be present at the D/A's output pin. The VREF is supplied via jumpers or from an external source.

A jumper block consisting of two rows of six pins is located on the upper right corner of the board. There are two groups of pins, one for D/A 0 and one for D/A 1. Each group of pins provide a means of supplying either –5V or –10V to each D/A.

NOTE: The board is shipped with both the D/A 0 and D/A 1 VREF jumpers in the external (X) position. With jumpers in the X position, the required D/A reference voltage(s) must be supplied to the 25-pin connector VREF input pins.

A –5VREF provides a ±5V output on the D/A bipolar output, 0-5V output on the unipolar output and a 4-20 mA output on the current output.
If other ranges are desired, an external voltage between –10 and +10 volts should be supplied.




**OUTPUT RANGE SELECT JUMPER BLOCK · The jumpers are in the -5V REF position.**

Figure 1-4.
Output Range Select Jumper Block

The on-board voltage reference jumper supplies the same signals available at the 25-pin connector directly to the D/A VREF input, without the bother of looping the –5VREF or –10VREF outputs back into the D/A VREF inputs, as is required with the MetraByte DAC-02.



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## 1.6 INSTALLING BOARD IN THE COMPUTER

1. Turn the power off.

2. Remove the cover of your computer. Be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

3. Locate an empty ISA expansion slot in your computer.

4. Push the board firmly down into the connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard or the board.

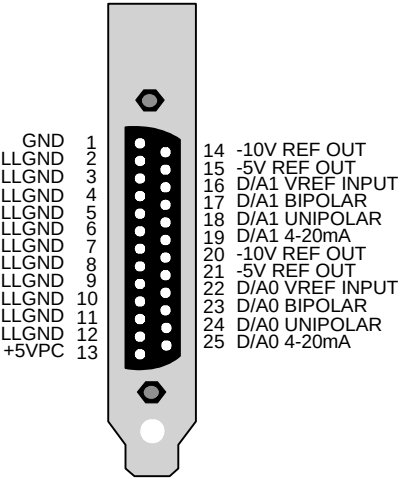
# 2: SIGNAL CONNECTION

## 2.1 CONNECTOR DIAGRAM - CIO-DAC02

The CIO-DAC02 signal connector is a 25-pin D type connector accessible from the rear of the PC through the expansion backplate.

The connector accepts male 25-pin D type connectors. The C25FM-# cable may be used along with a CIO-MINI25 screw terminal board for connecting your field wiring.

As an alternative to a cable, you may attach field wiring to the 25-pin connector with a DMCON-25 connector kit available from Measurement Computing.




**CIO-DAC02 CONNECTOR - View from the rear of the PC.**

Figure 2-1. CIO-DAC02 Signal Connector



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## 2.2 ANALOG OUTPUTS

Each D/A converter has three analog outputs; a unipolar voltage, a bipolar voltage and a 4-20 mA current output. The range of the output is determined by the reference voltage selected on that D/A's VREF input. The CIO-DAC02 provides two on-board jumper selectable reference voltages; –5V and –10V.

Choosing a VREF input of –5V provides a range of 0 to +5 volts on the unipolar output and ±5V on the bipolar output. The 4-20 mA output is also available at this setting.

Choosing a VREF input of –10V provides a unipolar output of 0 to +10 volts and a ±10V bipolar output.

Choosing an external voltage reference will provide:

A **unipolar** output equal to: VREF/4096 * (D/A VALUE) * (–1)

A **bipolar** output equal to: VREF/2048 * ( (D/A VALUE) –2048 )



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## 2.3 4-20 mA OUTPUTS

In addition to voltage outputs, each D/A can supply a 4-20mA output with a resolution of 0.0039 mA per bit. The 4-20 mA outputs may be used to control devices in a 4-20 mA control loop. The 4-20 mA current loop circuit is a precision current sink employing a VMOS FET. A diode provides reverse hookup protection (Figure 2-2).

Select the on - board -5V reference for 4-20mA use.

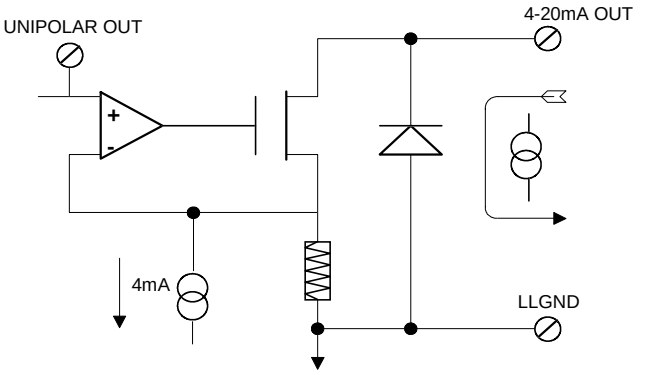



Figure 2-2. Circuit Diagram (Simplified) 4-20 mA Output

A minimum of 8 VDC and a maximum of 36 VDC external excitation voltage is used to power the loop. A typical application would use a 24V loop supply. The loop may use either a grounded load (the supply "floats"), or a grounded supply, (the load "floats"). See Figure 2-3 below.

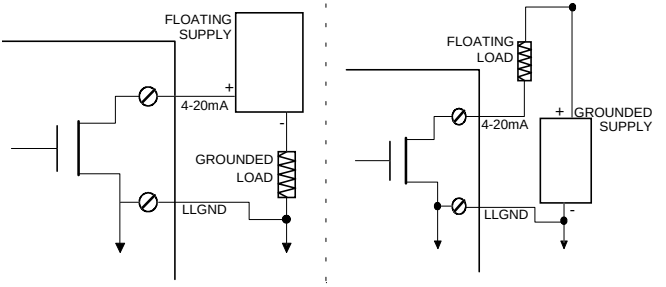



Figure 2-3. Loop Grounding Methods



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# 3: REGISTER PROGRAMMING

## 3.1 INTRODUCTION AND EXAMPLE

The CIO-DAC02 can be programmed by direct register-writes. The board has four registers grouped in sets of two. Each set corresponds to one D/A output chip. Writing to the registers causes an output of the D/A according to the transfer function explained earlier.

An explanation of direct register programming of the CIO-DAC02 follows. We suggest that using the Measurement Computings Universal Library is a more efficient means of programming the registers.

A short example follows:

```
10 Voltage = 2.25                          'Desired output voltage is 2.25V
20 DACOUNTS % = Int (2.25/0.00244)          'Converts volts to D/A digital value
30 MSB % = Int (DACOUNTS%/16)              'Extract the most significant byte (MSB)
40 LSB% = (DACOUNTS% - MSB% * 16)          'Extract the LSB
50 LSB% = LSB% * 16                        'Shift the LSB four places left
60 OUT & H300, LSB%                        'Write LSB to D/A0 LSB register
70 OUT & H301 MSB%                         'Write MSB to D/A0 MSB and update output
```

This BASIC example can be translated to any other language capable of PORT I/O.

The registers of the CIO-DAC02 are:

| | |
|---|---|
| BASE + 0 | D/A0 LSB |
| BASE + 1 | D/A0 MSB & UPDATE |
| BASE + 2 | D/A1 LSB |
| BASE + 3 | D/A1 MSB & UPDATE |

The format of the data registers is:

LSB REGISTER

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D/A9 | D/A10 | D/A11 | D/A12 (LSB) | X | X | X | X |

MSB REGISTER

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D/A1 (MSB) | D/A2 | D/A3 | D/A4 | D/A5 | D/A6 | D/A7 | D/A8 |



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The LSB register of each D/A is buffered and writing to it does not update the D/A output. Writing to the MSB updates the D/A output with the full 12 bits from the LSB buffer and the MSB data.

The CIO-DAC02 may be used as an 8-bit D/A by storing a 0 in the LSB. From that point on, write 8-bit bytes to the MSB for immediate 8-bit updates.

## 3.2 D/A CODING

The coding of the D/A is true binary for the unipolar and 4-20 mA outputs.
The bipolar scheme requires more complex coding. The transfer functions for both are as follows:

A unipolar output is equal to:

D/A OUT = VREF/4096 * (D/A VALUE) * (–1)

A bipolar output is equal to:

D/A OUT = VREF/2048 * ( (D/A VALUE) –2048 )

Table 3-1. D/A Equivalent Outputs

| D/A VALUE | UNIPOLAR OUTPUT | BIPOLAR OUTPUT |
|---|---|---|
| 0 | 0.0V | +5V |
| 2048 | 2.5V | 0.0V |
| 4095 | 5.0V | –5.0V |

NOTE: This table applies for VREF = –5V.



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# 4: SPECIFICATIONS

## Power Consumption:

| | |
|---|---|
| +5V supply | 135 mA typ, 300mA max |
| +12V supply | 15 mA typ, 25mA max |
| -12V supply | 25 mA typ, 35mA max |

## Analog Output:

| | |
|---|---|
| ***D/A converter type*** | **AD7548** |
| ***Resolution*** | ***12 bits*** |
| ***Number of channels*** | ***2 Voltage or Current Output*** |
| Voltage Ranges (Bipolar output) | ±5V, ±10V and user range (determined by value of external reference between -10V and +10V) jumper selectable |
| Voltage Ranges (Unipolar output) | 0 to 5V, 0 to 10V and user range (determined by value of external reference between -10V and +10V) jumper selectable |
| Current Ranges (Current output) | 4 to 20mA (using on-board or external -5V reference) |
| Offset error | Adjustable to zero |
| Gain error | Adjustable to zero |
| Differential nonlinearity | ±0.5LSB max |
| Integral nonlinearity | ±0.5LSB max |
| Relative accuracy | ±0.5LSB (0.01%) max |
| ***Monotonicity*** | ***Guaranteed to 12 bits over temperature*** |
| Gain drift (internal referece) | ±25 ppm/°C max |
| Offset drift | ±3 ppm/°C max |
| Slew Rate | 0.3 V/uS Typical |
| ***Current Drive (voltage outputs)*** | ***±5 mA min*** |
| Voltage Compliance (current out) | 8 to 36V |
| ***Output resistance (OP-07)*** | ***0.1 ohm max*** |
| ***Output short-circuit duration*** | ***40 mA min Continuous*** |
| Miscellaneous | Double buffered output latches<br>Reference input resistance 7 kOhm min |

## Environmental

| | |
|---|---|
| Operating temerature range | 0 to 70°C |
| Storage temerature range | -55 to 125°C |
| Humidity | 0 to 90% non-condensing |



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| CIO-DAC02 | Analog Output Board |
|---|---|
| Part Number | Description |

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

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**EN 50082-1**: EC generic immunity requirements.

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Carl Haapaoja, Director of Quality Assurance

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