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CIO-DAS08-AOH
CIO-DAS08-AOL
CIO-DAS08-AOM

Analog Input &
Digital I/O Board



Revision 5
October, 2000

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1 INTRODUCTION

The CIO-DAS08-AO family of boards, referred to as CIO-DAS08-AOx in this manual, has three members. Where specific aspects of a board are described, the specific part number CIO-DAS08-AOH, CIO-DAS08-AOL, or CIO-DAS08-AOM are used.

The three boards differ only in the A/D gain ranges. The AOH has 'high' gains, the AOL has 'low' gains, and the AOM has 'MetraByte' gains and gain codes.

The analog amplifier is located approximately in the center of the board. The amplifier on the CIO-DAS08-AOH and CIO-DAS08-AOM is part number PGA202. The amplifier on the CIO-DAS08-AOL is part number PGA203.

The CIO-DAS08-AOx boards are an extension of the popular CIO-DAS08 architecture. The two boards are identical at the register level, performance and connector with the following exceptions.

1. Gains are software-programmable. There is only one version of the MetraByte DAS-8AO with gains of 0.5, 1, 10, 100, and 500. Measurement Computing offers two versions. They are the CIO-DAS08-AOH and CIO-DAS08-AOL. The 'H' gains are 0.5, 1, 5, 10, 50, 100, 500, and 1000. The 'L' gains are 0.5, 1, 2, 4, and 8.

2. Analog inputs are differential vs. the single-ended inputs of a CIO-DAS08. To maintain compatibility with signal conditioning boards such as the CIO-EXP16, an optional SIP resistor provides ground reference to the CH LO inputs.

3. A stable crystal oscillator provides the A/D pacer clock pulse. To allow software-compatibility with programs written for the CIO-DAS08, a jumper is provided to choose between the crystal or the PC Bus clock.

4. A DC/DC converter supplies stable +/-15V power to the analog circuitry. An optional version of the board without the DC/DC converter is available on special order of 10 or more units. The cost is lower but the ranges of analog inputs are limited.

5. There is a second digital connector on the CIO-DAS08-AOx as there is on the CIO-DAS08. The MetraByte DAS-08AO does not provide the additional digital I/O lines.

2 SOFTWARE INSTALLATION

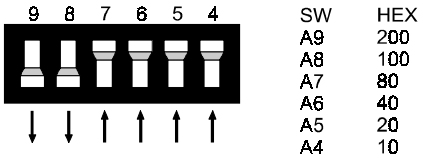
Before you open your computer and install the board, install and run *Insta*Cal™, the installation, calibration and test utility included with your board. *Insta*Cal™ will guide you through switch and jumper settings for your board. Detailed information regarding these settings can be found below. Refer to the *Software Installation* manual for *Insta*Cal™ installation instructions.

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3 HARDWARE INSTALLATION

The CIO-DAS08-AOx has three banks of switches and three jumper blocks which must be set before installing the board in your computer.

3.1 BASE ADDRESS



BASE ADDRESS SWITCH - Address 300H shown here.

Figure 3-1. Base Address Switches

The base address of the CIO-DAS08-AOx is set by switching a bank of DIP switches on the board (Figure 3-1). This bank of switches is labeled ADDRESS and numbered 9 to 4.
Ignore the word ON and the numbers printed on the switch

The switch works by adding up the weights of individual switches to make a base address. A 'weight' is active when the switch is down. Shown to the right, switches 9 and 8 are down, all others are up. Weights 200h and 100h are active, equaling 300h base address. Refer to Table 1-1 for a list of standard PC addresses.

Table 3-1. Standard PC I/O Addresses

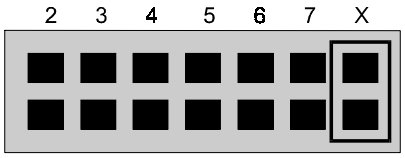
ADDRESS RANGE	FUNCTION	ADDRESS RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

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3.2 INTERRUPT LEVEL SELECT

The interrupt jumper need only be set if the software you are using requires it. If you do set the interrupt jumper, please check your PC's current configuration for interrupt conflicts, and do not use IR2 in PC/AT class machines (or higher).

There is a jumper block on the CIO-DAS08-AOx located just above the PC bus interface (gold pins). The factory default setting is that no interrupt level is set. The jumper is in the 'X' position.



INTERRUPT JUMPER BLOCK - Jumper in X position = No IRQ.

Figure 3-2. Interrupt Jumper Block

If you need to pace conversions through hardware (either the on - board pacer or an external clock), move this jumper to one of the other positions (see table 3-2).

The following table shows some typical interrupt assignments on a PC. The CIO-DAS08-AOx may be configured for interrupt levels 2 through 7. The levels most often available are 5 and 7.

Table 3-2. Interrupt Assignments

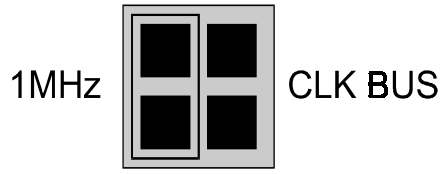
NAME	DESCRIPTION	NAME	DESCRIPTION
NMI	PARITY	IRQ8	REAL TIME CLOCK (AT)
IRQ0	TIMER	IRQ9	RE-DIRECTED TO IRQ2 (AT)
IRQ1	KEYBOARD	IRQ10	UNASSIGNED
IRQ2	RESERVED (XT) INT 8-15 (AT)	IRQ11	UNASSIGNED
IRQ3	COM OR SDLC	IRQ12	UNASSIGNED
IRQ4	COM OR SDLC	IRQ13	80287 NUMERIC CO-P
IRQ5	HARD DISK (XT) LPT (AT)	IRQ14	HARD DISK
IRQ6	FLOPPY DISK	IRQ15	UNASSIGNED
IRQ7	LPT	Note: IRQ8-15 are AT only	

3.3 XTAL/PC BUS CLOCK JUMPER

The A/D pacer clock sources for the MetraByte DAS-8PGA and DAS-8 are different. The source for the DAS-8PGA is fixed at 1 MHz while the source for the DAS-8 is dependent on PC bus speed. The CIO-DAS08-AOx attempts to deal with these differences in a way that satisfies software written for either board.

The CIO-DAS08-AOx is equipped with a jumper which allows you to choose the source of the A/D pacer clock pulse (Figure 3-3). The default for this jumper is the 1 MHz position.

The MetraByte DAS-8PGA is only available with a 1MHz XTAL as the source for the A/D pacer clock. This created problems for users who wanted to use the DAS-8PGA in place of the DAS-8and use existing software because the DAS-8 gets its A/D pacer clock pulse from the PC Bus Clock.



CLOCK SOURCE JUMPER - Place jumper on the two leftmost pins for a standard DAS-8PGA 1 MHZ A/D Pacer Clock. Place jumper on two rightmost pins for DAS-8 type A/D Pacer from P/C Bus Clock.

Figure 3-3. Clock Source Jumper

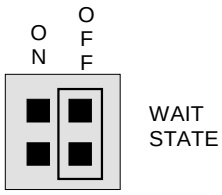
If you need compatibility with the DAS-8 pacing scheme, you can select the PC Bus Clock as the source for the A/D pacer clock.

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3.4 WAIT STATE

A wait state may be enabled on the CIO-DAS08-AOx by selecting WAIT STATE ON at the jumper provided on the board. Enabling the wait state causes the personal computer's bus transfer rate to slow down whenever the CIO-DAS08-AOx is written to or read from.

The wait state jumper is provided in case you one day own a personal computer with an I/O bus transfer rate which is too fast for the CIO-DAS08-AOx. If your board were to fail sporadically in random ways, you could try using it with the wait state ON.

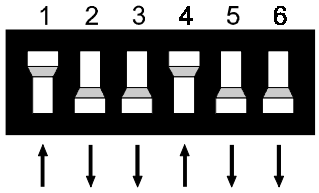


WAIT STATE JUMPER BLOCK - A wait state is not selected on this jumper block. For a wait state, place the jumper on the two leftmost pins.

Figure 3-4. Wait State Jumper Block

3.5 D/A RANGE SWITCH

The analog output voltage range is selectable. A set of DIP switches, one set of six per channel, allow you to choose a range for each channel (Figure 3-5 and Table 3-3). .



+/-5v OUTPUT RANGE - Factory default.

Figure 3-5. Analog Output Range Switches - Typical

Table 3-3. Analog Output Range Select Switches Coding

RANGE	S1	S2	S3	S4	S5	S6
+/-10V	U	D	U	D	D	D
+/-5V	U	D	D	U	D	D
+/-2.5V	U	D	D	D	U	D
+/-1.67V	U	D	D	D	D	U
0-10V	D	U	U	D	D	D
0-5V	D	U	D	U	D	D
0-2.5V	D	U	D	D	U	D
0-1.67	D	U	D	D	D	U

RANGE SELECTION SWITCH SETTINGS - U = Up, D = Down

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3.6 D/A SIMULTANEOUS UPDATE JUMPER

The dual D/A converter can be updated simultaneously or individually. A jumper controls this feature.

When the jumper (see Figure 3-6) is in the NORMAL position, the DAC low byte is written to first, then the high byte (4 bit nibble). When the high byte is written, the DAC output is updated.

When the jumper is in the SIM position, both DACs outputs are updated when you read from DAC 0 Low Byte. First you must load the new output value into both or one DAC, then when the DACs have the correct output value loaded, read from BASE + 8 and the outputs will be updated. Analog Output Range Select Switches

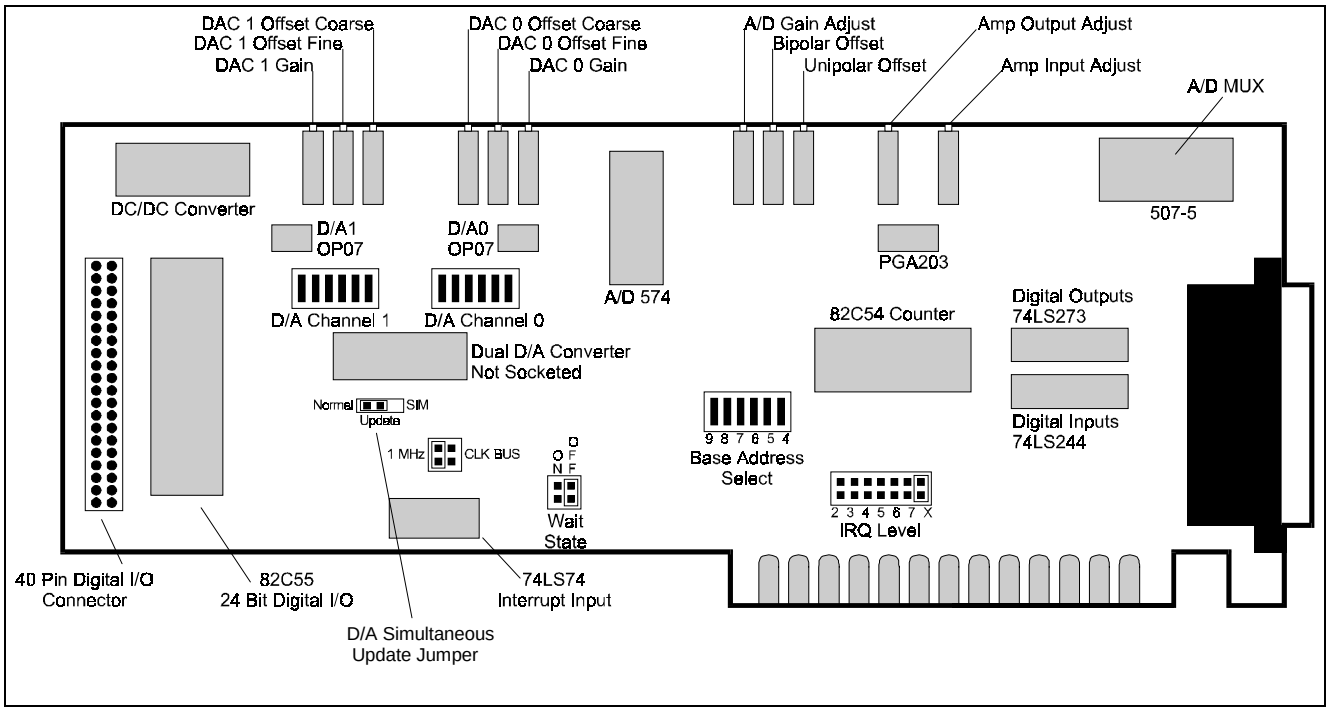


Figure 3-6. CIO-DAS08-A0x Board Layout

3.7 INSTALL THE CIO-DAS08-AOx IN THE COMPUTER

Turn the power off.

Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

Locate an empty expansion slot in your computer.

Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DAS08-AOx.

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4 CALIBRATION AND TEST

The CIO-DAS08-AOx is supplied with *Insta*Cal software which also performs calibration and board testing.
Every board is fully tested and calibrated before shipment. For normal environments, a calibration interval of 6 months to one year is recommended. If frequent variations in temperature or humidity are common, re-calibrate at least every three months. It requires less than 30 minutes to calibrate the CIO-DAS08-AOx.

The CIO-DAS08-AOx does not require recalibration when moved from one computer to another. The reason is that the board has a stable DC/DC converter on-board which supplies the analog +/−15V voltages.

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5 SIGNAL CONNECTION

Making correct signal connections is one of the most important aspects of applying a data acquisition board. Failure to properly connect signals is the most common reason for calls to technical support. Usually, a problem can be located by cross-checking the wiring against the connector diagram

5.1 ANALOG CONNECTOR DIAGRAM

The CIO-DAS08-AOx analog connector is a male 37-pin D-type connector, accessible from the rear of the PC through the expansion backplate.

The connector accepts female 37-pin D-type connectors, such as those on the C73FF-2, 2 foot cable with connectors.

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-TERMINAL and CIO-MINI37 screw terminal boards, CIO-EXP32, 32 channel analog MUX/AMP. Isolation amplifiers may be mounted using the ISO-RACK08 and 5B isolation modules.

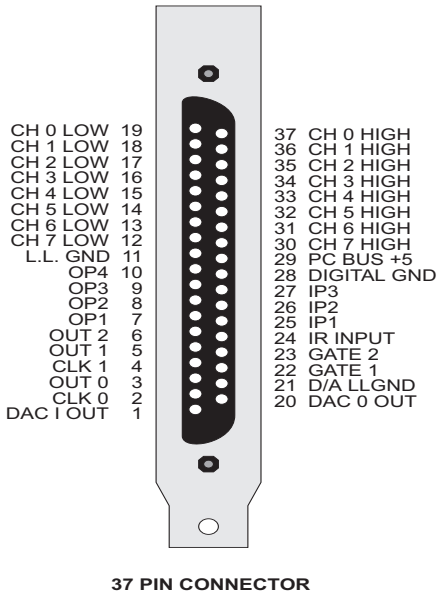


Figure 4-1. Analog Connector Diagram

5.2 DIFFERENTIAL INPUTS

The CIO-DAS08-AOx has eight differential analog inputs. For a detailed description of differential vs. single-ended analog inputs, turn to the section of this manual on Analog Electronics.

Briefly, differential inputs are three-wire analog hookups consisting of a signal-high, a signal-low, and a chassis ground. The benefits of differential inputs are the ability to reject noise, and the ability to eliminate ground loops or potentials between signal low and chassis ground.

Although differential inputs are often preferable to single ended inputs, there are occasions when the floating nature of a differential input can cause input reading difficulties. In those cases, the CIO-DAS08-AOx inputs can be converted to modified differential.

Examine the diagram of the CIO-DAS08-AOx board. A position for an optional Single Inline Package (SIP) of resistors is located near the 37-pin connector. Installing the SIP converts the analog inputs from fully differential to modified differential with a resistive reference to ground. A SIP resistor network is included with the board for this purpose.

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NOTE: When using the CIO-DAS08-PGx with the CIO-EXP16 or CIO-EXP32, the optional SIP resistor must be installed. The CIO-EXP16 and CIO-EXP32 (and MetraByte EXP16) were designed to interface to a single-ended input. Failure to install the SIP resistor when the board is used with these expansion boards will result in floating, unstable readings.

Special instructions and solder are packaged with the SIP resistor. Follow the installation instructions carefully and use the solder provided. Use of any other solder, or failure to follow instructions can result in a degradation of the analog input's accuracy and may require out-of-warranty repair.

5.3 DIGITAL OUTPUTS & INPUTS OP0-2 & IP0-3

The digital outputs and inputs located on the main, or analog connector, may best be reserved for use as CIO-EXP mux controls or trigger inputs. General digital interfacing should be done on the rear 24-bit digital connector.

The digital inputs/outputs on the CIO-DAS08-AOx are at TTL level. TTL is an electronics industry term, short for Transistor Transistor Logic, with describes a standard for digital signals. It is a common misconception that TTL signals are always 0V for low and +5V for high. Although the low signal is reliably close to 0V, the high signal may be anywhere from 2.4V to 5V, and be within the TTL specification.

5.4 DIGITAL I/O CONNECTOR

The 24 bits of digital I/O at the rear of the board are brought to a 40-pin header connector. You can assemble your own cable or purchase a BP40-37 which translates the 40-pin header into a 37-pin, D-type connector with mounting bracket.

Figure 4-2 is the schematic for the BP40-37.

After connection to a BP40-37, the signals at the 37-pin D connector are exactly the same as a CIO-DIO24 or MetraByte PIO12 standard.

Figure 4-3 has the pin assignments at the 37-pin connector.

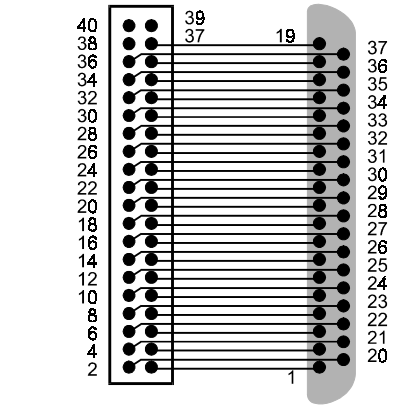


Figure 4-2. BP-37 Cable Schematic

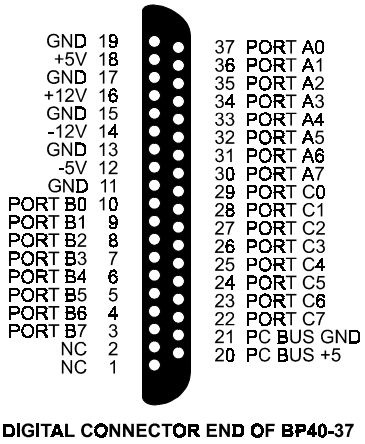


Figure 4-3. Pin Assignments on D-37 End of BP40-37

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6 CIO-DAS08-AOx ARCHITECTURE

All of the programmable functions of the CIO-DAS08-AOx are accessible through the control and data registers, which are explained here.

6.1 REGISTER LAYOUT

The CIO-DAS08-AOx is controlled and monitored by writing to and reading from 16 consecutive 8-bit I/O addresses. The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

Register manipulation is best left to experienced programmers as most of the possible functions are implemented in easy to use Universal Library™.

The register descriptions use the following format:

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	CH8	CH4	CH2	CH1

The numbers along the top row are the bit positions within the 8-bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or hexadecimal, the bit weights in Table 6-1 apply:

Table 6-1. Byte Bit Weights

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write control words or data to a register, the individual bits must be set to 0 or 1 then combined to form a byte. Data read from registers must be analyzed to determine which bits are on or off.

The method of programming required to set/read bits from bytes is beyond the scope of this manual. It will be covered in most Introduction To Programming books, available from a bookstore.

In summary form, the registers and their function are listed on Table 6-2. Within each register are eight bits which may constitute a byte of data or they may be eight individual bit set/read functions.

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Table 6-2. Register Functions

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D Bits 9 - 12 (LSB)	Start 8 bit A/D conversion
BASE + 1	A/D Bits 1 (MSB) - 8	Start 12 bit A/D conversion
BASE + 2	EOC, IP1 - IP3, IRQ, MUX Address	OP1 - OP4, INTE & MUX Address
BASE + 3	Channel MUX and Gain Status	Programmable gain control
BASE + 4	Read Counter 0	Load Counter 0
BASE + 5	Read Counter 1	Load Counter 1
BASE + 6	Read Counter 2	Load Counter 2
BASE + 7	Not used	Counter Control
BASE + 8	Simultaneous Update	DAC 0 Low Byte
BASE + 9	Simultaneous Update	DAC 0 High Byte (& individual update)
BASE + 10	Simultaneous Update	DAC 1 Low Byte
BASE + 11	Simultaneous Update	DAC 1 High Byte (& individual update)
BASE + 12	PORT A 82C55	PORT A 82C55
BASE + 13	PORT B 82C55	PORT B 82C55
BASE + 14	PORT C 82C55	PORT C 82C55
BASE + 15	None	82C55 Control

6.2 A/D DATA REGISTER

BASE ADDRESS (Read / Write)

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	0	0	0	0

READ
On read, it contains the least significant four digits of the analog input data.

These four bits of analog input data must be combined with the eight bits of analog input data in BASE + 1, forming a complete 12 bit number. The data is in the format 0 = minus full scale. 4095 = +FS.

WRITE
Writing any data to the register causes an immediate 8-bit A/D conversion.

BASE ADDRESS + 1 (Read / Write)

7	6	5	4	3	2	1	0
A/D1 MSB	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7	A/D8

READ
On read the most significant A/D byte is read.

The A/D Bits code corresponds to the voltage on the input according to the table below.

DECIMAL	HEX	BIPOLAR	UNIPOLAR
4095	FFF	+ Full Scale	+ Full Scale
2048	800	0 Volts	½ Full Scale
0	0	- Full Scale	0 Volts

WRITE
Writing to this register starts a 12-bit A/D conversion.
A note of caution: Place several NO-OP instructions between consecutive 12-bit A/D conversions to avoid overrunning the A/D converter.

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6.3 STATUS AND CONTROL REGISTER

BASE ADDRESS + 2 (Read / Write) Read Functions

7	6	5	4	3	2	1	0
EOC	IP3	IP2	IP1	IRQ	MUX2	MUX1	MUX0

READ = STATUS

EOC = 1 the A/D is busy converting and data should not be read.

EOC = 0 the A/D is not busy and data may be read.

IP3 to IP1 are the digital input lines on the 37-pin analog connector.

IRQ is the status of an edge triggered latch connected to pin 24 of the analog connector. It is high (1) when a positive edge has been detected. It may be reset to 0 by writing to the INTE mask at BASE + 2 write.

MUX 2 to MUX 0 is the current multiplexer channel. The current channel is a binary coded number between 0 and 7 .

WRITE = CONTROL

BASE + 2 (Read / Write) Write Functions

7	6	5	4	3	2	1	0
OP4	OP3	OP2	OP1	INTE	MUX2	MUX1	MUX0

OP4 to OP1 are the digital output lines on the 37-pin analog connector.

INTE = 1 enables interrupts (positive edge triggered) onto the PC bus IRQ selected via the IRQ jumper on the CIO-DAS08-AOx.

INTE = 0 disables the passing of the interrupt detected at pin 24 to the PC bus.

IRQ is set to 1 every time an interrupt occurs. If you want to process successive interrupts then set INTE = 1 as the last step in your interrupt service routine.

MUX2 to MUX0. Set the current channel address by writing a binary coded number between 0 and 7 to these three bits.

NOTE

Every write to this register sets the current A/D channel MUX setting to the number in bits 2-0.

6.4 PROGRAMMABLE GAIN REGISTER

BASE ADDRESS + 3

A software-programmable register controls the input amplifier. It allows you to select unipolar/bipolar ranges and gains of 1, 10, 100 or 1000 (...AOH) or 1, 2, 4 or 8 (...AOL) via software command.

The register is addressed at the board's Base Address + 3. This register is unused on the CIO-DAS08 and so represents no conflict with existing CIO-DAS08 software.

To set the input range of the CIO-DAS08-AOx board, select the desired range from the table and write the code in decimal or hexadecimal to base address +3. Here is an example in BASIC:

```
100 OUT &H303, 6          'Set gain = 1000, +/-0.005V range.
```


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The register's **Write** layout is :
BASE + 3 (Read / Write) Write Functions

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	R3	R2	R1	R0

The register's **Read** layout is :
BASE + 3 (Read / Write) Read Functions

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	MA2	MA1	MA0	R3	R2	R1	R0

R3 to R0: Indicate the current analog input range.

MA2 to MA0: Indicate the analog input channel that is currently selected (by writing to base +2).

6.4.1CIO-DAS08-AOH GAIN/RANGES

The gain/range of the board is controlled by writing a control code to the Base + 3 register. The gain/range codes are:

BI-POLAR AOH		**CONTROL CODES**					
GAIN	**RANGE V**	**DEC**	**HEX**	**R3**	**R2**	**R1**	**R0**
0.5	+/-10	8	8	1	0	0	0
1	+/-5	0	0	0	0	0	0
5	+/-1	10	A	1	0	1	0
10	+/-0.5	2	2	0	0	1	0
50	+/-0.1	12	C	1	1	0	0
100	+/-0.05	4	4	0	1	0	0
500	+/-0.01	14	E	1	1	1	0
1000	+/-0.005	6	6	0	1	1	0

UNI-POLAR AOH		**CONTROL CODES**					
GAIN	**RANGE V**	**DEC**	**HEX**	**R3**	**R2**	**R1**	**R0**
1	0 to 10	1	1	0	0	0	1
10	0 to 1	3	3	0	0	1	1
100	0 to 0.1	5	5	0	1	0	1
1000	0 to 0.01	7	7	0	1	1	1

6.4.2 CIO-DAS08-AOL GAIN/RANGES

There are fewer ranges available for the CIO-DAS08-AOL. Gains of 2, 4 & 8 are often called binary gains. These ranges are not available on the MetraByte DAS-8AO. The gain/range of the board is controlled by writing a control code to the Base + 3 register.

BI-POLAR AOL		**CONTROL CODES**					
GAIN	**RANGE V**	**DEC**	**HEX**	**R3**	**R2**	**R1**	**R0**
0.5	+/-10	8	8	1	0	0	0
1	+/-5	0	0	0	0	0	0
2	+/-2.5	2	2	0	0	1	0
4	+/-1.25	4	4	0	1	0	0
8	+/-0.625	6	6	0	1	1	0

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UNI-POLAR AOL		CONTROL CODES					
GAIN	RANGE V	DEC	HEX	R3	R2	R1	R0
1	0 to 10	1	1	0	0	0	1
2	0 to 5	3	3	0	0	1	1
4	0 to 2.5	5	5	0	1	0	1
8	0 to 1.25	7	7	0	1	1	1

6.4.3 GAIN/RANGES CIO-DAS08-AOM

For those who require the exact ranges and gain codes of the MetraByte DAS08-AO, the CIO-DAS08-AOM is available. The codes entered in Base + 3 register for the desired range follow:

BI-POLAR AOM		CONTROL CODES					
GAIN	RANGE V	DEC	HEX	R3	R2	R1	R0
0.5	+/-10	8	8	1	0	0	0
1	+/-5	0	0	0	0	0	0
10	+/-0.5	10	A	1	0	1	0
100	+/-0.05	12	C	1	1	0	0
500	+/-0.01	14	E	1	1	1	0

UNI-POLAR AOM		CONTROL CODES					
GAIN	RANGE V	DEC	HEX	R3	R2	R1	R0
1	0 to 10	9	9	1	0	0	1
10	0 to 1	11	B	1	0	1	1
100	0 to 0.1	13	D	1	1	0	1
1000	0 to 0.01	15	F	1	1	1	1

6.5 COUNTER LOAD & READ REGISTERS

COUNTER 0
BASE ADDRESS + 4 (Read / Write)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

COUNTER 1
BASE ADDRESS + 5 (Read / Write)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

COUNTER 2
BASE ADDRESS + 6 (Read / Write)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The data in the counter read register, and the action taken on the data in a counter load register, is wholly dependent upon the control code written to the control register.

The counters are 16-bit counters, each with an 8-bit window, the read / load register. Data is shifted into and out of the 16-bit counters through these 8-bit windows according to the control byte.

You will need an 8254 data sheet if you want to program the 8254 directly at the register level.

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6.6 COUNTER CONTROL REGISTER

BASE ADDRESS + 7 (Write Only)

7	6	5	4	3	2	1	0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

WRITE

SC1 to SC0 are the counter select bits. They are binary-coded between 0 and 2.

RL1 to RL0 are the read and load control bits:

RL1	RL0	OPERATION
0	0	Latch counter
0	1	Read/load high byte
1	0	Read/load low byte
1	1	Read/load low the high byte (Word Transfer)

M2 to M0 are the counter control operation type bits:

M2	M1	M0	OPERATION TYPE
0	0	0	Change on terminal count
0	0	1	Programmable one-shot
0	1	0	Rate generator
0	1	1	Square wave genrator
1	0	0	Software tirggered strobe
1	0	1	Hardware triggered strobe

BCD = 0 then counter data is 16 bit binary. (65,535 max)
BCD = 1 then counter data is 4 decade Binary Coded Decimal. (9,999 max)

6.7 COUNTER TIMER OPERATION

The 8254 counter timer chip (Figure 6-1) can be used for event counting, frequency and pulse measurement and as a pacer clock for the A/D converter. All the inputs, outputs, and gates of the counter are accessible through the 37-pin analog connector with the exception of the counter 2 input.

The counter is easy to understand. The GATE line determines whether or not TTL level pulses present at the CLK input will decrement the counter. The OUT line then transitions (pulses or shifts) depending on the codes in the control register and the count value in the count register.

The counter gates, inputs and outputs are all simple TTL.

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The primary purpose of the counter timer chip is to pace the A/D samples. The input of counter 2 is jumper selectable for a crystal controlled source or the PC bus clock source.

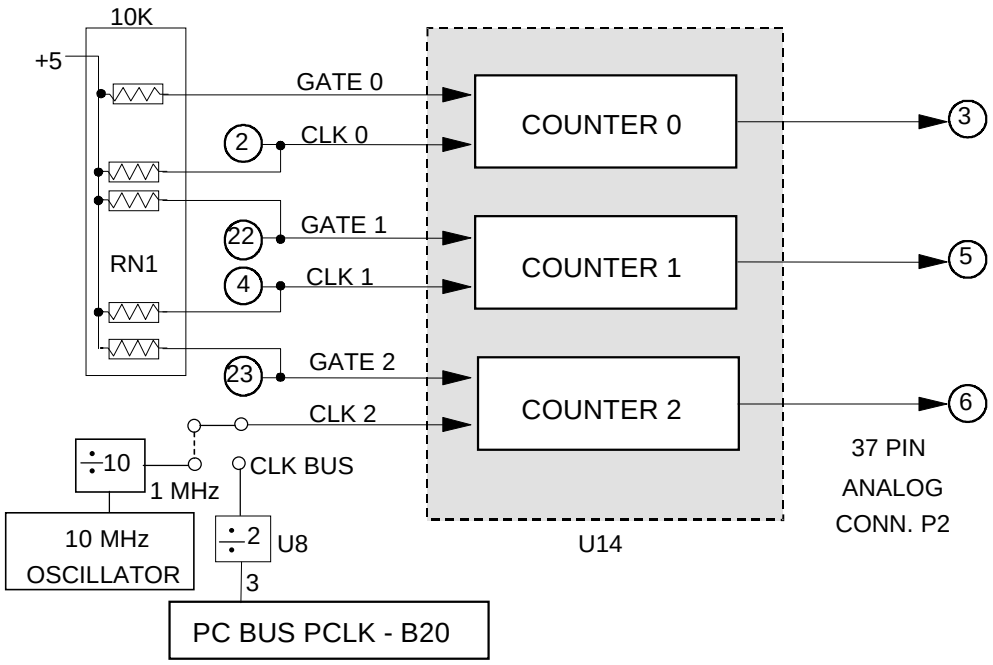


Figure 6-1. 82C54 Counter/Timer Control

The PCLK signal is divided by two prior to the input at counter 2. Therefore, if the PCLK signal on your PC/AT were 8 MHz, the signal at the input of counter 2 would be 4 MHz. The 10 MHz crystal source is divided by 10.

Assuming a 4 MHz signal at counter 2, the rates out of counter 2 (pin 6) may vary between 2 MHz (4 MHz / 2) to 61 Hz (4 MHz / 65,535). For rates slower than 61 Hz, the output of counter 2 should be wired to the input of counter 1. The output of counter 1 would then be wired to the interrupt input (pin 24). The slowest rate would then be once every 17 minutes.

When using the crystal source, the minimum rate would be about 15 Hz using only one counter.

6.8 D/A 0 CONTROL REGISTERS

Each D/A is controlled by a pair of 8-bit registers. These registers contain the low byte and the high nibble of the D/A 12-bit control word. The value written to these two registers controls the output of the D/A chip relative to the range selected by the D/A range select switch.

The D/A output range can generally be calculated as (#/4096) * FSR.

The #/4096 is a proportion of the Full Scale Range selected by the range switch.

Bipolar ranges are 0V at DAC value 2048.

BASE ADDRESS + 8, DAC 0 LOW BYTE (Read / Write)

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0 LSb

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WRITE

A write to this register loads the value written into DAC0's register, but does not update the DAC output.

READ
A read from this register updates both DACs when the Update jumper is set for simultaneous mode. The value read contains no meaningful information.

BASE ADDRESS + 9, DAC 0 HIGH BYTE (Read / Write)

7	6	5	4	3	2	1	0
X	X	X	X	DA11 MSb	DA10	DA9	DA8

WRITE

A write to this register loads the value written into DAC0's register and updates DAC0's output when the Update jumper is set for normal mode.

READ
A read from this register updates both DACs when the Update jumper is set for simultaneous mode. The value read contains no meaningful information.

6.9 D/A 1 CONTROL REGISTERS

BASE ADDRESS + 10, DAC 1 LOW BYTE (Read / Write)

7	6	5	4	3	2	1	0
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0 LSb

WRITE

A write to this register loads the value written into DAC1's register, but does not update the DAC output.

READ
A read from this register updates both DACs when the Update jumper is set for simultaneous mode. The value read contains no meaningful information.

BASE ADDRESS + 11, DAC 1 HIGH BYTE (Read / Write)

7	6	5	4	3	2	1	0
X	X	X	X	DA11 MSb	DA10	DA9	DA8

WRITE

A write to this register loads the value written into DAC1's register and updates DAC1's output when the Update jumper is set for normal mode.

READ
A read from this register updates both DACs when the Update jumper is set for simultaneous mode. The value read contains no meaningful information.

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6.10 82C55 CONTROL & DATA REGISTERS

The 24 bits of digital I/O is composed of one 82C55 parallel I/O chip which contains three data and one control register occupying four consecutive I/O locations.

In summary form, the registers and their function are listed on the following table. Within each register are eight bits which may constitute a byte of data or they may be eight individual bit set/read functions.

BASE + 12	Port A Input of 82C55 #1	Port A Output
BASE + 13	Port B Input	Port B Output
BASE + 14	Port C Input	Port C Output
BASE + 15	None. No read back on 82C55	Configure 82C55 #1

PORT A DATA
BASE ADDRESS +12 (Read / Write)

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

PORT B DATA
BASE ADDRESS + 13 (Read / Write)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Ports A & B may be programmed as input or output. Each is written to and read from in bytes, although for control and monitoring purposes the individual bits are used.

Bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

PORT C DATA
BASE ADDRESS + 14 (Read / Write)

7	6	5	4	3	2	1	0
C7	C6	C5	C4	C3	C2	C1	C0
CH3	CH2	CH1	CH0	CL3	CL2	CL1	CL0

Port C may be used as one 8-bit port of either input or output, or it may be split into two, 4-bit ports which independently may be input or output. The notation for the upper 4-bit port is CH3 - CH0, and for the lower, CL3 - CL0.

Although it may be split, every read and write to port C carries eight bits of data so unwanted information must be ANDed out of reads, and writes must be ORed with the current status of the other port.

OUTPUT PORTS
In 82C55 mode 0 configuration, ports configured for output hold the output data written to them. This output byte may be read back by reading a port configured for output.

INPUT PORTS
In 82C55 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed, transitions are not latched.

For information on modes 1 (strobed I/O) and 2 (bi-directional strobed I/O), you will need to acquire an Intel or AMD data book and see the 82C55 data sheet.

82C55 CONTROL REGISTER
BASE ADDRESS + 15 (Write Only)

7	6	5	4	3	2	1	0
MS	M3	M2	A	CU	M1	B	CL
	Group A				Group B		

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The 82C55 may be programmed to operate in Input/ Output (mode 0), Strobed Input/ Output (mode 1) or Bi-directional Bus (mode 2).

NOTE

Information on programming the 82C55 in mode 0 is included here. Those wishing to use the 82C55 in modes 1 or 2 must procure a data book from Intel Corporation Literature Department.

When the PC is powered up or RESET, the 82C55 is reset. This places all 24 lines in Input mode. No further programming is needed to use the 24 lines as TTL inputs.

To program the 82C55 for other modes, the following control code byte must be assembled into on 8-bit byte.

MS = Mode Set. 1 = mode set active

M3	M2	GROUP A FUNCTION	
0	0	Mode 0	Input / Output
0	1	Mode 1	Strobed Input / Output
1	X	Mode 2	Bi-Directional Bus

A	B	CL	CH	INDEPENDENT FUNCTION
1	1	1	1	Input
0	0	0	0	Output

M1 = 0 is mode 0 for group B. Input / Output
M1 = 1 is mode 1 for group B. Strobed Input / Output

Port A, Port B, Port C-High, and Port C-Low can be independently programmed for inputs or outputs.

The two groups of ports, group A and group B, may be independently programmed in one of several modes. The most commonly used mode is mode 0, input/output mode. The codes for programming the 82C55 in mode 0 are shown in the table below.
D7 is always 1 and D6, D5 & D2 are always 0.

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	OUT	IN	OUT
0	0	1	1	83	131	OUT	OUT	IN	IN
0	1	0	0	88	136	OUT	IN	OUT	OUT
0	1	0	1	89	137	OUT	IN	OUT	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	OUT	IN	OUT
1	0	1	1	93	147	IN	OUT	IN	IN
1	1	0	0	98	152	IN	IN	OUT	OUT
1	1	0	1	99	153	IN	IN	OUT	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

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Power consumption

+5V:	670 mA typical, 840 mA max

Analog input section

A/D converter type	574AJ
Resolution	12 bits
Number of channels	8 differential (configurable as quasi-differential via installation of SIP resistor)
Input Ranges	
CIO-DAS08-AOH	±10V, ±5V, ±1V, ±0.5V , ±0.1V, ±0.05V, ±0.01V, ±0.005V, 0 to 10V, 0 to 1V, 0 to 0.1V, 0 to 0.01V software selectable
CIO-DAS08-AOL	±10V, ±5V, ±2.5V, ±1.25V, ±0.625V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V software selectable
CIO-DAS08-AOM	±10V, ±5V, ±0.5V, ±0.05V, ±0.01V, 0 to 10V, 0 to 1V, 0 to 0.1V, 0 to 0.01V software selectable
Polarity	Unipolar/Bipolar, software selectable
A/D pacing	Internal counter or external source (Interrupt Input, jumper selectable, rising edge) or software polled
A/D Trigger sources	External hardware/software (Digital In 1)
Data transfer	Interrupt or software polled
DMA	None
A/D conversion time	25 µs
Throughput	20 KHz, PC dependent
Accuracy	±0.01% of reading ±1 LSB ±0.05% of full scale
Differential Linearity error	±1 LSB
Integral Linearity error	±0.5 LSB
No missing codes guaranteed	12 bits
Gain drift (A/D specs)	±25 ppm/°C
Zero drift (A/D specs)	±10 µV/°C
Common Mode Range	±10V
CMRR	72 dB
Input leakage current (@25 Deg C)	100 nA
Input impedance	10 Meg Ohms min
Absolute maximum input voltage	±35V

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Analog Output:

D/A converter type	AD7237 dual DAC
Resolution	12 bits
Number of channels	2
Output Ranges	±10V, ±5V, ±2.5V, ±1.67V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.67V Each channel independently switch selectable
Offset error	±1 LSB max (adjustable to 0 with potentiometer)
Gain error	±1 LSB max (adjustable to 0 with potentiometer)
Differential nonlinearity	±0.9 LSB max
Integral nonlinearity	±1 LSB max
Monotonicity	Guaranteed monotonic to 12 bits over temperature
D/A Gain drift	±3 ppm/°C max
D/A Bipolar offset drift	±30 ppm/°C max
D/A Unipolar offset drift	±50 ppm/°C max
D/A pacing	Software paced
D/A trigger modes	Software
Data transfer	Programmed I/O
Settling time (D/A converter) (full scale step to ±0.5 LSB)	8 µs max
Slew Rate (OP07)	0.3V/µs
Current Drive	±5 mA
Output short-circuit duration	indefinite
Output coupling	DC
Output impedance	0.1 Ohms max
Miscellaneous	Double buffered output latches Update DACs individually or simultaneously (jumper selectable)

Digital Input / Output

Digital Type (main connector)	
Output:	74LS273
Input:	74LS244
Configuration	4 fixed output bits, 3 fixed input bits
Number of channels	4 out, 3 in
Output High	2.7 volts min @ –0.4 mA
Output Low	0.4 volts max @ 8 mA
Input High	2.0 volts min, 7 volts absolute max
Input Low	0.8 volts max, –0.5 volts absolute min
Output power-up / reset state	
Digital Type (Digital I/O connector)	82C55
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	3.0 volts min @ –2.5mA
Output Low	0.4 volts max @ 2.5mA
Input High	2.0 volts min, 5.5 volts absolute max
Input Low	0.8 volts max, –0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)
Interrupts	2 through 7, jumper-selectable
Interrupt enable	Programmable
Interrupt sources	External (Interrupt In), rising edge

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Counter section

Counter type	82C54
Configuration	3 down counters, 16 bits each Counter 0 - independent, user configurable Source: user connector (Counter 0 In) Gate: tied high through 10k (enabled) Output: user connector (Counter 0 Out) Counter 1 - independent, user configurable Source: user connector (Counter 1 In) Gate: user connector (Gate 1) Output: user connector (Counter 1 Out) Counter 2 - independent, user configurable Source: 1MHz (from 10MHz Xtal via divide-by-ten) or PC SysClk (via divide by 2 circuit) selectable by jumper Gate: user connector (Gate 2) Output: user connector (Counter 2 Out)
Clock input frequency	10 Mhz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	–20 to 70°C
Humidity	0 to 95% non-condensing

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8.1 VOLTAGE DIVIDERS

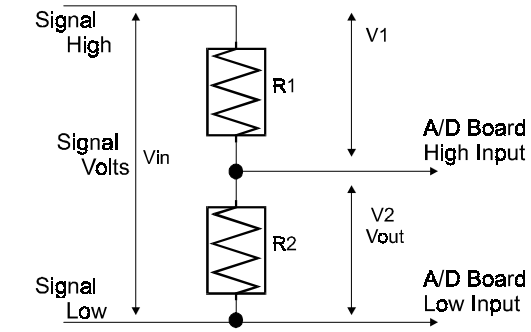
If you wish to measure a signal which varies over a range greater than the input range of an analog or digital input, a voltage divider must be used to drop the voltage of the input signal to the level the analog or digital input can measure.

A voltage divider takes advantage of Ohm's law, which states,

Voltage = Current * Resistance

and Kirkoff's voltage law which states,

The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.



SIMPLE VOLTAGE DIVIDER - $\frac{Vin}{Vout} = \frac{R1+R2}{R2}$

Implied in the above is that any variation in the voltage drop for the circuit as a whole will have a proportional variation in all the voltage drops in the circuit.

In a voltage divider, the voltage across one resistor in a circuit is proportional to the voltage across the total resistance in the circuit.

The object in using a voltage divider is to choose two resistors with the proper proportions relative to the full scale of the analog or digital input and the maximum signal voltage.

Dropping a voltage proportionally is called attenuation. The formula for attenuation is:

$$\text{Attenuation} = \frac{R1 + R2}{R2}$$

The variable attenuation is the proportional difference between the signal voltage max and the full scale of the analog input.

$$2 = \frac{10K + 10K}{10K}$$

For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the Attenuation is 2:1 or just 2.

$$R1 = (A-1) * R2$$

For a given attenuation, pick a handy resisitor and call it R2, the use this formula to calculate R1.

Digital inputs may require the use of voltage dividers. For example, if you wish to input a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to the CIO-AD digital inputs. The voltage must be dropped to 5 volts max when on. The attenuation is 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 1K. Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

IMPORTANT NOTE

The resistors, R1 and R2, are going to dissipate all the power in the divider circuit according to the equation Current (I) = Voltage / Resistance and power (W) = I^2 * R. The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit. Here are two simple rules:

For Attenuation of 5:1 or less, no resistor should be less than 10K.

For Attenuation of greater than 5:1, no resistor should be less than 1K.

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The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. The CIO-TERMINAL is a 16" by 4" screw terminal board with two 37-pin D-type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you may complete with the proper value components for your application.

8.2 DIFFERENTIAL & SINGLE ENDED INPUTS

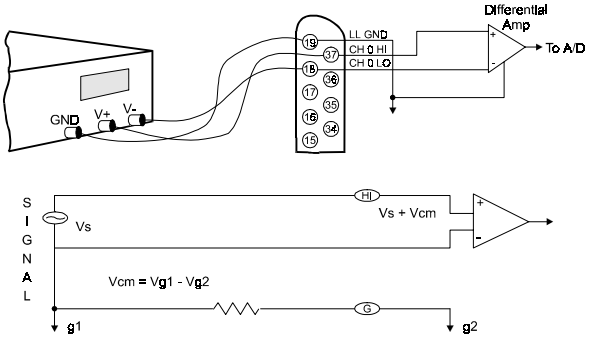
This application note uses the CIO-DAS16 as the example board. Please apply the signal names to the board you have.

Two type of analog inputs are commonly found on A/D boards, they are differential and single ended. Single-ended is typically the less expensive of the two since input connector density is double that for differential inputs.

8.3 COMMON MODE RANGE

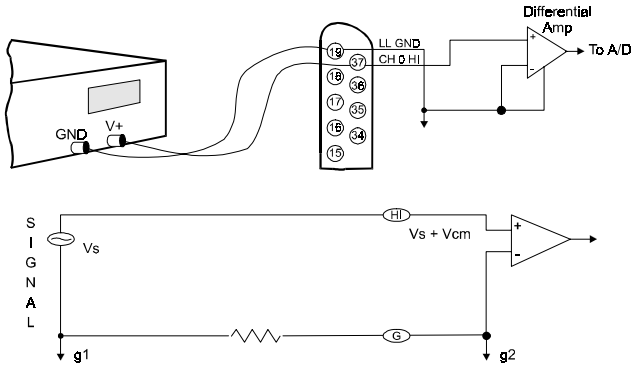
Differential inputs have a common mode range (CMR) (Vcm). Single ended inputs have no CMR. Common mode range is the voltage range over which differences in the low side of the signal and A/D input ground have no impact on the A/D's measurement of the signal voltage. A differential input can reject differences between signal ground and PC ground.

Shown here is a CIO-DAS16 in differential mode. The multiplexer is omitted for simplicity.



DIFFERENTIAL INPUT

A single ended input has no common mode range because there is only one LOW wire, which is assumed to be the same voltage at the source and at the A/D board.



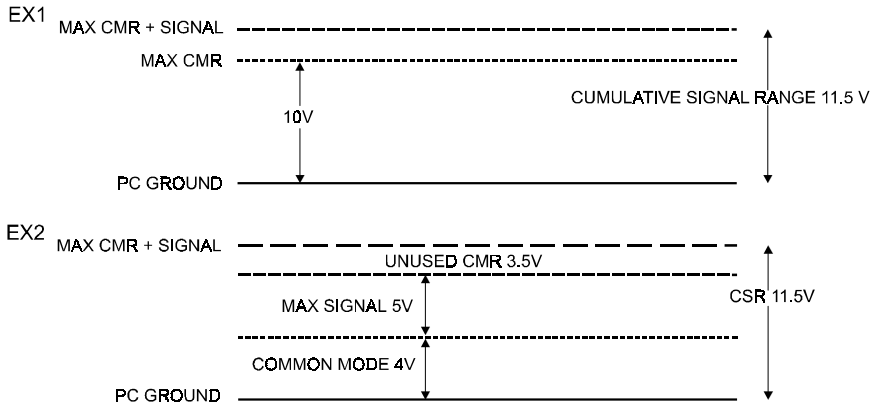
SINGLE ENDED INPUT

The maximum difference which may be rejected is the CMR.

For example, the CIO-DAS16 has a common mode plus signal range of 11.5 volts, common mode not to exceed 10 volts.

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This specification is illustrated graphically here and will be referred to as Cumulative Signal Range (CSR).



Most manufactures of A/D boards specify the CMR directly from the component data sheet, ignoring the effect of the board level system on that specification. A data sheet of that type might claim 10 volts of CMR. Although this is a factual specification and the designer of the board (or other EE) would be able to translate that into a systems specification, most A/D board owners are confused or mislead by such specs.

8.4 COMMON MISUNDERSTANDINGS

The CMR specification of a differential input is often confused with an isolation specification, which it is not. It makes sense. doesn't it, that 10 volts of CMR is the same as 10 volts of isolation? No. The graph above shows why.

Also, failure to specify the common mode plus signal system specification leads people to believe that a DC offset equal to the component CMR can be rejected regardless of the input signal voltage. It cannot as the graph above illustrates.

When is a differential input useful? The best answer is whenever electromagnetic interference (EMI) or radio frequency interference (RFI) may be present in the path of the signal wires. EMI and RFI can induce voltages on both signal wires and the effect on single ended inputs is generally a voltage fluctuation between signal high and signal ground.

A differential input is not affected in that way. When the signal high and signal low of a differential input have EMI or RFI voltage induced on them, that common mode voltage is rejected, subject to the system constraint that common mode plus signal not exceed the A/D board's CSR specification.

8.5 GROUND LOOPS

Ground loops are circuits in which the signal ground and the PC ground are not the same. Ground loop inducing voltage differential may be a few volts of hundreds of volts. They may be constant or transient (spikes). A differential input will prevent a ground loop as long as the CSR specifications is not exceeded.

If ground differences greater than the CMR are encountered, isolation is required.

8.6 USE OF SINGLE-ENDED INPUTS

Why use single ended inputs? First, single ended inputs require fewer parts so they cost less. On an A/D board, the parts cost to go from 16 single ended channels to 16 differential channels is small so that cannot be the reason. The real reason is connector space. Single ended inputs require one analog high input per channel and one LLGND shared by all inputs. Differential inputs require signal high and signal low inputs for each channel and one common shared LLGND.

Single ended inputs save connector space, parts cost and in all cases where there is no common mode voltage or EMI/RFI they work just as well as differential inputs.

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8.7 LOW PASS FILTERS

A low pass filter is placed on the signal wires between a signal source and an A/D board input. It greatly reduces frequencies greater than the cut off frequency that are entering the A/D board's analog or digital inputs.

The key term in a low pass filter circuit is cut-off frequency. The cut-off frequency is that frequency above which no variation of voltage with respect to time may enter the circuit. For example, if a low pass filter had a cut-off frequency of 30 Hz, the kind of interference associated with line voltage (60Hz) would be filtered out but a signal of 25Hz would be allowed to pass.

Also, in digital circuits, low pass filters are often used remove to switch bounce noise.

A simple low pass filter can be made from one resistor (R) and one capacitor (C). The cut off frequency is determined by the formula:

$$Fc = \frac{1}{2 * Pi * R * C}$$

therefore,

$$R = \frac{1}{2 * Pi * C * Fc}$$

Fc = cycles/sec
Pi = 3.14...
R = Ohms
C = Farads

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For Your Notes

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EC Declaration of Conformity

We, Measurement Computing Corp., declare under sole responsibility that the product:

CIO-DAS08-AOx	
Part Number	Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

Carl Haapaoja, Director of Quality Assurance

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Measurement Computing Corporation
16 Commerce Boulevard,
Middleboro, Massachusetts 02346
(508) 946-5100
Fax: (508) 946-9500
E-mail: info@measurementcomputing.com
www. measurementcomputing.com

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