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CIO-DAS16/330i

USER'S MANUAL

REVISION 2, JANUARY 1994

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1 QUICK START

The CIO-DAS16/330i is easy to use. Here is the quick start procedure for those who know how to open the PC an install expansion boards, and want to dive right in.

BOARD SETUP

The CIO-DAS16/330i is setup at the factory with:

BASE ADDRESS	300H (768 Decimal) Same as data sheet.
DMA CHANNEL SELECT	1 Choices are 1 & 3. 3 is used by the hard disk in an XT.
1/10 MHz jumper	1 MHz
8/16 CHANNEL SELECT	8 Differential input channels.
GAIN/RANGE	Programmable. Power-on default is +/- 5 volts
MODE SWITCH	UP Position 7 of the Base Address DIP switch Only DAS16 Compatible when UP. No extended fetures.

Open your PC (after turning off the power) and install the board. Leave the switches as they were set at the factory or refer to the data sheet to change the settings. They are described in detail on the data sheet and in this manual.

After the board is installed and the computer is closed up, turn the power back on.

SOFTWARE SETUP

Insert the CIO-DAS16/330i UTILITY disk in drive A:, or...

Answer your software program setup questions with the information above. The LABLOG II program shipped with your disk has a CIO-DAS16/330i installed. So does the LabTech Acquire program. The Compatible I/O Series utility software and drivers are also preconfigured.

Keep in mind, the CIO-DAS16/330i is 100% compatible with the CIO-DAS16, CIO-DAS16/F and MetraByte DAS-16 series. Software written for these other boards is already configured for the CIO-DAS16/330i.

SIGNAL CONNECTION

The board is factory configured in differential input mode. Differential Input mode requires 3 connections be made from the signal source to the CIO-DAS16/330i. These are SIGNAL HIGH, SIGNAL LOW & GROUND.

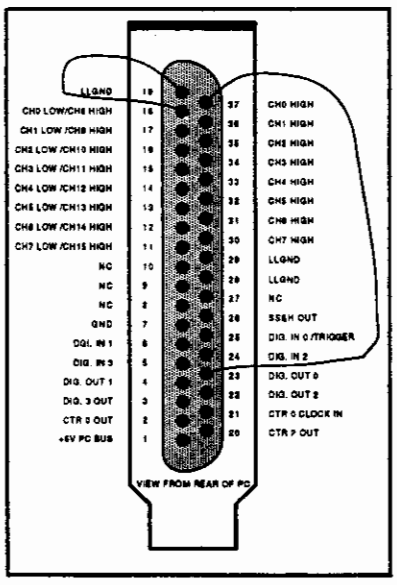
To test the analog inputs you need a known signal to connect to them. The simplest signal to connect is the Digital Output 0 from the CIO-DAS16/330i.

The DAS-16 compatible analog inputs are on the 37 pin connector which extends through the faceplate out the back of the PC when the board is installed.

Using the shorting wires supplied with the board, short pins 18 to 19 and pins 37 to 9 as shown to the right.

Run the program 'IOTEST' on the CIO-DAS16/330i utility disk. Select Digital output channel 0 and Analog input channel 0.

You should see a slow moving square wave on the screen.



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2 CIO-DAS16/330i FEATURES OVERVIEW

The CIO-DAS16/330i is two architectectures on one A/D board; standard DAS-16 registers and extended registers.

To maintain compatibility with existing DAS-16 software, such as Labtech, SnapShot and Language Drivers, a complete set of DAS-16 (CIO-DAS16) registers exist at BASE + 0 through BASE + 15. When in *Compatible Mode,* the CIO-DAS16/330i behaves as a CIO-DAS16 (DAS-16G) would with the exception of much faster sample rates.

A second set of registers exists at BASE + 16 through BASE + 24. In addition, a special register at BASE + 11 opens up when the CIO-DAS16/330I is in *enhanced mode.*

INITIATING ENHANCED MODE

The CIO-DAS16/330I is placed in enhanced mode by setting one switch, then by writing to a specific address. When in enhanced mode, the CIO-DAS16/330I occupies 32 I/O addresses and so may only be placed on even-tens I/O addresses. Examples of achievable base addresses are; 300H, 320H, 340H. Addresses such as 310H and 330H are not possible in enhanced mode.

WHAT DOES ENHANCED MODE GIVE ME?

Enhanced mode opens up additional counters and control registers which allow:

- 16 bit bus transfers.
- Transfer rates of 330KHz using the REP-INSW command.
- Pre-trigger and post-trigger sample buffers.
- 256 entry Channel/Gain queue.

Enhanced mode is fully supported by the BASIC language driver which was shipped with your CIO-DAS16/330i. Using it, you can acquire data at rates to 330KHz and store pre/post trigger buffers of unlimited size (system RAM limits).

THIRD PARTY SOFTWARE

Software packages such as Labtech Notebook will support the enhanced features of the CIO-DAS16/330I in the near future.

Because the CIO-DAS16/330i remains compatible with the DAS-16 even when the enhanced mode features are activated, all third party software will operate regardless of the mode switch position.

A/D WILL BE FASTER - Because the CIO-DAS16/330 has a FIFO buffer which is employed by both DMA and REP-INSW transfers. For example, you may run the version of Labtech which is not upgraded for enhanced mode at 160KHz. When Labtech adds a driver for enhanced mode, the A/D rate will be 330 KHz.

AS YOU FOLLOW THE INSTALLATION PROCEDURES, CONSIDER WHICH MODE YOU WANT TO RUN IN.

USING THE iSBX EXPANSION CONNECTORS

The iSBX expansion connectors are independent of the operation of the CIO-DAS16/330i A/D section and are not affected by the mode switch. They are available in either mode.

There are two expansion connectors on the CIO-DAS16/330i. These expansion connectors conform to Intel's iSBX expansion bus standard. A complete bus specification is avalaible from: Literature Department, Intel Corporation, 3065 Bowers Ave, Santa Clara, CA 95051. The manual order number is 142686-002.

It is not likely that you will need this document unless you plan to design your own iSBX board.

The iSBX bus is widely used. Frequently, manufacturers change the name to something similar such as cSBX (ComputerBoards) or DTX (Data Translation) when they use iSBX bus for their own products.

As implimented on your CIO-DAS16/330i, the iSBX expansion connectors provide access to the personal computer's bus, including address, data, interrupt and DMA. The rear iSBX connector is an 8 bit iSBX bus and the forward iSBX connector is a 16 bit bus. There are reasons for this.

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You will find setup of the iSBX bus in another section of this manual. Separate manuals for ComputerBoards, Inc. cSBX expansion boards are provided with each cSBX expansion boards.

As of this writing, three cSBX expansion boards are available from ComputerBoards:

cSBX Board	Features	Compatibility
cSBX-DDA4	4 Ch D/A @ 330KHz + 14 Dig. Out @ 500 KHz	
cSBX-CTR05	Five, 16 bit counter timers (AM9513A)	CIO-CTR05
cSBX-DIO24H	24 High Drive digital I/O	CIO-DIO24H

THE REASON FOR THE iSBX EXPANSION CONNECTORS

The primary functions of a high performance A/D board are on the main board along with limited DIO and CTR capability. The high performance A/D is the main purpose for purchasing the board.

Frequently, lab set-ups require some mix of digital I/O, counters or analog output to compliment the main measurement functions of the A/D board. The iSBX connectors are there to allow you to customize the CIO-DAS16/330i for your application. If we do not make the cSBX accessory you require, please call tech support and discuss it with us.

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3 INSTALLATION

The CIO-DAS16/330i has one bank of switches, two single function switches and one jumper block which must be set before installation of the board inside your computer. Other switches and jumpers associated with the iSBX expnasion connectors are irrelevant to the operation of the CIO-DAS16/330i main board. The calibration and test program included with the CIO-DAS16/330i will show how these switches are to be set and should be run before you open your computer.

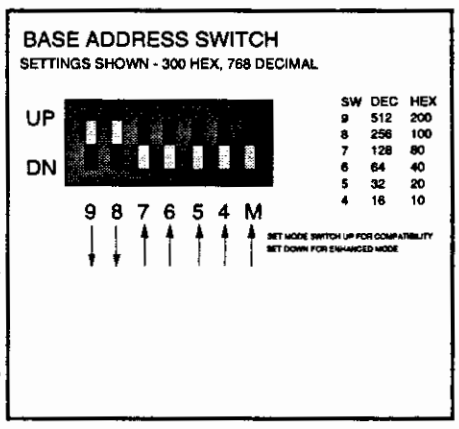
To run the calibration and test program, first install the software included on the CIO-DAS16/330i Utility disk. Create a directory on your hard disk using the command:

[enter]	This means hit enter, don't type the brackets.
MD \CIO16 [enter]	Create a hard disk directory named \CIO16.
CD \CIO16 [enter]	Change to that directory.
	Now put the utility disk in the A: drive.
COPY A:*.* [enter]	The files will be copied.
D1633ISW [enter]	De-compress the programs from the distribution file.
CAL1633i [enter]	The CIO-DAS16/330i calibration and test program.

3.1 BASE ADDRESS

Menu choice number 1 from the CAL main menu is 'SELECT BASE ADDRESS' and runs a program that allows you to choose a desired base address and adjusts the base address if necessary to place it on a 32 or 16 bit boundary.

After a base address is chosen, a diagram of the switch setting is drawn on the PC screen.[1] Set the switches on your base address switch as shown on the diagram. Unless there is already a board in your system which uses address 300 HEX (768 Decimal) then you can leave the switches as they are set at the factory.



In the example shown here, the CIO-DAS16/330i is set for base address 300H.

Switch #7 of the base address switch is a MODE SWITCH and does have an effect on the attainable base address.

When switch 7 is down (enhanced mode) then switch 4 must be up (zero). Whith switch 4 up, base addresses are constrained to 300, 320, 340 and so on. Base addresses such as 310 and 330 are not available.

3.2 MODE SWITCH

Switch #7 of the base address switch is the mode switch. The mode switch enables and disables extended addresses and features of the CIO-DAS16/330i. The extended features are those associated with addresses base+15 through base + 31. When the mode switch is up, no features associated with those registers are available.

NOTE: When the mode switch is DOWN (active), the address 4 switch must be UP (zero).

The state of the mode switch may be read back at Base Address + 11. When the mode switch is UP, Base Address + 11, BIT 4 reads back as 0 (zero). When the mode switch is down, Base Address + 11, BIT 4 reads back as 1 (one).

When the switch is ON (UP), the CIO-DAS16/330i is compatible with the MetraByte DAS-16 and ComputerBoards CIO-DAS16

Because only 16 I/O addresses are used when the mode switch is off, the CIO-DAS16/330i may be placed on 16 bit boundaries, such as 300H, 310H 320H, 330H and 340H.

1 This program attempts to locate conflicts but can only do so if the device occupying the base address you have chosen has read-back registers.

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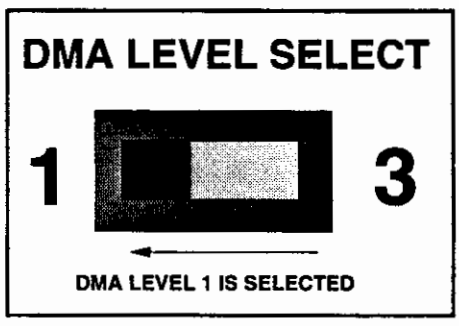
When the mode switch is OFF (DOWN), the CIO-DAS16/330i is in extended features mode, or full PC/AT mode. Additional control bits are present in the upper nibble of Base Address + 11 and a second 8254 counter is addressable for pre/post trigger control. When the mode switch is down, addresses such as 300H, 320H and 340H are available while addresses such as 310H and 330H are not. In enhanced mode, the CIO-DAS16/330i occupies 32 I/O addresses.

The mode switch must be down to access extended features through software.

3.3 DMA LEVEL SELECT

What kind of computer are you installing the board in? If it is an XT then there are only two DMA levels available and level 3 is probably used by the hard disk controller in your XT computer. Set the DMA level switch to the level 1 position.

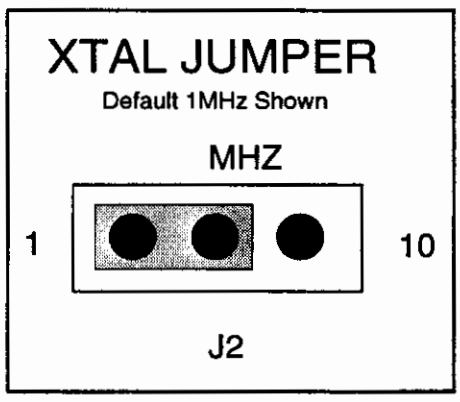
If you have an AT or 386 type computer the hard disk controller is not at level 1 or 3 so either level may be used.



There are other boards that use DMA levels. Some network boards do and so do some IEEE-488 interface boards. Do you have other boards in your computer with DMA level switches on them?

3.4 1/10 MHz XTAL JUMPER

The 1/10 MHz XTAL jumper selects the frequency of the square wave which is connected to OUT 2, the output of 8254 counter 2. Counter 2 is used to pace the A/D start conversion trigger.



Why is this jumper on the board? Because the original DAS-16, designed in 1984, had a 1 MHz crystal. When MetraByte redesigned the DAS-16 and added the faster 10MHz crystal, a jumper was provided to maintain compatibility with older software. The CIO-DAS16/330i has the jumper because the DAS-16 has the jumper and some software expects the jumper to be in the 1 MHz position and some software expects the 10 MHz position.

The CIO-DAS16/330i is shipped with the jumper in the 1 MHz position. The BASIC CALL routine, CIO16, allows you to specify a 1 or 10 MHz position in the setup[2]. Certain MODES, 50 and 51 for example, allow the sample rate to be specified in Hz rather than having to independently set the counter speed. To calculate the counter load values the counter 2 input frequency must be known.

Some software programs, such as UNKELSCOPE, ASYST and ASYSTANT+ require that the jumper be in the 1MHz position. Please refer to the software program user's manual for guidence. Other programs, such as Labtech Notebook, have a 1/10MHz choice in the set-up menu.

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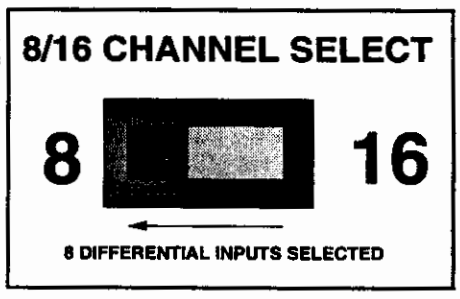
2 See the explaination of MODE 0 in the section on BASIC CALL software.

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3.5 8/16 CHANNEL SELECT

The analog inputs of the CIO-DAS16/330i may be configured as 8 differential or 16 single ended[3]. Using single ended inputs means you have more separate analog input channels available to connect signals. Using differential inputs allows up to 10 volts of common mode (ground loop) rejection and can be more noise immune.

The CIO-DAS16/330i comes from the factory configured for 8 differential inputs so the 8/16 switch is in the position shown here. Set it for the type and number of inputs you desire.



3.6 INSTALLING THE CIO-DAS16/330i IN THE COMPUTER

Turn the power off.

Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

Locate an empty expansion slot in your computer.

Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DAS16/330i.

3.7 PROGRAMMABLE RANGE AND GAIN SETTING

The CIO-DAS16/330i analog input range is fully programmable. The range is set by writing to a register at base address + 11. The 4 lower bits of that register correspond to settings of:

Range	Uni/Bip	G1	G0	Input Range	Decimal
1	0	0	0	±10V	8
0	0	0	0	±5V	0
0	0	0	1	±2.5V	1
0	0	1	0	±1.25V	2
0	0	1	1	±0.625V	3
0	1	0	0	0-10V	4
0	1	0	1	0-5V	5
0	1	1	0	0-2.5V	6
0	1	1	1	0-1.25V	7

Of course, the bits and control words are only of interest to programmers. Applications software takes care of programming the analog input range for you, as does the calibration program.

For those wishing more information on programming the analog inputs, examine the section of register base+11 and the section on BASIC programming.

IMPORTANT NOTE: The CIO-DAS16/330i has a channel/gain queue which may be programmed to align a channel and gain in a programmed channel scan sequence. This feature is implemented in the advanced registers. Base + 11 is a standard DAS-16 gain register and may be used to place the CIO-DAS16/330i in a single range for all channels. It is not possible to program individual gains for each channel when in high speed mode (DMA or REP-INSW) using base+11.

3 For a full discussion of the differences, benefits and applications of single ended and differential inputs see the sections on signal connection, the introduction to analog electronics and the application notes.

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3.8 SIGNAL CONNECTION TO TEST THE INSTALLATION

To test the installation of the CIO-DAS16/330i there must be electrical signals for it to read and display. You can supply the signal with a function generator or other voltage source or you can loop-back the CIO-DAS16/330i output signals onto the CIO-DAS16/330i inputs.

Please, before you connect a voltage from a signal generator or other source, be sure that the signal does not exceed +/- 10V, the maximum analog input range of the board, or 0-5V, the maximum digital input range. The analog inputs are protected to 30V but why prove it.

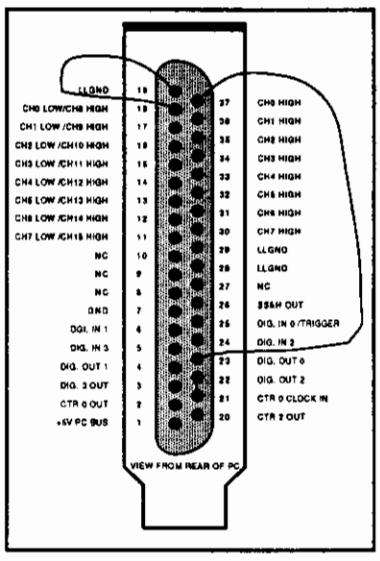
Supplied with the CIO-DAS16/330i are some wires with plugs on each end. These are intended to be plugged directly on the CIO-DAS16/330i 37 pin connector for loop-back testing. If you purchased a screw terminal then connect it up and use it instead.

To test the installation of the CIO-DAS16/330i the digital output 0 will be looped back into the A/D 0 input.

If you are using a signal generator feed the signal directly into A/D channel 0.

The CIO-DAS16/330i is ready to test. You can try running the software supplied with your board now, or you can continue reading the next two sections on Software Installation and Calibration.

The program IOTEST will display the loopback Digital output into the A/D on a strip chart on the screen.



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4 SOFTWARE INSTALLATION

There is a program, InstaCal, supplied on the disk included with your CIO-DAS16330i. This program may be used to configure, install, calibrate and test your board. It is self documenting and requires little explaination beyond the simple instruction to load it on your computer and run it. Help screen may be accessed by pressing F1.

For access to the CIO-DAS16/330i through program control, please refer to the Universal Library programmers manual.

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5 CALIBRATION AND TEST

The CIO-DAS16/330i is supplied with software for calibration and test.

5.1 FREQUENCY OF CALIBRATION

Every board was fully tested and calibrated before being placed in finished goods inventory at the factory. *Your brand new CIO-DAS16/330i should not require calibration before initial use.* For normal environments a calibration interval of 6 months to one year is recommended. If frequent variations in temperature or humidity are common then recalibrate at least once every three months. It takes less than 30 minutes to calibrate the CIO-DAS16/330i.

5.2 REQUIRED EQUIPMENT

Ideally, you will need a precision voltage source, a calculator and some pieces of wire. If you do not have a precision voltage source, you will need a non-precision source and have to make a few calculations.

You will not need an extender card to calibrate the board but you will need to have the cover off your computer with the power on, so trimpots can be adjusted during calibration. For that reason a plastic screwdriver has been supplied with your CIO-DAS16/330i. In the event that the screwdriver is dropped into the PC, no damage will result from short circuits.

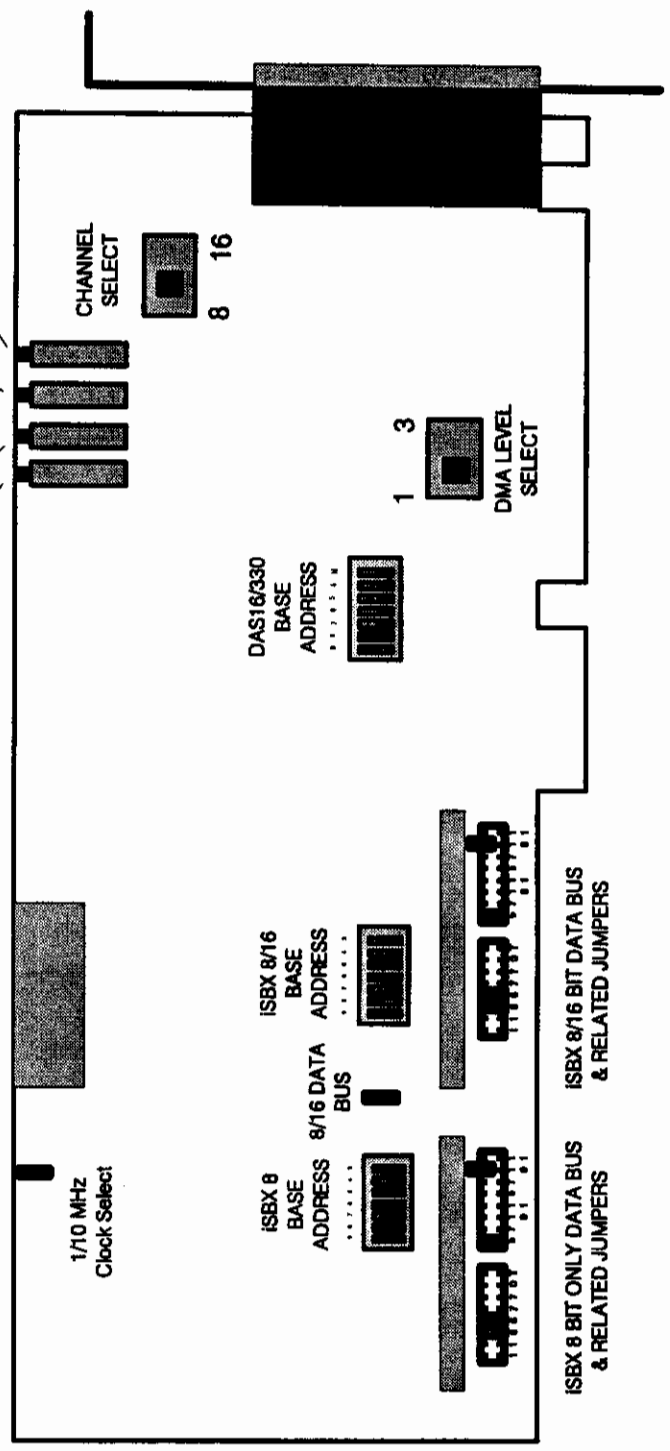
5.3 CALIBRATING THE ANALOG INPUTS

The A/D is calibrated by applying a known voltage to any analog input channel and adjusting trimpots for gain, amplifier input offset, bipolar offset and unipolar offset. There are four trimpots requiring adjustment to calibrate the analog input section of the CIO-DAS16/330i.

The CIO-DAS16/330i should be calibrated for the range you intend to use it in. When the range is changed, slight variation in Zero and Full Scale may result. These variations can be measured and removed in software if desired.

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BOARD LAYOUT WITH CALIBRATION POTS & JUMPERS & SWITCHES



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CALIBRATION PROCEDURE

The entire calibration procedure is provide in the program CAL16JR.EXE which is on the CIO-DAS16/330i utility disk. Please refer to the automated procedure if you want to calibrate your CIO-DAS16/330i. The calibration procedure provided here is informational only.

BIPOLAR OFFSET ADJUSTMENT

1) Set the gain register to the bipolar range which is likely to be used most often.

2) Apply 0V + 1/2 LSB of the specified range to the channel 0 input.

3) Adjust R4, bipolar offset pot, until A/D reads 0/1 counts.

UNIPOLAR OFFSET ADJUSTMENT

1) Set the gain register to the unipolar range which is likely to be used most often.

2) Apply 0V + 1/2 LSB of the specified range to channel 0 input.

3) Adjsut R2, unipolar offset, until A/D reads 0/1 counts.

AMPLIFIER INPUT ADJUSTMENT

1) Apply 0V to the channel 0 input. Shorting cahnnel 0 to LLGND (pin 37 to pin 19) is ideal.

2) Set the gain register to the ±0.625 volt range (code = 3).

3) Adjust R3 until A/D reads 0 counts.

GAIN ADJUSTMENT

1) Set the gain register to the range likely to be used most often.

2) Apply +Full Scale - 1.5 * LSB to the channel 0 input

3) Adjust R1, gain adjust pot, until:
   for unipolar, adjust to 4094/4095 counts.
   for bipolar, adjust to 2046/2047 counts.

5.4 TESTING THE COUNTER/TIMER & DIGITAL I/O

There is no calibration to be performed on the counter timer, which is crystal controlled, or the digital I/O, which are TTL.

CAL16JR can test the cascaded counters 1 and 2 against the system clock to ensure that they are functioning. It can also stimulate the digital outputs and read the digital inputs. A better dynamic test of the counters and digital I/O can be performed by the IOTEST.EXE program.

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6 SIGNAL CONNECTION

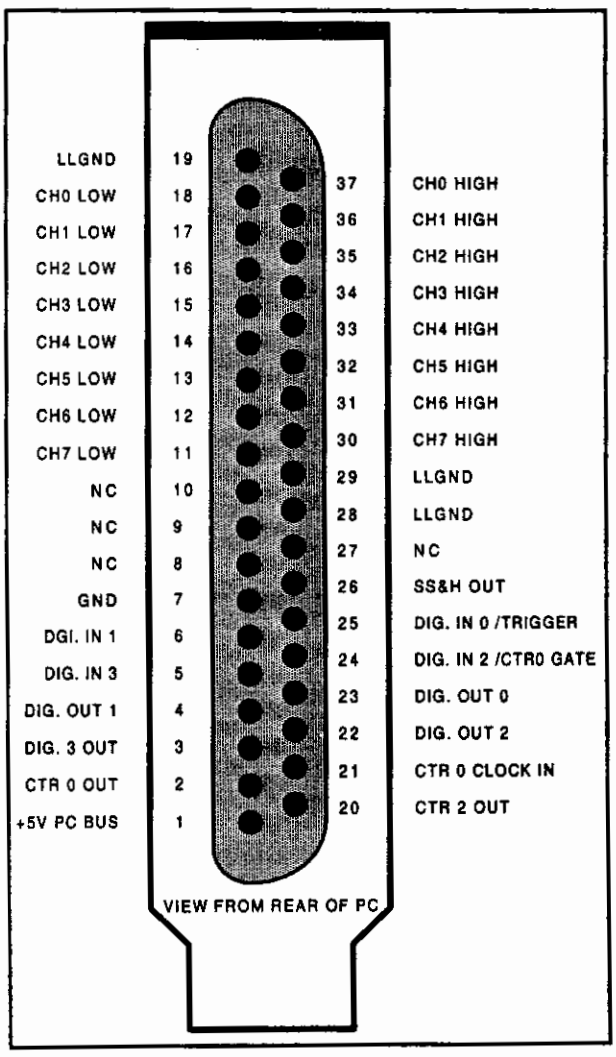
Signal connection can be one of the most challenging aspects of applying a data acquisition board. If you are an *Analog* Electrical Engineer then this section is not for you, but if you are like most PC data acquisition people these simple examples should get you started. The objective here is to present 'how to connect' common signals while avoiding discussion of electrical theory and special symbols. If you need a connection we do not show, or invent one, please call and tell us so we can add it to this manual.

6.1 CONNECTOR DIAGRAM

The CIO-DAS16/330i analog connector is a 37 pin D type connector accessible from the rear of the PC through the expansion backplate. With the exception of the missing D/A signals, the signals available are identical to the DAS-16, an additional signal, SS&H OUT, may be accessed at pin 26.

The connector accepts female 37 D type connectors, such as those on the C73FF-2, 2 foot cable with connectors.

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-TERMINAL screw terminal board, CIO-MUXTC32 32 channels analog MUX/AMP, CIO-SSH-16 16 channel simultaneous sample & hold board or the ISO-RACK08 (and CMUXDAS16-10 cable) 5B module interface rack.



6.2 ANALOG INPUTS

Analog inputs to the CIO-DAS16/330i may be connected in three different configurations. In order of complexity, these are Single Ended, Floating Differential and Differential.

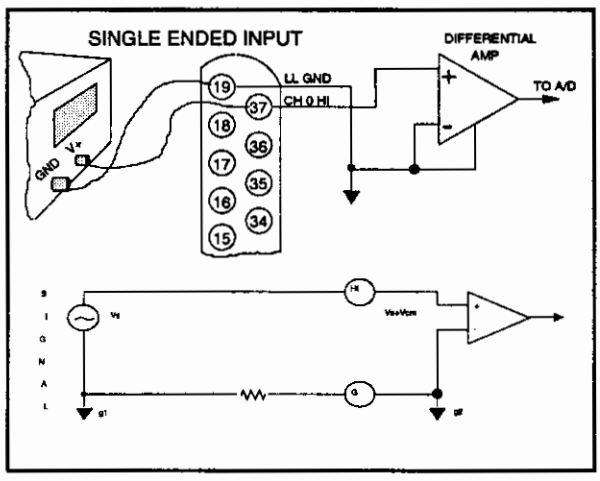
WARNING - PLEASE READ

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Here is a good tip. Measure the voltage potential (difference) between the ground signal at the signal source and the PC. Use a volt meter and place the red probe on the PC ground and the black probe on the signal ground. If there is a difference of ***more the 10 volts,*** *do not connect the CIO-DAS16/330i to this signal source because you will not be able to make any reading. If the difference is* ***more than 30 volts, DO NOT connect this signal to the CIO-DAS16/330i*** *because it will damage the board and possibly the computer.*

6.2.1 SINGLE ENDED

A single ended input is two wires connected to the CIO-DAS16/330i; a channel high (CH# HI) and a Low Level Ground (LLGND). The LLGND signal *must be the same ground the PC is on.* The CH# HI is the voltage signal source.

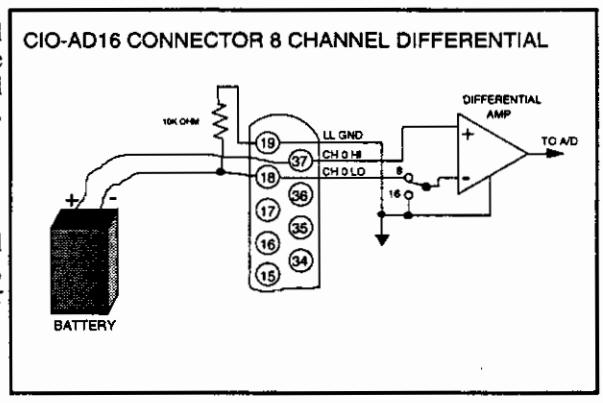


6.2.2 FLOATING DIFFERENTIAL

A floating differential input is two wires from the signal source and a 10K ground reference resistor installed at the CIO-DAS16/330i input. The two signals from the signal source are Signal High (CH# HI) and Signal Low (CH# LO).

The reference resistor is connected between the CIO-DAS16/330i CH# LO and LLGND pins.

A floating differential hookup is handy when the signal source is floating with respect to ground, such as a battery, 4-20mA transmitter or and the lead lengths are long or subject to EMI interference.



The floating differential input will reject up to 10V of EMI energy on the signal wires.

WARNING! Is the signal source really floating? Check it with a voltmeter before risking the CIO-DAS16/330i and PC!

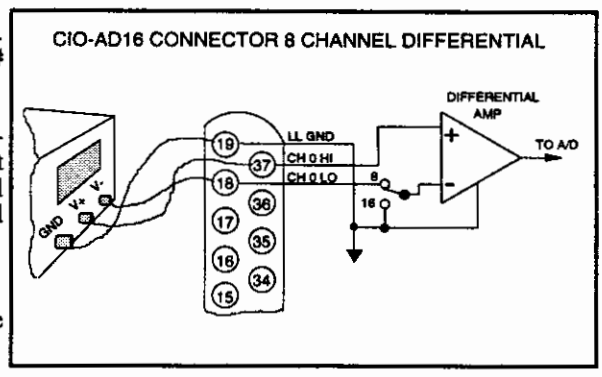
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6.2.3 DIFFERENTIAL

A differential signal is three wires from the signal source. The signals are Signal High (CH# HI), Signal Low (CH# LO) and Signal Ground (LLGND).

A differential connection allows you to connect the CIO-DAS16/330i to a signal source with a ground that is different than the PC ground, but less than 10V difference, and still make a true measurement of the signal between CH# HI and CH# LO.

EXAMPLE:
A laboratory instrument with its own wall plug. There are sometimes differences in wall GND between outlets.



6.3 DIGITAL OUTPUTS & INPUTS

All the digital outputs inputs on the CIO-DAS16/330i are TTL level. TTL is an electronics industry term, short for Transistor Transistor Logic, with describes a standard for digital signals which are either at 0V or 5V. The binary logic inside the PC is all TTL or LSTTL (Low power Schotky TTL). Both specifications are presented here.

Digital signal connections are common and easy to understand when the simple rules presented in the section on analog electronics are applied.

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7 iSBX BUS EXPANSION CONNECTORS

There are two expansion connectors on the CIO-DAS16/330i. These expansion connectors conform to Intel's iSBX expansion bus standard. A complete bus specification is avalaible from: Literature Department, Intel Corporation, 3065 Bowers Ave, Santa Clara, CA 95051. The manual order number is 142686-002.

It is not likely that you will need this document unless you plan to design your own iSBX board.

The iSBX bus is widely used. Frequently, manufacturers change the name to something similar such as cSBX (ComputerBoards) or DTX (Data Translation) when they use iSBX bus for their own products.

As implemented on your CIO-DAS16/330i, the iSBX expansion connectors provide access to the personal computer's bus, including address, data, interrupt and DMA. The rear iSBX connector is an 8 bit iSBX bus and the forward iSBX connector is an 8/16 bit data bus (jumper selectable). There are reasons for this.

As of this writing, three cSBX expansion boards are available from ComputerBoards:

cSBX Board	Features	Compatibility
cSBX-DDA4	4 Ch D/A @ 330KHz + 14 Dig. Out @ 500 KHz	
cSBX-CTR05	Five, 16 bit counter timers (AM9513A)	CIO-CTR05
cSBX-DIO24H	24 High Drive digital I/O	CIO-DIO24H

THE REASON FOR THE iSBX EXPANSION CONNECTORS

The cSBX expansion connectors allow you to add a CIO-DIO24H, CIO-CTR05 or DDA04 directly to your CIO-DAS16/330i at a lower cost than buying a complete digital, counter or D/A plug-in board.

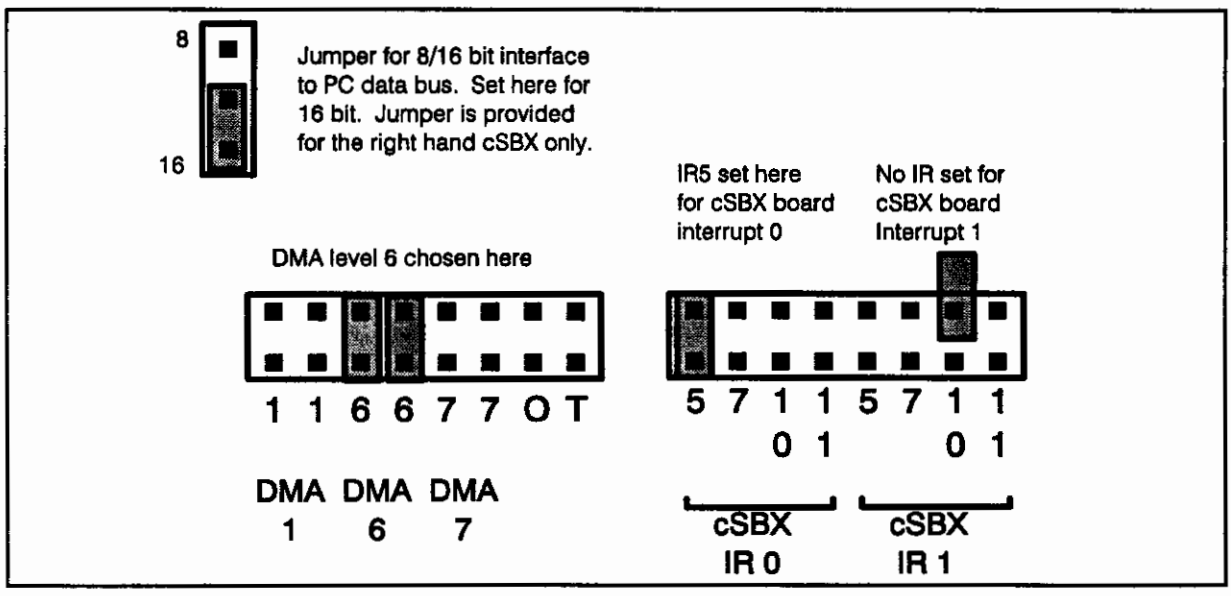
The primary functions of a high performance A/D board are on the main board along with limited DIO and CTR capability. The high performance A/D is the main purpose for purchasing the board.

Frequently, lab set-ups require some mix of digital I/O, counters or analog output to compliment the main measurement functions of the A/D board. The iSBX connectors are there to allow you to customize the CIO-DAS16/330i for your application. If we do not make the cSBX accessory you require, please call tech support and discuss it with us.

The CIO-DAS16/330i has two iSBX connectors, one located on the lower center and one on the lower rear of the board.

7.1 iSBX SET UP

For those of you familiar with data acquisition plug-in boards, set-up of the cSBX expansion connectors will be easy to understand. The following diagram shows the connectors and associated base address, interrupt and DMA jumpers.



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7.1.1 BASE ADDRESS

The base address switch of each iSBX connector performs the same function as a base address switch on an I/O board. If you are using software that will expect a CIO-DIO24H at base address 340, just set that address on the iSBX base address switch.

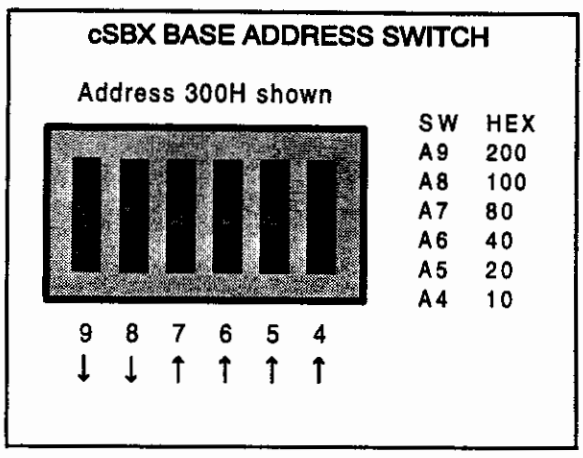
If no board is installed in an iSBX connector, the state of the base address switch is irrelevant. Since no board is installed there are no active devices on the bus. In other words, whatever base address happens to be set on a iSBX base address switch where no board is installed is still available to other boards in your computer.

Each iSBX connector has a base address switch which can locate the 16 iSBX I/O locations anywhere within the PC's I/O address space of 0 to 3FF (hex).

The address switch allows an individual iSBX connector to be located on any 16 byte boundary, such as 300, 310, 320 etc.

The iSBX specification calls for 16 bytes of address for each iSBX connector. That is why the iSBX connectors on your CIO-DAS16/330i use 16 bytes of address even though the cSBX card you have installed may require fewer addresses.

The iSBX center position connector uses 16 address locations regardless of the 8/16 jumper position.



7.1.2 iSBX 8/16 JUMPER

There is a jumper labeled 8/16 which controls the data bus width of the center positioned iSBX connector. It is only for the center positioned connector and has no effect on the rear positioned iSBX connector.

If you set the 8/16 jumper to 8 (only available for the center position iSBX connector), software may write to the board installed in that connector in bytes. If the jumper is set at 16, software **must** write words.

If you have an 8 bit cSBX board such as the cSBX-DIO24H or cSBX-CTR05, the 8/16 jumper must be in the 8 position.

If you have 16 bit cSBX boards, such as the cSBX-DDA4, the 8/16 jumper must be in the 16 position.

The rear positioned iSBX connector is always in 8 bit mode.

7.1.3 iSBX INTERRUPT JUMPERS

The iSBX specification calls for two interrupts for each iSBX connector. There are two sets of interrupt jumpers associated with each iSBX connector and they allow iSBX boards to assert interrupts 5, 7, 10 and 11.

Above the interrupt jumper blocks you will see these interrupt numbers as well as the words INT0 and INT1. The INT0 and INT1 are the two possible interrupt lines coming from an iSBX board. Not all iSBX boards employ interrupts.

To connect INT0 to PC bus interrupt 5, place a jumper on the two pins under the 5 in the group under INT0.

See your iSBX board manual to see if interrupts are required.

7.1.4 iSBX DMA JUMPERS

DMA channels 1, 6, and 7 are available to cSBX boards at each iSBX connector. Select a DMA level by placing a jumper at each of two locations labeled 11, 66 or 77. The jumpers are placed so they span a pin and the one below it. They will not work when oriented side to side.

See the manual for your iSBX board to see if DMA jumpers must be placed.

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7.1.5 iSBX DMA TERMINAL COUNT (T) JUMPER

The terminal count jumper connects a signal from the PC's DMA terminal count signal to the iSBX board when the jumper is in place. See your iSBX board manual to see if this jumper is required.

7.1.6 iSBX OPTION POSTS O1 & O2

The option posts O1 & O2 are provided per iSBX specifications. See your iSBX board manual to see if these posts are required.

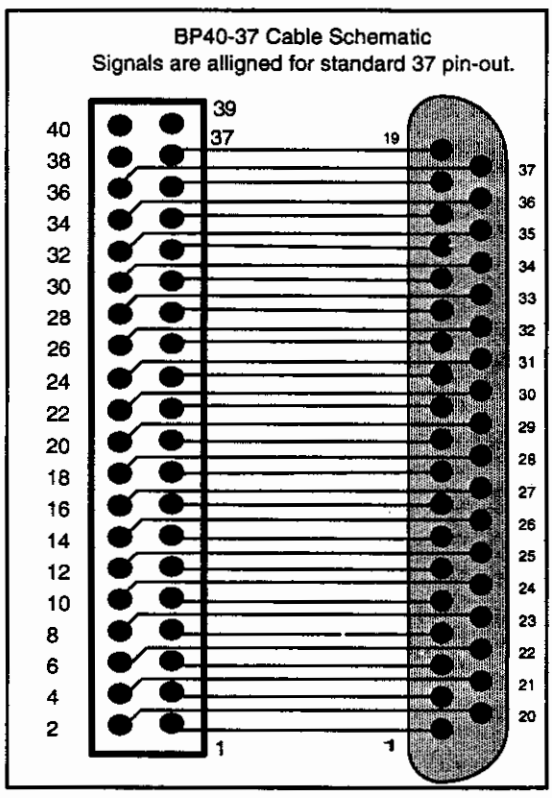
7.1.7 REGISTER & CONNECTOR COMPATIBILITY

The idea of putting the iSBX connectors on the high performance A/D board, CIO-DAS16/330i, was to provide accessory I/O that was **100% COMPATIBLE WITH EXISTING PLUG-IN BOARDS**. To allow you the option of adding digital I/O, counters and D/A that are compatible with existing software (Labtech, ASYST) and have connectors compatible with existing accesory boards and cables.

To learn more about register compatibility between the CIO-CTR05 and cSBX-CTR05, or the CIO-DIO24H and cSBX-DIO24H, please refer to the manuals for those products. You will find that they are register identical.

The cSBX boards have 40 pin headers for signal connection. In line headers are used because of the low profile of the headers as compared to a 37 D type connector.

The signal arrangement of the header is such that when connected to a BP40-37 the signals map directly to a 37pin D type connector and have an identical pin out to the cSBX's corresponding CIO board.



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8 CIO-DAS16/330i ARCHITECTURE

8.1 DATA TRANSFERS

The CIO-DAS16/330i bus interface is a PC/XT/AT bus interface. In compatibility mode (mode switch up) it the CIO-DAS16/330I interfaces to the XT bus only. In enhanced mode, the CIO-DAS16/330I employs the full 16 bit PC/AT bus.

Because 16 bit data transfers are faster, the CIO-DAS16/330i can transfer A/D samples taken with old DAS-16 software at speeds over 150KHz. Old DAS-16 software use DMA to transfer A/D data.

Of course, using the REP INSW command which can only be employed by the CIO-DAS16/330i, data transfers of 330KHz and sample sets of any size up to the size of available memory may be taken.

8.2 FIFO DATA BUFFER

The First In First Out (FIFO) is a specialized memory 1024 samples deep. After each conversion the A/D data is transfered to the FIFO memory. Samples are retrieved from the FIFO by the computer program which stores the data in the PC's memory. This may be a language program, or an application program.

The FIFO is active all the time, regardless of mode. The FIFO does not affect compatibility with existing software, in fact, it does enhance it by allowing data to be transfered asynchronously, therefore at higher speeds.

In addition to enhancing standard interrupt and DMA operations, the FIFO makes possible the use of advanced instructions like REP-INSW, a block transfer.

8.3 CONTROL & DATA REGISTERS

The CIO-DAS16/330i is controlled and monitored by writing to and reading from 16 or 20 consecutive 8 bit I/O addresses. The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

A register is easy to read and write to. Most often, register manipulation is best left to ASSEMBLY language programs as most of the CIO-DAS16/330i possible functions are implemented in easy to use Universal Library routines callable from Basic, PASCAL, C and FORTRAN libraries.

The register descriptions follow all follow the format:

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	CH8	CH4	CH2	CH1

Where the numbers along the top row are the bit positions within the 8 bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write control or data to a register, the individual bits must be set to 0 or 1 then combined to form a Byte. Data read from registers must be analyzed to determine which bits are on or off.

The method of programming required to set/read bits from bytes is beyond the scope of this manual. It will be covered in most Introduction To Programming books, available from a book store.

In summary form, the registers and their function are listed on the following table. Within each register are 8 bits which may constitute a byte of data or 8 individual bit set/read functions.

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ADDRESS	READ FUNCTION - ALL MODES	WRITE FUNCTION
BASE	A/D Bits 9 - 12(LSB) & Channel #	Start A/D Conversion
BASE + 1	A/D Bits 1(MSB) - 8	None
BASE + 2	Channel MUX Read	Channel MUX Set, Clear FIFO
BASE + 3	Digital 4 Bit Input	Digital 4 Bit Output
BASE + 4	None	None
BASE + 5	None	None
BASE + 6	None	None
BASE + 7	None	None[4]
BASE + 8	Status EOC, UNI/BIP, Current Ch.	None
BASE + 9	DMA, Interrupt &Trigger Control	Set DMA, INT etc
BASE + 10	None	Pacer clock control register.
BASE + 11	Gain setting read-back.	Gain, Enhanced Mode, DT Conn.
BASE + 12	Counter 0 Data	Counter 0 Data
BASE + 13	CTR 1 Data - A/D Pacer Clock	CTR 1 Data - A/D Pacer
BASE + 14	CTR 2 Data - A/D Pacer Clock	CTR 2 Data - A/D Pacer
BASE + 15	None. No read back on 8254.	Pacer Clock Control (8254)
	ENHANCED MODE ONLY	
BASE + 11	Upper nibble, enhanced features status.	Upper nibble, enhanced features control.
BASE + 16	Total sample MS Counter	CTR 0. Total counter (1/2).
BASE + 17	Total sample LS Counter	CTR 1. Total counter (1/2).
BASE + 18	Pre-trigger count.	CTR 2. Pre-trigger counter
BASE + 19	None. No read back on 8254	Advanced features counter control (8254).
Base + 22	Channel/Gain Pointer	Set Channel/Gain Pointer
Base + 24	Channel/Gain Data at pointer.	Load Channel/Gain Data at pointer

8.3.1 A/D DATA & CHANNEL REGISTERS

Note: When in enhanced mode the bus interface is 16 bits wide and all registers should be read as 16 bit pairs. To whit, the register at BASE + 1 should be read as the most significant 8 bits of a 16 bit read to BASE + 0.

BASE ADDRESS Example, 300 HEX, 768 Decimal

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	CH8	CH4	CH2	CH1

A read/write register.

READ

4 These four addresses, Base + 4 through Base + 7, are the addresses used by the analog output chips on the CIO-DAS16 (MetraByte DAS-16). In order to stay 100% software compatible, these four registers are empty on the CIO-DAS16/330i.

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On read, it contains two types of data. The least significant 4 digits of the Analog input data and the channel number which the current data was taken from.

These 4 bits of analog input data must be combined with the 8 bits of analog input data in BASE + 1, forming a complete 12 bit number. The data is in the format 0 = minus full scale. 4095 = +FS.

The channel number is binary. The weights are shown in the table above. If the current channel were 5 then bits CH4 and CH1 would be high, CH8 and CH2 would be low.

WRITE

Writing any data to the register causes an immediate A/D conversion.

BASE ADDRESS + 1 301 HEX, 769 Decimal

7	6	5	4	3	2	1	0
A/D1 MSB	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7	A/D8

A Read-only register.

On read the most significant A/D byte is read.

8.3.2 CHANNEL MUX SCAN LIMITS REGISTER

BASE ADDRESS + 2 302 HEX, 770 Decimal

7	6	5	4	3	2	1	0
CH H8	CH H 4	CH H 2	CH H 1	CH L8	CH L4	CH L2	CH L 1

A read and write register.

READ

The current channel scan limits are read as one byte. The high channel number scan limit is in the most significant 4 bits. The low channel scan limit is in the least significant 4 bits.

WRITE

The channel scan limits desired are written as one byte. The high channel number scan limit is in the most significant 4 bits. The low channel scan limit is in the least significant 4 bits.

That is one way of looking at this register, and probably the most sensible way. In fact, the bits 3-0 contain the starting channel number and bits 7-4 contain the ending channel number. If you wanted to scan channels 1, 2, 3 in that order, you could do so by placing the 3 in bits 7-4 and the 1 in bits 3-0.

NOTE: Every write to this register sets the current A/D channel MUX setting to the number in bits 0-3. See BASE + 8.

NOTE: Every write to this register clears the FIFO buffer.

NOTE: This register is disabled in enhanced mode, whenever the channel/gain queue is enabled.

8.3.3 4 BIT DIGITAL I/O REGISTERS

BASE ADDRESS + 3 303 HEX, 771 Decimal

When read...

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7	6	5	4	3	2	1	0
0	0	0	0	DI3	DI2, CTR 0 GATE	DI1	DI0, TRIG

READ

The signals present at the inputs are read as one byte, the most significant 4 bits of which are always zero. The pins 25 (digital input 0) and 24 (digital input 2) digital inputs have two functions each.

The TRIG function of digital input 0 may be used to hold off the first sample of an A/D set by holding it low (0V) until you are ready to take samples, which are then paced by the 8254. It can also be used as the source of an external start conversion pulse, synchronizing A/D conversions to some external event.

When written to..

7	6	5	4	3	2	1	0
X	X	X	X	DO3	DO2	DO1	DO0

WRITE

The upper four bits are ignored. The lower four bits are latched TTL outputs. Once written, the state of the inputs cannot be read back because a read back would read the separate digital input lines (see above).

8.3.4 STATUS REGISTER

BASE ADDRESS + 8 308 HEX, 776 Decimal

7	6	5	4	3	2	1	0
EOC	U/B	MUX	INT	CH8	CH4	CH2	CH1

A read mostly, one-function-write register.

READ

EOC = 1, the A/D converter is busy. EOC = 0, it is free.

U/B = 1, the amplifier is in Unipolar mode. U/B = 0, is bipolar.

MUX = 1, Channels are configured 16 single ended. MUX = 0, 8 differential.

INT = 1, an external pulse has been received. INT = 0, the flip-flop is ready to receive a pulse..

There is a flip-flop on the TRIGGER input (pin 25) which will latch a pulse as short as 200 nanoseconds. Once triggered, this flip-flop must be reset by a write to this register. Your interrupts service routine must do this before another interrupt trigger can be received.

CH8, CH4, CH2 & CH1 are a binary number between 0 and 15 indicating the channel number that the MUX is currently set to and is valid only when EOC = 0. The channel MUX increments shortly after EOC = 1 so may be in a state of transition when EOC = 1. The binary weight of each bit is shown in the table above.

WRITE

A write of any data to this register resets the flip-flop on the pin 25 input and sets the INT bit to 0.

8.3.5 DMA, INTERRUPT & TRIGGER CONTROL

BASE ADDRESS + 9 309 HEX, 777 Decimal

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7	6	5	4	3	2	1	0
INTE	IR4	IR2	IR1	Don't Care	DMA	TS1	TS0

A read and write register.

READ

INTE = 1, Interrupts are enabled. An interrupt generated will be placed on the PC bus interrupt level selected by IR4, IR2 & IR1. INTE = 0, interrupts are disabled.

IR4, IR2, IR1 are bits in a binary number between 0 and 7 which map interrupts onto the PC bus interrupt levels 2 - 7. Interrupts 0 & 1 map into interupts 10 and 11.

DMA = 1, DMA transfers are enabled. DMA = 0, DMA transfers are disabled. It is worth noting that this bit only allows the CIO-DAS16/330i to assert a DMA request to the PC on the DMA request level selected by the DMA switch on the CIO-DAS16/330i. Before this bit is set to 1, the PC's 8237 (or appropriate) DMA controller chip must be set up.[5]

TS1 & TS0 control the source of the A/D start conversion trigger according to the table below.

TS1	TS0	
0	X	Software triggered A/D only.
1	0	Start on rising TRIGGER (Digital input 0, Pin 25)
1	1	Start on Pacer Clock Pulse (CTR 2 OUT, no external access)

8.3.6 PACER CLOCK CONTROL REGISTER

BASE ADDRESS + 10 30A HEX, 778 Decimal

7	6	5	4	3	2	1	0
X	X	X	X	X	X	CTR0	TRIG0

Write only

CTR0 = 1. When CTR0 = 1, an on-board 100KHz clock signal is ANDed with the COUNTER 0 CLOCK INPUT (pin 21). A high on pin 21 will allow pulses from the on-board source into the 8254 Counter 0 input.

CTR0 = 0. When CTR0 = 0, the input to 8254 Counter 0 is entirely dependent on pulses at pin 21, COUNTER 0 CLOCK INPUT.

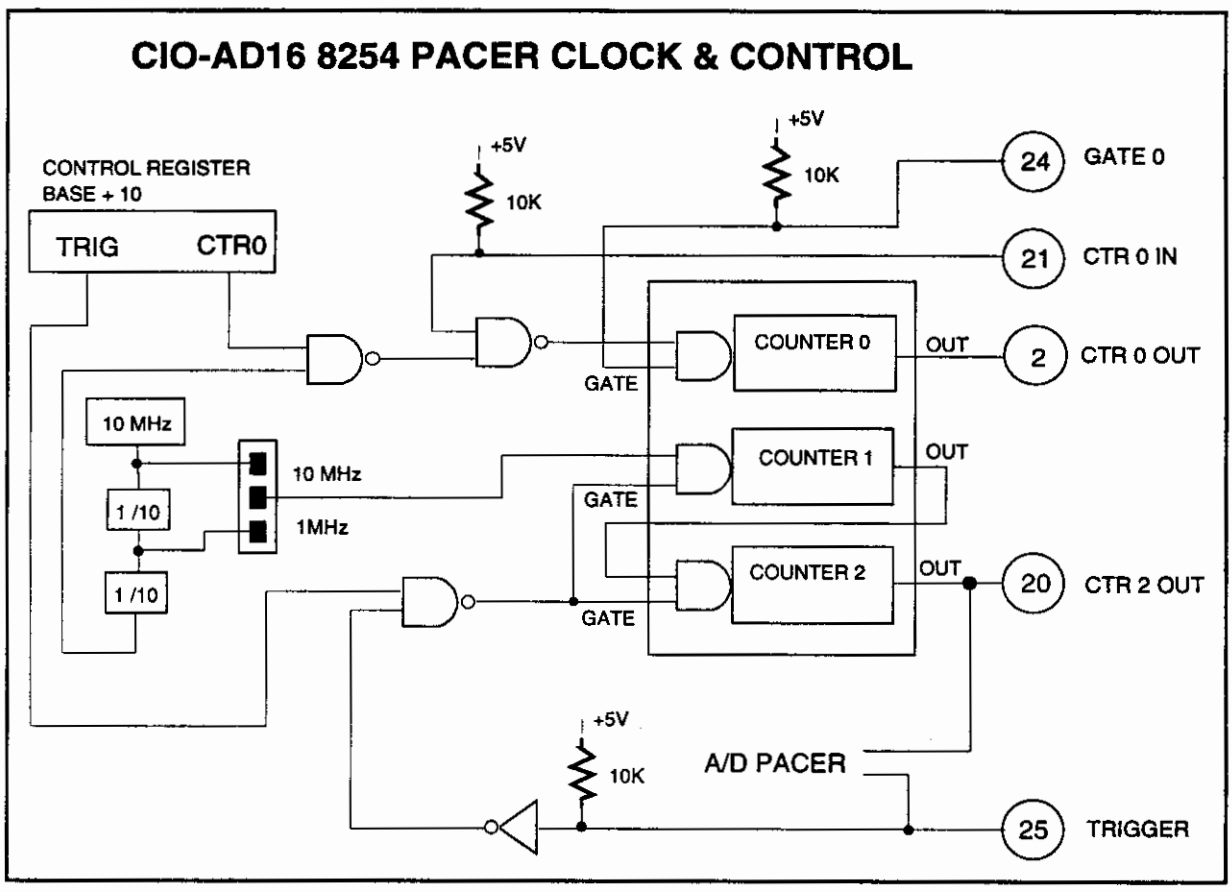
TRIG0 = 1. When TRIG0 = 1, the TRIGGER input at pin 25 is ANDed with TRIG0 which must therefore be high for the pulses from the on-board pacer clock (8254) to start A/D conversions. The input at pin 25 is pulled up and will always be high unless pulled low externally.

TRIG0 = 0. When TRIG0 = 0, the GATEs of counter 1 & 2 are held high, preventing any pulses from acting as a source of A/D start pulses.

The following diagram may help understand these registers, and is further explained in the section covering the 8254.

5 An example of how to set up the DMA controller may be found in the BASIC CALL source code. The code is the same for PC/XT/AT and 386. The source code is for sale only after executing a non-disclosure agreement. Please contact our technical support for a copy of the agreement.

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8.3.7 ANALOG INPUT RANGE REGISTER

BASE ADDRESS + 11 - **Compatible Mode** 30B HEX, 779 Decimal

A write to this register sets the analog input range for all 8/16 analog inputs. The lower 4 bits set the analog input range. The upper 4 bits are not used in compatibility mode.

7	6	5	4	3	2	1	0
X	X	X	X	Range	Uni/Bip	G1	G0

Range	Uni/Bip	G1	G0	Input Range	Decimal
1	0	0	0	±10V	8
0	0	0	0	±5V	0
0	0	0	1	±2.5V	1
0	0	1	0	±1.25V	2
0	0	1	1	±0.625V	3
0	1	0	0	0-10V	4
0	1	0	1	0-5V	5
0	1	1	0	0-2.5V	6
0	1	1	1	0-1.25V	7

To set the analog inpput range of the CIO-DAS16/330i programatically, write the correct input range code to the base address + 11. For example, from BASIC:

If the board's base address is 300 HEX (768 decimal), then the gain register is at 768 + 11 = 779

MVC KNIFE
MVC DYNO
EST GRIP
EST KNIFE

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```
100  OUT 779, 5                    'Set analog output range to 0-5V
```

The decimal range codes are in the far right column above.

BASE ADDRESS + 11 - Enhanced Mode **30B HEX, 779 Decimal**

A write to this register sets the analog input range for all 8/16 analog inputs as well as enabling and disabling extended featuresand controlling extended features for pre-triggering and DT-CONNECT. The lower 4 bits set the analog input range. The upper four bits control and provide status of enhanced features.

7	6	5	4	3	2	1	0
DT-Connect Enable	Pre-Trigger Enable	Overrun Status	Set/Read Mode	Range	Uni/Bip	G1	G0

GAINS: Gain control is identical in both compatibility and enhanced mode.

BIT 4 - Set Compatible/Enhanced Mode. Read Mode Status

WRITE: 0 = disable enhanced mode. 1 = enable enhanced mode (mode switch must be down).

READ: 0 = Switch 7 of base address switch, the mode switch, is up. It is not possible to enable enhanced features when the mode switch is up. When Bit 4 = 1, the mode switch is down and enhanced features may be enabled.

BIT 5 - Set Pretrigger, DT-Connect. Read FIFO, Over Run

READ: 0 = No over run. 1 = FIFO buffer full (> 1024 samples) or DT-CONNECT over run if DT-CONNECT is enabled. This signal is the logical OR of these two possible over run signals. To determine the source of the over run error: If DT-Connect is not enabled then the over run is FIFO. If DT-CONNECT is enabled, issue a clear to the FIFO then re-read the status bit. If it is still active then the over run was at the DT-CONNECT.

WRITE: Enable channel gain queue mode. Access to Base+2 is inhibited when the channel gain queue is enabled.

BIT 6 - Pre-Trigger Enable. Trigger Status.

WRITE: 0 = Disable pre-trigger mode. 1 = enable pre-trigger. The trigger index counter (CTR 2 of 2nd 8254) is gated to the packet interrupt. Because it is gated to the FIFO packet interrupt, the trigger flushes the FIFO at the instant of the trigger, ensuring the only samples prior to and all samples prior to the trigger are in the pre-trigger buffer.

READ: Valid only when pre-trigger is enabled. 0 = Trigger has not yet occurred. 1 = Trigger occurred.

BIT 7 - DT-CONNECT Eanble/Disable & Status

WRITE: 0 = Disable DT-Connect. 1 = Enable DT-CONNECT.
For DT-Connect to operate the Total Counter output must be forced low. The simplest way to do this is to write the value 16 to Base+19 (both decimal).

READ: 0 = DT-CONNECT is disabled. 1 = DT-CONNECT is enabled.

8.3.8 PACER CLOCK DATA & CONTROL REGISTERS

8254 COUNTER 0 DATA
BASE ADDRESS + 12 30C HEX, 780 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 1 DATA
BASE ADDRESS + 13 30D HEX, 781 Decimal

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7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 2 DATA
BASE ADDRESS + 14 30E HEX, 782 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

The three 8254 counter/timer data registers may be written to and read from. Because each counter will count as high as 64,536, it is clear that loading or reading the counter data must be a multi-step process. The operation of the 8254 is explained in the section on the counter/time and the Intel 8254 data sheet.

8254 COUNTER CONTROL
BASE ADDRESS + 15 30F HEX, 783 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

This register controls the operation and loading/reading of the counters. The configuration of the 8254 codes which control the 8254 chip is explained in the section on the counter timer and the Intel 8254 data sheet.

8.3.9 ENHANCED FEATURES PACER CLOCK DATA & CONTROL REGISTERS

8254 COUNTER 0 DATA - Total Count MS Counter
Chained from counter 1

BASE ADDRESS + 16 310 HEX, 784 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 1 DATA - Total Count LS Counter
Clocked by Pacer (See XTAL jumper) - Chained to counter 0

BASE ADDRESS + 17 311 HEX, 785 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 2 DATA - Pretrigger Index Counter

BASE ADDRESS + 18 312 HEX, 786 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

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The three 8254 counter/timer data registers may be written to and read from. Because each counter will count as high as 64,536, it is clear that loading or reading the counter data must be a multi-step process. The operation of the 8254 is explained in the section on the counter/time and the Intel 8254 data sheet.

8254 COUNTER CONTROL
BASE ADDRESS + 19 313 HEX, 787 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

This register controls the operation and loading/reading of the counters. The configuration of the 8254 codes which control the 8254 chip is explained in the section on the counter timer and the Intel 8254 data sheet.

8.3.10 CHANNEL/GAIN QUEUE CONTROL REGISTERS

Before using the channel gain queue, the board must be placed in enhanced mode. To do this, set the compatible mode switch to OFF and write a 1 to bit 4 of Base+11. Please see explainations of both elsewhere in this manual.

To enable the channel gain queue, write a 1 to bit 5 of Base + 11.

CHANNEL/GAIN MEMORY ADDRESS POINTER
BASE ADDRESS + 22 316 HEX, 790 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

The channel/gain queue is implemented with a simple 8 bit up-counter and a 256 byte memory and some control logic. Each channel/gain (C/G) pair is loaded as one byte.

The first C/G in the scan is loaded into C/G memory address 0. The second C/G in the scan is loaded into C/G memory address 1, and so on until the last C/G in the scan is the last item loaded into C/G memory.

A register stores the most recently written C/G memory address and this C/G element becomes the RESTART ADDRESS. Each time the restart address is reached, the C/G address pointer will be reset to point to address 0, which contains the first element in the C/G list.

When the A/D starts the acquisition scan, the first sample is controlled from the first entry in the C/G memory, address 0. The second sample is controlled by the second entry made in C/G memory and so on until the RESTART ADDRESS (last entry) address of C/G memory is reached, at which point the C/G memory pointer is reset to the address 0 and the sequence of C/G begins again.

The process will repeat as long as the A/D is acquiring data.

For the programmer who wants to write to the C/G memory directly, this means that you must arrange the C/G scan like so:

Order to execute	Channel	C/G Memory Address Pointer
First	3	0
Second	1	1
Third	2	2
Fourth	3	3
Fifth	4	4
Sixth (restart address)	5	5

Note also that the C/G data must be loaded into C/G memory in the order 0, 1, 2, 3, 4, 5 in the example above.

To load the C/G memory:
First write to Base + 22 to point to the C/G memory address,
then write to Base + 24 to load the C/G data into the C/G memory address

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pointed to by Base + 22.
Do this for each element in the C/G list.
The last address written to the pointer, Base + 22, is the restart address.

NOTE: If you have loaded a long series of C/G entries into the C/G memory and you want to shorten the list to use only the first N entries, simply re-write the Nth entry again. This updates the RESTART ADDRESS in the restart address register.

NOTE: Any write to this register will clear the FIFO buffer.

CHANNEL/GAIN MEMORY CONTENTS REGISTER
BASE ADDRESS + 24 318 HEX, 792 Decimal

7	6	5	4	3	2	1	0
RANGE	U/B	G1	G2	CH3	CH2	CH1	CH0

Range	Uni/Bip	G1	G0	Input Range	Decimal Gain Code*
1	0	0	0	±10V	128
0	0	0	0	±5V	0
0	0	0	1	±2.5V	16
0	0	1	0	±1.25V	32
0	0	1	1	±0.625V	48
0	1	0	0	0-10V	64
0	1	0	1	0-5V	80
0	1	1	0	0-2.5V	96
0	1	1	1	0-1.25V	112

Decimal codes are for upper four bits only. In other words, this is the correct byte to write if the channel is equal to zero. Channel values may be 0 to 15 (single ended) or 0 to 8 (differential) The code to write an input range of ±2.5V on channel 7 would be 16 + 7 = 23.

NOTE: *This table and the table of gain values shown for Base+11 and for mode 30 do not have the same decimal values. This is not an error in the manual.*

8.3.10.1

8.3.11 C/G & SAMPLE & HOLD - PIN 26

The optional sample & hold signal used to trigger a CIO-SSH16 is generated each time the C/G memory address = 0.

Of course, repeating channels within a scan list will not provide updated values for repeated channels because the CIO-SSH16 will only update all channels at once, an only when the C/G memory address is 0.

Mixing the order of the channels when a CIO-SSH16 board is attached has no effect since all channels are triggered simultaneously and only once per scan.

The C/G queue used with a CIO-SSH16 has only two possible benefits:

1) Skipping channels.

2) Applying C/G gains to achieve ranges not available from the CIO-SSH16 alone.

8.3.12 CG QUEUE GAINS AND SSH16 GAINS

External boards which provide gains, such as the CIO-SSH16 and CIO-EXP## may be used with the CIO-DAS16/330i with this caution: Just because a range is achievable by adding the accessory board gain to the main board gain does not mean that the reading will be noise free.

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For example, if a CIO-SSH16 channel were set to a gain of 800 and the CIO-DAS16/330i were set to a gain of 8, the multiplicative effect of these two gains would be 64,000. Let's take a look at that; 1.25V / 800 = 0.00156 volts for the full range. Divide that by 4096 (12 bit converter) = 0.00000038 Volts per bit. You are not going to get a decent reading in that range!

Exceeding a maximum cumulative gain of 800 is not recommended.

You can try higher cumulative gains on your own and see if you are satisfied with the results.

8.4 ANALOG INPUT

Analog signals connected to P3, the 37D connector which protrudes from the expansion slot of the PC, are first fed into the two HI-0508 analog multiplexors. A multiplexor's (MUX) function is to select on of several (8) inputs and connect that input to the MUX output. MUX U27 connects CH0-CH7 high inputs. MUX U28 connects CH0-CH7 Low input (differential input mode) or CH8-CH15 High inputs (single ended mode) depending on the state of the channel configuration switch located at the upper right of the board and marked 8/16.

From the output of the MUX, the analog signal is fed into a programmable differential amplifier.

The A/D converter chip has an integral sample & hold circuit, greatly simplifying design and improving signal integrity. The A/D converter is capable of sampling rates to 330KHz but the DMA transfer circuitry of the personal computer's 8 bit bus is limited to a maximum synchronous transfer rate of about 130KHz. Therefore the maximum sampling rate of the CIO-DAS16/330i is up to 130KHz, depending on the computer.

8.5 DIGITAL INPUT & OUTPUT

There are 4 bits of output only and 4 bits of input only on the CIO-DAS16/330i analog connector. From the original DAS-16 design these were the only 8 bits of digital I/O.

For complete programming information turn to the section on CIO-DAS16/330i registers.

8.5.1 OUTPUT

The output bits are part of chip U39, a 74LS197 output buffer. The other half of the chip is used for on board control. If the digital output lines are blown by overload or high voltage connection you may replace this chip.

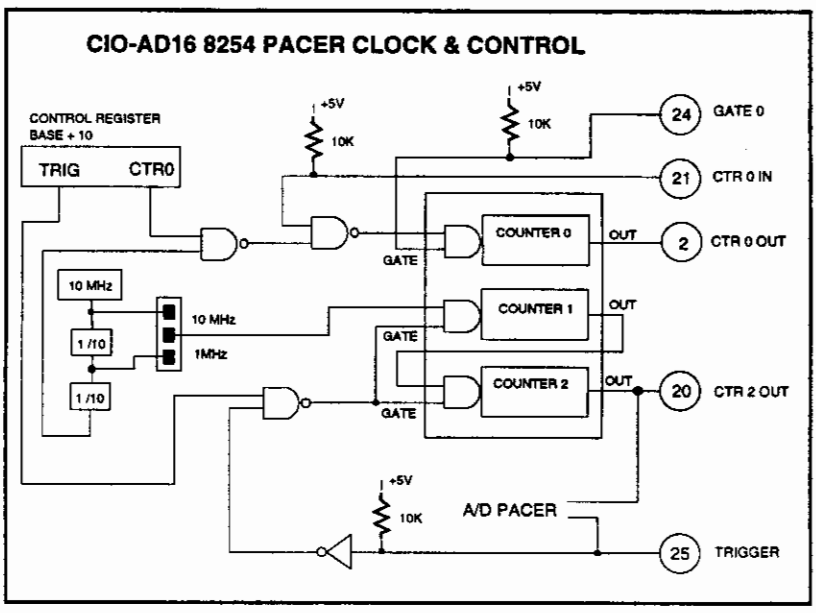
8.5.2 INPUT

The input bits are part of chip U38, a 74LS244 buffer. The other half of this chip is used for on board functions. This chip is socketed.

8.6 INTERRUPT & TRIGGER CONTROL

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The interrupt and trigger control of the CIO-DAS16/330i is accessible via programming at register BASE + 9 and is really quite simple. Interrupts are enabled by setting a bit. The PC bus interrupt number, 2-7 & 10 & 11 is register programmed. The source, either from the 8254 or external is programmed also.



BASE ADDRESS + 9 309 HEX, 777 Decimal

7	6	5	4	3	2	1	0
INTE	IR4	IR2	IR1	Don't Care	DMA	TS1	TS0

A read and write register.

READ

INTE = 1, Interrupts are enabled. An interrupt generated will be placed on the PC bus interrupt level selected by IR4, IR2 & IR1. INTE = 0, interrupts are disabled.

IR4, IR2, IR1 are bits in a binary number between 0 and 7 which map interrupts onto the PC bus interrupt levels 2 - 7. Interrupts 0 maps into 10 and interrupt 1 maps into 11.

TS1 & TS0 control the source of the A/D start conversion trigger according to the table below.

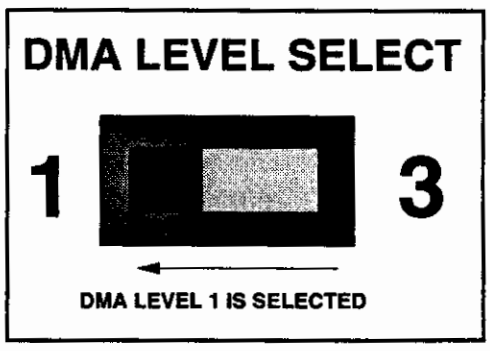
TS1	TS0	
0	X	Software triggered A/D only.
1	0	Start on rising TRIGGER (Digital input 0, Pin 25)
1	1	Start on Pacer Clock Pulse (CTR 2 OUT, no external access)

8.7 DMA CONTROL LOGIC

The Direct Memory Access (DMA) controller is on the personal computer CPU board, not on the CIO-DAS16/330i. The CIO-DAS16/330i has the logic on board to request a DMA transfer. In addition to the on board logic, the DMA controller must be programmed.

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Complete register specifications for the CIO-DAS16/330i DMA control registers will be found in the previous section on the CIO-DAS16/330i control registers.



A discussion of the CIO-DAS16/330i DMA level selection and the PC's DMA controller will be found in the section on the architecture of the PC.

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8.8 SPECIFICATIONS

POWER CONSUMPTION

+5	450mA MAX,	375mA Typical
+12	0V	
-12	0V	

ANALOG INPUT

Channels	8 Differential	16 Single Ended
Resolution	12 Bits	1 part in 4095
Accuracy	0.01% of reading, ±1 bit	
Input Range	±10V MAX	± 0.625 MIN
	See table in section on Analog Input	
Coding	Bipolar	Offset binary
	Unipolar	True binary
Overvoltage	±35V continuous	
Input Current	250 nA MAX	12 nA Min @ 25 deg C
Input Impedance	10 Meg Ohm	
Temp. Coeff.	Full Scale	±25 ppm/deg C MAX
	Zero	±12 ppm/dec C MAX
Type	Successive Approximation	
Conversion Time		3 uSec MAX
Model		
Monotonicity	Guaranteed over operating temp. range.	
Linearity	±1 Bit	
Zero drift	±10 ppm/deg C MAX	
Gain drift	±30 ppm/deg C MAX	
Vref Output	-5V ±0.05V	

PROGRAMMABLE TIMER

Type	82C54	
Counters	3, 16 Bit down counters	
	2 dedicated to A/D pacer	
XTAL	1 or 10 MHz	
Output Drive	2.2mA @ 0.45V	
Input	TTL	
Frequency	DC to 10MHz	
Active count edge	Negative	
Clock pulse width	30nSec High	50nSec Low

iSBX BUS

Rear Connector	8 Bit data bus, Full iSBX Spec.
Center Conn.	8/16 Bit Data, Full iSBX Spec.
Address	Switch Selectable
Interrupts	2, jumper selectable to 5, 7, 10 or 11
DMA	Jumper selectable to 1, 6 or 7

DIGITAL I/O

Input only	4 bits	74LS244
Output only	4 bits	74LS197
Input low volts	74LS244	0.8V MAX
Input high volts	74LS244	2.0V MIN @ 20uA
Output low volts	74LS197	0.5V MAX @ 8.0mA
Output high volts	74LS197	2.4V MIN @-0.4mA

INTERRUPT

Level	2-7, 10, 11	Software programmable
Enable	INTE Bit	CIO-DAS16/330i Control register
Trigger	On board	8254 pacer clock
	External	User supplied TTL pulse

DMA A/D TRANSFER

Level	1 or 3	Switch selectable
Enable	DMA Bit	CIO-DAS16/330i Control register
Termination	Single Cycle	Interrupt on terminal count
	Recycle	
Pacing	Internal	8254 pacer clock
	External	User supplied TTL pulse

POWER OUTPUTS

Direct from PC bus		See your PC spec.
Voltage	±5V ±5%	Depends on PC power
Loading	22AWG	64.9 Ohms/ 1000 feet

ENVIRONMENTAL

CIO-DAS16/330i	*Normal Temp Model*
Operating Temp	0 to 50 Deg C
Storage Temp	-20 to 70 Deg C
Humidity	0 to 90% non-condensing
Weight	10.25 Oz

CIO-DAS16/330i	*Extended Temp Model*
Operating Temp	-30 to 60 Deg C
Storage Temp	-165 to 150 Deg C
Humidity	0 to 90% non condensing
Weight	10.25 Oz
Dimensions	4.5" tall by 13.25" long (PC/AT full size)

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9 ANALOG ELECTRONICS

This short, simple introduction to the analog electronics most often needed by data acquisition board users covers a few key concepts. They are:

- Voltage dividers.
- Differential vs. Single Ended Inputs.
- Isolation vs. Common Mode Range
- Low pass filters for analog and digital inputs.
- A/D Resolution
- Conversion to Engineering units.
- 4-20 mA inputs
- Noise; sources and solutions.

Each deals with the impact on measurements made with data acquisition boards. If you are truly interested in the subject of data converters and analog electronics, Radio Shack has written an excellent Op Amp handbook and has an Op Amp experimenters kit.

A more advanced treatment may be found in the Analog-Digital Conversion Handbook (32.95) and the Transducer Interfacing Handbook ($14.50) published by Prentice-Hall.

9.1 VOLTAGE DIVIDERS

If you wish to measure a signal which varies over a range greater than the input range of an analog or digital input, a voltage divider can drop the voltage of the input signal to the level the analog or digital input can measure.

A voltage divider takes advantage of Ohm's law, which states,

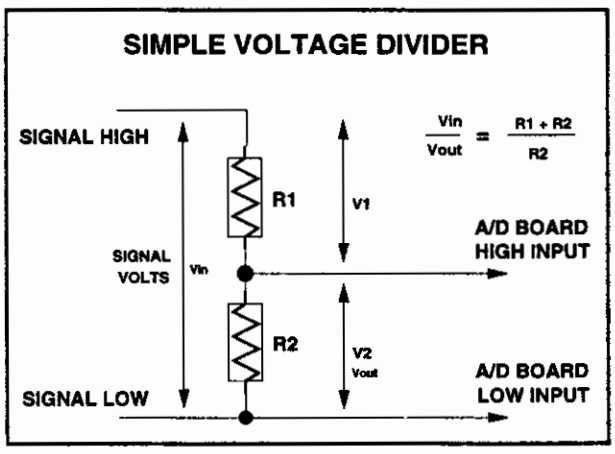
Voltage = Current * Resistance

and Kirkoff's voltage law which states,

The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

Implied in the above is that any variation in the voltage drop for the circuit as a whole will have a *proportional* variation in all the voltage drops in the circuit.

A voltage divider takes advantage of the fact that the voltage across one of the resistors in a circuit is proportional to the voltage across the total resistance in the circuit.
The trick to using a voltage divider is to choose two resistors with the proper proportions relative to the full scale of the analog or digital input and the maximum signal voltage.



The phenomena of dropping the voltage proportionally is often called attenuation. The formula for attenuation is:

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Attenuation =	R1 + R2 -------- R2	The variable *Attenuation* is the proportional difference between the signal voltage max and the full scale of the analog input.
2 =	10K + 10K ---------- 10K	For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the *Attenuation* is 2:1 or just 2.
R1 =	(A - 1) * R2	For a given attenuation, pick a handy resistor and call it R2, then use this formula to calculate R1.

Digital inputs also make use of voltage dividers, for example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to the CIO-AD digital inputs. The voltage must be dropped to 5 volts max when on. The *Attenuation* is 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 1K. Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

IMPORTANT NOTE: The resistors, R1 and R2, are going to dissipate all the power in the divider circuit according to the equation Current = Voltage / Resistance. The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit. Here is a simple rule:

For Attenuation of 5:1 or less, no resistor should be less than 10K.

For Attenuation of greater than 5:1, no resistor should be less than 1K.

The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. The CIO-TERMINAL is a 16" by 4" screw terminal board with two 37 pin D type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you may complete with the proper value components for your application.

9.2 DIFFERENTIAL & SINGLE ENDED INPUTS

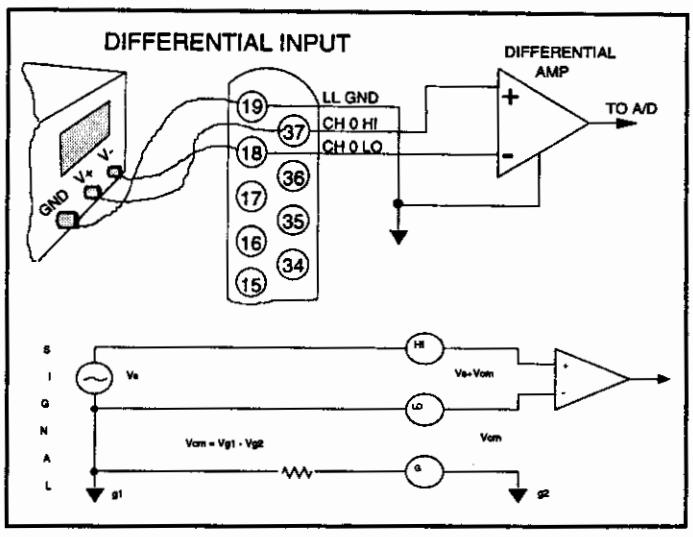
Two type of analog inputs are commonly found on A/D boards, they are differential and single ended. Single ended is the less expensive of the two.

COMMON MODE RANGE

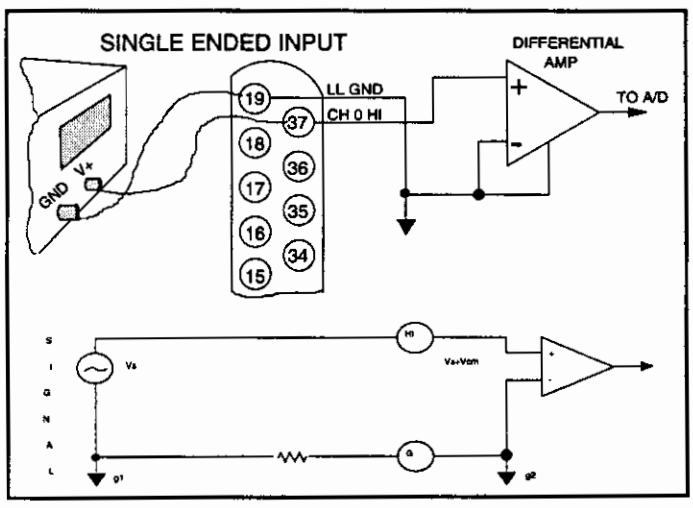
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Differential inputs have a common mode range (CMR) (Vcm). Single ended inputs have no CMR . Common mode range is the voltage range over which differences in the low side of the signal and A/D input ground have no impact on the A/D's measurement of the signal voltage. A differential input can reject differences between signal ground and PC ground.

Shown here is a CIO-DAS16/330i in differential mode.



A single ended input has no common mode range because there is only one LOW wire, which is assumed to be at the same level at the signal and at the A/D board.

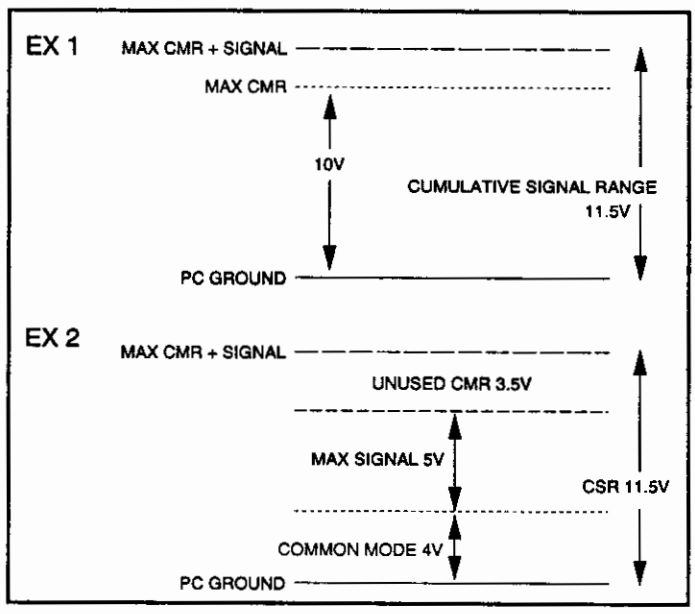


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The maximum difference which may be rejected is the CMR.

For example, the CIO-DAS16/330i has a common mode plus signal range of 11.5 volts, common mode not to exceed 10 volts.

This specification is illustrated graphically here and will be referred to as **Cumulative Signal Range (CSR)**.



Most manufactures of A/D boards specify the CMR directly from the component data sheet, ignoring the effect of the board level system on that specification. A data sheet of that type might claim 10 volts of CMR. Although this is a factual specification and the designer of the board (or other EE) would be able to translate that into a systems specification, most A/D board owners are confused or mislead by such specs.

COMMON MISUNDERSTANDINGS

The CMR specification of a differential input is often confused with an isolation specification, which it is not. It makes sense. doesn't it, that 10 volts of CMR is the same as 10 volts of isolation? No. The graph above shows why.

Also, failure to specify the common mode plus signal *system* specification leads people to believe that a DC offset equal to the component CMR can be rejected regardless of the input signal voltage. It cannot as the graph above illustrates.

When is a differential input useful? The best answer is whenever electromagnetic interference (EMI) or radio frequency interference (RFI) may be present in the path of the signal wires. EMI and RFI can induce voltages on *both* signal wires and the effect on single ended inputs is generally a voltage fluctuation between signal high and signal ground.

A differential input is not affected in that way. When the signal high and signal low of a differential input have EMI or RFI voltage induced on them, that ***common mode voltage*** is rejected, subject to the system constraint that common mode plus signal not exceed the A/D board's CSR specification.

GROUND LOOPS

Ground loops are circuits (E=I*R) created when the signal ground and the PC ground are not the same. Ground loop inducing voltage differential may be a few volts of hundreds of volts. They may be constant or transient (spikes). A differential input will prevent a ground loop as long as the CSR specifications is not exceeded.

If ground differences greater than the CMR are encountered, isolation is required.

WHY USE SINGLE ENDED?

Unanswered still is the question of why use single ended inputs? First, single ended inputs require fewer parts so they cost less money. On an A/D board the parts cost to go from 16 single ended channels to 16 differential channels is about $6.00 so that cannot be the reason. The real reason is connector space. Single ended inputs require one analog high input per channel and one LLGND shared by all inputs. Differential inputs require signal high and signal low inputs for each channel and one common shared LLGND.

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Single ended inputs save connector space, parts cost and in all cases where there is no common mode or EMI/RFI they work just as well as differential inputs and are less complex to wire up.

9.3 LOW PASS FILTERS

A low pass filter is placed on the signal wires between a signal and an A/D board. It stops frequencies greater than the cut off frequency from entering the A/D board's analog *or* digital inputs.

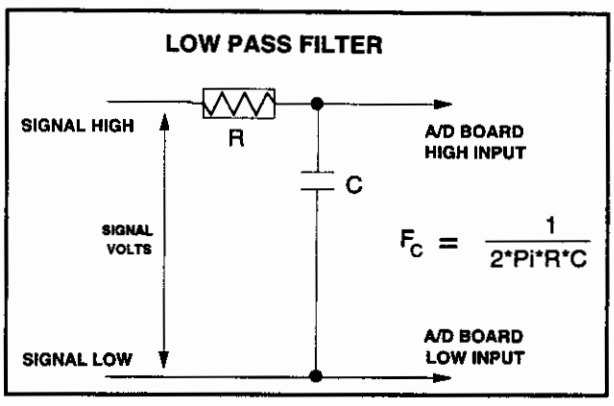
The key term in a low pass filter circuit is **cut off frequency**. The cut of frequency is that frequency above which no variation of voltage with respect to time may enter the circuit. For example, if a low pass filter had a cut off frequency of 30 Hz, the kind of interference associated with line voltage (60Hz) would be filtered out but a signal of 25Hz would be allowed to pass.

Also, in a digital circuit, a low pass filter might be used to de-bounce an input from a momentary contact button pushed by a person.

A low pass filter may be constructed from one resistor (R) and one capacitor (C). The cut off frequency is determined according to the formula:

$$F_c = \frac{1}{2 * Pi * R * C}$$

$$R = \frac{1}{2 * Pi * C * F_c}$$



9.4 A/D RESOLUTION & ENGINEERING UNITS

Resolution is specified in bits, such as 8, 10 or 12 bits. The 12 bits are really a power of 2 indicating the number of divisions of full scale the converter can resolve. For example, a 12 bit converter can resolve (2^12 - 1) = 4095 divisions of full scale. If the input of the board were +/- 5 volts full scale, each of the 4095 steps would be equal to 0.00244 volts.

Reading from the A/D converter would be thus:

Converter #	Volts
4095	5.0
4094	4.9976
4093	4.9951
2028	0.0
1	- 4.9976
0	- 5.0

The concept of resolution is the ability to differentiate between one voltage and another. Obviously, the more bits of resolution (13 bits = 8192 counts) the more divisions of full scale. The more divisions of full scale the finer the measurement.

ENGINEERING UNITS

When a program uses an A/D board to acquire data, the data file is filled with numbers like those above.

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To translate the A/D numbers back into the engineering units of the original measurement, we need to know:

The sensor's voltage output per engineering unit.

The full scale range of the board at the time the measurement was made.

The resolution of the converter.

Here is an example from the application note on interfacing a Voland TA to a PC found elsewhere in this manual.

The TA measures resistance in grams between +500 and -500 grams.

The voltage output of the instruments is +2.5 volts to -2.5 volts.

The voltage output corresponds to the grams of pressure exactly, so:

+/- 500 grams = 1000 grams.

+/- 2.5 volts = 5 volts.

5 volts / 1000 grams = 0.005 volts per gram.

The A/D was set for +/- 2.5 volts = 5 volts full scale.

5 volts / 4095 counts = 0.00122 volts per bit.

If the number in the file for one reading was 3061, then

3061 * 0.00122 = 3.7632 volts.

3.7632 volts / 0.005 volts per gram = 735 grams.

Now shift from full scale to +/- scale.

735 grams full scale - 500 = 235 grams of positive pressure.

It may look like a lot of steps because it is presented that way here for clarity only. It could be expressed as a single equation in a spreadsheet.

9.5 CURRENT LOOP 4-20 mA

Although the inputs of a CIO-AD board are voltage inputs, it is easy to convert a current to a proportional voltage which may be measured by the CIO-AD board. The current is converted to a proportional voltage by the formula V=I*R.

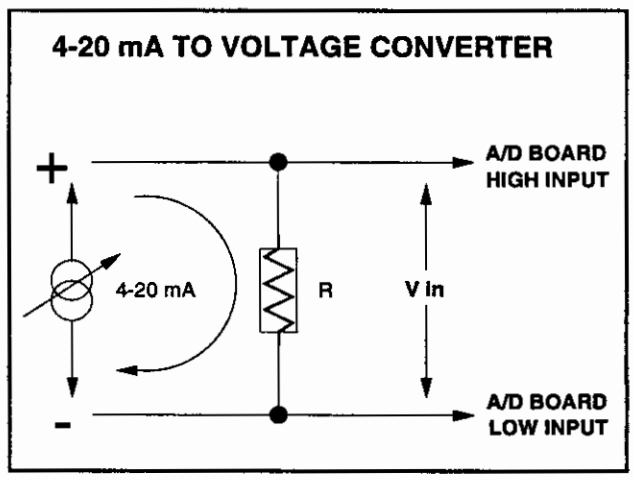
For example, if the CIO-AD board is set up to read 0 to 5 volts, then:

5 volts / 0.02 Amps = 250 Ohm shunt resistor.

So a full 20 mA will register 5 volts and 4 mA will register 1 volt.

To hook up the CIO-AD analog inputs to a 4-20 mA transducer or signal source, place the shunt resistor across the plus and minus terminals or signal wires of the 4-20 mA. Once the resistor is in place, connect the analog input CH# Hi to the plus terminal and the analog input CH# Lo to the minus input.

If they are backward, the A/D reading will be 0 or minus volts. Just reverse the connection.



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9.6 NOISE

Noise is unavoidable in PC based data acquisition systems. There is board induced noise which can be measured by shorting an analog input to ground and taking a series of readings and plotting them in a histogram. There is EMI and RFI induced noise along the path of the signal wires. There is also noise at the signal source itself. All these sources of noise combine to create a region of uncertainty around the signal value.

Our objective here is to discover the sources of noise and discuss the means to reduce it.

SOURCES OF NOISE

The first source of noise is the board itself. Manufacturers of A/D boards quote component specifications in their data sheets but rarely quote a system specification for general accuracy and noise. The reasons the system is not specified are that the system specification would be less accurate than component specification and that system specifications must also specify the conditions under which the specification was made. That means the PC, the PC's power supply and the connection to the front end.

No one likes to admit it but it is true. Take some very good components, put them on a circuit board and place that board in a PC and the **system** will be less accurate than the individual components. I have seen 12 bit A/D boards with the same components as a DAS-16 with as little as 9 bits of accuracy, due to board noise.

The system specification for the CIO-DAS16/330i and CIO-AD08 is plus or minus 1 LSB. That means that if an analog input is tied to ground and the CIO-DAS16/330i is on a bipolar scale, the reading will be 2048 90% of the time. The other 10% of the readings will be 2047 and 2049, which is +/- count (LSB). This is actually not very different from the component specifications.

You can verify this by grounding an analog input channel to LLGND and taking 1000 readings then plotting a histogram of those readings.

If your histogram is not +/- 1 LSB, check the +/- 12V PC power supply voltages or call Computer Boards' Tech Support.

SIGNAL WIRE NOISE

Signal wires, especially single ended inputs, are subject to EMI and RFI, both of which can induce noise on the wires carrying the transducer signal to the CIO-AD board. Fortunately, signal wire noise is often localized and can be reduced by repositioning the signal wire run.

To check for signal wire noise, first, short analog channel 0 to low level ground[6] at the connector and take 10,000 samples and plot the histogram. This is the best the signal can be and is what you will try to achieve with the signal wires in place.

After you have an ideal case histogram, remove the short between analog input 0 and low level ground. Attach the signal wires to the CIO-AD board inputs and run them to the sensor. Do not connect the sensor yet, just short the analog input(s) to LLGND.

Take data for the histogram and compare it to the best case data taken previously. If it shows noise, you can try to eliminate the noise by doing the following:

- Move the signal wires, trying to locate a 'quiet' run.
- Use a shielded twisted pair as the signal wire. Attach the shield at the PC **only.** If the shield is attached at both the PC and the sensor it may create a ground loop and add to signal interference.

SENSOR NOISE

When the signal wires have been tested and characterized for signal quality, connect the sensor and provide a known level to the sensor (ice bath for temp., etc.) then take data for the histogram plot. If additional noise has been introduced by the sensor *which exceeds the sensor specifications*, you can try moving the sensor or electrically isolating it from the device it is measuring.

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6 Differential inputs must have CH Hi, CH Lo and LLGND shorted. Single ended inputs must have CH Hi shorted to LLGND.

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SMOOTHING DATA

It is not always possible to eliminate all noise, especially with very low level sensors, but noise looks terrible when plotted and can raise doubts about otherwise excellent data.

There are two simple ways to eliminate noise from the data:

1) Apply a moving average to the data if you want to retain the same *apparent* accuracy.

2) Remove the information from the noisy range. For example, if the A/D is capable of , or, shift the data by the number of counts of noise. For example, if a 12 bit A/D converter is at +/- 5 volts (10 volts full scale) then one LSB = 10 / 4095 = 0.00244mV. If your system is inducing +/- 0.007mV of noise (+/- 3 counts), then just round all the readings by +/- 3 counts. In this way the reading's value reflects the true accuracy of the system.

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10 DIAGNOSIS & DEBUG

Computer Boards maintains technical support lines staffed by experienced Electrical Engineers and Technicians. There is no charge to call and calls are returned promptly if you have called when the lines were busy.

Most of the problems encountered with data acquisition plug in boards can be solved over the phone.

Signal connection and programming are the common sources of difficulty and Computer Boards' Tech Support people can solve these type of problems with you, especially if you prepare for the call.

1) Have the phone near the PC where you can try the things we suggest.
2) Be prepared to open the PC, remove the board and read back or change switch and jumper settings.
3) Have a volt meter available to make measurements of the signals you are trying to measure and the signals on the board and PC power supply.
4) Isolate the program lines that are not working as you expect them to.
5) Have all the source code to the program you are having trouble with so preceding modes and prerequisite modes may be discussed.
6) Have the manual ready.
7) Have the CIO-ADXX Utility diskette available so the revision # and programs can be checked.

THIS LITTLE BIT OF PREPARATION WILL SPEED DIAGNOSIS AND MAY SAVE YOU THE TROUBLE OF A CALL BACK.

PLEASE,

NO RETURNS

WITHOUT RMA NUMBERS

CALL (508) 261-1123

Please, and here is why.

It slows down the solution of your problem.

If we receive a return without an RMA number written on the outside of the box, a Tech Support person will call you before any work is done so we can determine the reason for the return.

We need to know what you want us to look for.

The RMA system is fully automated and all the Tech Support engineers have access to the information in it. They can track your RMA and discuss your return history with you. This is very valuable if the setup you are using is overloading inputs. We can spot that and discuss a solution.

HARSH ENVIRONMENT WARRANTY™

If a *Compatible I/O Series*™ board has been short circuited and visibly burnt or otherwise damaged beyond repair, return the board to us with an order for a replacement. There is a very large discount on the replacement which is specified in the current *Compatible I/O Series*™ catalog.

The entire CIO board must be returned with all components in place with a purchase order for the replacement.

I/O boards are used in harsh environments and they do get damaged by misconnection. We understand that and do not want to make a profit from your misfortune.

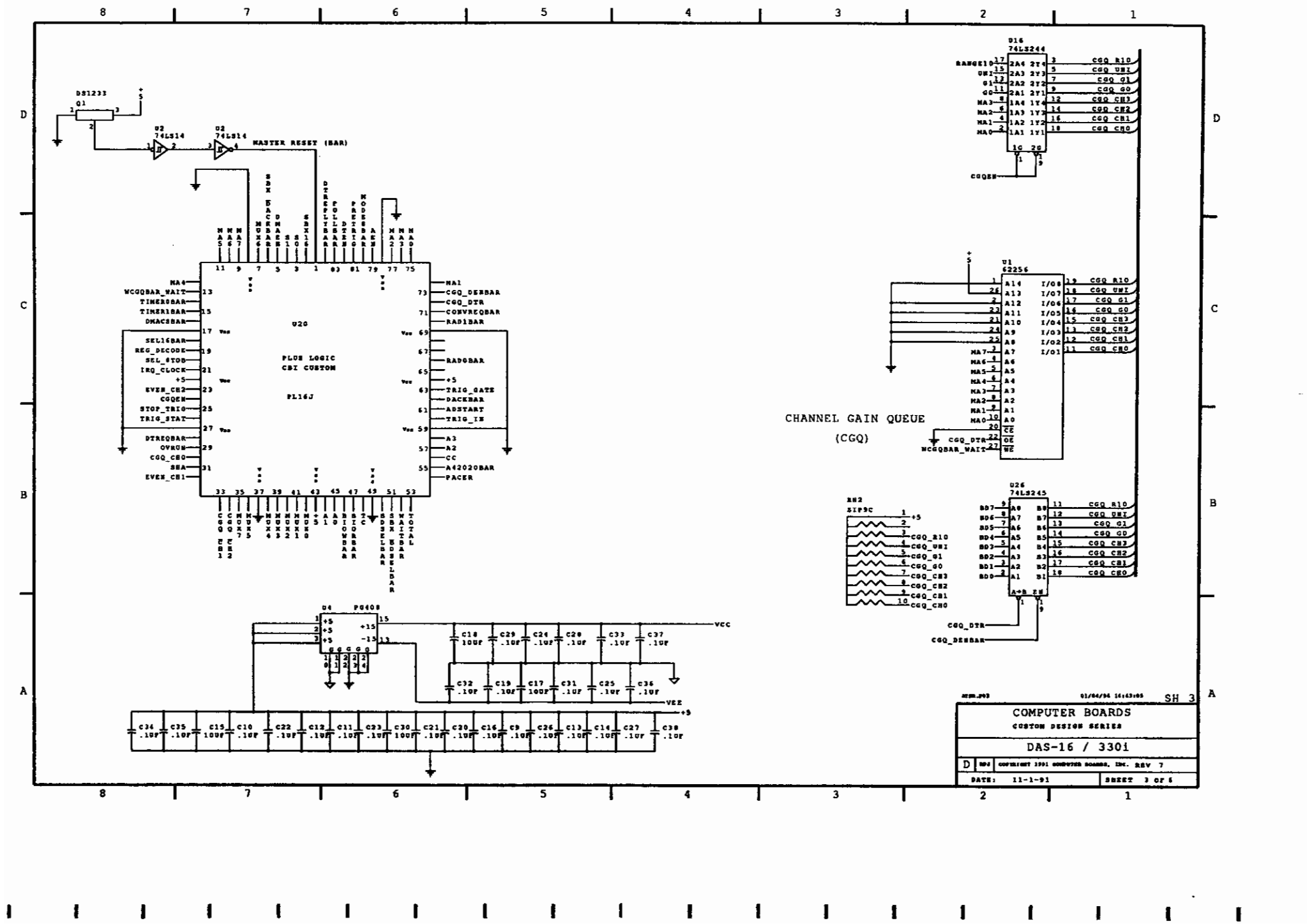
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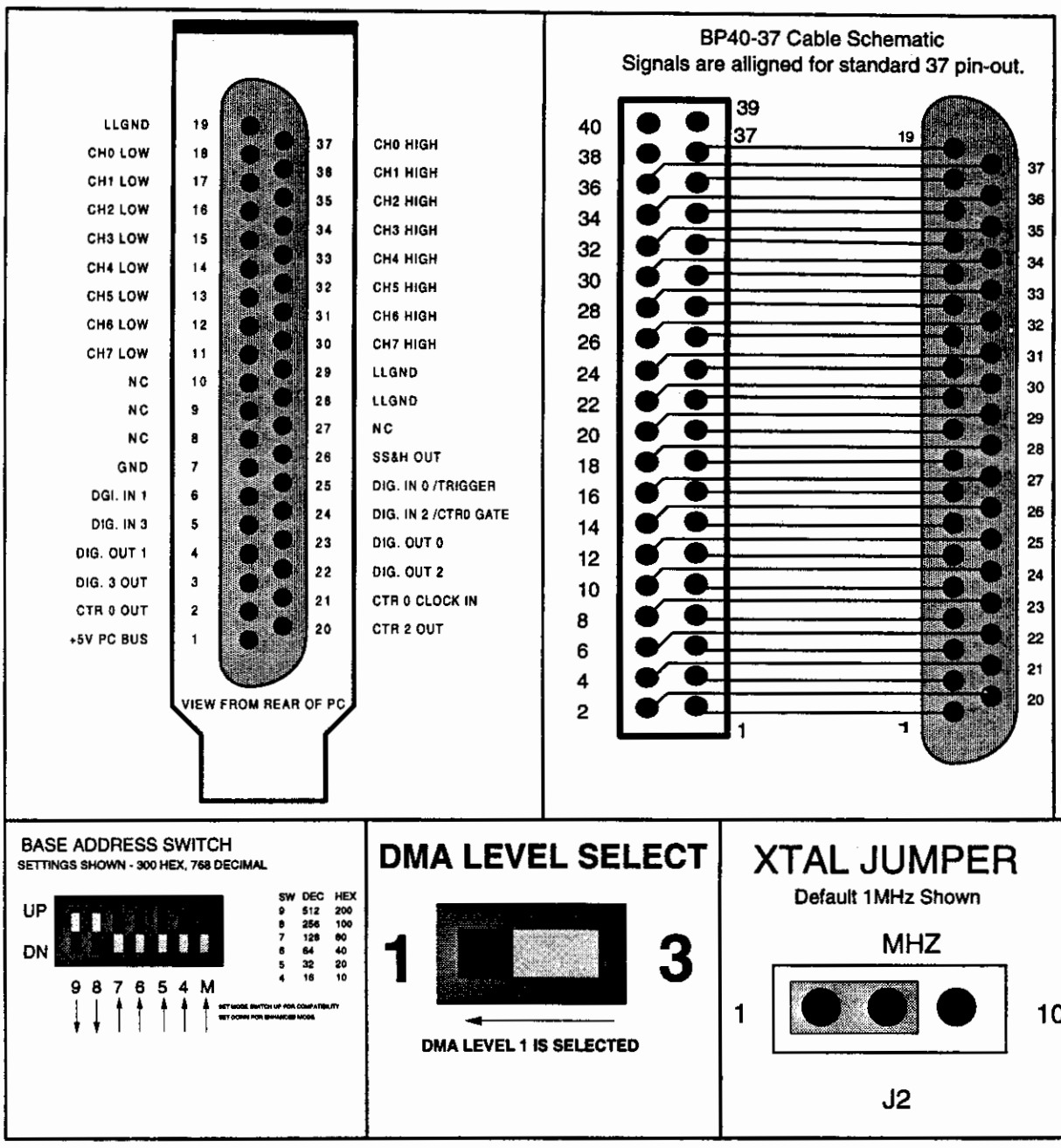
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