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CIO-DAS1600

USER'S MANUAL

REVISION 3, JANUARY 1994

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1 QUICK START

For simplicity sake, the name CIO-DAS1600 is used for CIO-DAS1601/12, Cio-DAS1602/12 and CIO-DAS1602/16. Where needed, specific board names are used.

The CIO-DAS1600 is easy to use. Here is the quick start procedure for those who know how to open the PC and install expansion boards, and want to dive right in.

BOARD SETUP

The CIO-DAS1600 is setup at the factory with:

BASE ADDRESS	300H (768 Decimal) Same as data sheet.
DIO 24 ADDRESS	Fixed at BASE + 400H
DMA CHANNEL SELECT	1 Choices are 1 & 3. 3 is used by the hard disk in an XT.
1/10 MHz jumper	1 MHz
8/16 CHANNEL SELECT	8 Differential input channels.
GAIN/RANGE	+/- 5 volts - Programmable gain default.
D/A REF JUMPER	Internal - 0-5V range for D/As
D/A RANGE	+/-5V
BURST MODE	Not Enabled is programmable default.

Open your PC (after turning off the power) and install the board. Leave the switches as they were set at the factory or refer to the data sheet to change the settings. They are described in detail on the data sheet and in this manual.

After the board is installed and the computer is closed up, turn the power back on.

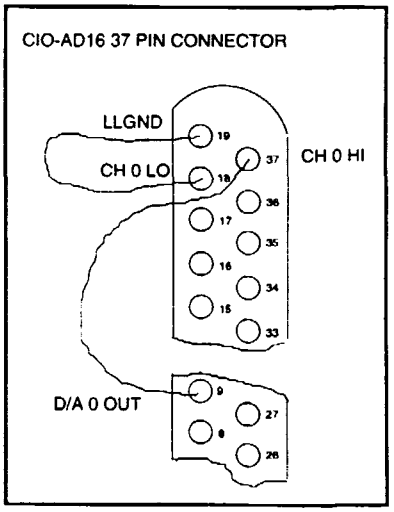
SIGNAL CONNECTION

The board is factory configured in differential input mode. Differential Input mode requires 3 connections be made from the signal source to the CIO-DAS1600. These are SIGNAL HIGH, SIGNAL LOW & GROUND.

To test the analog inputs you need a known signal to connect to them. The simplest signal to connect is the Analog Output 0 from the CIO-DAS1600.

The analog inputs are on the 37 pin connector which extends through the faceplate out the back of the PC when the board is installed.

Using the shorting wires supplied with the board, short pin 18 to pin 19, and pin 37 to pin 9 as shown to the right.



Run the program 'IOTEST' on the CIO-DAS1600 utility disk. Select output channel DA0 as signal source and input channel AD0 for input select.

You should see a slow moving sine wave on the screen.
The CIO-DAS1600 is installed and running correctly. You may now run other programs from the utility disk.

2 INSTALLATION

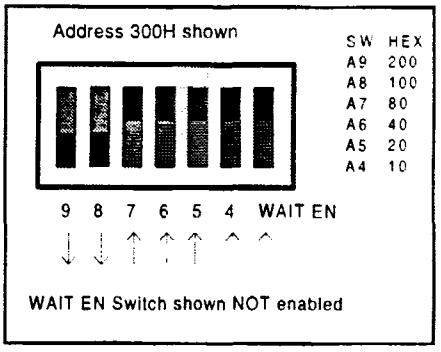
The CIO-DAS1600 has switches and jumpers which must be set before installation of the board inside your computer. Refer to this manual for switch settings other than factory default.

To run the calibration and test program, first install the software included on the CIO-DAS1600 Utility disk by following the instructions in the file READ.ME

2.1 BASE ADDRESS

Unless there is already a board in your system which uses address 300 HEX (768 Decimal) then you can leave the switches as they are set at the factory.

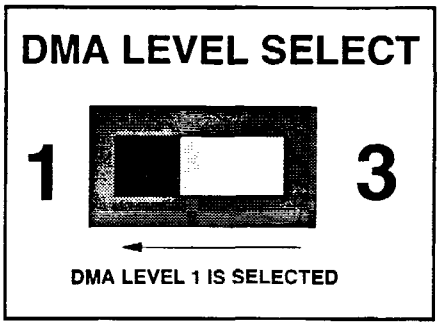
In the example shown here, the CIO-DAS1600 is set for base address 300H. That means the DAS-16 compatible section of the board is at 300H and the PIO-12 compatible section of the board is at 700H



2.2 DMA LEVEL SELECT

What kind of computer are you installing the board in? If it is an XT then there are only two DMA levels available and level 3 is probably used by the hard disk controller in your XT computer. Set the DMA level switch to the level 1 position.

If you have an AT or 386 type computer the hard disk controller is not at level 1 or 3 so either level may be used.



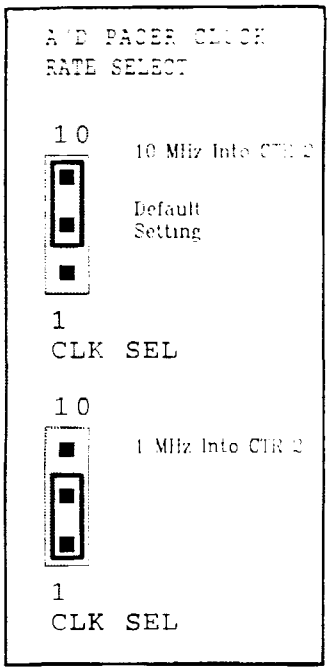
There are other boards that use DMA levels. Some network boards do and so do some IEEE-488 interface boards. Do you have other boards in your computer with DMA level switches on them?

2.3 1/10 MHz XTAL JUMPER

The 1/10 MHz XTAL jumper selects the frequency of the square wave which is connected to OUT 2, the output of 8254 counter 2. Counter 2 is used to pace the A/D start conversion trigger.

Why is this jumper on the board? Because the original DAS-16, designed in 1984, had a 1 MHz crystal. When MetraByte redesigned the DAS-16 and added the faster 10MHz crystal, a jumper was provided to maintain compatibility with older software. The CIO-DAS1600 has the jumper because the DAS-16 has the jumper and some software expects the jumper to be in the 1 MHz position and some software expects the 10 MHz position.

The CIO-DAS1600 is shipped with the jumper in the 1 MHz position. The BASIC CALL routine, CIO16, allows you to specify a 1 or 10 MHz position in the setup. Certain MODES, 50 and 51 for example, allow the sample rate to be specified in Hz rather than having to independently set the counter speed. To calculate the counter load values the counter 2 input frequency must be known.

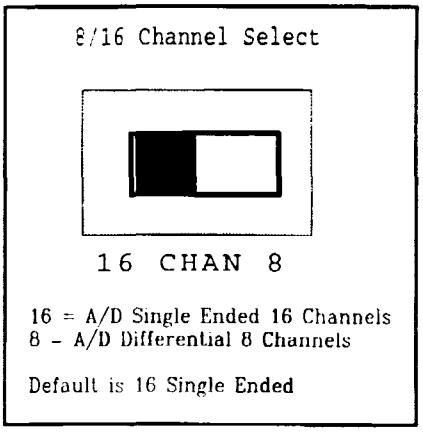


Some software programs, such as UNKELSCOPE, ASYST and ASYSTANT+ require that the jumper be in the 1MHz position. Please refer to the software program user's manual for guidence. Other programs, such as Labtech Notebook, have a 1/10MHz choice in the set-up menu.

2.4 8/16 CHANNEL SELECT

The analog inputs of the CIO-DAS1600 may be configured as 8 differential or 16 single ended. Using single ended inputs means you have more separate analog input channels available to connect signals. Using differential inputs allows up to 10 volts of common mode (ground loop) rejection and can be more noise immune.

The CIO-DAS1600 comes from the factory configured for 8 differential inputs so the 8/16 switch is in the position shown here. Set it for the type and number of inputs you desire.



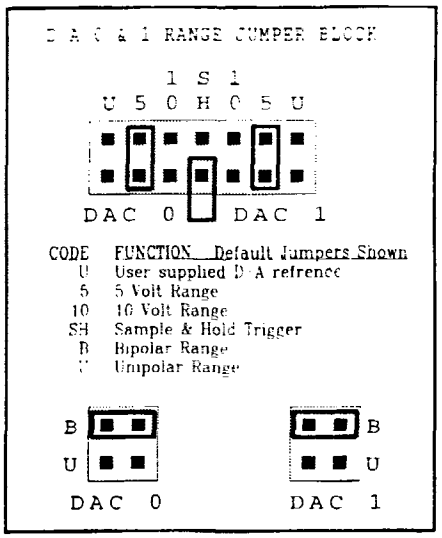
2.5 D/A CONVERTER REFERENCE JUMPER BLOCK

There is a jumper block located top center on the CIO-DAS1600. This block allows you to use the on board precision voltage reference to provide reference to either or both of the digital to analog converters.

Analog output is provided by two 12 bit multiplying D/A converters. This type of converter accepts a reference voltage and provides an output proportional to that. The proportion is controlled by the D/A output code (0 to 4095). Each bit represents 1/4095 of full scale.

A precision -5V and -10V reference provide on-board D/A ranges or 0-5V, 0-10V, +/-5V, +/-10V. Other ranges between 0V and 10V are available if you provide a precision voltage reference at pin 10 or 26 of the D/A connector.

Assuming the DAC0 reference is supplied on-board, pin 26 of the 37 pin connector is unused and may be employed as a simultaneous sample & hold trigger for use with the CIO-SSH16. To do so, place the jumper between the two pins 'SH'



2.6 RANGE AND GAIN SETTING

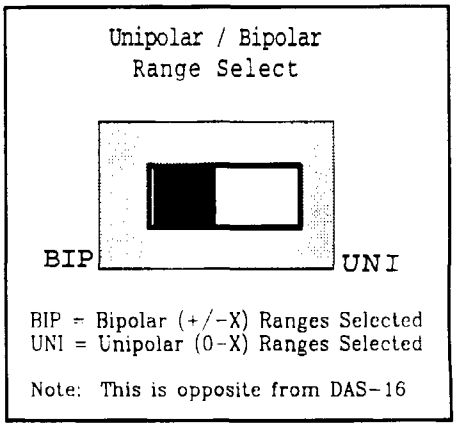
Range is controled by a switch and gain is controlled by a register located at BASE + A hex (11 decimal). The codes have different meaning for each board in the DAS1600 family

BOARD	CODE	BIPOLAR RANGE	UNIPOLAR RANGE
CIO-DAS1601/12	0	+/-10V	0-10V
	1	+/-1V	0-1V
	2	+/-0.1V	0-0.1V
	3	+/-0.01V	0-0.01V
CIO-DAS1602/12	0	+/-10V	0-10V
	1	+/-5V	0-5V
and	2	+/-2.5V	0-2.5V
CIO-DAS1602/16	3	+/-1.25V	0-1.25V

The range, unipolar or bipolar is controlled by a switch.

This switch is an artifact of old DAS-16 technology and should never have been designed into the DAS-1600. That it was designed into the DAS-1600 is unfortunate, but, since the CIO-DAS1600 is a perfect clone of the DAS-1600, we had to follow this scheme.

If your application is better served by programmable ranges, please consider the CIO-DAS16/Jr or CIO-DAS16/330 boards.



2.7 TRIGGER EDGE SELECT

This one baffles us. Why in the world would the DAS-1600 have been designed with a falling edge A/D trigger?

That is not how the original DAS-16 worked, nor how any other DAS-16 derivative works. In fact, we are not aware of *any* A/D board that uses a falling edge trigger.

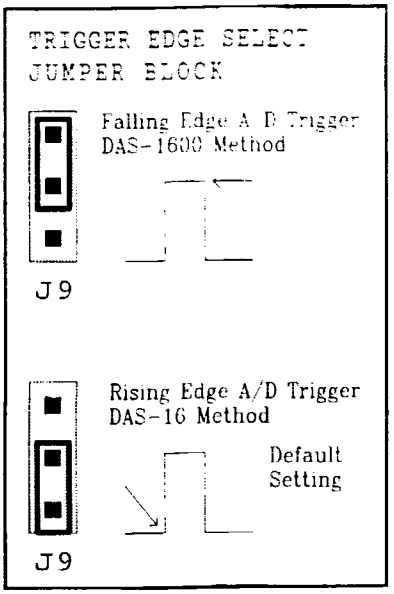
Because the falling edge trigger is such a bad idea, we have designed a jumper into the CIO-DAS1600 which allows you to select a rising or falling edge. The CIO-DAS1600 is shipped with this jumper in the rising edge position.

The only reason to supply you the option of a falling edge trigger is in the sorry case that you have developed software for a DAS-1600 using the AS-1600 drivers, AND, when using the CIO-DAS1600 with that software you observe sample timing differences.

You see, using the falling edge trigger, the A/D may be falsly triggered by 8254 pacer clock initialization glitching (easy to avoid but present in the DAS-1600), and to differences between the rising and falling edge.

The diagram shows this graphically.

For compatibility with all third party packages and with all DAS-16 software and with CIO-DAS1600 software. Leave this jumper in the rising edge position.



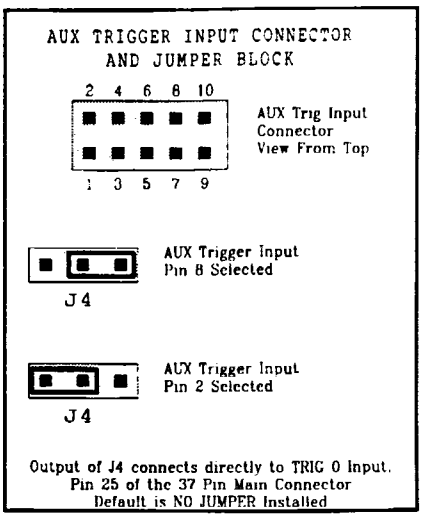
2.8 AUXILLARY TRIGGER

There is a position for a header connector at the rear of the CIO-DAS1600. This connector provides the same function as that found on the DAS-1600.

The A/D trigger signal may come from this connector, if installed. A jumper controls which pin the trigger signal comes in from.

We do not install this connector (neither is it installed on the DAS-1600).

If someone knows what it is for, or wants to use it. Call the factory and ask for technical support.



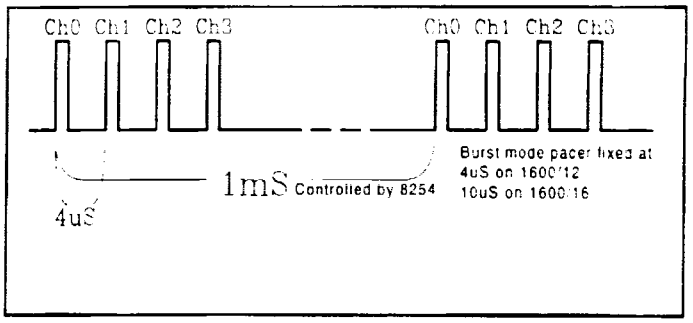
2.9 BURST MODE GENERATOR

The burst mode generator is a clock signal that paces the A/D at the maximum multi channel rate so that the channel to channel skew (time between succesive samples in a scan) may be minimized.

Burst mode must be enabled by a sequence of instructions to control registers. Those wishing to use burst mode should acquire the Universal Driver software.

The CIO-DAS1600 burst mode generator takes advantage of the fast A/D. The burst mode skew is 4uS between channels for the CIO-DAS1600/12.

It is 10uS for the CIO-DAS1600/16.



2.10 DT-CONNECT

There is nothing to install on the DT-Connect. Software enables or disables DT-Connect, and of course, you must have a DT-Connect equipped accessory before using the DT-Connect.

Please see the data sheet on the MEGA-FIFO, 128 million sample buffer board as an example of a DT-Connect accessory.

DT-CONNECT IN MASTER MODE ONLY

The CIO-DAS1600 impliments DT-Connect MASTER MODE only. DT-Connect is always enabled and is never busy. The ENABLED and BUSY signal levels are fixed in hardware. Since DT-Connect is always enabled, any A/D conversions are always transfered out the DT-Connect regardless of the bus transfer method specified.

The CIO-DAS1600 can only operate in DT-Connect schemes where it is the sole master.

To guaranty that DT-Connect is properly initialized prior to any A/D transfer, the DT-Connect DT-Request handshake line is reset each time the programmable gain (Base + 11) register is written to. Therefoe, it is not possible to use the DT-Connect for A/D sets which involve setting the gain between samples. This is not really a problem because any such scheme would be low speed and therefore store data to disk, obviating the need to use DT-Connect to store data on the MEGA-FIFO.

2.11 SIGNAL CONNECTION TO TEST THE INSTALLATION

To test the installation of the CIO-DAS1600 there must be electrical signals for it to read and display. You can supply the signal with a function generator or other voltage source or you can loop-back the CIO-DAS1600 output signals onto the CIO-DAS1600 inputs.

Please, before you connect a voltage from a signal generator or other source, be sure that the signal does not exceed +/- 10V, the maximum analog input range of the board, or 0-5V, the maximum digital input range. The analog inputs are protected to 30V but why prove it.

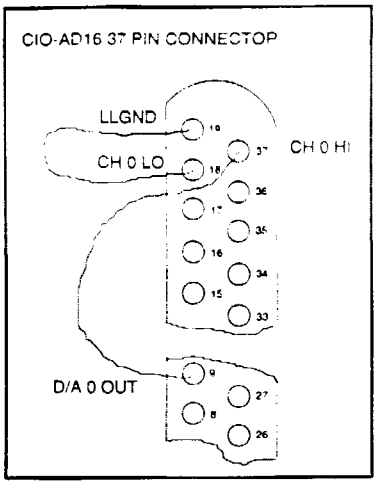
Supplied with the CIO-DAS1600 are some wires with plugs on each end. These are intended to be plugged directly on the CIO-DAS1600 37 pin connector for loop-back testing. If you purchased a screw terminal then connect it up and use it instead[1].

To test the installation of the CIO-DAS1600 the D/A 0 output will be looped back into the A/D 0 input.

If you are using a signal generator feed the signal directly into A/D channel 0.

The CIO-DAS1600 is ready to test. You can try running the software supplied with your board now, or you can continue reading the next two sections on Software Installation and Calibration.

The program IOTEST will display the loopback D/A into the A/D on a strip chart on the screen.



1 The CIO-TERMINAL and CIO-MINITERM are fully explained in the appendix. Briefly, the connector numbers on the screw terminals correspond to the numbers on the CIO-DAS1600 37 pin connector.

3 SOFTWARE INSTALLATION

InstaCal is an installation, calibration and test package. Use it to guide the installation procedure and to calibrate your data acquisition board. InstaCal also creates a configuration file required for programmers who have purchased the Universal Library programming libraries.

Use the calibration option to verify the installation.

IOTEST may also be used to verify the installation. It exercises the CIO-DAS1600 by stimulating the analog and digital output ports and reading the analog and digital inputs. The inputs are displayed on the screen on a line graph.

IOTEST can provide one output and read one input at a time. The activity on an output channel is fixed by the program. Analog output 0 and 1 produce a sine wave. Digital outputs produce a square wave. Counter outputs produce a square wave.

4 CALIBRATION AND TEST

FREQUENCY OF CALIBRATION: Every board was fully tested and calibrated before being placed in finished goods inventory at the factory. For normal environments a calibration interval of 6 months to one year is recommended. If frequent variations in temperature or humidity are common then recalibrate at least once every three months. It takes less than 30 minutes to calibrate the CIO-DAS1600.

4.1 REQUIRED EQUIPMENT

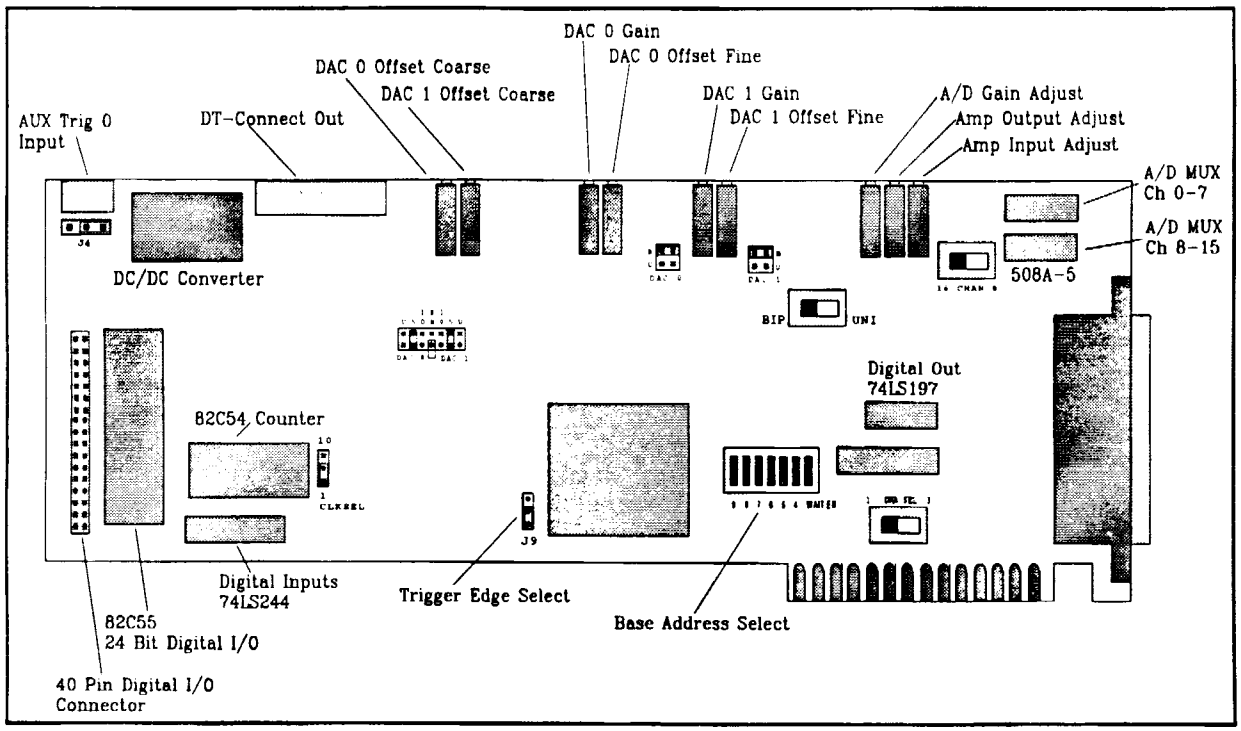
Ideally, you will need a precision voltage source, a 4 1/2 digit digital volt meter, a calculator and some pieces of wire. If you do not have a precision voltage source, you will need a non-precision source and have to make a few calculations.

You will not need an extender card to calibrate the board but you will need to have the cover off you computer with the power on, so trimpots can be adjusted during calibration. For that reason a plastic screwdriver has been supplied with your CIO-DAS1600. In the event that the screwdriver is dropped into the PC, no damage will result from short circuits.

4.2 CALIBRATING THE ANALOG INPUTS

The A/D is calibrated by applying a known voltage to any analog input channel and adjusting trimpots for offset and gain. There are three trimpots requiring adjustment to calibrate the analog input section of the CIO-DAS1600. These are the AMP INPUT ADJUST, AMP OUTPUT ADJUST, and GAIN ADJUST.

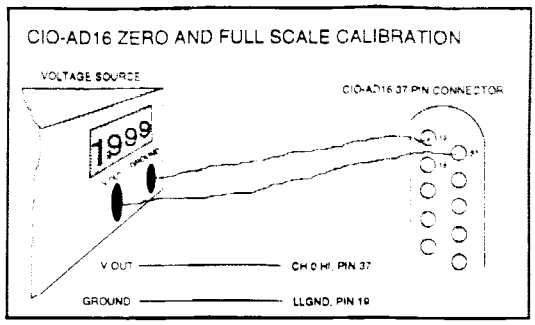
The CIO-DAS1600 should be calibrated for the range you intend to use it in. When the range is changed, slight variation in Zero and Full Scale may result. These variations can be measured and removed in software if desired.



Amp Output Adjust: Set the 8/16 switch for 16 channels differential input. Connect the V Out from your calibrator to CH0 High (pins 37), connect the calibrator ground to LLGND (pin 19). Switch the calibrator output to 0 volts, adjusting the Amp Output Adjust potentiometer until the A/D counts read 0.

Amp Input Adjust: Set the 8/16 switch for 16 channels single ended input. Connect the V Out of the calibrator to CH0 High (pin 37), connect the calibrator ground to LLGND (pin19).

Apply 0 volts and adjust the Amp Input Adjust potentiometer until the A/D counts read 0.



Full Scale Adjust (Gain): Set the 8/16 switch for 16 channels single ended input. Connect the V Out of the calibrator to CH0 High (pin 37), connect the calibrator ground to LLGND (pin19).

Apply a voltage of 1LSB below full scale and adjust the A/D Full Scale Adj pot.

Range	CAL Volts (12 bit)	A/D Counts	Cal Volts (16 b)	A/D
0 - 10V	9.99756V	4095	9.999847	65535
0 - 5V	4.99878V	4095	4.999924	65535
0 - 2.5V	2.4994V	4095	2.49996	65535
0 - 1.25V	1.2497V	4095	1.249981	65535
±10V	9.99522	4095	9.999695	65535
±5V	4.99756	4095	4.999847	65535
±2.5V	2.49878	4095	2.499924	65535
±1.25V	1.2494	4095	1.24996	65535

4.3 CALIBRATING THE ANALOG OUTPUTS

Calibrate the Digital to Analog converters using the on board -5Vref. The Vref jumpers are factory installed in the 'I' position so there are no wire hookups required to calibrate the D/A. If you are using an external Vref, place the Vref jumpers in the 'U' position to calibrate the D/As.

D/A #	COUNTS	ADJUST POT	OUTPUT DESIRED
Bipolar			
0	2048	D/A 0 Offset Coarse/Fine	0
0	4095	D/A 0 Gain	4.9988V
1	2048	D/A 0 Offset Coarse/Fine	0
1	4095	D/A 1 Gain	4.9988V
Unipolar			
0	0	D/A 0 Offset	0
0	4095	D/A 0 Gain	4.9996
1	0	D/A 1 Offset	0
1	4095	D/A 1 Gain	4.9996

Notes for unipolar calibration:

The D/A offset pot is the bipolar offset fine.

The D/A gain pot is the bipolar offset coarse.

The D/A bipolar gain pot is not used in unipolar.

4.4 TESTING THE COUNTER/TIMER & DIGITAL I/O

There is no calibration to be performed on the counter timer, which is crystal controlled, or the digital I/O, which are TTL.

InstaCal can test the cascaded counters 1 and 2 against the system clock to ensure that they are functioning. It can also stimulate the digital outputs and read the digital inputs. A better dynamic test of the counters and digital I/O can be performed by the IOTEST.EXE program.

5 SIGNAL CONNECTION

Signal connection can be one of the most challenging aspects of applying a data acquisition board. If you are an *Analog* Electrical Engineer then this section is not for you, but if you are like most PC data acquisition people these simple examples should get you started. The objective here is to present 'how to connect' common signals while avoiding discussion of electrical theory and special symbols. If you need a connection we do not show, or invent one, please call and tell us so we can add it to this manual.

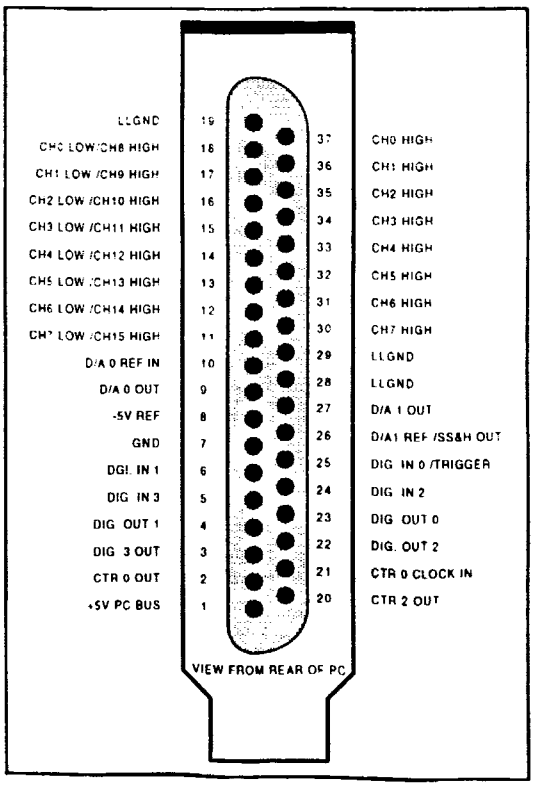
5.1 CONNECTOR DIAGRAM

ANALOG SIGNAL CONNECTOR

The CIO-DAS1600 analog connector is a 37 pin D type connector accessible from the rear of the PC through the expansion backplate. The signals available are identical to the DAS-16, or optionally, an additional signal, SS&H OUT, may be accessed at pin 26.

The connector accepts female 37 D type connectors, such as those on the C73FF-2, 2 foot cable with connectors.

If frequent changes to signal connections or signal conditioning is required a screw terminal board should be purchased.

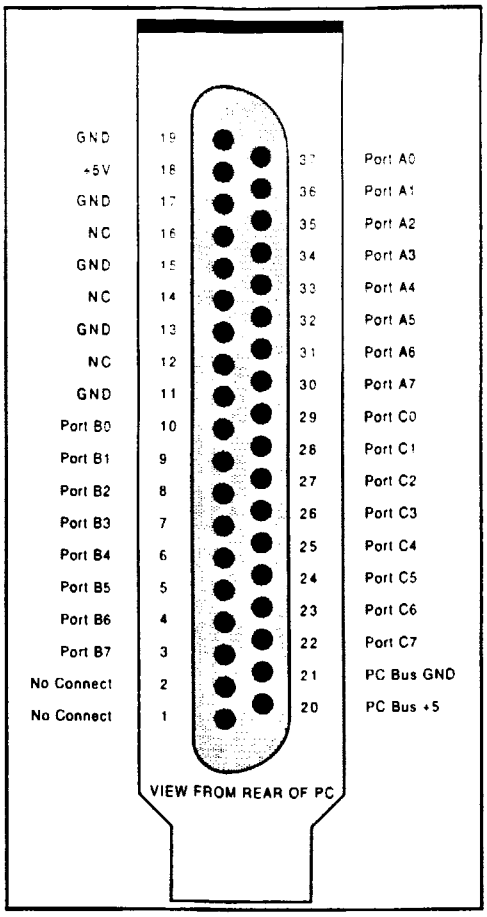


24 DIGITAL I/O CONNECTOR

The CIO-DAS1600 digital connector is identical to the CIO-DIO24 connector.

The connector is mounted at the rear of the CIO-DAS1600 and will accept a 40 pin header connector.

A BP40-37 will bring the signals to a backplate with a 37 pin male connector mounted in it.



5.2 ANALOG INPUTS

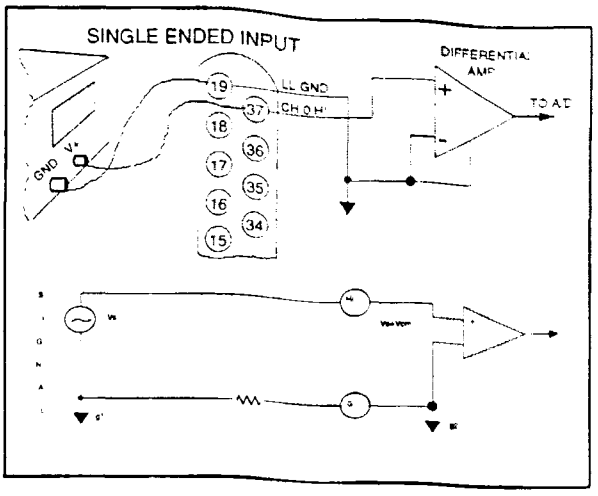
Analog inputs to the CIO-DAS1600 may be connected in three different configurations. In order of complexity, these are Single Ended, Floating Differential and Differential.

WARNING - PLEASE READ

Here is a good tip. Measure the voltage potential (difference) between the ground signal at the signal source and the PC. Use a volt meter and place the red probe on the PC ground and the black probe on the signal ground. If there is a difference of ***more than 10 volts,*** *do not connect the CIO-DAS1600 to this signal source because you will not be able to make any reading. If the difference is* ***more than 30 volts, DO NOT connect this signal to the CIO-DAS1600*** *because it will damage the board and possibly the computer.*

5.2.1 SINGLE ENDED

A single ended input is two wires connected to the CIO-DAS1600; a channel high (CH# HI) and a Low Level Ground (LLGND). The LLGND signal *must be the same ground the PC is on.* The CH# HI is the voltage signal source.

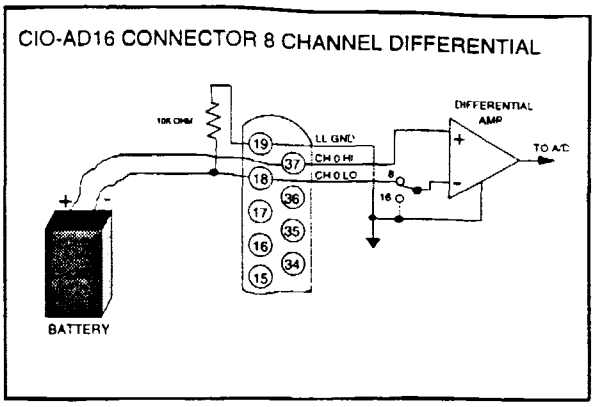


5.2.2 FLOATING DIFFERENTIAL

A floating differential input is two wires from the signal source and a 10K ground reference resistor installed at the CIO-DAS1600 input. The two signals from the signal source are Signal High (CH# HI) and Signal Low (CH# LO).

The reference resistor is connected between the CIO-DAS1600 CH# LO and LLGND pins.

A floating differential hookup is handy when the signal source is floating with respect to ground, such as a battery, 4-20mA transmitter or and the lead lengths are long or subject to EMI interference.



The floating differential input will reject up to 10V of EMI energy on the signal wires.

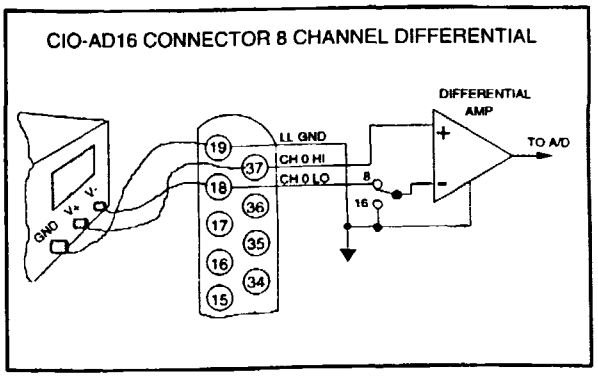
WARNING! Is the signal source really floating? Check it with a voltmeter before risking the CIO-DAS1600 and PC!

5.2.3 DIFFERENTIAL

A differential signal is three wires from the signal source. The signals are Signal High (CH# HI), Signal Low (CH# LO) and Signal Ground (LLGND).

A differential connection allows you to connect the CIO-DAS1600 to a signal source with a ground that is different than the PC ground, but less than 10V difference, and still make a true measurement of the signal between CH# HI and CH# LO.

EXAMPLE:
A laboratory instrument with its own wall plug. There are sometimes differences in wall GND between outlets.



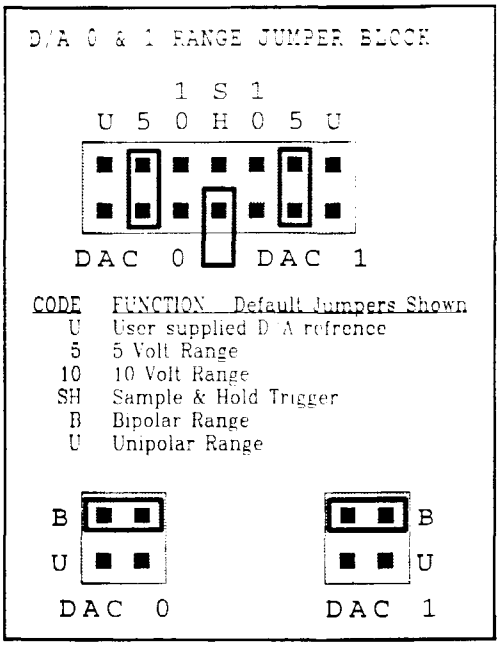
5.3 ANALOG OUTPUTS

Analog outputs are simple voltage outputs which can be connected to any device which will record, display or be controlled by a voltage.

The CIO-DAS1600 analog outputs are 4 quadrant multiplying DACs. This means that they accept an input voltage reference and provide an output voltage which is inverse to the reference voltage and proportional to the digital value in the output register.

For example, the supplied reference of -5V provides a +5V output when the value in the output register is 4095 (full scale at 12 bits of resolution). It provides a value of 2.5V when the value in the output register is 2048.

The diagram shows the on-board reference internally jumpered. Both D/A will have a range of -5 to 5 volts. This is the default factory configuration.

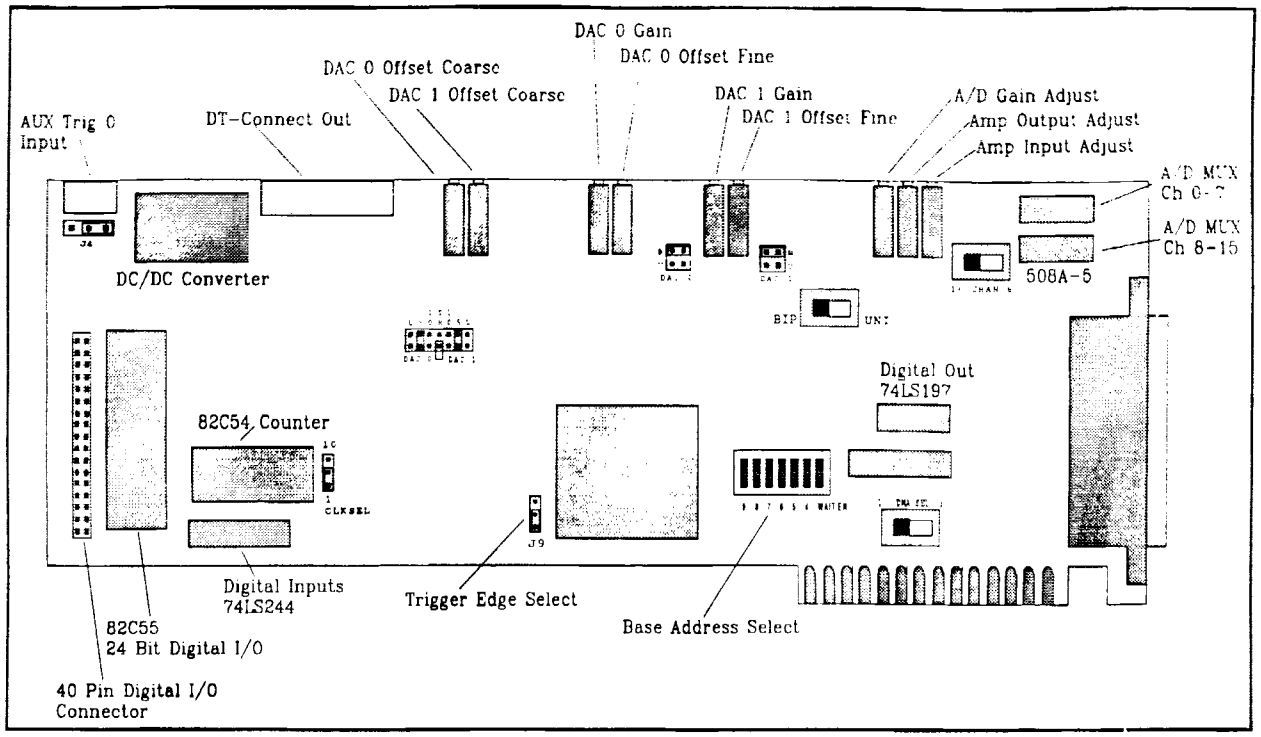


5.4 DIGITAL OUTPUTS & INPUTS

All the digital outputs inputs on the CIO-DAS1600 are TTL level. TTL is an electronics industry term, short for Transistor Transistor Logic.

Digital signal connections are common and easy to understand when the simple rules presented in the section on analog electronics are applied.

6 CIO-DAS1600 ARCHITECTURE



6.1 CONTROL & DATA REGISTERS

The CIO-DAS1600 is controlled and monitored by writing to and reading from consecutive 8 bit I/O addresses. The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

A register is easy to read and write to. Most often, register manipulation is best left to ASSEMBLY language programs as most of the CIO-DAS1600 possible functions are implemented in easy to use BASIC CALL routines or PASCAL, C FORTRAN libraries.

If you want to try direct register programming, experiment with the registers BASE + 400H to BASE + 403H, the 8255 registers.

The register descriptions follow the format:

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	CH8	CH4	CH2	CH1

Where the numbers along the top row are the bit positions within the 8 bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10

5	32	20
6	64	40
7	128	80

To write control or data to a register, the individual bits must be set to 0 or 1 then combined to form a Byte. Data read from registers must be analyzed to determine which bits are on or off.

The method of programming required to set/read bits from bytes is beyond the scope of this manual. It will be covered in most Introduction To Programming books, available from a book store.

In summary form, the registers and their function are listed on the following table. Within each register are 8 bits which may constitute a byte of data or 8 individual bit set/read functions.

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D Bits 9 - 12(LSB) & Channel #	Start A/D Conversion
BASE + 1	A/D Bits 1(MSB) - 8	None
BASE + 2	Channel MUX Set	Channel MUX Read
BASE + 3	Digital 4 Bit Input	Digital 4 Bit Output
BASE + 4	None	D/A 0 Bits 0-3
BASE + 5	None	D/A 0 Bits 4-11
BASE + 6	None	D/A 1 Bits 0-3
BASE + 7	None	D/A 1 Bits 4-11
BASE + 8	Status EOC, UNI/BIP etc.	Clear Interrupt
BASE + 9	DMA, Interrupt &Trigger Control	Set DMA, INT etc
BASE + 10	Pacer clock control/ Burst Length	Burts Length
BASE + 11	Programmable gain control.	Programmable Gain Control
BASE + 12	Counter 0 Data	Counter 0 Data
BASE + 13	CTR 1 Data - A/D Pacer Clock	CTR 1 Data - A/D Pacer
BASE + 14	CTR 2 Data - A/D Pacer Clock	CTR 2 Data - A/D Pacer
BASE + 15	None. No read back on 8254.	Pacer Clock Control (8254)
BASE + 400	Port A Input of 8255	Port A Output
BASE + 401	Port B Input	Port B Output
BASE + 402	Port C Input	Port C Output
BASE + 403	None. No read back on 8255.	Configure 8255
BASE + 404	None	Conversion Enable/Disable
BASE + 405	None	Burst Mode Enable/Disable
BASE + 406	None	DAS1600 Enable/Disable
BASE + 407	Status of extended features	None

6.1.1 A/D DATA & CHANNEL REGISTERS - CIO-DAS1600/12

BASE ADDRESS Example, 300 HEX, 768 Decimal

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	CH8	CH4	CH2	CH1

A read/write register.

READ

On read, it contains two types of data. The least significant 4 digits of the Analog input data and the channel number which the current data was taken from.

These 4 bits of analog input data must be combined with the 8 bits of analog input data in BASE + 1, forming a complete 12 bit number. The data is in the format 0 = minus full scale. 4095 = +FS.

The channel number is binary. The weights are shown in the table above. If the current channel were 5 then bits CH4 and CH1 would be high, CH8 and CH2 would be low.

WRITE

Writing any data to the register causes an immediate A/D conversion.

BASE ADDRESS + 1 301 HEX, 769 Decimal

7	6	5	4	3	2	1	0
A/D1 MSB	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7	A/D8

A Read-only register.

On read the most significant A/D byte is read.

6.1.2 A/D DATA & CHANNEL REGISTERS - CIO-DAS1600/16

BASE ADDRESS Example, 300 HEX, 768 Decimal

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12	A/D13	A/D14	A/D15	A/D16 LSB

A read/write register.

READ

On read, it contains the least significant 8 digits of the Analog input data.

These 8 bits of analog input data must be combined with the 8 bits of analog input data in BASE + 1, forming a complete 16 bit number. The data is in the format 0 = minus full scale. 65,536 = +FS.

WRITE

Writing any data to the register causes an immediate A/D conversion.

BASE ADDRESS + 1 301 HEX, 769 Decimal

7	6	5	4	3	2	1	0
A/D1 MSB	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7	A/D8

A Read-only register.

On read the most significant A/D byte is read.

6.1.3 CHANNEL MUX SCAN LIMITS REGISTER

BASE ADDRESS + 2 302 HEX, 770 Decimal

7	6	5	4	3	2	1	0
CH H8	CH H 4	CH H 2	CH H 1	CH L8	CH L4	CH L2	CH L 1

A read and write register.

READ

The current channel scan limits are read as one byte. The high channel number scan limit is in the most significant 4 bits. The low channel scan limit is in the least significant 4 bits.

WRITE

The channel scan limits desired are written as one byte. The high channel number scan limit is in the most significant 4 bits. The low channel scan limit is in the least significant 4 bits.

NOTE: Every write to this register sets the current A/D channel MUX setting to the number in bits 7-4. See BASE + 8.

6.1.4 4 BIT DIGITAL I/O REGISTERS

BASE ADDRESS + 3 303 HEX, 771 Decimal

When read...

7	6	5	4	3	2	1	0
1	1	0	0	DI3	DI2, CTR 0 GATE	DI1	DI0, TRIG

READ

The signals present at the inputs are read as one byte, the most significant 4 bits of which are always zero. The pins 25 (digital input 0) and 24 (digital input 2) digital inputs have two functions each.

The TRIG function of digital input 0 may be used to hold of the first sample of an A/D set by holding it low (0V) until you are ready to take samples, which are then paced by the 8254. It can also be used as the source of an external start conversion pulse, synchronizing A/D conversions to some external event.

When written to..

7	6	5	4	3	2	1	0
X	X	X	X	DO3	DO2	DO1	DO0

WRITE

The upper four bits are ignored. The lower four bits are latched TTL outputs. Once written, the state of the inputs cannot be read back because a read back would read the separate digital input lines (see above).

***NOTE:** The digital lines 0-4, pins 3,4,5,6,22,23,24 & 25 of the analog connector should not be used as ON/OFF Digital I/O. Read on..*

The digital inputs have multiple functions as described above. The digital outputs are also used by the MUX-TC32, 32 channel analog multiplexor/amplifier. The original DAS-16 design is woefully short of digital I/O, so we added a CIO-DIO24 compatible 24 line 8255 to the design. It is our suggestion that these lines be used for ON/OFF digital functions, keeping the 4 bit ports on the analog connector free.

6.1.5 D/A REGISTERS

D/A 0 REGISTERS

BASE ADDRESS + 4 304 HEX, 772 Decimal

7	6	5	4	3	2	1	0
D/A3	D/A2	D/A1	D/A0	X	X	X	X

BASE ADDRESS + 5 305 HEX, 773 Decimal

7	6	5	4	3	2	1	0
D/A11	D/A10	D/A9	D/A8	D/A7	D/A6	D/A5	D/A4

D/A 1 REGISTERS

BASE ADDRESS + 6 306 HEX, 774 Decimal

7	6	5	4	3	2	1	0
D/A3	D/A2	D/A1	D/A0	X	X	X	X

BASE ADDRESS + 7 307 HEX, 775 Decimal

7	6	5	4	3	2	1	0
D/A11	D/A10	D/A9	D/A8	D/A7	D/A6	D/A5	D/A4

WRITE ONLY

Each 12 bit D/A output line has two registers. The first contains the 4 least significant bits of the data and 4 bits that don't matter. The second register contains the 8 most significant bits of the data.

The D/A will be updated when the 8 most significant bits (upper register) are written. In this way, the lower 4 bits may be written with no effect on the D/A output until the remainder of the data is written to the upper 8 bits.

6.1.6 STATUS REGISTER

BASE ADDRESS + 8 308 HEX, 776 Decimal

7	6	5	4	3	2	1	0
EOC	U/B	MUX	INT	CH8	CH4	CH2	CH1

A read mostly, one-function-write register.

READ

EOC = 1, the A/D converter is busy. EOC = 0, it is free.

U/B = 1, the amplifier is in Unipolar mode. U/B = 0, is bipolar.

MUX = 1, Channels are configured 16 single ended. MUX = 0, 8 differential.

INT = 1, an external pulse has been received. INT = 0, the flip-flop is ready to receive a pulse..

There is a flip-flop on the TRIGGER input (pin 25) which will latch a pulse as short as 200 nanoseconds. triggered, this flip-flop must be reset by a write to this register. Your interrupts service routine must do this another interrupt trigger can be received.

CH8, CH4, CH2 & CH1 are a binary number between 0 and 15 indicating the channel number that the MU currently set to and is valid only when EOC = 0. The channel MUX increments shortly after EOC = 1 so may in a state of transition when EOC = 1. The binary weight of each bit is shown in the table above.

WRITE

A write of any data to this register resets the flip-flop on the pin 25 input and sets the INT bit to 0.

6.1.7 DMA, INTERRUPT & TRIGGER CONTROL

BASE ADDRESS + 9 *309 HEX, 777 Decimal*

7	6	5	4	3	2	1	0
INTE	IR2	IR1	IR0	Don't Care	DMA	TS1	TS0

A read and write register.

READ

INTE = 1, Interrupts are enabled. An interrupt generated will be placed on the PC bus interrupt level selected by IR4, IR2 & IR1. INTE = 0, interrupts are disabled.

IR4, IR2, IR1 are bits in a binary number between 0 and 7 which map interrupts onto the PC bus interrupt levels 2 - 7. Interrupts 0 & 1 may not be asserted by the CIO-DAS1600.

IR2	IR1	IR0	Interrupt Level
0	0	0	None
0	0	1	None
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

DMA = 1, DMA transfers are enabled. DMA = 0, DMA transfers are disabled. It is worth noting that this bit only allows the CIO-DAS1600 to assert a DMA request to the PC on the DMA request level selected by the DMA switch on the CIO-DAS1600. Before this bit is set to 1, the PC's 8237 (or appropriate) DMA controller chip must be set up.

TS1 & TS0 control the source of the A/D start conversion trigger according to the table below.

TS1	TS0	
0	X	Software triggered A/D only.
1	0	Start on rising TRIGGER (Digital input 0, Pin 25)
1	1	Start on Pacer Clock Pulse (CTR 2 OUT, no external access)

6.1.8 PACER CLOCK CONTROL REGISTER

BASE ADDRESS + 10 *30A HEX, 778 Decimal*

7	6	5	4	3	2	1	0
BL3	BL2	BI1	BL0	X	X	CTR0	TRIG0

Write only

BL3 - BL0 = BURST LENGTH. Nibble determines number of conversions per trigger when in burst mode. One to sixteen samples (single ended) or eight samples (differential) in a burst. When the CIO_DAS1600 is not in burst mode these bits have no function.

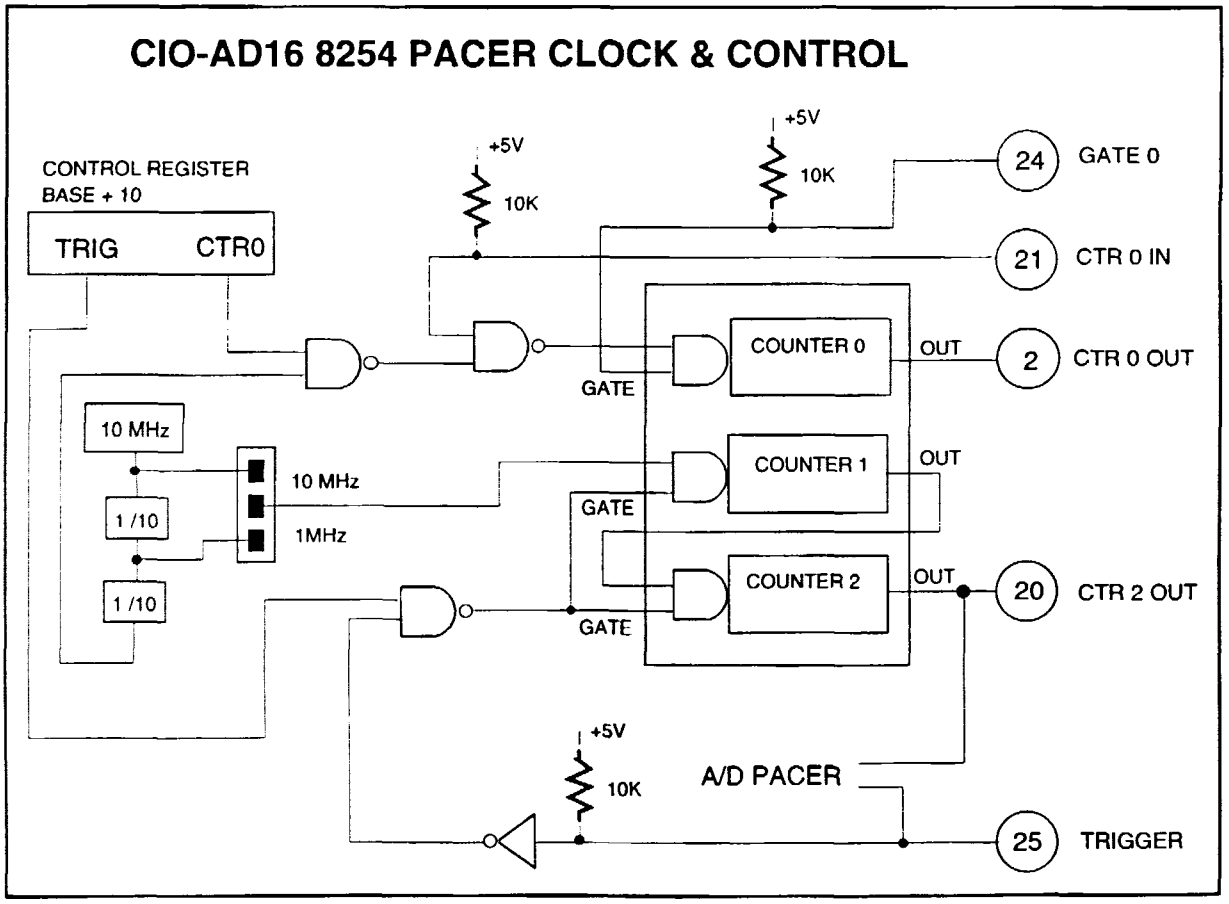
CTR0 = 1. When CTR0 = 1, an on-board 100KHz clock signal is ANDed with the COUNTER 0 CLOCK INPUT (pin 21). A high on pin 21 will allow pulses from the on-board source into the 8254 Counter 0 input.

CTR0 = 0. When CTR0 = 0, the input to 8254 Counter 0 is entirely dependent on pulses at pin 21, COUNTER 0 CLOCK INPUT.

TRIG0 = 1. When TRIG0 = 1, the TRIGGER input at pin 25 is ANDed with TRIG0 which must therefore be high for the pulses from the on-board pacer clock (8254) to start A/D conversions. The input at pin 25 is pulled up and will always be high unless pulled low externally.

TRIG0 = 0. When TRIG0 = 0, the GATEs of counter 1 & 2 are held high, preventing any pulses from acting as a source of A/D start pulses.

The following diagram may help understand these registers, and is further explained in the section covering the 8254.



6.1.9 PROGRAMMABLE GAIN GONTROL REGISTER / BURST RATE

BASE ADDRESS + 11 30B HEX, 779 Decimal

7	6	5	4	3	2	1	0
X	X	X	X	X	X	G1	G0

BURST RATE is fixed at: CIO-DAS1600/12 = 4uS (250KHz) between burst samples. CIO-DAS1602/16 = 10uS (100kHz) between burst samples.

The MetraByte DAS-1600 manual lists this register as containing the control bits of a settable burst rate. Although the bits are described in detail, no amount of writing to them will cause a change in the burst rate. The MetraByte catalog lists the burst rate as fixed at 10uS and we found this to be consistant with the board's operation. The MetraByte manual appears to be in error.

Given the nature and purpose of burst mode, a rate fixed at the maximum possible *is* the best choice.

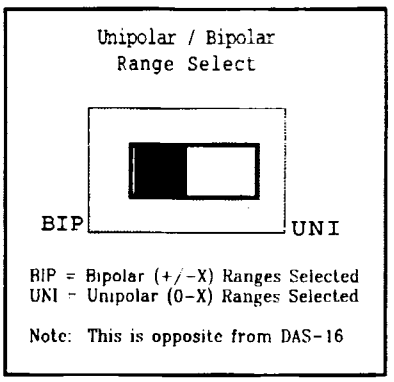
PROGRAMMABLE GAIN CONTROL: Range and gain is controlled by a register located at BASE + A hex (11 decimal). The codes have different meaning for each board in the DAS1600 family

BOARD	CODE	BIPOLAR RANGE	UNIPOLAR RANGE
CIO-DAS1601/12	0	+/-10V	0-10V
	1	+/-1V	0-1V
	2	+/-0.1V	0-0.1V
	3	+/-0.01V	0-0.01V
CIO-DAS1602/12	0	+/-10V	0-10V
	1	+/-5V	0-5V
and	2	+/-2.5V	0-2.5V
CIO-DAS1602/16	3	+/-1.25V	0-1.25V

The range, unipolar or bipolar is controlled by a switch.

This switch is an artifact of old DAS-16 technology and should never have been designed into the DAS-1600. That it was designed into the DAS-1600 is unfortunate, but, since the CIO-DAS1600 is a perfect clone of the DAS-1600, we had to follow this scheme.

If your application is better served by programmable ranges, please consider the CIO-DAS16/Jr or CIO-DAS16/330 boards.



DT-CONNECT NOTE:

To guaranty that DT-Connect is properly initialized prior to any A/D transfer, the DT-Connect DT-Request handshake line is reset each time the programmable gain (Base + 11) register is written to. Therefoe, it is not possible to use the DT-Connect for A/D sets which involve setting the gain between samples. This is not really a problem because any such scheme would be low speed and therefore store data to disk, obviating the need to use DT-Connect to store data on the MEGA-FIFO.

6.1.10 PACER CLOCK DATA & CONTROL REGISTERS

8254 COUNTER 0 DATA
BASE ADDRESS + 12 — 30C HEX, 780 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 1 DATA
BASE ADDRESS + 13 — 30D HEX, 781 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 2 DATA
BASE ADDRESS + 14 30E HEX, 782 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

The three 8254 counter/timer data registers may be written to and read from. Because each counter will count as high as 64,535, it is clear that loading or reading the counter data must be a multi-step process. The operation of the 8254 is explained in the section on the counter/time and the Intel 8254 data sheet.

8254 COUNTER CONTROL
BASE ADDRESS + 15 30F HEX, 783 Decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

This register controls the operation and loading/reading of the counters. The configuration of the 8254 codes which control the 8254 chip is explained in the section on the counter timer and the Intel 8254 data sheet.

6.1.11 24 LINE DIGITAL I/O REGISTERS

PORT A DATA
BASE ADDRESS + 400 700 HEX

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0
Pin 30	Pin 31	Pin 32	Pin 33	Pin 34	Pin 35	Pin 36	Pin 37

PORT B DATA
BASE ADDRESS + 401 701 HEX

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10

Ports A & B may be programmed as input or output. Each is written to and read from in Bytes, although for control and monitoring purposes the individual bits are more interesting.

Bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

PORT C DATA
BASE ADDRESS + 402 702 HEX

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH4	CH3	CH2	CH1	CL4	CH3	CH2	CH1
128 Bit	64 Weight	32 Dec.	16	8	4	2	1
80 Bit	40 Weight	20 HEX	10	8	4	2	1
Pin 22	Pin 23	Pin 24	Pin 25	Pin 26	Pin 27	Pin 28	Pin 29

Port C may be used as one 8 bit port of either input or output, or it may be split into two 4 bit ports which may be independently input or output. The notation for the upper 4 bit port is PCH3 - PCH0, and for the lower, PCL3 - PCL0.

Although it may be split, every read and write to port C carries 8 bits of data so unwanted information must be ANDed out of reads, and writes must be ORed with the current status of the other port.

OUTPUT PORTS

In 8255 mode 0 configuration, ports configured for output hold the output data written to them. This output byte may be read back by reading a port configured for output.

INPUT PORTS

In 8255 mode 0 configuration, ports configured for input read the state of the input lines at the moment, transitions are not latched.

8255 CONTROL REGISTER
BASE ADDRESS + 403 703 HEX

7	6	5	4	3	2	1	0
MS	M3	M2	A	CU	M1	B	CL
	Group A				Group B		

The 8255 may be programmed to operate in Input/ Output (mode 0), Strobed Input/ Output (mode 1) or Bi-Directional Bus (mode 2).

When the PC is powered up or RESET, the 8255 is reset. This places all 24 lines in Input mode and no further programming is needed to use the 24 lines as TTL inputs.

To program the 8255 for other modes, the following control code byte must be assembled into on 8 bit byte.

MS = Mode Set. 1 = mode set active

M3	M2	Group A Function	
0	1	Mode 0	Input / Output
0	1	Mode 1	Strobed Input / Output
1	X	Mode 2	Bi-Directional Bus

A	B	CL	CH	Independent Function
1	1	1	1	Input
0	0	0	0	Output

M1 = 0 is mode 0 for group B. Input / Output
M1 = 1 is mode 1 for group B. Strobed Input / Output

The Ports A, B, C High and C Low may be independently programmed for input or output.

The two groups of ports, group A and group B, may be independently programmed in one of several modes. The most commonly used mode is mode 0, input / output mode. The codes for programming the 8255 in this mode are shown below. D7 is always 1 and D6, D5 & D2 are always 0.

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	OUT	IN	OUT
0	0	1	1	83	131	OUT	OUT	IN	IN
0	1	0	0	88	136	OUT	IN	OUT	OUT
0	1	0	1	89	137	OUT	IN	OUT	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	OUT	IN	OUT
1	0	1	1	93	147	IN	OUT	IN	IN
1	1	0	0	98	152	IN	IN	OUT	OUT
1	1	0	1	99	153	IN	IN	OUT	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

6.1.12 CONVERT DISABLE REGISTER

BASE ADDRESS + 404 HEX

7	6	5	4	3	2	1	0
T	T	T	T	T	T	T	T

WRITE ONLY. Writing a 0 to this register enables A/D triggers from reaching the A/D converter *if* the DAS1600 mode is enabled. On power-up or reset this register is reset to conversion triggers enabled. Writing a 40H to this register disables A/D conversions.

6.1.13 MODE ENABLE REGISTER

BASE ADDRESS + 405 HEX

7	6	5	4	3	2	1	0
M	M	M	M	M	M	M	M

WRITE ONLY. DAS1600 mode enable. Writing 40 HEX to this register enables the DAS1600 functions. Writing 0 to this register disables DAS1600 functions. On power-up or reset the DAS1600 functions are disabled.

6.1.14 BURST MODE ENABLE REGISTER

BASE ADDRESS + 405 HEX

7	6	5	4	3	2	1	0
B	B	B	B	B	B	B	B

WRITE ONLY. Burst mode enable. Writing 40 HEX to this register enables the burst trigger. Writing 0 to this register disables burst trigger. On power-up or reset the burst trigger is disabled.

6.1.15 BURST STATUS REGISTER

BASE ADDRESS + 407 HEX

7	6	5	4	3	2	1	0
0	BME	ME	CD	0	0	WS	CLK

READ ONLY. This register provides status on:
The clock select switch and wait state switch.
The DAS1600 enable, Conversion Disable and Burst Mode Enable bits.

The register defaults to 000100XX on power-up or reset, which corresponds to the programmable bit default settings plus the state of the switches. The bit assignments are as follows.

BME 1 = Burst Mode Enabled, 0 = disabled.

ME 1 = DAS1600 Mode Enabled, 0 = disabled.

CD 1 = Conversions allowed, 0 = conversions disabled.
NOTE: This is oposite of the control bit you write.

WS 1 = Wait State Enabled, 0 = No wait state.

CLK 1 = 10MHz clock selected, 0 = 1MHz clock selected.

6.2 SPECIFICATIONS

POWER CONSUMPTION

+5	2.1A MAX,	1.4A Typical
+12	Not Used	
-12	Not Used	

ANALOG INPUT - CIO-DAS1600/12

Channels	8 Differential	16 Single Ended
Resolution	12 Bits	1 part in 4095
Accuracy	0.01% of reading, ±1 bit	
Input Range	±10V MAX	± 0.25V MIN
	See table in section on Analog Input	
Coding	Bipolar	Offset binary
	Unipolar	True binary
Overvoltage	±35V continuous	
Input Current	250 nA MAX	12 nA typ @ 25 deg C
Input Impedance	10 Meg Ohm	
Temp. Coeff.	Full Scale	±25 ppm/deg C MAX
	Zero	±12 ppm/dec C MAX
Type	Successive Approximation	
Conversion Time	3.3 uSec MAX	ADS7800
Monotonicity	Guaranteed over operating temp. range.	
Linearity	±1 Bit	
Zero drift	±10 ppm/deg C MAX	
Gain drift	±30 ppm/deg C MAX	
Vref Output	-5V ±0.05V	

ANALOG INPUT - CIO-DAS1600/16

Only specifications which differ from DAS1600/12

Resolution	16 Bits	1 part in 65,535
Accuracy	±1.5 LSB	
Conversion Time	10.0 uSec MAX	ADS7805
Monotonicity	Guaranteed over operating temp. range.	
Linearity	-1, +0.5 LSB	
Zero drift	±2 ppm/deg C MAX	
Gain drift	±7 ppm/deg C MAX	

D/A CONVERTERS

Channels	Two Independent
Type	12 bit multiplying, double buffered
Linearity	±1bit
Monotonicity	±1bit
Output range	±10V MAX
Output drive	±5mA MIN
Output resistance	<0.1 Ohm
VREF Input range	±10V
Full scale out	Gain = -1 * VREF
Settling time	30 uSec to 1% for full scale step.

PROGRAMMABLE TIMER

Type	82C54	
Counters	3, 16 Bit down counters	
	2 dedicated to A/D pacer	
XTAL	1 or 10 MHz	
Output Drive	2.2mA @ 0.45V	
Input	TTL	
Frequency	DC to 10MHz	
Active count edge	Negative	
Clock pulse width	30nSec High	50nSec Low

DIGITAL I/O

Input/Output	24 bits	8255, three 8 bit ports
Input only	4 bits	74LS244
Output only	4 bits	74LS197
Input low volts	74LS244	0.8V MAX
	8255	0.5V MAX
Input high volts	74LS244	2.0V MIN @ 20uA
	8255	2.0V MIN, 7.0V MAX
Output low volts	74LS197	0.5V MAX @ 8.0mA
	8255	0.5V MAX @ 2.5mA
Output high volts	74LS197	2.4V MIN @-0.4mA
	8255	2.4V MIN @ -200uA

INTERRUPT

Level	2-7	Software programmable
Enable	INTE Bit	CIO-DAS1600 Control register
Trigger	On board	8254 pacer clock
	External	User supplied TTL pulse

DMA A/D TRANSFER

Level	1 or 3	Switch selectable
Enable	DMA Bit	CIO-DAS1600 Control register
Termination	Single Cycle	Interrupt on terminal count
	Recycle	
Pacing	Internal	8254 pacer clock
	External	User supplied TTL pulse

POWER OUTPUTS

Direct from PC bus		See your PC spec.
Voltage	±5V ±5%	Depends on PC power
Loading	22AWG	64.9 Ohms/ 1000 feet

ENVIRONMENTAL

CIO-DAS1600	*Normal Temp Model*
Operating Temp	0 to 50 Deg C
Storage Temp	-20 to 70 Deg C
Humidity	0 to 90% non-condensing
Weight	11.2 Oz

CIO-DAS1600	*Extended Temp Model*
Operating Temp	-30 to 60 Deg C
Storage Temp	-165 to 150 Deg C
Humidity	0 to 90% non condensing
Weight	10.25 Oz

7 ANALOG ELECTRONICS

7.1 VOLTAGE DIVIDERS

If you wish to measure a signal which varies over a range greater than the input range of an analog or digital input, a voltage divider can drop the voltage of the input signal to the level the analog or digital input can measure.

A voltage divider takes advantage of Ohm's law, which states,

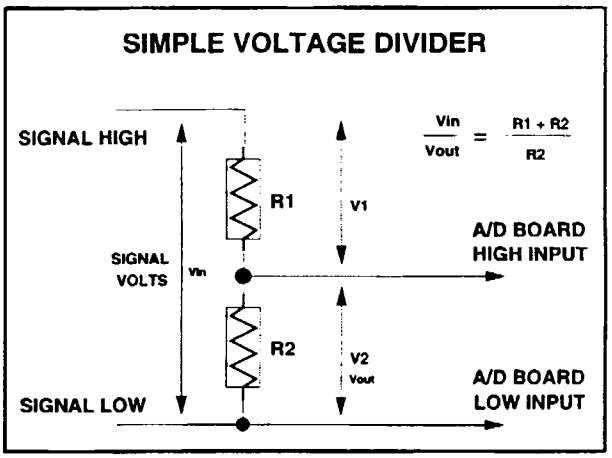
Voltage = Current * Resistance

and Kirkoff's voltage law which states,

The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

Implied in the above is that any variation in the voltage drop for the circuit as a whole will have a *proportional* variation in all the voltage drops in the circuit.

A voltage divider takes advantage of the fact that the voltage across one of the resistors in a circuit is proportional to the voltage across the total resistance in the circuit.
The trick to using a voltage divider is to choose two resistors with the proper proportions relative to the full scale of the analog or digital input and the maximum signal voltage.



The phenomena of dropping the voltage proportionally is often called attenuation. The formula for attenuation is:

Attenuation =	$\frac{R1 + R2}{R2}$	The variable *Attenuation* is the proportional difference between the signal voltage max and the full scale of the analog input.
2 =	$\frac{10K + 10K}{10K}$	For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the *Attenuation* is 2:1 or just 2.
R1 =	(A - 1) * R2	For a given attenuation, pick a handy resistor and call it R2, then use this formula to calculate R1.

Digital inputs also make use of voltage dividers, for example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to the CIO-AD digital inputs. The voltage must be dropped to 5 volts max when on. The *Attenuation* is 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 1K. Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

IMPORTANT NOTE: The resistors, R1 and R2, are going to dissipate all the power in the divider circuit according to the equation Current = Voltage / Resistance. The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit. Here is a simple rule:

For Attenuation of 5:1 or less, no resistor should be less than 10K.

For Attenuation of greater than 5:1, no resistor should be less than 1K.

The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. The CIO-TERMINAL is a 16" by 4" screw terminal board with two 37 pin D type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you may complete with the proper value components for your application.

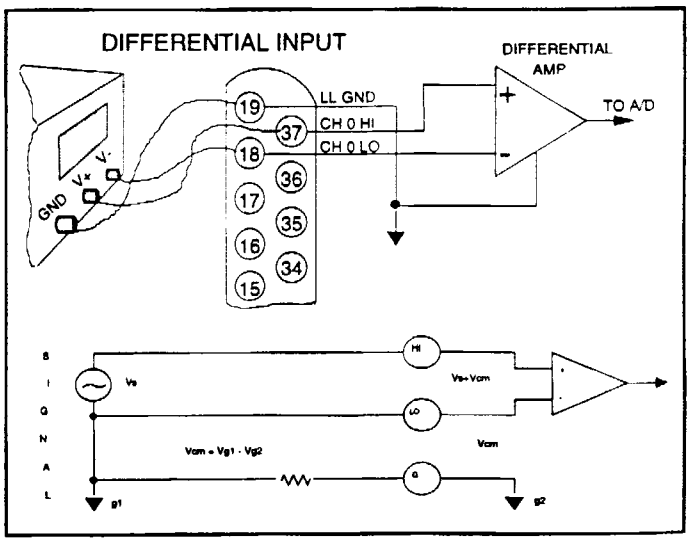
7.2 DIFFERENTIAL & SINGLE ENDED INPUTS

Two type of analog inputs are commonly found on A/D boards, they are differential and single ended. Single ended is the less expensive of the two.

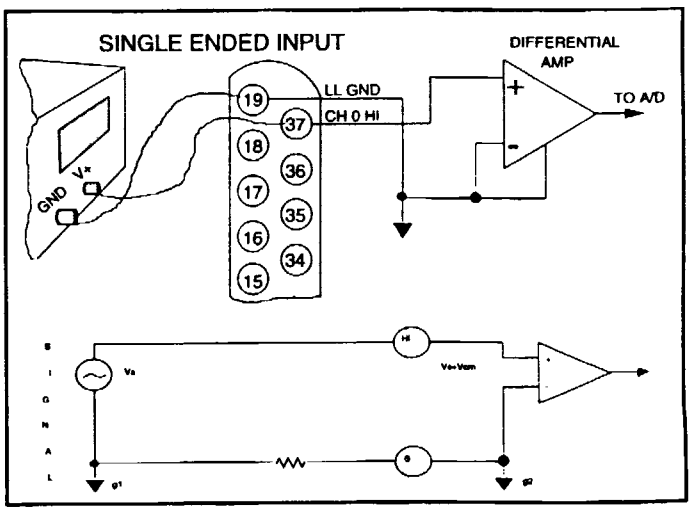
COMMON MODE RANGE

Differential inputs have a common mode range (CMR)(Vcm). Single ended inputs have no CMR . Common mode range is the voltage range over which differences in the low side of the signal and A/D input ground have no impact on the A/D's measurement of the signal voltage. A differential input can reject differences between signal ground and PC ground.

Shown here is a CIO-DAS1600 in differential mode.



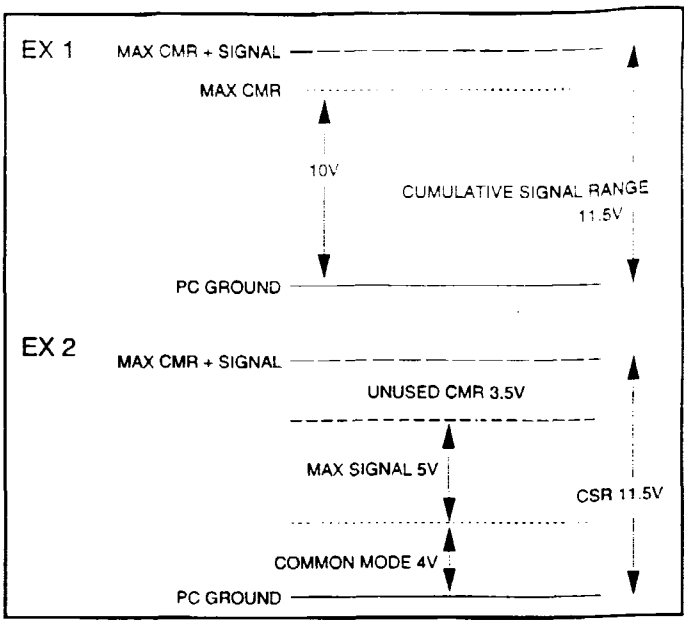
A single ended input has no common mode range because there is only one LOW wire, which is assumed to be at the same level at the signal source and at the A/D board.



The maximum difference which may be rejected is the CMR.

For example, the CIO-DAS1600 has a common mode plus signal range of 11.5 volts, common mode not to exceed 10 volts.

This specification is illustrated graphically here and will be referred to as **Cumulative Signal Range (CSR)**.



Most manufactures of A/D boards specify the CMR directly from the component data sheet, ignoring the effect of the board level system on that specification. A data sheet of that type might claim 10 volts of CMR. Although this is a factual specification and the designer of the board (or other EE) would be able to translate that into a systems specification, most A/D board owners are confused or mislead by such specs.

COMMON MISUNDERSTANDINGS

The CMR specification of a differential input is often confused with an isolation specification, which it is not. It makes sense, doesn't it, that 10 volts of CMR is the same as 10 volts of isolation? No. The graph above shows why.

Also, failure to specify the common mode plus signal *system* specification leads people to believe that a DC offset equal to the component CMR can be rejected regardless of the input signal voltage. It cannot as the graph above illustrates.

When is a differential input useful? The best answer is whenever electromagnetic interference (EMI) or radio frequency interference (RFI) may be present in the path of the signal wires. EMI and RFI can induce voltages on *both* signal wires and the effect on single ended inputs is generally a voltage fluctuation between signal high and signal ground.

A differential input is not affected in that way. When the signal high and signal low of a differential input have EMI or RFI voltage induced on them, that ***common mode voltage*** is rejected, subject to the system constraint that common mode plus signal not exceed the A/D board's CSR specification.

GROUND LOOPS

Ground loops are circuits (E=I*R) created when the signal ground and the PC ground are not the same. Ground loop inducing voltage differential may be a few volts of hundreds of volts. They may be constant or transient (spikes). A differential input will prevent a ground loop as long as the CSR specifications is not exceeded.

If ground differences greater than the CMR are encountered, isolation is required.

WHY USE SINGLE ENDED?

Unanswered still is the question of why use single ended inputs? First, single ended inputs require fewer parts so they cost less money. On an A/D board the parts cost to go from 16 single ended channels to 16 differential channels is about $6.00 so that cannot be the reason. The real reason is connector space. Single ended inputs require one analog high input per channel and one LLGND shared by all inputs. Differential inputs require signal high and signal low inputs for each channel and one common shared LLGND.

Single ended inputs save connector space, parts cost and in all cases where there is no common mode or EMI/RFI they work just as well as differential inputs and are less complex to wire up.

7.3 LOW PASS FILTERS

A low pass filter is placed on the signal wires between a signal and an A/D board. It stops frequencies greater than the cut off frequency from entering the A/D board's analog *or* digital inputs.

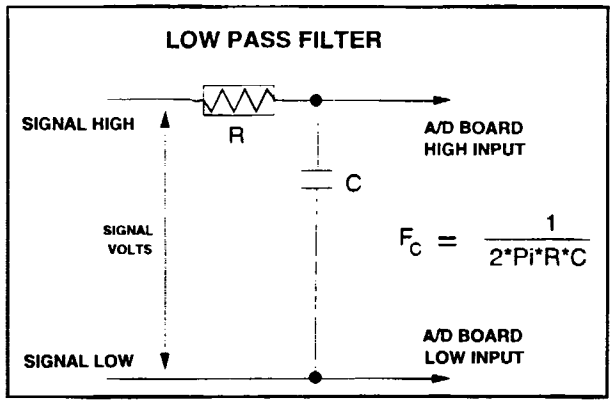
The key term in a low pass filter circuit is **cut off frequency**. The cut of frequency is that frequency above which no variation of voltage with respect to time may enter the circuit. For example, if a low pass filter had a cut off frequency of 30 Hz, the kind of interference associated with line voltage (60Hz) would be filtered out but a signal of 25Hz would be allowed to pass.

Also, in a digital circuit, a low pass filter might be used to de-bounce an input from a momentary contact button pushed by a person.

A low pass filter may be constructed from one resistor (R) and one capacitor (C). The cut off frequency is determined according to the formula:

$$F_c = \frac{1}{2 * Pi * R * C}$$

$$R = \frac{1}{2 * Pi * C * F_c}$$



7.4 A/D RESOLUTION & ENGINEERING UNITS

Resolution is specified in bits, such as 8, 10 or 12 bits. The 12 bits are really a power of 2 indicating the number of divisions of full scale the converter can resolve. For example, a 12 bit converter can resolve (2^12 - 1) = 4095 divisions of full scale. If the input of the board were +/- 5 volts full scale, each of the 4095 steps would be equal to 0.00244 volts.

Reading from the A/D converter would be thus:

Converter #	Volts
4095	5.0
4094	4.9976
4093	4.9951
2048	0.0
1	- 4.9976
0	- 5.0

The concept of resolution is the ability to differentiate between one voltage and another. Obviously, the more bits of resolution (13 bits = 8192 counts) the more divisions of full scale. The more divisions of full scale the finer the measurement.

ENGINEERING UNITS

When a program uses an A/D board to acquire data, the data file is filled with numbers like those above.

To translate the A/D numbers back into the engineering units of the original measurement, we need to know:

The sensor's voltage output per engineering unit.

The full scale range of the board at the time the measurement was made.

The resolution of the converter.

Here is an example from the application note on interfacing a Voland TA to a PC found elsewhere in this manual.

The TA measures resistance in grams between +500 and -500 grams.

The voltage output of the instruments is +2.5 volts to -2.5 volts.

The voltage output corresponds to the grams of pressure exactly, so:

+/- 500 grams = 1000 grams.

+/- 2.5 volts = 5 volts.

5 volts / 1000 grams = 0.005 volts per gram.

The A/D was set for +/- 2.5 volts = 5 volts full scale.

5 volts / 4095 counts = 0.00122 volts per bit.

If the number in the file for one reading was 3061, then

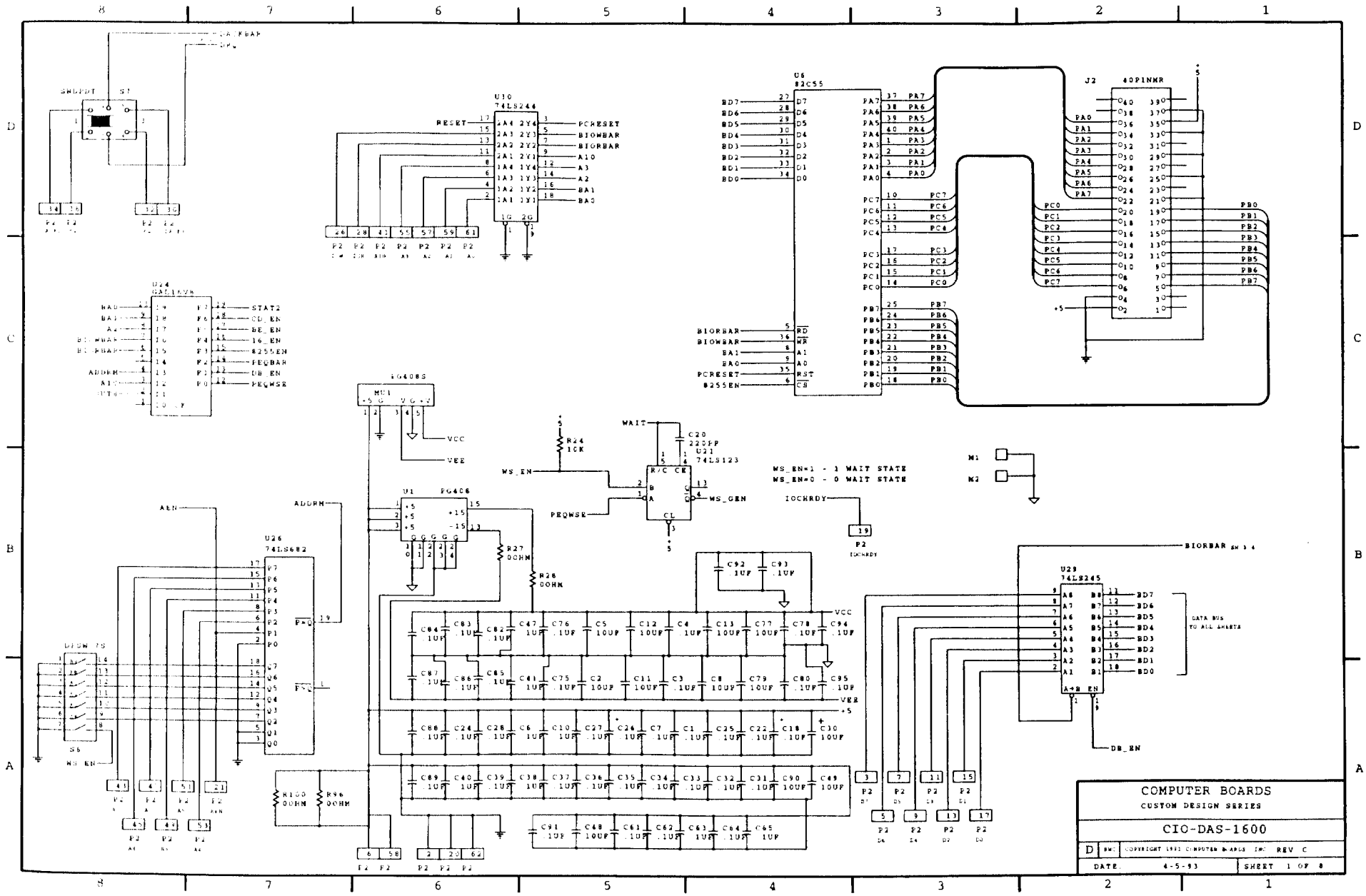
3061 * 0.00122 = 3.7632 volts.

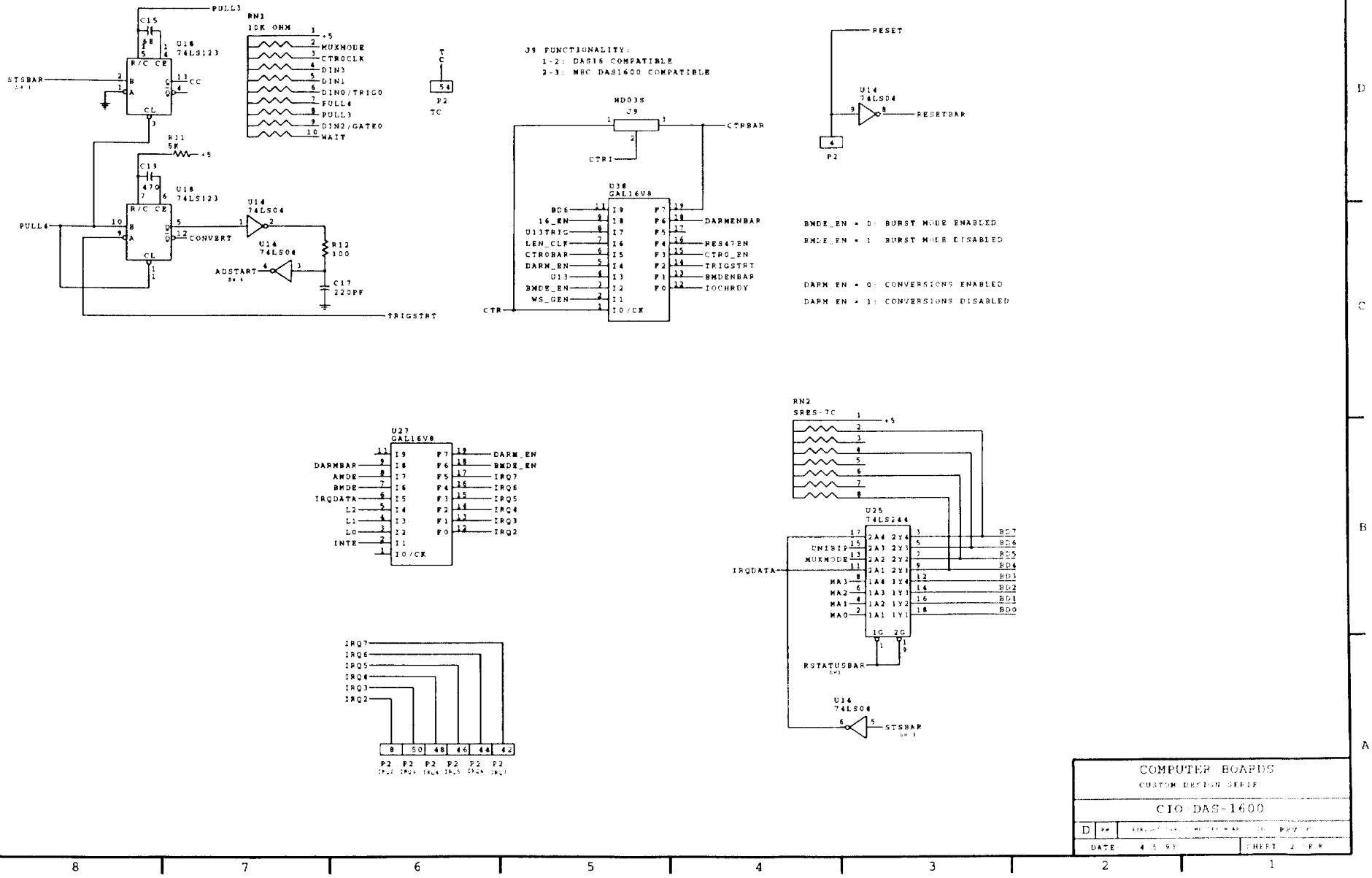
3.7632 volts / 0.005 volts per gram = 735 grams.

Now shift from full scale to +/- scale.

735 grams full scale - 500 = 235 grams of positive pressure.

It may look like a lot of steps because it is presented that way here for clarity only. It could be expressed as a single equation in a spreadsheet.


COMPUTER BOARDS
CUSTOM DESIGN SERIES
CIO-DAS-1600
D
DATE: 4-5-93
SHEET 1 OF 8
WS_EN=1 - 1 WAIT STATE
WS_EN=0 - 0 WAIT STATE
DATA BUS TO ALL SHEETS
U6 82C55
U10 74LS244
U29 74LS245
U26 74LS682
U21 74LS123
J2 40PINHDR
U1 PG406
MU1 PG408S
R24 10K
R27 OOHM
R28 OOHM
R100 OOHM
R96 OOHM
C20 .22UF
C92 .1UF
C93 .1UF
VCC
VEE
WAIT
WS_EN
WS_GEN
IOCHRDY
AEN
ADDRM
RESET
PCRESET
BIOWBAR
BIORBAR
A10
A3
A2
BA1
BA0
STAT2
CD_EN
BE_EN
16_EN
8255EN
PEQBAR
DB_EN
PEQWSE
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
PC7
PC6
PC5
PC4
PC3
PC2
PC1
PC0
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
DB_EN



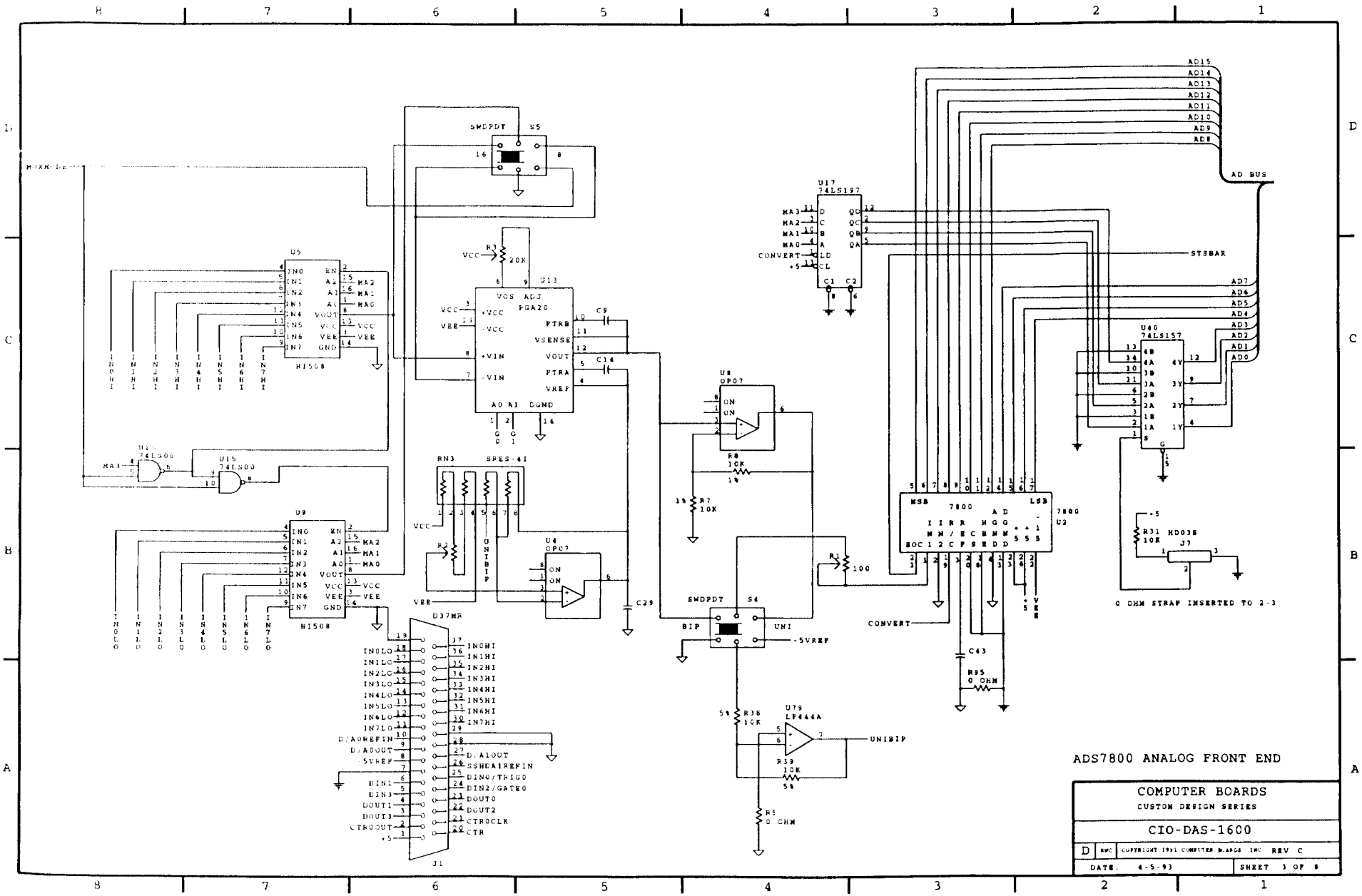
COMPUTER BOARDS

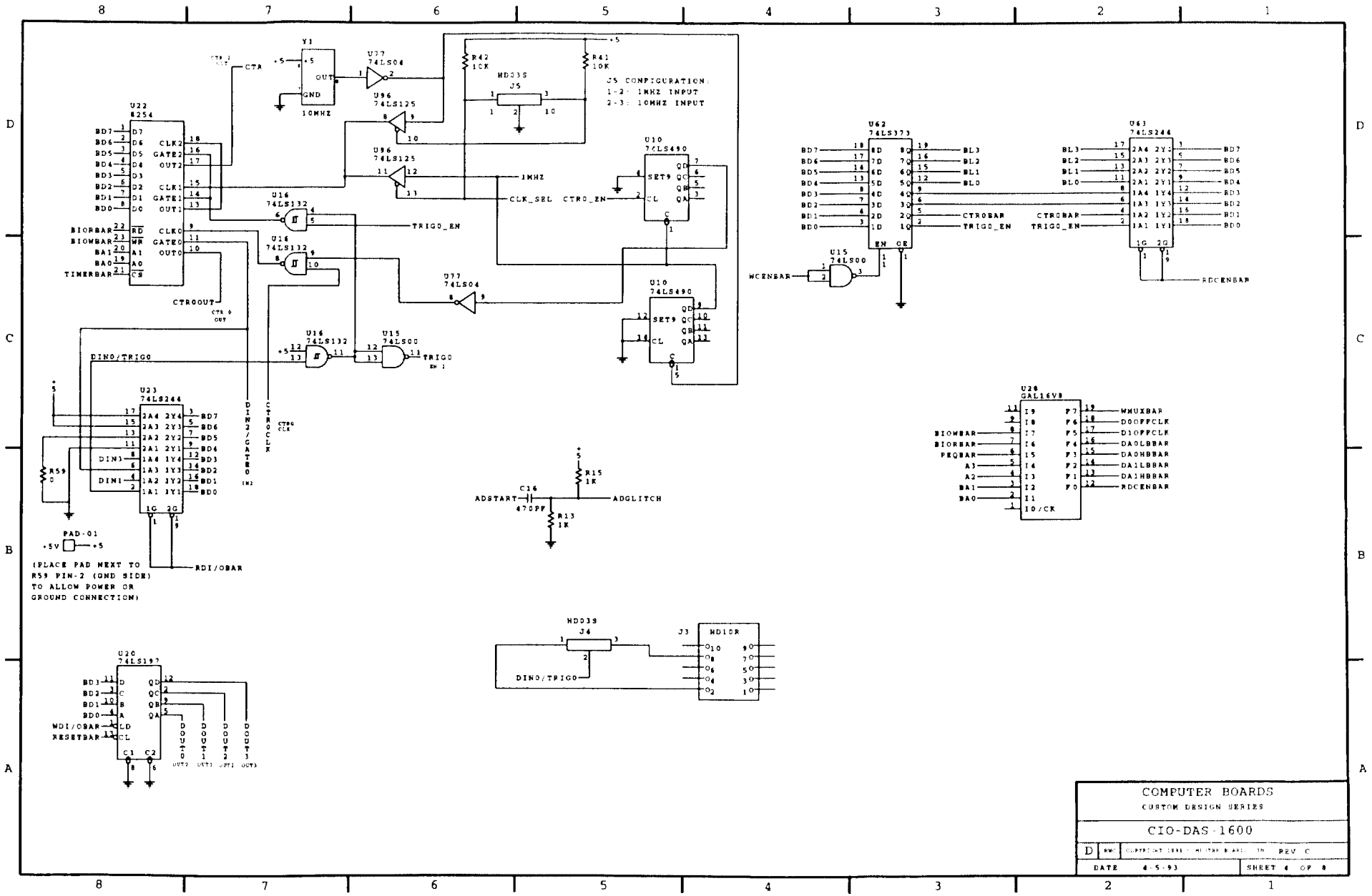
CUSTOM DESIGN SERIES

CIO-DAS-1600

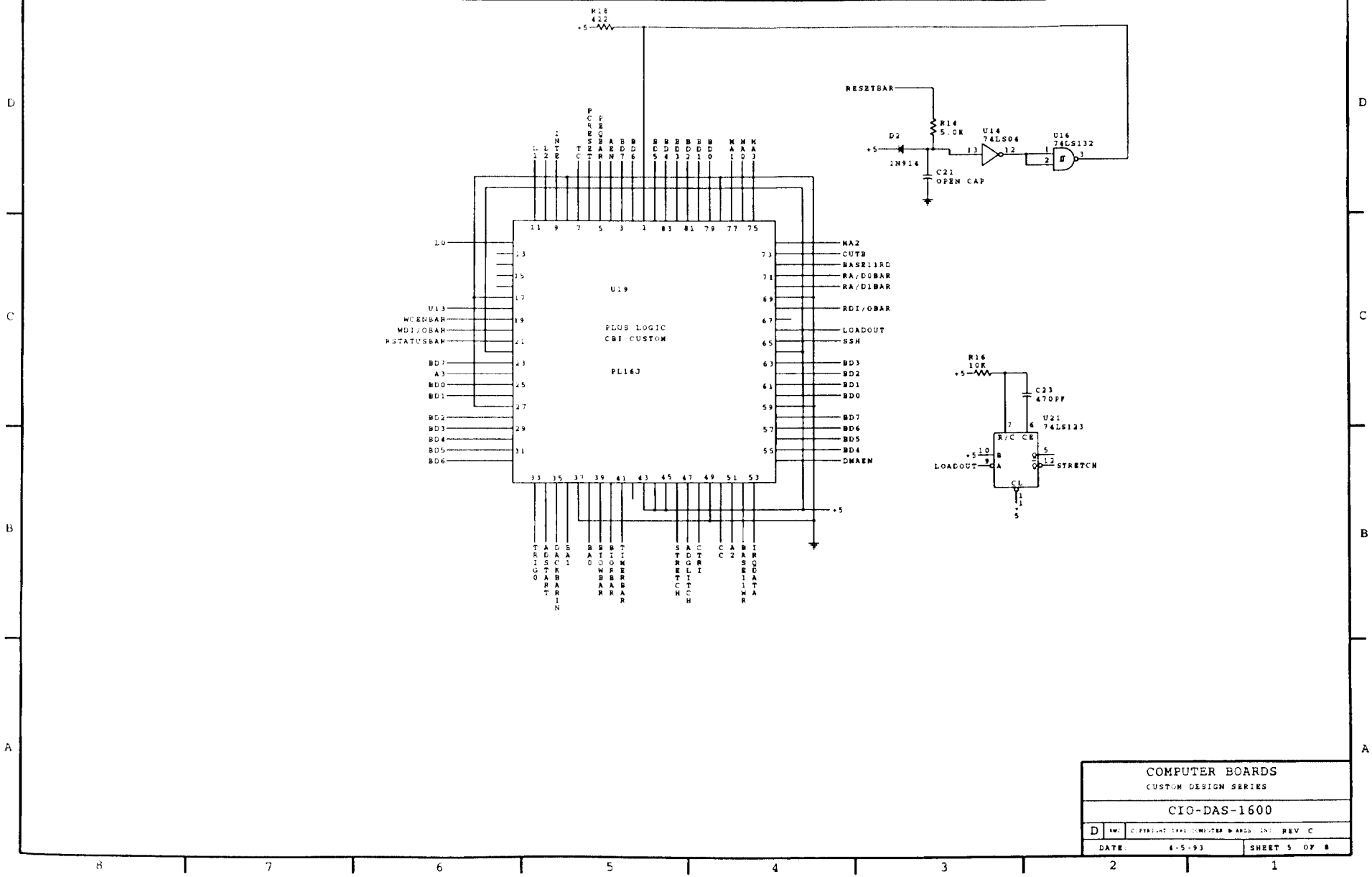
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DATE: 4-5-93

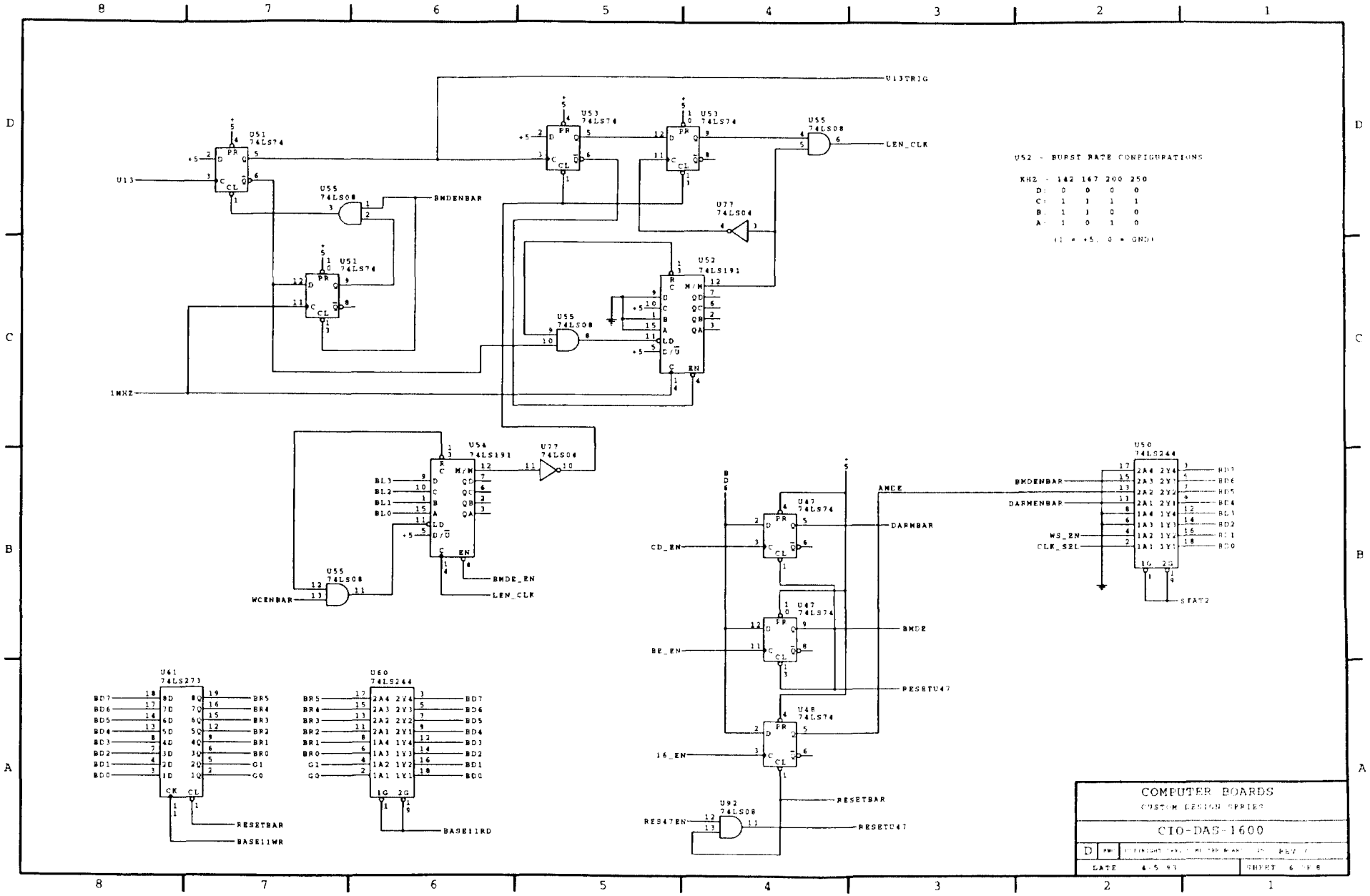

ADS7800 ANALOG FRONT END
COMPUTER BOARDS
CUSTOM DESIGN SERIES
CIO-DAS-1600
D
REV C
DATE: 4-5-93
SHEET 3 OF 8
0 OHM STRAP INSERTED TO 2-3
AD BUS
STSBAR
CONVERT
SMDPDT S5
SMDPDT S4
U17 74LS197
U40 74LS157
U79 LF444A
U8 OP07
U4 OP07
U5 HI508
U9 HI508
U1 74LS00
U15 74LS00
U13 PGA20
U2 7800
D37MR
J1
J7
R1 20K
R7 10K
R8 10K
R36 10K
R39 10K
R5 0 OHM
R95 0 OHM
R31 10K
C43
C29
RN3 SPRS-41
HD03E

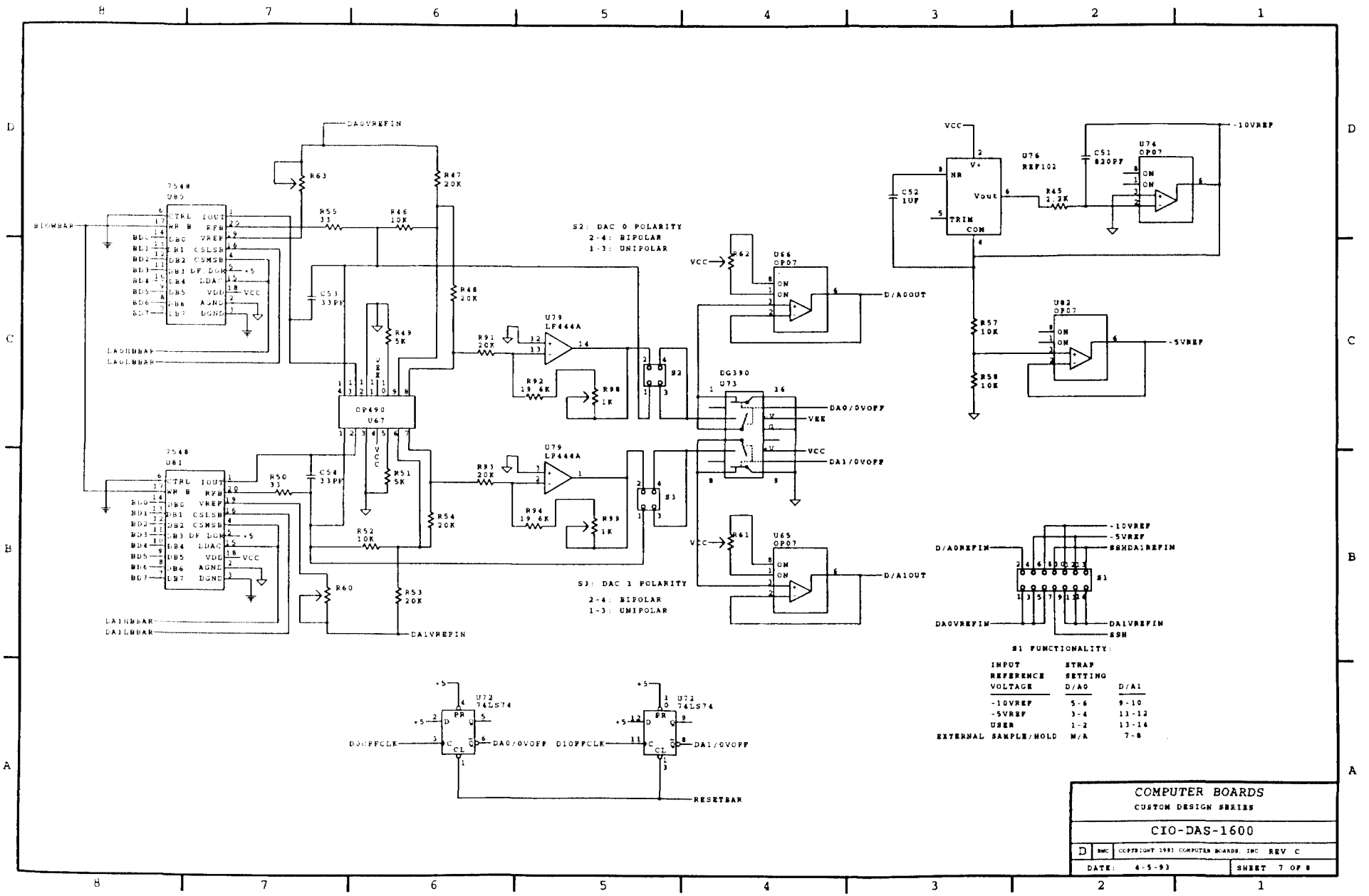


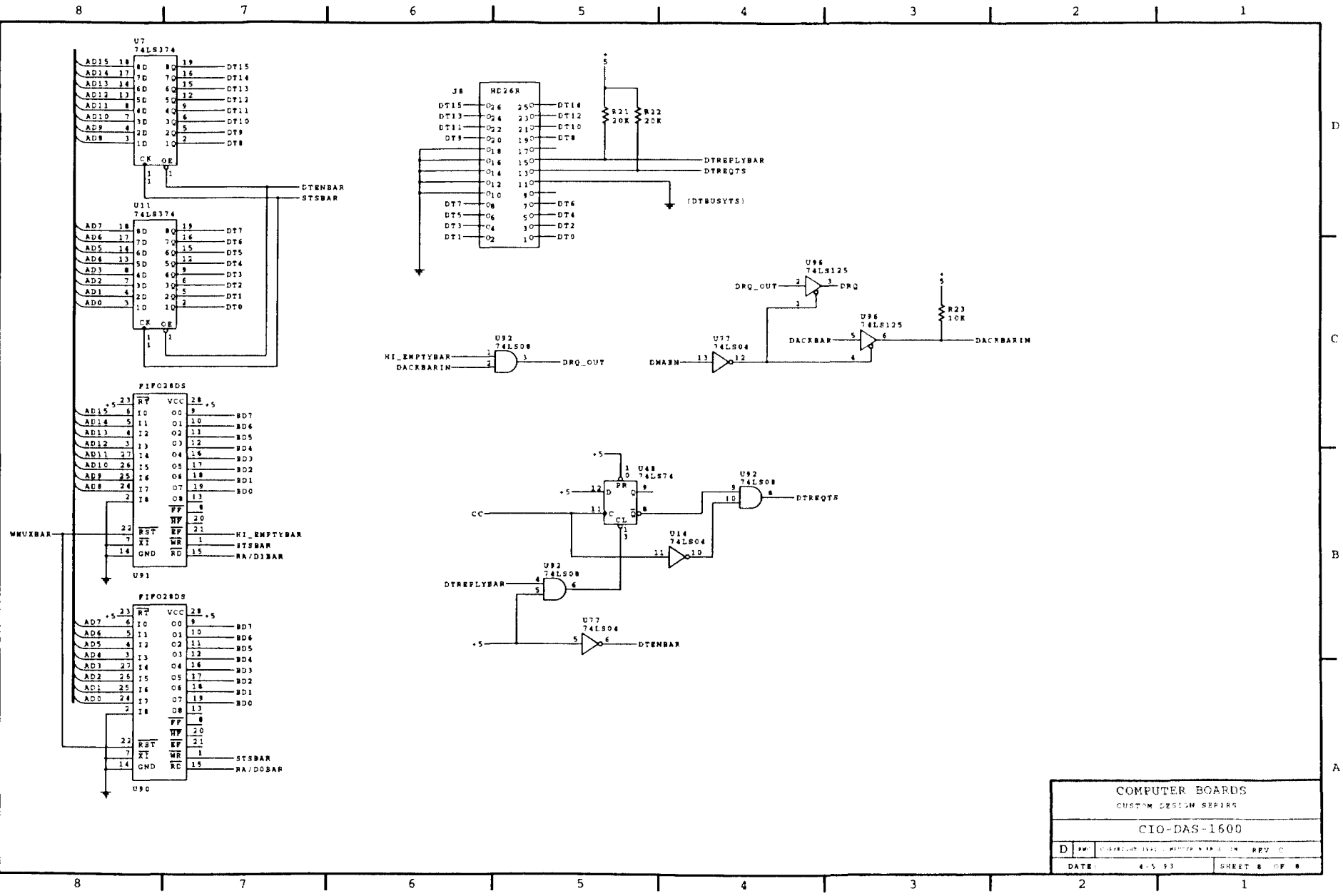
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CIO-DAS-1600		
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DATE: 4-5-93		SHEET 5 OF 8


U13TRIG
U51 74LS74
U53 74LS74
U55 74LS08
LEN_CLK
U13
BMDENBAR
U77 74LS04
U52 74LS191
1MHZ
U54 74LS191
BMDE_EN
WCENBAR
U47 74LS74
DARMBAR
CD_EN
BMDE
BE_EN
RESETU47
U48 74LS74
16_EN
RESETBAR
U92 74LS08
RES47EN
U50 74LS244
AMDE
DARMENBAR
WS_EN
CLK_SEL
STAT2
U61 74LS273
U60 74LS244
BASE11WR
BASE11RD
U52 - BURST RATE CONFIGURATIONS
KHZ - 142 167 200 250
D: 0 0 0 0
C: 1 1 1 1
B: 1 1 0 0
A: 1 0 1 0
(1 = +5, 0 = GND)
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CUSTOM DESIGN SERIES
CIO-DAS-1600
DATE 4 5 93


DA0VREFIN
R63
R47 20K
7548
U80
R55 33
R46 10K
BIOWBAR
C53 33PF
R48 20K
R49 5K
DA0HBBAR
DA0LBBAR
U79 LF444A
R91 20K
R92 19.6K
R98 1K
S2
OP490 U67
VCC
R50 33
C54 33PF
R51 5K
7548
U81
R54 20K
R52 10K
R60
R53 20K
DA1HBBAR
DA1LBBAR
DA1VREFIN
R93 20K
R94 19.6K
R99 1K
S3
S2: DAC 0 POLARITY
2-4: BIPOLAR
1-3: UNIPOLAR
S3: DAC 1 POLARITY
2-4: BIPOLAR
1-3: UNIPOLAR
VCC
R62
U66 OP07
D/A0OUT
DG390 U73
DA0/0VOFF
VEE
DA1/0VOFF
R61
U65 OP07
D/A1OUT
U76 REF102
C52 1UF
C51 820PF
U74 OP07
R45 2.2K
-10VREF
R57 10K
R58 10K
U82 OP07
-5VREF
D/A0REFIN
D/A1REFIN
S1
SSH
U72 74LS74
D0OFFCLK
D1OFFCLK
RESETBAR
S1 FUNCTIONALITY:
INPUT REFERENCE VOLTAGE
STRAP SETTING D/A0
STRAP SETTING D/A1
-10VREF 5-6 9-10
-5VREF 3-4 11-12
USER 1-2 13-14
EXTERNAL SAMPLE/HOLD N/A 7-8
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CIO-DAS-1600
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REV C
DATE: 4-5-93
SHEET 7 OF 8



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