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ISA-GPIB-PC2A

User's Manual



Revision 5
November, 2000

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1 INTRODUCTION

The ISA-GPIB-PC2A is a 100% compatible replacement for the National Instruments PCII, PCIIA and all other GPIB interfaces which are register and functionally compatible with them. To set up the ISA-GPIB-PC2A , set the switches and jumpers on the board to match the configuration of the GPIB interface board and software you currently use.

1.1 NATIONAL INSTRUMENTS PCII & PCIIA OWNERS

The ISA-GPIB-PC2A is easy to use if you are familiar with the National Instruments, Inc. PCIIA GPIB interface board. All of the ISA-GPIB-PC2A switches and jumpers are in the same location and have the same function as the PCIIA.

If you are using the National Instruments PCII board, you will find that the switches and jumpers are in a different location although the functions of the switches and jumpers on the NI PCII and PCIIA are nearly identical.

Because the ISA-GPIB-PC2A is designed to be 100% compatible with the NI PCIIA from the connector to the registers, and to look similar as well, references to the NI PCIIA board in this manual apply to the ISA-GPIB-PC2A also.

This manual supplies information on switch settings and jumper position for base address, DMA channel, interrupt level and wait state. Information on programming is found in the manual for the software package you intend to use with the ISA-GPIB-PC2A.

1.2 GPIB HISTORY

The GPIB (General Purpose Interface Bus) has become the worldwide standard for connecting instruments to computers. Invented in the 1960s by Hewlett Packard and originally designated as HPIB, the bus specification was eventually adopted by a wide variety of both instrument and computer manufacturers. The original specification was documented and sanctioned by the IEEE as IEEE-488.

The advent of the inexpensive and powerful personal computer has driven the GPIB market through explosive growth. As GPIB bus usage expanded, there arose the need for some additional capability and standardization, so in 1987, IEEE-488.2 was adopted. IEEE-488.2 was revised/ammended in 1992 and represents the current GPIB specification. The new specification provides some standardization among compliant instruments. This standardization greatly simplifies the job of the GPIB system designer since 488.2 compliant instruments share common programming conventions.

1.3 GPIB SYSTEM DESCRIPTION

1.3.1 Talkers, Listeners, and Controllers

A GPIB device can be a **Talker**, **Listener**, and/or **Controller**. As the name implies, a Talker sends data to one or more Listeners, A Listener accepts data from a Talker and a Controller manages the flow of information over the bus. A GPIB Digital Voltmeter is acting as a Listener as its input configurations and ranges are set, and then as a Talker when it actually sends its readings to the computer.

The Controller is in charge of all communications over the bus. The Controller's job is to make sure only one device tries to talk at a time, and make sure the correct Listeners are paying attention when the Talker talks. Each GPIB system has a single system controller. The system controller is ultimately in charge of the bus, and is in control as the bus is powered up. There can be more than one Controller on the bus and the System Controller can pass active control to another controller capable device, though only one can be Controller In Charge at a given time. The GPIB board is usually designated as the System Controller.

1.3.2 GPIB Electrical Signal Configuration

The GPIB is an 8-bit parallel data transfer bus. In addition to the eight data bits, the bus carries three handshaking lines and five GPIB specific management and control lines. The remainder of the standard 24-pin GPIB cable is used for the cable shield, signal grounds and returns. The GPIB connector pin-out is shown in Figure 1-1 below:

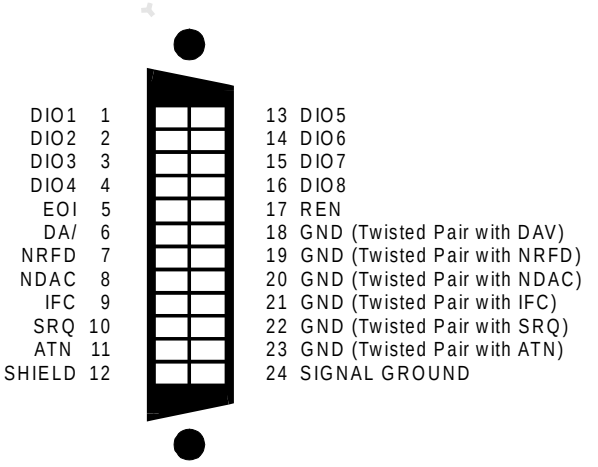


Figure 1-1 ISA-GPIB-PC2A Connector Pin-Out

1.3.3 Data Lines

DIO1 through DIO8 are the data transfer bits. Most GPIB systems send 7-bit data and use the eight bit as a parity or disregard it entirely

1.3.4 Handshaking Lines

There are three handshaking lines that control the data transfer between devices.

- **NRFD (Not Ready For Data):** this bit is used to indicate the readiness (or lack thereof) of a device to accept data
- **DAV (Data Valid):** bit is used to indicate to receiving devices that data has been placed on the bus and is available to read.
- **NDAC (Not Data Accepted):** is asserted by the receiving device to indicate that data has been read and may now be removed from the bus.

1.3.5 System Management Lines

- **ATN (Attention):** is used by the controller to specify how data on the DIO lines is interpreted and which devices must respond to the data
- **IFC (Interface Clear):** is used by the system controller to place the entire system in a known quiescent (Cleared) state and to assert itself as Controller In Charge (CIC).
- **SRQ (Service Request):** is used by a device on the bus to indicate the need for attention and requests an interrupt of the current event sequence.
- **REN (Remote Enable):** is used by the controller in conjunction with other messages to place a device on the bus into either remote or local mode
- **EOI (End or Identify):** Is used by Talkers to indicate the end of a message string, or is used by the Controller to command a polling sequence.

1.4 CONNECTION CONFIGURATIONS

The GPIB specification is quite definitive regarding the number of devices and cable lengths allowed in a GPIB system. There can be no more than 15 devices on a single contiguous GPIB bus. Larger systems are possible by installing additional GPIB interface boards in your computer

The maximum, total length of all cables on a single GPIB system is 20 meters. In addition, cable length between consecutive devices must be no greater than four meters, and average cable length must be two meters or less. Stated another way, the total cable length (in meters) in the system cannot be longer than two times the number of devices (up to 20 meters). Longer length systems are possible, but only

with the use of a GPIB extender card. In addition to the above rules, at least two-thirds of all devices on the bus should be powered on for proper operation.

Keeping the above constraints in mind, there is no limitation on the actual connection scheme used to connect the GPIB devices together. Star, Linear or any combination of both may be used. These are shown in Figures 1-2 and 1-3 below.

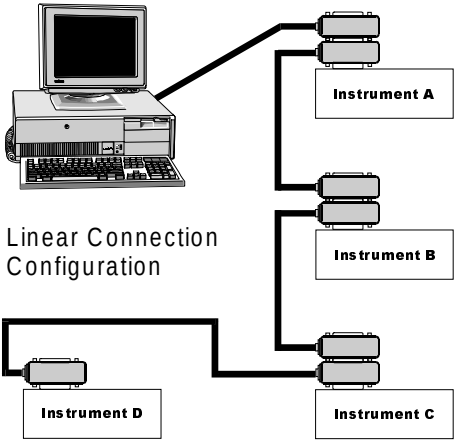


Figure 1-2. GPIB Linear Connection Configuration

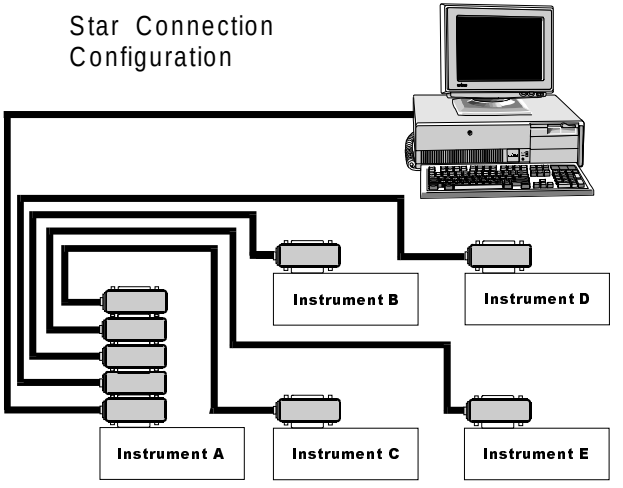
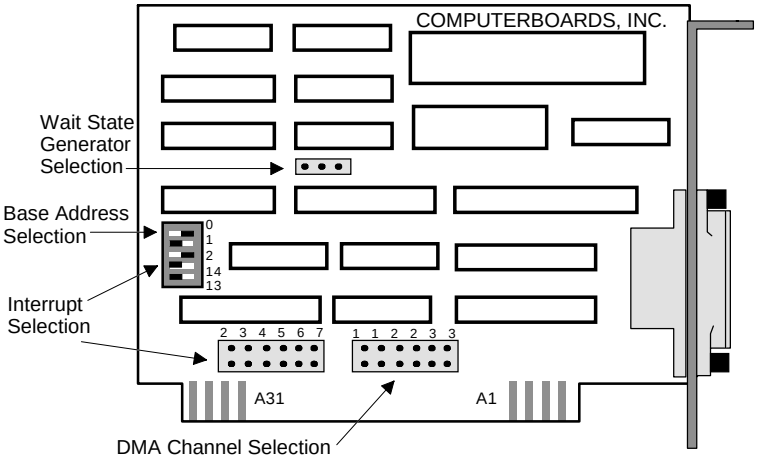


Figure 1-3. GPIB Star Connection Configuration

2 INSTALLATION

2.1 BOARD LAYOUT

The ISA-GPIB-PC2A has one bank of switches and three jumper blocks which must be set before installing the board in your computer.



ISA-GPIB-PC2A - Switch positions and functions are identical to those on the NI PCIIA.

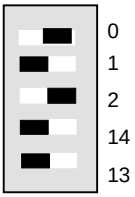
Figure 2-1. Board Switch and Jumper Locations

2.2 BASE ADDRESS

The base address of the ISA-GPIB-PC2A is set with the two switches labeled 14 and 13. Only four possible base addresses are available. In addition, there is considerable 'rollover', or addresses which are not deselected by the address enable circuitry of the ISA-GPIB-PC2A.

The default address chosen by National Instruments for the PCIIA was 02E1h, so that is the default setting for the ISA-GPIB-PC2A.

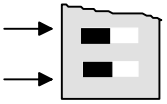
Unlike most other I/O boards, the National Instrument PCIIA uses nonconsecutive I/O addresses and the ISA-GPIB-PC2A does the same to maintain compatibility.



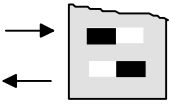
The ISA-GPIB-PC2A I/O address is selected using only the two lowest switches on the 5 position DIP switch.

The upper three switches are interrupt select switched.

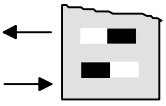
BASE ADDRESS = 02EI Both switches to the right.



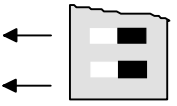
Base Address = 02E1



Base Address = 22E1



Base Address = 42E1



Base Address = 62E1

ISA-GPIB-PC2A BASE ADDRESS SWITCH

Figure 2-2. Base Address Switches

Following are the tables of addresses also used for a given setting. Be sure that any other I/O boards installed in your computer do not use one of these addresses.

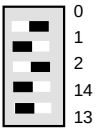
02E1	06E1	0AE1	0EE1	**22E1**	26E1	2AE1	2EE1
12E1	16E1	1AE1	1EE1	32E1	36E1	3AE1	3EE1
42E1	46E1	4AE1	4EE1	**62E1**	66E1	6AE1	6EE1
52E1	56E1	5AE1	5EE1	72E1	76E1	7AE1	7EE1

The ISA-GPIB-PC2A uses eight I/O Addresses.

2.3 INTERRUPT LEVEL SELECT

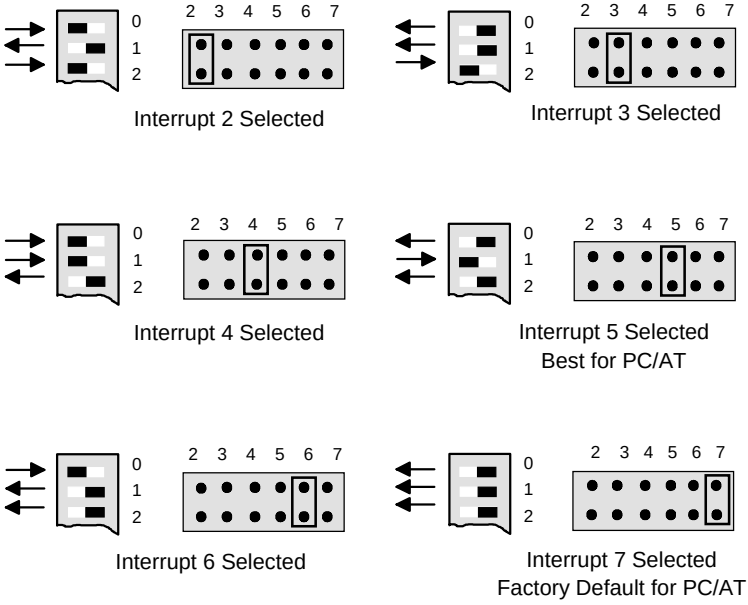
The interrupt used by the ISA-GPIB-PC2A is set with three switches, a jumper, and your software. **All three must match or interrupts will not function properly**.

The following table shows switch settings and jumper locations for each of the six possible interrupts, 2 to 7.



ISA-GPIB-PC2A Interrupt logic is controlled by a combination of switched 0, 1 & 2 and the interrupt jumper.

Switches 13 and 14, the lower two, select the base address.



The six possible switch settings and jumper locations for each of the interrupts, 2 to 7.

Figure 2-3. Interrupt Switch and Jumper Settings

National Instruments chose interrupt level 7 (IRQ7) as the default for the PCIIA. Your ISA-GPIB-PC2A is configured at the factory for IRQ7.

Although IRQ7 is acceptable, that interrupt is reserved for the LPT1: printer device. A better choice is IRQ5 on most machines.

2.4 WAIT STATE JUMPER & DMA JUMPERS

The ISA-GPIB-PC2A boards have a wait state jumper which enables an onboard wait state generator. A wait state is an extra delay injected into the processor's clock via the bus. This delay slows down the processor so that signals from slow devices (chips) will be valid. You will probably not need a wait state since the I/O bus is slowed down on even the fastest PCs. The default is no wait state selected.

The ISA-GPIB-PC2A can use DMA levels 1, 2, 3 or none. The factory default is level 1.

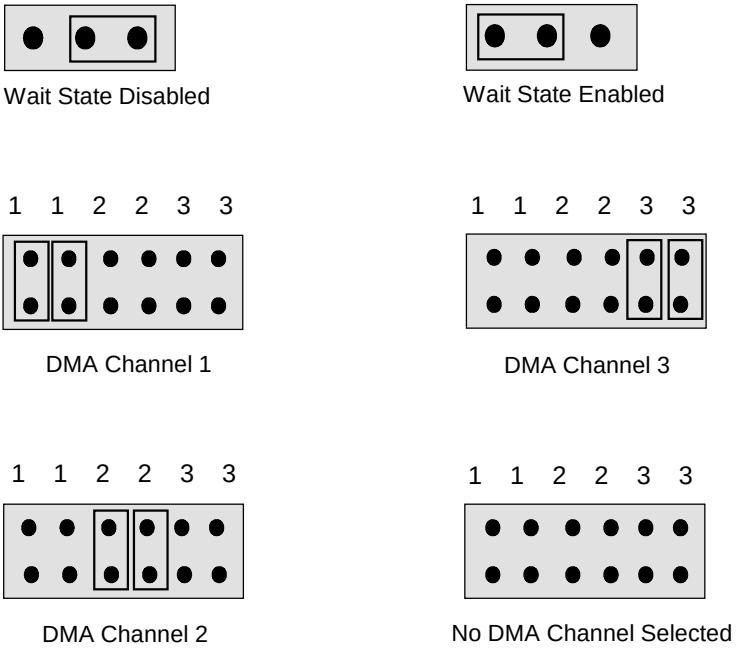


Figure 2-4. Wait State and DMA Select Jumpers

On PC/XT class machines, the hard disk controller usually occupies DMA level 3 and the floppy disk controller usually occupies level 2. Neither level 2 nor 3 are a good choice of DMA level on a PC/XT equipped with a floppy and hard disk.

On PC/AT/386 class computers, both DMA channels 1 and 3 are available.

3 REGISTER MAPS

3.1 ADDRESS DECODING

There are only four possible base addresses which can be selected using the switches on the ISA-GPIB-PC2A. Those four base addresses are shown below in bold type. For a given base address, the ISA-GPIB-PC2A registers appear at eight additional addresses within the personal computer's I/O address space.

Table 3-1. Board Base Addressing

02E1	06E1	0AE1	0EE1	**22E1**	26E1	2AE1	2EE1
12E1	16E1	1AE1	1EE1	32E1	36E1	3AE1	3EE1
42E1	46E1	4AE1	4EE1	**62E1**	66E1	6AE1	6EE1
52E1	56E1	5AE1	5EE1	72E1	76E1	7AE1	7EE1

If the addressing scheme in the table above appears confusing and unconventional, we agree, it is.

The addressing of the ISA-GPIB-PC2A is easiest to understand in relation to National's PCII board (NI PCIIA). Here are the addresses of the PCII board.

3.2 NI PCII REGISTERS (**NOT** ISA-GPIB-PC2A)

Table 3-2. NI PCII Registers

ADDRESS	WRITE	READ
Base + 0	Byte out register	Byte In register
Base + 1	Interrupt Mask 1 register	Interrupt Status 1 register
Base + 2	Interrupt Mask 2 register	Interrupt Status 2 register
Base + 3	Serial Poll Mode register	Serial Poll Status register
Base + 4	Address Mode register	Address Status register
Base + 5	Auxiliary Mode register	Command Pass-through register
Base + 6	Address Register 0/1	Address 0 register
Base + 7	End-Of-String register	Address 1 register

The addressing of the PCII is easy to understand. A Base-Address-Switch selects the boards Base Address and the register functions on the board occupy consecutive I/O addresses. Eight of them in total.

Complete descriptions of each register and it's functions follow in a later section.

Back to the ISA-GPIB-PC2A (NI PCIIA). The registers on the ISA-GPIB-PC2A are the same as those of the NI PCIIA shown below. The logic of the address decoding is very different. The eight registers are not consecutive. The registers are offset by 400h between each register.

3.3 ISA-GPIB-PC2A (NI PCIIA) REGISTERS

Table 3-3 ISA-GPIB-PC2A (NI PCIIA Registers

ADDRESS	WRITE	READ
Base +0	Byte out register	Byte In register
Base +400	Interrupt Mask 1 register	Interrupt Status 1 register
Base +800	Interrupt Mask 2 register	Interrupt Status 2 register
Base +C00	Serial Poll Mode register	Serial Poll Status register
Base +1000	Address Mode register	Address Status register
Base +1400	Auxiliary Mode register	Command Pass-through register
Base +1800	Address Register 0/1	Address 0 register
Base +1C00	End-Of-String register	Address 1 register
2F0 + IR	Interrupt clear bit	

Table 3-4 below is an example of the actual physical register addresses for a ISA-GPIB-PC2A board Base Address of 02E1.

3.4 ISA-GPIB-PC2A (NI PCIIA) REGISTERS

Table 3-4. Physical Register Addresses for Board Base Address 02E1

ADDRESS	WRITE	READ
02E1	Byte out register	Byte In register
06EI	Interrupt Mask 1 register	Interrupt Status 1 register
0AEI	Interrupt Mask 2 register	Interrupt Status 2 register
0EE1	Serial Poll Mode register	Serial Poll Status register
12E1	Address Mode register	Address Status register
16E1	Auxiliary Mode register	Command Pass-through register
1AE1	Address Register 0/1	Address 0 register
1EE1	End-Of-String register	Address 1 register

3.5 CONVERTING PCII DRIVERS FOR THE ISA-GPIB-PC2A

If you are working with your own PCII driver, converting it for the ISA-GPIB-PC2A, is an easy task. The register functions of the PCII and ISA-GPIB-PC2A (NI PCIIA) are identical, the addressing is very different. Refer to the prior descriptions to learn how different.

If you have hard-coded all the addresses into your driver, converting your driver to work with both the PCII and ISA-GPIB-PC2A will require that you replace all the hard-coded addresses with variables.

If you have referenced all other addresses as an offset from the base address, such as IN Base+4 or OUT Base+7, you will have to replace each such reference with variable names. Table 3-5 is a list of proposed variable names.

Table 3-5. Proposed ISA-GPIB-PC2A Registers Mnemonics

ADDRESS	WRITE		READ	
Base + 0	BOR	Byte Out	BIR	Byte In
Base + 400	IRM1	Interrupt Mask 1	IRS1	Interrupt Status 1
Base + 800	IRM2	Interrupt Mask 2	IRS2	Interrupt Status 2
Base + C00	SPM	Serial Poll Mode	SPS	Serial Poll Status
Base + 1000	ADM	Address Mode	ASR	Address Status
Base + 1400	AMR	Auxiliary Mode	CPT	Command Pass-through
Base + 1800	A01	Address 0/1	A0R	Address 0
Base + 1C00	EOS	End-Of-String	A1R	Address 1
2F0 + IR	Interrupt clear bit			

After all the register functions have unique variable names, and all IN and OUT statements reference the variable names and not a hard address or merely an offset from the base address, you can implement the following code to fix the addresses in the variable for PCII or ISA-GPIB-PC2A boards.

```
BASEADR = 02E1
;
; If PCII then REGOFFSET = 1
; If PC2A then REGOFFSET = 400h
REGOFFSET = 400h
;
;Write registers.
;
BOR  =          BASEADR+(0 * REGOFFSET)
IRM1 =          BASEADR+(1 * REGOFFSET)
IRM2 =          BASEADR+(2 * REGOFFSET)
SPM  =          BASEADR+(3 * REGOFFSET)
ADM  =          BASEADR+(4 * REGOFFSET)
AMR  =          BASEADR+(5 * REGOFFSET)
A01  =          BASEADR+(6 * REGOFFSET)
EOS  =          BASEADR+(7 * REGOFFSET)
```

```
;
;               Read registers.
;
BIR   =         BASEADR+(0 * REGOFFSET)
IRS1  =         BASEADR+(1 * REGOFFSET)
IRS2  =         BASEADR+(2 * REGOFFSET)
SPS   =         BASEADR+(3 * REGOFFSET)
ASR   =         BASEADR+(4 * REGOFFSET)
CPT   =         BASEADR+(5 * REGOFFSET)
A0R   =         BASEADR+(6 * REGOFFSET)
A1R   =         BASEADR+(7 * REGOFFSET)
```

For your notes.

For your notes.

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Part Number	Description
ISA-GPIB-PC2A	GPIB Interface board

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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