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Specifications

PCI-DAS4020/12



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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

Analog input

Table 1. Analog input specifications

A/D converter type	AD9225, 25 MSPS pipelined A/D
Resolution	12-bits
Programmable ranges	±5 V, ±1 V
Number of channels	4 single-ended, independent ADC's per channel
Connection	4 independent BNC
Bandwidth	17 MHz typical
Coupling	DC
Input leakage current	*2 uA typ, 10 uA max*
Input impedance	1.5 Mohm typ, or 50 ohm, selectable (coaxial cable termination)
Absolute maximum input voltage	±15 V

Timing and throughput

Table 2. Timing and throughput specifications

Simultaneous sampling	Software selectable option - 1, 2, or 4 channels	
A/D Convert clock source	Internal:	On-card crystal oscillator Frequency: 40 MHz Frequency accuracy: 50% duty cycle, 50 ppm
	External:	Trig/Ext Clk BNC, or A/D External Clock on the 40-pin connector 24-bit internal pre-scale counter (min pre-scale = 2) Clock Rate: 40 MHz max, 2 kHz min Duty Cycle: 50% ± 5%
A/D Gate source	Digital: Analog:	Trig/Ext Clk BNC or A/D Pacer Gate on 40-pin connector Any of the four input channels
A/D Gate modes	Digital: Analog:	Programmable active high/low, level/edge Above/below reference, positive/negative Hysteresis, inside/outside window Resolution: 12-bit Slew rate: 10V/sec. minimum
A/D Start Trigger (TRIG1)	Software: Digital: Analog:	Using a DAQ start command. Trig/Ext Clk BNC, A/D Start Trigger In (on the 40-pin connector) Any of the four input channels
A/D Stop Trigger (TRIG2)	Digital: Analog:	Trig/Ext Clk BNC, A/D Stop Trigger In (on the 40-pin connector) Any of the four input channels
A/D Triggering modes	Digital: Analog:	Programmable rising or falling edge Trigger above/below reference Resolution: 12-bit
Pre-trigger mode	Unlimited number of pre-trigger samples, 16 Meg post-trigger samples. Compatible with both digital and analog trigger/gate options. Data acquisition initiated via TRIG1. Post-trigger phase initiated via TRIG2.	

Data transfer	Via dual 32 K x 24 sample FIFO, SRAM based, with Bus-Master DMA and scatter-gather, interrupt, or software polled.
A/D Conversion time	40 ns
Sample rate	20 MHz max, 1 kHz min
Throughput	Single channel: 20 MHz continuous Two channels (0 and 1 or 2 and 3): 20 MHz continuous Four channels: 10 MHz continuous In background mode, the maximum throughput may be impacted by bus or interrupt activity.

Accuracy

Table 3. Analog input accuracy specifications

Absolute accuracy		±5.5 LSB worst case error (either range)
Typical accuracy		±3.0 LSB error (either range)
Accuracy components:		
	Gain error	±2.0 LSB max, ±1.0 LSB typ
	Offset error	±1.5 LSB max, ±1.0 LSB typ
	Integral linearity error	±2.5 LSB max, ±1.0 LSB typ
	Differential linearity error	*±1.0 LSB max , ±0.4 LSB typ (No missing codes guaranteed)*

Board error is a combination of gain, offset, integral linearity, and differential linearity error. The overall absolute worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are both at their maximum level, and causing error in the same direction. Though this is very uncommon, it is still possible, and the calculated worst case error of the PCI-DAS4020/12 board is ±7.0 LSB.

Each PCI-DAS4020/12 board is tested at the factory to make sure that its actual worst case error is less than ±5.0 LSB. Allowing for a 10% guard-band, the absolute worst-case error of a board is ±5.5 LSB. Typical accuracy can be calculated from the various component typical errors in a similar fashion. This typical maximum error calculation for the PCI-DAS4020/12 board yields ±3.4 LSB. However, this again assumes that each of the errors is forcing an error in the same direction. Empirical evidence supports a conservative typical error budget of ±3.0 LSB.

Table 4. Calibration specifications

Calibration	Auto-calibration. Calibration factors for each range stored on board in non-volatile RAM

Temperature

Table 5. Temperature specifications

Gain drift	±5 V range: ±0.10 LSB/°C max ±1 V range: ±0.13 LSB/°C max
Offset drift	±0.11 LSB/°C max, all ranges
Overall board temperature drift	±5 V range: ±0.21 LSB/°C max ±1 V range: ±0.24 LSB/°C max

Overall, worst-case temperature drift is calculated by adding the drifts corresponding to the gain and offset drifts. This worst case number is unlikely to occur, as it requires both gain and offset drifts to be at their maximum levels, and to be affecting the measurement in the same direction. However, the overall board D/A drift specifications have been calculated in this fashion.

Dynamics and noise

Table 6. Dynamics and noise specifications

SNR (Signal-to-noise ratio)		66.6 dB
SINAD (signal-to-noise and distortion ratio)		66.5 dB
SFDR (spurious free dynamic range)		80 dB
THD (total harmonic distortion)		80 dB
Noise distribution:		
(Rate = 10 KHz-20 MHz, Average % ± 2 bins, Average % ± 1 bin, Average # bins)	Bipolar (5V):	100% / 98% / 5 bins
	Bipolar (1V):	100% / 98% / 5 bins

Trig/Ext Clk BNC

Software selectable for A/D Start Trigger (TRIG1), A/D Stop Trigger (TRIG2) or A/D Pacer Gate (AGATE); also used as an A/D clock input 2X clock source (DAQ_CLK).

Table 7. Trig/Ext Clk BNC specifications

Input impedance	50 ohm, 1 Mohm selectable (coaxial cable termination)
Input threshold	Programmable 2.5 V threshold or 0 V threshold
Input slew rate	1 V/µsec min
Input range	±5 V
Bandwidth	40 MHz
Coupling	DC

Analog output

Table 8. Analog output specifications

D/A converter type	AD7237
Resolution	12-bits
Number of channels	2
Output range	±10 V, ±5 V software selectable
D/A pacing	Software paced
Throughput	System dependent. Using the Universal Library programmed output function (`cbAout`) in a loop in Visual Basic, a typical update rate of 500 Hz (± 50 Hz) can be expected. The rate was measured on a 330 MHz Pentium II based PC.
Data transfer	Programmed I/O

Accuracy

Table 9. Analog output accuracy specifications

Absolute accuracy	±13 LSB max
Offset error	±6 LSB max
Gain error	±5 LSB max
Differential non-linearity	±1 LSB max
Integral non-linearity	±1 LSB max

Total analog output error is a combination of gain, offset, integral linearity, and differential linearity error. The overall absolute worst-case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors are both at

their maximum level, and causing error in the same direction. Though this is very uncommon, it is still possible.

Monotonicity	Guaranteed monotonic over temperature
Analog output drift	±0.11 LSB/°C max, all ranges
Settling time (20 V step to ± ½ LSB)	5µs max
Slew rate	5 V/µs
Current drive	±5 mA
Output short-circuit duration	25 mA indefinite
Output coupling	DC
Output impedance	0.5 Ohm max
Miscellaneous	Single buffered output latch Update DACs individually On power-up and reset, the inputs to both D/A output buffers are grounded and the board's D/A outputs will be set to 0 volts ± 6 mV. Upon writing to the D/A converters, the output buffers will reflect the D/A outputs and achieve rated accuracy. However, upon writing a 0 to the D/A's, a small output change may be noted (up to 10 LSB).

Digital input / output

Table 10. DIO specifications

Digital type (40-pin connector)	8255A
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output high	3.0 volts min @ 2.5 mA
Output low	0.4 volts max @ 2.5 mA
Input high	2.0 volts min, Vcc + 0.5 volts absolute max
Input low	0.8 volts max, GND – 0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)

Interrupts

Table 11. Interrupt specifications

Interrupts	INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Software programmable
ADC Interrupt sources	DAQ_ACTIVE: Interrupt is generated when a DAQ sequence is active. DAQ_STOP: Interrupt is generated when A/D Stop Trigger In is detected. DAQ_DONE: Interrupt is generated when a DAQ sequence completes. DAQ_FIFO_1/2_FULL: Interrupt is generated when ADC FIFO is ½ full. DAQ_SINGLE: Interrupt is generated after each conversion completes.
External	Interrupt is generated via edge-sensitive transition on the Interrupt In pin on the 40-pin connector. Rising/falling edge polarity selection. The Interrupt In pin is pulled up to 5 V through a 10 K resistor.
External Interrupt Enable	Active low Interrupt Enable signal on the 40-pin connector. The Interrupt Enable pin is pulled up to 5 V through a 10 K resistor.

Environmental

Table 12. Environmental specifications

Operating temperature range	0 to 70 °C
Storage temperature range	–40 to 100 °C
Humidity	0 to 90% non-condensing

Power consumption

Table 13. Power consumption specifications

+5 V Operating (A/D to FIFO)	1.5 A typical, 2.0 A max

Connector and pin out

Table 14. Connector specifications

Connector type	BNC connector: five standard female connectors Auxiliary connector (P3): 40-pin header connector
Compatible cables (for the 40-pin auxiliary connector)	C40FF-x
	C40-37F-x
	BP40-37-x
Compatible accessory products (with the C40FF-x cable)	CIO-MINI40
Compatible accessory products (with the C40-37F-x cable) OR (with the BP40-37-x and the C37FF-x or C37FFS-x cable)	CIO-MINI37 SCB-37 CIO-ERB24 CIO-ERB08 SSR-RACK24 SSR-RACK08

Auxiliary connector P3 pinout

Table 15. Auxiliary connector (P3) pin out

Pin	Signal Name	Pin	Signal Name
1	INTERRUPT IN *	2	+5V
3	INTERRUPT ENABLE *	4	GND
5	Port B 7	6	Port C 7 (A/D Pacer Gate)
7	Port B 6	8	Port C 6 (A/D Stop Trigger In)
9	Port B 5	10	Port C 5 (Start Trigger In/Ext Clock)
11	Port B 4	12	Port C 4
13	Port B 3	14	Port C 3
15	Port B 2	16	Port C 2
17	Port B 1	18	Port C 1
19	Port B 0	20	Port C 0
21	GND	22	Port A 7
23	n/c	24	Port A 6
25	GND	26	Port A 5
27	n/c	28	Port A 4
29	GND	30	Port A 3
31	n/c	32	Port A 2
33	GND	34	Port A 1
35	+5V	36	Port A 0
37	GND	38	D/A GND
39	D/A OUT 0	40	D/A OUT 1

***** Pins 1 and 3 have 10 K pull-up resistors installed.

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