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PCI-DAS4020/12

User's Manual

ComputerBoards, Inc.

Revision 1, April, 2000

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Table of Contents

1. INTRODUCTION AND PRODUCT DESCRIPTION 1

1.1 INTRODUCTION 1
1.2 ANALOG SIGNAL PATH 2
1.3 ANALOG OUTPUT SECTION 2
1.4 ANALOG OUTPUT SECTION - BLOCK DIAGRAM (FIGURE 1-2) 3
1.5 DIGITAL I/O SECTION 3
1.6 POWER DISTRIBUTION SECTION 3

2. INSTALLATION 4

3. CONNECTIONS 5

4. PROGRAMMING AND APPLICATIONS 7

4.1 PROGRAMMING LANGUAGES 7
4.2 PACKAGED APPLICATIONS PROGRAMS 7

5. REGISTER DESCRIPTION 8

5.1 PCI-DAS4020/12 MEMORY MAP 8
5.2 LOCALSPACE0 WRITE-ONLY REGISTERS 9
5.3 LOCALSPACE0 READ-ONLY REGISTERS 9
5.4 LOCALSPACE0 READ/WRITE REGISTERS 9
5.4.1 LocalSpace0 Read/Write Registers 10
5.4.2 LocalSpace0 Serial Devices 10
5.4.3 Register Descriptions – Detailed 10
5.4.4 LocalSpace0 Write-only Registers 10
5.4.5 I2C INTERFACE: 21

6. INITIATING A/D CONVERSIONS 23

6.1 DEFINITIONS AND IMPLEMENTATION 23
6.2 INITIATING CONVERSION VIA THE BNC CONNECTION: RELATED PIN DESCRIPTIONS 24
6.3 INITIATING CONVERSION VIA ANALOG INPUT BNC CONNECTIONS: 24

7. CALIBRATION 25

CALIBRATING THE PCI-DAC4020/12 25

8. SPECIFICATIONS 26

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1. INTRODUCTION AND PRODUCT DESCRIPTION

1.1 INTRODUCTION

The PCI-DAS4020/12 (Figure 1-1) is a multi-function I/O board. It consists of the following:

1. Four high-speed analog input channels. Each channel can be configured by software for an input range of +/-1V or +/-5V. Resolution is 12 bits. Throughput is 10 to 20 MHz depending on the number of channels accessed. Triggering sources are by hardware or software, internal or external, and four different modes are software selectable. A/D gating is likewise by either hardware or software, internal or external. Input connectors are BNC types. Refer to the specifications in this manual for full details.
2. Two analog output channels. Each channel can be configured by software for an output range of +/-10V or +/-5V. Resolution is 12 bits. Throughput is system-dependent. Triggering mode is software gate. D/A pacing is software. Refer to the specifications in this manual for full details.
3. Twenty-four digital I/O channels. The I/O chip type is 82C55A configured as two banks of eight and two banks of four, programmable by bank as input or output. Signal levels are TTL. The digital I/O and analog out connector is a 40-pin header.

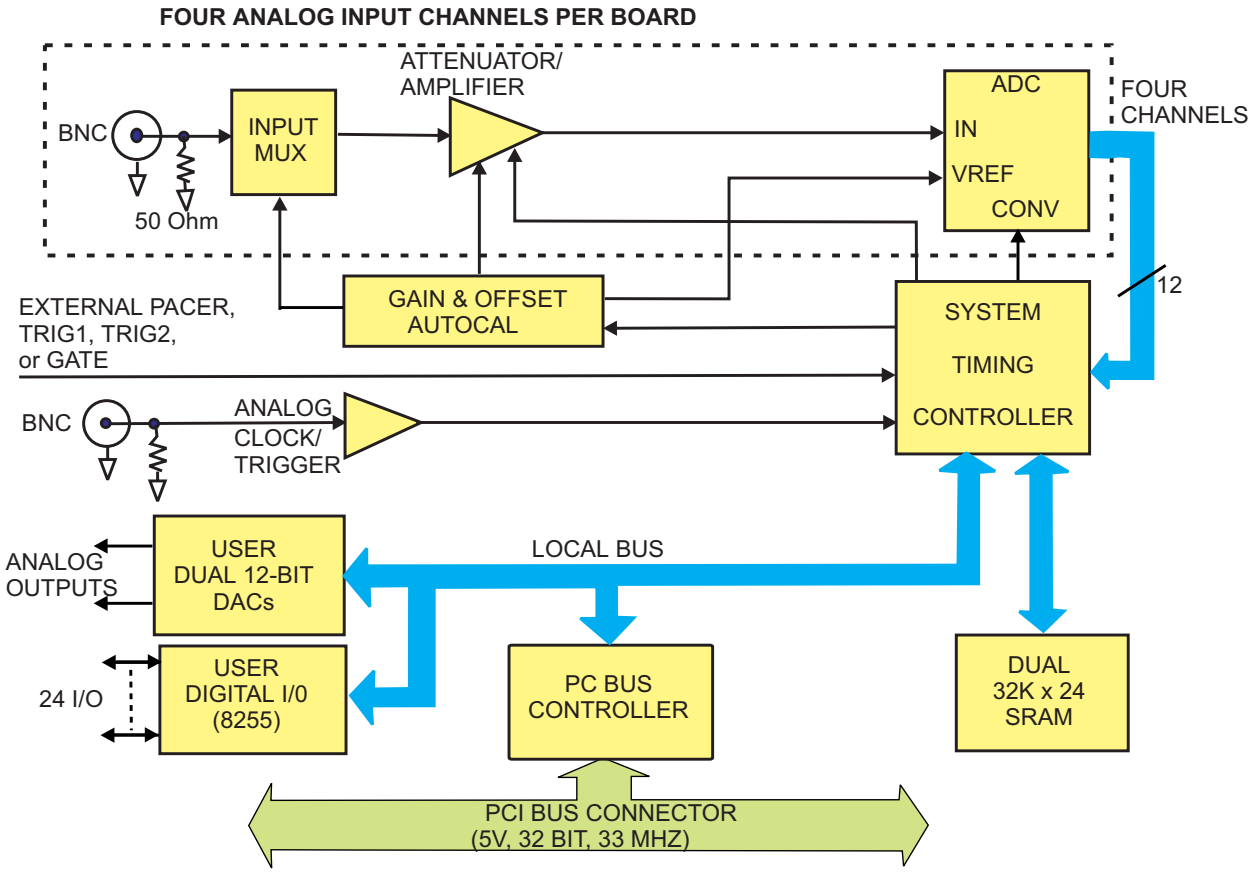


Figure 1-1. PCI-DAS4020/12 Block Diagram

1.2 ANALOG SIGNAL PATH

Four single-ended analog input channels connect from BNC connectors to individual amplifiers, then to dedicated ADC's. Each path allows for:

- 50 ohm or high-Z termination, selected by solder gap;
- +/-1V or +/-5V bipolar ranges, software-selectable (Table 1-1);
- Auto-calibration for offset and gain adjustments for each channel and each range.

Table 1-1. Input Range

FULL SCALE INPUT RANGE	ATTENUATION	DIVIDER **OUTPUT**
+5V to -5V	5	+/-1V
+1V to -1V	1	+/-1V

1.3 ANALOG OUTPUT SECTION

Two 12-bit voltage outputs are software programmable for +/- 10V or +/- 5V. The D/A is the Analog Devices AD7237 Dual DAC. Since the DAC is dual buffered, the DAC output voltage is updated after the MS nibble is written to the DAC.

The DACs initially power-up and are reset to 0V.

There is no calibration on these DACs. The offset and gain errors are minimized by using precision components in Table 1-2 shows the DAC input coding.

Table 1-2. DAC Input Coding

DAC RANGE	INPUT CODE BINARY	12 BIT INPUT CODE HEX	12 BIT OUTPUT VOLTAGE
+/- 10V	0000 0000 0000	000h	–10.000 V
+/- 10V	1000 0000 0000	800h	0 V
+/- 10V	1111 1111 1111	FFFh	+9.99513 V
+/- 5V	0000 0000 0000	000h	–5.000 V
+/- 5V	1000 0000 0000	800h	0 V
+/- 5V	1111 1111 1111	FFFh	+4.99756 V

1.4 ANALOG OUTPUT SECTION - BLOCK DIAGRAM (FIGURE 1-2)

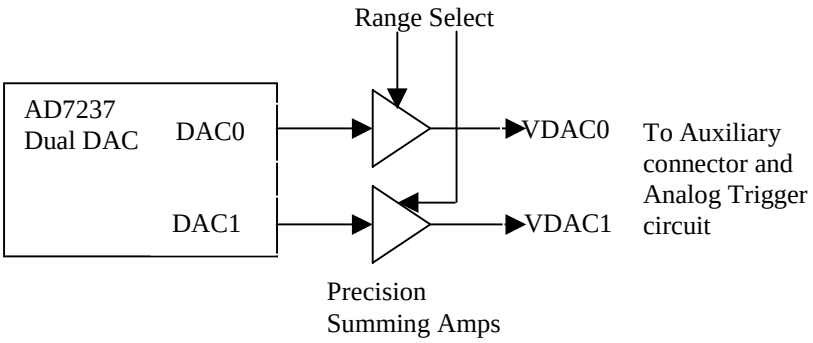


Figure 1-2. Analog Output Block Diagram

1.5 DIGITAL I/O SECTION

The digital I/O is comprised of an 82C55 digital logic device. The pinout is identical to the auxiliary DIO24 on a 40-pin header (P3).

For external interrupts, an external interrupt source pin and external interrupt enable pin are provided on connector P3. These lines are pulled up and OR'ed to generate the external interrupt signal. Both are active low.

1.6 POWER DISTRIBUTION SECTION

Power for the board is from the PCI bus. The only power used is +5V.

2. INSTALLATION

The PCI-DAS4020/12 is completely plug and play. There are no switches or jumpers to set. Configuration is controlled by your systems' BIOS. Simply turn off your PC, open it up and insert the PCI-DAS4020/12 into any available PCI slot.

If you are using an operating system with support for Plug and Play (such as Windows 95 or 98), a dialog box will pop up as the system loads indicating that new hardware was detected. If the information file for this board is not already loaded onto your PC, you are prompted for a disk containing it. The *Insta*Cal™ software supplied with your board contains this file. Just insert the disk or CD and click OK.

To easily test your installation, install I*nsta*Cal, the installation, calibration, and test utility supplied with your board. Refer to the *Software Installation Manual* for information on the initial setup, loading, and installation of *Insta*Cal and optional universal library™ software.

Figure 3-1 shows the pinout for the 40-pin connector. Figure 3-2 shows the *Analog Inputs* and *Trigger In* BNC connectors.

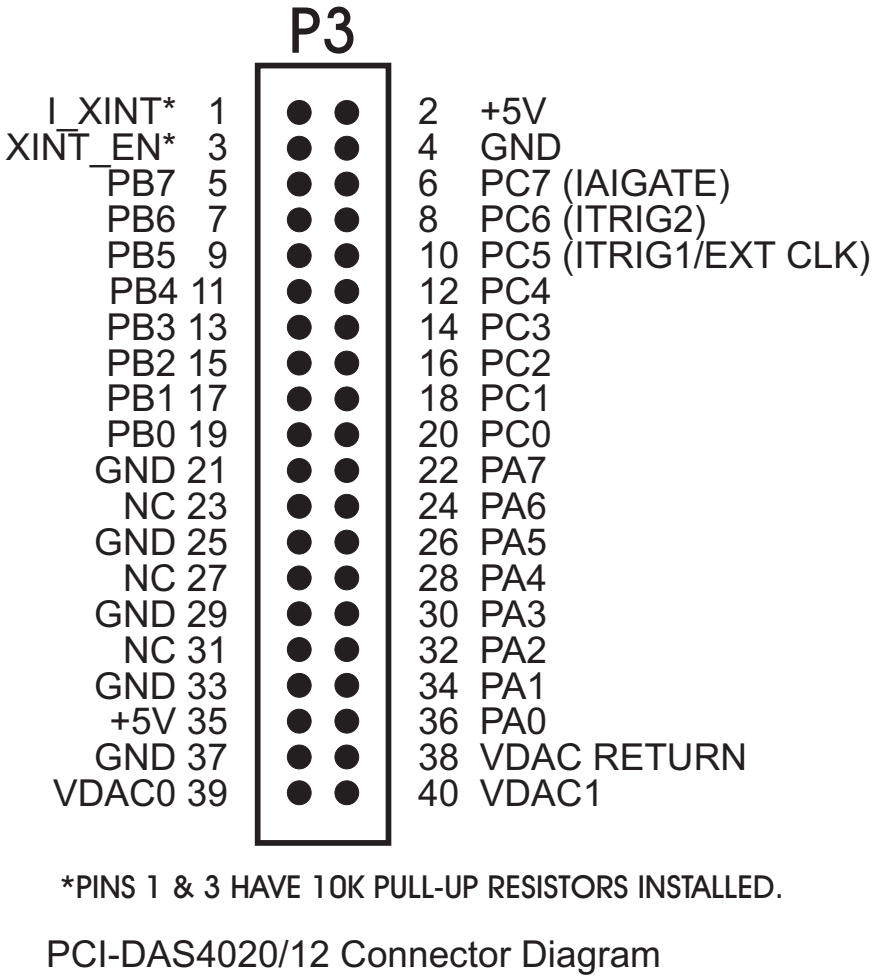


Figure 3-1. 40-Pin Connector

NOTE: When using analog outputs VDAC0 and VDAC1, use VDAC RETURN only (pin 38) for the return.

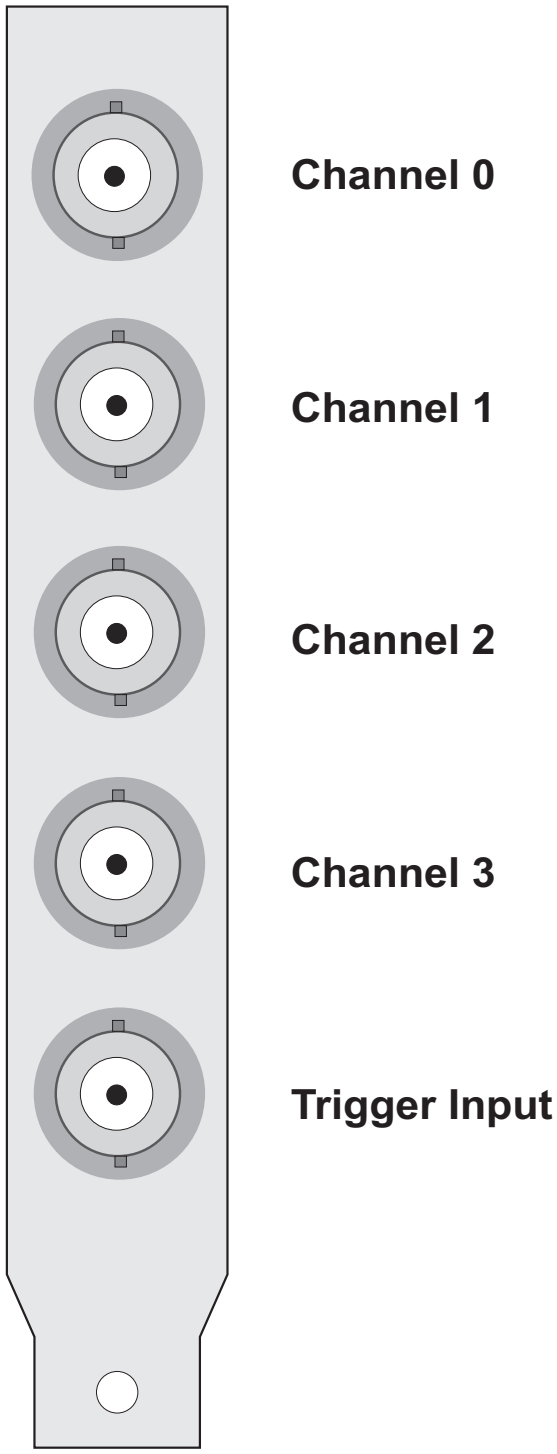


Figure 3-2. Analog Inputs and Trigger Input BNC Connectors

4. PROGRAMMING AND APPLICATIONS

After following the installation instructions, your PCI-DAS4020/12 is ready for use. Although the board is part of the larger DAS family, there is no correspondence between registers. Software written at the register level for other DAS models will not work with the PCI-DAS4020/12.

4.1 PROGRAMMING LANGUAGES

The ComputerBoards Universal Library™ provides complete access to the PCI-DAS4020/12 functions from a variety of Windows programming languages. If you are planning to write programs, or would like to run the example programs for Visual Basic or any other language, please refer to the Universal Library manual.

VIX Components is a set of programming tools based on a DLL interface to Windows languages. A set of VBX, OCX or ActiveX interfaces allows point-and-click construction of graphical displays, analysis and control structures. Please refer to the catalog for a complete description of the package.

4.2 PACKAGED APPLICATIONS PROGRAMS

Many packaged application programs, such as DAS-Wizard™, Labtech Notebook™, and HP-VEE™, now have drivers for the PCI-DAS4020/12. If the package you own does not appear to have drivers for the board, please fax or e-mail the package name and the revision number from the install disks. We will research the package for you and advise how to obtain PCI-DAS4020/12 drivers.

Some application drivers are included with the Universal Library package, but not with the Application package. If you have purchased an application package directly from the software vendor, you may need to purchase our Universal Library and drivers. Please contact us for more information on this topic.

5. REGISTER DESCRIPTION

5.1 PCI-DAS4020/12 MEMORY MAP

Table 5-1 lists PCI Base Address Assignments.

Table 5-1. PCI Base Address Assignments

Memory Region	Function	Operations
BAR0	PLX 9080 PCI controller operation registers	32-bit DWORD
BAR2	PCI-DAS4020/12 16-bit registers	16-bit WORD
BAR3	PCI-DAS4020/12 FIFO	32-bit DWORD

Any operations to the PLX 9080 PCI controller registers at BAR0 require a thorough understanding of the 9080 chip specification. Detailed descriptions of 9080 operation are beyond the scope of this document. The interested reader is encouraged to obtain the "PLX New Products Catalog, February 1998" for detailed programming information.

The PLX 9080 provides internal address decoding which allows remapping of BAR2 and BAR3 to convenient Local Address values. This eases the burden of Local Bus address decoding. The remap and space-specific parameters for the PCI-DAS4020/12 are summarized in Table 5-2 below:

Table 5-2. Address Remap

PCI BAR	Space	Width	Burst Enabled	Size	Remap Address
BAR2	Registers	16	N	4K	0x0000 2000
BAR3	FIFOs	32	Y	4K	0x0000 3000

NOTE: Unless otherwise specified, the remapped version of BAR2 is referred to as LocalSpace0 while the remap of BAR3 will be referred to as LocalSpace1.Register Summary

5.2 LOCALSPACE0 WRITE-ONLY REGISTERS

Table 5-3 summarizes the LocalSpace0 write-only registers (16-bit).

Table 5-3. LocalSpace0 Write-Only Registers

Register Group	Register Name	Offset Address
Configuration Group	Interrupt Enable Register	0x00
	Hardware Configuration Register	0x02
	Memory Size Register	0x04
ADC Register Group	ATRIG LOW Register	0x0C
	ATRIG HIGH register	0x0E
	Control Register 0	0x10
	Control Register 1	0x12
	Sample Interval Register (LOW)	0x16
	Sample Interval Register (HIGH)	0x18
	Sample/Scan Count Register (LOW)	0x1E
	Sample/Scan Count Register (HIGH)	0x20
	DAQ Soft Start Command	0x22
	DAQ Single Conversion Command	0x24
	ADC FIFO pointer clear command	0x2A
DAC Register Group	DAC Control Register 1	0x52
	DAC0 Single Conversion Command (LSB)	0x70
	DAC0 Single Conversion Command (MSB)	0x72
	DAC1 Single Conversion Command (LSB)	0x74
	DAC1 Single Conversion Command (MSB)	0x76

5.3 LOCALSPACE0 READ-ONLY REGISTERS

Table 5-4 summarizes the LocalSpace0 read-only registers (16-bit).

Table 5-4. LocalSpace0 Read-Only Registers

Register Name	Offset Address
Hardware Status Register	0x00
ADC Read Pointer Register	0x08
ADC Write Pointer Register	0x0C
User XFER Counter Register (LOW)	0x10
Pre/Post Register	0x14
User Chip Select 1	0x48:4E

5.4 LOCALSPACE0 READ/WRITE REGISTERS

Table 5-5 summarizes the LocalSpace0 read/write registers (16-bit):

Table 5-5. LocalSpace0 Read/Write Registers

Register Group	Register Name	Offset Address
Primary Digital I/O (8255)	Digital Port A	0x48
	Digital Port B	0x4A
	Digital Port C	0x4C
	Digital Port Control	0x4E

5.4.1 LocalSpace0 Read/Write Registers

Table 5-6 identifies the LocalSpace0 read/write register (32-bit):

Table 5-6. LocalSpace0 Read/Write Register

Register Name	Offset Address
ADC XFIFO	0x200

5.4.2 LocalSpace0 Serial Devices

Table 5-7 summarizes the LocalSpace0 write-only serial devices:

Table 5-7. LocalSpace0 Write-Only Serial Devices

I2C Device	Address
I2C Register	0x40
CAL DAC0	0x18
CAL DAC1	0x1A

5.4.3 Register Descriptions – Detailed

This section provides detailed descriptions of all LocalSpace0 registers. Note that the DAQ refers to *analog-input* data acquisition while DAC refers to *analog output* operations. Bit locations that are hard-coded with either (0) or a (1) must be written with these values during register accesses.

5.4.4 LocalSpace0 Write-only Registers

Configuration Group

Interrupt Enable Register

15	14	13	12	11	10	9	8
OVERRUN					DAQ_STOP	DAQ_ACTIVE	XINT

MSB

7	6	5	4	3	2	1	0
				DAQDONE	DAQ_IENB	0	DAQ_ISRC0

LSB

Bit	Name	Description
15	OVERRUN	DAQ Overrun Enable – If this bit is set, a DAQ overrun condition can be detected. DAQ overrun does not cause an interrupt but does set a bit in the Status register.
10	DAQ_STOP	DAQ STOP Interrupt Enable – If this bit is set, an interrupt is generated when the stop trigger (TRIG2) is detected.
9	DAQ_ACTIVE	DAQ ACTIVE Interrupt Enable – If this bit is set, an interrupt is generated when a DAQ sequence is active.
8	XINT	XINT Interrupt Enable – If this bit is set, the external XINT signal can generate an interrupt.
3	DAQDONE	DAQDONE Interrupt Enable – If this bit is set, an interrupt is generated when the DAQ sequence completes. A DAQ sequence ends by running its course or when an OVERRUN condition occurs.
2	DAQ_IENB	DAQ Interrupt Enable – If this bit is set, one of the DAQ_ISRC conditions generates an interrupt.
0	DAQ_ISRC0	DAQ Interrupt Source select – This bit is used to select an additional DAQ interrupt source, in addition to the DAQDONE source.

DAQ_ISRC0	Description
0	DAQ FIFO ¼ Full
1	DAQ Single Conversion: An interrupt is generated each conversion. Single Conversion Command: An interrupt can be generated for each ADC conversion when the corresponding ADC data is available in the AFIFO. Paced Conversions: An interrupt can be generated each ADC conversion during paced conversions when the corresponding ADC data is available in the AFIFO. The following restrictions apply to this mode: 1. For single-channel paced conversions, place the STC in 2-Channel mode via DAQ Control 1 register. 2. Set the DSBL_DMA bit via the DAQ Control 0 register. 3. After the interrupt has been received, issue an ADC FIFO pointer clear command to permit data to be retrieved form the FIFO.

Hardware Configuration Register

15	14	13	12	11	10	9	8
							XINT_POL

MSB

7	6	5	4	3	2	1	0
0	0	0	0	0	0	WCLK_SRC1	WCLK_SRC0

LSB

Bit	Name	Description
8	XINT_POL	External Interrupt (XINT) polarity select: 0 = rising edge sensitive; 1 = falling edge sensitive.
1-0	WCLK_SRC(1:0)	PACER Base Clock Source:

WCLK_SRC1	WCLK_SRC0	Description
0	0	Inactive
0	1	On Card 40MHz oscillator
1	0	Analog Clock
1	1	Digital TRIG1 pin

Memory Size Register

15	14	13	12	11	10	9	8

7	6	5	4	3	2	1	0
	ASEG6	ASEG5	ASEG4	ASEG3	ASEG2	ASEG1	ASEG0
							LSB

Bit	Name	Description
6-0	ASEG(6:0)	ADC buffer segment size (FIFO size): The FIFO size can range from 256 samples deep upward to 32K samples deep, in increments of 256 samples. Note that the FIFO is actually 24 bits wide; therefore, two samples can be stored per FIFO location.

ASEG(6:0)	FIFO size	In sample
7F	256	512
7E	512	1K
7C	1K	2K
78	2K	4K
70	4K	8K
60	8K	16K
40	16K	32K
00	32K	64K

Note: There are actually two FIFO banks (X and Y) populated on the board. Each bank can provide 64K samples. In Burst mode the total FIFO size maximum is 2 x 64K = 128K samples.

DAQ ATRIG LOW Register

15	14	13	12	11	10	9	8
XAGATE_SRC	XTRIG2_SRC	XTRIG1_SRC		THRESH_L11	THRESH_L10	THRESH_L9	THRESH_L8

MSB

7	6	5	4	3	2	1	0
THRESH_L7	THRESH_L6	THRESH_L5	THRESH_L4	THRESH_L3	THRESH_L2	THRESH_L1	THRESH_L0

LSB

15	XTRIG1_SRC	External TRIG1 Source select: 0 = TRIG1 pin; 1 = BNC source. The External XTRIG1 Mode bit in the DAQ Control Register 0 must be set for this bit to be used.
14	XTRIG2_SRC	External TRIG2 Source select: 0 = TRIG2 pin; 1 = BNC source. The External XTRIG1 Mode bit in the DAQ Control Register 0 must be set for this bit to be used.
13	XAGATE_SRC	External AGATE Source select: 0 = AGATE pin; 1 = BNC source
12-2	THRESH_L(11:0)	Threshold Low Value: This register is used to load the LOW threshold value for Analog triggering.

DAQ ATRIG HIGH Register

15	14	13	12	11	10	9	8
				THRESH_H11	THRESH_H10	THRESH_H9	THRESH_H8

MSB

7	6	5	4	3	2	1	0
THRESH_H7	THRESH_H6	THRESH_H5	THRESH_H4	THRESH_H3	THRESH_H2	THRESH_H1	THRESH_H0

LSB

12-2	THRESH_H(11:0)	Threshold High Value: This register is used to load the HIGH threshold value for Analog triggering.

DAQ Control Register 0

15	14	13	12	11	10	9	8
DAQ_ENB	DMA_DSBL	GATE_SEQ	SAMPCNT ENB	XCONV_POL		TRIG2_ENB	TRIG2_POL

MSB

7	6	5	4	3	2	1	0
TRIG2_SRC	TRIG1_POL	TRIG1_SRC1	TRIG1_SRC0	AGATE_POL	AGATE_LVL	AGATE_SRC1	AGATE_SRC0

LSB

Bit	Name	Description
15	DAQ_ENB	Data Acquisition Enable – This bit enables and disables a data acquisition operation. It is the master enable for DAQ operations.
14	DMA_DSBL	DMA Disable; This bit should be cleared only when the STC device is transferring data to the host via DEMAND MODE DMA. Refer to the PLX New Products catalog for DEMAND MODE DMA details.
13	GATE_SEQ	GATE ON Sequence: If this bit is set in multi-channel mode, an inactive gate will pause the data acquisition after the current scan sequence has completed. If this bit is cleared, an inactive gate pauses the data acquisition immediately.
12	SAMPCNT ENB	Sample Counter Enable. When this bit is set, the DAQ Sample counter in enabled. This bit must be set for pre/post triggered mode.
11	XCONV_POL	External A/D Convert polarity control. This bit controls the polarity of the External A/D convert input signal. If a low-to-high edge of XCONV is to be used to initiate a conversion then this bit should be cleared. If a high-to-low edge of XCONV is to be used to initiate a conversion then this bit should be set.
9	TRIG2_ENB	TRIG2 pre-trigger Enable. This bit enables pre-trigger mode.
8	TRIG2_POL	TRIG2 trigger polarity select: 0 = rising edge trigger; 1 = falling edge trigger.
7	TRIG2_SRC	TRIG2 pre-trigger source select: 0 = External X_TRIG2 pin; 1 = Analog Trigger.
6	TRIG1_POL	TRIG1 trigger polarity select: 0 = rising edge trigger; 1 = falling edge trigger.
5-4	TRIG1_SRC(1:0)	TRIG1 Source select – These bits are used to select TRIG1 source.

TRIG1_SRC1	TRIG1_SRC0	DESCRIPTION
0	0	Disabled
0	1	Soft_Trigger
1	0	External XTRIG1
1	1	Analog Trigger

3	AGATE_POL	AGATE polarity select: 0 = active high gate; 1 = active low gate.
2	AGATE_LVL	AGATE Level select; 0 = edge sensitive gate; 1 = level sensitive gate;
1-0	AGATE_SRC(1:0)	AGATE Source select – These bits are used to select AGATE source.

AGATE_SRC1	AGATE_SRC0	DESCRIPTION
0	0	Disabled
0	1	Soft_Gate
1	0	External AGATE
1	1	Analog Gate

DAQ Control Register 1

15	14	13	12	11	10	9	8
PSC_ENB		CHANMODE1	CHANMODE0	HCHANSEL1	HCHANSEL0	LCHANSEL1	LCHANSEL0

MSB

7	6	5	4	3	2	1	0
0	SFT_AGATE	ATRIGSRC1	ATRIGSRC0	ATRIGMD2	ATRIGMD1	ATRIGMD0	

LSB

Bit	Name	Description
15	PSC_ENB	Pre-Scale Enable bit. If this bit is set then the WCLK is prescaled by 400. If the WCLK Source is 40 MHz then the Pacer clock source is 40 MHZ/400 = 100 kHz.
13-12	CHANMODE(3:0)	Channel MODE select bits.

CHANMODE1	**CHANMODE0**	**MODE**	**Comments**
0	0	Single Channel	20MHZ max. sample rate
0	1	Two Channels	20MHZ max. sample rate
1	0	Four Channels	10MHZ max. sample rate
1	1	Four Channel Transient	20MHZ max. sample rate; single burst of 32K samples max per channel.

11-10	UCHANSEL(1:0)	High Channel select bits. These bits are used to select the high channel in Two-Channel mode.

HCHANSEL1	**HCHANSEL0**	**Selected Channel**
0	0	Channel A
0	1	Channel B
1	0	Channel C
1	1	Channel D

9-8	LCHANSEL(1:0)	Low Channel select bits. These bits select the low channel in Two Channel mode.

LCHANSEL1	**LCHANSEL0**	**Selected Channel**
0	0	Channel A
0	1	Channel B
1	0	Channel C
1	1	Channel D

6	SFT_GATE	Software DAQ Gate - When SFT_GATE is cleared, no A/D conversions take place. When SFT_GATE is set, A/D conversions take place normally. SFT_GATE can be used as a software gating tool, or to inhibit random conversions during setup operations.

5-4	ATRIGSRC(1:0)	Analog Trigger Channel Source

ATRIGSRC1	**ATRIGSRC0**	**Selected Channel**
0	0	Channel A
0	1	Channel B
1	0	Channel C
1	1	Channel D

3-1	ATRIGMD(2:0)	Analog Trigger/Gate Mode select bits.

Analog Trigger/Gate Modes

ATRIGMD2	ATRIGMD1	ATRIGMD0	Mode	Description
0	0	0	INACTIVE	Inactive state. Prior to programming the analog trigger to the desired state, the analog trigger should be programmed to the inactive state to clear out the trigger circuitry.
0	1	0	Positive Hysteresis	The trigger is generated when the signal value is greater than the high-value, with hysteresis specified by low_value.
0	1	1	Negative Hysteresis	The trigger is generated when the signal value is greater than the low-value, with hysteresis specified by high_value.
1	0	0	Negative Slope	The trigger is generated when the signal value is less than low-value.
1	0	1	Positive Slope	The trigger is generated when the signal value is greater than high-value.
1	1	0	Window	The trigger is generated when the signal value is between the low-value and high-value.

ADC Sample Interval Register (Lower)

15	14	13	12	11	10	9	8
ADCSIL15	ADCSIL14	ADCSIL13	ADCSIL12	ADCSIL11	ADCSIL10	ADCSIL9	ADCSIL8

MSB

7	6	5	4	3	2	1	0
ADCSIL7	ADCSIL6	ADCSIL5	ADCSIL4	ADCSIL3	ADCSIL2	ADCSIL1	ADCSIL0

LSB

Bit	Name	Description
15-0	ADCSIL(15:0)	ADC Sample Interval Lower - The lower 16 bits of the Sample Interval divisor.

ADC Sample Interval Register (Upper)

15	14	13	12	11	10	9	8

MSB

7	6	5	4	3	2	1	0
ADCSIL23	ADCSIL22	ADCSIL21	ADCSIL20	ADCSIL19	ADCSIL18	ADCSIL17	ADCSIL16

LSB

BIT	**Name**	**Description**
15-0	ADCSIL(23:16)	ADC Sample Interval upper - The upper 8 bits of the Sample Interval divisor.

ADC Pacer Frequency = Base_clock/(Divider + 2)

ADC Sample/Scan Count Register (Lower)

15	14	13	12	11	10	9	8
ADCSMP15	ADCSMP14	ADCSMP13	ADCSMP12	ADCSMP11	ADCSMP10	ADCSMP9	ADCSMP8

MSB

7	6	5	4	3	2	1	0
ADCSMP7	ADCSMP6	ADCSMP5	ADCSMP4	ADCSMP3	ADCSMP2	ADCSMP1	ADCSMP0

Bit	Name	Description
15-0	ADCSMP(15:0)	ADC Sample Count lower - The lower 16 bits of the Sample Counter.

Note: The sample counter must always be loaded with a non-zero value prior to enabling a DAQ sequence. This holds true even when the sample counter is disabled via the SAMPCNT_ENB bit in the DAQ Control 0 register.

ADC Sample/Scan Count Register (Upper)

15	14	13	12	11	10	9	8

MSB

7	6	5	4	3	2	1	0
ADCSMP23	ADCSMP22	ADCSMP21	ADCSMP20	ADCSMP19	ADCSMP18	ADCSMP17	ADCSMP16

LSB

Bit	Name	Description
15-0	ADCSMP(23:16)	ADC Sample Count upper - The upper 8 bits of the Sample Counter.

DAQ Start Register

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

MSB

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

LSB

Bit	Name	Description
15-0	Don’t care	

Accessing the DAQ Start Register location initiates a multiple A/D conversion data acquisition operation.

To trigger the board with the Start DAQ register, the TRIG1_SRC(1:0) bits need to select the soft-trigger source. Otherwise, strobing the Start DAQ register has no effect.

DAQ Single Conversion Register

15	14	13	12	11	10	9	8
X	X	X	X	X	X	CHANSEL1	CHANSEL0

MSB

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

LSB

Bit	**Name**	**Description**
9-9	CHANSEL(1:0)	These bits select the desired channel to be acquired during the Single Conversion command. “00” = Chan. A; “01” = Chan. B; “10” = Chan. C; “11” = Chan. D.

Prior to issuing a DAQ Single Conversion command, access the Attenuation register and select the desired gain. Note also that since the ADC converters are pipelined, the Sample Interval register must be programmed with the desired pacer rate prior to issuing this command. Accessing the Single Conversion Register location initiates a single A/D conversion. Retrieve the actual ADC value by reading the FIFO.

ADC Buffer Pointer Clear Register

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

MSB

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

LSB

Bit	Name	Description
15-0	Don't care	

Accessing the ADC buffer pointer clear register resets the pointer to home state and clears the internal STC pipeline registers (PIPE2, PIPE1, and PIPE0).

DAC Control Register 1

15	14	13	12	11	10	9	8

MSB

7	6	5	4	3	2	1	0
DAC_OE					DAC1R0		DAC0R0

LSB

Bit	Name	Description
7	DAC_OE	DAC Output Enable -
2	DAC1R0	These bits configure the range of DAC1 in the analog output section. 0 = bipolar +/-10V; 1 = bipolar +/-5V.
0	DAC0R0	These bits configure the range of DAC0 in the analog output section. 0 = bipolar +/-10V; 1 = bipolar +/-5V.

DAC0 Single Conversion Registers (LSB)

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

MSB

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

LSB

Bit	Name	Description
7-0	Lower DAC byte	The lower 8-bits of DAC0.

DAC0 Single Conversion Registers (upper nibble)

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

MSB

7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8

LSB

Bit	Name	Description
3-0	Upper DAC nibble	The upper 4-bits of DAC0.

Note: DAC0 is up-dated after the upper nibble has been loaded. Thus, to program DAC0 correctly, load the lower byte first, then the upper nibble.

DAC1 Single Conversion Registers (LSB)

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

MSB

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

LSB

Bit	Name	Description
7-0	Lower DAC byte	The lower 8-bits of DAC1.

DAC1 Single Conversion Registers (upper nibble)

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

MSB

7	6	5	4	3	2	1	0
X	X	X	X	D11	D10	D9	D8

LSB

Bit	Name	Description
3-0	Upper DAC nibble	The upper 4-bits of DAC1.

Note: DAC0 is updated after the upper nibble has been loaded. To program DAC1 correctly, load the lower byte first, then the upper nibble.

Hardware Status Register

15	14	13	12	11	10	9	8
REV2	REV1	REV0	NEXT_CHAN	PIPEFULL1	PIPEFULL0	TRIG2_FLG	XINT_FLG

MSB

7	6	5	4	3	2	1	0
DAQDONE	0	ASRC_FLG	0	DAQ_ACTIVE	0	DAQ_OVERRUN	0

LSB

Bit	Name	Description
15-13	REV(2:0)	REV Control Field: Currently = 001'b.
12	NEXT_CHAN	NEXT_CHAN status. This bit is used to determine if an odd or even sample was the last loaded into FIFO memory. If this bit is 0, the DAQ operation ended on an even boundary. If this bit is 1, the DAQ operation ended on an odd boundary.
11-10	PIPEFULL(1:0)	STC PIPE FULL status: The STC contains three internal pipe line registers in the DAQ data path. At the completion of a DAQ operation, these pipeline registers may contain residual ADC data. The PIPEFULL(1:0) bits provides status on which pipe register contains valid data.
9	TRIG2_FLG	If this bit is set, a DAQ stop trigger interrupt is pending.
8	XINT_FLG	If this bit is set, an external interrupt is pending.
7	DAQDONE	If this bit is set, the current DAQ operation is complete. If the DAQDONE interrupt was enabled, it is pending.
5	ASRC_FLG	If this bit is set, one of the DAQ interrupt sources (DAQ_ISRC(1:0) field in the Interrupt Enable Register) is pending. This bit can also be polled to determine the ADC_BUSY status after a Single Covert Command has been issued.

3	DAQ_ACTIVE	If this bit is set, the current DAQ operation is active.
1	DAQ_OVERRUN	If this bit is set, an overrun error was detected during the previous DAQ operation.

All pending interrupts sourced by the STCs interrupt control logic are serviced by reading the Hardware Status Register.

ADC Read Pointer Register

15	14	13	12	11	10	9	8
0	ARPNTR14	ARPNTR13	ARPNTR12	ARPNTR11	ARPNTR10	ARPNTR9	ARPNTR8

MSB

7	6	5	4	3	2	1	0
ARPNTR7	ARPNTR6	ARPNTR5	ARPNTR4	ARPNTR3	ARPNTR2	ARPNTR1	ARPNTR0

LSB

Bit	Name	Description
14-0	ARPNTR(14:0)	The Lower ADC Read pointer data. The overall ADC Read pointer is a 17-bit address. This register provides the lower 15-bits. Reference the Upper User Transfer Counter for the remaining upper two bits.

ADC Write Pointer Register

15	14	13	12	11	10	9	8
0	AWPNTR14	AWPNTR13	AWPNTR12	AWPNTR11	AWPNTR10	AWPNTR9	AWPNTR8

MSB

7	6	5	4	3	2	1	0
AWPNTR7	AWPNTR6	AWPNTR5	AWPNTR4	AWPNTR3	AWPNTR2	AWPNTR1	AWPNTR0

LSB

Bit	Name	Description
14-0	AWPNTR(14:0)	The Lower ADC Write pointer data. The overall ADC Write pointer is a 17-bit address. This register provides the lower 15-bits. Reference the Upper User Transfer Counter for the remaining upper two bits.

Lower User Transfer Counter Register

15	14	13	12	11	10	9	8
XFERCNT15	XFERCNT14	XFERCNT13	XFERCNT12	XFERCNT11	XFERCNT10	XFERCNT9	XFERCNT8

MSB

7	6	5	4	3	2	1	0
XFERCNT7	XFERCNT6	XFERCNT5	XFERCNT4	XFERCNT3	XFERCNT2	XFERCNT1	XFERCNT0

LSB

Bit	Name	Description
15-0	XFERCNT(15:0)	Lower User Transfer counter data. The overall User Transfer Counter is a 24-bit address. This register provides the lower 16-bits. Reference the Upper User Transfer Counter for the remaining upper 8-bits.

Pre-Post Register

15	14	13	12	11	10	9	8
	0	0	0	0	0	0	0

MSB

7	6	5	4	3	2	1	0

CHAIN_FLG1	CHAIN_FLG2	0	0	0	0	0	0

LSB

7-6 CHAIN_FLG(1:0) Chain Flag bits. These bits help determine what scatter-gather chain entry data was last DMA transferred to. These bits can be compared to the LAD(4:3) bits programmed in the DMA Channel Local Address register to guarantee that the correct final chain entry has been located.

5.4.5 I2C INTERFACE:

The analog front-end and calibration circuitry is controlled by a 2-wire I2C interface. The following three I2C-compatible devices reside on the I2C:

1. I2C Register
2. Channel 0 and 1 Calibration DACs.
3. Channel 2 and 3 Calibration DAQs.

Each of these devices have a unique I2C address.

I2C REGISTER

Address Byte

MSB

7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0

LSB

DATA BYTE

MSB

7	6	5	4	3	2	1	0
THRESH_SEL	1	CSRC_SEL1	CSRC_SEL0	AD3ATTEN	AD2ATTEN	AD1ATTEN	AD0ATTEN

LSB

Bit	Name	Description
7	THRESH_SEL	BNC Threshold Select: 0 = TTL input (2.5V threshold). 1 = +/- 5V Bipolar input (0V threshold).
6-4	ADCSIG_SEL(1:0)	ADC Signal source select.

ADCSIG_SEL1	**ADCSIG_SEL0**	**Selected Channel**
0	0	BNC Input
0	1	Calibration SRC = 4.375V
1	0	Calibration SRC = 0.625V

3	AD3ATTEN	Channel D Attenuation Select: 0 = Gain of 1; 1 = Attenuation of 5.
2	AD2ATTEN	Channel C Attenuation Select: 0 = Gain of 1; 1 = Attenuation of 5.
1	AD1ATTEN	Channel B Attenuation Select: 0 = Gain of 1; 1 = Attenuation of 5.
0	AD0ATTEN	Channel A Attenuation Select: 0 = Gain of 1; 1 = Attenuation of 5.

Note: The I2C register reset with all of the bits in the high state.

I2C DAC0

Address Byte

MSB

7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	0

LSB

Pointer Byte

MSB

7	6	5	4	3	2	1	0
0	0	0	0	OFFSET1	GAIN1	OFFSET0	GAIN0

LSB

MSB Data Byte

MSB

7	6	5	4	3	2	1	0
0	0	1	0	D9	D8	D7	D8

LSB

LSB Data Byte

MSB

7	6	5	4	3	2	1	0
D5	D4	D3	D2	D1	D0	0	0

LSB

I2C DAC1

Address Byte

MSB

7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	0

LSB

Pointer Byte

MSB

7	6	5	4	3	2	1	0
0	0	0	0	OFFSET3	GAIN3	OFFSET2	GAIN2

LSB

MSB Data Byte

MSB

7	6	5	4	3	2	1	0
0	0	1	0	D9	D8	D7	D8

LSB

LSB Data Byte

MSB

7	6	5	4	3	2	1	0
D5	D4	D3	D2	D1	D0	0	0

LSB

6. INITIATING A/D CONVERSIONS

6.1 DEFINITIONS AND IMPLEMENTATION

Convert Clock: – Buffered continuous clock signal that generates ADC conversions.
Start Convert: – Command which initiates A-STC to start transferring data from ADC's to SRAM.
Trigger: – Initiates the Start Convert process (single conversion or scan of conversions).
Gate: – Masks off scans in a data acquisition sequence.

Figure 6-1 shows the various ways to initiate the executions of A/D conversion.
The description and methods for implementing Start Convert Sources, Trigger Methods, and Gating Methods are defined in Figure 6-1 below.

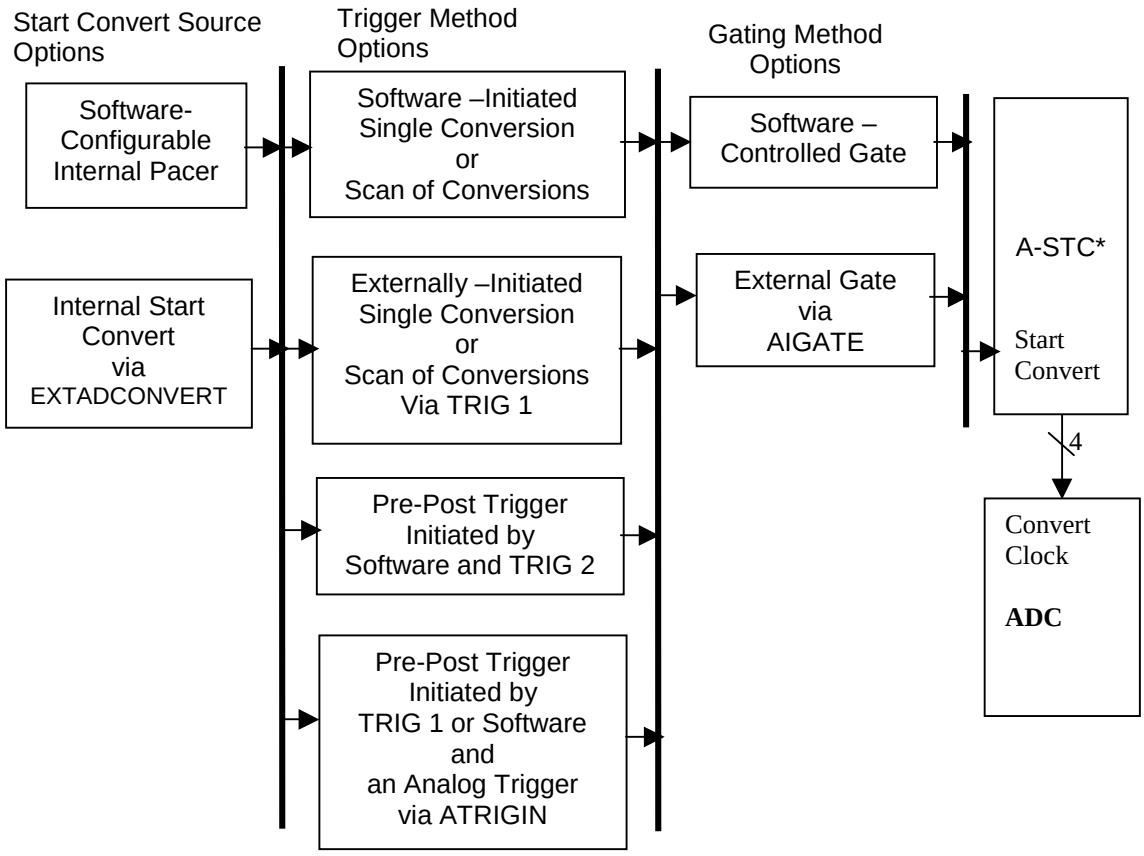


Figure 6-1. Initiating A/D Conversions

6.2 INITIATING CONVERSION VIA THE BNC CONNECTION: RELATED PIN DESCRIPTIONS

*NOTE: These functions share the same input BNC connection. Therefore, they are mutually exclusive. The BNC input can be configured for two different threshold settings, 2.5V threshold (TTL), or 0V threshold (+/-5V). See the I2C register for more details.

EXTBNCCLK	This BNC input signal generates start convert commands for the A-STC (System Timing Chip). It is software-configurable to be active on a rising or falling edge.
TRIG1	This BNC input signal triggers a scan (single) conversion. It is software-configurable to be active on a rising or falling edge. When used in Pre-/Post-Triggering applications, TRIG1 initiates the Pre-Triggers.
TRIG2	The BNC input signal is used in Pre-/Post-Triggering applications. TRIG2 initiates the Post-Triggers. It is software-configurable to be active on rising or falling edges.
AIGATE	The BNC input signal generates start convert commands for the A-STC. AIGATE masks off scans in a data acquisition sequence. It is software-configurable to be active HI or LO, or on a rising or falling edge.

6.3 INITIATING CONVERSION VIA ANALOG INPUT BNC CONNECTIONS:

ATRIGIN	Any of the four input channels can be used as an analog input trigger. They are software-configurable to trigger above or below a reference level (with or without hysteresis) or to trigger in or out of a reference window.

7. CALIBRATION

The PCI_DAS4020/12 provides self-calibration of the analog inputs, eliminating the need for external equipment and user adjustments. All adjustments are made via 10-bit calibration DACs that are referenced to the on-board factory calibrated standard. Each channel has a pair of dedicated 10-bit DACs used to trim out offset and gain errors. Offset calibration is performed by adjusting the offset voltage at the input of each ADC. Gain adjustment is performed via the ADC reference pin.

The board is fully calibrated at the factory with calibration coefficients stored in nvRAM. At run time, these calibration factors are loaded into system memory and are automatically retrieved each time a different ADC range is specified.

7.1 CALIBRATING THE PCI-DAC4020/12

The user can recalibrate any time using factory voltage standards by selecting the *"Calibrate"* option in *Insat*Cal. Simply launch *Insta*Cal, and select the "*Calibrate*" option. A full calibration typically requires less than two minutes. We strongly recommend that you turn your computer on, and allow at least 30 minutes for the internal case temperature to stabilize prior to calibrating the board.

8. SPECIFICATIONS

Typical for 25°C unless otherwise specified.

Analog Inputs

A/D converter type	AD9225, 25 Msps pipelined A/D
Resolution	12 bits
Programmable ranges	±5V, ±1V
Number of channels	4 single-ended, independent ADC's per channel
Connection	4 independent BNC
Coupling	DC

A/D Pacer (Conversion Clock) — Programmable: Internal counter, External source or software polled

A/D Auxiliary BNC — Software selectable for External Analog/Digital Trigger or gate; also used as an external data acquisition clock source.

External Analog Trigger -	EXTATRIG
Input Impedance	2.5 kilohms or 50 Ohms selectable (Coaxial termination)
Input Range	±5V
Bandwidth	40 MHz
Coupling	DC

External Digital Control

Function Select	Software programmable for External Pacer, External Trigger, or External Gate
External Pacer Mode -	EXTADCONVERT
Pacer Clock Rate	40 MHz max, 1 kHz min
Duty Cycle	50% ± 5%
External Trigger Mode	
Trigger Mode Select	Software programmable for TRIG1 or TRIG2
External Gate Mode -	AIGATE
Input impedance	50 ohms, 1Mohm selectable (Coaxial cable termination)
Input configuration	TTL (2.5V threshold) or +/-5V bipolar (0V threshold) with hysteresis

Simultaneous Sampling — Software selectable option - 1, 2, or 4 channels

A/D Trigger Sources — Internal software, External Analog or Digital

A/D Triggering Modes:

Internal Software:
Software trigger to begin a scan of conversions
Software convert to initiate single conversion

External digital:
Software configurable for rising or falling edge to initiate single conversion via TRIG1.

External analog:
Software selectable source for analog trigger: EXTATRIG or any of the four Analog Input channels.
Resolution: 12-bit, uncalibrated DACs

Hysteresis: Programmable
Levels: Software configurable for above/below reference levels and in/out of window

Pre- / Post-trigger:
Circular buffer allows unlimited pre-trigger conversions.
16 MB post-trigger conversion capability.
Data acquisition sequence initiated via Software, TRIG1 analog trigger (if not used for Post-triggering phase). For software initiated pre-trigger only, post-triggered phase initiated by TRIG2 or analog trigger (if not used for data acquisition initiation).

A/D Gating Modes

Internal Software:
Software gate to mask off scans in a data acquisition sequence. Available for all trigger modes.
External digital*:*
Software configurable for active HI or active LO external gating to mask off scans in a data acquisition sequence via AIGATE. Available for Internal Software trigger mode only.

Data transfer

Via dual 32Kx24 sample FIFO, SRAM based, with Bus-Master DMA and scatter-gather, interrupt, or software polled.

A/D conversion time	40 ns
Throughput	20 MHz max, 1 kHz min
Single Channel, single input gain	20 MHz continuous
Two Channels (0 and 1 or 2 and 3)	20 MHz continuous
Multiple Channels	10 MHz continuous, 20 MHz for 32k samples (one FIFO size)
Differential Linearity error	±0.4 LSB typ, ±1.0 LSB max
Integral Linearity error	±1.0 LSB typ, ±2.5 LSB max
No missing codes guaranteed	12 bits
Gain drift (A/D specs)	±0.4 ppm/°C + AD780 Reference: ±3 ppm/°C max
Zero drift (A/D specs)	±2 ppm/°C
Common Mode Range	±10 V
CMRR @ 60Hz	90 dB
Input leakage current	2 uA typ, 10 uA max
Input impedance	15 Mohms typ, or 50 ohms, selectable (coaxial cable termination)
Absolute maximum input voltage	±15V

SNR (Signal-to-noise Ratio)	66.6 dB
SINAD (Signal-to-noise and distortion Ratio)	66.5 dB
SFDR (Spurious Free Dynamic Range)	80 dB
THD (Total Harmonic Distortion)	80 dB

Analog Outputs

D/A converter type	AD7237
Resolution	12 bits
Number of channels	2
Output Range	±10V, ±5 software selectable
D/A pacing	Software paced
D/A trigger modes	Software gate.
Data transfer	Programmed I/O
Offset error	±9mV max (not calibrated)
Gain error	±2LSB max (not calibrated)
Differential nonlinearity	±1LSB max
Integral nonlinearity	±1LSB max
Monotonicity	Guaranteed monotonic over temperature
D/A Gain drift	±15 ppm/°C max
D/A Bipolar offset drift	±5 ppm/°C max
Throughput	System Dependent
Settling time (20V step to ±½LSB)	5µs max
Slew Rate	7V/µs
Current Drive	±5 mA
Output short-circuit duration	25 mA indefinite
Output coupling	DC
Output impedance	0.5 Ohms max
Miscellaneous	Single buffered output latch Update DACs individually On power-up and reset, both DACs are cleared to 0 volts

Digital Input / Output

Digital Type (40-pin connector)	8255A
Configuration	2 banks of 8, 2 banks of 4, programmable by bank as input or output
Number of channels	24 I/O
Output High	3.0 volts min @ 2.5mA
Output Low	0.4 volts max @ 2.5 mA
Input High	2.0 volts min, Vcc+0.5 volts absolute max
Input Low	0.8 volts max, GND −0.5 volts absolute min
Power-up / reset state	Input mode (high impedance)

Interrupts	INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Software programmable, External enable
Interrupt sources	External, internal FIFO status sources

Crystal oscillator	
Frequency	40MHz
Frequency accuracy	50% duty cycle, 50ppm

Environmental

Operating temperature range	0 to 70 °C
Storage temperature range	−40 to 100 °C
Humidity	0 to 90% non-condensing

Power consumption

+5V Operating (A/D converting to FIFO)	1.5A typical, 2.0A max

For your notes.

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EC Declaration of Conformity

We, ComputerBoards, Inc., declare under sole responsibility that the product:

Part Number	Description
PCI-DAS4020/12	**High speed analog and digital I/O board for PCI bus**

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other informative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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